Self-Interference and Cross-Interference Cancellation for 2x2 MIMO In-Band Full Duplex Radios

PROJECT REPORT

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2022

CERTIFICATE

This is to certify that this thesis (or project report) entitled ***"Self-Interference and Cross-Interference Cancellation for 2x2 MIMO In-Band Full Duplex Radios"*** submitted by **DEEPANSHU AGGARWAL** to the Indian Institute of Technology Madras, for the award of the degree of **Masters of Technology** is a bona fide record of the research work done by him under my supervision. The contents of this thesis (or project report), in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma..

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I would like to extend my appreciation to all my friends and for their help and support in completing my project successfully.

Abstract

Traditional Full duplex system uses different frequencies for transmission and reception but In-band Full duplex systems uses single frequency. Due to this a portion of the transmitted signal comes in received signal path and this interference is called self-interference. In MIMO a portion of the transmitted signal from other antennas also comes in received signal path and this interference is called cross interference. These interferers powers are very large as compare to power of intended received signal, that's why there power should be reduced below the noise floor so that the desired received signal can be detected effectively.

In this thesis, a RF self-interference cancellation and cross interference cancellation technique is presented. For an OFDM signal of bandwidth 100 MHz and peak power of 52.5 dBm, proposed technique acheives a 22.65 dB of self-interference cancellation and 26.3 dB of cross-interference cancellation in simulations.

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ABBREVIATIONS

ADS	Advanced Design System
CI	Cross-Interference
CIC	Cross-Interference Cancellation
HRPS	High Resolution Variable Phase Shifter
HRVA	High Resolution Variable Attenuator
IBFD	In-band Full Duplex
RI	Residual Interferer
RSIS	Residual Self-Interference Signal
SI	Self-Interference
SI	Self-Interference Cancellation
SS	Spectral Shaper

Chapter 1

Introduction

1.1 Introduction to In-band Full Duplex Radios

IBFD radios transmit and receive at same time and at same frequency. Theoretically it doubles the throughput but SI is main impediment in implementation of these systems as much stronger SI signal completely drowns the intended received signal and saturate the receiver chain. SI signal power should be reduced down to receiver noise floor so that received signal can be decode effectively.

1.2 Origin of Self-Interference

In receiver we receive not only intended received signal but also many copies of the transmitted signal coming through various paths. These paths arise because of the following reasons:

- Receiver and transmitter coupling at antenna due to finite isolation of a circulator.
- Transmitted signal from power amplifier leaks through substrate to receiver.
- Antenna picks up reflections of transmitted signal from surroundings.

1.3 Types of Self-Interference Cancellation

In order to achieve high SI cancellation, SI cancellation can be done at three places in a receiver chain. Three types of SI cancellation are as follows:

- **RF Cancellation:** It gives SI cancellation before LNA in a receiver chain so that SI signal does not saturate LNA of a receiver chain.
- **Baseband Analog Cancellation:** It gives additional SI cancellation in analog baseband domain before ADC so that received signal comes within dynamic range of ADC.
- **Baseband Digital Cancellation** It gives additional SI cancellation in digital domain after RF and baseband analog cancellation.

1.4 Aim and Motivation

In order to achieve a reliable communication with Full duplex, SI signal power should be reduced to noise floor. For 100 MHz OFDM signal of 41.5 dBm and noise floor -94 dBm, required SI cancellation is around 116 dB. SI cancellation is done at three different stages in receiver chain. This thesis focuses on RF SI and CI cancellation.

A two stage SI cancellation technique is proposed, which gives a 22.65 dB SI cancellation and 26.3 dB of CI cancellation. For CI cancellation, SI cancellation circuitry is replicated.

1.5 Outline of the Report

The organization of the thesis is as follows.Chapter 1 gives a brief introduction into the project. In chapter 2 presents the literature survey on the RF SI cancellation techniques. In chapter 3, a two stage SI cancellation technique is explained and its block diagram with required components is proposed. In chapter 4, design of a voltage variable phase shifter is explained. Chapter 5 presents the simulations setup and simulation results. Finally, conclusion is presented in chapter 6.

Chapter 2

Literature Survey

2.1 RF Interference Cancellation techniques

This section discusses about literature survey done regarding RF SI cancellation techniques.

2.1.1 Antenna Cancellation

In this two antenna is used for transmission and one is used for reception. Receive antennas is placed between two transmit such that there is a 180° path difference between signals coming from transmitting antenna. Thus it achieves a 30dB of antenna cancellation. After antenna cancellation, RF and digital cancellation is also applied to get 60dB SI cancellation[1].

It's main drawback is that it uses three antenna which increases form factor of the node. Performance degrades with increase in bandwidth as there is null at a

receiver only for a centre frequency. Performance also degrades with increase in transmitter power.

2.1.2 Balun Cancellation

In this balun is used to get a inverted copy of a transmitted signal. This copy is then passed through vector modulator and finally subtracted from received signal to get RF SI cancellation. For a ideal balun, it has no bandwidth and transmitted power constraints.

But practical balun response is not flat over a frequency, due to this it introduces a amplitude imbalance[2]. Balun cancellation performance degrades with increase in bandwidth. Balun cancellation has advantage over antenna cancellation as it requires only two antennas where as antenna cancellation requires three antennas. It gives better performance as bandwidth increases.

2.1.3 Taylor Approx. Based SI Canceller

SI signal contains reflected copies of transmitted signal. These copies are delayed and attenuated version of transmitted signal. Conventionally a multi tap RF filter is used to cancel these interference signal. This requires multiple delay lines, and achieving these delay lines at high frequencies is difficult. Difficult to get a small form factor RF filter. RF delay lines should be tuned, these increases complexity when we consider more numbers of taps.

In this paper a linearization technique based on taylor series approximation is presented which provides a two parameter self-interference channel model[3]. Delayed signal is approximated as linear combination of signal and it's derivative. 75 dB SI cancellation is reported for a 20 MHz signal.

2.1.4 Two-Tap RF SI Canceller

Residual spectrum shape after one tap phase based RF SI canceller is non-flat, due to this normal second tap phase based RF cancellation does not gives significant improvement in SI cancellation.

A spectral shaper is used in second RF tap to mimic the non-flat residual spectrum shape[4]. Spectral shaper is consist of a high resolution variable phase shifter and attenuator. Spectral shaper based two tap RF canceller gives a 42dB SI cancellation for 20 MHz bandwidth.

2.1.5 CI Cancellation for FD MIMO Radios

In MIMO tramit signal from each of the M transmitter act as an interference for a receiver. Interference due to TX chain with which receive chain share an antenna is called SI(self-talk) and interference due to other TX chain is called CI(cross-talk). For a $M \times M$ MIMO system if we replicate SI cancellation circuitry for CI cancellation as well then, system complexity increases exponentially as M^2 with M.

A cascaded technique is proposed in which ensures system complexity increases linearly with M. Cross-talk and self-talk transfer functions are correlated as they share a similar surrounding. Cross-talk transfer function can be implemented as a cascade of self-talk transfer function and cascade transfer function[7]. Basically, it reuses the self-talk cancellation circuitry.

2.2 Phase Shifter Design techniques

This section discusses about literature survey done regarding Phase Shifter Design techniques.

2.2.1 Varactor Based Linear Phase Shifter

Continuous phase modulator can be made by placing a varactor diode on one terminal of a circulator. Power from first port of the circulator is reflected at second port and emerges out from third port with a amplitude and phase dictated by the reflection coefficient of the diode. As the reverse bias voltage of the varactor is changed, the phase and magnitude of reflection coefficient changes.

Varactor reactance versus voltage curve is matched to tanθ curve to have a linear 180° phase modulation[5]. When two such varactors are 90° out of RF phase and connected in parallel, they provide 360° phase modulation when voltage is varied. A phase shifter has a constant insertion loss as control voltage is varied.

2.2.2 Distributed Analog Phase Shifter

A distributed analog phase shifter is designed by periodically loading coplanar-waveguide lines by varactors[6]. As reverse voltage of varactor diode changes, their capacitance also changes which in turn changes the phase velocity in these coplanar-waveguide lines, thus resulting in analog phase shift.A 0°–360° phase shifter is designed which have a maximum insertion loss (IL) of 4.2 dB at 20 GHz.

Chapter 3

Design of Variable Phase Shifter

3.1 Schematic of Phase shifter

A high resolution varactor based voltage variable phase shifter is designed. In figure 3.1 input is feed to port 1 of the hybrid 3 dB circulator and isolated port 2 is the output port.

Input power from port 1 splits into half and reach coupled ports 3 and 4. Coupled ports are loaded with a parallel combination of varactor and 90° out of RF phase varactor to get a 360 ° phase modulation. 90° RF phase shift is provided by a 100 ohm ($\lambda \div 4$) microstrip transmission line. Incoming power coming to port 3 and 4 is reflected to port 2 with a reflection magnitude and phase controlled by reverse voltage of varactor diodes. Thus with change in reverse bias voltage of varactor, the phase shifter provides variable phase shift.

A bias tee is implemented with a capacitor and an inductor. It has RF and DC as an input and gives RF+DC as output. Bias tee is used to feed the DC voltage to varactor diode.

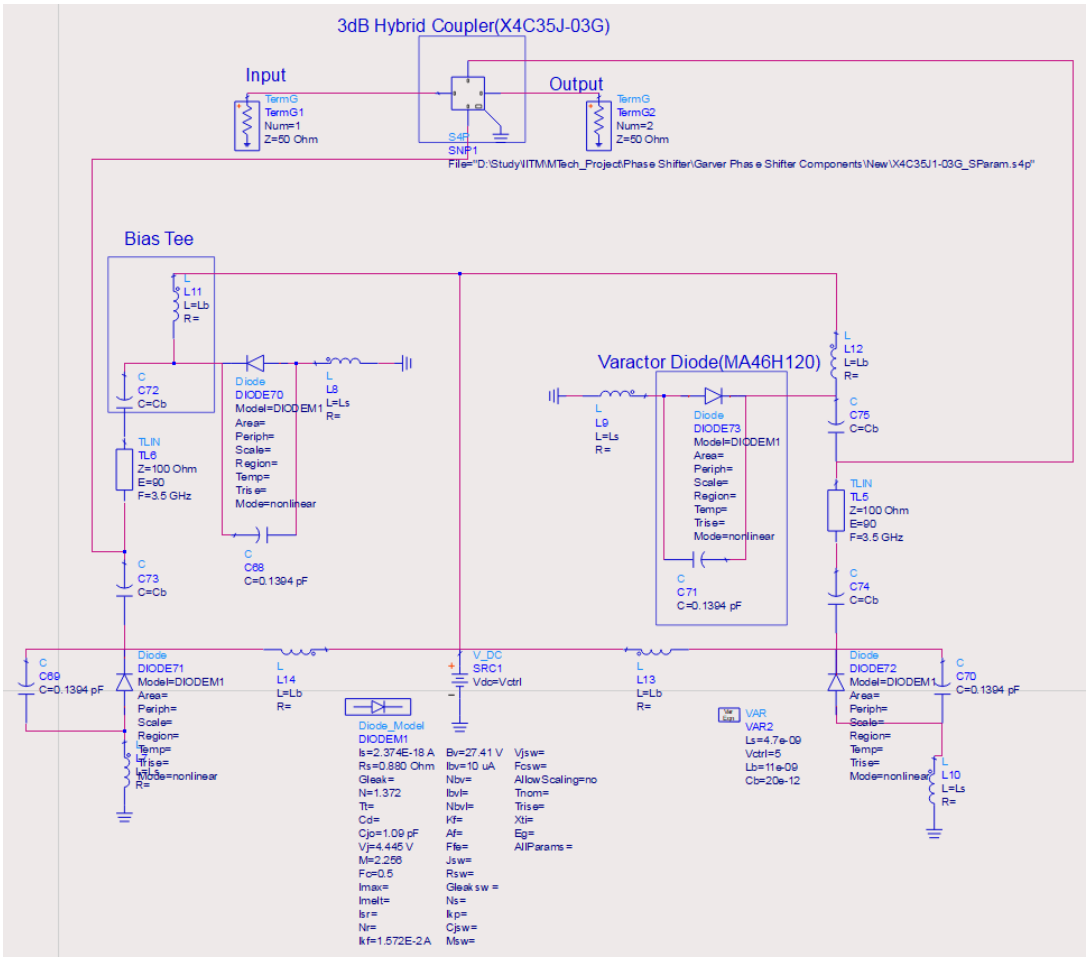


Figure 3.1: Phase shifter schematic

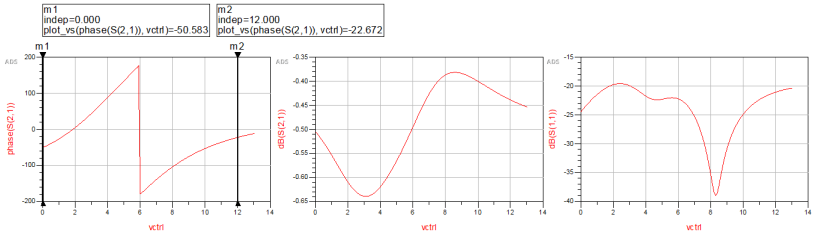


Figure 3.2: S parameters versus control voltage for phase shifter schematic

3.1.1 Simulation Results

Figure 3.2 shows phase shifter gives a complete 360° phase shift when control voltage is varied from 0 volts to 12 volts. A high resolution phase shift can be obtained by using a high resolution DC power supply. Figure 3.3 shows phase variations in a 100 MHz frequency band. Ideally, phase should be constant with respect to frequency. For achieving high cancellation phase variations should be minimum, in our design it is 32°. Phase shifter has a worst case P1dB of 19.1 dBm.

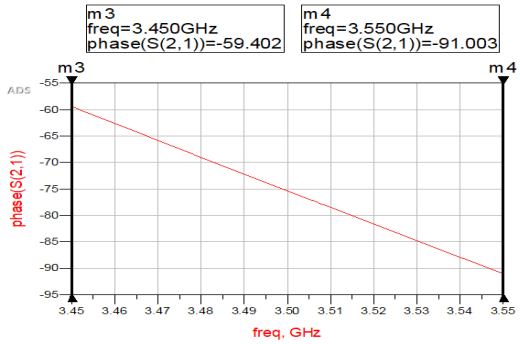


Figure 3.3: Phase shift versus frequency for phase shifter schematic

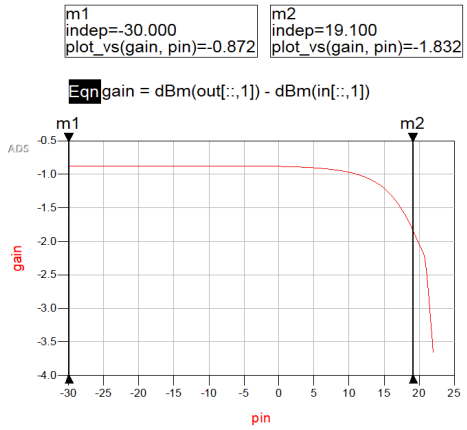


Figure 3.4: P1 dB(worst case) for phase shifter schematic

3.2 Layout of Phase Shifter

Figure 3.5 shows a two layer PCB layout of phase shifter. Refer A.1 for board stack-up information. Bottom layer conductor act as a ground plane for microstrip line. Edge SMA connector are used for input and output of RF signal. For feeding DC voltage, DC header pins are used. Foot prints of all components are done according to their specification sheets. Ground vias placed for RF return path.

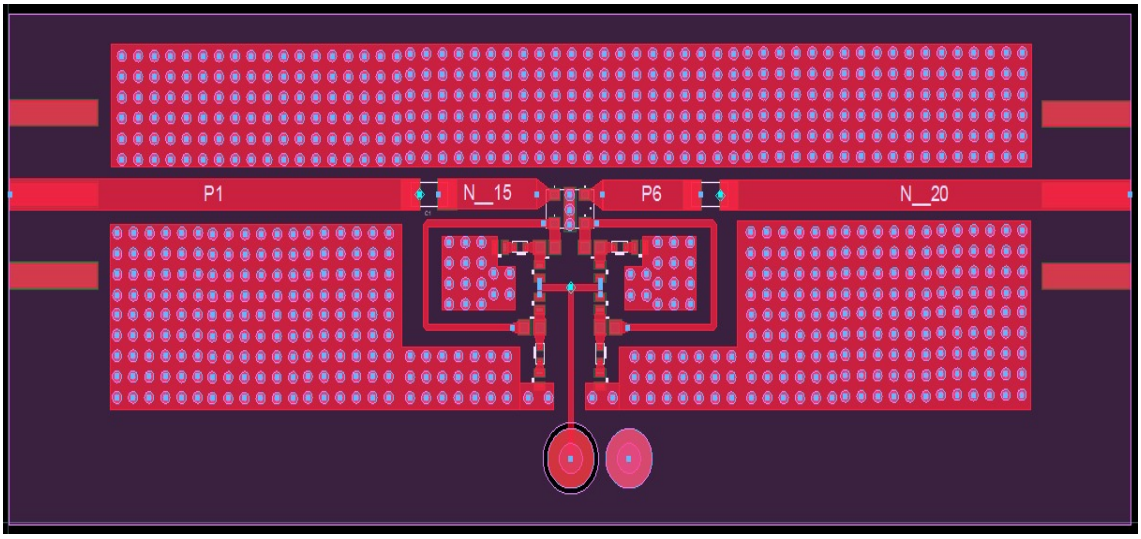


Figure 3.5: Phase shifter layout

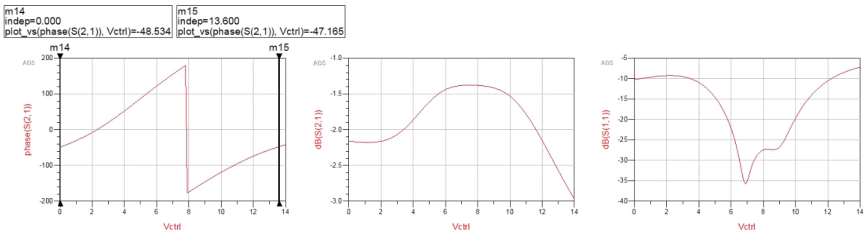


Figure 3.6: S parameters versus control voltage for phase shifter layout

3.2.1 Simulation Results

Figure 3.6 shows phase shifter gives a complete 360° phase shift when control voltage is varied from 0 volts to 13.6 volts. Figure 3.7 shows 45° phase variations in a 100 MHz frequency band. Phase shifter has a worst case P1dB of 17.6 dBm and insertion loss of 3 dB.Worst case S(1,1) is -7dB, due to this an isolator is needed before phase shifter input to improve S(1,1).

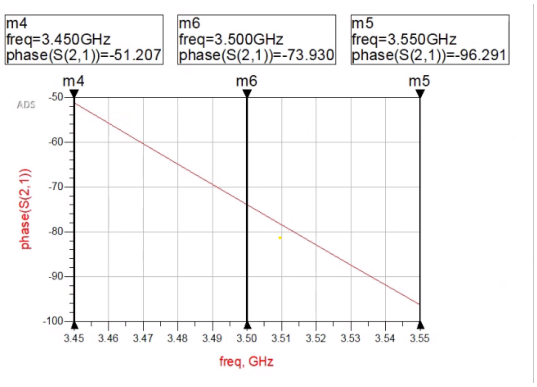


Figure 3.7: Phase shift versus frequency for phase shifter layout

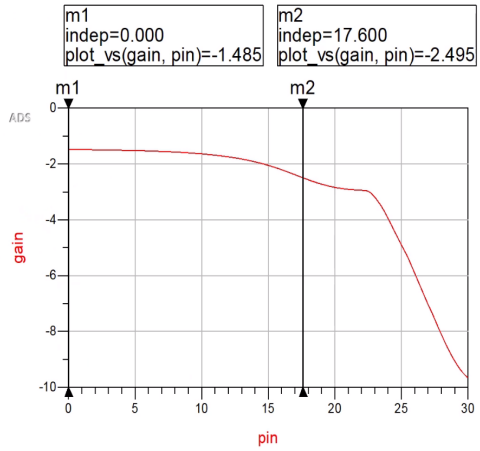


Figure 3.8: P1 dB(worst case) for phase shifter layout

Chapter 4

System Implementation

4.1 A SS Based Two-Tap RF SI Canceller

A spectral shaper based two tap RF SIC system is described which gives a significant improvement over conventional two tap RF SIC system.

4.1.1 Single tap RF SIC

Typical single tap RF SIC system in Figure 4.1 consists of a directional coupler which takes a sample of transmitted signal and then this sample is pass through vector modulator to changes its amplitude and phase. Output of a vector modulator is a first antidote signal. Power combiner combines first antidote and SI signal.

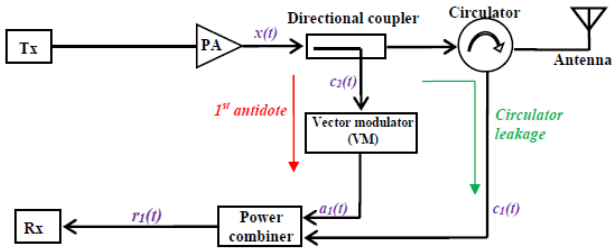


Figure 4.1: Single tap RF SIC system[4]

4.1.2 Conventional two tap RF SIC

As shown in figure 4.2 single tap RF SIC system distorts the shape of spectrum of residual SI signal. Any conventional only vector modulator based second tap RF SI cancellation technique does not provides any significant improvement because of the amplitude imbalance between second antidote and stage one RSIS.

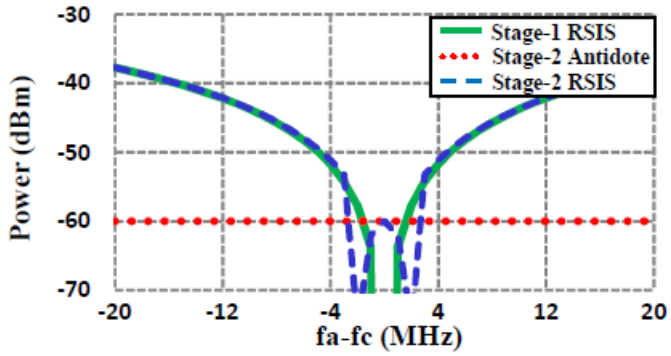


Figure 4.2: Conventional two tap RF SIC[4]

4.1.3 Spectral Shaper

To get a significant improvement through second stage, spectral shaper is used to mimic the amplitude profile of first stage RSIS. In figure 4.3 incoming signal is divided into two paths, one path consists of consists of a High Resolution Variable

Attenuator (HRVA) and other path consists of a High Resolution Variable Phase Shifter (HRPS).These two paths are combined through a power combiner.

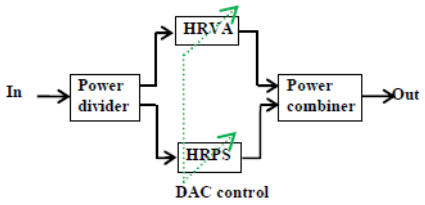


Figure 4.3: Spectral shaper[4]

Input of SS is second RF tap and it's output will dictate the second antidote signal spectrum. Here HRVA controls the loss difference between two paths which in in turn dictates the slope of second antidote spectrum. HRPS controls the phase difference between two paths which in in turn dictates the position of notch in spectrum of second antidote. Values of loss difference and phase difference is tuned to match the second antidote frequency spectrum to that of first stage RSIS.

In figure 4.4 Spectral shaper is implemented in ADS with voltage controlled phase shifter controls phase difference and variable attenuator controls loss difference between two paths.

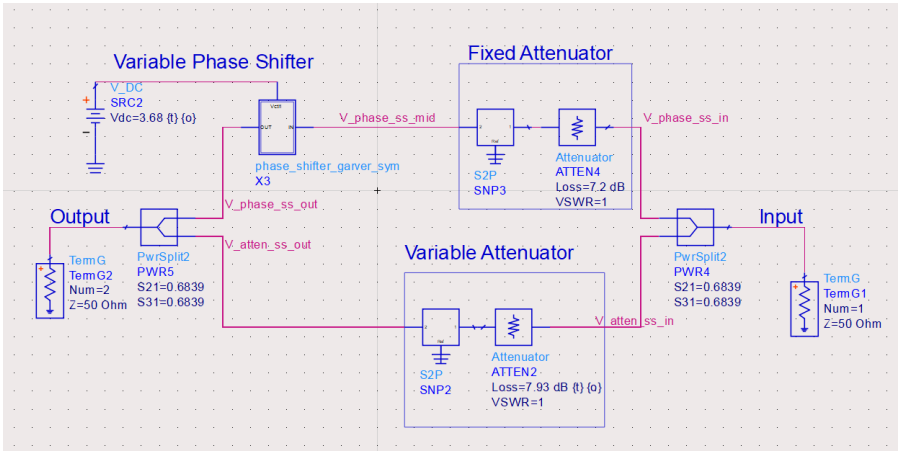


Figure 4.4: Spectral shaper schematic

Figure 4.5 shows the spectral shaper response for different values of loss difference between two paths. Loss difference dictates the slope of the spectrum around notch. Figure 4.6 shows the spectral shaper response for different values of path difference between two paths. Path difference dictates the position of notch.

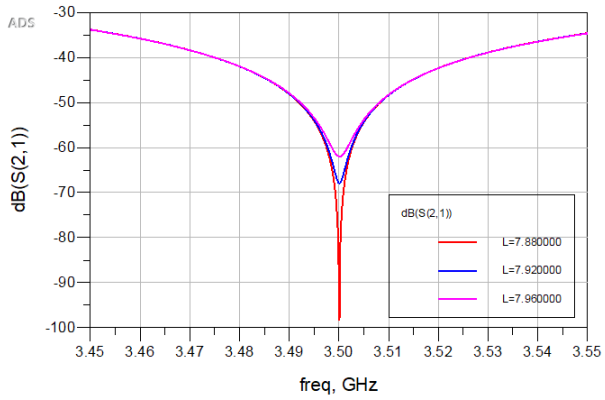


Figure 4.5: Spectral shaper for different values of loss difference(dB)

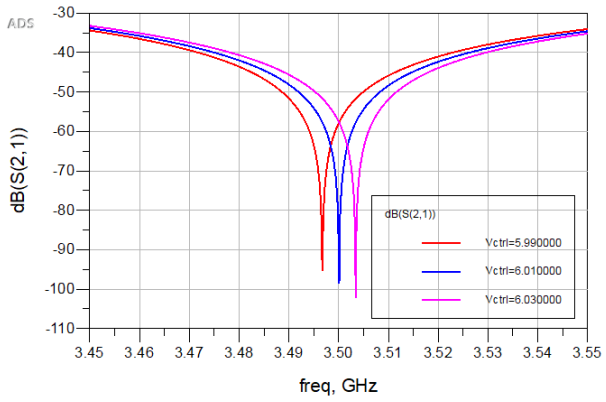


Figure 4.6: Spectral shaper for different values of phase difference

4.2 SIC and CIC Block Diagram for MIMO

In figure 4.7 2×2 MIMO SI and CI cancellation circuitry block diagram is presented. We assume that two antenna are 8 cm apart, So 20 dB attenuated and $(8 \div 30)$ns delayed version of a transmitted signal act as an cross-interference to other receiver. 10 dB PAPR OFDM signal having 100 MHz bandwidth and 41.5 dBm average power is the output of the power amplifier which is a transmitter signal. 20 dB isolation between transmit and receive port is provided by circulator. A receiver experience a 21.5 dB of SI and 21.5 dB of CI. A 20 dB coupler samples this transmitter signal, which act as an input for interference cancellation circuitry.

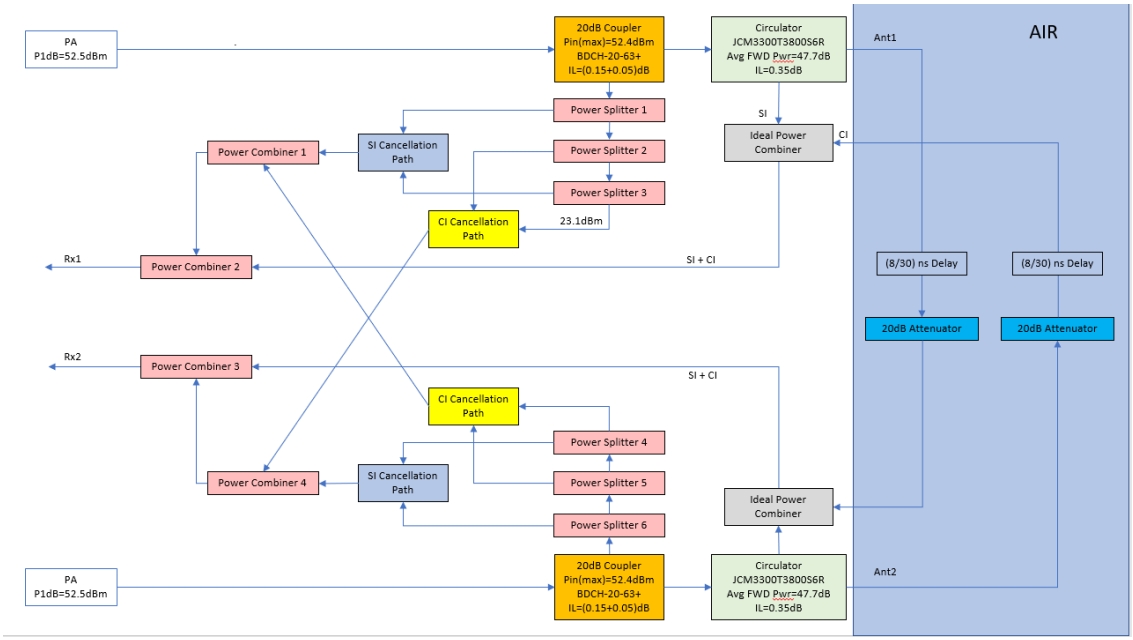


Figure 4.7: SIC and CIC block diagram for MIMO

4.2.1 SI and CI Cancellation Path

In figure 4.8 output from power splitter 3 and 1 act as a first and second RF tap for SI cancellation block. It gives combination of first antidote and second antidote

signal as an output. Combination of a variable attenuator and phase shifter act as a vector modulator. First stage consist of a vector modulator and fixed amplifiers. Second stage consists of a spectral shaper, vector modulator and fixed amplifier. Parameters of vector modulator are varied through a gradient descent algorithm on basis of residual interference signal power. Fixed amplifiers are used to match power level of combined antidote to that of interference signal. In figure 4.9 CI cancellation path block diagram inputs are first and second RF tap and it's output is combination of first antidote and second antidote signal. This method of CI cancellation is called "SISO Replication Based Design".In this SI cancellation block is replicated for CI cancellation as well.

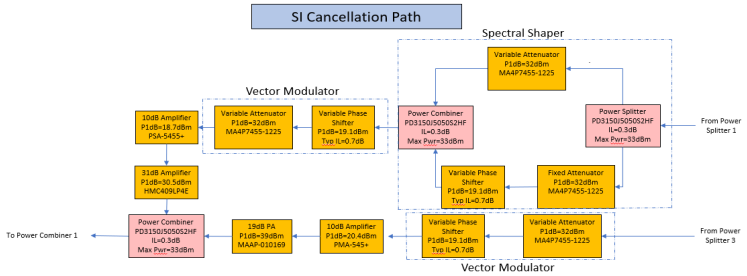


Figure 4.8: SI cancellation path block diagram for phase shifter schematic

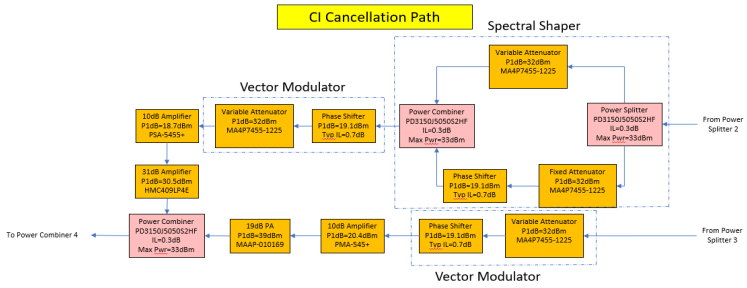


Figure 4.9: CI cancellation path block diagram for phase shifter schematic

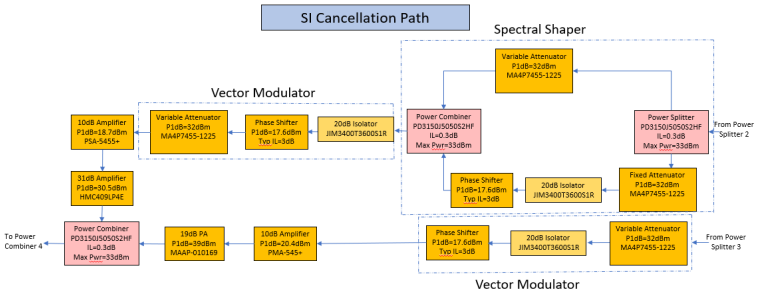


Figure 4.10: SI cancellation path block diagram for phase shifter layout

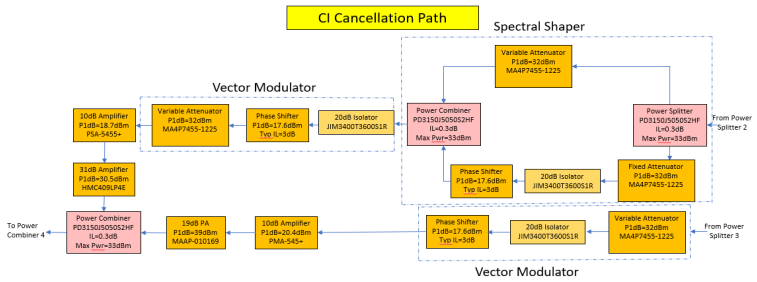


Figure 4.11: CI cancellation path block diagram for phase shifter layout

Chapter 5

Simulation Results

All simulations are done in Advanced Design System (ADS) software. S parameter files of components are used for simulations. ADS inbuilt gradient descent algorithm is used for optimization of variables according to residual interference power. Figure 5.1 shows frequency spectrum of the output of a power amplifier, an OFDM signal having a 11 dB PAPR and average power of 41.5 dBm. This signal has a bandwidth of 100 Mhz with a centre frequency of 3.5 GHz.

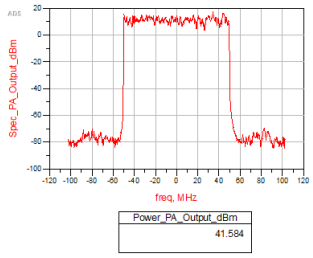


Figure 5.1: PA output frequency spectrum

5.1 Simulations with Phase Shifter Schematic

5.1.1 Single Stage SI Cancellation

Figure 5.2 shows the schematic of single stage SI cancellation circuitry when only SI is present (**No CI**). According to figure 5.3 interferer power is reduced from 21.221 dBm to 8.076 dBm, thus giving 14.14 dB cancellation.

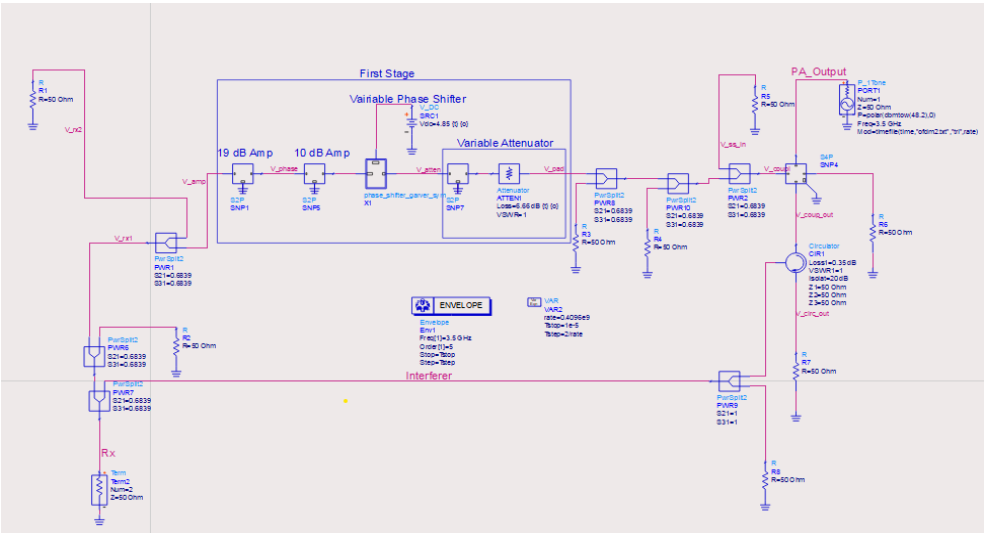


Figure 5.2: Single stage SIC schematic with phase shifter schematic

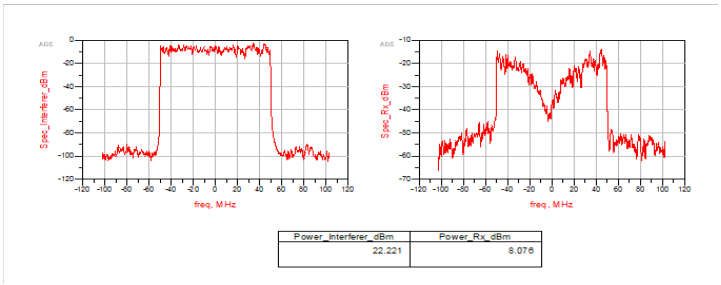


Figure 5.3: Single stage SIC spectrum with phase shifter schematic

5.1.2 Two Stage SI Cancellation

Figure 5.4 shows the schematic of two stage SI cancellation circuitry when only SI is present (**No CI**). According to figure 5.5 interferer power is reduced from 21.220 dBm to 0.264 dBm, thus giving 20.95 dB cancellation.

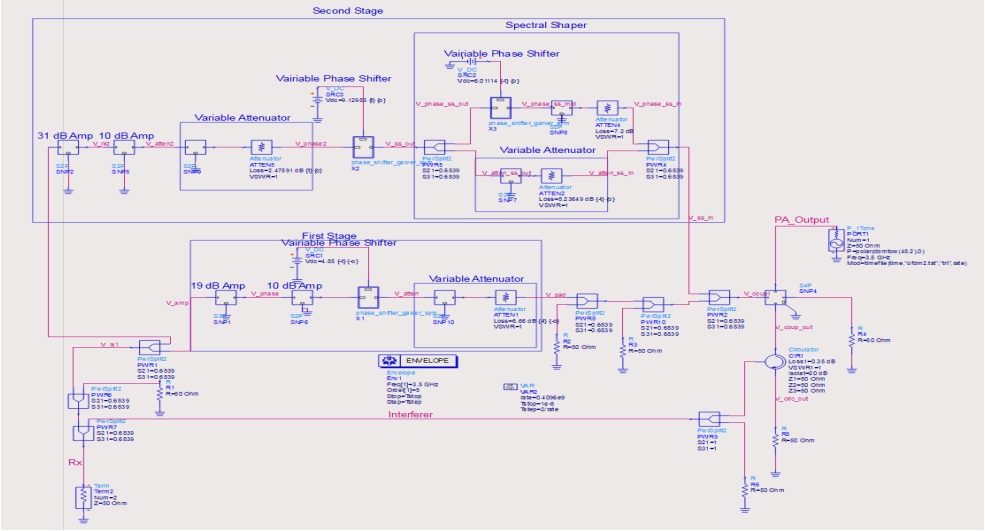
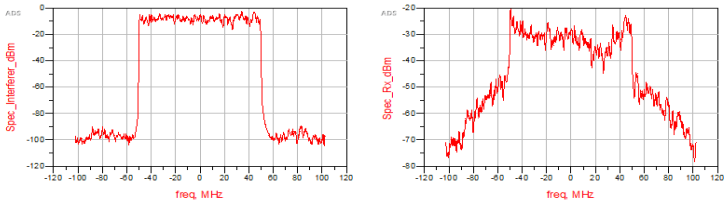


Figure 5.4: Two stage SIC schematic with phase shifter schematic



Power_Interferer_dBm	Power_Rx_dBm
22.220	0.264

Figure 5.5: Two stage SIC spectrum with phase shifter schematic

5.1.3 Single Stage CI Cancellation

Figure 5.6 shows the schematic of single stage CI cancellation circuitry when only CI is present (**No SI**). According to figure 5.7 interferer power is reduced from 21.784 dBm to 7.437 dBm, thus giving 14.34 dB cancellation.

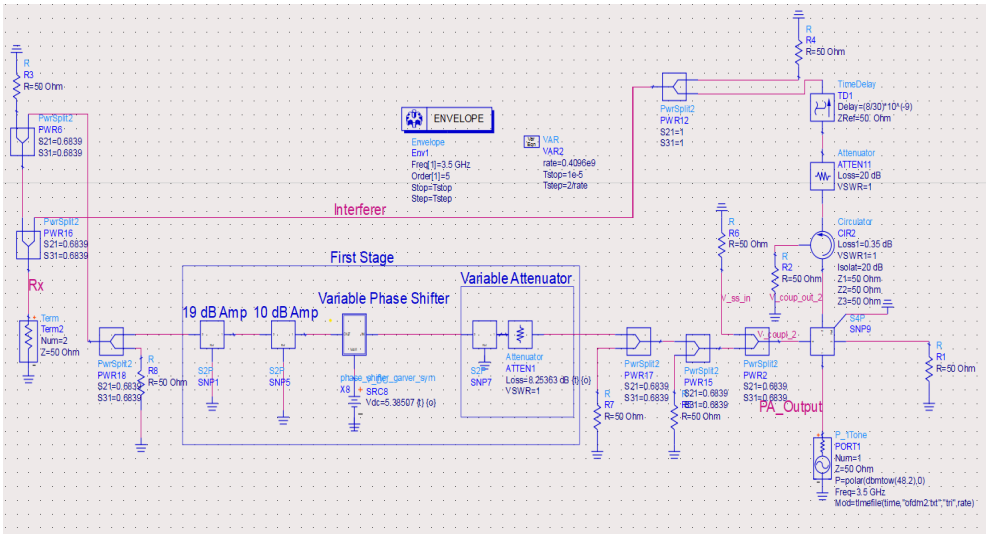


Figure 5.6: Single stage CIC schematic with phase shifter schematic

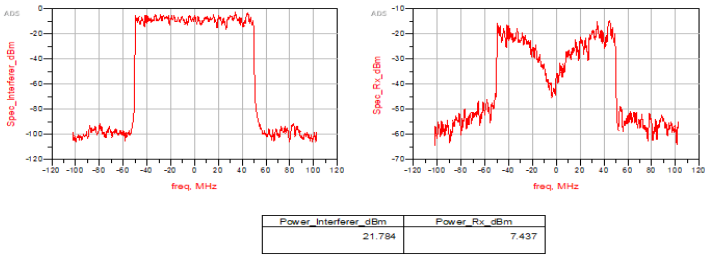


Figure 5.7: Single stage CIC spectrum with phase shifter schematic

5.1.4 Two Stage CI Cancellation

Figure 5.8 shows the schematic of single stage CI cancellation circuitry when only CI is present (**No SI**). According to figure 5.9 interferer power is reduced from 21.784 dBm to -4.284 dBm, thus giving 26.07 dB cancellation.

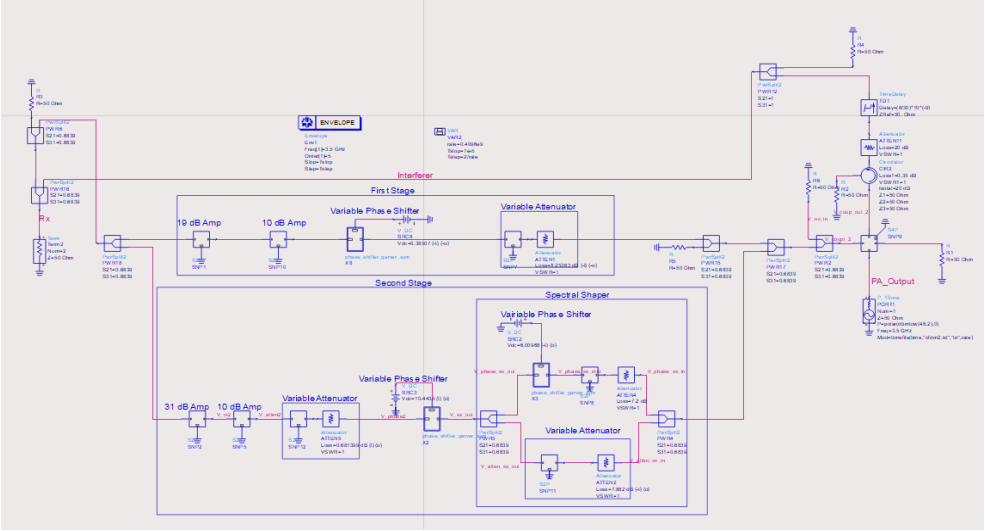


Figure 5.8: Two stage CIC schematic with phase shifter schematic

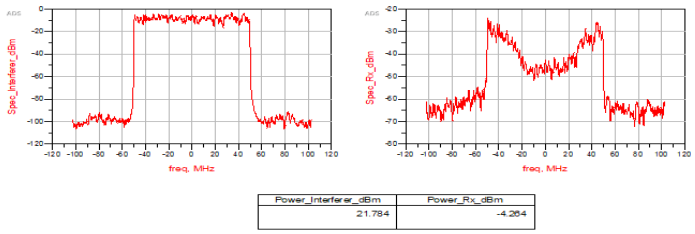


Figure 5.9: Two stage SIC schematic with phase shifter schematic

5.2 Simulations with Phase Shifter Layout

5.2.1 Single Stage SI Cancellation

Figure 5.10 shows the schematic of single stage SI cancellation circuitry when only SI is present (**No CI**). According to figure 5.11 interferer power is reduced from 22.221 dBm to 9.515 dBm, thus giving 12.71 dB cancellation.

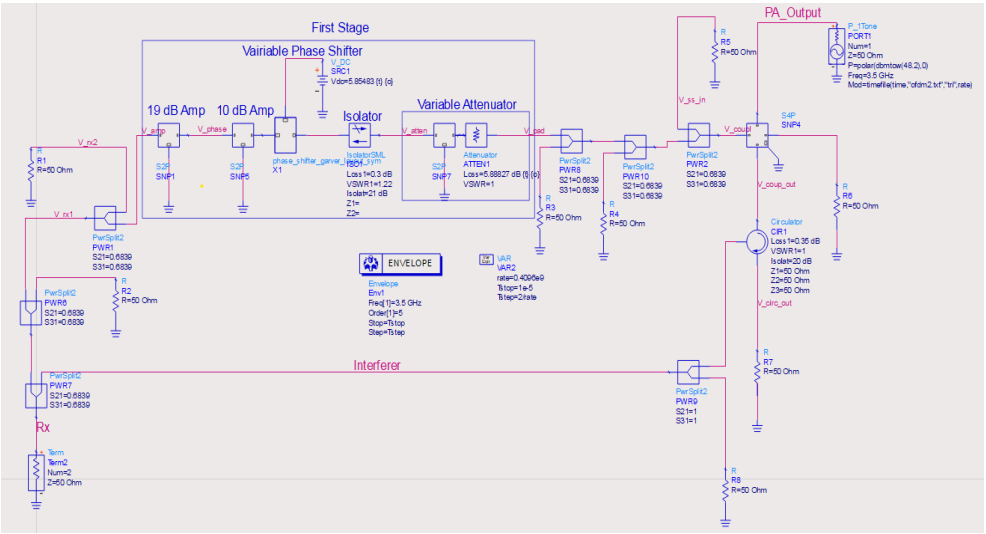
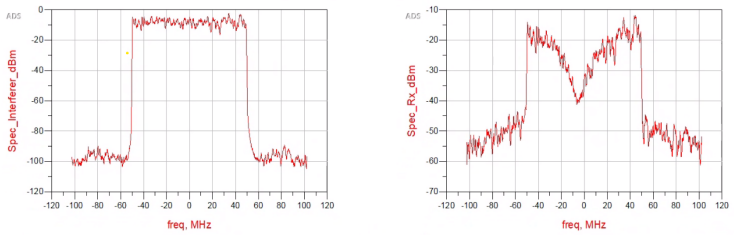


Figure 5.10: Single stage SIC schematic with phase shifter layout



P_Interferer_dBm	Power_Rx_dBm
22.221	9.515

Figure 5.11: Single stage SIC spectrum with phase shifter layout

5.2.2 Two Stage SI Cancellation

Figure 5.12 shows the schematic of two stage SI cancellation circuitry when only SI is present (**No CI**). According to figure 5.13 interferer power is reduced from 22.22 dBm to 2.862 dBm, thus giving 19.36 dB cancellation.

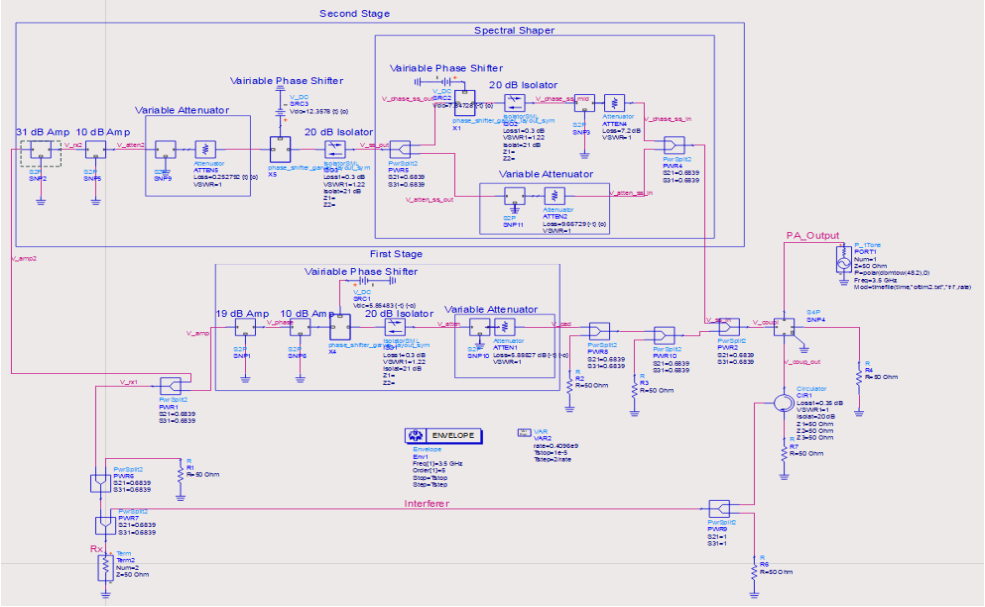


Figure 5.12: Two stage SIC schematic with phase shifter layout

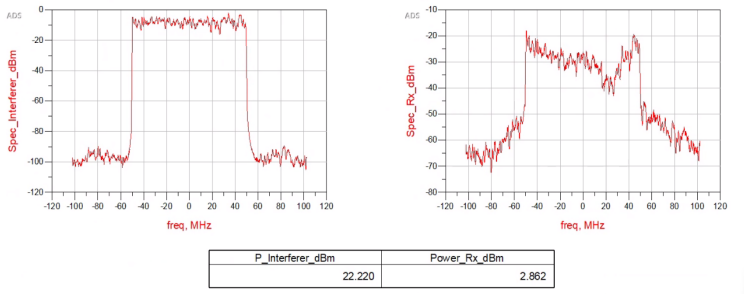


Figure 5.13: Two stage SIC spectrum with phase shifter layout

5.2.3 Single Stage CI Cancellation

Figure 5.14 shows the schematic of single stage CI cancellation circuitry when only CI is present (**No SI**). According to figure 5.15 interferer power is reduced from 21.784 dBm to 7.775 dBm, thus giving 14.01 dB cancellation.

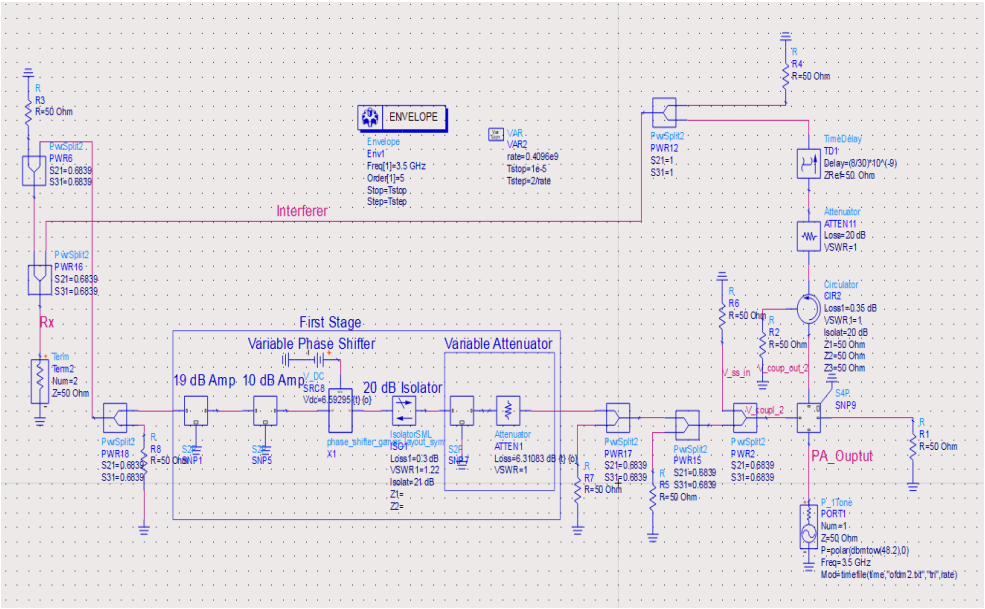
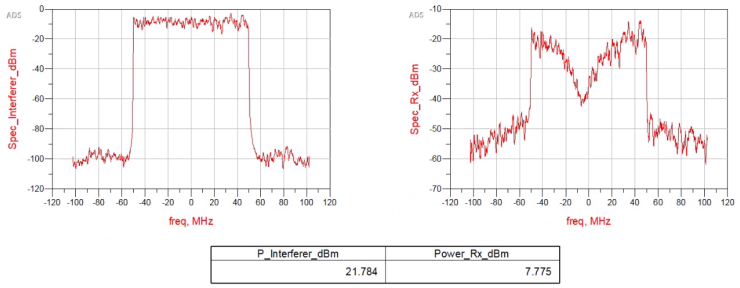


Figure 5.14: Single stage CIC schematic with phase shifter layout



P_Interferer_dBm	Power_Rx_dBm
21.784	7.775

Figure 5.15: Single stage CIC spectrum with phase shifter layout

5.2.4 Two Stage CI Cancellation

Figure 5.16 shows the schematic of single stage CI cancellation circuitry when only CI is present (**No SI**). According to figure 5.17 interferer power is reduced from 21.784 dBm to -3.609 dBm, thus giving 25.4 dB cancellation.

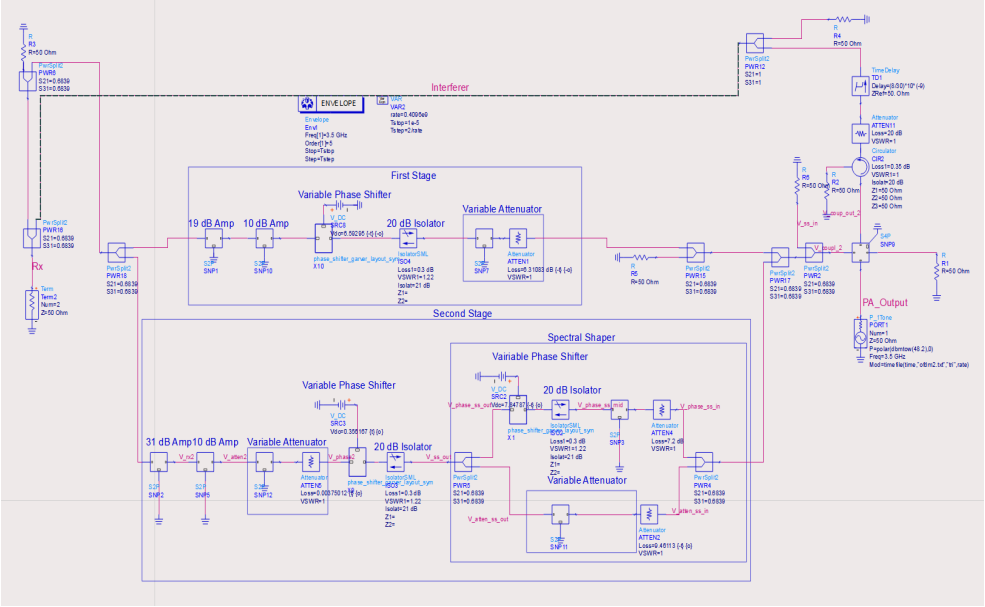
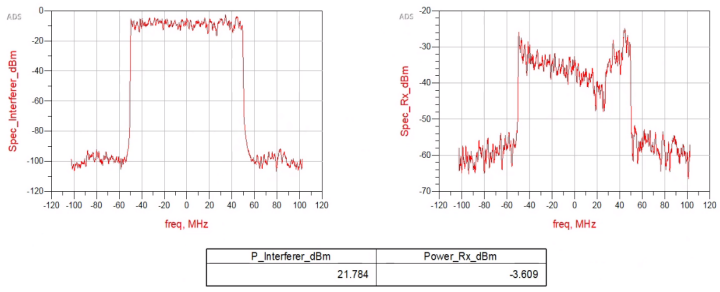


Figure 5.16: Two stage CIC schematic with phase shifter layout



P_Interferer_dBm	Power_Rx_dBm
21.784	-3.609

Figure 5.17: Two stage CIC spectrum with phase shifter layout

5.3 Two Stage SIC and CIC in MIMO

Figure 5.18 shows schematic of two stage SI and CI cancellation in 2×2 MIMO. V_interferer_1 denotes over all interference(**SI and CI**) at first receiver before cancellation and V_rx_1 denotes the residual interference. Refer figure4.8 and figure 4.9 for SI Cancellation Path block and CI Cancellation Path block respectively.

A 20 dB attenuated and $(8 \div 30)$ns delayed version of a transmitted signal from other antenna act as an CI to a receiver. A 20 dB attenuated version of a own transmitted signal act as an SI to a receiver.

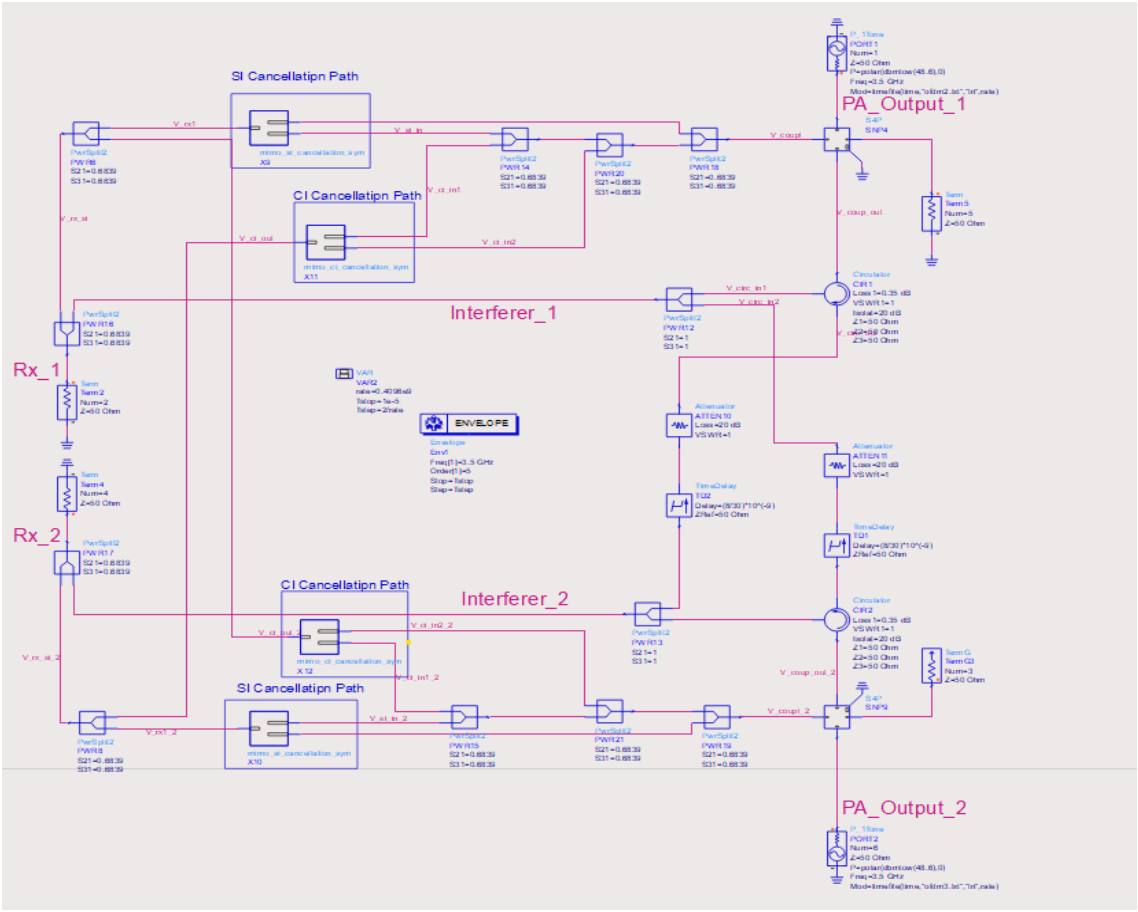
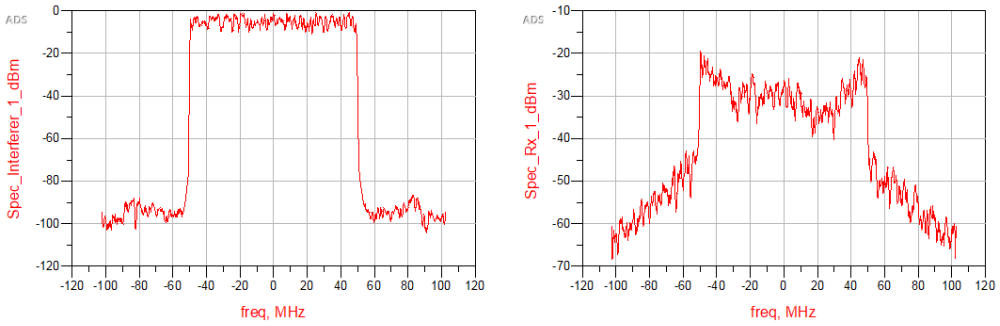


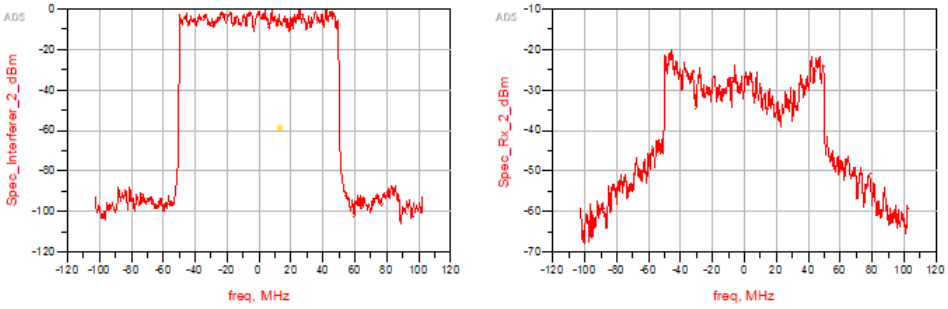
Figure 5.18: Two stage SIC and CIC in MIMO schematic

According to figure 5.19 total interferer power at first receiver is reduced from 25.255 dBm to 2.016 dBm, thus giving 23.24 dB cancellation. In figure 5.20 total interferer power at second receiver is reduced from 25.289 dBm to 2.420 dBm, thus giving 22.9 dB cancellation.



Power_Interferer_1_dBm	Power_Rx_1_dBm
25.255	2.016

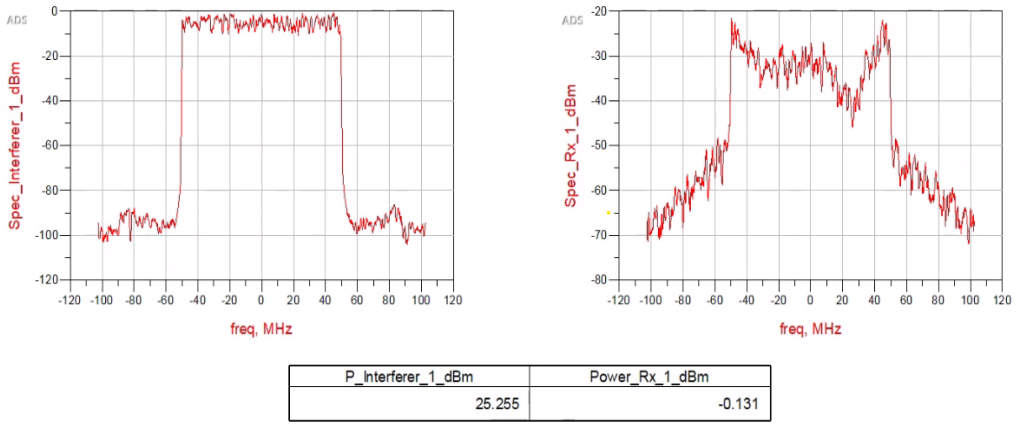
Figure 5.19: First receiver interference cancellation with phase shifter schematic



Power_Interferer_2_dBm	Power_Rx_2_dBm
25.289	2.420

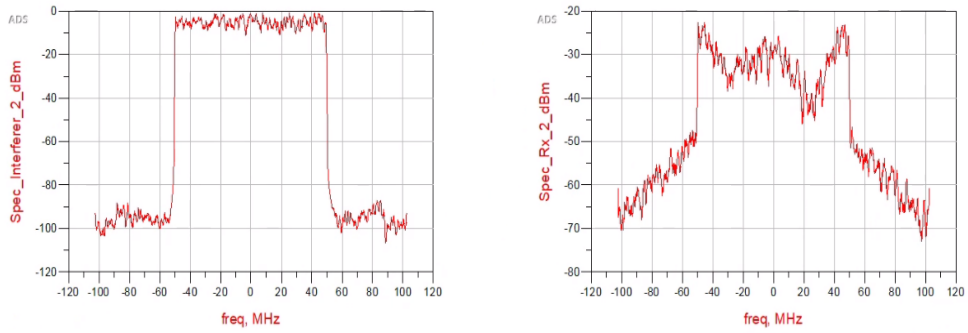
Figure 5.20: Second receiver interference cancellation with phase shifter schematic

According to figure 5.21 total interferer power at first receiver is reduced from 25.255 dBm to -0.131 dBm, thus giving 25.39 dB cancellation. In figure 5.22 total interferer power at second receiver is reduced from 25.289 dBm to 0.118 dBm, thus giving 25.17 dB cancellation.



P_Interferer_1_dBm	Power_Rx_1_dBm
25.255	-0.131

Figure 5.21: First receiver interference cancellation with phase shifter layout



P_Interferer_2_dBm	Power_Rx_2_dBm
25.289	0.118

Figure 5.22: Second receiver interference cancellation with phase shifter layout

5.4 Cancellation Numbers

Figure 5.23 shows cancellation obtained with phase shifter schematic and phase shifter layout in different interference condition. Single stage SIC with phase shifter layout is 1.4 dB less then with phase shifter schematic. Two stage SIC with phase shifter layout is 1.6 dB less then with phase shifter schematic.

Similarly, Single stage CIC with phase shifter layout is .3 dB less then with phase shifter schematic. Two stage CIC with phase shifter layout is .6 dB less then with phase shifter schematic.

Phase shifter with layout gives less cancellation because it has more phase shift variations across frequency as compare to that of phase shifter schematic.

Interference condition	Cancellation type	Cancellation(dB) with Phase Shifter Schematic	Cancellation(dB) with Phase Shifter Layout
Only SI present	Single Stage SIC	14.1	12.7
	Two Stage SIC	21	19.4
Only CI present	Single Stage CIC	14.3	14
	Two Stage CIC	26	25.4
Both CI and SI present	Two Stage CIC and SIC	22.9	25.2

Figure 5.23: Cancellation numbers

Chapter 6

Conclusions and Future Work

Through RF interference cancellation techniques, interferer power is reduced to 0.8 dBm but for effective communication interferer power should be reduced down to noise floor around -94 dBm. Complete system with analog baseband and digital cancellation as well can be explored.

Proposed SISO Replication Based CIC technique complexity increases exponentially with MIMO size that's why this technique is infeasible for massive MIMO. A technique with a linear complexity can be explored so that in-band full duplex can be used in massive MIMO as well.

Proposed phase shifter has a P1dB of 17.6 dBm, due to this coupled signal is attenuated then phase shifter is used and then high gain amplifiers are used. Complexity and cost of cancellation circuitry is increased. Phase shifter has a phase variation of 30° in a 100 MHz band, due to this low cancellation is obtained. A better phase shifter design with higher P1dB and lower phase variation can be explored.

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Appendix A

Layout Information

A.1 Board Stack-Up

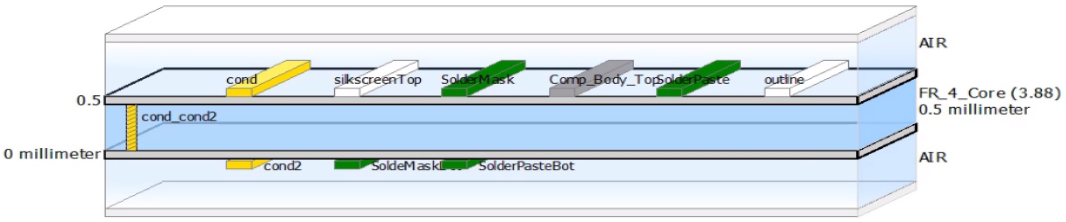

Figure A.1: Board stack-up

Isola 185HR laminate is used. Cond and Cond2 are copper metal layer of thickness 35.56um and conductivity 5.8e7 S.

A.2 Variable Attenuator Layout

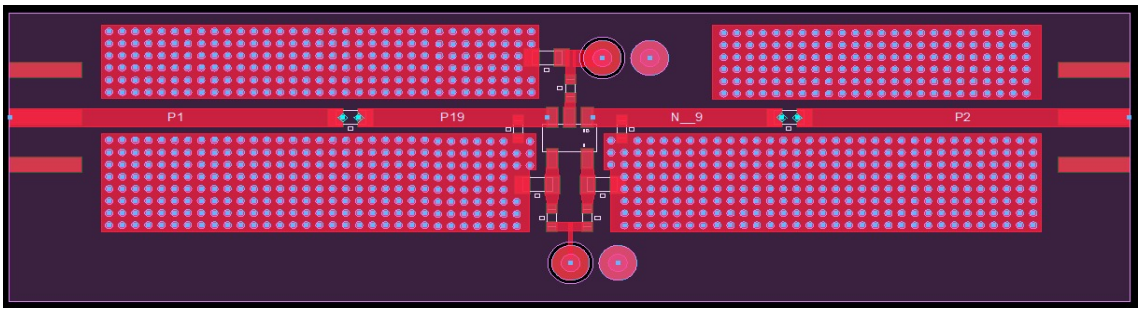

Figure A.2: Variable attenuator layout

Recommended PCB layout of MA4P7455-1225 is done according to component specification sheet.

Appendix B

Components Information

Component Name	Component Number
20dB Coupler	BDCH-20-63+
Power Combiner/Splitter	ZB2PD-63+
Variable Attenuator	MA4P7455-1225
10dB Amplifier	PMA-545+
10dB Amplifier	PSA-5455+
19dB PA	MAAP-010169
31dB Amplifier	HMC409LP4E
19dB PA Evaluation Board	MAAP-010169-001SMB
31dB Amplifier Evaluation Board	108355-HMC409LP4
PSA-5455+ Evaluation Board	TB-534-5+
PMA-545+ Evaluation Board	TB-501+
Varactor	MA46H120
3dB Hybrid Coupler	X4C35J1-03G
100pF capacitors for attenuator setup	Murata 0603 (GCM1885C1H101FA16D)
1000Ohms resistors for attenuator setup	Panasonic 0402 (ERJ-PA2D1001X)
20pF Capacitor	CBR02C200F5GAC
4.7nH Inductor	LQW03AW4N7J00D
11nH Inductor	LQW03AW11NJ00D
Edge SMA Connectors	EMPCB.SMAFSTJ.C.HT
20dB Isolator	JIM3400T3600S1R
DC Header pins	61300311121

Figure B.1: Components name and number