DESIGN OF CMOS RING OSCILLATOR

PROJECT REPORT

Submitted by

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CERTIFICATE

This is to certify that this thesis (or project report) entitled ***"DESIGN OF CMOS RING OSCILLATOR"*** submitted by **SAI SUMANTH POTHURI** to the Indian Institute of Technology Madras, for the award of the degree of **Masters of Technology** is a bonafide record of the research work done by him under my supervision. The contents of this thesis (or project report), in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma..

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I would like to extend my appreciation to all my friends and for their help and support in completing my project successfully.

Abstract

This project presents the design of a 3-stage CMOS Ring Oscillator that oscillates at 20MHz frequency. The 3-stage CMOS Ring Oscillator is implemented using TSMC 65nm low power process. The Ring Oscillator will work across all the corners, with supply voltage variation from 1.1V to 1.4V across the temperature of 0°C to 100°C. The achieved output frequency is 20MHz±3% including across all the corners, temperature and supply voltages. The dimension of the realized layout is 155.85μm x 62.96μm.

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ABBREVIATIONS

RO	Ring Oscillator
LDO	Low Drop Out
CMOS	Complementary Metal–Oxide–Semiconductor
NMOS	Negative channel Metal Oxide Semiconductor
PMOS	Positive channel Metal Oxide Semiconductor

Chapter 1

Introduction

1.1 Outline Of Report

Chapter 1 gives the outline of the report. In chapter 2, section 2.1 gives the introduction to the oscillator and section 2.2 gives the Design of the Ring Oscillator. Chapter 3 shows the outputs or results of the designed Ring Oscillator.

Chapter 2

Ring Oscillator

2.1 Introduction to Oscillator

An oscillator is a system that takes dc as input in the form of power supply and gives output an alternating voltage current or voltage signal. Apart from the power supply, no input ac signal will be given to the oscillator, so we can treat the system as no input required for the output oscillations to produce. The oscillator is a positive feedback system. It is made up of a gain block and a frequency-selection network connected in a positive-feedback loop, as shown in the figure 2.1. Although an actual oscillator does not have an input X(s) signal to drive it, the assumption of this input signal simplifies the s-domain analysis of the feedback loop.

As the oscillator is in positive feedback, the analysis will be nonlinear. For the simple analysis, we consider the system as linear one. By using linear system analysis, we can make reasonable first-order approximation. From the figure 2.1, the transfer function can be written as shown in the equation 2.1.1

$$H(s) = \frac{X(s)}{Y(s)} = \frac{A(s)}{1 - A(s)\alpha(s)} \tag{2.1.1}$$

Where A(s) is the s-domain function of the amplifier block, and $\alpha(s)$ is the s-domain transfer function of the frequency-selective network or feedback network. Let us define the loop gain L(s) as $L(s) = A(s) * \alpha(s)$.

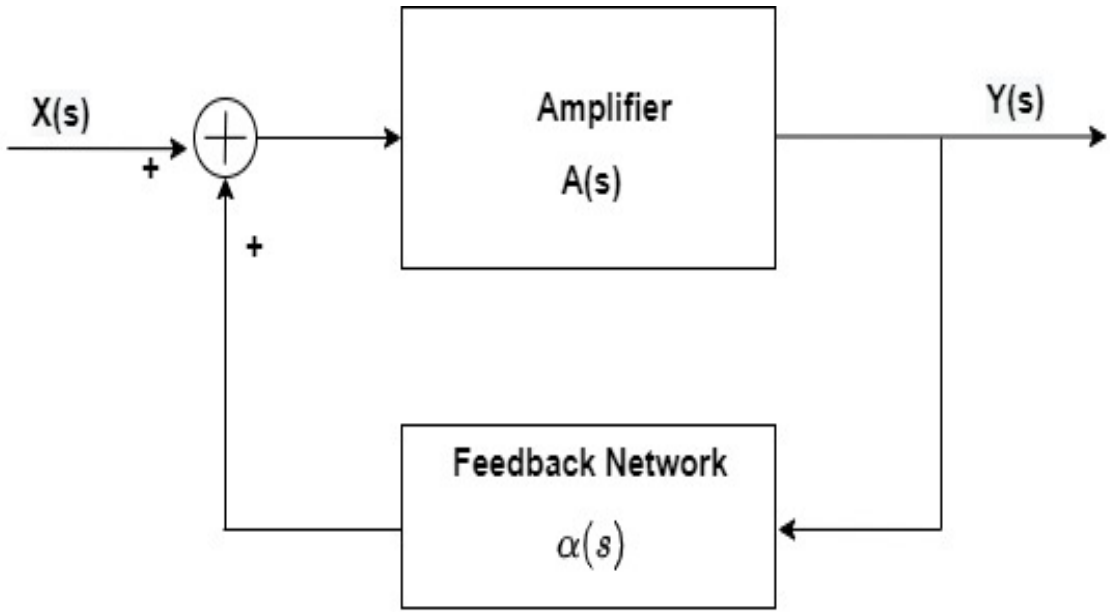

Figure 2.1: Positive feedback oscillator system modelled in s-domain

From the definiton of the standard oscillator, the system must have a finite output even in the absence of the input signal. The above equations show that this condition occurs when the transfer function converges to infinity at a specific frequency, which implies that the loop gain L(s) should be equal to one at this frequency. For the feedback loop to provide a stable oscillation, the magnitude of the loop gain should be equal to unity and the phase of the loop gain should be an integer multiple of 2n which is known as the Barkhausen criterion. It should be noted that this criterion only guarantees that the oscillator will be sustained after

it starts, not that it will start.

Generally, the magnitude of the loop gain will be designed to be slightly greater than unity in order for the oscillation to begin. So, due to the positive feedback, the signal will grow indefinitely, unless there is some mechanism to stop the signal's growth. Physically, the noise present in the components will be amplified by the positive feedback gain, which results to the periodic signal at the output.

The feedback gain will then drop to unity as the signals grow larger due to the amplitude limiting mechanism, resulting in a steady-state oscillatory signal. The gain of the loop function determines whether or not the oscillator starts, but the phase characteristics of the feedback loop determine the oscillation frequency. The feedback system oscillates when the phase is zero or an integer multiple of 2n.

2.1.1 Barkhausen Criteria

Because the ring oscillator is a nonlinear larger signal feedback system, obtaining an exact analysis of the ring oscillator is extremely difficult. However, we can analyze using the small signal model approximation for the understanding. The ring oscillator's operation can be explained using the first order approximation. The oscillator is a positive feedback system that is built by the amplifier block, as shown in figure 2.1.1. Because the amplifier block must have too much phase shift at a certain frequency for the oscillation to begin, the oscillator must be a positive feedback system. In other words, the noise signal will be amplified and accumulated on the input signal again; then the oscillation will start. If the phase shift is not enough, the system will become an amplifier

Even if the phase shift is sufficient, the oscillation cannot begin in some cases because the gain of the amplifier block is insufficient. If the gain is less than one, the

positive feedback system will also latch up to the power supply instead of oscillating. There is a theory named " Barkhausen Criteria" to describe the conditions needed to make oscillation. The Barkhausen Criteria can be summarized as follows:

- The gain of the amplifier block of oscillator must be more than 1 as:

$$|A(s)| > 1 \tag{2.1.2}$$

- The phase shift of the amplifier block must equal to 360° as:

$$\angle A(s) = 360^\circ \tag{2.1.3}$$

Even when the gain of the amplifier block is equal to one, the oscillation does not start or is unstable in most cases. In general, the oscillator designer maximises the gain, which CMOS technology can easily achieve. Furthermore, the Barkhausen Criteria are necessary but not sufficient conditions for the oscillation.

2.2 Design of Ring Oscillator

2.2.1 CMOS Ring Oscillator

CMOS Ring Oscillators are the oscillators made using CMOS technologies which can be realizable completely on the chip. In CMOS Ring Oscillator the amplifier block is replaced by using the inverters here and unity feedback is used in our CMOS Ring Oscillator. The CMOS Ring Oscillator is a critical component of all digital and

analog systems which can be used as clocks in systems, are one of the most common. The most significant advantage of CMOS Ring Oscillator is that it is compatible with integration which requires very less area of the die in the chip.

The CMOS ring oscillator is more stable in terms of oscillation frequency versus supply voltage variation. The combined structure, in fact, has less frequency deviation with noisy supply voltages. A ring oscillator is composed of several delay stages. An oscillator can be built with an odd number of single-input, single-output delay stages or with an even number of differential delay stages. According to the Barkhausen criteria, each stage should add (or reduce) 180/N phase to the signal, with the other 180° provided by the sign of inverters (N; number of stages are odd). Here in our project, we considered three stage ring oscillator, so the value of N is equal to 3.

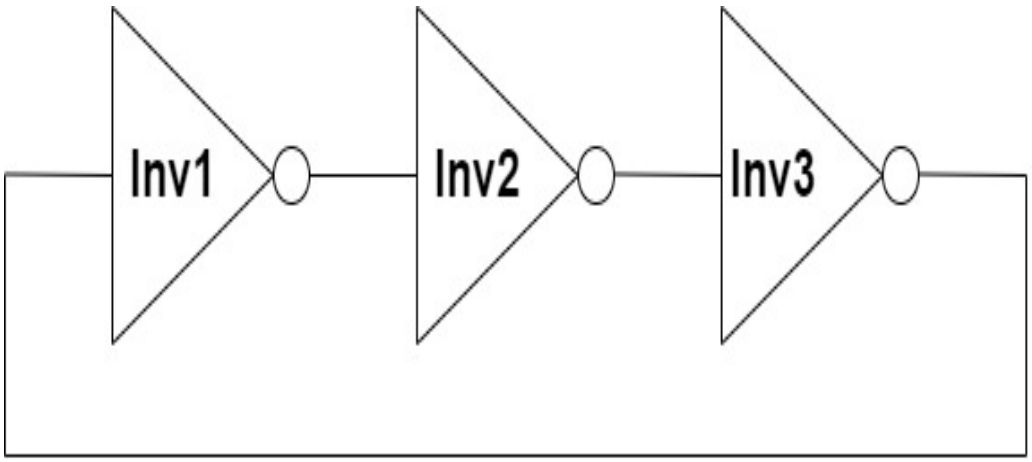

Figure 2.2: 3-stage Ring Oscillator

The CMOS Ring Oscillator contains odd number of inverters in a feedback loop so that it will keep on oscillate. Here in the CMOS Ring Oscillator, inverters were also made by CMOS process. Each inverter will introduce certain amount of delay, so, that frequency of oscillation is adjusted by changing the delay introduced by

each inverter. Here in this project, we considered 3 stage ring oscillator, so that here n = 3. Here as the output of the 1st inverter is connected to the 2nd and the output of the 2nd inverter is connected to the 3rd inverter and the output of the 3rd inverter is connected back to the 1st inverter. Due to the noise, let us say, the output at the 3rd inverter is 1, then it will drive the 1st inverter to get to 0 which is the inverter operation, and as now, the output at 1st inverter is 0, it will drive the 2nd inverter to get to 1 and this will drive the 3rd inverter to get the output to 0. So, the output at the 3rd inverter starts from 1 and it again converted to 0. To convert from 1 to 0 or 0 to 1, it will take time which is nothing but the delay of the Ring Oscillator. This delay will be introduced by each of the inverter in the circuit.

Here for our 20MHz oscillator, the time period (one 1 and one 0) is 0.05 microseconds. So, to change from 1 to 0 or 0 to 1 it should take 0.05/2 which is equal to 0.025 microseconds. So, this means that, each inverter should constitute 0.025 microseconds of delay. This delay can be adjusted by adding a load capacitor to the inverter, by which the inverter current should drive the load which takes the time to charge or to discharge through PMOS or NMOS transistors of the inverter. The length of the transistors changes the output impedance of the inverter which again alters the delay of the inverter and this is also one of the ways to change the delay produced by each inverter. Here in this project, the length is made constant and the load capacitor to the inverter is changed to get the suitable delay.

2.2.2 Current Bias Inverter

A CMOS inverter, which consists of an NMOS and a PMOS transistor, is the most commonly used single-ended ring oscillator stage. However control operation is not there in the conventional inverter. A control method can be added in a variety of ways, including changing the strength of an inverter in the loop by changing the current, changing the loads, or varying Vdd. Figure 2.3 depicts an implementa-

tion in which the strength of an inverter is changed by adding two more transistors, M1 and M4, to the inverter structure, which is known as the current starved inverter.

The normal inverter that consists of one NMOS and PMOS inverter can be used, but there the current through the transistor is $I = \frac{\mu_n Cox W(Vgs-V_{th})^2}{2L}$ and so, the current driving the load is directly proportional to the square of the voltage, and so with the small voltage variation, the change in the current is more and the delay changes by a large amount which changes the frequency of operation. So Current starved inverter is preferred to the normal inverter.

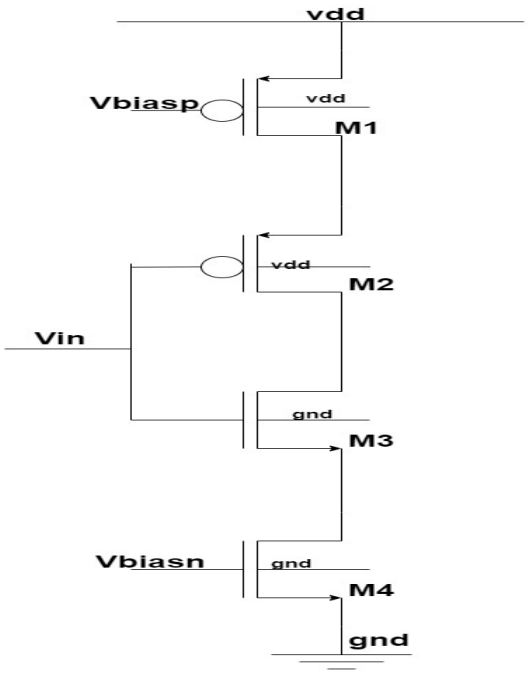

Figure 2.3: Current Biased Inverter

Here M1, M4 are the current source transistors used for the biasing of the inverter and M2 and M3 constitutes the core inverter of the Current Biased Inverter which inverts the input voltage Vin. Here the current is dependent on the M1 and

M4 transistors and Vbiasp and Vbiasn are the bias voltages given so that the enough current can be supplied from the M1 and M4 transistors which are required to drive the load and so the delay can be controlled by the current provided by the Vbiasp or Vbiasn.

Here in this project, capacitor is used as a load to the current biased inverter, and the load capacitor is tuned to get the frequency of oscillation. Although ring oscillator architectures can use power supply control, using a low power supply voltage result in smaller output swings. This reduces phase noise performance and makes the circuits more susceptible to supply and ground disturbances. Shifts in DC levels due to supply voltage changes are also undesirable.

2.2.3 Design of Ring Oscillator

The 3-stage ring oscillator is made by the above current baised inverters with feedback connected from the output of 3^{rd} stage of inverter to the input of the 1^{st} inverter as shown in the figure 2.4

The transistors M1, M4, M5, M8, M9, M12 are the current source transistors and M2, M3, M6, M7, M10, M11 constitute the three inverters. The voltage to the PMOS current source transistors is given from the constant voltage source and the current to the NMOS transistors is fed by the current mirror made by the transistors M16 and M17.

This type of inverter is known as current starved inverter, because the biasing is done using the current rather than using the voltage. The advantage of biasing with current is to reduce the variation of the oscillation frequency along the corners and temperature. The current through MOS transistor depends with the square of the voltage and so the small variation in voltage leads to large variation of current

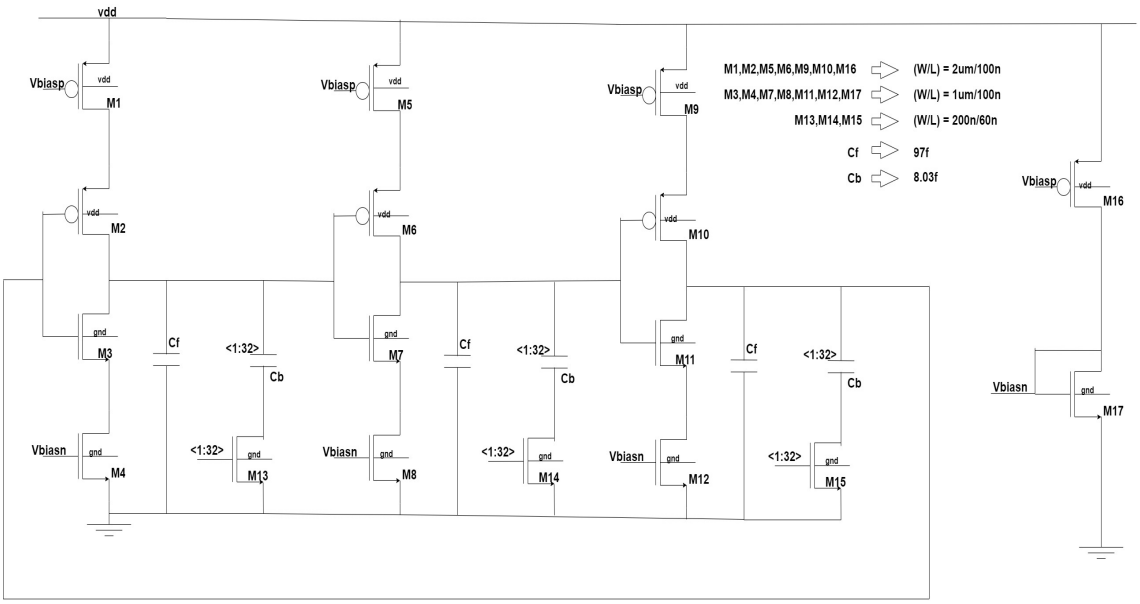

Figure 2.4: 3-stage Ring Oscillator

that charges or discharges the capacitor and so leads to the large variation in the delay to charge or discharge and so the frequency variation is very high in voltage biasing. So, in the ring oscillator current biasing is used.

Length of the transistors and the capacitors at the load to the inverter is varied to set the frequency of the oscillation. Here in our project the length of the transistor is kept fixed and the load capacitor is tuned to get the required frequency of oscillation. As the load capacitor changes, the product of resistance and the capacitance which is the time constant changes, and so the delay changes, and the frequency can be varied. The variation of the frequency is more at the different corners, so to fix that a bank of capacitor with 32-bit control using mosfet and a fixed capacitor is used. Fixed capacitor acts as fixed load to the inverter and the capacitve load can be varied by changing the no. of bits given to the MOSFET and so the capacitor is tuned at each and every corner by changing the no. of bits to get the oscillation frequency close to 20MHz. The values of the fixed and the load capaci-

tor is chosen so that across all the corners, frequency of oscillation is close to 20MHz.

The oscillator will have comparatively less delay at ff corner, so at ff corner, it needs more number of bits in the capacitive bank and at ss corner, it has smaller delay so it needs less number of bits or less capacitance to achieve 20MHz frequency of oscillation. The fixed capacitor value is chosen as 97fF capacitance and the value of the variable capacitor, that is the capacitor in the capacitive bank value was chosen to be 8.03fF, so that with 2 bits, we will get 20MHz at ff corner and with 29 bits, we will get 20MHz at ss corner.

Here the constant voltage Vbiasp given to the current source transistors in the current biased inverters is generated from the Band Gap Reference circuit.

2.2.4 Band Gap Reference circuit

To reduce the variation across temperature variations, a constant current source is required, and thus BGR is required. Band Gap Reference circuit gives the voltage or current independent of temperature by combining or adding the two temperature coefficients positive and negative temperature coefficients. Thus, the BGR reference voltage is the sum of the negative temperature coefficient voltage and the positive temperature coefficient voltage as shown in the figure 2.5. So, BGR is made up of CTAT and PTAT circuits that can compensate each other to provide a constant voltage regardless of the change in temperature.

When current passed through the diode, the voltage across the diode is equal to $V_T ln(\frac{I_0}{I_s})$ which is inversely proportional to the temperature. To get the current which is directly proportional to the temperature, the difference in the voltages of the diode and the diode of 8 times the area of the diode taken. This will give the voltage that is directly proportional to the temperature which is $V_T ln(8)$. By adding

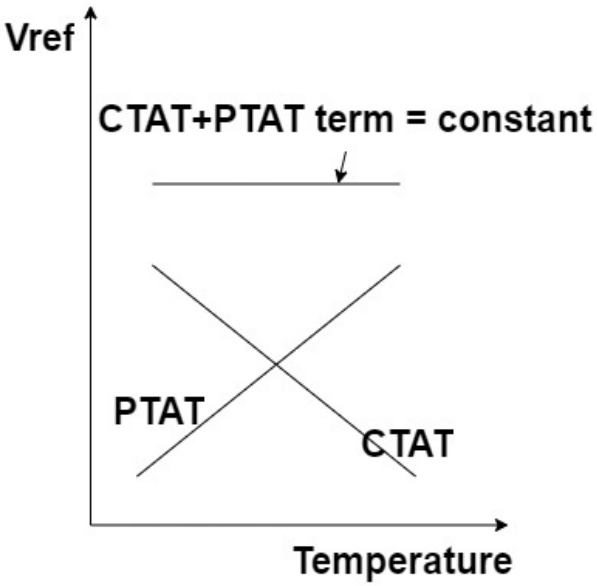

Figure 2.5: Combination of CTAT and PTAT graph

these two voltages which is both positive and negative temperature coefficient, we can get the zero-temperature coefficient. For this to work, the current in the both of the diodes should be same which is $\frac{V_T ln(8)}{R}$ where R is the resistor to get the difference in the voltages of two diodes whose voltage is of positive temperature coefficient.

As shown in the figure 2.6, the current through the resistor R0 will have positive temperature coefficient, i.e., the current is directly proportional to the temperature, and the current through R1, R2 will have negative temperature coefficient, i.e., the current is inversely proportional to the temperature. Both the currents are adjusted to have equal temperature coefficients by adjusting the resistor values R1, R0, R2.

The amplifier of the band gap reference circuit is a 2stage differential input amplifier to get sufficient gain for the proper functioning of the circuit. The bias voltage to the current source of the amplifier is taken by mirroring the amplifier output voltage using the transistors M10 and M11. The sizes of the transistors are taken such

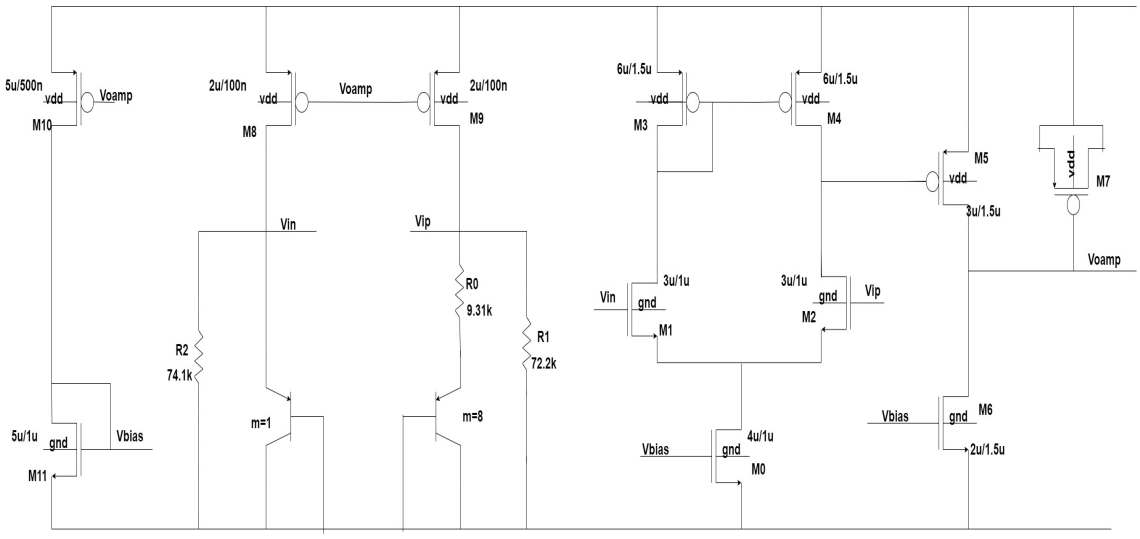

Figure 2.6: Bias voltage generation using Band Gap Reference circuit

that enough current is driven through amplifier to make all the transistors to drive into saturation. Here as the amplifier is used in the bandgap reference circuit, which is operating at dc voltage, bandwidth becomes no constraint. The W/L ratios of the transistors are chosen such that all the transistors are to be in saturation. The lengths of the transistors are increased to get enough gain to the amplifier such that the difference between Vin and Vip is kept low as much as possible. Here MOS capacitor is placed at the output of the amplifier connected to VDD to make the amplifier stable. The capacitor is made by using MOS transistor instead of metal capacitor to reduce the area of the chip. The output of the amplifier is given to the current transistors of inverters in the ring oscillator circuit for the biasing of the inverters. Here for the proper start up of the circuit, slight variation in the resistance was placed between resistors R1 and R2.

Here as the core 3-stage Ring Oscillator has the negative temperature coefficient and as the current increases, frequency increases, so Band Gap Reference circuit is designed such that the current through the transistor M9 has some positive temperature coefficient of 3.7nA/deg Centigrade as shown in the figure 2.7.

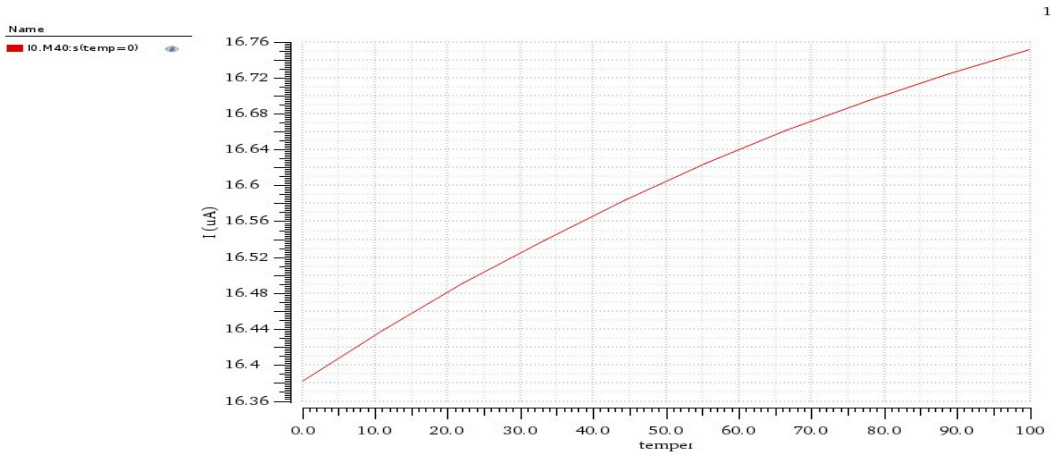

Figure 2.7: Temperature Coefficient of Current Source(BGR)

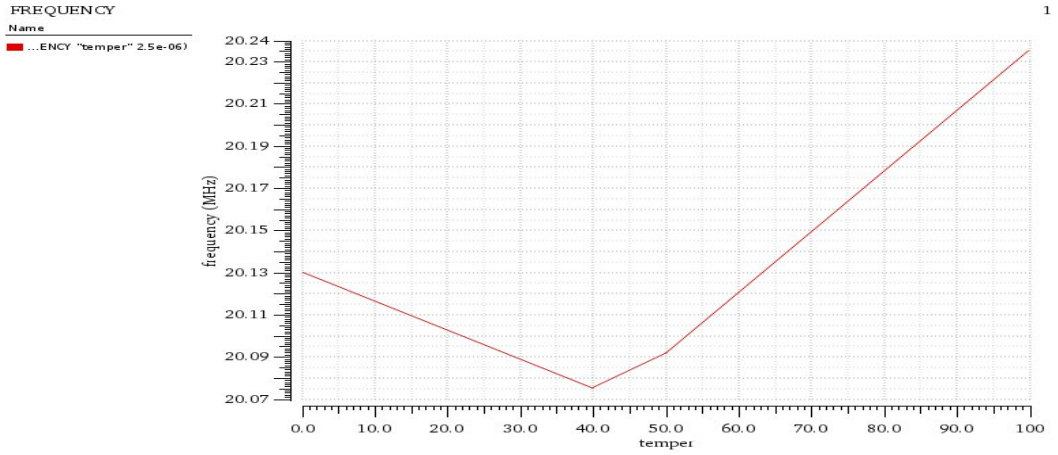

Figure 2.8: Frequency of the ring oscillator with respect to the temperature

Here after giving the voltage from Band Gap Reference circuit, from the figure 2.8, the frequency varies from 20.07 to 20.23 as shown in the above figure. The above graph is simulated at typical corner with the supply voltage of 1V.

But with the voltage variations, the supply voltage is varied from 1.1 to 1.4Volts,

and the variation of the frequency of oscillation is very high as shown in the figure 2.9

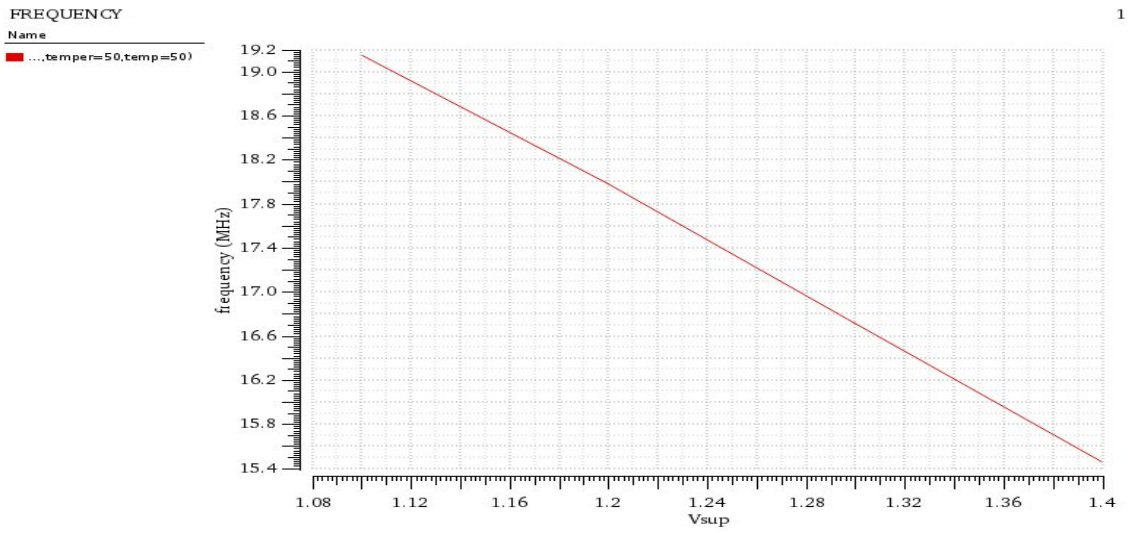

Figure 2.9: Frequency of the ring oscillator with respect to the supply voltage

The above graph is plotted at typical corner and 50 deg centigrade.

We know that the delay of the oscillator T_{osc} is $T_{osc} = 2 * N * T_D$ where T_D is the delay of the inverter and N is the no. of inverters, here in our case, as it is 3-stage CMOS Ring Oscillator, N = 3. The expression for the delay of the inverter is given by $T_D = \frac{C_L V_{DD}}{2I_D}$ where I_D is the current through the inverter and C_L is the capacitance of the load capacitor. So the frequency of the oscillation can be written as shown in the equation 2.2.1. From the equation 2.2.1, the frequency of oscillation is inversely proportional to the supply voltage V_{DD} which justifies the plot as shown in the figure 2.9

$$f_{osc} = \frac{I_D}{NC_L V_{DD}} \tag{2.2.1}$$

So, as the supply voltage changes, the frequency of the oscillation changes and

the variation is very high. So in order to supress the variation of the frequency of oscillation with supply voltage variations, Low Drop Out voltage regulator is used.

2.2.5 Low Drop Out Voltage Regulator

In order to reduce the variation of the frequency of oscillation with supply voltage, LDO is used.

A low-drop-out regulators (LDO) is one of the most common voltage regulators. As its name suggests, An LDO supports very small drop-out, the voltage difference between input and output voltage, by using P-MOSFET power transistors. The small drop-out voltage improves power efficiency. An LDO uses negative feedback control to regulate its output voltage. First, it detects the voltage error, i.e., the voltage difference between output voltage and reference voltage. Based on the error, its controller produces voltage to determine the amount of current to supply and adjust its resistance. Then, power transistor produce current required for its load.

LDO consists of an amplifier and one large P-MOSFET power transistor. The amplifier has two inputs from reference voltage and output voltage, whether they are scaled by a resistive divider or not. The amplifier produces analog voltage output which is proportional to the differential input voltage. The output voltage of the amplifier is applied to the gate of single large PFET power transistor to adjust V_{GS} of the transistor, thus current provided from the power transistor. Large gain from the amplifier and power transistor allows a wide range of supply current with only small error voltage. High bandwidth of feedback control loop in analog LDOs allows to regulate large load current change without having large compensation and output capacitors.

In the figure 2.10, LDO schematic was shown. The LDO is used to maintain the

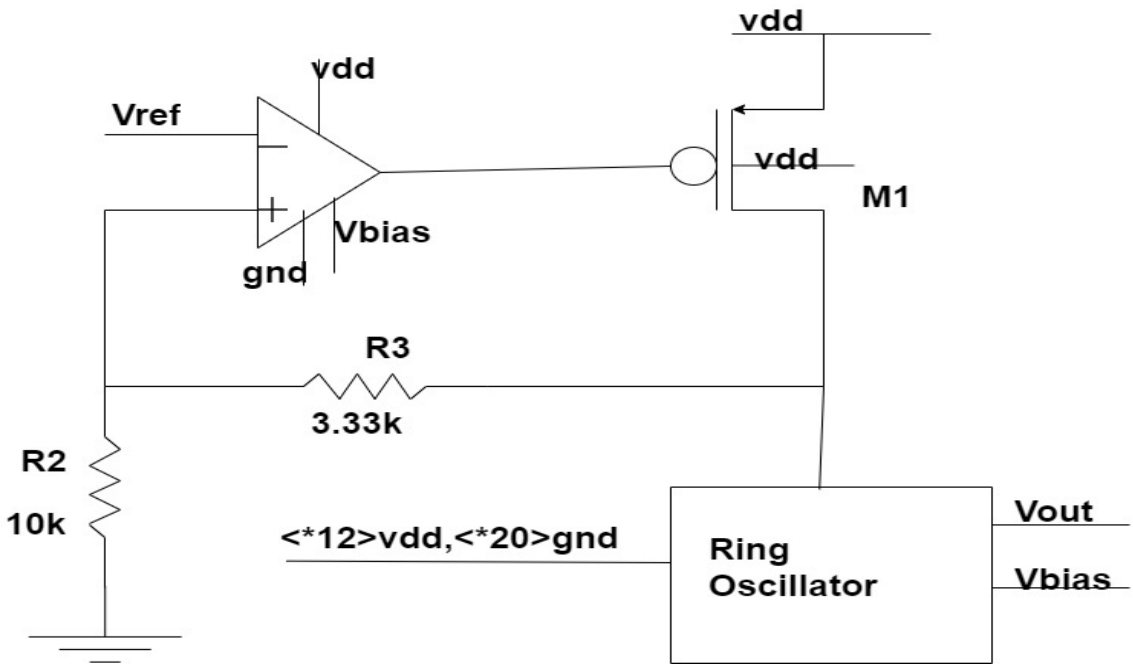

Figure 2.10: Block Diagram of LDO

vdd of the ring oscillator to 1V even with the variation of the supply voltage. The transistor M1 is the pass PMOS transistor which pushes the current through the load which is ring oscillator in our case. In LDO single stage amplifier is used as an amplifier whose gain is enough just to make the error voltage low. Here resistive feedback is used to amplify the reference voltage from 0.75V to 1V at the output of the LDO which becomes the V_{DD} to the Ring Oscillator. The feedback factor which is equal to the ratio of Vpos/Vout is R2/(R2+R3) where Vpos is the voltage at the positive terminal of the amplifier and the Vout is the output voltage taken at the drain of M1. The bias voltage to the amplifier in the LDO is also taken from the same Band Gap Reference circuit so that nearly constant voltage is maintained across all the corners and also to reduce the extra circuitry.

Here the Ring Oscillator acts as load to the LDO where the output of the LDO acts as vdd to the ring oscillator. The supply voltage to LDO is varied from 1.1

to 1.4 volts to maintain the output voltage at 1V. The (W/L) ratio of the PMOS transistor is kept large so that the drop Vsd across the transistor was made low. The reference voltage is chosen to be 0.75 volts and is amplified to 1V to the output of LDO, so as to meet the common bias voltage required for the input of the differential amplifier of the LDO.

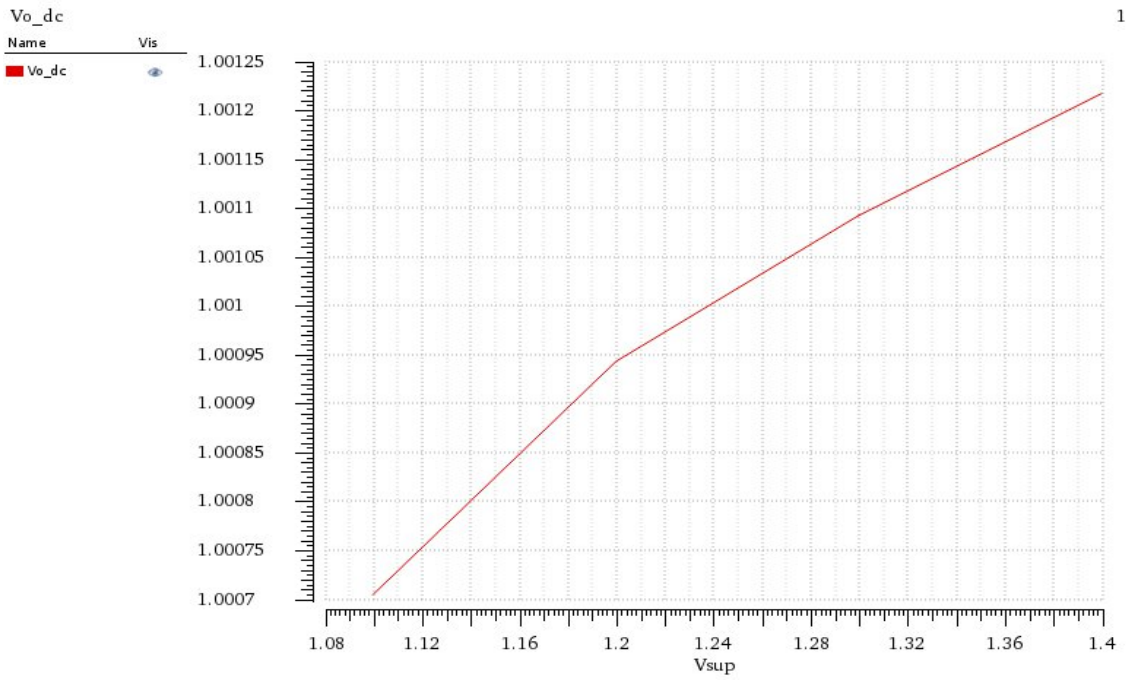

Figure 2.11: Output voltage of LDO versus Supply voltage

As shown in the figure 2.11, the output voltage of the LDO with respect to the supply voltage that varies from 1.1 to 1.4 volts, where the output voltage is very close to 1V. Above LDO characteristics are simulated at typical corner, 50deg centigrade with the reference voltage of 0.75volts.

2.2.6 Reference Voltage Generator

The reference voltage chosen is 0.75 volts and to realize the reference voltage generator using CMOS process, we use Band Gap Reference circuit. The current which is constant in the above Band Gap Reference circuit is converted into voltage by using current mirror M14, M15 and the resistor R3. Here cheap cascode technique is used for the PMOS transistors in the Band Gap Reference circuit as shown in the figure 2.12

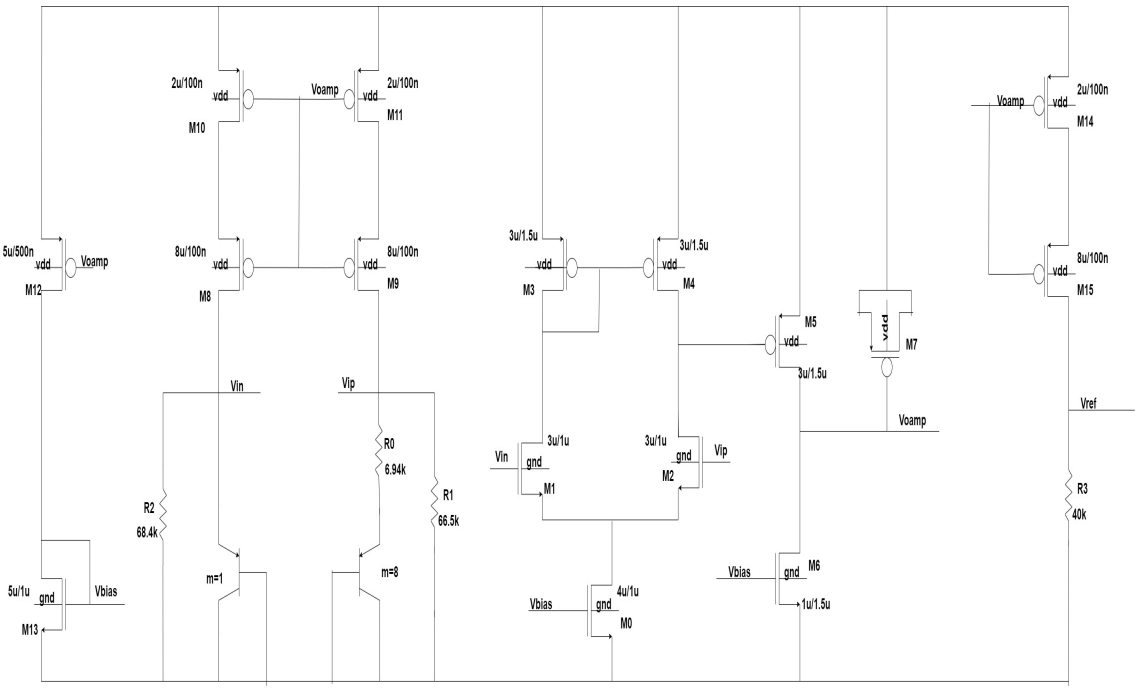

Figure 2.12: Reference Voltge Generator circuit

Here cascode technique is used to reduce the current error while mirroring the current to generate the voltage using the resistor R1.

Cascode circuit

The cascode is a two-stage amplifier that consists of a common-source stage feeding into a common-gate stage. Cascode technique have several advantages such as higher gain, higher output impedance, etc. Here the gate of the two transistors in cascode is connected to avoid the external circuit to generate the bias voltage to the cascode transistor. The cascode technique is as shown in the figure 2.13

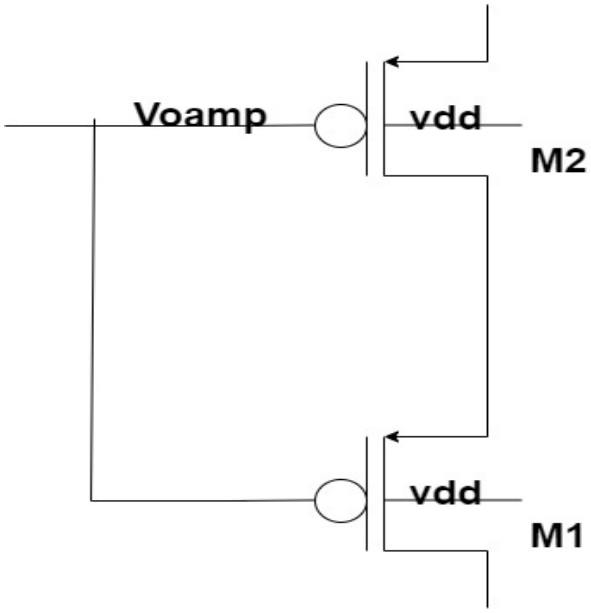

Figure 2.13: Cascode circuit

Here the common source transistor and common gate transistor is driven with same gate voltage. The cascode transistor should have higher (W/L) and lower Vt for both of the transistors to be in saturation. The condition for the common source transistor to be in saturation is Vd$\leq$Vg+|Vt| and so drain voltage of the common source transistor will be lesser than the drain voltage required for saturation to make sure the common source transistor is in saturation. Now for the voltage required for the gate to be ON is Vsg $\geq$ |Vt|. So, the cascode transistor should have less Vt as much as possible, so that the voltage required for the gate of the cascode

transistor will be close to the gate voltage of common source transistor. As Vgs = Vt + $\sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}$, Vgs will be equal to Vt only when (W/L) is large. So, the cascode transistor has larger W/L and smaller V_t for both of the transistors to be in saturation. This technique helps to avoid the extra circuit needed for the generation of the bias voltage for the cascode transistor.

The reference voltage is generated using the resistor and the current mirrored from the Band Gap Reference circuit as shown in the figure. The value of the resistor is chosen such that the voltage at the output of Vref is equal to 0.75 volts.

After giving the reference voltage from the Reference voltage generator to the LDO which has load as the ring oscillator, the Reference voltage is very close to 0.75volts as shown in the figure 2.14

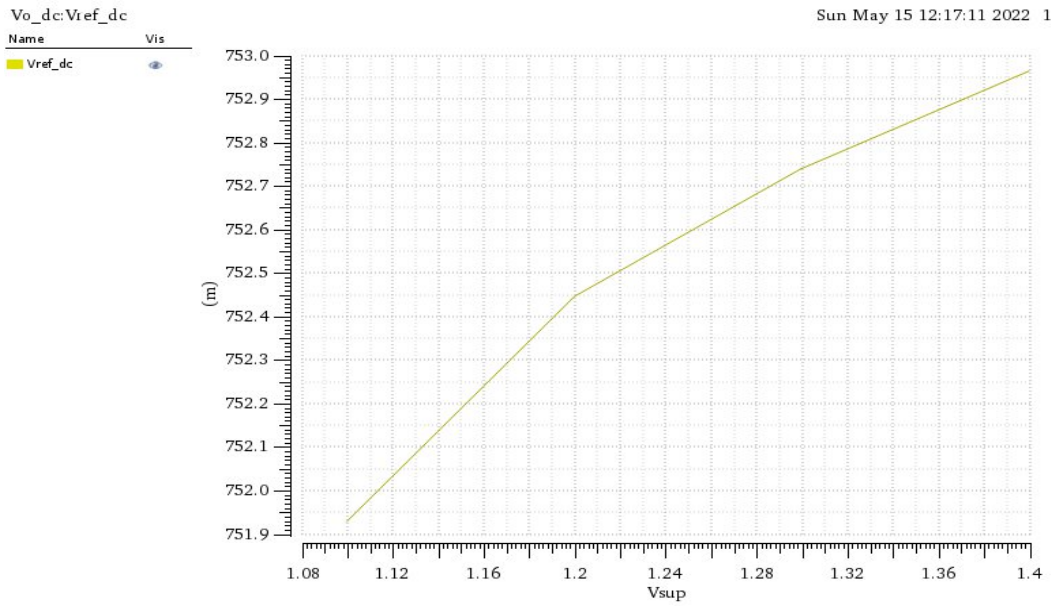

Figure 2.14: Reference voltage versus Supply voltage

The output voltage of the LDO by varying the supply voltage is as shown in the

figure 2.15

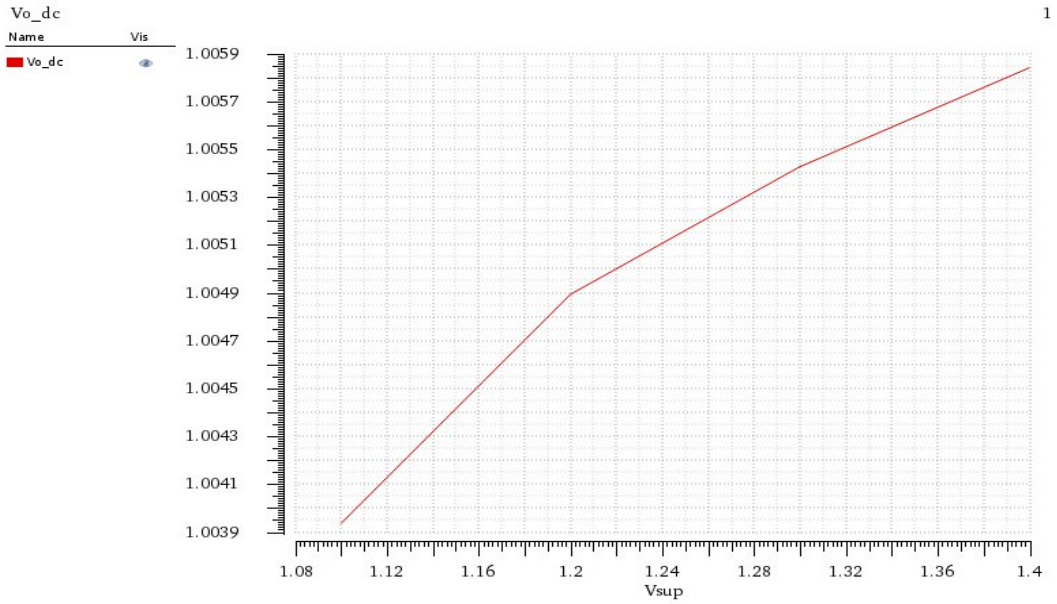

Figure 2.15: Output voltage of LDO versus Supply voltage

The circuit is simulated with the supply voltage varying from 1.1 to 1.4volts at typical corner 50deg centigrade. As shown in the above figure, the reference voltage is close to 750mV and the output of the LDO is very close to 1V.

2.2.7 Ring Oscillator

By adding all the above blocks, the final schematic of the CMOS Ring Oscillator is as shown in the figure 2.16

The output reference voltage from the Reference voltage generator is given to the negative terminal of the amplifier of LDO and the core Ring Oscillator is as the load to the LDO and the output of the Ring Oscillator is taken at the output of the

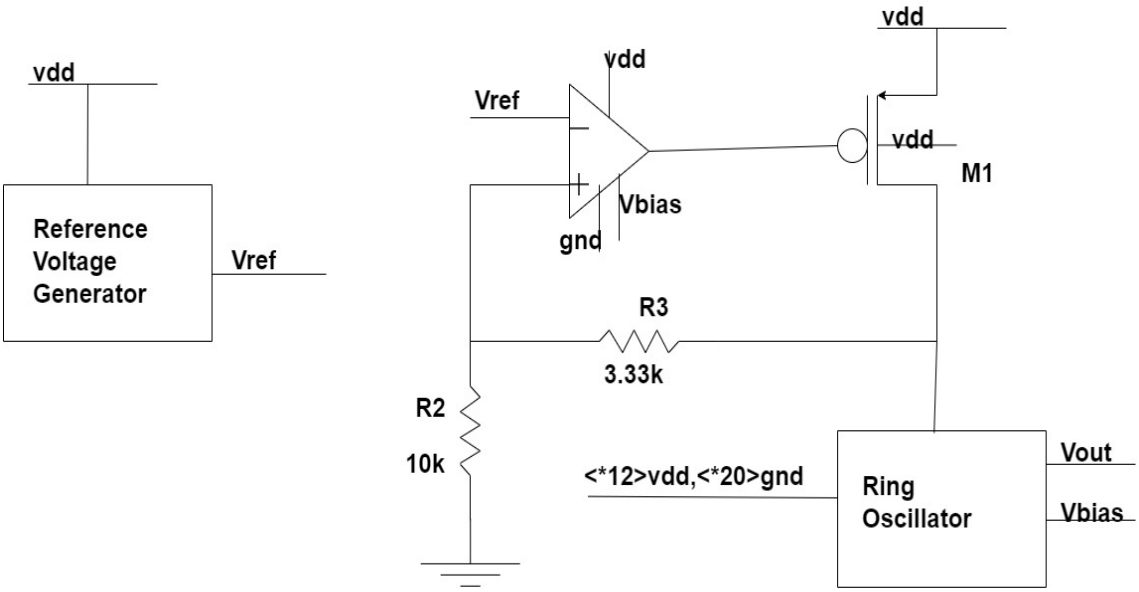

Figure 2.16: Schematic of the CMOS Ring Oscillator

Ring Oscillator block Vout as shown in the figure.

The above circuit is simulated with the supply voltage varying from 1.1 to 1.4volts at all temperatures varying from 0°C to 100°C across all the corners. The frequency of the Ring Oscillator is close to 20MHz at all corners and all the temperatures and the results are shown below.

Chapter 3

Results

Layout

The layout of the complete ring oscillator is shown in the figure 3.1. The dimension of the realized layout is 155.85μm x 62.96μm.

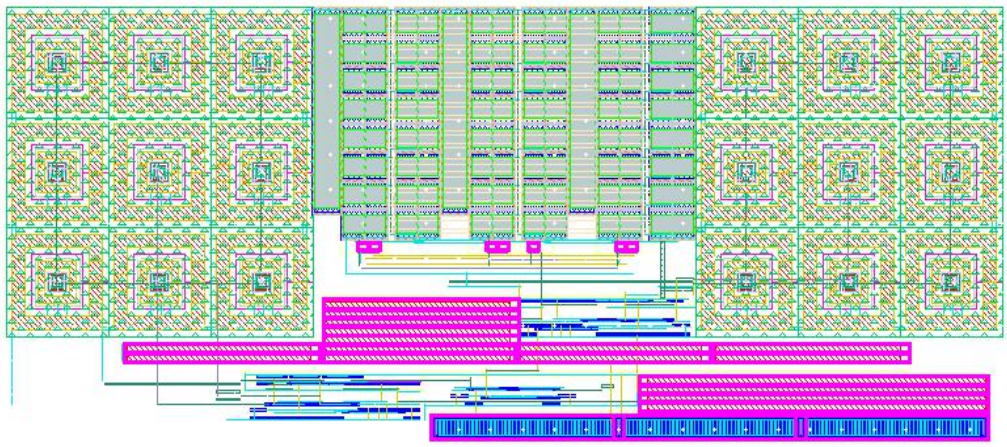

Figure 3.1: Layout of the ring oscillator

The simulations were done with supply voltage varying from 1.1 to 1.4volts and with the temperature ranging from 0 to 100°C across all the corners.

The below graphs shows the waveforms at typical corner, 50°C.

The average power consumption of the complete ring oscillator at typical corner, 50°C is 285.5μA.

Transient waveform

The below waveform shows the transient sine waveform at the output of the ring oscillator at the output of the 3_rd inverter.

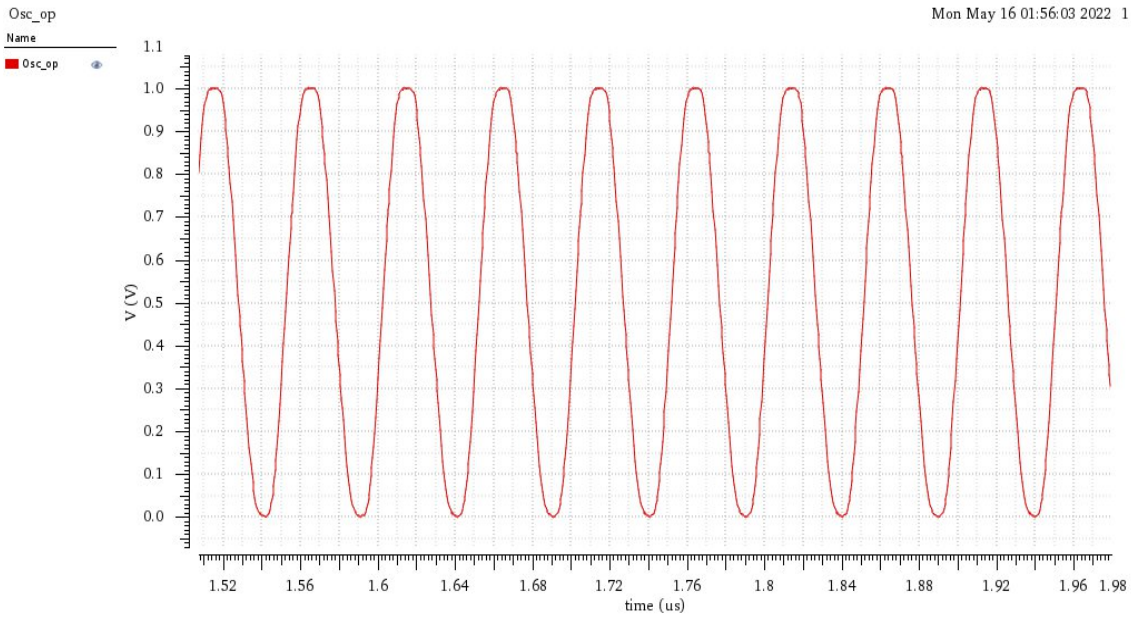

Figure 3.2: Transient output waveform of the ring oscillator

Frequency of Ring Oscillator

The below plot shows the frequency of the ring oscillator with respect to the time

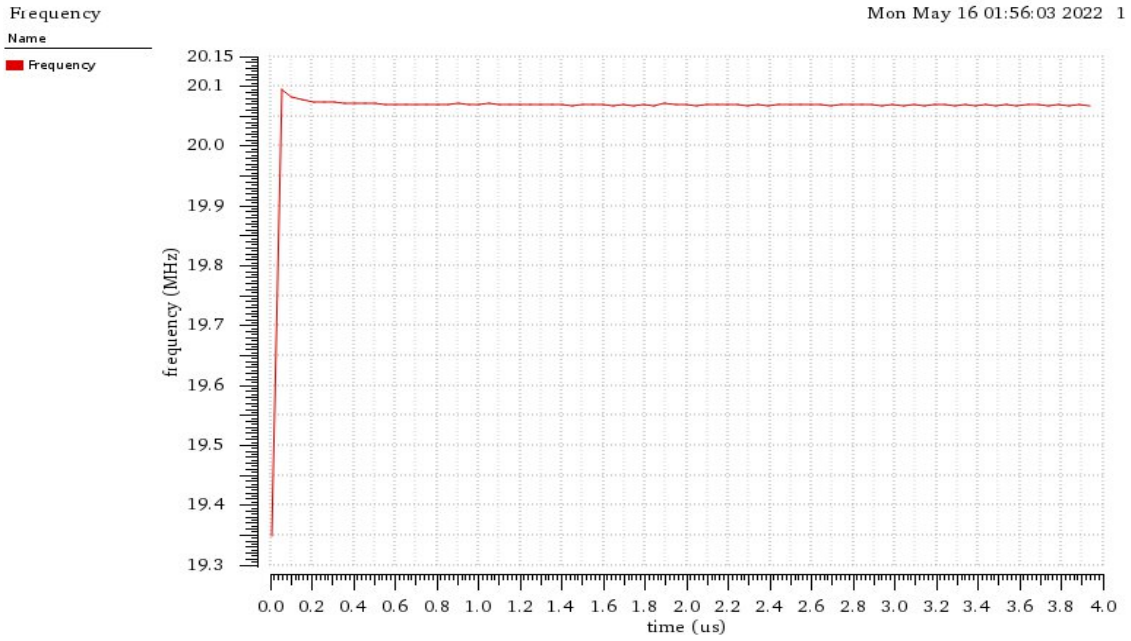

Figure 3.3: Frequency of ring oscillator with respect to time

The above plot shows that the frequency of oscillation is close to 20MHz

Phase Noise of Ring Oscillator

The below plot shows the Phase Noise of the Ring Oscillator at tt corner, 50°C temperature.

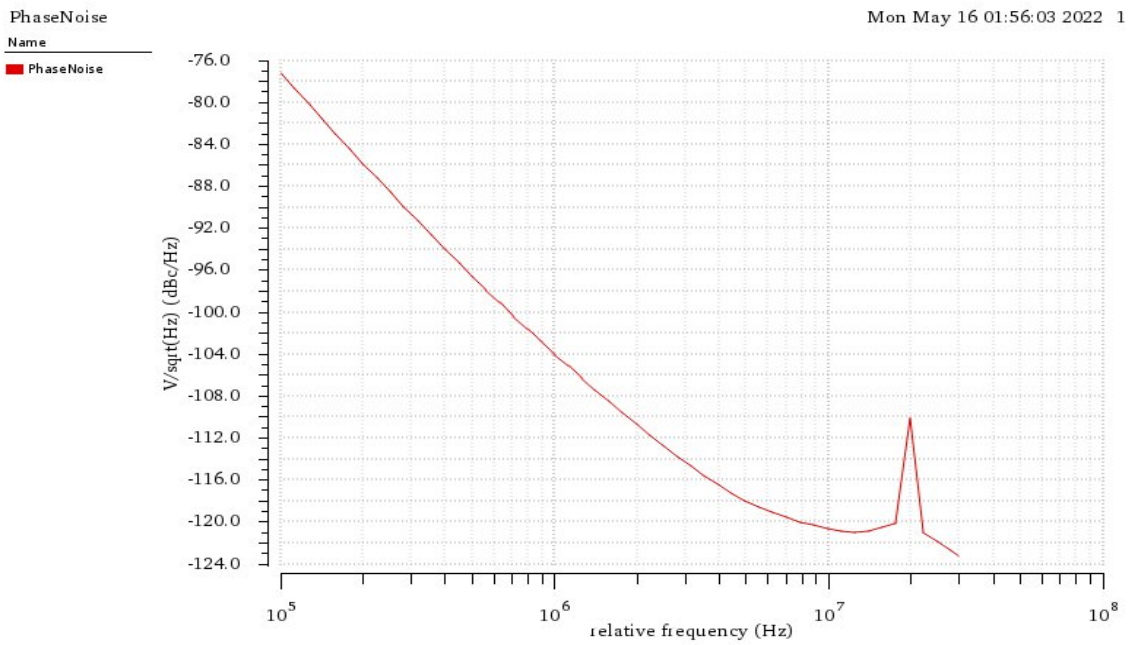

Figure 3.4: Phase Noise of the ring oscillator

Results at all corners, temperatre and supply voltages

The table showing the frequency of operation noted at tt, mos_tt, mos_ff, ss, ff corners as shown in the table 3.1.

Table 3.1: Frequency of operation at different corners

Supply Voltage	Corner	No. of Bits	0°C	50°C	1000°C
1.1	tt	12	20.11	20.06	20.16
1.1	mos_ff	16	20.36	19.87	19.52
1.1	ff_lib	29	20.49	20.06	19.76
1.1	ss_lib	02	19.53	19.90	20.4
1.1	mos_ss	09	19.41	19.78	20.3
1.2	tt	12	20.13	20.06	20.14
1.2	mos_ff	16	20.39	19.86	19.49
1.2	ff_lib	29	20.52	20.05	19.72
1.2	ss_lib	02	19.54	19.91	20.41
1.2	mos_ss	09	19.42	19.79	20.31
1.3	tt	12	20.14	20.06	20.13
1.3	mos_ff	16	20.40	19.85	19.46
1.3	ff_lib	29	20.53	20.04	19.70
1.3	ss_lib	02	19.54	19.90	20.40
1.3	mos_ss	09	19.42	19.78	20.31
1.4	tt	12	20.14	20.05	20.12
1.4	mos_ff	16	20.41	19.84	19.45
1.4	ff_lib	29	20.53	20.03	19.68
1.4	ss_lib	02	19.55	19.90	20.40
1.4	mos_ss	09	19.42	19.78	20.30

Therefore from the table 3.1, the frequency variation is from 19.41MHz to 20.53MHz which is $\pm$ 2.95% across all the corners in the temperature range of 0°C to 100°C and supply voltage is from 1.1V to 1.4V.

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