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ENERGY EFFICIENT AND WIDE RANGE SERDES

A Project Report

Submitted by

MUKUND M

In the partial fulfilment of requirements

For the award of the degree

Of

MASTER OF TECHNOLOGY

June 30, 2021

DEDICATION

To my beloved family

CERTIFICATE

This is to undertake that the project report titled **ENERGY EFFICIENT AND WIDE RANGE SERDES**, submitted by me to the Indian Institute of Technology Madras for the award of M.Tech, is a bonafide record of the research work done by me under the supervision of Dr. Saurabh Saxena. In whole or in parts, the contents of this project report have not been submitted to any other Institute or University for the award of any degree or diploma.

Place: Chennai 600 036

Date: 30th June 2021

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EE19M078

Prof. Saurabh Saxena

Project Guide

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I wish to thank my friends for helping me get through the difficult times and for all the emotional support, entertainment, and care they provided during my MTech. Finally, I dedicate this work to my family members for their sacrifice, cooperation, support, affection, and patience shown during the course work, making it possible to complete this work on time.

Thank you all MUKUND M

ABSTRACT

Today, links such as PCIe, HDMI, USB are used everywhere. These are some examples of link standards used for data communication. This is achieved by using a SerDes (Serializer/Deserializer). A SerDes implementation includes parallel-to-serial (serial-to-parallel) data conversion, impedance matching circuitry, and clock data recovery functionality. The primary role of SerDes is to minimize the number of I/O interconnects. To implement a full SerDes system, we also need other blocks such as Phase Locked Loop, Delay Locked Loop, output drivers, equalization circuits and CDRs (clock and data recovery circuits).

The goal here is to transmit 21 bits of data by using 3 lanes, each employing a 7:1 serializer and 1:7 deserializer. This project work focuses mainly on designing a wide range Phase Locked Loop (PLL). PLL is a negative feedback system used to generate stable clock signals which are locked to a clean reference. The PLL output signal is fed to LVDS (Low Voltage Differential Signalling) and CML (Current Mode Logic) output drivers for testing purposes as a standalone IC (Integrated Circuit) . It is designed with a reference clock varying as 15-75MHz giving an output clock signal varying as 105-525MHz with 3-30ps R.M.S jitter.

This PLL is used to generate clocks for the serializer and synchronizer used in the transmitter as well as the deserializer and CDR used in the receiver. A startup circuit is implemented to enable the DLL to work across wide range of frequencies and the transmitter results are discussed.

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ABBREVIATIONS

IITM	Indian Institute of Technology Madras
IC	Integrated Circuit
PLL	Phase Locked Loop
PFD	Phase Frequency Detector
CP	Charge Pump
LF	Loop Filter
FF	Flip Flop
VCO	Voltage Controlled Oscillator
LVDS	Low Voltage Differential Signalling
CML	Current Mode Logic
VCDL	Voltage Controlled Delay Line
TX	Transmitter
RX	Receiver
NTF	Noise Transfer Function
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square
PSNR	Power Supply Noise Rejection

CHAPTER 1

INTRODUCTION

1.1 Motivation

Chip area and number of pins are 2 major factors which decide the cost budgeting of a chip. In applications like data communication, this is very important since we generally have to deal with multiple bits. This motivates the use of a SerDes system which greatly minimizes the number of I/O ports and enables the use of minimum number of lanes. In this case we have 21 bits divided into 3 lanes, each having 7 bits. Another advantage of using a SerDes system is that we can transfer the data at higher speeds and then de-serialize it to its original data rate. An example in this case is the data rate of incoming bits is 75Mbps and the serialized data rate of a particular lane is 525Mbps. This also helps to minimize the latency associated in data communication applications.

In summary, we utilize SerDes for the conversion of incoming parallel data into serial data. We transmit this input data via a physical channel like fiber, copper-twisted pair, or even a back-plane. The data that we receive is serial data via our physical channels, and the receiver converts this data back into parallel data. The overall process affords designers the ability to increase data transmission speed between two points within a system without the need for additional pins on a component.

To enable all this, we need a good Phase Locked Loop to generate all the required clock frequencies. This will make the task of designing a Serdes much easier. Thus a PLL is the block capable of generating a stable clock with the desired frequencies. We will also be using a LVDS output driver since it is an efficient method of transmitting data. This is efficient in the sense that differential signalling eliminates the common mode noise on the line and also we can conserve power by limiting the transmitted voltages (here upto 400mV amplitude). So by transmitting only 400mV amplitude instead of the 1.8V supply voltage in the technology, a lot of power is saved in the TX drivers.

1.2 Outline

The thesis mainly focuses on the PLL design part and the results. The PLL chip is taped out with 2 output drivers (CML and LVDS). A startup circuit is used to ensure that the PLL starts across all corners(FF-SS and -40°C to 125°C) . 2-bit control is used in the regulator to make it work across the wide frequency range. Block level and chip level results are discussed.

The startup system for the DLL is designed which enables the DLL to operate across a wide reference frequency range.The transmitter is integrated and the results of the DLL and TX are discussed.

Chapter 2 gives a overview of the entire SerDes system.

Chapter 3 dives into the PLL details and results.

Chapter 4 deals with the DLL and overall TX part.

CHAPTER 2

SerDes system level Overview

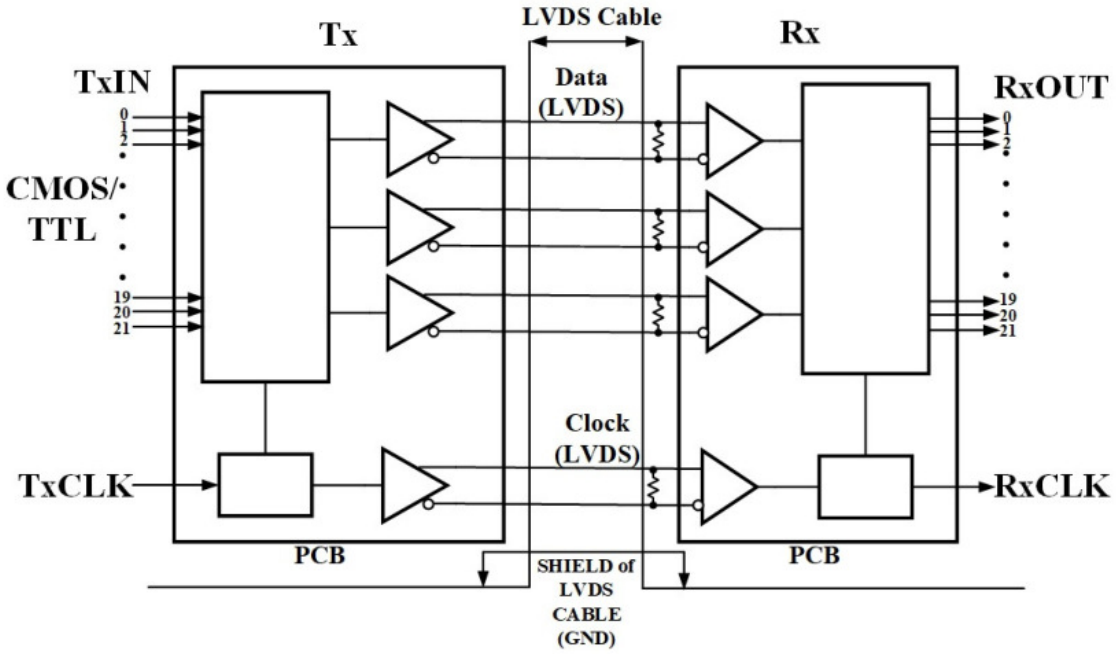


Fig. 2.1: SerDes System

The block diagram in Figure 2.1 shows the SerDes system to be designed in this project. It consists of 21 data inputs of 3.3V which are first level shifted to 1.8V signals. Then 7 signals are lumped together and serialized into a single bit stream to be transmitted through the cable. The transmit medium and output drivers use Low Voltage Differential Signalling scheme (LVDS). This transmitter follows a clock forwarded architecture and hence the low frequency reference clock is forwarded using a 4^{th} transmit lane.
The receiver side first has a front-end block to amplify the received signal followed by a clock and data recovery circuit. After we have recovered the data and clock, they are fed to the deserializer to recover the original bit stream of data.

2.1 Transmitter

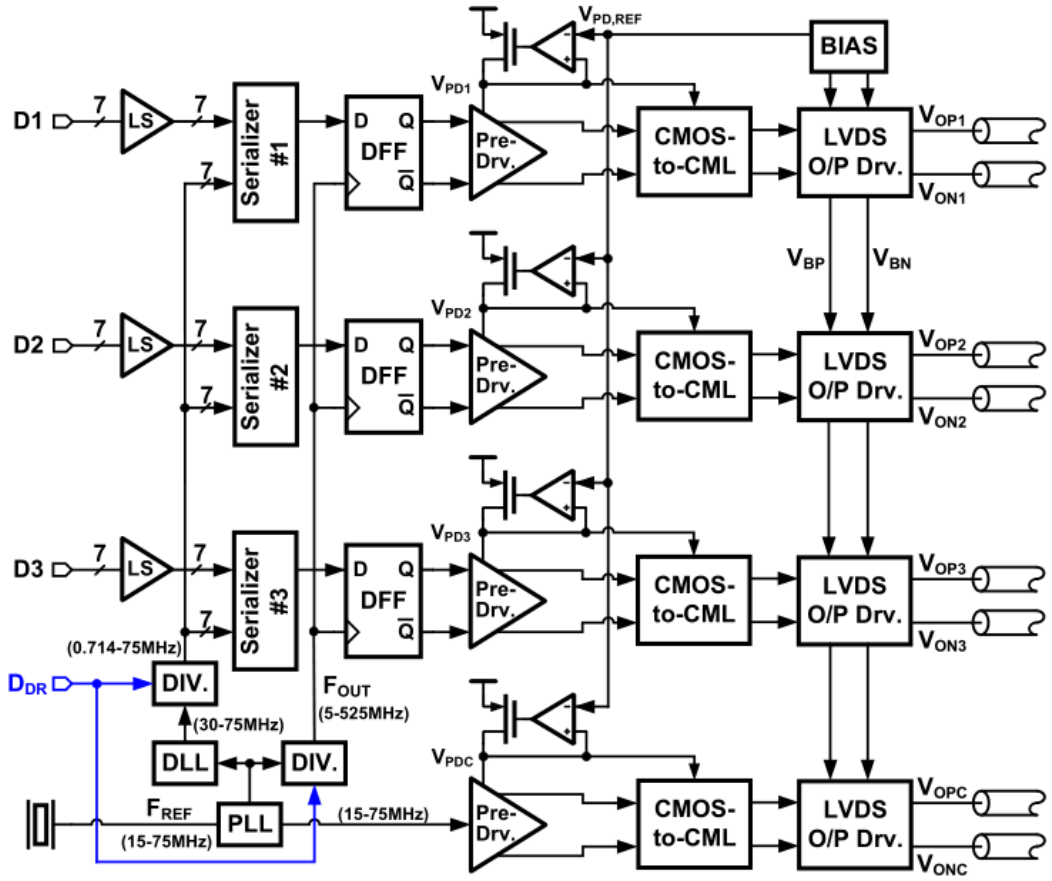


Fig. 2.2: Transmitter components

Figure 2.2 shows the transmitter components in more detail. Here a PLL is used to generate the clocks to DLL and synchronizer from a low frequency reference ranging from 15-75MHz. Dividers are used to give the correct clocks to the synchronizer and the DLL, since we need a low frequency clock for the DLL reference and a high frequency clock for the synchronizer. The DLL is used to generate the 7 phases required for serializing the data. The DLL output has dividers since the DLL operating range is not very high. By the use of dividers the frequency range of the phases are extended according to the specification. The synchronizer is used to align the data at the rising edge of the high speed clock. The blocks that follow the synchronizer are part of the output driver. We have a regulated pre-driver followed by CMOS to CML logic conversion block. These signals are finally given to the LVDS output driver to be transmitted to the load. The clock is forwarded at low frequency to save power.

2.2 Receiver

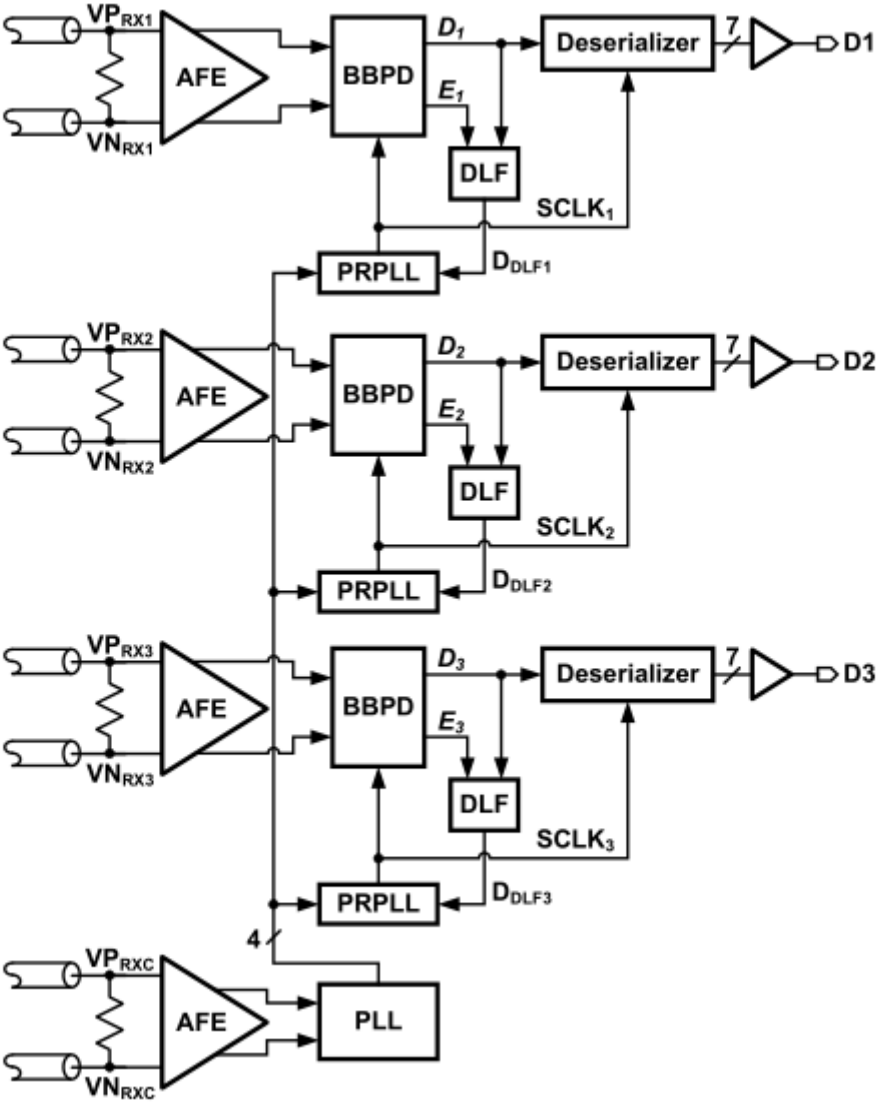


Fig. 2.3: Receiver components

The receiver block consists of an analog front end which acts as an equalizer in this case. This block has amplifiers which convert the received signal to full scale voltage. Thus we can feed full scale signals to the clock recovery block. The clock recovery is done using the received clock, which is multiplied using a phase rotating phase locked loop (PRPLL) to generate the high frequency clock. This recovered clock is fed to the phase detector along with the amplified data. The phase recovery loop uses a Bang Bang phase detector (BBPD) or a digital phase detector. Since the BBPD gives only digital

outputs, a digital loop filer (DLF) is used to generate the control for the VCO (voltage controlled oscillator) in the PRPLL. Thus clock and data recovery is performed.
The resulting data and clock are fed to the 1:7 deserializer. This block converts the single bit stream into the original 7 bit streams. The job of the receiver is to recover the transmitted data with minimum bit errors.

CHAPTER 3

Phase Locked Loop

A wide-range PLL is designed and taped out as a part of this project. The design specifications of the PLL is shown in the table below.

Description	**Specification**
Technology	SCL 180nm
Supply Voltage	1.8V
Reference Clock	15-75MHz
Output Clock	105-525MHz , Single Phase
$PSNR_{VCO}$	<0dB
R.M.S Jitter	Minimum (<0.5% of Period, Tout)
Power consumption	Minimum
LVDS Spec	400mV amplitude @ fout/2
CML Spec	250mV amplitude @fout

Table 3.1: PLL Specifications

The PLL operates on a low frequency reference of 15-75MHz and gives a output ranging as 105-525MHz. The feedback divider ratio is 7. The PLL follows a traditional charge pump based topology. It consists of a 3 state Nand based Phase Frequency Detector (PFD), 2-bit controlled current steering charge pump to cater to the wide operating range, a type-2 order-3 loop filter and a 2-bit controlled supply regulated VCO. In the below figure R, C1 & C2 form the loop filter. C3 is the supply decoupling capacitor for the VCO. The opamp and the PMOS act as the regulator. (2 bit control is not shown.)

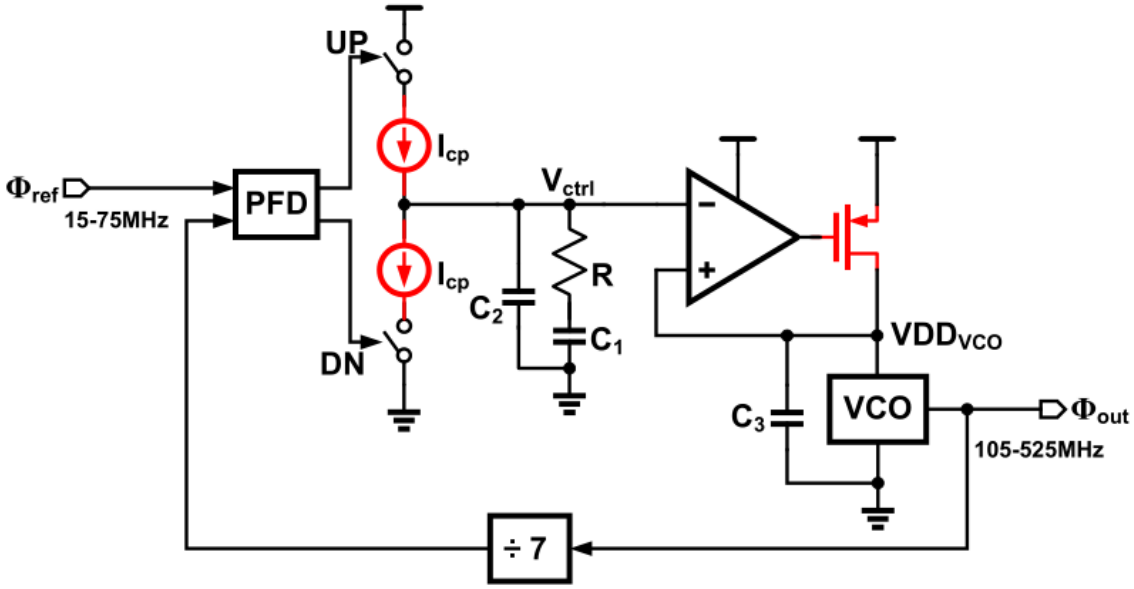


Fig. 3.1: Integer N Charge Pump PLL

MATLAB analysis is done as part of deciding the loop parameters and as a first level verification of the design. The KVCO of the PLL is taken based on previous simulations in the technology. All other parameters are decided from the MATLAB script written to optimize for minimum jitter. The noise contributions of individual components like PFD, CP, VCO are multiplied with their respective Noise Transfer Functions (NTFs) to give it's output noise contribution. This is compared against the simulated results which takes into account that the system is not a truly-continuous time system. Simulated results for 525MHz is as shown. (These results agree well at higher frequency.)

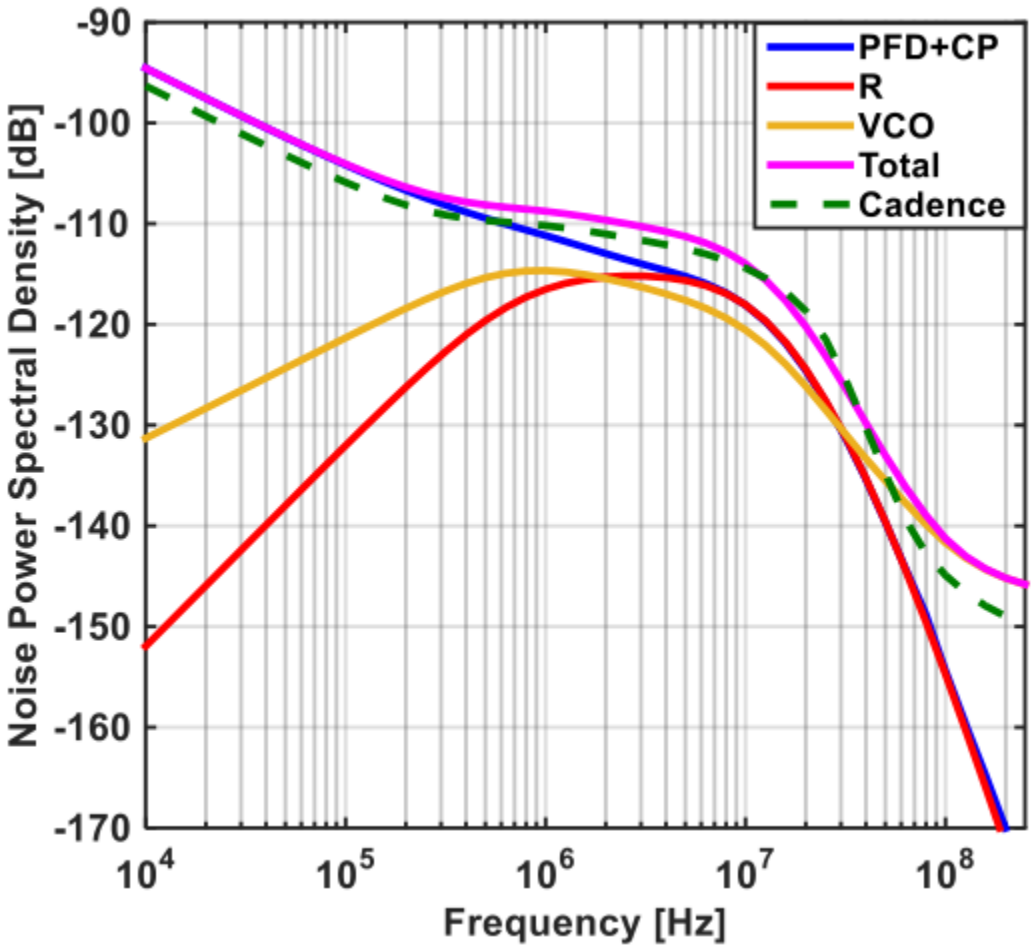


Fig. 3.2: System level simulations

3.1 Design of the PLL

3.1.1 Phase Frequency Detector

The PFD implemented here follows the 3-state PFD topology. It is implemented using NAND gates with 2, 3 and 4 inputs. The three state PFD has 3 states and functions as follows: Consider the 2 input signals reference as R and the feedback as V to the PFD. If R leads V, then we need to make the edge of V arrive faster and thus UP signal is high and DN signal is low and vice versa when R lags V. If both Up and Down are high then the PFD is reset. These are the states of operation of the PFD. It has a linear range of approximately (except dead zones) 4π periodically. The below figure shows how the PFD is implemented in a circuit level.

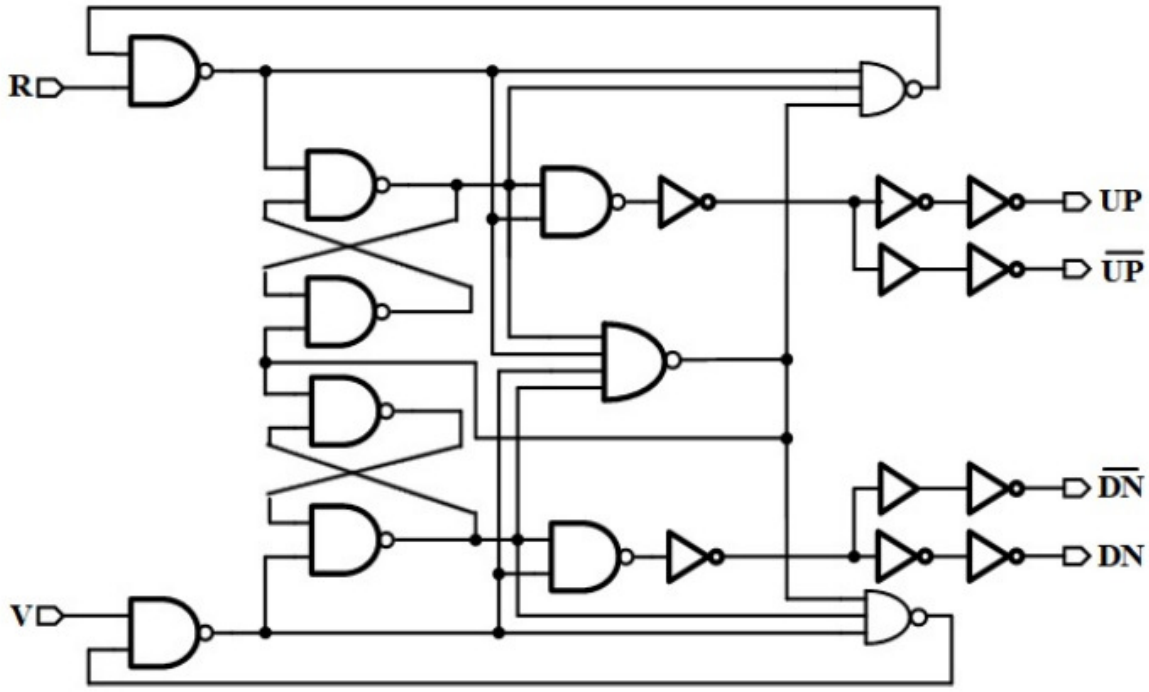


Fig. 3.3: NAND based PFD

The critical factor is the overlap period which causes the jitter from PFD and CP to appear at the output. Also it cannot be too low since the CP will fail to act for low phase differences. This overlap time when the phase difference is 0, is modified by adding a buffer after the 4-input NAND gate.

3.1.2 Charge Pump

The charge pump is implemented as shown in the figure 3.3 below. It is implemented in a differential form to lessen the ripples at the control voltage node. Also the current is always on and steered to either side to minimize the ripples due to switching. Here a 4 bit control is shown but these controls are encoded into a upper level 2 bit control which is in sync with the regulator controls. Thus by using only 2 bits we can operate the PLL in the different frequency settings.

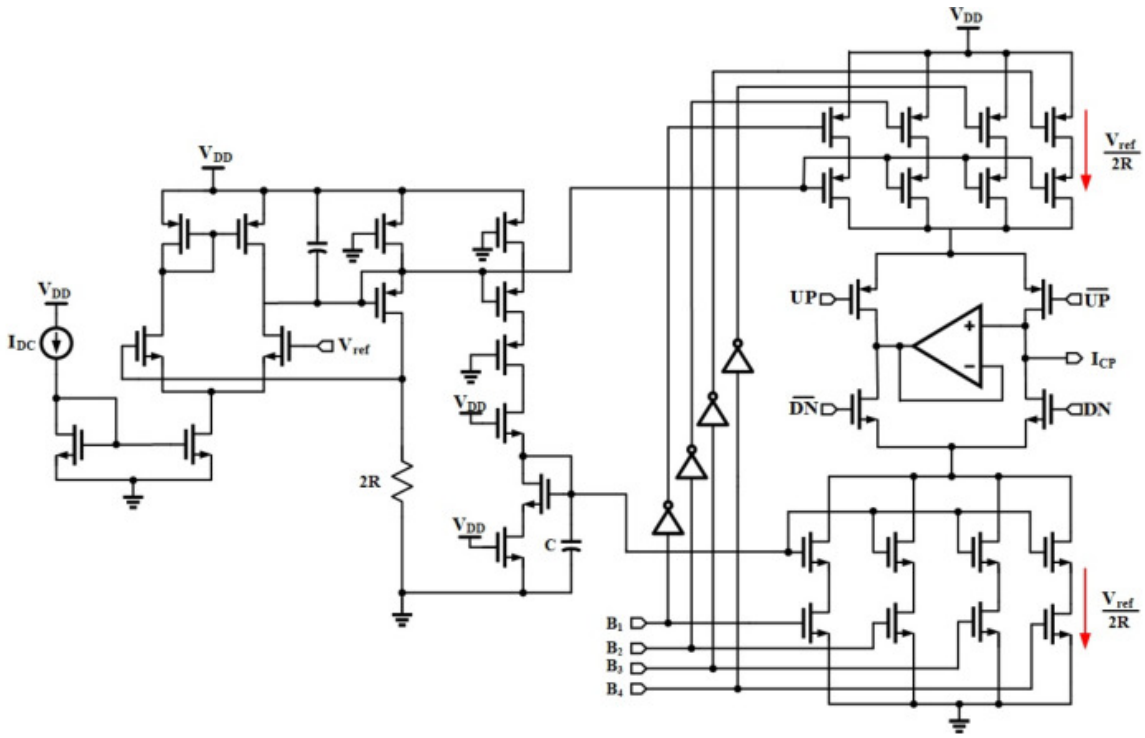


Fig. 3.4: Charge Pump Implementation

The current reference of the charge pump is generated as Vref/2R. This ensures that the charge pump current and the loop filter resistor variations are in the opposite manner. Eg. If the resistor is in the minimum corner then the current is in the maximum corner. Thus PVT variations in the loop are minimized.

The below figure shows the transient results of PFD+CP in series for the zero phase difference case.

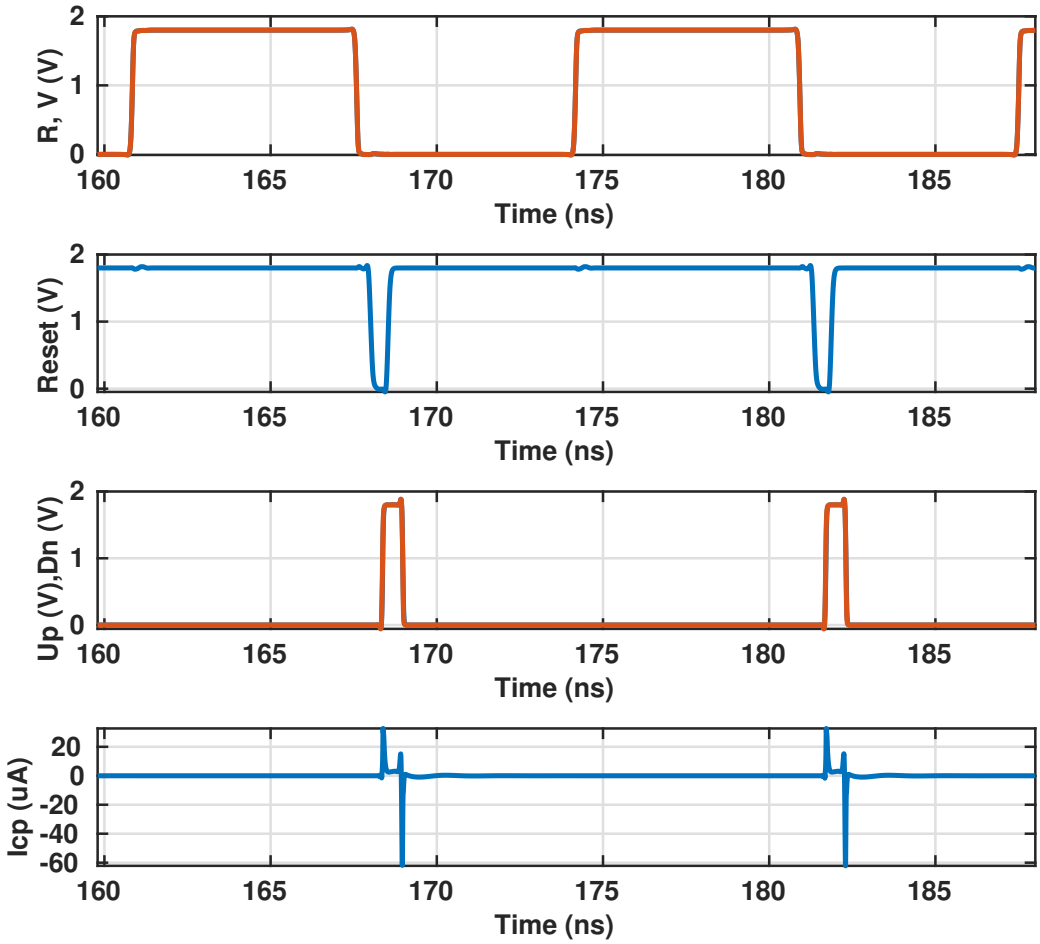


Fig. 3.5: PFD and CP working

The PFD works at the falling edge of its inputs. At zero phase error we see that the UP and DN signals are overlapping for the overlap time and the reset pulse is getting activated. At the same time the charge pump is also activated but the net average current into the loop filter is zero.

3.1.3 VCO and Regulator Design

The regulator loop is as shown in figure 3.1 consisting of the amplifier, PMOS transistor and the VCO. PLL design is started first with the VCO design. This is because the VCO parameters are not easily tunable. Here in 1.8V technology, the VCO is designed to operate from 0.6V to 1.55V across corners. The VCO used here follows a 8 stage

pseudo-differential ring oscillator. The oscillator is followed by ac coupling capacitor and buffers. We can take 4 phases output from this circuit and thereby use it for the receiver side PLL also.

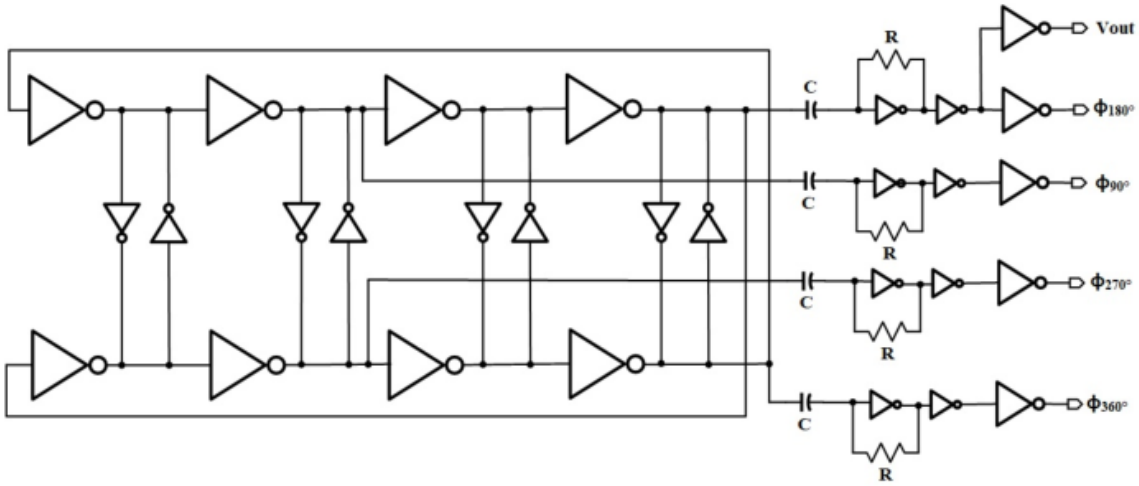


Fig. 3.6: VCO schematic

The operational amplifier used is a simple NMOS input 5 transistor OTA designed to satisfy the voltage range. The PMOS transistor (pass FET) should be able to supply the current for the VCO to function properly and we should maintain the region of operation as saturation across corners. This is not possible with the use of a single transistor which motivates the use of multiple transistors with digital controls. 2-bit active low control is used here.

Reference Frequency Range (MHz)	**VCO code (b1bar b0bar)**
15-30	11
30-45	10
45-60	01
60-75	00

Table 3.2: Regulator Control settings

Stability and PSNR (Power Supply Noise Rejection) are also 2 important factors which characterize the regulator. To evaluate stability, loop gain analysis is done by

replacing the regulator with an equivalent resistor (calculated as Supply of VCO/ Current of VCO). Dominant pole is taken at the output so as to have a good PSRR(Power Supply Rejection Ratio). This in-turn gives a good PSNR. PSNR is defined as

$$PSNR = 20 * log\frac{\phi_{out}}{\Delta_{vdd}} \tag{3.1}$$

Thus we can see that the PSNR shows how much of supply noise is being translated into the output phase of the PLL. This equation is further split as

$$\frac{\phi_{out}}{\Delta_{vdd}} = \frac{\phi_{out}}{\Delta_{vddvco}} * \frac{\Delta_{vddvco}}{\Delta_{vdd}} \tag{3.2}$$

Here the first term is the Noise Transfer Function (NTF) of the VCO and the second term is the PSRR of the regulator. The aim is to keep the PSNR below 0 in the log scale so that we don't get any supply noise amplified to the output phase. PSNR simulated results across corners is shown below.

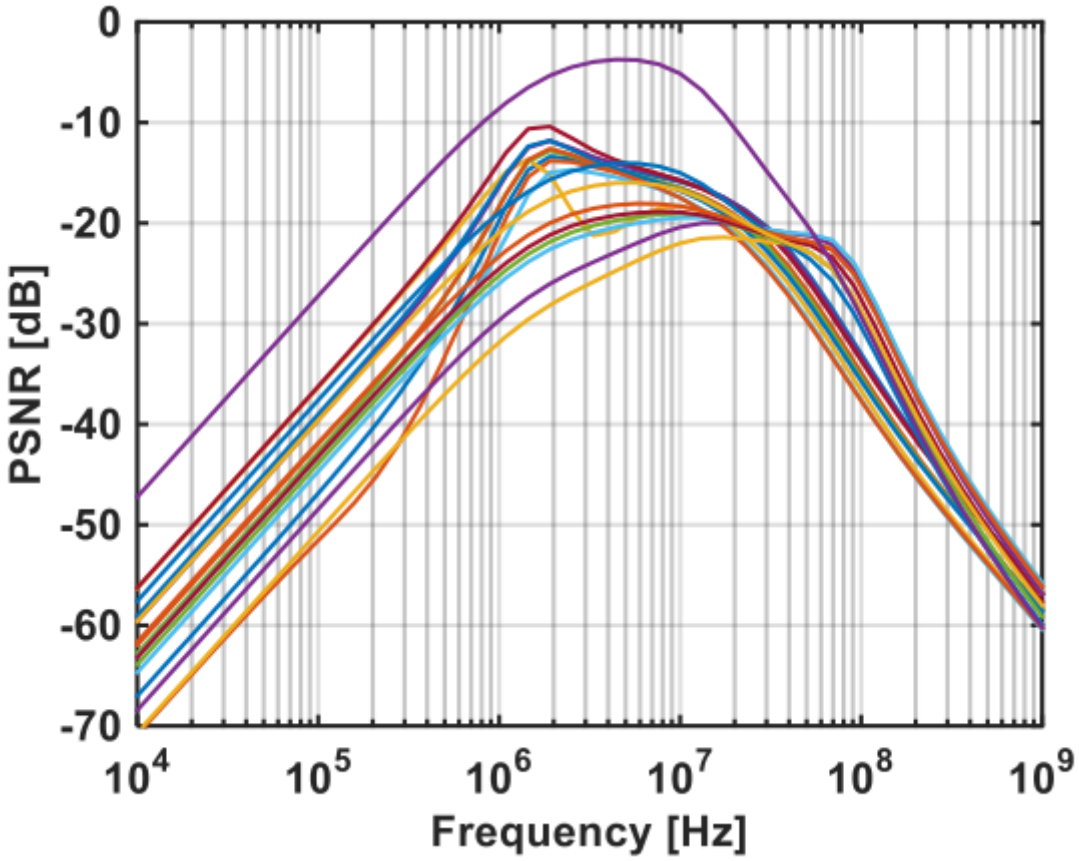
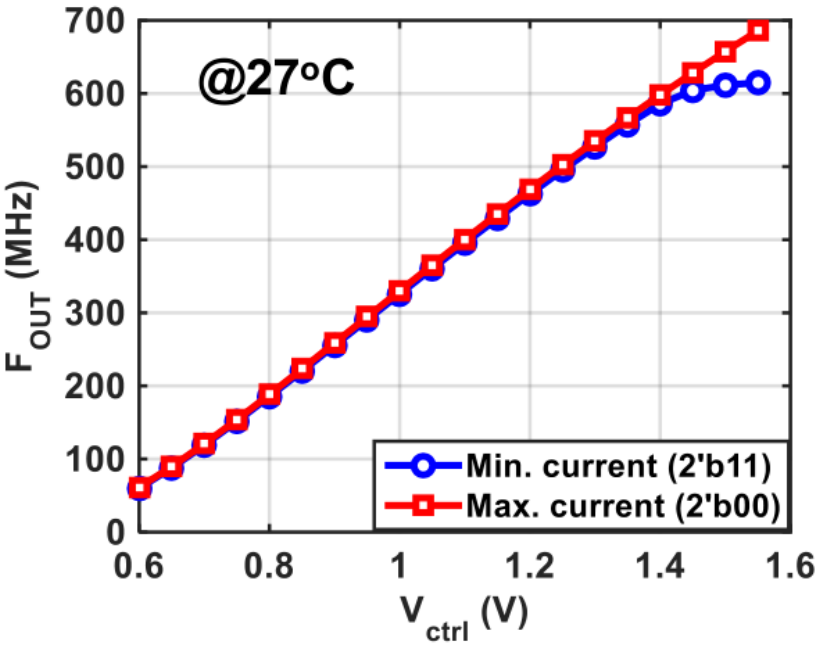


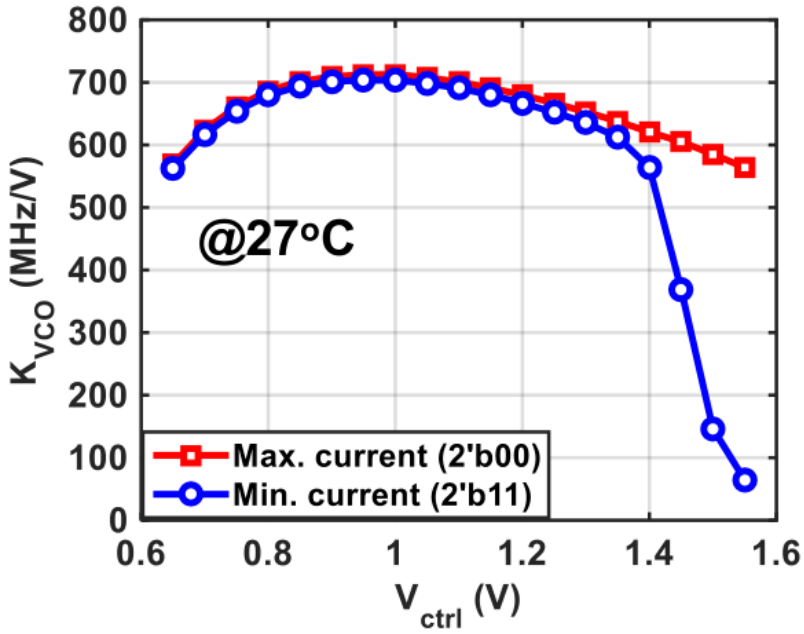
Fig. 3.7: PSNR results

Thus the PSNR is not going above 0 dB and the supply noise will not cause an increased change in the output phase of the PLL. This means that the output rms jitter will not increase with supply variations at the regulator.

The top level VCO is characterized and the results are shown in the following table and figure.



(a) Frequency variation



(b) Kvco variation

Fig. 3.8: VCO charecterisitcs at TT27

Fout (MHz)	**T (°C**	**VDD$_{VCO}$ (V)**	**Ivco (μA)**	**Kvco (GHz/V)**	**F$_{REG}$ (MHz)**	**PM$_{REG}$ (deg)**
105	-40	0.715	43.05	0.852	14.1	78
105	27	0.686	42.19	0.695	12.27	79
105	125	0.648	41.37	0.546	10.2	80
525	-40	1.19	346.3	0.818	47.71	57
525	27	1.284	389.7	0.649	42.5	60
525	125	1.415	461.43	0.486	36.14	65

Table 3.3: VCO parameters

The above simulation is done with a step size of 50mV and gives an overview of the VCO characteristics over its supply range.

3.1.4 Startup

The pseudo-differential ring VCO has even number of stages and it should not get latched up in a stable state. Thus startup circuit is implemented to ensure that the PLL starts up across all corners. It was observed through simulations that a higher current value starts the oscillator so it is decided to start the oscillator at the highest voltage and let it settle. The voltages at the control node and VCO supply are pulled to VDD so that the PLL starts up.

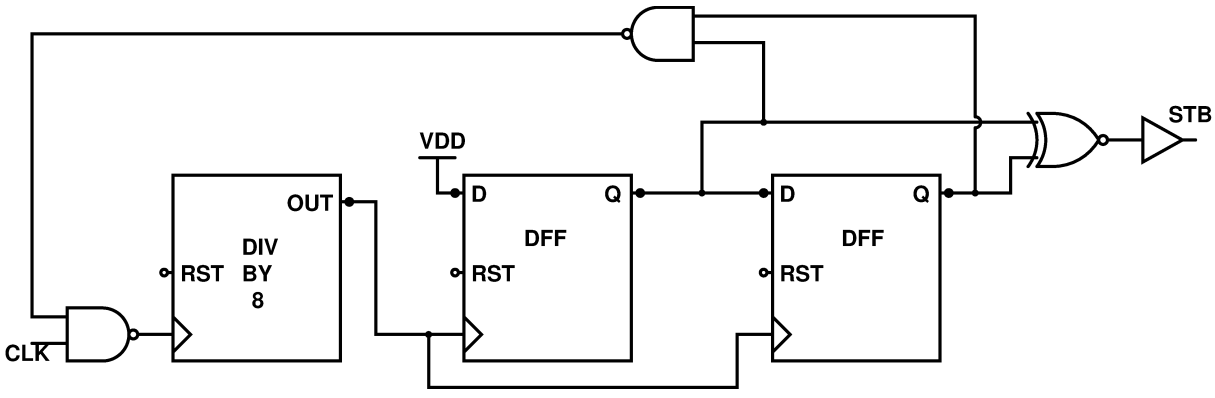


Fig. 3.9: Startup Schematic

An active low pulse is given for 8 reference cycles to PMOS transistors at the 2

nodes. This is generated by a divide by 8 circuit (cascade of 3 divide by 2 circuits), 2 flip flops(FF) and an ex-nor gate. The divide by 2 block is just a D-FF where the Qbar is fed back to the D terminal. There is also a logic so that the divide by 8 block gets deactivated once the startup cycle (8 reference periods) is over. This conserves power. All the blocks are implemented using standard cells since it can easily handle the low reference frequencies.

The transient results of startup circuit is shown below. The startup pulse is activated after the reset pulse and we see that the control voltages are pulled up thereby, starting the PLL.

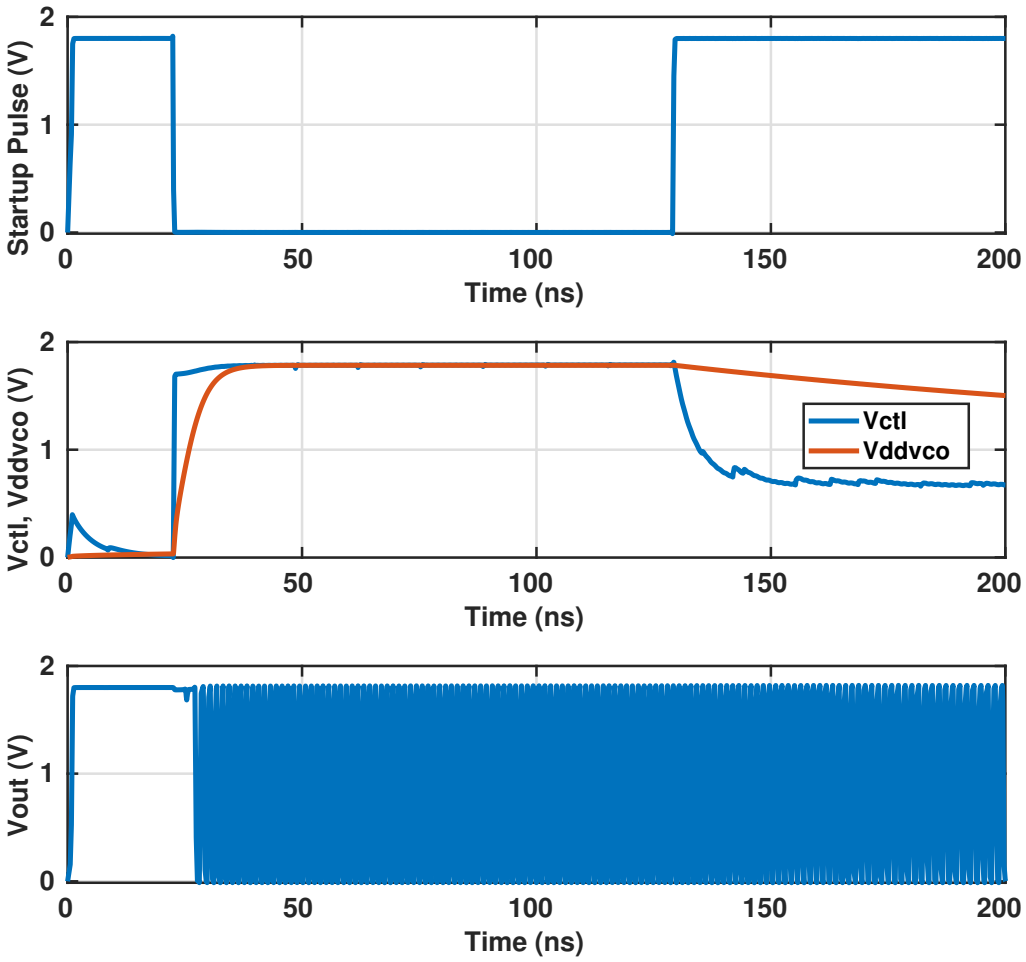


Fig. 3.10: Startup transient result

3.1.5 Bias

The bias currents to blocks such as the regulator, charge-pump op amp etc are given through a simple current mirror as shown below. A current reference of 10μA, is copied to a PMOS cascode-current source from where the required bias currents are scaled accordingly and distributed. There is enough headroom to keep all transistors well in saturation.

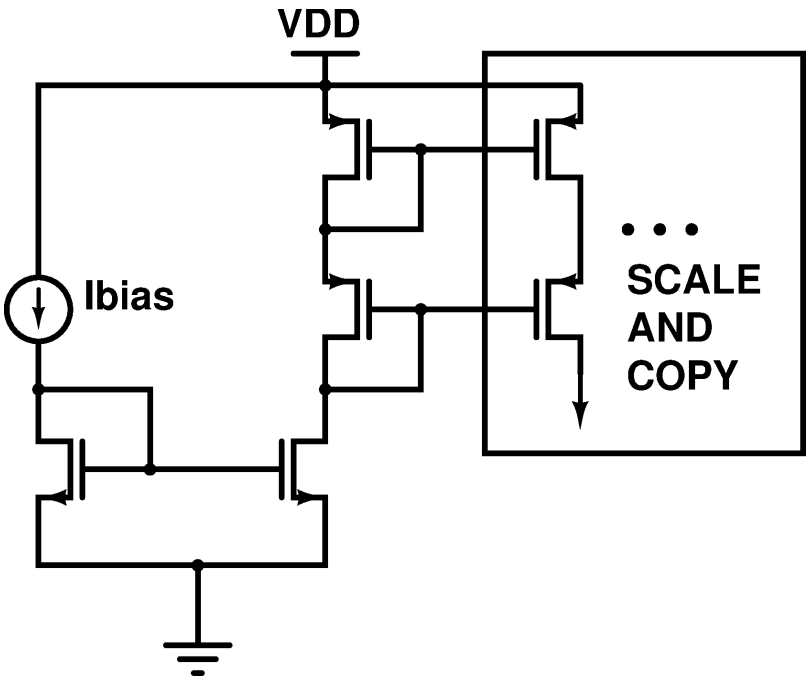


Fig. 3.11: Bias Schematic

A Monte-Carlo analysis is done to find the variation of copied current. The 3σ value is found to be 1μA. Thus the bias block is up scaled and redesigned such that the 3σ value is less than 0.5μA. The histogram of Monte-Carlo simulations is shown below.

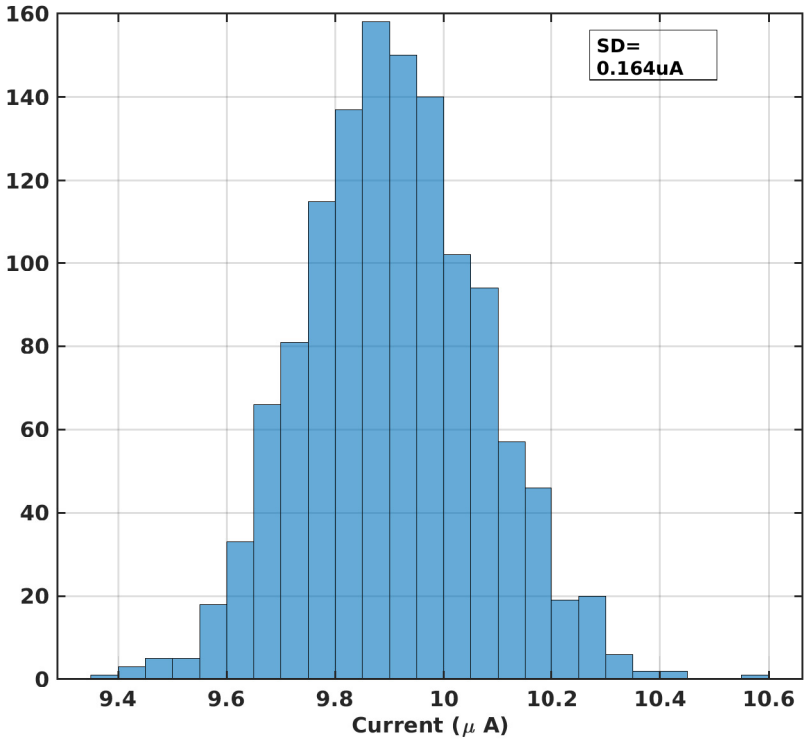


Fig. 3.12: Bias- Monte Carlo Results

3.1.6 Input and Output Buffers

Reference Buffer :

A reference buffer is used to convert the input RF sinusoidal signal (or any reference input) to a square wave reference of the same frequency and 50% duty cycle. It is a single ended clock buffer with 50Ω termination. It adds maximum rms input jitter of 577fs.

Output Buffers :

There are 2 output drivers used in the PLL chip which are CML and LVDS drivers. The CML output driver operates with a current budget of 10mA and 0.25V output amplitude whereas the LVDS output driver is configured to operate at a current of 4mA and 0.4V output amplitude. Since the LVDS driver was initially designed as a output stage for the transmitter, here a Divide by 2 stage is used and it outputs the signal at half the clock frequency. The CML driver adds a maximum of 111fs rms jitter at the output.

3.2 Top level simulations and results

	F_{OUT} (MHz)	**T °C**	**Icp (μA)**	**Fu (MHz)**	**PM_{PLL} (deg)**	**I_{PLL} (mA)**	**Jitter (ps)**
FF	105	-40	3.84	1.48	58.26	0.791	28.39
TT	105	27	4.05	1.26	54.78	0.769	28.56
SS	105	125	4.3	1.07	50.56	0.77	30.14
FF	525	-40	22.89	7.62	67.93	1.652	2.97
TT	525	27	23.86	6.96	67.37	1.673	3.01
SS	525	125	24.65	4.91	67.8	1.738	3.13

Table 3.4: Top Level PLL parameters

The PLL consists of 24pins. There are 12 pins dedicated to supplies (and ground), 3 pins dedicated to bias currents, 4 pins configured as digital controls and 5 IO pins. The supplies required for the circuits present in the PADS take up 4 pins. There are 2 supplies for the PLL core and 3 grounds for the chip. The supplies for the IO buffers are also separated. There is a reset pin to reset the PLL and an enable pin to have only one of the output drivers active at a time. The 2 digital controls DCTRL_PLL are used to configure the charge pump and the regulator. The PLL bias is only 10μA which supplies current to all the required biasing circuits. The CML and LVDS bias are high current values and they are also supplied off-chip. The top level layout of the PLL chip is shown below.

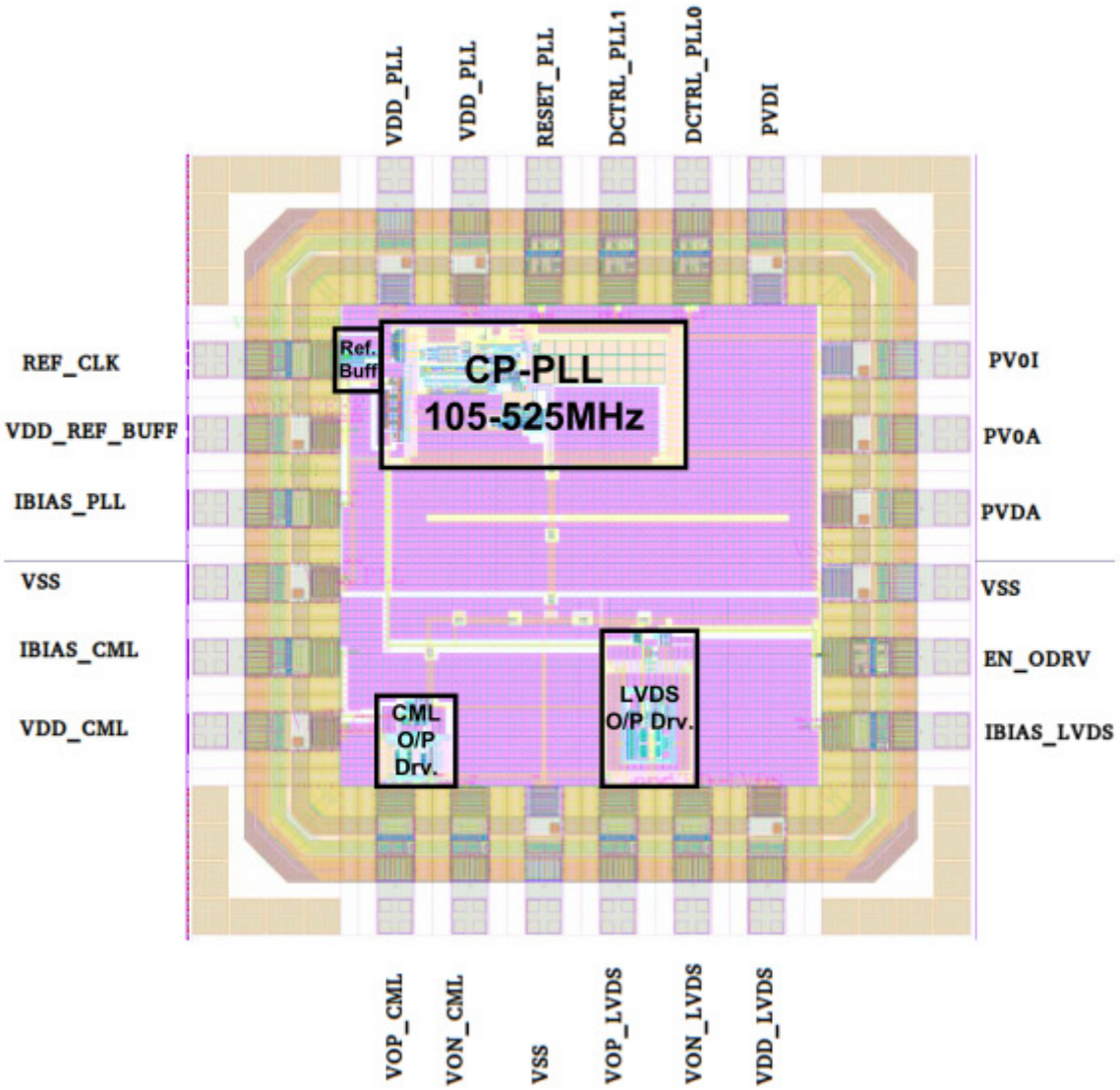


Fig. 3.13: PLL chip

As shown in table 3.3, bandwidth (Fu) of the PLL is kept within $\frac{f_{ref}}{8}$, whereas the Phase margin is kept above 45° across PVT. The jitter varies from 3ps-30ps and the maximum current consumption (of PLL only) is 1.74mA.

The resistors and capacitors in a process have a 20% variation across its minimum and maximum corners. Here a passive loop filter is used to design the PLL. To check if the design is resistant to these changes, simulations are done in TT corner with only passive component variations. (Cadence results are shown.)

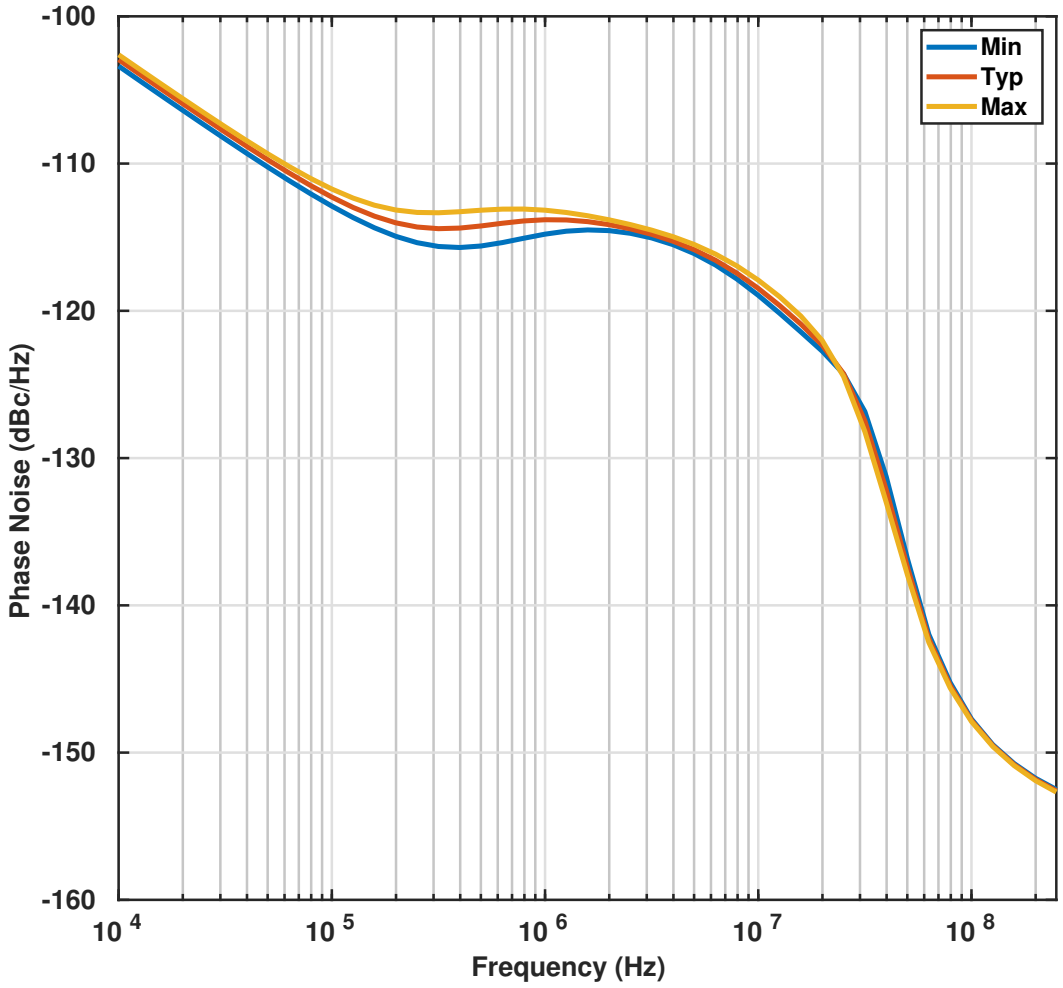


Fig. 3.14: RC corners

Transient analysis results are shown below. First of these shows time domain waveforms at steady state showing reference, feedback, up, down signals and the control voltage. Next the chip level results are shown with frequency settling and CML and LVDS outputs. The chip is operated in such a way that at a time only one of the output drivers is active.

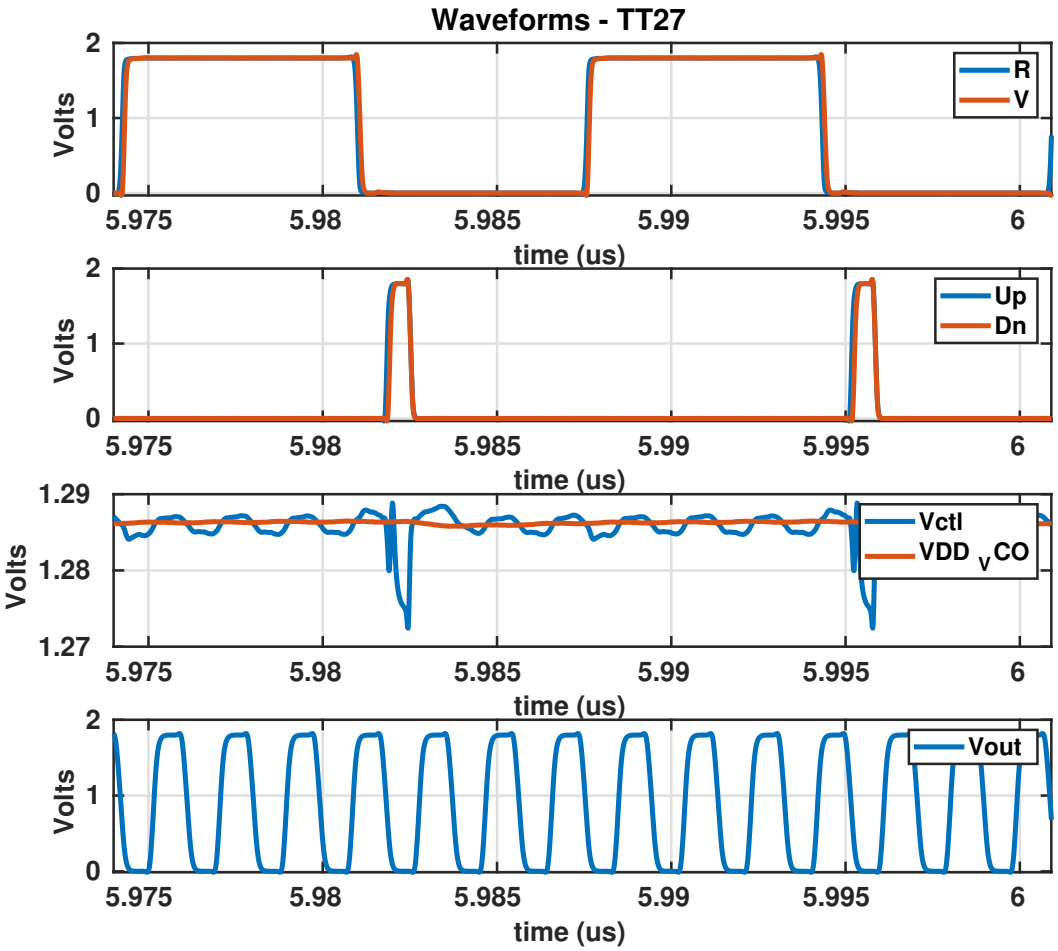


Fig. 3.15: Time domain waveforms

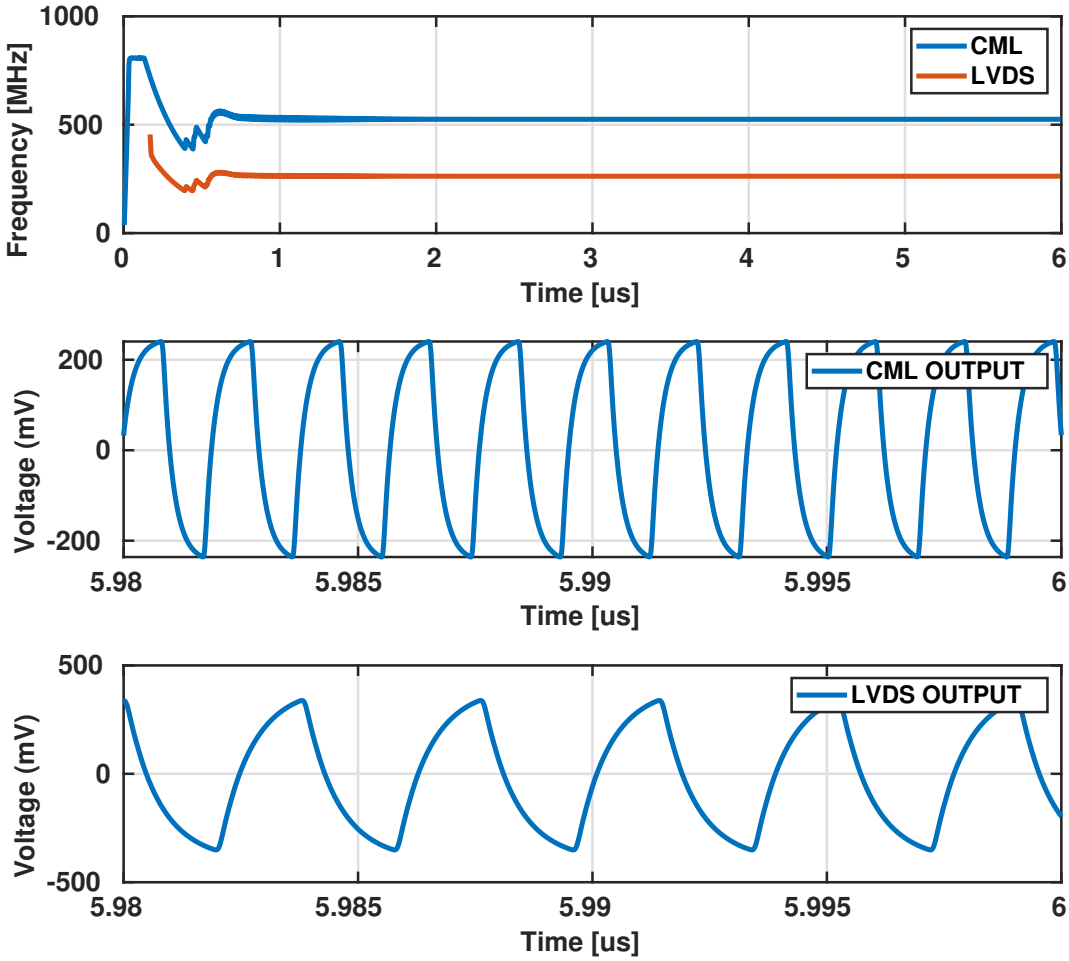


Fig. 3.16: Chip level time domain results

CHAPTER 4

DLL and TX results

The data transitions at the input of the serializer were happening nearby the clock edge causing errors in the serializer. Thus a DFF bank is implemented and the data is synchronized to phase 6 of the DLL.

A startup circuit is designed for the DLL so that the DLL starts up at the correct control voltage for settling. This avoids the problems like harmonic locking or not settling at all.

The startup controls are split into 3 zones for operation of the DLL. It is given in table 4.1.

E1	E0	DLL REF (MHz)
0	0	OFF
0	1	30
1	0	45
1	1	60,75

Table 4.1: DLL startup controls

A pulse generator is used as an input to scaled mosfets , thereby realizing the startup circuit for different cases. The 00 case ensures that the control voltage is reset to 0V.

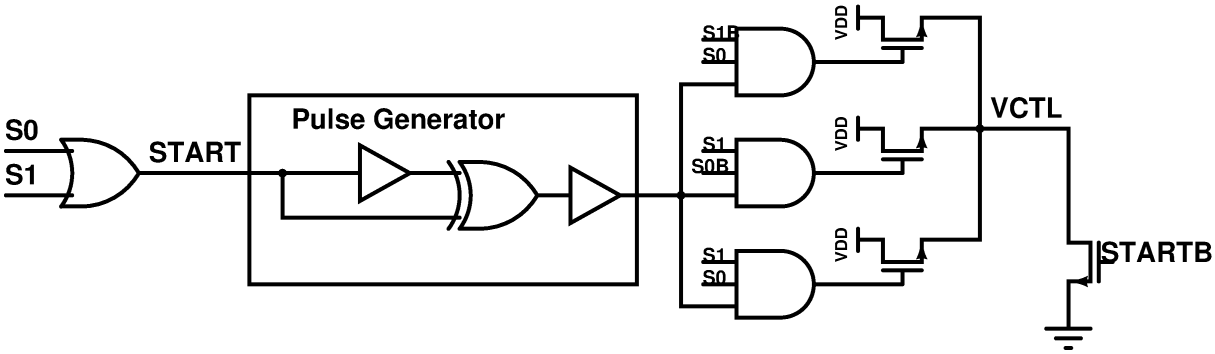


Fig. 4.1: DLL startup Schematic

The DLL results (TT 75MHz) showing control voltage settling and eye diagrams of the output phases are as follows

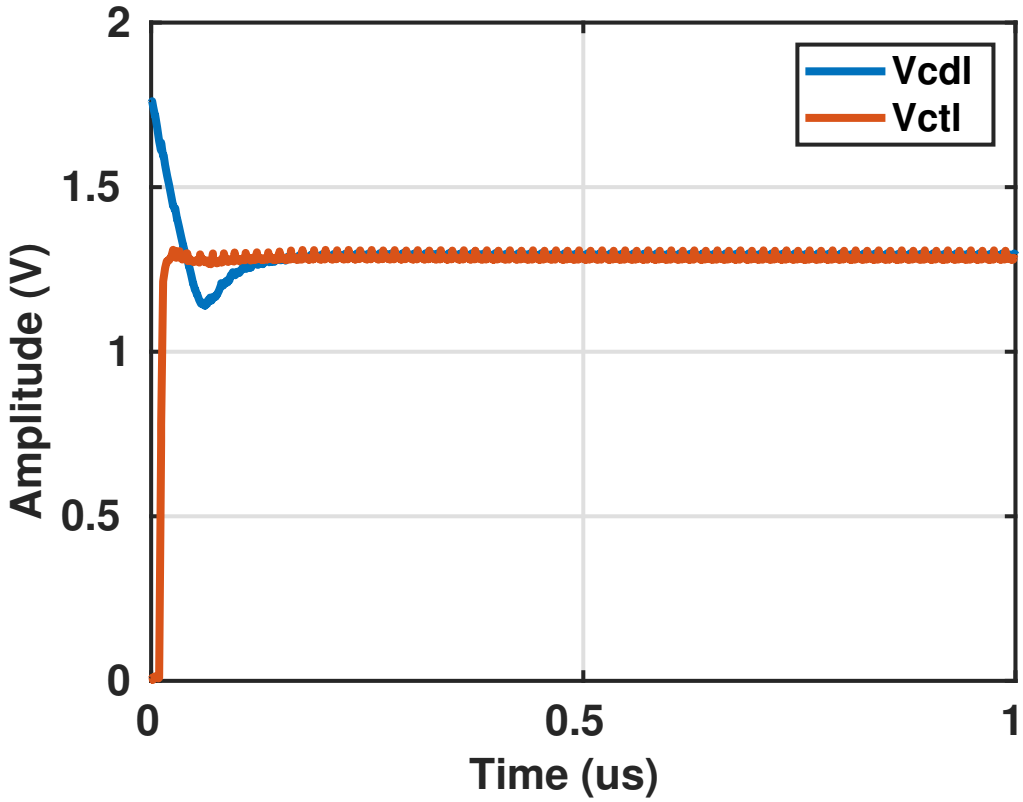


Fig. 4.2: DLL Settling Behaviour

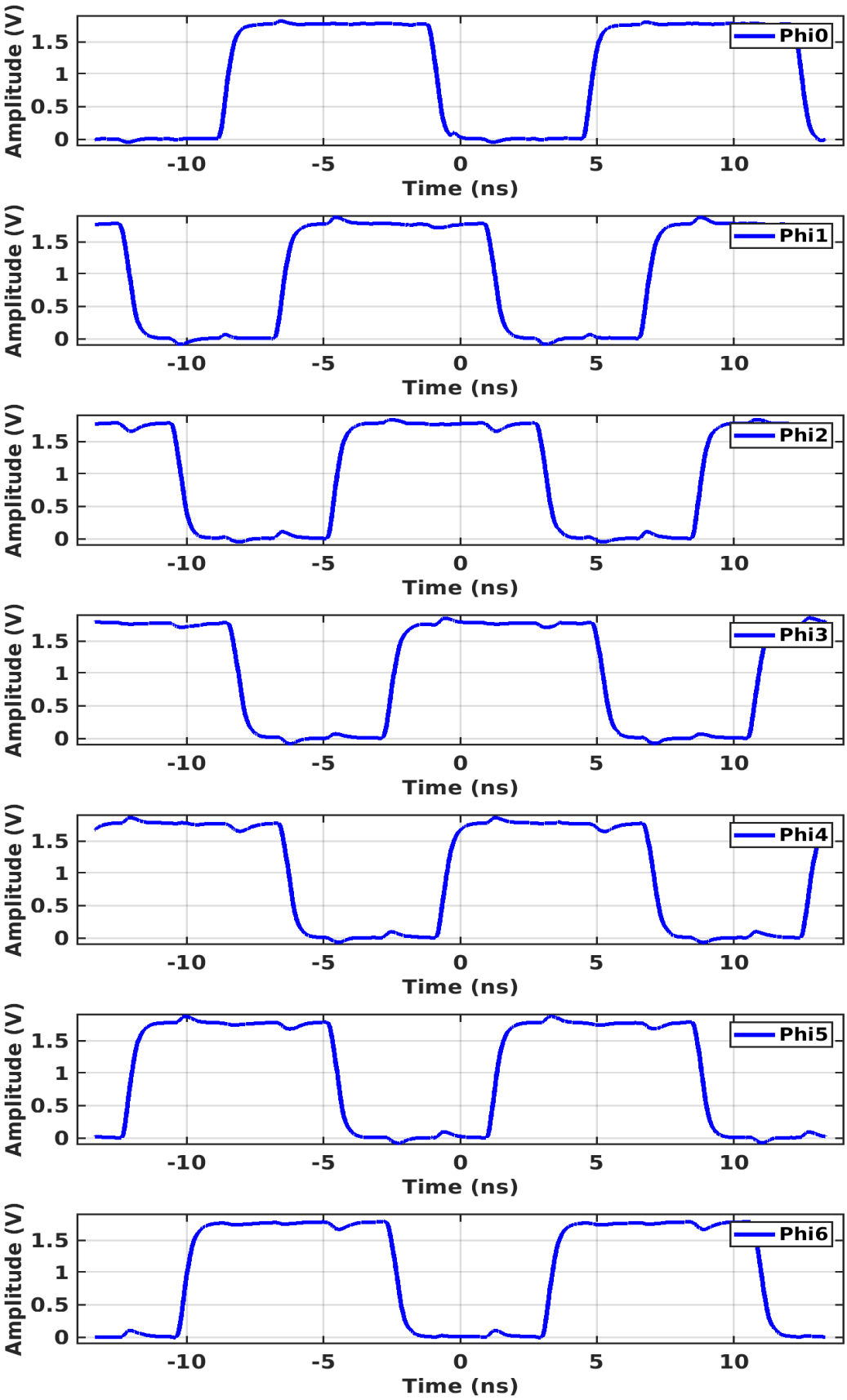


Fig. 4.3: DLL Phase Eye diagrams

The control voltage results across PVT and 2 corner frequencies 30,75MHz are shown below.

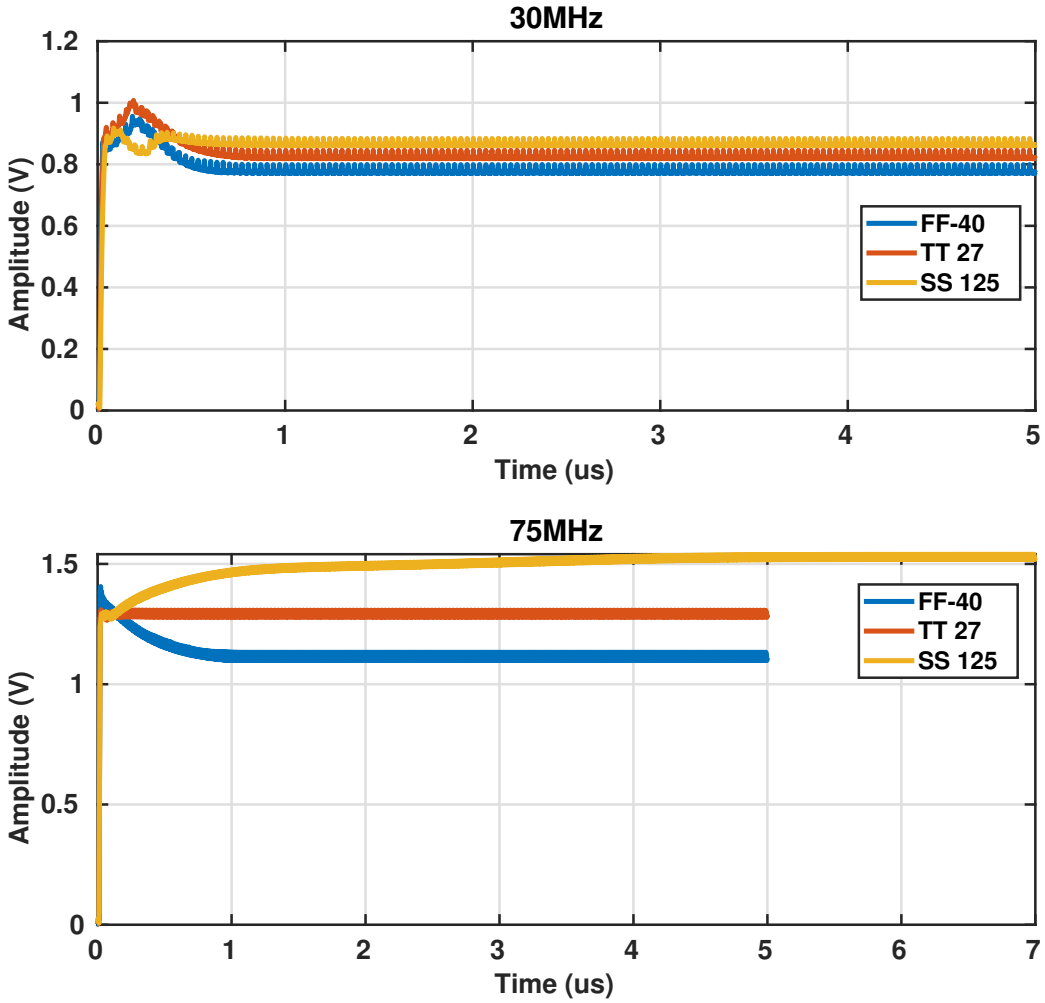


Fig. 4.4: DLL settling across PVT

The transmitter is integrated and buffers are added as required. The bit pattern is verified across corners and for various data rates. This is done by comparing the LVDS output data with the theoretical serialized data obtained from the data bits in MATLAB. The transmitter eye results (at TT 525Mbps) are as follows:

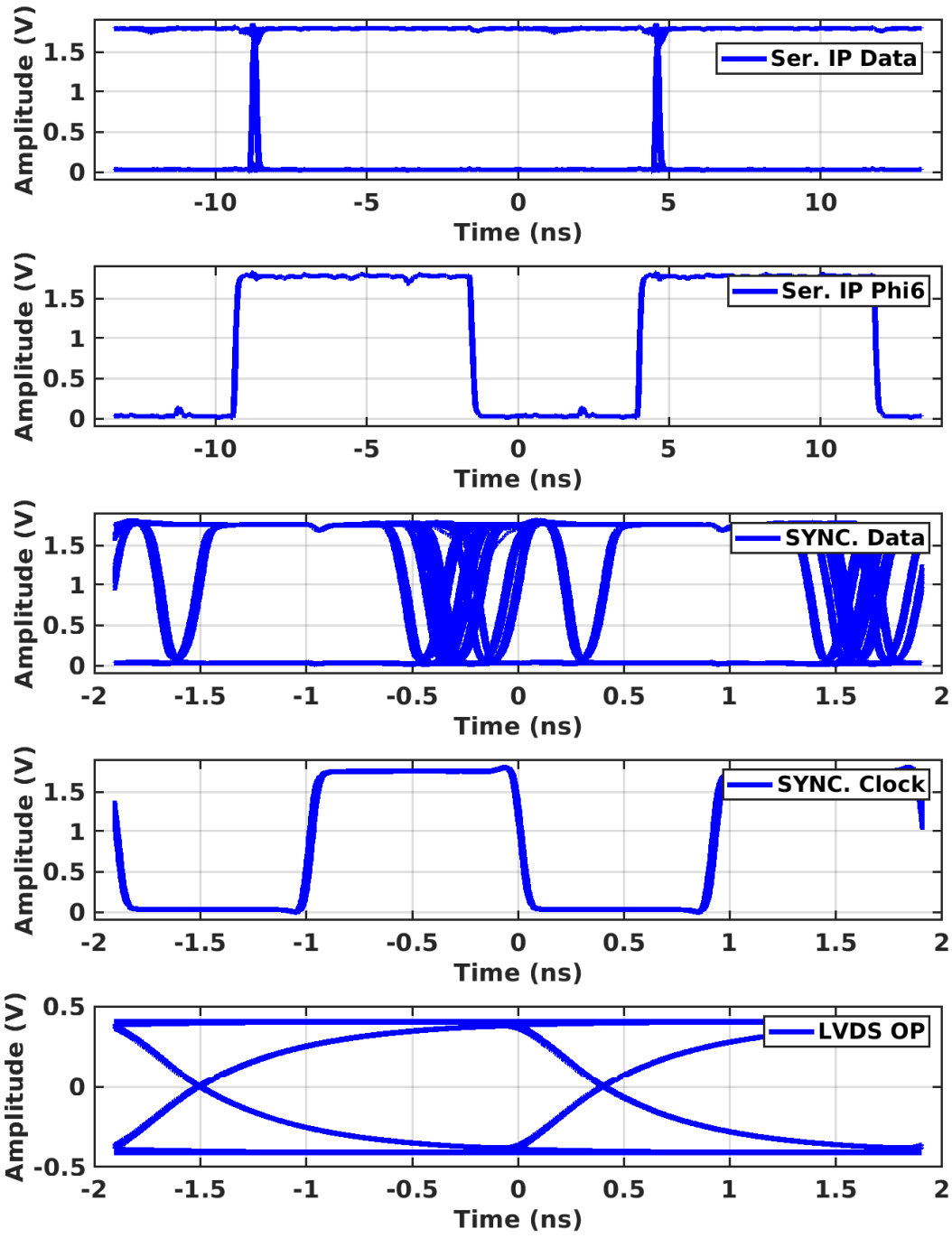


Fig. 4.5: TX results

CHAPTER 5

FUTURE WORK

The synchronizer input needs the clock to be at the centre (ideally) of the serialized data to sample it correctly. Thus a delay block can be designed to ensure it is in a optimal region to get clean eye diagrams.

The PLL output goes to the DLL reference as well as the synchronization clock. The divider to the DLL reference can be implemented using a divide by 7 block and the other divider can be a 4 stage cascade of 2/3 dividers. Using this method data rates from 5Mbps to 525Mbps can be obtained.

The RX PLL is an extension of the TX PLL with 4 phase outputs. Here stability of the regulator loop should be tested before finalizing the design.

The RX chain of components: Analog Front End, Phase Rotating PLL should be designed to complete the SerDes.

REFERENCES :

- Thesis work of Sreenivasa Rao, Nagendra Babu, Kiran Kumar.
- PLL and Serial Link Circuits Course Lectures.