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# Reference Buffer, CML Driver and Multiplying Delay Locked Loop (MDLL)

*A Project Report*

*Submitted by*

**RAYASAM GOPINATH**

*In the partial fulfilment of requirements*

*For the award of the degree*

*Of*

**MASTER OF TECHNOLOGY**

July 2021

# CERTIFICATE

This is to undertake that the Thesis titled **REFERENCE BUFFER, CML DRIVER AND MULTIPLYING DELAY LOCKED LOOP (MDLL)**, submitted by **RAYASAM GOPINATH** to the Indian Institute of Technology Madras, for the award of **M.Tech** degree, is a bona fide record of the research work done by me under the supervision of **DR. SAURABH SAXENA**. The contents of this Thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

**Place: Chennai 600 036**

**Date: 20th Sep 2021**

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# ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my guide Dr. Saurabh Saxena for his continuous support, patience, enthusiasm and immense knowledge. I would also like to express my gratitude to R. Gautham for his guidance and support.

I would like to express my gratitude towards my parents for their encouragement and support.

# ABSTRACT

This thesis covers schematic and layout of Reference Buffer, CML output driver in SCL 180nm and modelling of Multiplying Delay Locked Loop. Reference Buffer is placed at the input of PLL which takes Crystal oscillator clock as input and gives reference clock to PLL. This stage helps in driving various loads present at input of PLL. CML driver uses current steering technique to drive load and is used to transmit PLL output clock. For low PLL phase noise, LC-VCO is used. But LC-VCO occupies more space compared to ring-VCO. By injecting clean reference edges into ring-VCO, one can achieve low phase noise near to LC-VCO and also achieve small form factor of ring-VCO. In MDLL, ring-VCO output clock is periodically realigned with reference edges limiting jitter accumulation which reduces total output jitter. Comparison of total PLL output jitter between with realignment and without realignment is presented.

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# ABBREVIATIONS

| | |
|---|---|
| PLL | Phase Locked Loop |
| MDLL | Multiplying Delay Locked Loop |
| VCO | Voltage Controlled Oscillator |
| CML | Current Mode Logic |
| BBPD | Bang-Bang Phase Detector |
| DCO | Digitally Controlled Oscillator |
| LF | Loop Filter |
| LG | Loop Gain |
| UGB | Unity Gain Bandwidth |

# CHAPTER 1

# INTRODUCTION

Reference buffer is used as an input stage to provide reference clock to PLL from crystal oscillator. This helps in driving phase detector input load. CML driver is used as an output stage which transmits PLL clock. For better noise performance, LC-VCO is generally used. Large space occupied by inductance and capacitance in LC-VCO degrade the form factor of PLL. Ring VCO has less form factor but high phase noise compared to LC-VCO. One way to achieve low phase noise of LC-VCO and small space of ring VCO is to apply realignment to ring VCO edges. Periodic realignment of ring VCO edges with clean edges of crystal oscillator helps in removing the jitter that gets accumulated due to VCO nature. In MDLL, once PLL is locked, reference clock is periodically used to realign the noisy edges of VCO to reference edges. This happens at every reference cycle. In this thesis, design of reference buffer, CML driver and modelling of MDLL is covered. Chapter 2 is about reference buffer design and results. Chapter 3 discusses the various stages of CML driver with its design and results. Chapter 4 elaborates on modelling of MDLL. It contains noise analysis of MDLL comparing noise performance between no realignment and realignment of VCO edges with reference edges.

# CHAPTER 2

# REFERENCE BUFFER

## 2.1 Reference Buffer as PLL input stage

Reference Buffer is used as input stage for PLL which takes Crystal oscillator clock and gives it to Phase detector of PLL as reference clock. It consists of a series of inverters in signal path with first inverter biased at VDD/2. bias Input termination resistance of 50 ohm is used to avoid ringing due to mismatch in impedance. Successive increase in sizing of inverters is done to maintain 50% duty cycle in reference clock. Minimum NMOS sizes and PMOS length was chosen for inverters in signal path. PMOS width was chosen for equal rise-fall delay. Below figure shows schematic of reference buffer.

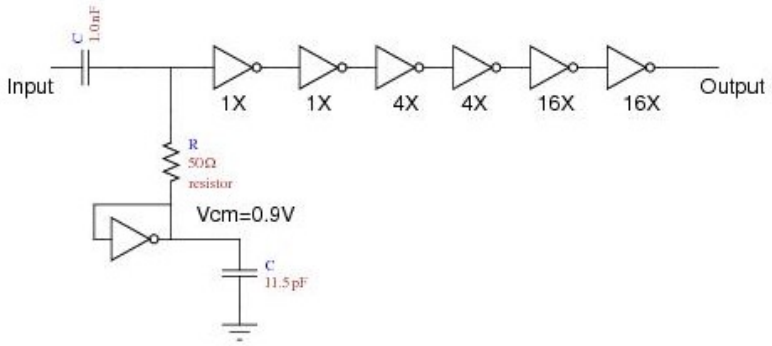



Fig. 2.1: Schematic of Reference Buffer

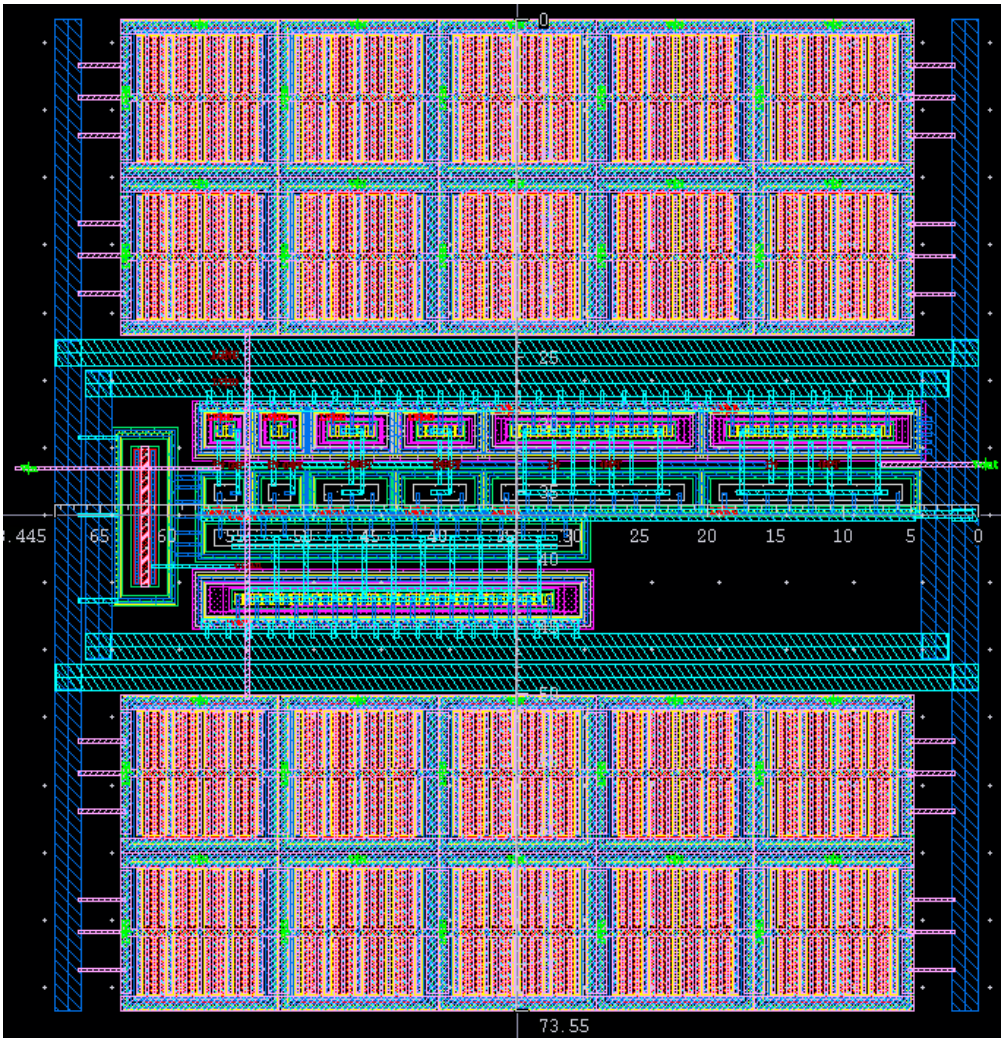



Fig. 2.2: Layout of Reference Buffer

rpmpoly2t resistance with less process variation is used as input termination resistance. Top 10 and bottom 10 square blocks are capacitance with 580fF each, which are used as bias capacitance at common mode inverter. High width common mode inverter is chosen to have better bias at input.

## 2.2 Results

Below results are obtained from r-c extracted view simulation.

Table 2.1: Jitter, Power dissipation, rise and fall time results for 15MHz reference clock

| $15MHzfrequency$ | $ss, 125°C$ | $tt, 27°C$ | $ff, -40°C$ |
|---|---|---|---|
| Jitter | 578fs | 403fs | 300fs |
| Power Dissipation | 1.586mW | 2.34mW | 3.276mW |
| Duty Cycle | 49.15% | 50.44% | 51.26% |
| Rise time | 130.24ps | 79.3ps | 54.53ps |
| Fall time | 101.59ps | 69.45ps | 53.11ps |

Table 2.2: Jitter, Power dissipation, rise and fall time results for 75MHz reference clock

| $75MHzfrequency$ | $ss, 125°C$ | $tt, 27°C$ | $ff, -40°C$ |
|---|---|---|---|
| Jitter | 676.58fs | 492fs | 425.8fs |
| Power Dissipation | 1.58mW | 2.36mW | 3.3mW |
| Duty Cycle | 49.4% | 50.56% | 51.3% |
| Rise time | 129.1ps | 78.72ps | 54.29ps |
| Fall time | 102.4ps | 70.34ps | 53.23ps |

# CHAPTER 3

# CML DRIVER

## 3.1 CML Driver

CML driver is used as output stage which transmits PLL clock. It uses current steering technique to drive loads. It consists of CMOS2CML stage, CML pre-driver and CML output driver. CMOS2CML stage converts CMOS logic to CML. CML pre-driver amplifies CMOS2CML signal and gives it to CML output driver. CML output driver drives transmission lines and differential load of 100 ohm. Below figure depicts the schematic of CML Driver stages.

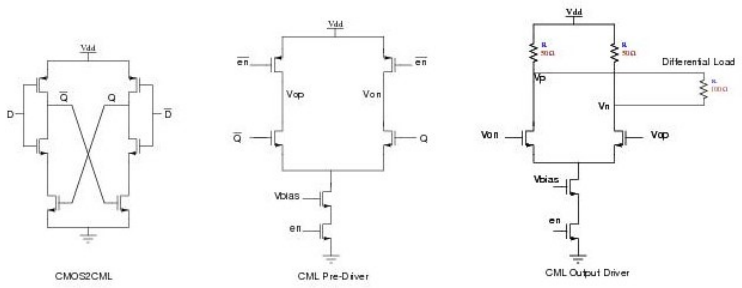



Fig. 3.1: Schematic of CML Driver stages

It consists of common source MOS differential pair with 50 ohm drain resistance which are output termination resistances. Output voltage swing is obtained by steering bias current between the output transistors. Differential output swing of 0.5V was obtained with 10mA bias current. Switch transistors are placed below bias transistors, they are enabled when transmission of PLL clock is required. Output 50 ohm termination resistance is used to avoid reflection due to impedance mismatch between transmission line and differential load termination.

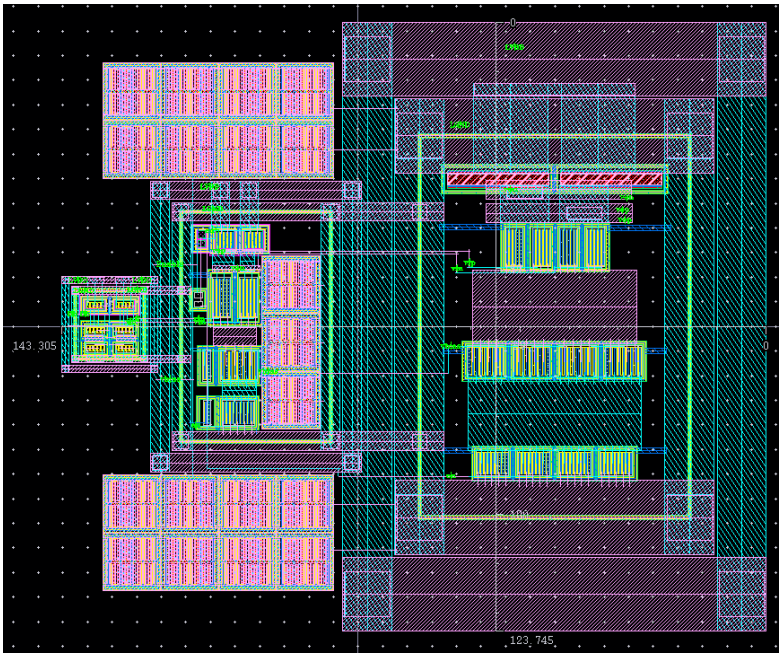


Fig. 3.2: Layout of CML Driver

Thick metal lines were used to carry large current between output transistors. For widths above 50um, separate body contacts are placed.

## 3.2 Results

Below are jitter and power consumption results for CML Driver.

Table 3.1: Jitter and Power dissipation results for 105MHz clock

| $105MHz frequency$ | $ss, 125°C$ | $tt, 27°C$ | $ff, -40°C$ |
|---|---|---|---|
| Jitter | 331.5fs | 412.8fs | 473.2fs |
| Power Dissipation | 21.78mW | 22.77mW | 23.12mW |

Table 3.2: Jitter and Power dissipation results for 525MHz clock

| $525MHz frequency$ | $ss, 125°C$ | $tt, 27°C$ | $ff, -40°C$ |
|---|---|---|---|
| Jitter | 101.9fs | 100.6fs | 106.8fs |
| Power Dissipation | 23.13mW | 24.15mW | 24.6mW |

# CHAPTER 4

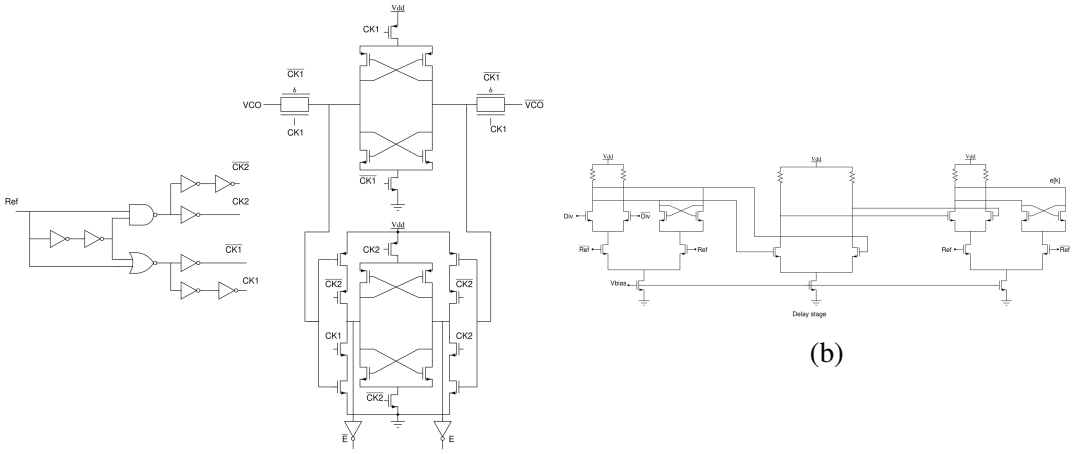
# MULTIPLYING DELAY LOCKED LOOP (MDLL)

## 4.1 Building Blocks of Multiplying Delay Locked Loop

A digital PLL consists of digital phase detector and loop filter unlike analog PLL where PFD, charge pump and analog loop filter are present. Digital output of loop filter is given to VCO after converting it to continuous control voltage using a DAC. In digital PLL, loop filter can be programmed unlike analog PLL where it is fixed. It is also scalable with technology. In this thesis MDLL model was analysed with Bang-Bang phase detector, digital loop filter, $\Delta\Sigma$ DAC, ring VCO and fractional divider.

### 4.1.1 Bang-Bang Phase Detector

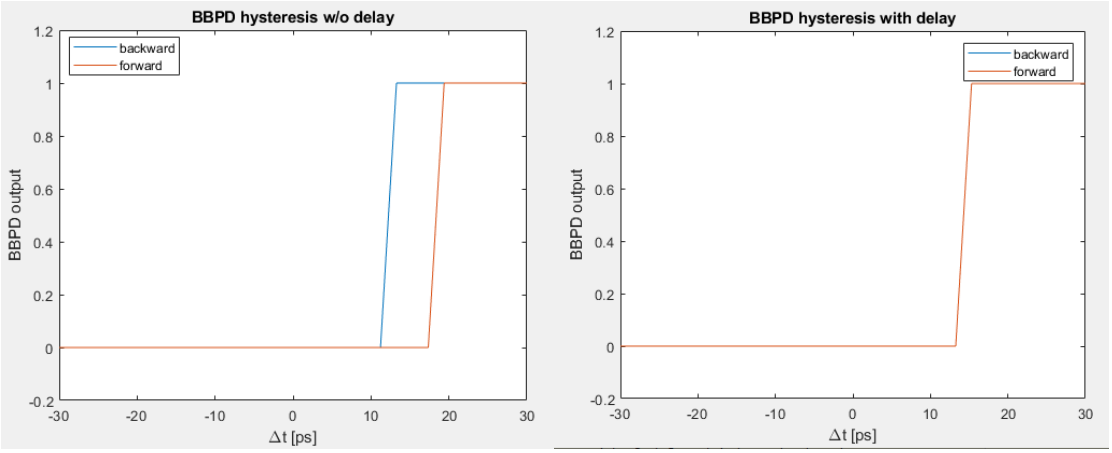
In Bang-Bang phase detector, 1-bit TDC is used in which output becomes high when reference clock leads divider clock. Due to presence of thermal noise, Bang-Bang phase detector can be considered as a linear phase detector with very high gain whose value is dependent on jitter between reference and divider clock rising edges($\sigma_{\Delta t}$). Gain of BBPD is $\frac{de(\Delta t)}{d\Delta t} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\Delta t}}$




(a) (b)

Fig. 4.1: (a)BBPD with overlapping clock generator, (b) CML BBPD with additional delay stage

BBPD can be designed using a master-slave flip flop. Care must be taken as there is memory effect present in them which gives rise to memory hysteresis. Memory hysteresis deteriorates jitter as there is time offset due to memory effect which adds to jitter. It can be prevented by using a non-overlapping clock generator. It takes reference clock and generates non-overlapping clock which makes sure to not turn ON both master and slave latches for small duration. Also by introducing a delay stage in between master and slave latch, memory effect can be avoided.




(a) (b)

Fig. 4.2: Hysteresis was observed for fixed reference and moving divider rising edge (a) without delay stage between master and slave latches, (b) with delay stage between master and slave latches

### 4.1.2 Digital Loop Filter

Loop filter is present to remove high frequency content from phase detector output and generate a control word which controls DCO frequency. It accumulates the output of phase detector to give control word. Loop filter consists of two paths: Proportional $\beta$ and Integral path$\alpha$. Proportional path ensures that open loop gain of PLL has good phase margin which keeps PLL stable. Loop filter gain is LF= $\beta + \frac{\alpha}{1-z^{-1}}$ . Accumulators with good resolution ( 14 bit resolution) are needed for tracking as they are used in fine tuning DCO. Due to high gain of BBPD, gain of DCO falls near kHz/word which is difficult to achieve. To increase DCO gain, additional gain stage($1/\gamma$) is introduced after proportional and integral path. The delay present in integral path is considered as $z^{-D}$.

### 4.1.3 Digitally Controlled Oscillator

DCO consists of DAC and VCO. DAC converts digital control word to continuous control voltage which controls VCO frequency.

**Delta-Sigma DAC**

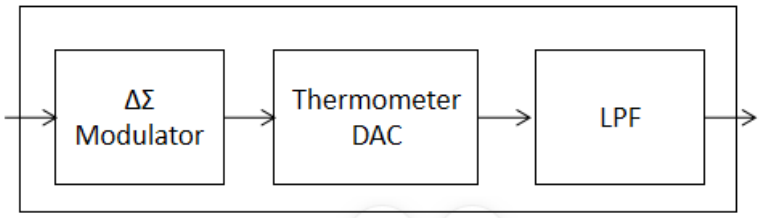



Fig. 4.3: $\Delta\Sigma$ DAC

For DAC, Delta Sigma DAC is used as it maintains Loop filter resolution (14 bits) at its output using a low resolution DAC (5 bits) and Delta Sigma modulator operating at frequency higher than reference. Delta Sigma modulator dithers its output so that average over a reference cycle is equal to its input. This helps in achieving high bit resolution of input at output using less number of levels. Since less number of levels are used, DAC with resolution lower than Delta Sigma modulator input can be used to maintain high resolution. Delta Sigma modulator also does noise shaping. It shapes low

frequency noise into high frequency which is later filtered using a low pass filter after DAC. This allows to give better jitter performance using a low bit DAC and maintains high resolution of Loop filter. For a second order Delta Sigma modulator, STF= 1 NTF= $(1\text{-}z^{-1})^2$

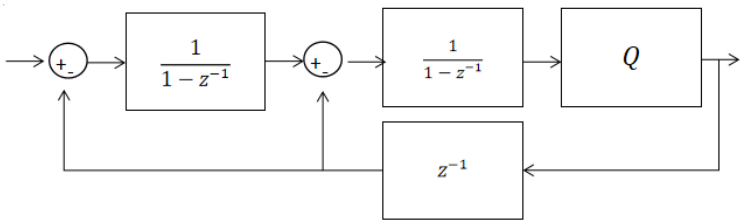



Fig. 4.4: Second order $\Delta\Sigma$ modulator

DAC with thermometer coding reduces DNL/INL. Each unit cell is turned on individually in thermometer coding. This reduces mismatch in voltage steps across different levels at output. CML logic can be used to build unit cell which switches current between two switch transistors from a constant bias MOS. Since bias MOS is always ON, no extra time is needed to charge its drain capacitance. It can also drive large loads. For low resolution DAC, units cells with 1 LSB current controlled by thermometer coding can be used whereas for high resolution DAC, segmented architecture is used so less space is occupied with better DNL/INL specification.

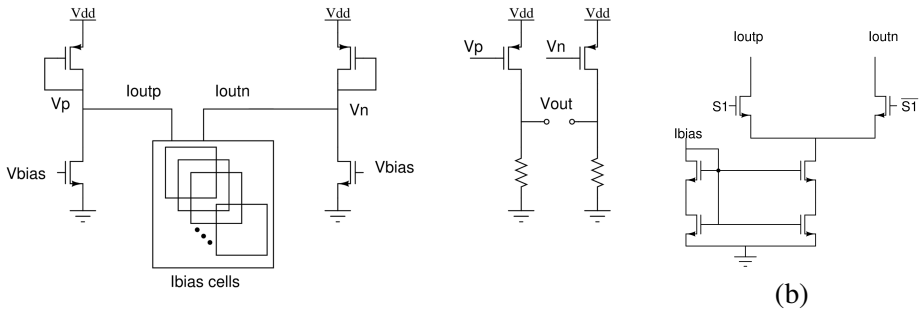



Fig. 4.5: (a) non-inverting DAC, (b) unit cell

**Pseudo Differential Ring Oscillator**

Pseudo Differential Ring oscillator can be used to build a VCO. Key advantage of this oscillator is its small form factor. Current starved inverters are used to generate required frequency. Changing the current amount in inverters directly affects output frequency. The output frequency is controlled using a control voltage which controls the amount of current through inverters. The inverters are biased using cross-coupled inverters. The output frequency is sustained due to positive feedback present inside the loop. VCO can be viewed as a integrating stage with a gain $2\pi K_{VCO}$ as control voltage directly affects frequency and phase is integration of frequency w.r.t time giving $\frac{2\pi K_{VCO}}{s}$,

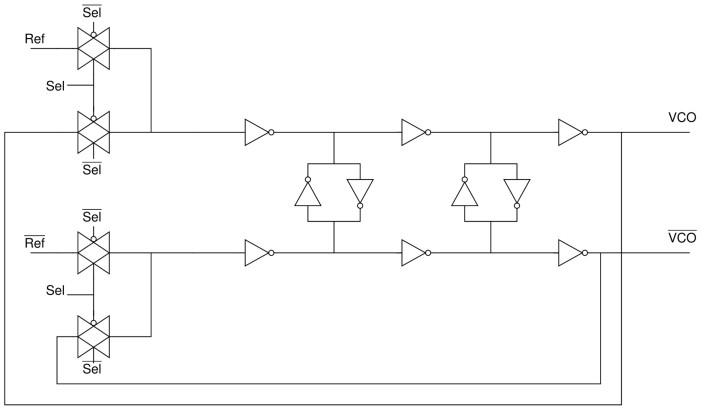



Fig. 4.6: Ring VCO

Due to VCO integrating nature, jitter accumulation happens. Most of VCO phase noise can be filtered using high unity gain bandwidth of PLL open loop, but at cost of increase in BBPD and reference phase noise at output. Another way to reduce VCO phase noise without increasing output phase noise from BBPD or reference is to realign VCO edges using clean edges from crystal oscillator. This limits jitter accumulation at VCO output as at every reference cycle VCO edges are corrected. Reference clock is given to ring VCO through a MUX which selects reference clock edge after every $N * T_{VCO}$, where $T_{VCO}$ is VCO output period and selects ring VCO output otherwise. Since reference clock is given to ring VCO, a direct path exists from reference to PLL output. Also as reference edge realigns the VCO edges every reference cycle, accumulation of VCO phase is periodically removed which is like a high pass filter after VCO. So due

to realignment, a path exists directly from reference to PLL output with gain $H_{up}$ and a high pass filter after VCO with gain $H_{rl}$ are present.

$$\mathrm{H}_{up} = \frac{\beta_{rl} N}{1+(\beta_{rl}-1)e^{-sT_{ref}}} . e^{-\frac{sT_{ref}}{2}} \frac{sin(\frac{sT_{ref}}{2})}{\frac{sT_{ref}}{2}}$$

$$H_{rl} = 1 - \frac{\beta_{rl}}{1+(\beta_{rl}-1)e^{-sT_{ref}}} e^{-\frac{sT_{ref}}{2}} \frac{sin(\frac{sT_{ref}}{2})}{\frac{sT_{ref}}{2}}$$ where $\beta_{rl}$ is realignment factor.

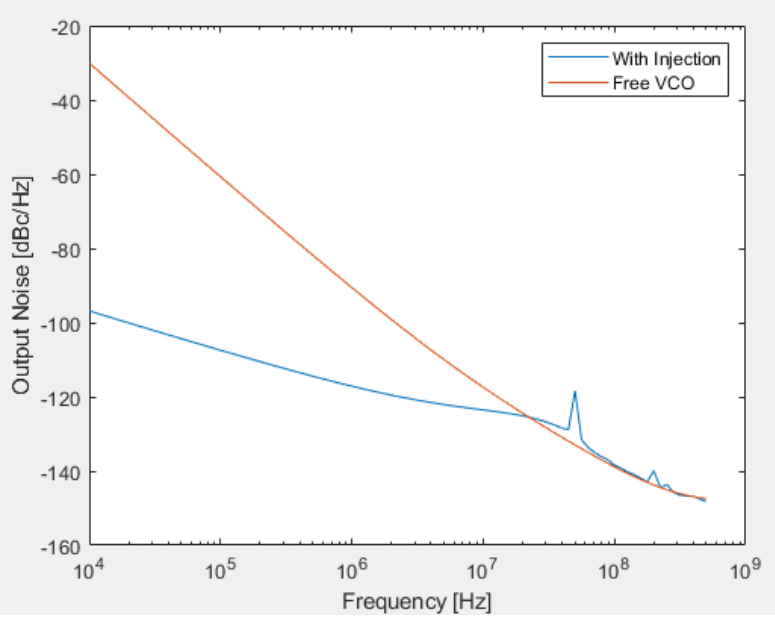



Fig. 4.7: Phase noise of free running VCO vs with realignment.

when realignment takes place, phase noise of free running VCO is filtered by $H_{rl}$ which is a high pass filter. This reduces overall VCO phase noise improving PLL output jitter. In above figure, phase noise of free running VCO got reduced from -90dBc/Hz @ 1MHz to -112dBc/Hz @ 1MHz when realignment is done. This value is near to LC-VCO phase noise (near -120dbc/Hz @ 1MHz).

### 4.1.4 Divider

#### Fractional Divider

Fractional divider consists of $\Delta\Sigma$ modulator and Multi Modulus divider. It is used to generate divider ratio of any fractional value which depends on the length of accumula-

tor used in $\Delta\Sigma$ modulator. Divider ratio is given as frequency control word, its integer part is directly given to MMD whereas the fractional part is added with LSB of MMD through $\Delta\Sigma$ modulator and modulo adder. $\Delta\Sigma$ modulator dithers its output which helps in avoiding reference spur. Any change in divider ratio affects the loop after acummulation as it affects the output frequency.

### 4.1.5 Small Signal Model

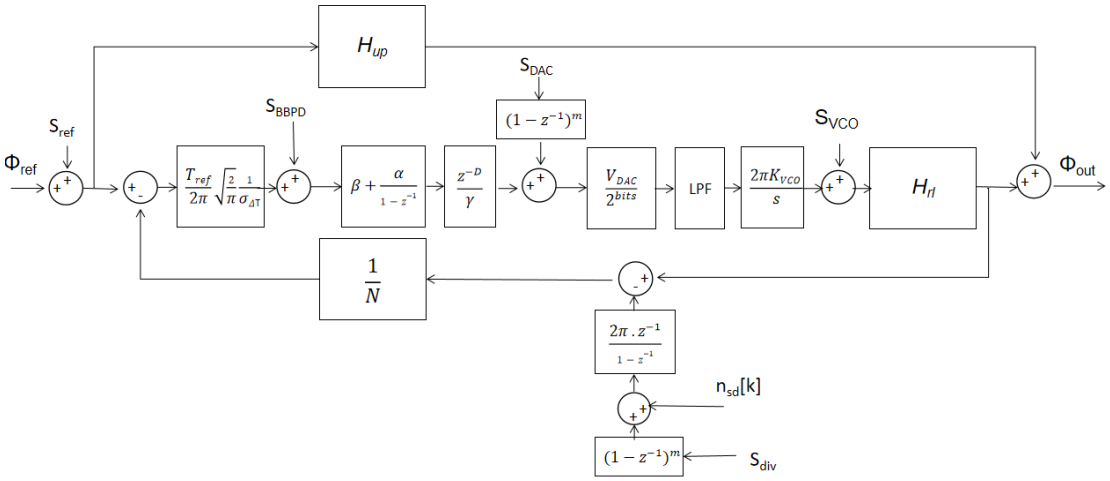



Fig. 4.8: Fractional Multiplying Delay Locked Loop

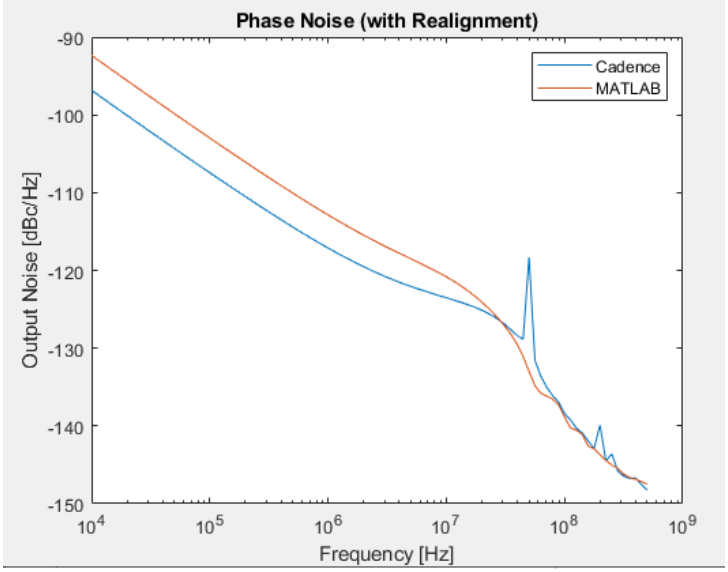



Fig. 4.9: Comparison of VCO phase noise after realignment between small signal model and cadence simulation

## 4.2 Loop Gain Analysis

From small signal model, open loop gain of MDLL is $k(\frac{\beta s T_{ref}+\alpha}{s^2})(LPF)H_{rl}$ where,$k$=$\frac{K_{DCO}}{N\gamma\sigma_{\Delta t}}\sqrt{\frac{2}{\pi}}$

Loop gain has been plotted for following parameters:

Table 4.1: Parameters used for Loop Gain

| Parameter | Value |
|---|---|
| Reference Frequency | 40MHz |
| VCO Frequency | 2.5GHz |
| $\sigma_{\Delta t}$ | 800fs |
| $K_{VCO}$ | 2.333GHz/V |
| $V_{DAC}$ | 200mV |
| DAC bits | 5 bits |
| DAC frequency | 320MHz |
| Order of $\Delta\Sigma$ DAC | 2 |
| Order of $\Delta\Sigma$ divider | 2 |
| LPF poles | 20MHz and 40MHz |
| Unity Gain Bandwidth | 200kHz |
| Phase Margin | 60° |

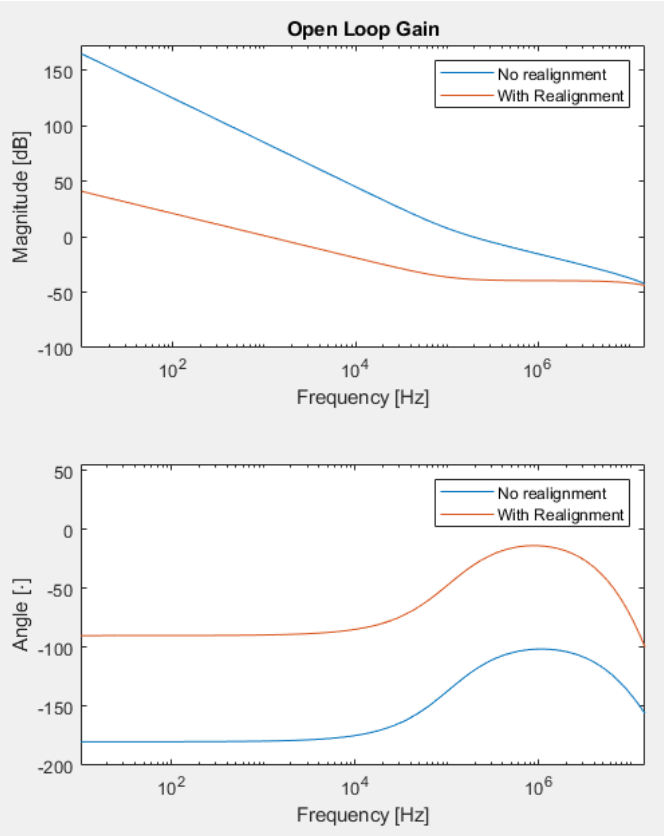



Fig. 4.10: Open Loop Gain of MDLL

When realignment takes place, open loop gain is further filtered by high pass filter $H_{rl}$. Due to this, unity gain bandwidth decreases and phase margin rises from 60°at old UGB to 89°at new UGB. It does not affect stability of loop. Since unity loop gain bandwidth decreases with realignment, less BBPD and reference noise is contributed into total output phase noise.

## 4.3 Noise Analysis

Noise sources present in small signal model are reference, BBPD, DAC, VCO and divider. PSD of BBPD is $\frac{0.368}{f_{ref}}$ . PSD of DAC is $\frac{1}{12*f_{DAC}}$ and PSD of divider is $\frac{1}{12*f_{DIV}}$ where $f_{DAC}$ and $f_{DIV}$ are operating frequencies of DAC and divider. Free running VCO PSD is obtained from cadence simulation. Noise transfer functions for the above sources are:

$NTF_{ref} = H_{up} + \frac{N*LG}{1+LG}$

$NTF_{BBPD} = \frac{1}{K_{BBPD}} \frac{N*LG}{1+LG}$

$NTF_{DAC} = \frac{(2sin(\frac{\pi f}{f_{DAC}}))^{mdac}}{1+LG}$

$NTF_{VCO} = \frac{H_{rl}}{1+LG}$

$NTF_{DIV} = 2\pi(2sin(\frac{\pi f}{f_{DIV}}))^{mdiv-1} * \frac{LG}{1+LG}$

where mdac and mdiv are the order of $\Delta\Sigma$ DAC and $\Delta\Sigma$ divider. Noise transfer functions of BBPD and reference has low pass nature whereas for VCO it is of high pass nature. For low UGB, VCO noise dominates output phase noise of PLL whereas for high UGB, BBPD and reference noise contribute more.

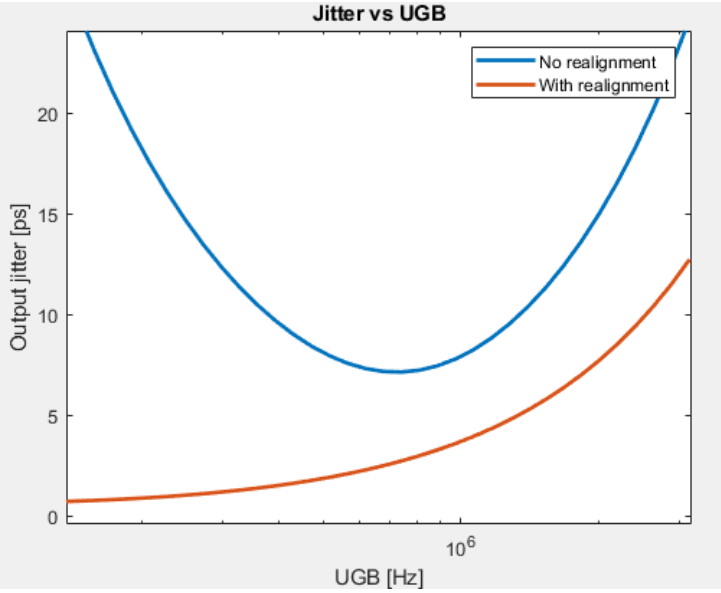
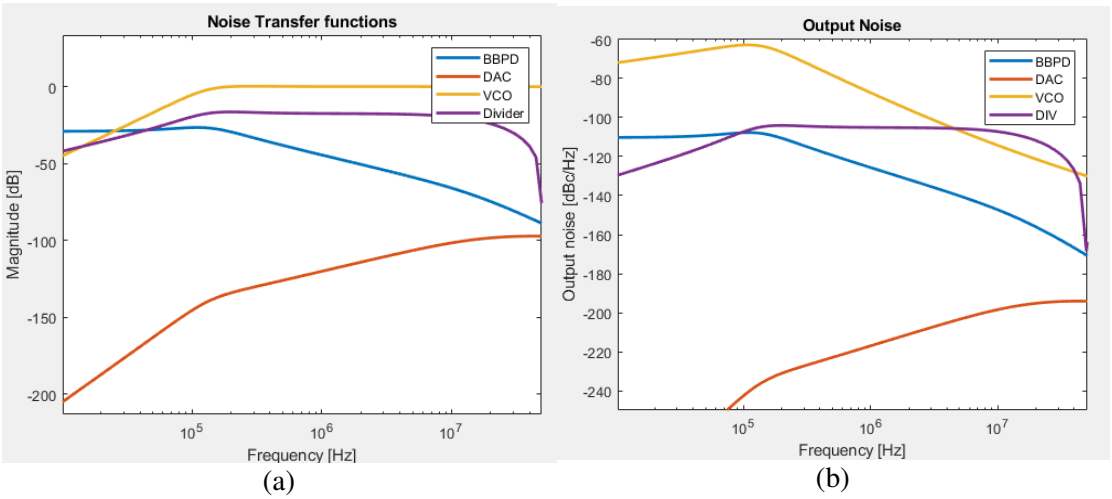


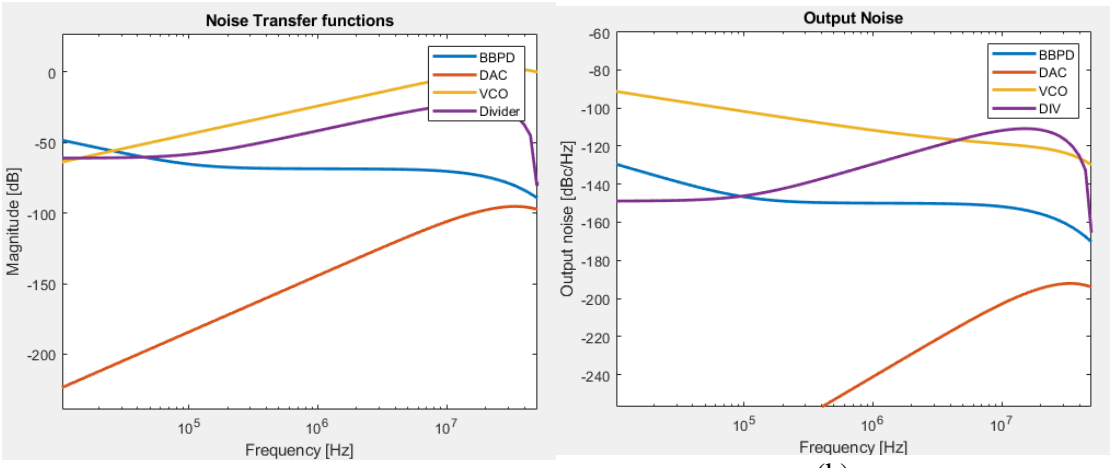

Fig. 4.11: Output Jitter vs Unity Gain Bandwidth

When realignment happens, VCO phase noise is filtered with $H_{rl}$ which has higher cut off frequency than old UGB reducing VCO phase noise contribution to total output phase noise. Therefore, at low UGB, jitter with realignment is small compared to no realignment. But as UGB increases, BBPD phase noise dominates and total jitter starts to rise in both cases. Following noise transfer functions and output noise are plotted for 200kHz UGB.




(a) (b)

Fig. 4.12: Without realignment (a) Noise Transfer Functions, (b) Output Phase Noise




(a) (b)

Fig. 4.13: With realignment (a) Noise Transfer Functions, (b) Output Phase Noise

Due to $H_{rl}$, noise transfer function of VCO is filtered at higher cut off frequency. Also BBPD, DAC and divider are further filtered at lower cut off frequency. Therefore, total jitter is reduced when realignment is performed. Total jitter at 200kHz UGB under no realignment is 18.2ps and when realignment is performed it reduced to 870fs.

## 4.4 Phase Modulation

In MDLL, VCO edges are realigned using reference edges. During realignment, any shift in reference edge directly modulates output phase. This can be used for phase modulation of output signal. Using DTC reference edges can be modulated by a message signal that controls delay of DTC. When these shifted reference edges are used for realignment, VCO edges also shift accordingly causing phase modulation at output.

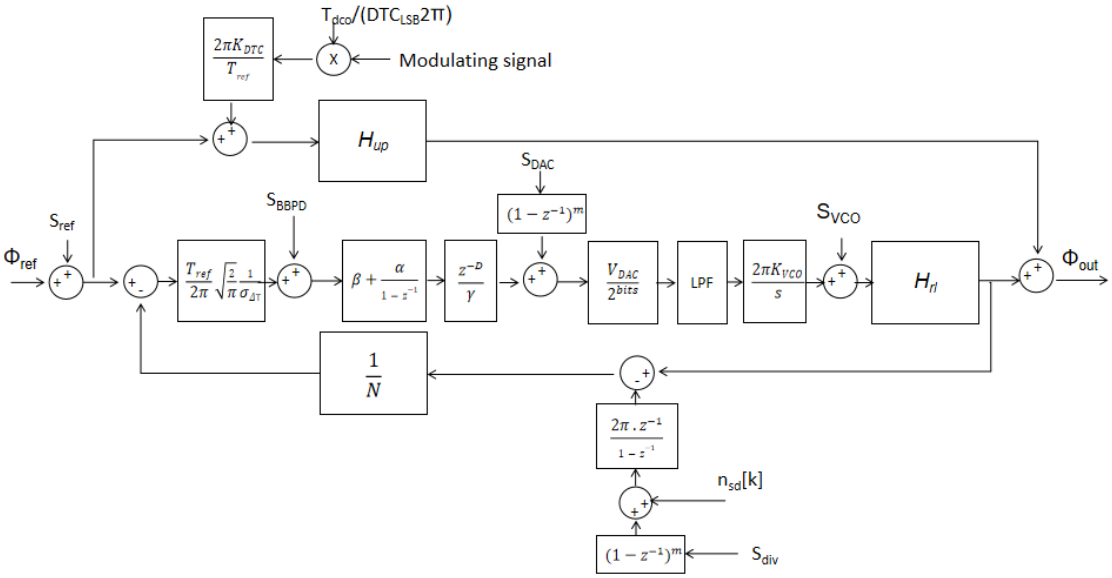



Fig. 4.14: Phase Modulation in MDLL

Phase modulation transfer function is $\frac{\phi_{out}}{\phi_m} = \frac{K_{DTC}}{T_{ref}} \frac{T_{VCO}}{DTC_{LSB}} H_{up}$ where $\phi_m$ is modulating signal and $K_{DTC}$ is DTC gain. Following plot is phase modulation transfer function for DTC gain of 30ps/LSB.

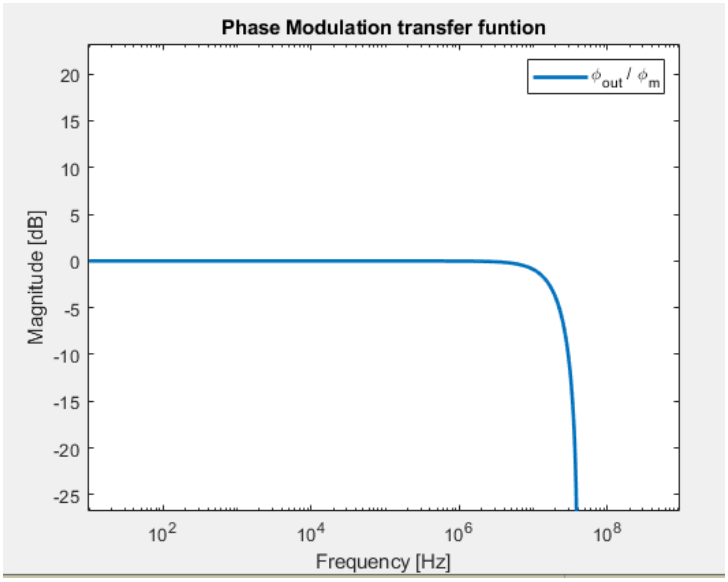



Fig. 4.15: Phase Modulation Transfer function

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