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# INJECTION LOCKED CLOCK MULTIPLIER MODELLING

*A Project Report*

*Submitted by*

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*In the partial fulfilment of requirements*

*For the award of the degree*

*Of*

**MASTER OF TECHNOLOGY**

July, 2021

# CERTIFICATE

This is to undertake that the Project report titled **INJECTION LOCKED CLOCK MULTIPLIER MODELLING**, submitted by me to the Indian Institute of Technology Madras for the award of M.Tech, is a bonafide record of the research work done by me under the supervision of Dr. Saurabh Saxena. In whole or in parts, the contents of this Project report have not been submitted to any other Institute or University for the award of any degree or diploma.

**Place: Chennai 600 036**

**Date: 18th June 2021**

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Project Guide

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Thank you all Rahul Lagisetti

# ABSTRACT

This thesis discusses the fundamentals of PLL, explains the accurate modelling of ILRO for phase noise at the output and compares the results with a TSMC65nm process ILRO design. In the proposed modelling, extracted PDR is used to obtain the injection strength to further include it in the phase domain model of ILRO. This also helps in showing how the reference frequency has a remarkable effect on resetting jitter. This modelled ILRO is incorporated into ILCM for more precise phase noise analysis at the output of oscillator. The proposed model also helps in obtaining an optimum value for fine current step size.

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# ABBREVIATIONS

| | |
|---|---|
| IITM | Indian Institute of Technology Madras |
| ILCM | Injection Locked Clock Multiplier |
| ILO | Injection Locked Oscillator |
| ILRO | Injection Locked Ring Oscillator |
| PLL | Phase Locked Loop |
| CP | Charge Pump |
| PFD | Phase Frequency Detector |
| VCO | Voltage Controlled Oscillator |
| PSD | Phase noise Spectral Density |
| $f_{ugb}$ | Unity Gain Frequency |
| BBPD | Bang Bang Phase Detector |
| IoT | Internet of Things |
| PDR | Phase Domain Response |
| CCO | Current Controlled Oscillator |

# CHAPTER 1

# INTRODUCTION

More systems are connected by IoT, there is a need for more energy-efficient IoT-enabled devices. These devices generate enormous data which is stored and processed by the local servers and large-scale data centers. The battery life is improved if storing, processing and transferring of data is energy- efficient. The systems with wireless and wireline transceivers, clock plays a major role in the power consumption optimization. Hence there is a necessity of clock generator with low power and low jitter.

The research proposed is for low-jitter wide-range frequency synthesizer to implement 128X clock multiplier with two stages. The first stage incorporate delay-locked loop and an edge combiner to implement a 8X clock multiplier using a reference clock of 38.4MHz. The second stage is a 16X clock multiplier uses a injection locked ring oscillator and also embedded with a frequency tracking loop. The second stage is injection locked to the first stage output clock frequency. The ILO resets the accumulated jitter at the output at a sub-harmonic frequency equal to the output frequency of the first stage. The frequency drifts are corrected by FTL

This thesis focuses on the modelling of second stage, mainly incorporates the accurate analysis for PDR of injection locked ring oscillator. The chapter 2 decodes the basics of charge pump based PLL and its limitations in achieving a better noise performance. Chapter 3 exemplifies the PDR analysis and include it in the modelling for accurate analysis. The complete modelling of ILRO with embedded FTL is typified in chapter 4.

# CHAPTER 2

# Fundamentals of PLL

## 2.1 Charge Pump based PLL

The charge pump based PLL is established as shown in Fig. 2.1 using Phase Frequency Detector(PFD), Charge Pump(CP), Loop Filter(LF), Voltage Controlled Oscillator(VCO) and Divider Block(N). The purpose of each block is elucidated below.

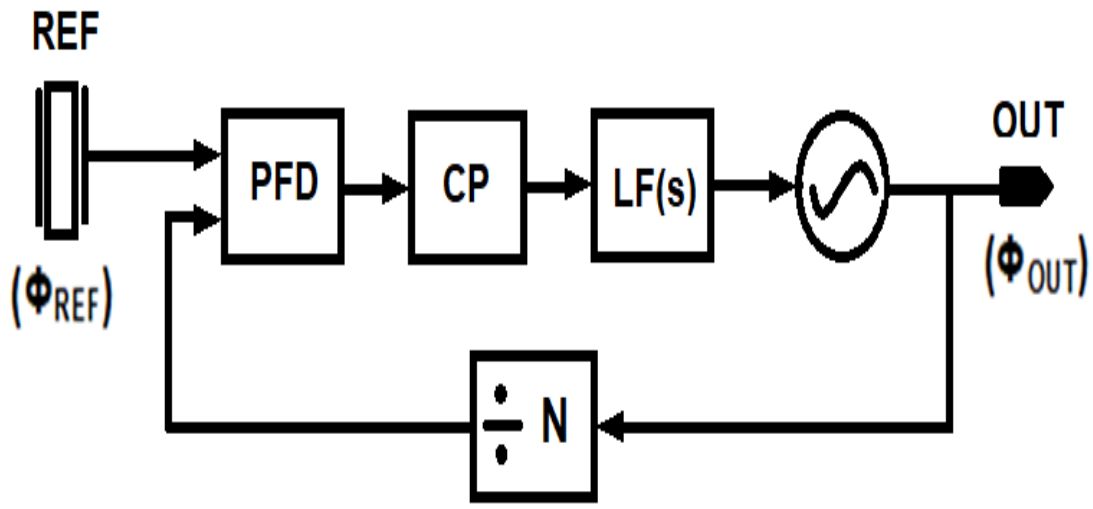


Fig. 2.1: Charge Pump based PLL

### 2.1.1 Phase Frequency Detector(PFD)

The PFD detects the phase difference between the reference clock and the feedback clock from the divider. It generates a pulse width modulated signal proportional to the phase difference between reference and feedback clock.The power consumption of PFD is significant compared to over all power consumption of PLL. So in order to decrease the over all power consumption of PLL we need to minimize the PFD power dissipation.

### 2.1.2 Charge Pump(CP)

A charge pump is purely a bipolar switched current source. The positive and negative current pulses are the outputs which are fed to the loop filter. The pulse width modulated signal is employed by charge pump to generate a control signal that treats the VCO to correct the output clock phase following filtering by the loop filter. The non-idealities in the charge pump such as finite rising and falling time, channel length modulation of transistors results in reference spurs in the output clock.

### 2.1.3 Loop Filter(LF)

The loop filter is decisive in dictating the bandwidth of the PLL. The loop filter without an integrator can only correct the phase change upto $2\pi$ radians i.e. without cycle slipping. In case of cycle slipping, the integral path extracts the DC component and cater the voltage to the VCO for frequency correction. The spurious tones can be attenuated by using an additional capacitor, still the capacitance value being large this upshots the PLL area.

### 2.1.4 Voltage Controlled Oscillator(VCO)

The oscillating frequency of the oscillator is controlled by the input voltage applied to an oscillator. Therefore the VCO is used in PLL whose input voltage is the output voltage of the loop filter. Predominantly there are two types of VCOs used, LC-oscillator and ring oscillators. LC-oscillators uses a parallel resonating LC-tank, these devices noise contribution is ideally zero, they exhibits a good phase noise compared with a ring oscillator. It utilizes a large area and tuning range is small. In case of ring oscillator there are many ways to control frequency, the tuning range is wide and comfortably generates multi-phase outputs. Ring oscillators has poor stability at high frequency in contrast to LC-oscillators. The gain of VCO is constant in case of Ring oscillator, LC-oscillators uses a capacitor bank with overlap bands to keep the gain constant.

### 2.1.5 Divider(N)

The divider in the feedback is used to divide the output frequency to the reference frequency and cater the signal to the PFD. Generally dividers are categorized into integer and factional divider. Multi-Modulus divider is used for integral divisions on the other hand a delta sigma modulator is used in case of fractional division.

## 2.2 Noise Performance And Bandwidth Optimization

All the independent noise sources together put up the output phase noise of the PLL. As shown in Fig. 2.2, the noise sources are added at the output of each block and the power spectral density of the kth noise source represented using $S_k^N(f)$. These noise spectrum gets shaped accordingly depending on the behaviour of the noise transfer function.

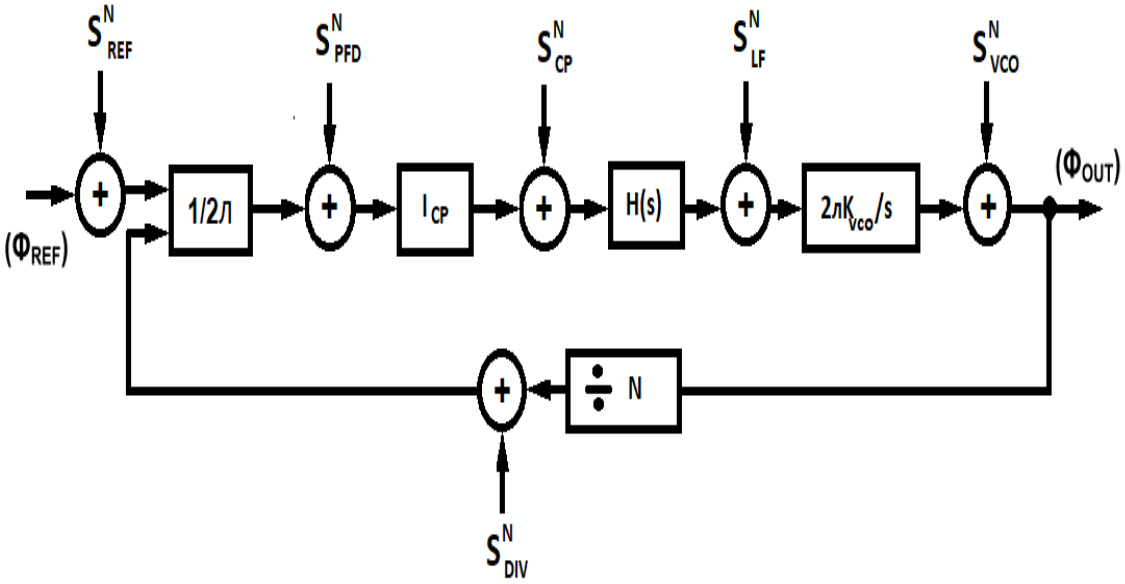


Fig. 2.2: Noise sources in PLL

The noise transfer functions and output power spectral density is evaluated as shown below.

$$\begin{aligned} \mathrm{S}_{OUT}^{N}(f) = S_{REF}^{N}(f)\left|NTF_{REF}(f)\right|^2 + S_{PFD}^{N}(f)\left|NTF_{PFD}(f)\right|^2 + S_{CP}^{N}(f)\left|NTF_{CP}(f)\right|^2 \\ + S_{LF}^{N}(f)\left|NTF_{LF}(f)\right|^2 + S_{VCO}^{N}(f)\left|NTF_{VCO}(f)\right|^2 + S_{DIV}^{N}(f)\left|NTF_{DIV}(f)\right|^2 \end{aligned}$$

$$NTF_{REF}(s) = \frac{N \times LG(s)}{1 + LG(s)} \tag{2.1}$$

$$NTF_{PFD}(s) = \frac{2\pi \times N \times LG(s)}{1 + LG(s)} \tag{2.2}$$

$$NTF_{CP}(s) = \frac{2\pi \times N}{I_{CP}} \frac{LG(s)}{1 + LG(s)} \tag{2.3}$$

$$NTF_{LF}(s) = \frac{2\pi K_{VCO}}{s} \frac{1}{1 + LG(s)} \tag{2.4}$$

$$NTF_{VCO}(s) = \frac{1}{1 + LG(s)} \tag{2.5}$$

$$NTF_{DIV}(s) = \frac{N \times LG(s)}{1 + LG(s)} \tag{2.6}$$

$$TotalJitterR.M.S = \frac{1}{2\pi F_{OUT}} \sqrt{\int S^N_{OUT}(f)df} \tag{2.7}$$

$$whereLG(s) = \frac{I_{CP}}{2\pi \times N} H(s) \frac{2\pi K_{VCO}}{s} \tag{2.8}$$

From the noise transfer functions intuitively we can understand the type of responses. The Phase frequency detector, charge pump, and divider noises are low pass filtered. The loop filter and the VCO are band pass and high pass filtered respectively. At low frequencies the PFD, CP, divider noise dominates and at high frequencies VCO noise is dominated. We can come up with a optimum value of bandwidth which gives a minimal phase noise at the output. The choice of loop filter components begins with the determination PLL bandwidth. The noise bandwidth trade off gives an empirical value for bandwidth, here the noise contribution of the loop and the VCO are equal.

After noise optimization any further finer noise performance can only be established by laying hard limits for the VCO noise or the loop noise contribution therefore resulting in higher power consumption.

# CHAPTER 3

# INJECTION LOCKED RING OSCILLATOR

As explained in the previous chapter the conventional PLL have limitations that obstructs them to achieve a better noise performance, for example in CP based PLL the noise bandwidth trade off impede the noise performance. On an account of this limitation either the loop noise or the VCO noise must have strict bound so that the output noise is reduced. One way is using a sub-sampling based PFD which removes the requirement for divider, therefore attenuating the noise transfer function of the CP and PFD. Due to capture range limitation at lower voltages and large loop filter capacitor is required due to high PFD gain. Another approach is to reset the accumulated random jitter as a regular clock intervals improves the phase noise of the VCO.

## 3.1 Injection locked oscillators

In a free running oscillator the accumulated jitter can be reset by injecting a narrow pulses at a reference clock frequency, narrow pulse generation shown in the fig. 3.1. The injected pulse shorts the output nodes of the oscillator which are of opposite polarity. The free running frequency of the VCO is injection locked to $N \times F_{REF}$ as shown in fig. 3.2

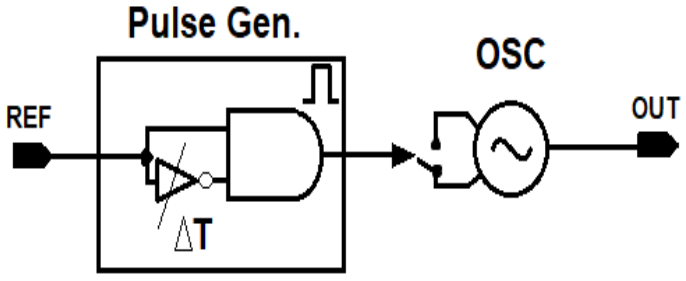


Fig. 3.1: Injection Locked Oscillator

The oscillator phase noise is greatly suppressed around the oscillator frequency when locked to the reference frequency. The higher the reference frequency, the accumulated random jitter is reset at a faster rate thus resulting in even better phase noise.

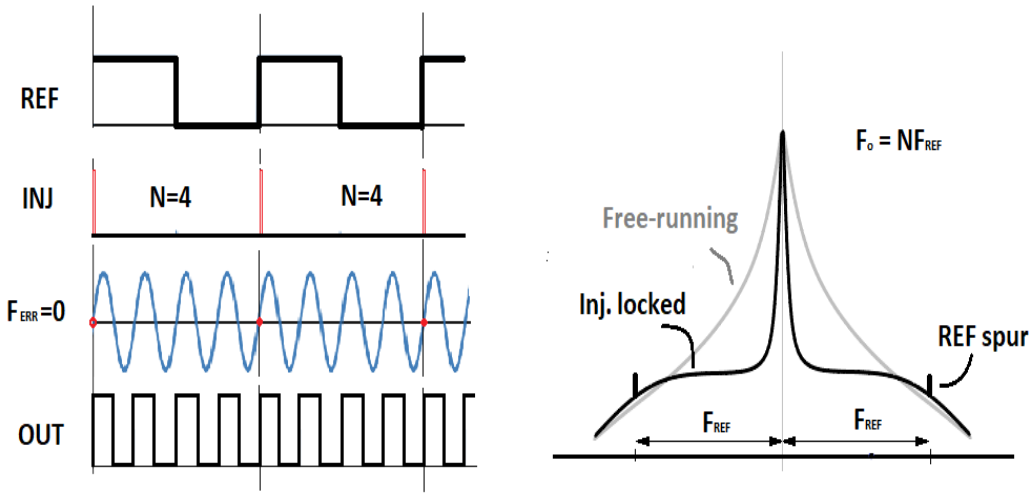


Fig. 3.2: Phase noise when injection locked $F_{ERR} = 0$

Due to supply and temperature variations the oscillator can come out of lock and the phase noise degrades along with increase in reference spurs. It can be interpreted as a pulse is added at reference frequency to the oscillator output to correct the jitter this interfere in a non-linear fashion and results in reference spur.As the oscillator frequency drifts the amplitude of the pulse added increases resulting in increase in reference spur amplitude, this is shown in fig. 3.3. The oscillator phase change is will depend on the position of the pulse with respect to the output phase.

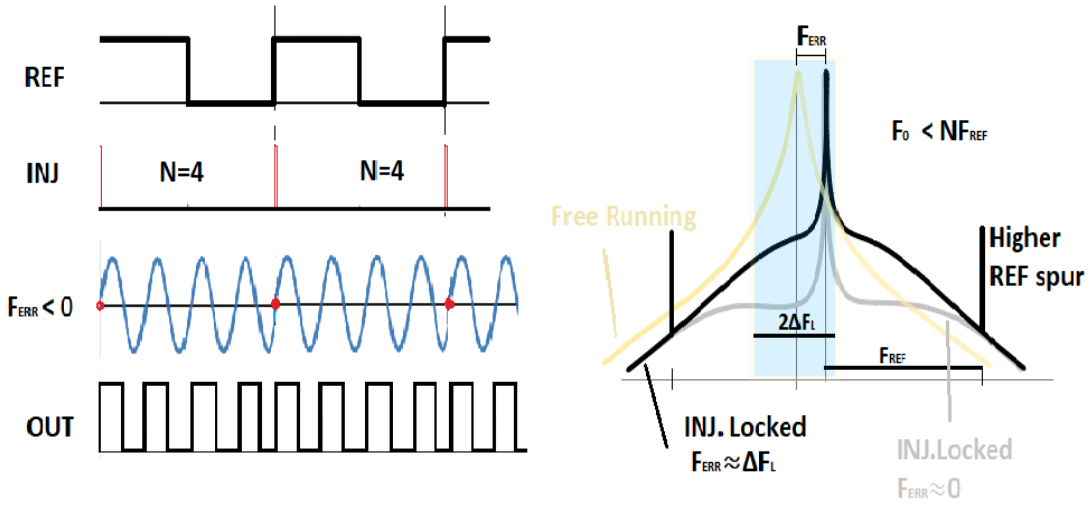


Fig. 3.3: Phase noise when injection locked $F_{ERR} \neq 0$

## 3.2 Phase Domain Response

The pulse injection will disturb the phase and amplitude of the output of the oscillator. As discussed earlier the phase change is dependent on the position of pulse and output phase, therefore when injected at zero crossing will only change phase no change in amplitude and when injected at peak will change the amplitude no change in phase. The phase domain analysis proposed by Elkholy *et al.* (2015) is used for analytical analysis for the phase domain response. The PDR of an ILRO is extracted by varying the injection pulse position relative to the output phase and measuring the steady state change in the output phase after injection. The plot of steady state phase change at the output vs the input relative phase between the injection pulse and the output gives the PDR as shown in fig 3.4.

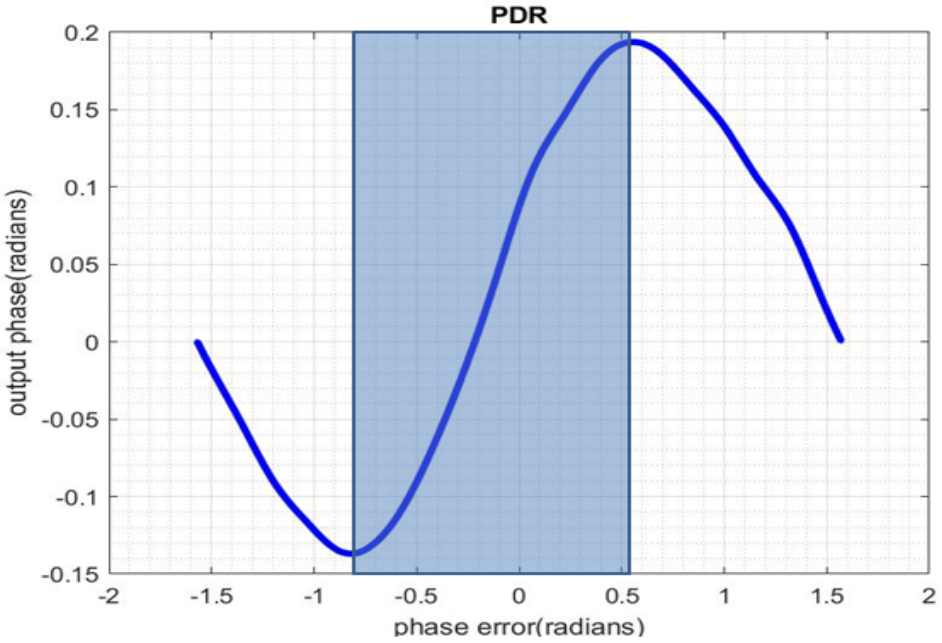


Fig. 3.4: Phase domain response of ILRO

$$B = \frac{d\Phi_0}{d\Phi_{err}} \tag{3.1}$$

The injection strength(B) is slope of the PDR as shown in the equation 3.1, a linear approximation of the curve in the blue shaded region gives a constant injection strength. The shaded region is the lock in range of the ILRO, any input phase error outside thus region makes the system unstable. PDR is periodic with periodicity of $\pi$ radians.

## 3.3 Phase domain model of sub-harmonic ILRO

The sub-harmonic injection output phase is governed by the discrete time equation 3.2. In steady state if the $F_{ERR}$ is zero then the output phase is zero since the input injection will yank the output phase such that following input phase error decreases. Over a period of time the input phase error will settle to a zero and the oscillator gets locked to reference clock $\Phi_i(n+1) = \Phi_i(n)$ and $\Phi_o = 0$ . If the $F_{ERR} \neq 0$ then the output phase will settle to $-2\pi\alpha N$. The phase domain model of ILRO is shown in fig. 3.5.

$$\Phi_i[n+1] = \Phi_i[n] - \Phi_o[n] - 2\pi\alpha N \tag{3.2}$$

where $\alpha = F_{ERR}/F_{FREE}$

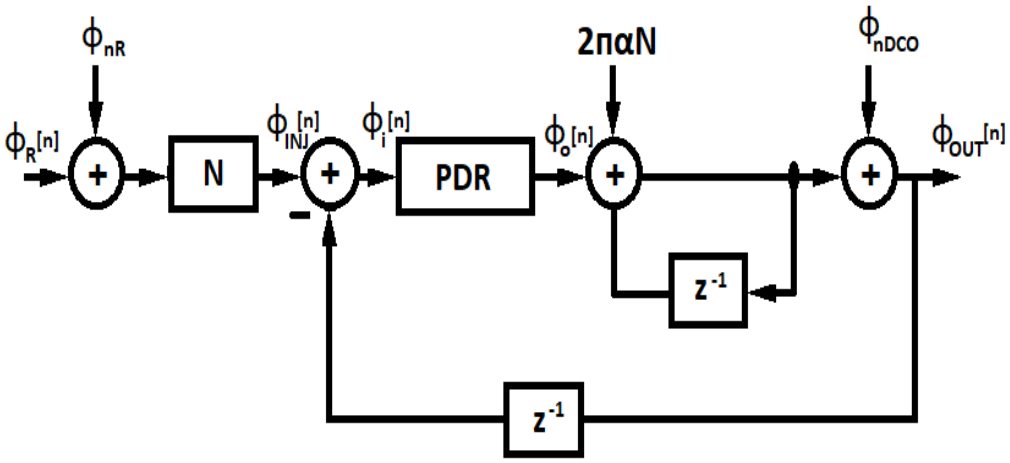


Fig. 3.5: Phase domain model of ILRO.

The reference phase noise is low pass filtered by the loop and the phase noise of the VCO is high pass filtered are also depicted in fig. 3.6. The total output phase noise is calculated as follows.

$$S^{\phi}_{OUT}(f) = S^{\phi}_{REF}(f)\left|NTF_{REF}(f)\right|^2 + S^{\phi}_{VCO}(f)\left|NTF_{VCO}(f)\right|^2$$

$$NTF_{REF}(s) = \frac{N \times LG(s)}{1 + LG(s)} \tag{3.3}$$

$$NTF_{VCO}(s) = \frac{1}{1 + LG(s)} \tag{3.4}$$

$$where \qquad LG(s) = \frac{B(1 - sT_{ref})}{sT_{ref}} \tag{3.5}$$

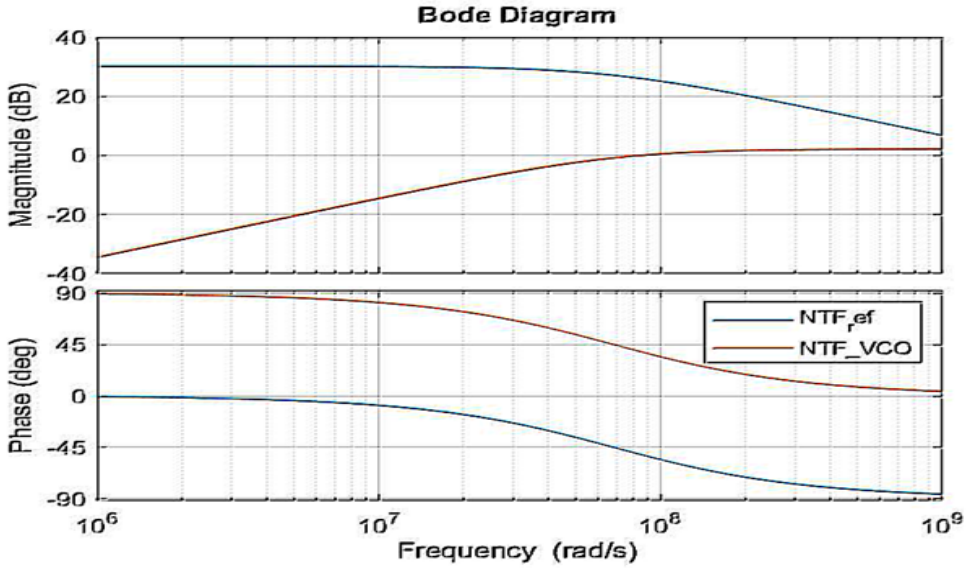


Fig. 3.6: Magnitude and Phase plot of NTFs.

## 3.4 Phase noise of ILRO

The phase noise of the modeled ILRO is compared with the designed ILRO using 65nm process technology, as shown in the fig. 3.7. Here the free running frequency of the oscillator is 4GHz.

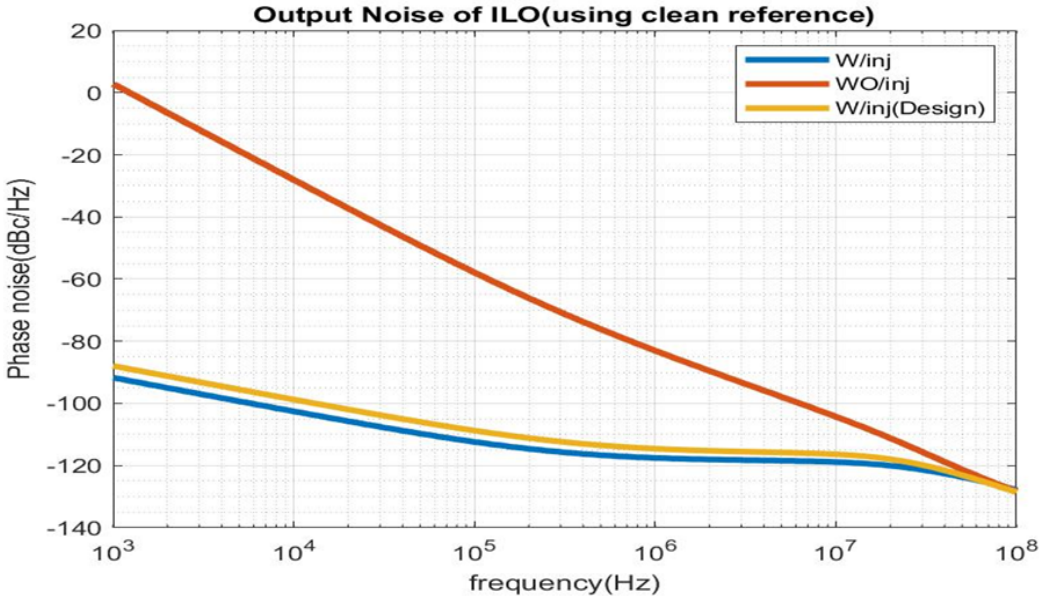


Fig. 3.7: Phase noise of ILRO operating at 4GHz frequency.

The oscillator is injection locked to 250MHz. reference signal, the reference is a

clean signal. The red curve is the phase noise of the free running oscillator. Curve in blue is the phase noise of the modelled ILRO and the yellow curve is the phase noise. The linear approximation in the injection strength resulted in a deviation, it is a time variable entity. The fig. 3.8 the reference frequency is scaled downed by one order i.e., 25MHz the phase noise is has deteriorated by 20dB. This is obvious because the resetting rate of the output clock is decreased resulting in more jittery clock.

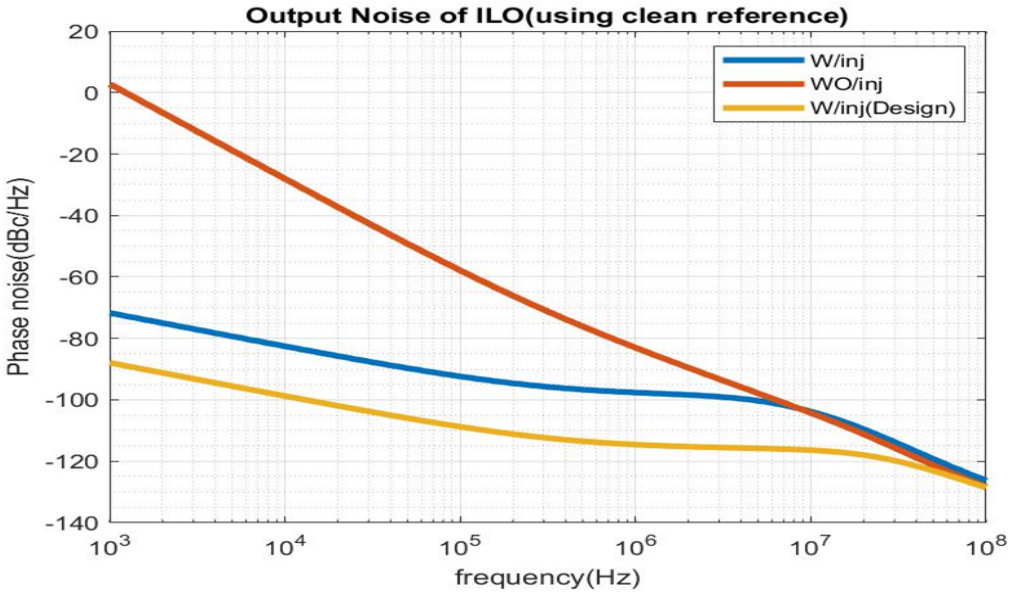


Fig. 3.8: deterioration in phase noise with decrease in ref. frequency.

# CHAPTER 4

# FREQUENCY TRACKING LOOP

Due to supply and temperature variations the output frequency of the oscillator drifts from the free running. This drift in frequency is detected and corrected by an additional loop. This loop continuously tunes the oscillator frequency to $N \times F_{REF}$ ensures the ILRO is locked to the reference frequency.ILRO output is jitter corrected at every reference frequency, this will turn out the FTL loop not detecting the frequency drift. To overcome this the FTL are operated in a time interleaved fashion.

## 4.1 Architecture of ILCM

The block diagram of the ILCM is shown in fig. 4.1, it is embedded with FTL which corrects the frequency drifts in the oscillator and bring it back to lock.

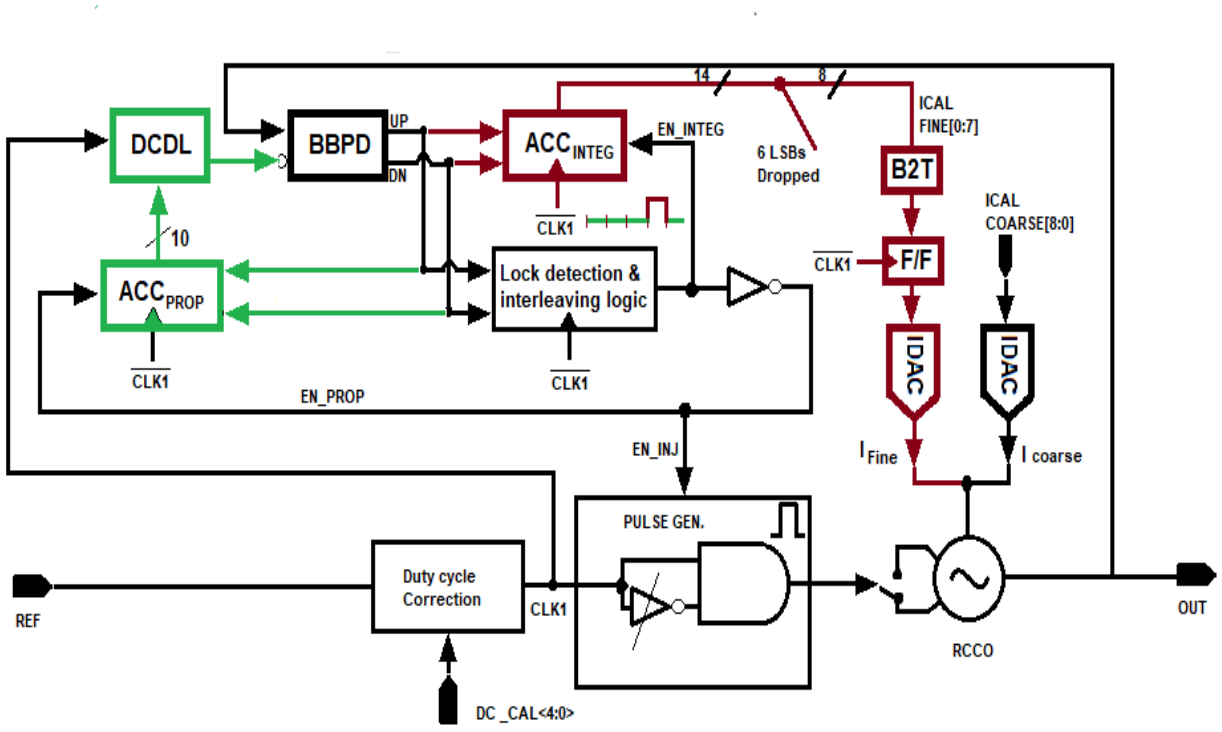


Fig. 4.1: Block diagram of ILRO.

The FTL has two paths proportional path and integral path, which corrects the phase offsets and the frequency drifts respectively.ILCM has BBPD, proportional path, integral path and a gated pulse logic generator.

### 4.1.1 Bang bang phase detector(BBPD)

The BBPD detects the phase error between the input reference and output clock and generate a UP or DW signals accordingly. BBPD has large gain and is dependent on the jitter RMS of reference and output Tertinek *et al.* (2010).

$$K_{BBPD} = \frac{1}{\sqrt{2\pi}\sigma_{\Delta t}} \tag{4.1}$$

where $\sigma_{\Delta t}$ is the R.M.S jitter of both reference and oscillator output

### 4.1.2 Proportional path

Different paths have different delays in ILCM therefore this triggers a false frequency error signal at the BBPD output. So when the ILRO is correcting the jitter, the phase offsets due to different delay paths is corrected by proportional path.The BBPD detects the phase error and accumulator detects this change and correct the delay in digital control delay line. The proportional accumulator holds a value for the offset error as it corrects the offset errors between the reference and the output clock.

### 4.1.3 Integral path

The integral path corrects the drift in output frequency, by fine tuning the current to the current controlled oscillators. The integral path operated every $K^{th}$ cycle of the reference where K=4,8 depending on the BBPD up,dw signals. A pulse is generated which enables the integral path for frequency correction.

## 4.2 Noise analysis of ILCM

The linear model of ILCM is shown in fig. 4.2. The integral path has variable gain the $I_{CAL}$ fine is obtained from the simulation. The DCDL and IDAC contribute quantization noise, the BBPD noise is negligible as it is in multiple feedback path. The FTL operate at a low frequency relative to ILRO , hence its noises are filtered.

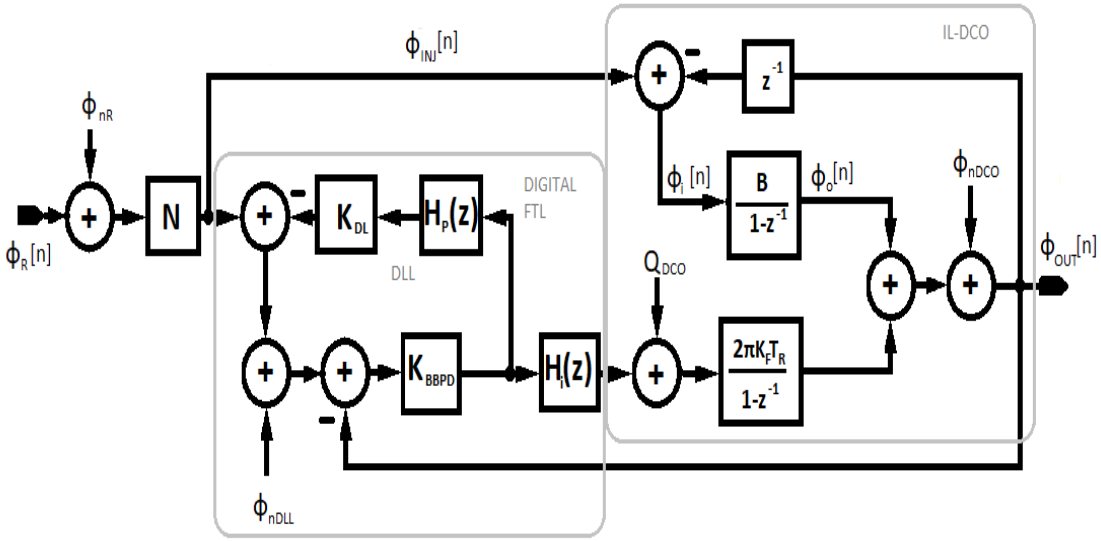


Fig. 4.2: Discrete Time Linear model of ILRO.

The output phase noise is calculated as shown below.

$$S^{\phi}_{OUT}(f) = S^{\phi}_{REF}(f)\left|NTF_{REF}(f)\right|^2 + S^{\phi}_{BBPD}(f)\left|NTF_{BBPD}(f)\right|^2 + S^{\phi}_{DCDL}(f)\left|NTF_{DCDL}(f)\right|^2 + S^{\phi}_{CCO}(f)\left|NTF_{CCO}(f)\right|^2 + S^{\phi}_{IDAC}(f)\left|NTF_{IDAC}(f)\right|^2$$

$$NTF_{REF}(s) = \frac{N}{\frac{T_{int}s^2}{2\pi K_{CCO}K_I K_{BBPD}} + \frac{T_{int}K_{DCDL}s}{2\pi K_{CCO}K_I T_{PROP}} + 1} + \frac{N \times B}{T_{REF}(1-B)s + B} \quad (4.2)$$

$$NTF_{BBPD}(s) = \frac{2\pi K_{CCO}K_I T_{PROP}T_{REF}}{DEN} \quad (4.3)$$

$$where DEN = T_{PROP}T_{REF}T_{INT}(1-B)s^2 + (K_{BBPD}K_{DCDL}T_{INT}T_{REF}(1-B) +$$

$T_{INT}T_{PROP}B)s + K_{BBPD}(2\pi K_{CCO}K_I T_{PROP}T_{REF} + K_{DCDL}T_{INT}B)$

$$NTF_{DCDL}(s) = K_{BBPD}NTF_{BBPD}(s) \tag{4.4}$$

$$NTF_{CCO}(s) = NTF_{BBPD}(s)T_{INT}\frac{T_{PROP}s + K_{BBPD}K_{DCDL}}{T_{PROP}} \tag{4.5}$$

$$NTF_{IDAC}(s) = NTF_{CCO}(s)\frac{s}{2\pi K_{CCO}L_I} \tag{4.6}$$

$$TotalJitterR.M.S = \frac{1}{2\pi F_{OUT}}\sqrt{\int S^{\phi}_{OUT}(f)df} \tag{4.7}$$

The NTF magnitude are shown in fig. 4.3. The reference noise, DCDL noise and BBPD noise are low pass filtered, the noise at the output is high pass filtered.

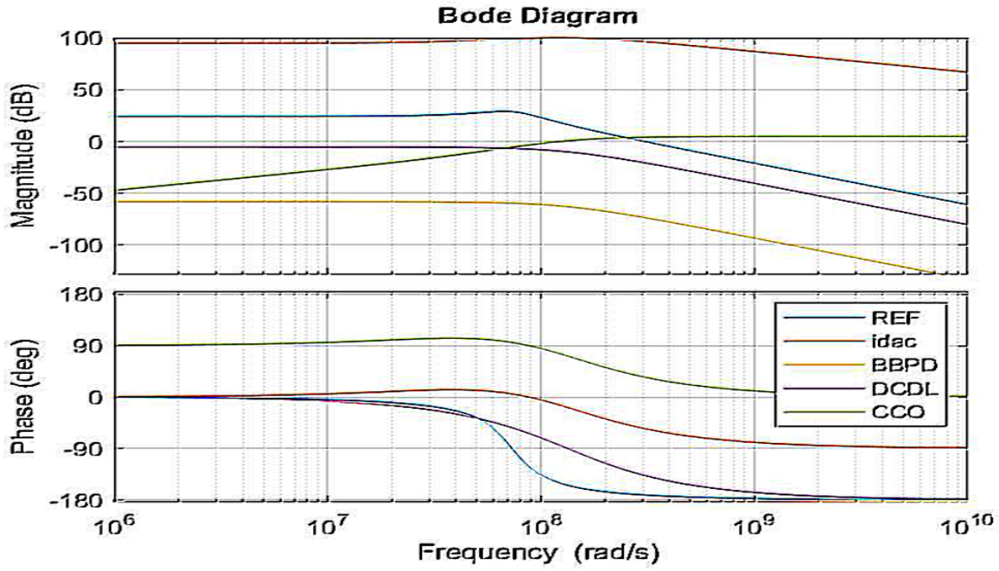


Fig. 4.3: Bode plots of NTFs.

From the plot 4.4 it is clear that the output phase is dominated by the reference noise. Further small improvement in the jitter is obtained by varying the integral path gain.

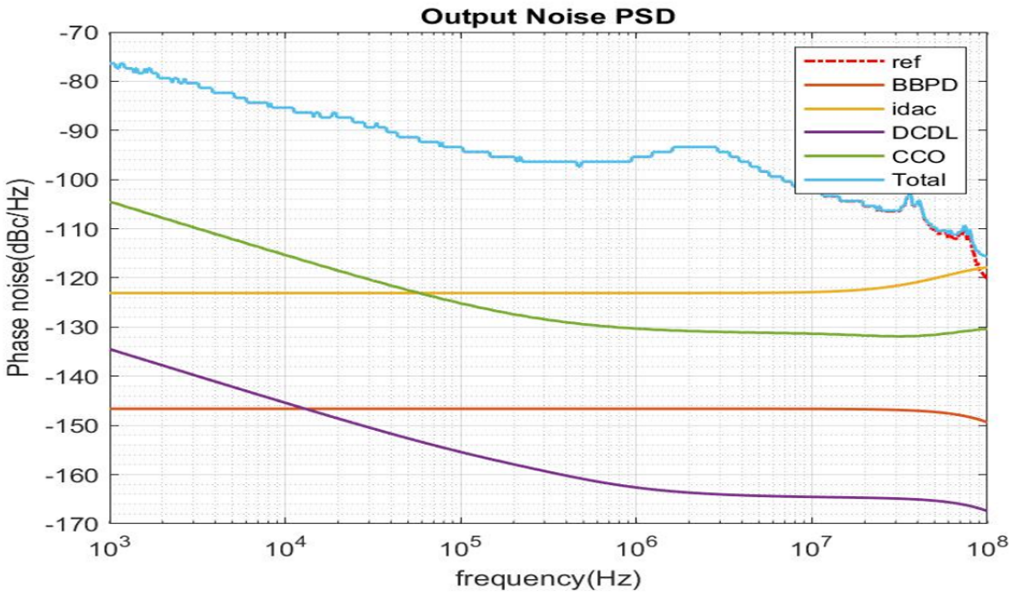


Fig. 4.4: Phase noises at the output.

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