# STUDY AND DEVELOPMENT OF BI-DIRECTIONAL DC-DC CONVERTER

*A Project Report*

*submitted by*

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*in partial fulfilment of the requirements*
*for the award of the degree of*

**MASTER OF TECHNOLOGY**


**DEPARTMENT OF ELECTRICAL ENGINEERING**
**INDIAN INSTITUTE OF TECHNOLOGY MADRAS**

**JUNE 2021**

# CERTIFICATE

This is to certify that the thesis titled **STUDY AND DEVELOPMENT OF BI-DIRECTIONAL DC-DC CONVERTER** ,submitted by **SCARIA THOMAS**,to the Indian Institute of Technology Madras,for the award of the degree of **Master of Technology**,is a bona fide record of the research work done by him under my supervision. The contents of this thesis , in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Place: Chennai

Date: 20th June 2021

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# ACKNOWLEDGEMENTS

First and foremost,I would like to thank Almighty God for his showers of blessings and helping me overcome the stumbling obstacles.

The completion of my work would not have been possible without the excellent guidance, expertise and motivating support of my guide, Prof. Kamalesh Hatua and no amount of gratitude and thanks would be enough. I consider myself fortunate and privileged to work under his supervision.

I thank all of my lab members for their support and guidance.

I also take this opportunity to thank my family for their constant support and motivation.

Last, but not the least, I would like to thank all the professors of the institute for helping me to elevate my knowledge to what it is now. I consider myself lucky to have utilized their wisdom and knowledge.

# ABSTRACT

Among the significant issues in static power converters are high switching frequency and high efficiency. However, switching losses usually limit switching frequencies. Presently, hard-switching buck/boost converters are dominantly used for automotive applications. Automotive applications have stringent system requirements for dc-dc converters, such as wide input voltage range and limited EMI noise emission. High switching frequency of the dc-dc converters is much desired in automotive applications for avoiding AM band interference and for compact size. However, hard-switching buck converter is not suitable at high frequency operation because of its low efficiency. In addition, buck converter has high EMI noise due to its hard-switching.Therefore, soft-switching topologies are considered in this thesis work to improve the performance of the dc-dc converters.

Another approach in the development of bidirectional dc-dc converter is using the principle interleaving or multi-phasing the converter and directing the power flow into different parallel section keeping the input and output voltage same.The load is met through the control of each parallel section

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# ABBREVIATIONS

| | |
|---|---|
| GaN | Gallium nitride |
| SiC | Silicon Carbide |
| ZVS | Zero Voltage Switching |
| ZCS | Zero Current Switching |
| PWM | Pulse Width Modulator |
| FET | Field Effect Transistor |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| PM | Phase Margin |
| FPGA | Field Programmable Gate Array |

# CHAPTER 1

# Introduction

As the need for power electronics converters are increasing mainly in the automobile sector due to the need of changing more into hybrid and electric vehicles for cost efficient and environmentally friendly operation, the need for efficient and compact converters are required. In order to reduce the size of the converter and to improve the efficiency, the losses have to reduce. The losses mainly are the conduction and switching losses. The switching losses is due to the overlap of voltage and current during transition. One way reducing the switching losses is by using resonant converter [1]. By reducing the switching losses, the switching frequency can be increased. The size of the converters mainly depends on the magnetic and electrostatic components like inductor, capacitor and transformer. By increasing the switching frequency of operation, the size of these components can reduce and the compactness of the converter can be improved.

## 1.1 Background

As the need for DC-DC converter is increasing in the automobile sector mainly in onboard charging technology for electric vehicle charging, the need for efficient converter with compact size is required. Thus more and more research are moving into resonant converter thus to reduce the switching losses and to improve the switching frequency and making the converter more compact

The development in the field of silicon semiconductor has reached to a limit and any advancement further is not possible. So more resarch is going in the field of wide band gap devices like Gallium Nitride(GaN) and Silicon Carbide(SiC). The developments in these field are in the beginning stage and have more advantages compared to old Silicon technology in the converter application

## 1.2 Goals Of Project

The report mainly discusses the use of GaN semiconductor that will mostly replace Si soon for high frequency DC-DC converters. Implementation of a new type of DC-DC converter topology using series resonance is needed to be done shall be studied.Average current mode control of DC-DC converter is also being discussed.

## 1.3 Outline of the thesis

In Chapter 2 a very basic description of the superiority of GaN over Si based switches will be discussed, various types of GaNFETs available in today's market and their manufacturers, the use of GaN will be discussed as well.

In Chapter 3 start off with the various type resonant converters and detailed study of quasi resonant converters is also done

In Chapter 4 A new topology of resonant converter is being discussed with the detailed explanation for different modes of operation

In Chapter 5 The average current mode control is explained with buck converter as example.Simulation studies are also being done.

In Chapter the conclusion of the work is mentioned

# CHAPTER 2

# Gallium Nitride (GaN)

## 2.1 About GaN

Most electronics today are based on silicon. Most of the present research are in the field of wide band gap devices like GaN and SiC. Gallium itself is a silvery metal melting at 85F in our palm. In its pure form is not good to use due to its melting at small temperature. It forms a number of interesting compounds. GaAs is used as semiconductor. Cell phone has GaAS as radio amplifier. GaN forms a hard yellowish crystal.

GaN is a semiconductor. The valence electron of semiconductor is some what lazy and when supplied from external means like heat it starts conducting and let electricity fall. Then they move from the valence band to conduction band. Gan is interesting because the band gap, the amount of energy needed to kick electron from valence band to conduction band is about three times than of Si. For Si it is about 1.12ev and for GaN it is 3.4ev. It is harder to switch between insulator to a conductor. It had many benefits; the semiconductor can operate at very high temperature. GaN transistor can operate at a temperature about 300C. GaN also have a high breakdown voltage compared to silicon.

The bandgap of GaN is about three times than that of silicon 2. They are labelled as wide band gap materials. This means that the bonds are three times stronger and high breakdown field in WBG materials. For a given voltage the critical electrical field will decide how close the terminals can bring close before the arcing occurs. For GaN it is ten times stronger implies for a given voltage, smaller is the distance between the Drain and the Source which means the electron don't have to travel much and this reduces the ON resistance. The electron mobility that implies how sticky the electrons are, higher this value they are freer to move. GaN has high electron mobility this reduces the ON

resistance. The properties mentioned before makes Gan a device with superior ON resistance, breakdown voltage and lesser in size.

## 2.2 Working of GaN

GaN is inherently piezoelectric that is if we apply pressure on a layer of GaN, it produces voltage or electrons [3]. Now if we apply a layer of AlGaN on it, more electrons are produced off the same strain, this produces a 2D-electron gas resulting in higher current through it.

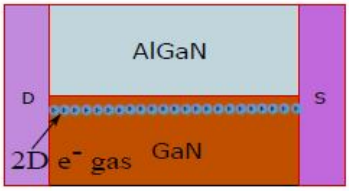


Fig. 2.1: Production of 2D e gas

## 2.3 Types Of GaN

1. Depletion mode type: A Depletion Mode type GaNFET is a naturally ON type device but when a negative gate-source voltage is applied it is turned OFF [4]. Depletion mode transistors are inconvenient because, at start-up of a power converter, a negative bias must first be applied to the power devices or a short circuit will result.

2. Enhancement mode type: In recent times a new technology of GaNET has been developed namely the Enhancement mode type or eGANFETs, in such technology when a zero voltage is applied on the gate, the electrons are wiped off and the device turns off and when a positive voltage is applied to the gate it pulls the electrons to the surface completing the circuit hence turning ON the device.

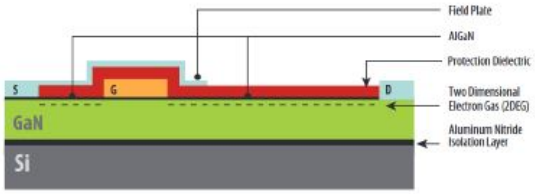


Fig. 2.2: Enhancement mode GaN

## 2.4 Manufactures of GaN

Few manufacturers of GaN devices in today's market are[11]: Exagan, EPC, Transphorm, Infineon, Cree, e-Front Runners, Global Power Technologies, Panasonic, Fairchild Semiconductors, Rohm, GaN Systems, ON Semiconductor, Avago Technologies. Among the above stated manufacturers the leading vendors[11], Infineon uses CoolGaN Technology, EPC uses eGaN Technology and Transphorm uses Cascode Technology

## 2.5 Usage of GaN

Due to their capability of handling very high frequencies, GaNs can potentially be used in Microcontrollers, SSDs, antennas, RF MOSFETs, RF Amplifiers, RF Switch ICs, Power MOSFETs, High Power LEDs and Batteries.

## 2.6 Conclusion

In summary, a discussion has been done on GaN in today's market. We also see the amny reasons making GaN as the probable substitute to Si based devices in the near future. Out of the many mentioned uses of GaN in Power Electronics Field GaNFET's are gaining more popularity due to there ability to switch at such high frequencies hence developing a compact and efficient converter for high power ratings shall remain no longer a challenge.

# CHAPTER 3

# Resonant Converters

The major thrusts in switching converter design are to achieve a higher power packing density and higher conversion efficiency. To increase the power packing density, the switching frequency of the switching converter is often increased to reduce the size and weight of its reactive components[5]. However, the conventional or hard-switching switching converter, employing pulse-width modulation to control the dynamic transfer of electrical energy from the input to the output, suffers an excessive switching loss as its switching frequency approaches 1MHz.

The higher switching losses of the power transistor require a larger heat sink capacity that offsets the net magnetic size reduction when operating at a higher switching frequency. At high switching frequencies, capacitive turn-on losses in power MOSFETs become the predominant switching loss.

Resonant converters offer an attractive solution to the above dilemma. There are many topological variations of the resonant converter. The main two of the common resonant converter topologies are the quasi-resonant converter and the load-resonant converter.

One of the major advantages of resonant converters is the absorption of the switching transistor capacitance and other parasitic components into the converter topologies. However, the switching transistors in the resonant converters generally have to carry a higher peak current or voltage for the same output power than their counterparts in conventional switching converters. Since resonant converters regulate their output by changing their switching frequencies or by frequency modulation, electromagnetic interference may be unpredictable. The choice of using resonant converters over conventional switching converters should be based on the fact that the reduction in switching losses is greater than the increase in semiconductor device conduction losses associated with the higher peak current or voltage in the resonant topologies.

## 3.1 QUASI RESONANT CONVERTERS

### 3.1.1 INTRODUCTION

The quasi-resonant converter employs an LC tank circuit to shape the current or voltage waveform of the switching transistor, resulting in a zero-current or zero-voltage condition during device turn-off or turn-on [6]. Zero-current-switching quasi-resonant switches are employed to reduce the turn-off switching losses, while zero-voltage-switching quasi-resonant switches are used to mitigate the turn-on switching losses. In general, zero-voltageswitching is preferable to zero-current-switching at high switching frequencies.

The main two type of quasi resonant converters are

1 Zero voltage switching(ZVS)

2 Zero current switching(ZCS)

The principle in quasi resonant converter is that the normal switches in the DC-DC converter like buck and boost are replaced by resonant switches[7]. The two main type of resonant switches are the L=type and M-type.

All the basic switching converter topologies can be converted into quasiresonant converters simply by replacing the switching transistor with either the current-mode or voltage-mode quasi-resonant switch. They are called quasi-resonant converters because there are resonant and non-resonant intervals in the switching waveforms

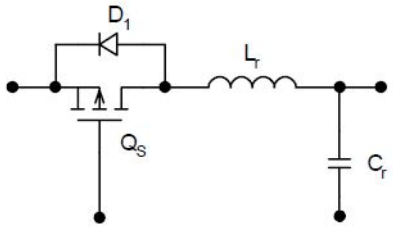


Fig. 3.1: L-Type Switch [7]

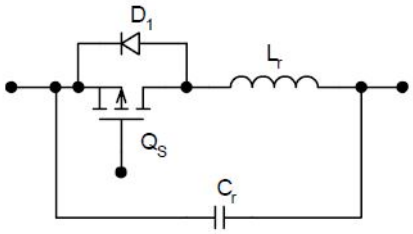


Fig. 3.2: M-Type Switch[7]

## 3.2 ZVS-BUCK CONVERTER

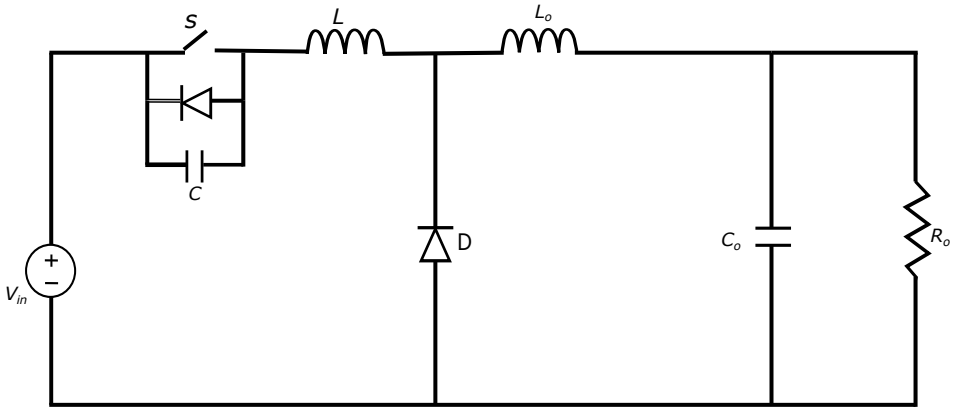


Fig. 3.3: ZVS Buck Converter Circuit

The fig 3.3 shows the circuit diagram for the ZVS-BUCK converter with the M-type switch. The inductor(L) and the capacitor(C) forms the resonant switch element. The equivalent circuit is given in fig 3.4 with constant input voltage source and output constant current source. The analysis of the circuit can be done using the equivalent circuit and can be divided into four modes

### 3.2.1 MODE 1 $t_0 < t < t_1$

The MODE1 circuit is given fig 3.5. Assume initially for t<0 the switch S is conducting and the diode D is turned OFF.In this mode, since switch has been closed for t<0 the initial capacitor voltage(Vc) is zero and the inductor current is Io

$$v_c(0) = 0 \tag{3.1}$$

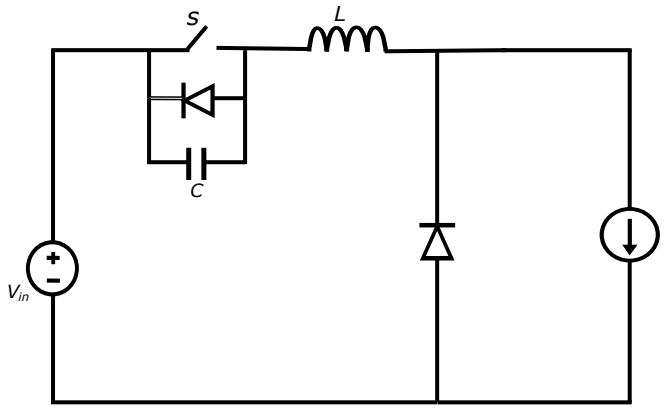


Fig. 3.4: ZVS Buck Equivalent Circuit

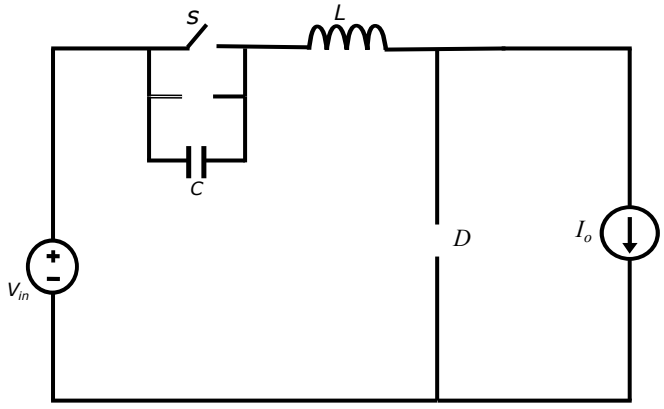


Fig. 3.5: MODE1 Circuit

$$i_l(0) = I_o \tag{3.2}$$

$$C\frac{dv_c}{dt} = i_l(t) \tag{3.3}$$

$$v_c(t) = \frac{I_o t}{C} \tag{3.4}$$

The voltage across the diode $V_{in}$-$v_c(t)$ . As long as $v_c < V_{in}$ the diode remain OFF. The capacitor voltage reaches the input voltage at $t = t_1$ causing the diode to turn On. Hence at $t = t_1$, we have

$$v_c(t_1) = V_{in} \tag{3.5}$$

At t=$t_1$ the circuit enters MODE2

$$t_! = \frac{CV_{in}}{I_O} \tag{3.6}$$

### 3.2.2 MODE 2 $t_1$<t<$t_2$

This mode starts at $t_1$ and the circuit enters into the resonant stage. During the time between $t_1$ and $t_2$ the switch remains OFF. At $t = t_2$ the capacitor voltage tends to go negative forcing the diode across switch S to turn ON as shown in fig 3.7.Thus at the end of $t_2$ the switch can turned ON at zero voltage

$$v_c(t_1) = V_{in} \tag{3.7}$$

$$i_l(t_1) = I_0 \tag{3.8}$$

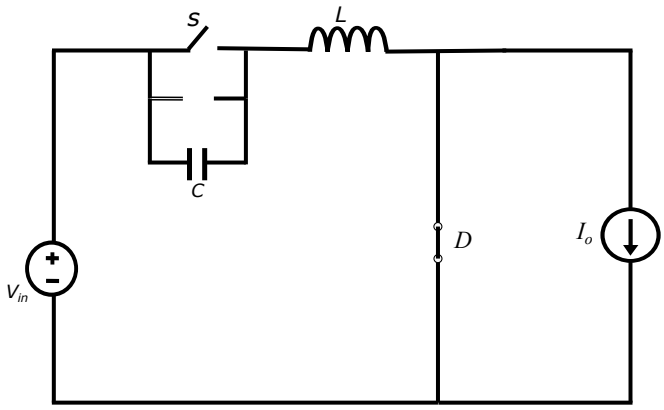


Fig. 3.6: MODE2 Circuit

The expression for the resonant inductor current and capacitor voltage in this time domain are

$$i_l(t) = I_o \cos \omega_o(t - t_1) \tag{3.9}$$

$$v_c(t) = V_{in} + I_o Z_o \sin \omega_o(t - t_1) \tag{3.10}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \quad Z_o = \sqrt{\frac{L}{C}} \tag{3.11}$$

$$t_2 - t_1 = \frac{1}{\omega_o} \sin^{-1}(\frac{-V_{in}}{I_o Z_o}) = \frac{\alpha}{\omega_o} \tag{3.12}$$

at $t = t_2$ the inductor current is

$$i_l(t_2) = I_o \cos(\alpha) \tag{3.13}$$

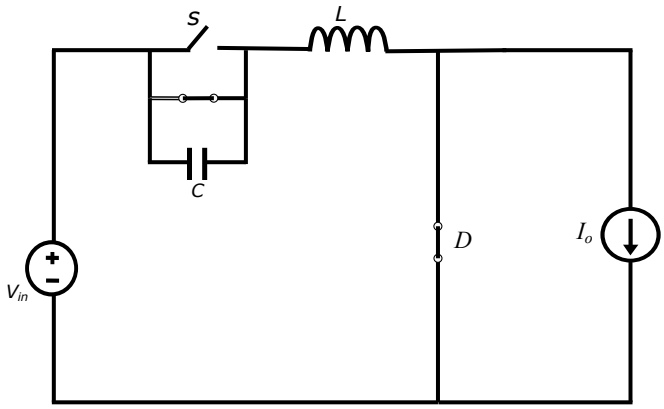


Fig. 3.7: Circuit At Instant of Turn ON

### 3.2.3 MODE 3 $t_2$<t<$t_3$

At $t_2$ the capacitor voltage becomes zero then negative so the body diode conducts and at this instant switch can turned On. During this mode both the switch and diode conducts and this continues until the inductor current reaches the output current after that the diode stops conducting. The fig 3.8 shows in circuit in MODE3.
The initial value of capacitor voltage at MODE3 is zero

$$vc(t_2) = 0 \tag{3.14}$$

The voltage across inductor is input voltage

$$\frac{Ldi_l}{dt} = V_{in} \tag{3.15}$$

$$i_l(t) = \frac{V_{in}(t - t_2}{L} + I_o \cos\alpha \tag{3.16}$$

At t= $t_3$ the inductor current reaches the output current $i_l(t_3) = I_o$, forcing the diode to turn OFF. The interval is given

$$t_3 - t_2 = \frac{I_o L(1 - \cos\alpha}{V_{in}} \tag{3.17}$$

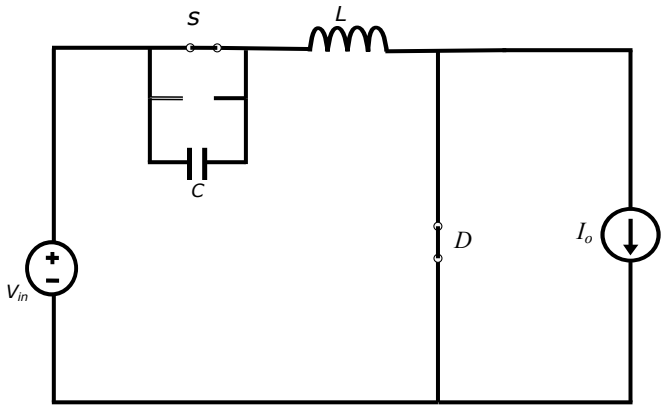


Fig. 3.8: MODE3 Circuit

### 3.2.4 MODE 4 $t_3 < t < t_4$

From $t_3$ the MODE4 begins in which the switch remains turned ON.

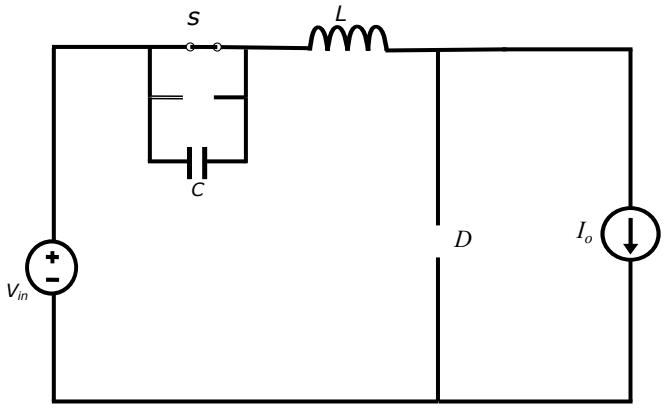


Fig. 3.9: MODE4 Circuit

The turn ON time of the circuit is fixed and the output voltage is varied by varying the turn OFF time. MODE 4 will continue as long as the switch remains ON By turning OFF the switch at t=$t_4 = T_s$ the switching cycle repeats. The dead time $t_4 - t_3$ is given by

$$t_4 = t_3 = T_s - t_1 - (t_2 - t_1) - (t_3 - t_2) \tag{3.18}$$

## 3.3 ZCS-BOOST CONVERTER

The below fig 3.10 shows the boost converter with resonant switch for ZCS operation.

The sequence of operation[8] in each switching cycle can be given in the following

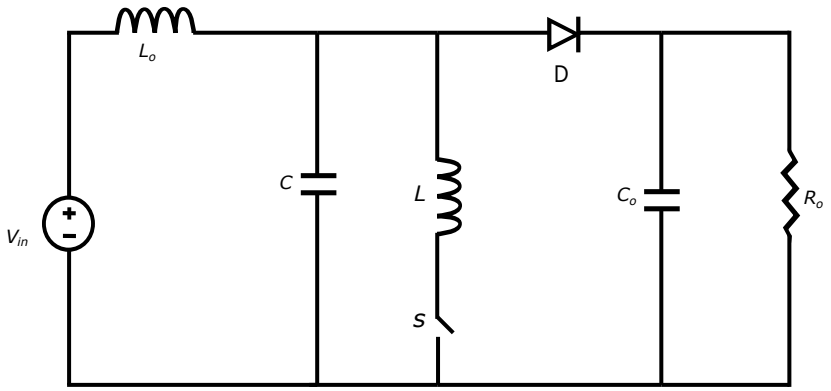


Fig. 3.10: ZCS Boost Circuit

four modes

1 Charging of inductor at constant voltage

2 Resonant mode operation

3 Charging of capacitor at constant current

4 Load current freewheeling through the diode

The fig 3.11 shows the equivalent circuit with constant current input $I_{in}$ and constant voltage source $V_o$. The operation of the circuit can be explained in four different modes.

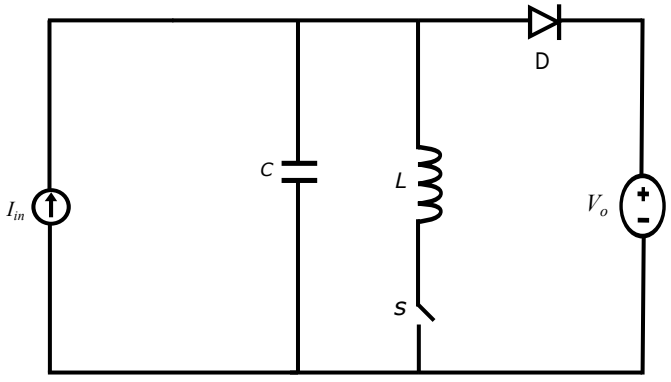


Fig. 3.11: ZCS Boost Equivalent Circuit

### 3.3.1 MODE 1 $t_0$<t<$t_1$

The fig 3.12 shows the equivalent circuit in MODE1. For $t < 0$ the switch is turned OFF and the resonant capacitor is charged to the output voltage. At $t = 0$ the switch is turned ON and the inductor starts charging at constant voltage

$$V_{in} = \frac{Ldi_l}{dt} \tag{3.19}$$

The initial conditions at t=0 are

$$i_l(0) = 0 \qquad v_c(0) = V_o \tag{3.20}$$

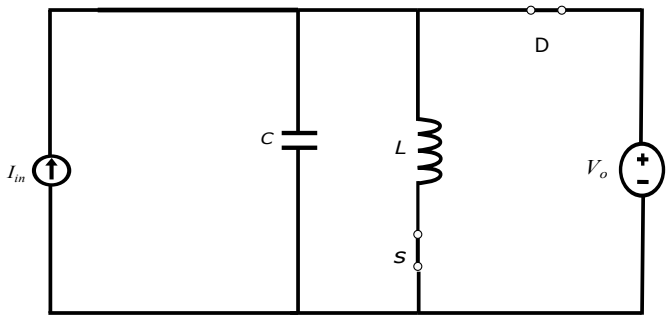


Fig. 3.12: MODE1 Circuit

The resonant inductor current

$$i_l(t) = \frac{V_o t}{L} + i_l(0) = \frac{V_o t}{L} \tag{3.21}$$

This mode continues until the inductor current becomes $I_{in}$ and the diode is reverse biased The time $t_1$ is given

$$t_1 = \frac{I_{in} L}{V_o} \tag{3.22}$$

### 3.3.2 MODE 2 $t_1$<t<$t_2$

The resonant condition begins in this mode with initial conditions are

$$v_c(t_1) = V_o \qquad i_l(t_1) = I_{in} \tag{3.23}$$

The circuit equation during this period

$$\frac{Ldi_l}{dt} = v_c(t) \tag{3.24}$$

$$\frac{Cdv_c(t)}{dt} = I_{in} = i_l(t) \tag{3.25}$$

Solving the above equation using Laplace transform

$$i_l(t) = I_{in} + \frac{V_o \sin \omega_o(t - t_1)}{Z_o} \tag{3.26}$$

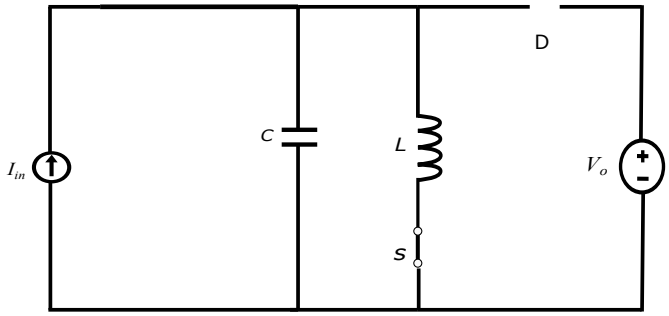


Fig. 3.13: MODE2 CIrcuit

$$v_c(t) = V_o \cos \omega_o(t - t_1) \tag{3.27}$$

The inductor current becomes zero at $t_2$. At this instant the switch is opened at zero current

$$(t_2 - t_1) = \frac{1}{\omega_o} \sin^{-1}(\frac{-I_{in}Z_o}{V_o}) \tag{3.28}$$

$$= \frac{1}{\omega_o}[\pi + \sin^{-1}(\frac{I_{in}Z_o}{V_o})] \tag{3.29}$$

### 3.3.3 MODE 3 $\mathbf{t_2}$<t<$\mathbf{t_3}$

During this the capacitor is charged at constant input current and this continues until the diode is forward biased

$$v_c(t) = \frac{1}{c} \int I_{in} dt \tag{3.30}$$

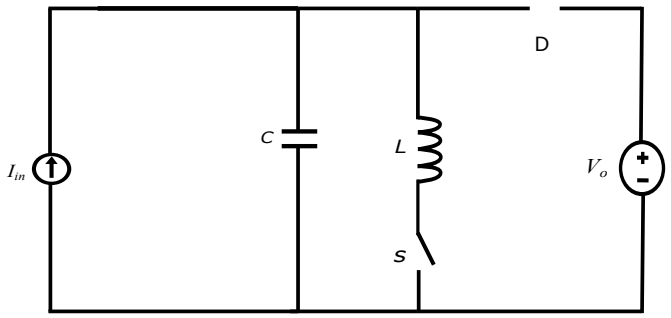


Fig. 3.14: MODE3 Circuit

$$\frac{I_{in}(t-t_2}{C}+v_c(t_2) \tag{3.31}$$

At t=$t_3$ the capacitor is charged to the output voltage

$$v_v(t_3)=V_o=\frac{I_{in}(t_3-t_2}{C}+v_c(t_2) \tag{3.32}$$

The mode three interval is given by

$$t_3-t_2=\frac{C[V_o-v_c(t_2)]}{I_{in}} \tag{3.33}$$

### 3.3.4 MODE 4 $t_3<t<t_4$

In this mode the input current freewheel through the diode to the output. This mode continues until the switch is turned ON and the cycle repeats

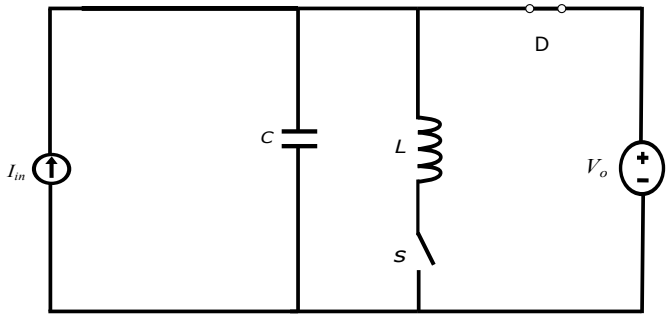


Fig. 3.15: MODE4 Circuit

$$t_4-t_3=T_s-t_1-(t_2-t_1)-(t_3-t_2) \tag{3.34}$$

### 3.3.5 DESIGN EXAMPLE

For a simple design consider $V_{in}$=20V $V_o$=40V $P_o$=20W and the normalized frequency $f_{ns}$=.38 Gain M=

$$M = \frac{V_o}{V_{in}} = \frac{40}{20} = 2 \tag{3.35}$$

$$Z_o = \frac{R_o}{Q} = \frac{V_o^2}{P_o Q} = \frac{80}{6} = 13.33 \tag{3.36}$$

$$f_o = \frac{f_s}{f_{ns}} = \frac{250}{.38} = 657.89kHz \tag{3.37}$$

$$L = \frac{Z_o}{2\pi f_o} = \frac{13.33}{2\pi 657.89 * 10^3} = 3.22 * 10^{-6}H \tag{3.38}$$

$$C = \frac{1}{Z_o \omega_o} = \frac{1}{13.33 * 2 * \pi 657.89 * 10^3} = 18.14nF \tag{3.39}$$

The input inductor and output capacitor are selected such that

$$L_o = 100 * L = 322 * 10^{-6}H \tag{3.40}$$

$$C_o = 100C = 1814nF \tag{3.41}$$

MODE 1 time

$$t_1 = \frac{I_{in} L}{V_o} \tag{3.42}$$

Equating input and output power we have

$$I_{in} * V_{in} = V_o * I_o \tag{3.43}$$

$$I_{in} * 20 = 40 * \frac{40}{80} \tag{3.44}$$

Substituting in 3.42 we get

$$t_1 = .805\mu \tag{3.45}$$

MODE2

$$(t_2 - t_1) = \frac{1}{\omega_o} \sin^{-1}(\frac{-I_{in} Z_o}{V_o}) \tag{3.46}$$

$$= \frac{1}{\omega_o}[\pi + \sin^{-1}(\frac{I_{in} Z_o}{V_o})] \tag{3.47}$$

From 3.46 and 3.47

$$t_2 - t_1 = .8422\mu s \tag{3.48}$$

$$t_2 = .9226\mu s \tag{3.49}$$

This is the actual turn ON time of the switch we need to turn OFF at $t_2$

MODE3

$$t_3 - t_2 = \frac{V_o(1 - \cos\alpha)}{\omega_o Z_o I_{in}} \tag{3.50}$$

$$t_3 - t_2 = 1.4115\mu s \tag{3.51}$$

MODE 4

$T_s = \frac{1}{250KHz} = 4\mu s$ The duty cycle for this fixed frequency

$$D = \frac{t_2}{T_s} = 2.306 \tag{3.52}$$

### 3.3.6 Simulation Result Of ZCS Boost Converter

Based on the design procedure stated in section 3.3.6 simulation in MATLAB Simulink was and the resulting waveform is shown in fig 3.16 and3.17

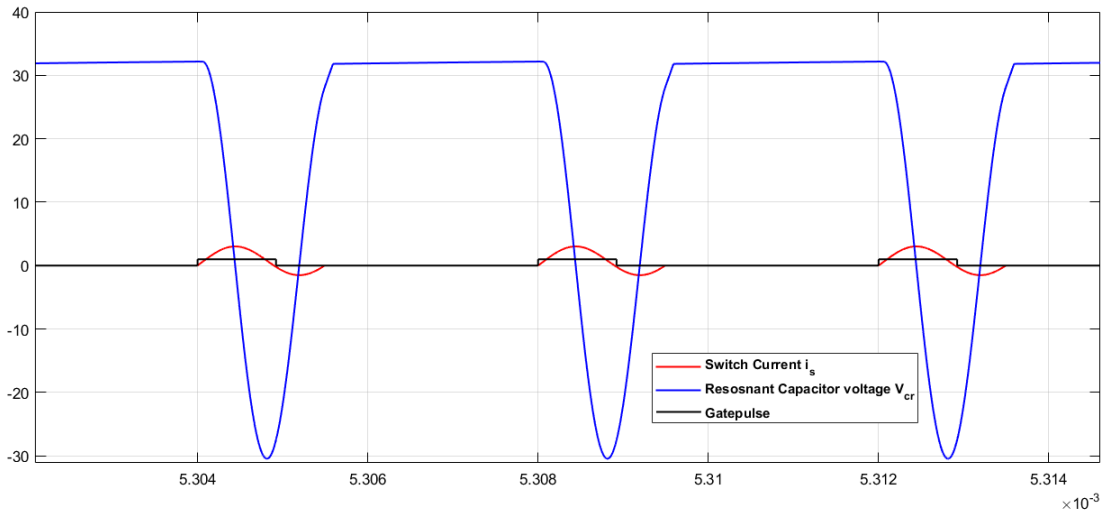


Fig. 3.16: Switch Current,Resonant Capacitor Voltage Waveform and Gate Pulse Signal

As explained before the switch current (red graph in fig 3.16) becomes zero due to

resonance and at that instant the switch is turned off by removing the gate pulse. Thus ZCS condition thus can be met.

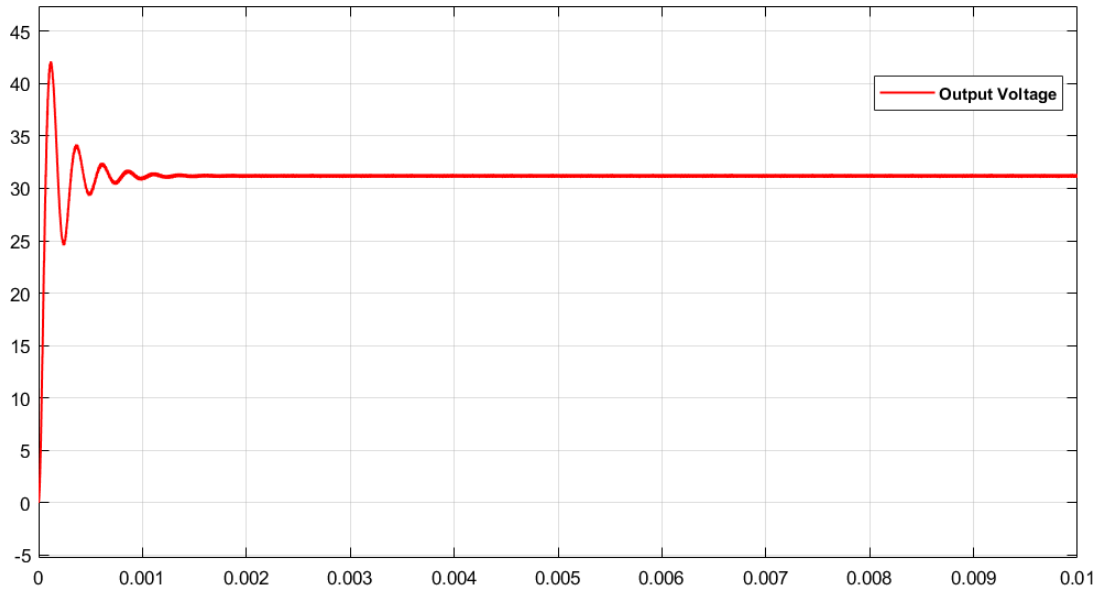


Fig. 3.17: Output Voltage waveform

# CHAPTER 4

# Soft-Switching Bidirectional DC/DC Converter with a LC Series Resonant Circuit

## 4.1 INTRODUCTION

The proposed converter topology [9] is given in fig 4.1. It is basically a bidirectional buck boost converter with additional soft switching cell for resonant operation.The soft switching of the proposed converter is achieved by LC resonance. The proposed converter is based on the conventional bidirectional buck–boost converter. The soft-switching cell that consists of a snubber capacitor $C_s$ , a resonant inductor $L_r$ , and a resonant capacitor $C_r$ is added. In the boost mode, the snubber capacitor $C_s$ induces the switch $S_{boost}$ to turn OFF under ZVS condition by changing the current path flowing to switch. The ZVS condition is achieved by series resonance between resonant inductor and resonant capacitor.

Actually, the ZVS condition can be achieved when the current of resonant inductor is larger than that of main inductor. The current of resonant inductor can be increased by series resonance between resonant inductor and capacitor during the switch-off time interval. The snubber capacitor can be fully discharged by the difference between currents of resonant inductor and of main inductor. After the discharge of snubber capacitor, the excessive current flow conducts the antiparallel diode of the main switch. Consequently, the ZVS condition of main switch can be satisfied due to the excessive current flow. The turn-off signal of main switch has to be supplied during this time interval for ZVS.

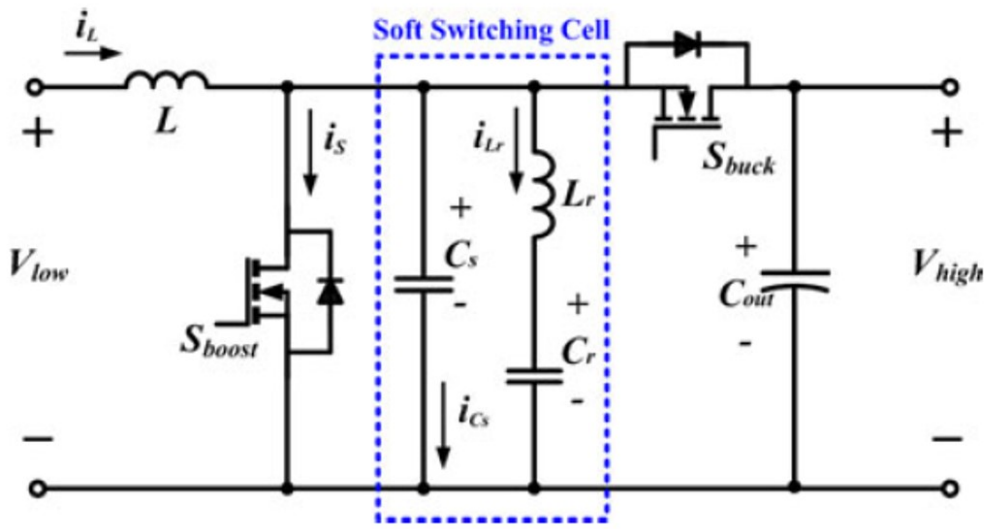


Fig. 4.1: Circuit diagram for the proposed topology[9]

## 4.2 BUCK MODE OF OPERATION

### 4.2.1 MODE 1 $t_0$<t<$t_1$

In this mode the $S_{buck}$ is in ON condition. The main inductor current $i_l$ increases and also the resonant inductor current $i_{lr}$ also increases linearly

$$\frac{Ldi_l}{dt} = V_{in} - V_o \tag{4.1}$$

$$i_l(t) = \frac{(V_{in} - V_o)t}{L} + i_l(t_0) \tag{4.2}$$

$$V_{in} = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.3}$$

By using laplace transform

$$i_{lr}(t) = \frac{V_{in} - V_{cr}(t_0)}{Z_r} \sin(\omega_r t) + i_{lr}(t_0) \cos(\omega_r t) \tag{4.4}$$

$$V_{cr}(t) = V_o - (V_o - V_{cr}(t_0) \cos(\omega_r t) + i_{lr}(t_0) Z_r \sin(\omega_r) \tag{4.5}$$

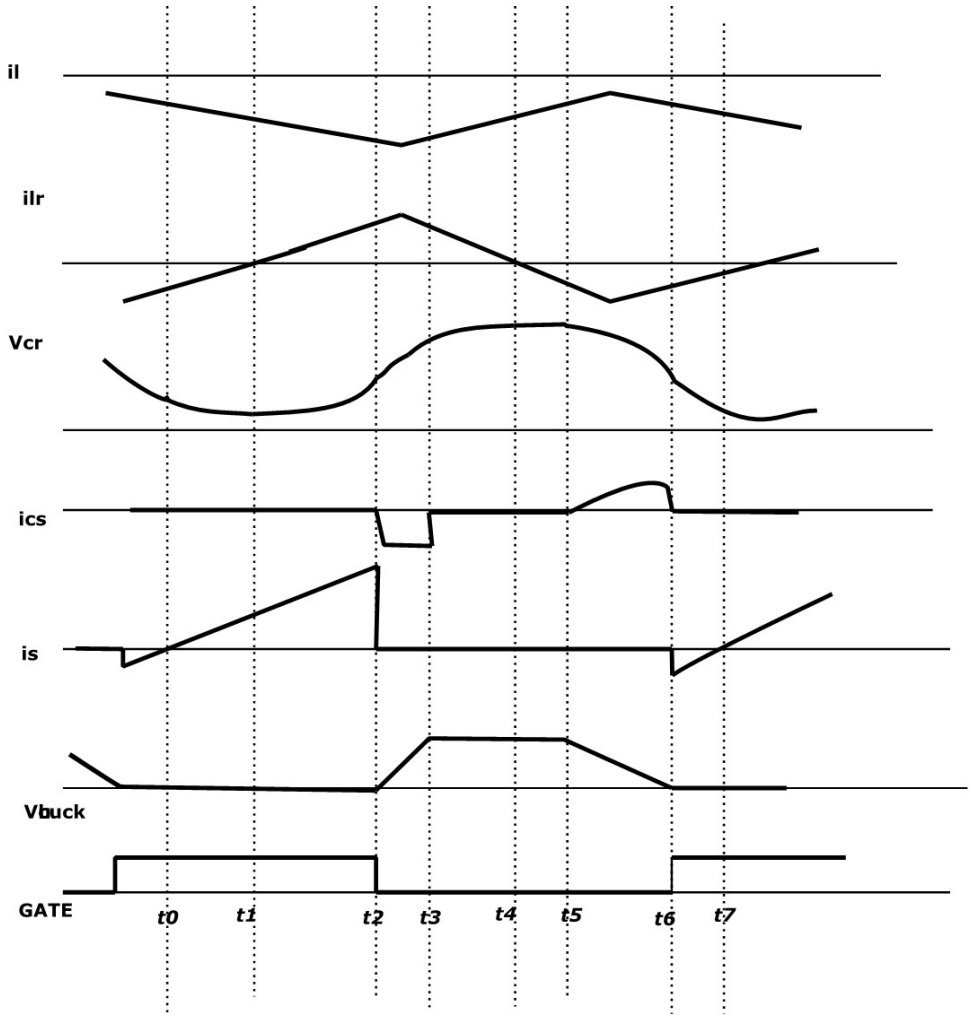


Fig. 4.2: Buck Mode Waveforms

### 4.2.2 MODE 2 $t_1$<t<$t_2$

This MODE starts at $t_1$ when the resonant inductor current increases linearly which started from the previous mode and it reaches zero at the beginning of this MODE and becomes positive and reverses its direction. The input current supplies both the resonant current and main inductor current.

$$\frac{Ldi_l}{dt} = V_{in} - V_o \tag{4.6}$$

$$i_l(t) = \frac{(V_{in} - V_o)t}{L} + i_l(t_1) \tag{4.7}$$

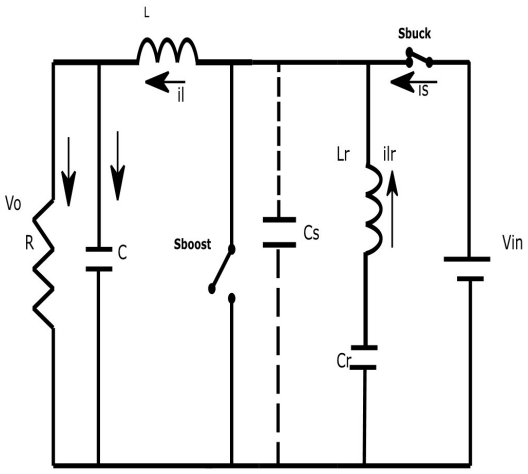


Fig. 4.3: Mode 1 equivalent circuit

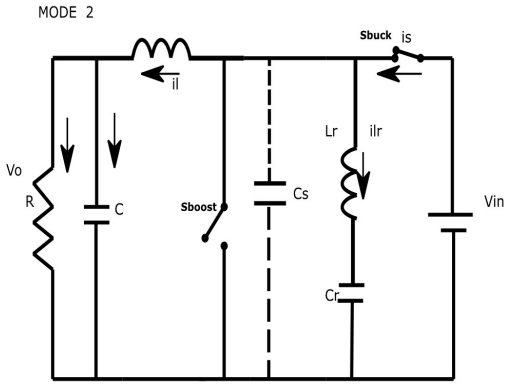


Fig. 4.4: Mode 2 equivalent circuit

$$V_{in} = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.8}$$

By using laplace transform

$$i_{lr}(t) = \frac{V_{in} - V_{cr}(t_1)}{Z_r} \sin(\omega_r t) \tag{4.9}$$

$$V_{cr}(t) = V_o - (V_o - V_{cr}(t_0) \cos(\omega_r t) + i_{lr}(t_1) \cos(\omega_r t) \tag{4.10}$$

### 4.2.3 MODE 3 $t_2$<t<$t_3$

At the start of this mode at $t_3$ the switch $S_{buck}$ is turned OFF. The snubber capacitor $C_s$ discharges and supplies the current to meet the KCL. The capacitor dicharges from input voltage to zero then its voltage becomes negative which results in MODE 4 operation of the circuit

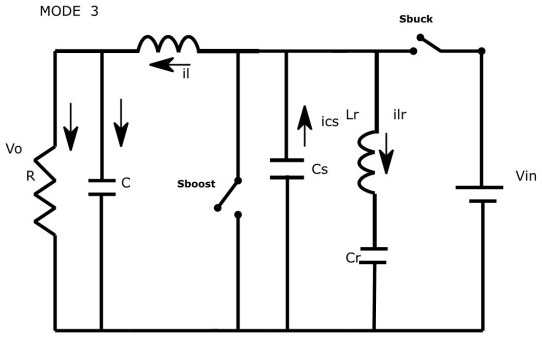


Fig. 4.5: Mode 3 equivalent circuit

### 4.2.4 MODE 4 $t_3$<t<$t_4$

At the end MODE3 the voltage across the snubber capacitor becomes negative the antiparallel diode of the switch $S_{boost}$ turned ON and the current path changes through this diode.This MODE continues until the resonant inductor current again becomes zero.

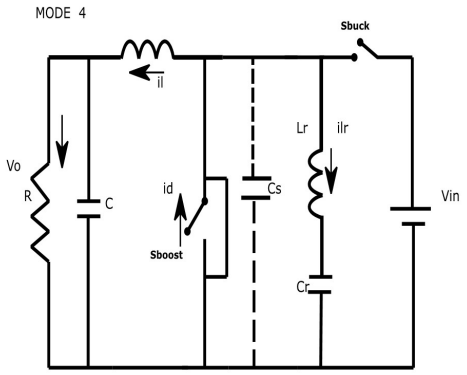


Fig. 4.6: Mode 4 equivalent circuit

$$\frac{Ldi_l}{dt} = -V_o \tag{4.11}$$

$$i_l(t) = \frac{-V_o t}{L} + i_l(t_3) \tag{4.12}$$

$$0 = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.13}$$

By using laplace transform

$$i_{lr}(t) = i_{lr}(t_3)\cos(\omega_r t) - \frac{V_{cr}(t_3)\sin(\omega_r t)}{Z_r} \tag{4.14}$$

$$V_{cr}(t) = Z_r i_{lr}(t_3)\sin(\omega_r t) + V_{cr}(t_3)\cos(\omega_r t) \tag{4.15}$$

### 4.2.5 MODE 5 $t_4 < t < t_5$

The previous MODE stops when the resonant inductor current becomes zero and this MODE begins in which the resonant inductor current goes to negative and reverses its direction, This mode continues until when both the resonant inductor current and the main inductor becomes equal.

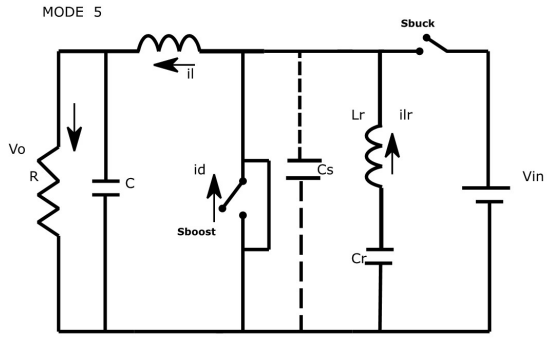


Fig. 4.7: Mode 5 equivalent circuit

$$\frac{Ldi_l}{dt} = -V_o \tag{4.16}$$

$$i_l(t) = \frac{-V_o t}{L} + i_l(t-4) \tag{4.17}$$

$$0 = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.18}$$

By using laplace transform

$$i_{lr}(t) = -\frac{V_{cr}(t_4)\sin(\omega_r t)}{Z_r} \tag{4.19}$$

$$V_{cr}(t) = +V_{cr}(t_4)\cos(\omega_r t) \tag{4.20}$$

### 4.2.6 MODE 6 $t_5$<t<$t_6$

At start of this MODE both the inductor current are equal.Further when the resonant inductor current becomes greater than the main inductor current the additional current flows through the snubber capacitor and charges.It charges until the voltage across it becomes the input voltage

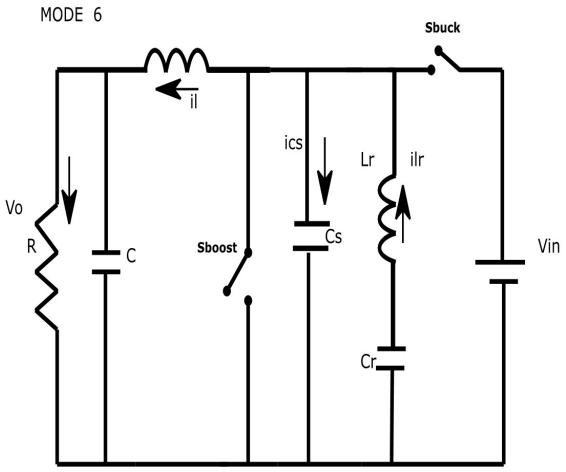


Fig. 4.8: Mode 6 equivalent circuit

### 4.2.7 MODE 7 $t_6$<t<$t_7$

At the beginning of this MODE the snubber capacitor charges to input voltage resulting the antiparallel diode of the switch $s_{bucK}$ starts conducting . Thus voltage acoss the switch becomes zero and can be turned ON under ZVS condition

$$\frac{Ldi_l}{dt} = V_{in} - V_o \tag{4.21}$$

$$i_l(t) = \frac{(V_{in} - V_o)t}{L} + i_l(t_6) \tag{4.22}$$

$$V_{in} = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.23}$$

By using laplace transform

$$i_{lr}(t) = \frac{V_{in} - V_{cr}(t_6)}{Z_r} \sin(\omega_r t) + i_{lr}(t_6) \cos(\omega_r t) \tag{4.24}$$

$$V_{cr}(t) = V_o - (V_o - V_{cr}(t_6) \cos(\omega_r t) + i_{lr}(t_6) Z_r \sin(\omega_r t) \tag{4.25}$$

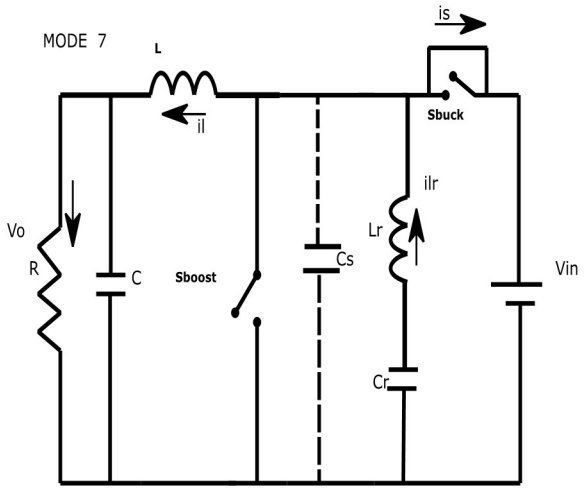


Fig. 4.9: Mode 7 equivalent circuit

## 4.3 BOOST MODE OF OPERATION

In this section the detailed analysis when the circuit operates in the boost mode is done. The analysis for one switching cycle can be divided into seven modes

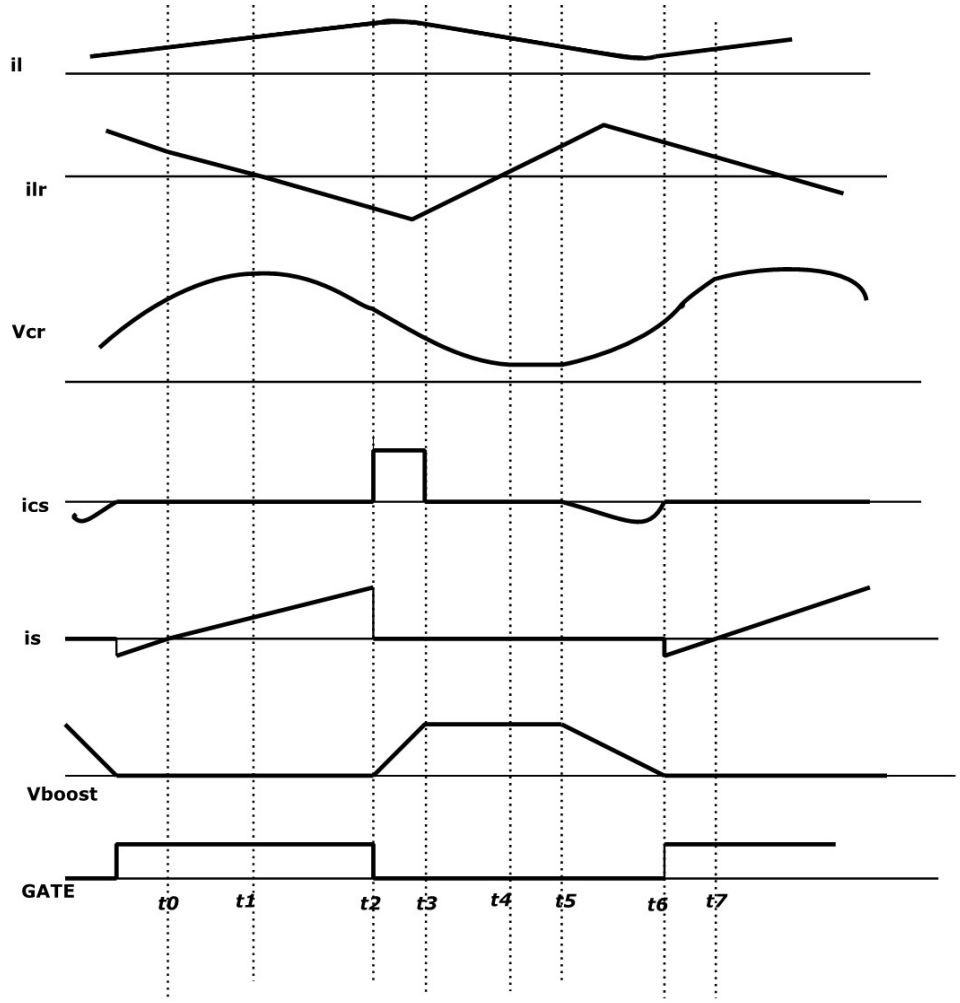


Fig. 4.10: Boost Mode Waveforms

### 4.3.1 MODE 1 $t_0$<t<$t_1$

The fig 4.11 shows the circuit in MODE1.Actually this mode is during the on time of switch. The voltage across the main inductor is $V_{in}$ so the inductor current increases. The initially inductor current is $i_l(t_o)$ the resonant initial current will be $i_{lr}(t_o)$

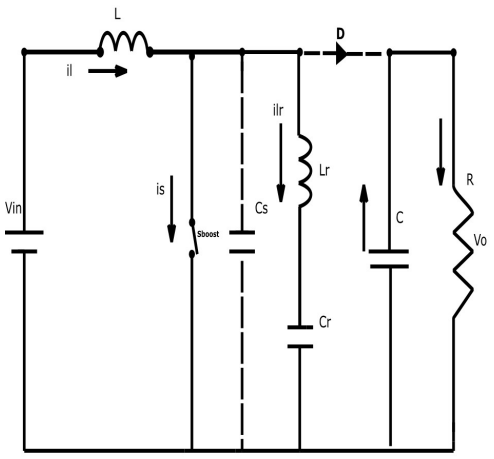


Fig. 4.11: Mode 1 equivalent circuit

$$\frac{Ldi_l}{dt} = V_{in} \tag{4.26}$$

$$i_l(t) = \frac{V_{in}t}{L} + i_l(t_0) \tag{4.27}$$

$$0 = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.28}$$

By using laplace transform

$$i_{lr}(t) = i_{lr}(t_0)\cos(\omega_r t) - \frac{V_{cr}(t_0)\sin(\omega_r t)}{Z_r} \tag{4.29}$$

$$V_{cr}(t) = Z_r i_{lr}(t_0)\sin(\omega_r t) + V_{cr}(t_0)\cos(\omega_r t) \tag{4.30}$$

### 4.3.2 MODE 2 $t_1$<t<$t_2$

The circuit for this MODE is given in fig4.12. In this MODE also the main inductor current increases while the resonant inductor current decreases and becomes zero and then conducts in the reverse direction. At time $t_1$, the direction of $i_{lr}$ is changed, $i_l$ and $i_{lr}$ are added and the resultant current flows through the switch

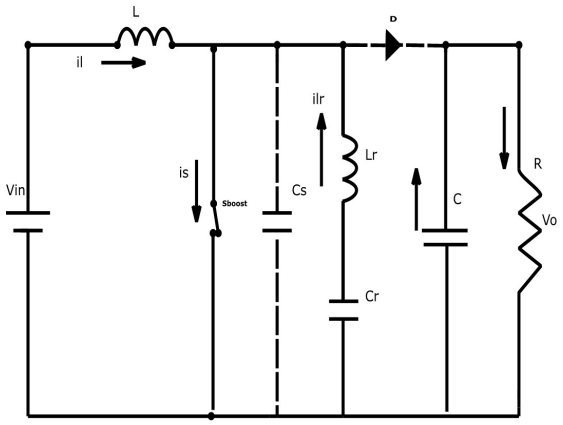


Fig. 4.12: Mode 2 equivalent circuit

$$\frac{Ldi_l}{dt} = V_{in} \tag{4.31}$$

$$i_l(t) = \frac{V_{in}t}{L} + i_l(t_1) \tag{4.32}$$

$$0 = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.33}$$

By using laplace transform

$$i_{lr}(t) = \frac{-V_{cr}(t_1)\sin(\omega_r t)}{Z_r} \tag{4.34}$$

$$V_{cr}(t) = V_{cr}(t_1)\cos(\omega_r t) \tag{4.35}$$

### 4.3.3 MODE 3 $t_2$<t<$t_3$

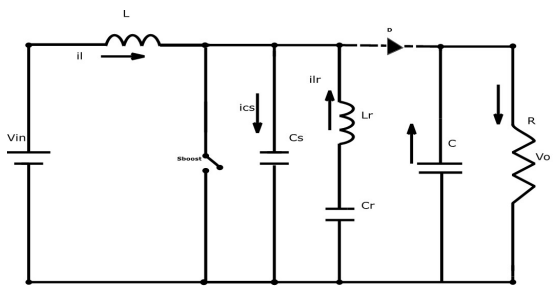


Fig. 4.13: Mode 3 equivalent circuit

This MODE is started when the switch $S_{boost}$ is turned OFF with ZVS condition and the current flows to snubber capacitor $C_s$. The voltage of the snubber capacitor increases to the output voltage $V_o$

### 4.3.4 MODE 4 $t_3$<t<$t_4$

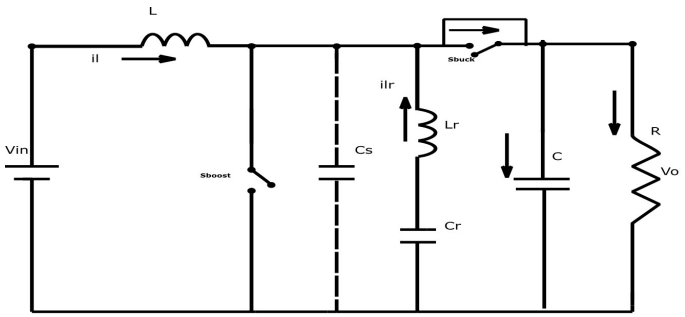


Fig. 4.14: Mode 4 equivalent circuit

At time $t_3$ the voltage across $C_s$ is equal to $V_o$ and the antiparallel diode of $S_{bucK}$ is turned ON. The charged energy of the main inductor L and resonant circuit is transmitted to the load through antiparallel diode of $S_{bucK}$. Mode 4 ends with $C_r$ is fully discharged and the direction of $i_l$ is changed

$$\frac{Ldi_l}{dt} = V_{in} - V_o \tag{4.36}$$

$$i_l(t) = \frac{(V_{in} - V_o)t}{L} + i_l(t-3) \tag{4.37}$$

$$Vo = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.38}$$

By using laplace transform

$$i_{lr}(t) = \frac{V_o - V_{cr}(t_3)}{Z_r} \sin(\omega_r t) + i_{lr}(t_3) \cos(\omega_r t) \tag{4.39}$$

$$V_{cr}(t) = V_o - (V_o - V_{cr}(t_3)) \cos(\omega_r t) + i_{lr}(t_r) Z_r \sin(\omega_r t) \tag{4.40}$$

### 4.3.5 MODE 5 $t_4$<t<$t_5$

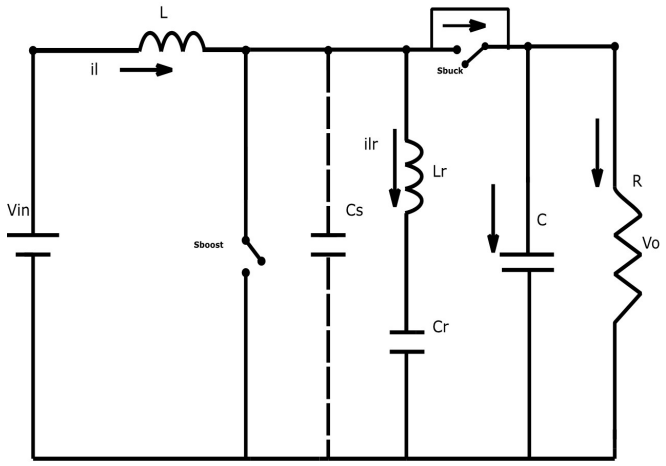


Fig. 4.15: Mode 5 equivalent circuit

The main inductor current $i_l$ flows to the resonant circuit and the load. The main inductor current is decreased and resonant inductor current $i_{lr}$ is increased. The direction of $i_{lr}$, is changed. When $i_l$ becomes large to $i_{lr}$ , this mode is finished

$$\frac{Ldi_l}{dt} = V_{in} - V_o \tag{4.41}$$

$$i_l(t) = \frac{V_{in} - V_o t}{L} + i_l(t-4) \tag{4.42}$$

$$V_o = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.43}$$

By using laplace transform

$$i_{lr}(t) = \frac{V_o - V_{cr}(t_4)\sin(\omega_r t)}{Z_r} \tag{4.44}$$

$$V_{cr}(t) = V_o - (V_o - V_{cr}(t_4))\cos(\omega_r t) \tag{4.45}$$

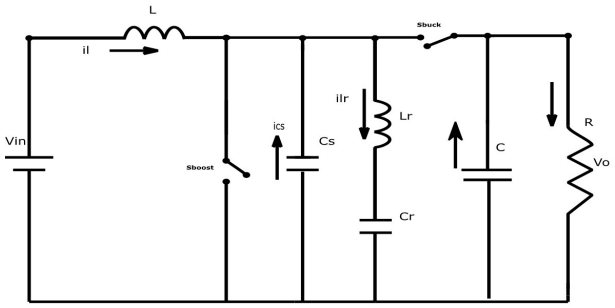


Fig. 4.16: Mode 6 equivalent circuit

### 4.3.6 MODE 6 $t_5$<t<$t_6$

Mode 6 starts with discharge of $C_s$. When the voltage across $C_s$ becomes lower than $V_o$ the antiparallel diode of $S_{buck}$ turns OFF And MODE 6 ends.

### 4.3.7 MODE 7 $t_6$<t<$t_7$

When $i_{lr}$ flows to antiparallel diode of switch $S_{boost}$ and voltage of $C_s$ is fully discharged this mode starts. When antiparallel diode of $S_{boost}$ turns off mode 7 ends

$$\frac{Ldi_l}{dt} = V_{in} \tag{4.46}$$

$$i_l(t) = \frac{V_{in}t}{L} + i_l(t_6) \tag{4.47}$$

$$0 = \frac{L_r di_{lr}}{dt} + \frac{1}{Cr} * \int i_{lr} dt \tag{4.48}$$

By using laplace transform

$$i_{lr}(t) = i_{lr}(t_6)\cos(\omega_r t) - \frac{V_{cr}(t_6)\sin(\omega_r t)}{Z_r} \tag{4.49}$$

$$V_{cr}(t) = i_{lr}(t_6)Z_r \sin(\omega_r t) + V_{cr}(t_6)\cos(\omega_r t) \tag{4.50}$$

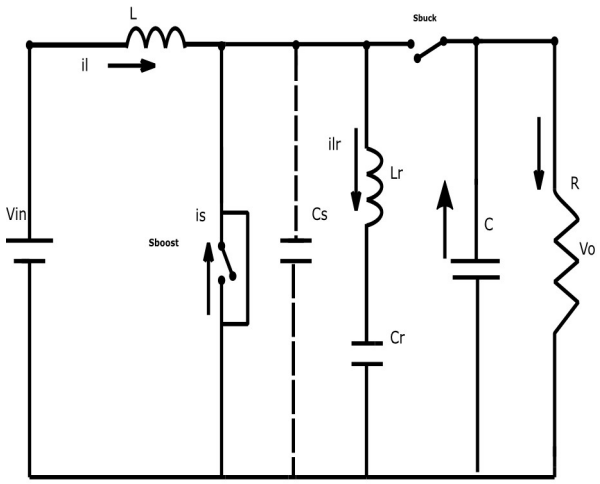


Fig. 4.17: Mode 7 equivalent circuit

## 4.4 CONTROL OF PROPOSED TOPOLOGY

For ZVS operation of the proposed converter, the switch-off time has to be determined according to the LC series resonant period. Thus, the output voltage is controlled by the switch on time modulation. This method is pulse frequency modulation (PFM) control,which changes the switching frequency. When the voltage of switch is zero, the switch is turned ON and maintains on state during set time.he topology satisfies ZVS condition because the voltage of snubber capacitor $C_s$ is increased to the output voltage during off time and decreased to zero voltage by resonance.

The output voltage and switch voltage are sensed to modulate the on time of main switch. For the on-time modulation, detected output voltage determines the amplitude of a carrier wave, and the voltage of switch determines the amplitude of reference wave.

## 4.5 DESIGN OF RESONANT ELEMENTS

Since the proposed converter turned ON and OFF under ZVS condition by using resonance without an auxiliary switch, the design of resonant components is important to ensure the ZVS condition.When the switch is ON, the current toward the switch flows into the snubber capacitor, so the process of the switch ON is made in the state that

the switch is zero voltage. When the resonant inductor current is greater than the main inductor current during the switch-off time, the current difference comes to form the current path through the snubber capacitor. During this time interval, the snubber capacitor is fully discharged to zero voltage.

### 4.5.1 Design of Resonant Inductor

The current variation of resonant inductor current to satisfy the resonant condition has to be greater than main inductor current ripple as represented in (4.51). The minimum value of main inductor current can be represented as (4.52), and the maximum value of resonant inductor current can be represented as (4.53). By substituting the (19) and (20) into the (18), the maximum value of resonant inductance can be derived as (4.54)

$$I_{lmin} \leq I_{lrpeak} \tag{4.51}$$

$$I_{lmin} = \frac{V_o}{V_{in}} I_o - \frac{T_{on}}{2L} V - i_n \tag{4.52}$$

$$I_{lrpeak} = \frac{1}{2} \frac{V_{in}}{L_r} T_{on} \tag{4.53}$$

$$L_r \leq \frac{V_{in}.L.T_{on}}{2.G_v.L - V_{in}.T_{on}} \tag{4.54}$$

### 4.5.2 Design of Resonant Capacitor

To achieve the ZVS operation, the resonant frequency should be lower than a half of switching frequency. In this paper, the resonant frequency is selected as 40% of the switching frequency. It can be represented as (4.55). After the design of resonant inductance, the resonant capacitance can be determined according to the selected resonant frequency as shown in (4.56)

$$\frac{2.5}{2.\pi.\sqrt{L_r.C_r}} \leq f_{sw} \tag{4.55}$$

$$C_r \leq \frac{6.25}{4.\pi^2.L_r.f_{sw}^2} \tag{4.56}$$

### 4.5.3 Simulation Result Of Boost Mode Operation

A simulation study was done with the design method mentioned in section 4.5. As mentioned in the design procedure the main aim in-order to attain the ZVS condition is the peak of the resonant inductor current should be greater than the main inductor current. In the fig 4.18 it is shown that during each cycle the resonant inductor current (blue graph) becomes greater than the main inductor current(red graph). During this the period the snubber capacitor discharges. The fig 4.19 shows the plot of snubber

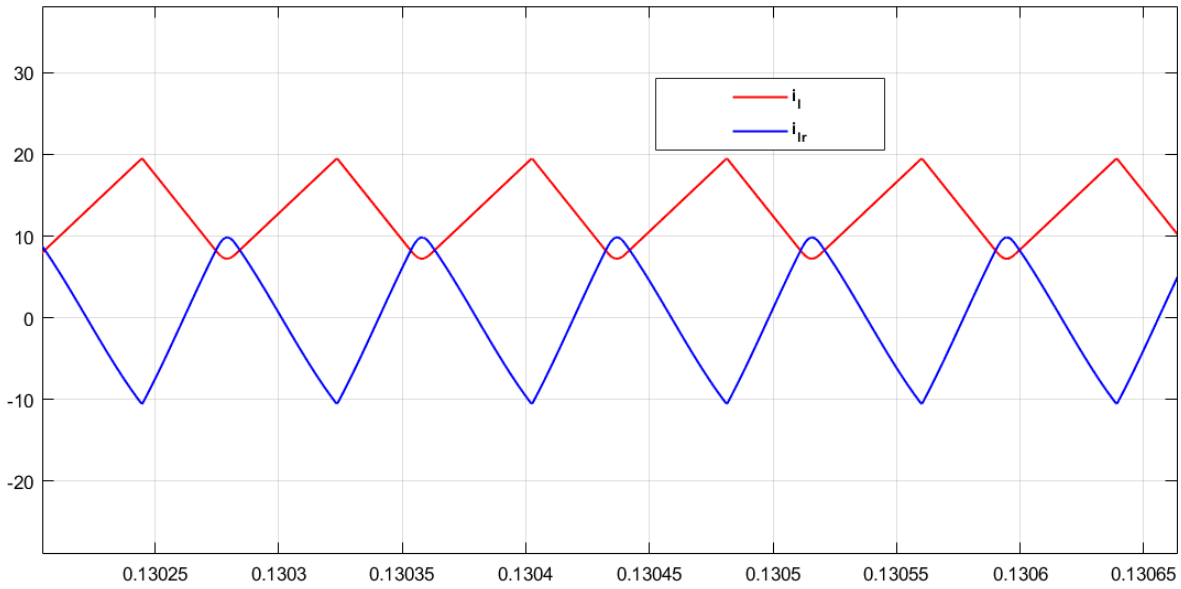


Fig. 4.18: Main Inductor Current $i_l$ and the resonant inductor current $i_{lr}$

capacitor current with repect to the gate pulse of the main boost switch. It can be seen that when switch goes ON to OFF condition the snubber capacitor gets charged and it deviates the current path.And also before the turn ON period the snubber capacitor discharge, when the resonant branch current gets more than the main inductor current. The fig 4.20 shows the snubber capacitor or the boost switch voltage with respect to the gate pulse. It can be seen that when the switch is turned OFF the voltage is slowly increasing because of the deviation of main switch current path through the snubber capacitor. Similarly it can be seen the switch comes down to zero before turn ON due to the discharge of snubber capacitor.

The fig 4.21 shows the enlarged figure of fig 4.20. It clearly shows the voltage profile

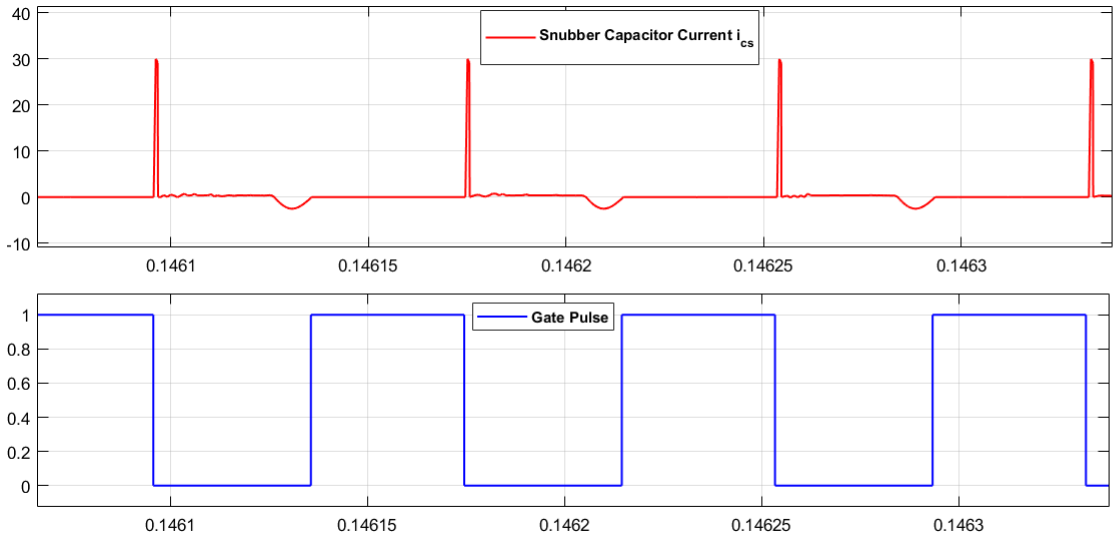


Fig. 4.19: Snubber Capacitor Current($i_{cs}$)Waveform

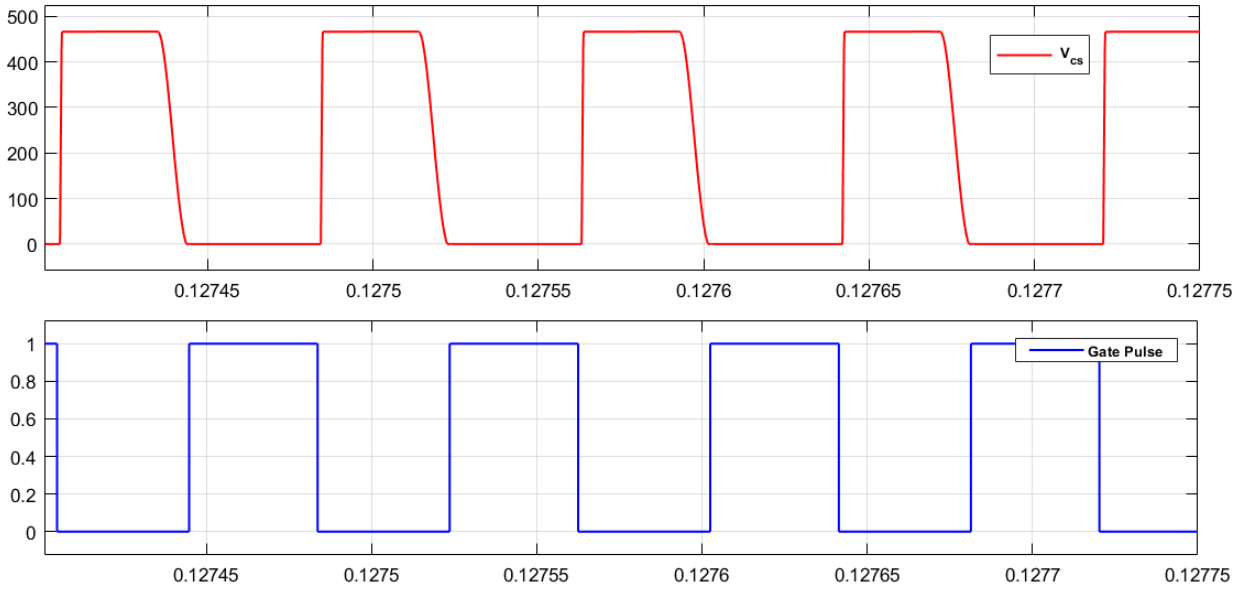


Fig. 4.20: The Switch(Snubber Capacitor) Voltage($V_{cs}$)Waveform With Respect to Gate Pulse

during turn ON and turn OFF. Finally the fig 4.22 shows the resonant operation of of resonant branch $L_r$ and $C_r$. It follows the basic principle of resonance that resonant capacitor is charged to positive and negative peak when the inductor current is zero.

The major limitation of the this circuit after analysing the simulation result is that the main switch current, during a part of switching cycle will be the sum of main inductor current and the resonant inductor current. So the circuit should be chosen such that

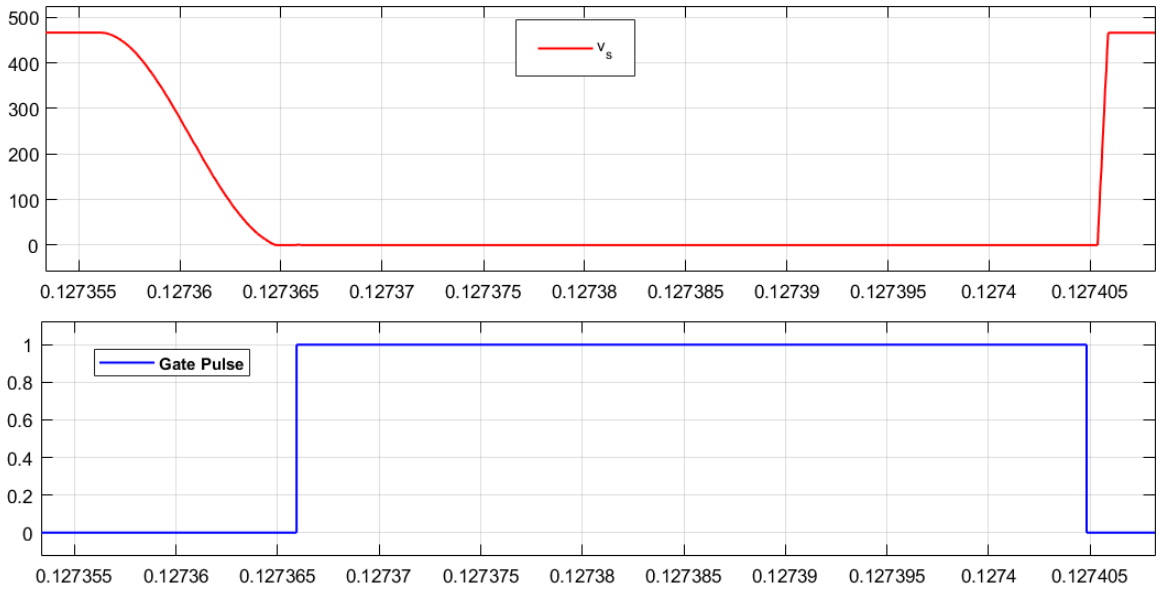


Fig. 4.21: Enlarged Switch Voltage Waveform

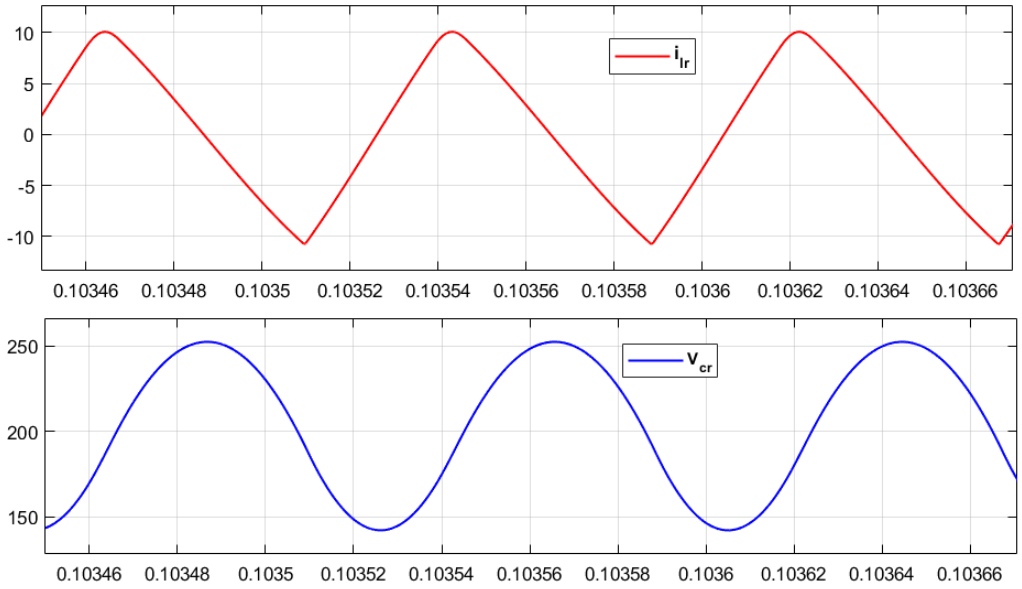


Fig. 4.22: Resonant Inductor Current And Capacitor Voltage Waveform

the input- output voltage relation should be such way that the current in the circuit will not causes a greater conduction losses which will cancels the advantages of reduced switching losses.

# CHAPTER 5

# AVERAGE CURRENT MODE CONTROL OF DC BUCK CONVERTER

## 5.1 Introduction to AC Modelling

The main objective of the control is to maintain the output voltage v(t) equal to accurate constant value V [10]. The factors which affects the output voltage are due to the disturbances in the input voltage v$g$(t) and in the load R. It may also due to uncertainties in the element values, in input voltage Vg and the load R. The main objective is to

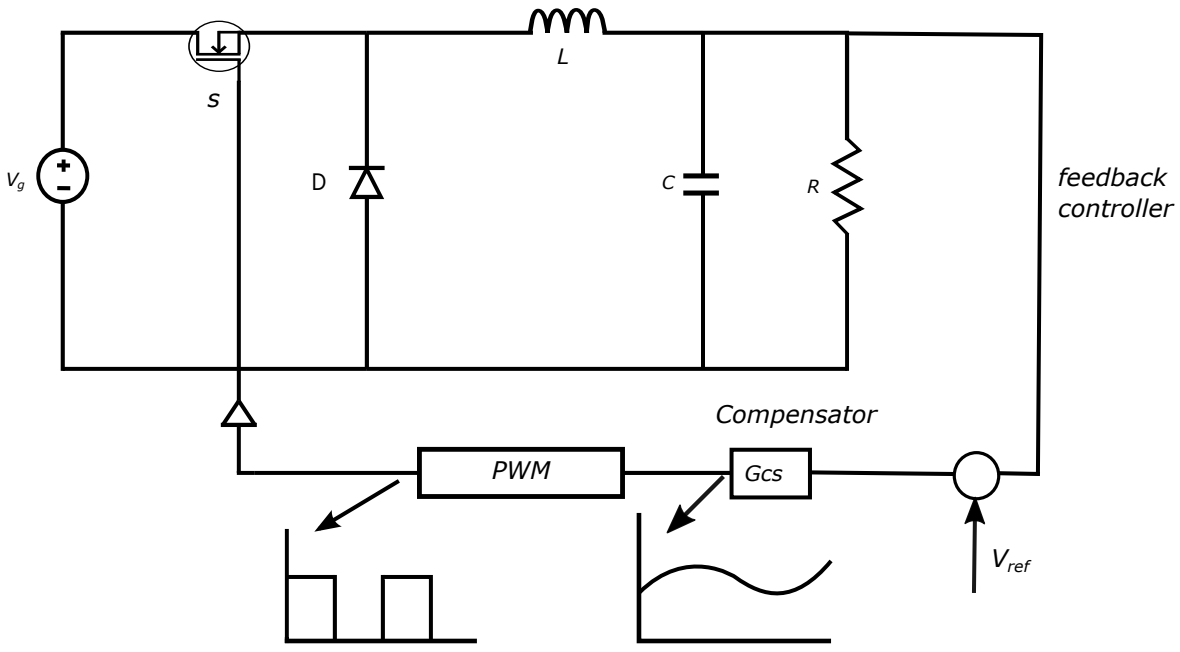


Fig. 5.1: A Simple DC-DC Regulator System Employing a Buck Converter

develop the dynamic models of the converters in-order to understand the ac variations in Vg(t),R or,d(t) and how it affects the output voltage v(t). Also to develop the small signal transfer functions of the converter to design the controller.

### 5.1.1 Averaging to remove switching ripple(moving average)

In-order to remove the switching ripple, the average of the waveform is done over one switching period as given in the

$$L\frac{d < i_l(t) >_{Ts}}{dt} =< v_l(t) >_{Ts} \tag{5.1}$$

$$C\frac{d < v_c(t) >_{Ts}}{dt} =< i_c(t) >_{Ts} \tag{5.2}$$

where $< x(t) >$ is given as

$$< x(t >_{Ts} = \frac{\int x(\tau)d\tau}{Ts} \tag{5.3}$$

It is to be noted that in steady state $< v_l(t) >_{Ts}$=0 and $< i_c(t) >_{Ts}$=0 by inductor volt-second balance and capacitor charge balance

### 5.1.2 Discussion of Averaging

#### Averaging the inductor waveform

For instantaneous inductor waveform, we have

$$L\frac{di(t)}{dt} = v_l(t) \tag{5.4}$$

We can write similar equation for the averaged waveform

$$d\frac{i(t)_{Ts}}{dt} = \frac{d}{dt}(\frac{1}{T_s}\int(i(\tau)d\tau)) \tag{5.5}$$

The condition to interchange integration and differentiation i.e the inductor current is continuous and its derivative has finite number of discontinuities has met so we can interchange and rewrite the equation as

$$\frac{d < i(t) >_{Ts}}{dt} = \frac{1}{T_s}\int\frac{di(\tau)d\tau}{dt} \tag{5.6}$$

$$\frac{d < i(t)_{T_s}}{dt} = \frac{1}{T_s}\int \frac{v_l(\tau)d\tau}{L} \tag{5.7}$$

$$L\frac{d < i(t) >}{dt} =< v_l(t) >_{T\ s} \tag{5.8}$$

So the average inductor current and voltage follow the same defining equations with no additional terms and with the same value of L Similarly we can write

$$C\frac{d < v(t)_{Ts}}{dt} =< i_c(t) >_{Ts} \tag{5.9}$$

### 5.1.3 Non-linear averaged equation

The averaged voltages and currents are, in general non-linear functions of the converter, duty cycle, voltages and currents.Hence the averaged equations given below constitute a system of non-linear differential equations.Hence must linearize a small signal converter model

$$L\frac{d < i_l(t) >_{Ts}}{dt} =< v_l(t) >_{Ts} \tag{5.10}$$

$$C\frac{d < v_c(t) >_{Ts}}{dt} =< i_c(t) >_{Ts} \tag{5.11}$$

### 5.1.4 Averaged AC Modelling of Buck Converter

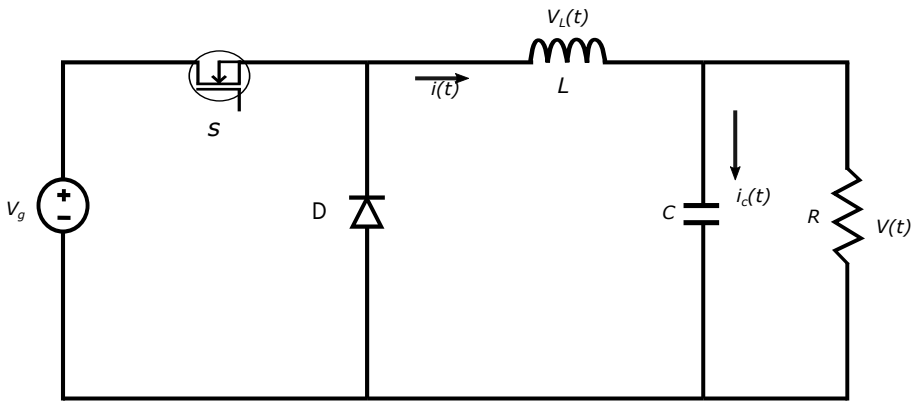


Fig. 5.2: Buck Circuit

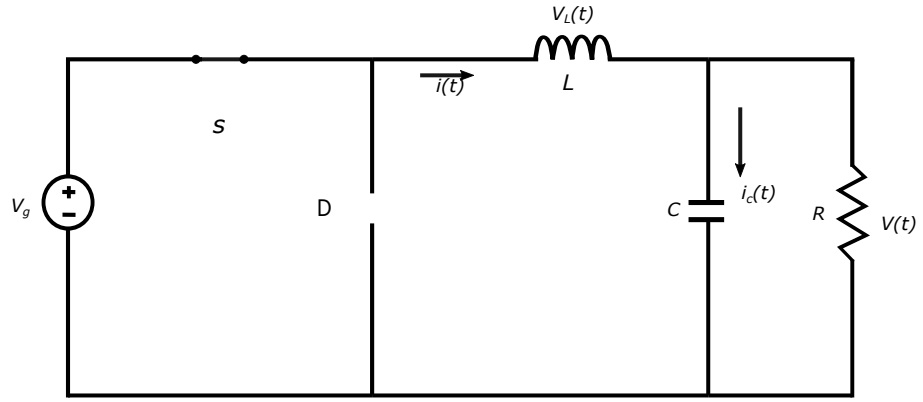


Fig. 5.3: Switch ON Equivalent Circuit

**When the Switch is ON**

Inductor voltage and capacitor current are

$$L\frac{di(t)}{dt} = v_l(t) = v_g(t) - v(t) \tag{5.12}$$

$$i_c(t) = i(t) = \frac{v(t)}{R} \tag{5.13}$$

Small ripple approximation : replace the waveforms with their low-frequency averaged values:

$$L\frac{di(t)}{dt} = v_l(t) = < v_g(t) >_{Ts} - < v(t) >_{Ts} \tag{5.14}$$

$$C\frac{dv(t)}{dt} = i_c(t) = < i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R} \tag{5.15}$$

**When the Diode is ON**

Inductor voltages and capacitor current are

$$L\frac{di(t)}{dt} = v_l(t) = -v(t) \tag{5.16}$$

$$C\frac{dv(t)}{dt} = i_c(t) = i(t) - \frac{v(t)}{R} \tag{5.17}$$

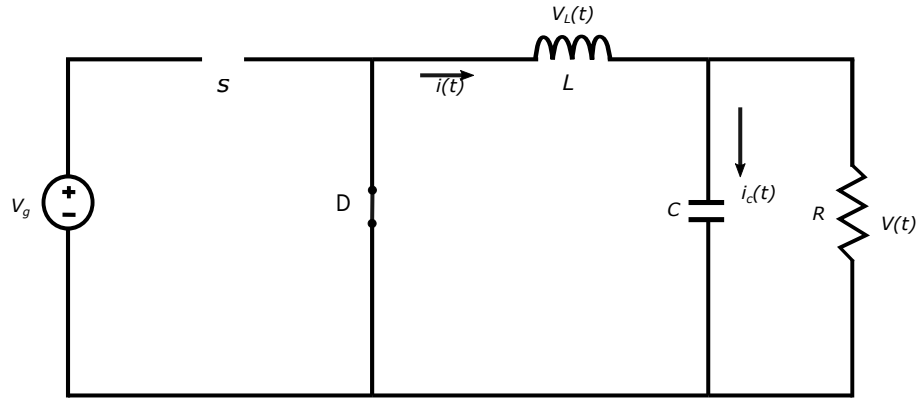


Fig. 5.4: Diode ON Equivalent Circuit

Small ripple approximation : replace waveform with their low frequency averaged values;

$$L\frac{di(t}{dt} = v_l(t) = - < v(t) >_{Ts} \tag{5.18}$$

$$C\frac{dv(t)}{dt} = i_c(t) =< i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R} \tag{5.19}$$

**Averaging the inductor waveform**

The average inductor voltage over one switching period is given as

$$L\frac{d < i(t) >_{Ts}}{dt} =< v_l(t) >_{Ts} = \frac{\int v(\tau)d\tau}{Ts} \approx d(t)(< v_g(t) >_{Ts} - < v(t) >_{Ts}) + d'(t)(- < v(t) >_{Ts} \tag{5.20}$$

On simplifying

$$< v_l(t) >_{Ts} \approx d(t) < v_g(t) >_{Ts} - < v(t) >_{Ts} \tag{5.21}$$

$$L\frac{< i_l(t) >}{dt} = d(t) < v_g(t) >_{Ts} - < v(t) >_{Ts} \tag{5.22}$$

**Averaging the capacitor waveform**

$$C\frac{d < v(t) >_{Ts}}{dt} =< i_c(t) >_{Ts} \approx d(t)(< i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R}) + d'(t)(< i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R}) \tag{5.23}$$

$$C\frac{d < v(t) >_{Ts}}{dt} \approx < i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R} \tag{5.24}$$

**The average input current**

Sometimes it is necessary to write an equation for the average converter input current,to derive a complete dc equivalent circuit model. It is likewise necessary to do this for ac model

$$< i_g(t) >_{Ts} = d(t) < i(t) >_{Ts} \tag{5.25}$$

**Discussion of the Average Approximation**

. Averaging facilitates derivation of tractable equations describing the dynamics of the converter

. Averaging removes the waveform component at the switching frequency and its harmonics, while preserving the magnitude and phase of the waveform at low frequency components.

.Averaging can be viewed as a form of low pass filtering that removes the ripple and contains only low frequency components.

### 5.1.5 Perturbation and Linearization

The converter averaged equations are given as

$$L\frac{< i_l(t) >}{dt} = d(t) < v_g(t) >_{Ts} - < v(t) >_{Ts} \tag{5.26}$$

$$C\frac{d < v(t) >_{Ts}}{dt} \approx < i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R} \tag{5.27}$$

$$< i_g(t) >_{Ts} = d(t) < i(t) >_{Ts} \tag{5.28}$$

These equations are non-linear because of multiplication of time varying quantity d(t) with other time varying quantity such as i(t) and v(t).

First linearize about quiescent-operating point. If the converter is driven with some steady- state or quiescent inputs as $d(t) = D$ and $< v(g) >_{Ts} = V_g$

Then,from the DC steady state analysis, after transients have subsided the inductor current, capacitor voltage and input current $< i(t)_{Ts}$,$< ig(t) >_{Ts}$,$< v(t) >_{Ts}$ reach the

quiescent values I ,V ,$I_g$ given by the steady state analysis as

$$V = DV_g \tag{5.29}$$

$$I_g = DI \tag{5.30}$$

$$I_g = D\frac{V}{R} \tag{5.31}$$

**Perturbation**

So let us assume that the input voltage and duty cycle are equal to some (DC) quiescent values, plus superimposed small ac variations

$$< v_g(t) >_{Ts} = V_g + \widehat{v_g}(t) \tag{5.32}$$

$$d(t) = D + \widehat{d}(t) \tag{5.33}$$

In response, and after any transients have subsided, the converter dependent voltages and currents will be equal to the corresponding quiescent values, plus small ac variations.

$$< i(t) >_{Ts} = I + \widehat{t}(t) \tag{5.34}$$

$$< v(t) >_{Ts} = V + \widehat{v}(t) \tag{5.35}$$

$$< i_g(t) >_{Ts} = I_g + \widehat{i}(t) \tag{5.36}$$

$$d(t) = D + \widehat{d}(t) \tag{5.37}$$

$$d\,'(t) = D\,' - \widehat{d}(t) \tag{5.38}$$

**Lineraization**

$$L\frac{< i_l(t) >}{dt} = d(t) < v_g(t) >_{Ts} - < v(t) >_{Ts} \tag{5.39}$$

$$L\frac{d(I + \widehat{t}(t))}{dt} = (D + \widehat{d}(t))(V_g + \widehat{v_g}(t)) - (V + \widehat{v}(t)) \tag{5.40}$$

simplifying and cancellation we get

$$L\frac{d\widehat{i}(t)}{dt} = \widehat{d}(t) * V_g - \widehat{v}(t) + D * \widehat{v_g}(t) \tag{5.41}$$

Siimilarly for capacitor waveform

$$C\frac{d < v(t) >_{Ts}}{dt} =< i(t) >_{Ts} - \frac{< v(t) >_{Ts}}{R} \tag{5.42}$$

$$C\frac{d(V + \widehat{v}(t)}{dt} = I + \widehat{i}(t) - \frac{V}{R} - \frac{\widehat{v}(t)}{R} \tag{5.43}$$

$$C\frac{d\widehat{v}(t)}{dt} = \widehat{i}(t) - \frac{\widehat{v}(t)}{R} \tag{5.44}$$

For the input current small signal model

$$< i_g(t) >_{Ts} = d(t) < i(t) >_{Ts} \tag{5.45}$$

$$I_g + \widehat{i_g}(t) = (D + \widehat{d}(t))(I + \widehat{i}(t)) \tag{5.46}$$

Thus after simplification

$$\widehat{i}(t) = D\widehat{i}(t) + \widehat{d}(t)I \tag{5.47}$$

From three equations eq 5.41, 5.44,5.47 we can develop the respective ciecuit model. These model are given in fig 5.5,5.6,5.7 respectively.

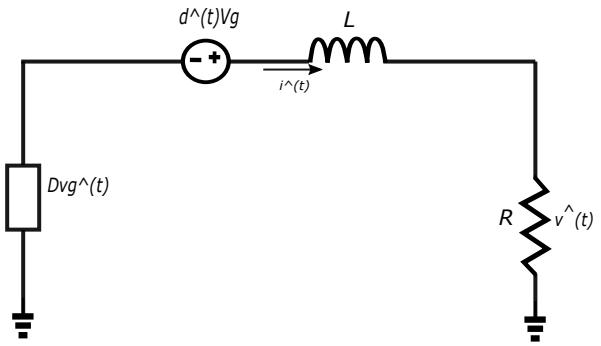


Fig. 5.5: Inductor Current Small Signal Model

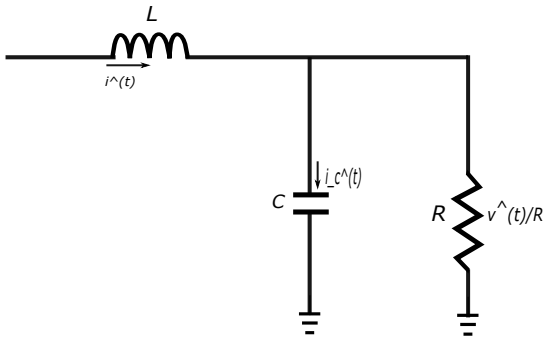


Fig. 5.6: Capacitor Voltage Small Signal Model

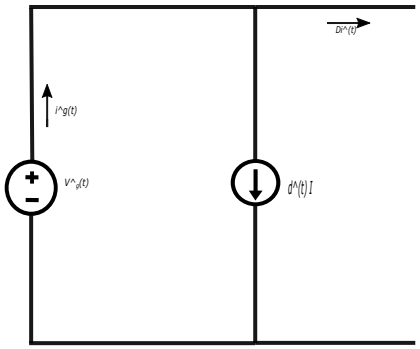


Fig. 5.7: Input Current Small Signal Model

Based on the above three figures we can develop the required small signal model and is given in fig 5.8 and the transformer model is given in fig 5.9

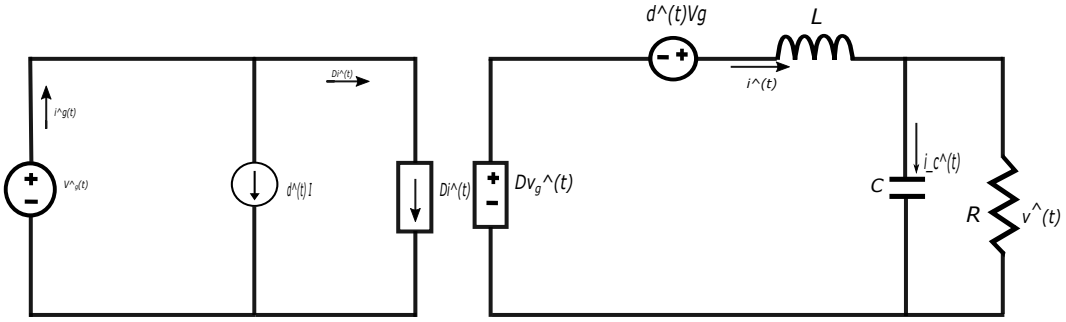


Fig. 5.8: Small Signal Model Of Buck Converter

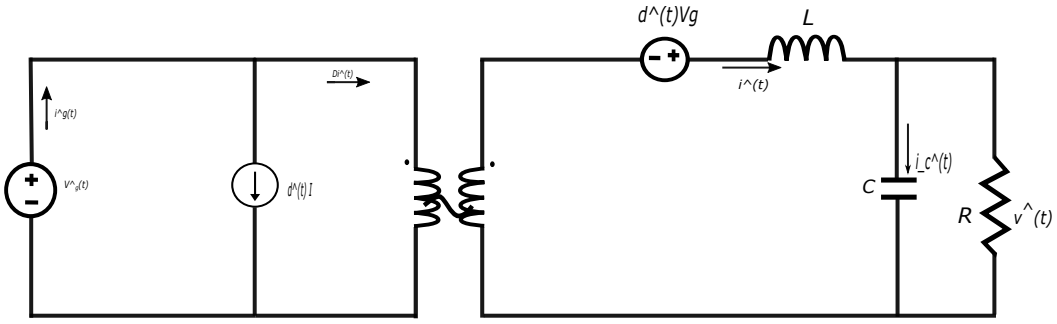


Fig. 5.9: Transformer Small Signal Model Of Buck Converter

## 5.2 BUCK CONVERTER TRANSFER FUNCTION

From the equivalent transformer model of fig 5.9 we can develop the transfer function for the buck converter

$$\widehat{v}(s) = G_{vd} * \widehat{d}(s) + G_{vg} * \widehat{v_g}(s) \tag{5.48}$$

$$G_{vd} = \frac{\widehat{v}}{\widehat{d}_{\widehat{v_g}(s)=0}} \tag{5.49}$$

$$G_{vg} = \frac{\widehat{v}}{\widehat{v_g}_{\,\widehat{d}(s)=0}} \tag{5.50}$$

When $v_g(s)$ = 0 the equivalent circuit is given by fig 5.9

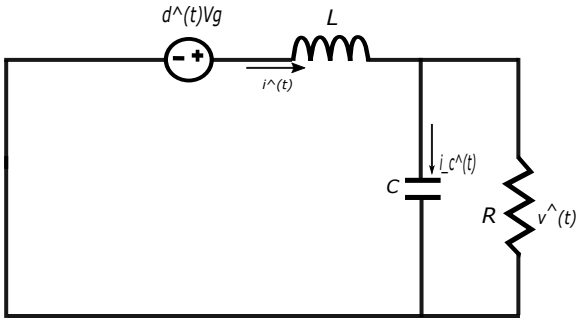


Fig. 5.10: Switch ON State Equivalent Circuit

$$\widehat{v}(t) = \widehat{d}(t)V_g * \frac{\frac{1}{sC}//R}{sL + \frac{1}{sC}//R} \tag{5.51}$$

$$= \frac{\widehat{d}(t)V_g * \frac{R}{(1+RCs)}}{sL + \frac{R}{1+sRC}} \tag{5.52}$$

$$= \frac{\widehat{d}(t)V_g * R}{R + sL(1 + sRC)} \tag{5.53}$$

$$G_{vd} = \frac{\widehat{v}(s)}{\widehat{d}(s)} = \frac{V_g}{1 + s\frac{L}{R} + s^2LC} \tag{5.54}$$

The standard form of various converter transfer function is given as equation (5.55)

$$G_{vd}(s) = \frac{G_{do} * (1 - \frac{s}{w_z})}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \tag{5.55}$$

In the case of buck converter the various terms of the standard form is given as

$$G_{do} = \frac{V}{D} \tag{5.56}$$

$$w_o = \frac{1}{\sqrt{LC}} \tag{5.57}$$

$$Q = R * \sqrt{\frac{C}{L}} \tag{5.58}$$

When d(s)=0 the equivalent circuit is given in fig 5.11

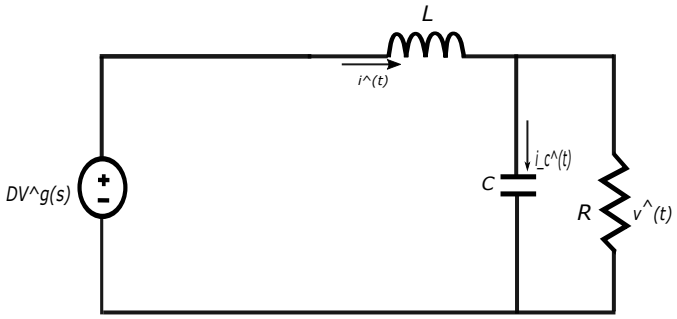


Fig. 5.11: Diode ON State Equivalent Circuit

$$G_{vg} = \frac{\widehat{v}(s)}{\widehat{v_g}(s)} \tag{5.59}$$

$$\widehat{v}(s) = D\widehat{v_g}(s) * \frac{1}{1 + \frac{sL}{R} + s^2LC} \tag{5.60}$$

$$G_{vg} = \frac{D}{1 + \frac{sL}{R} + s^2LC} \tag{5.61}$$

The standard form of converter transfer function is given by equation (5.62)

$$\frac{G_{go}}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \tag{5.62}$$

Where $G_{go}$ = D in the case of buck converter

### 5.2.1 Modelling the pulse-width modulator

Pulse width modulator converters the voltage signal $v_c(t)$ into duty cycle signal d(t):

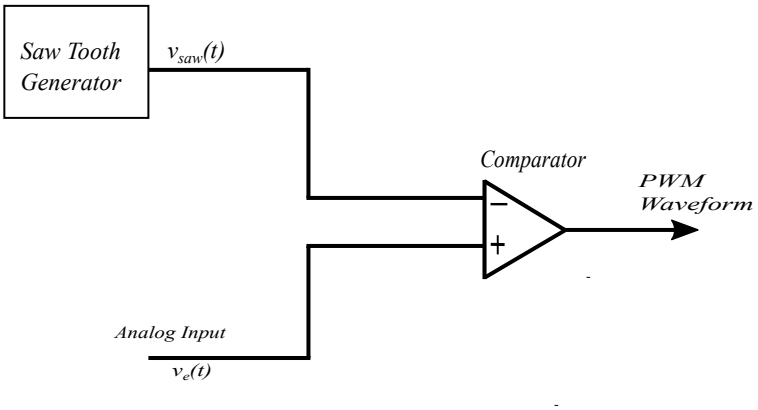


Fig. 5.12: PWM Generator Block Diagram

**Equation of pulse -width modulator**

For a linear saw-tooth waveform

$$d(t) = \frac{V_c(t)}{V_m} for 0 \leq V_c(t) \leq V_m \tag{5.63}$$

So d(t) is a linear function $v_c(t)$s The PWM equation can be in the form given as

$$d(t) = \frac{v_c(t)}{V_m} \tag{5.64}$$

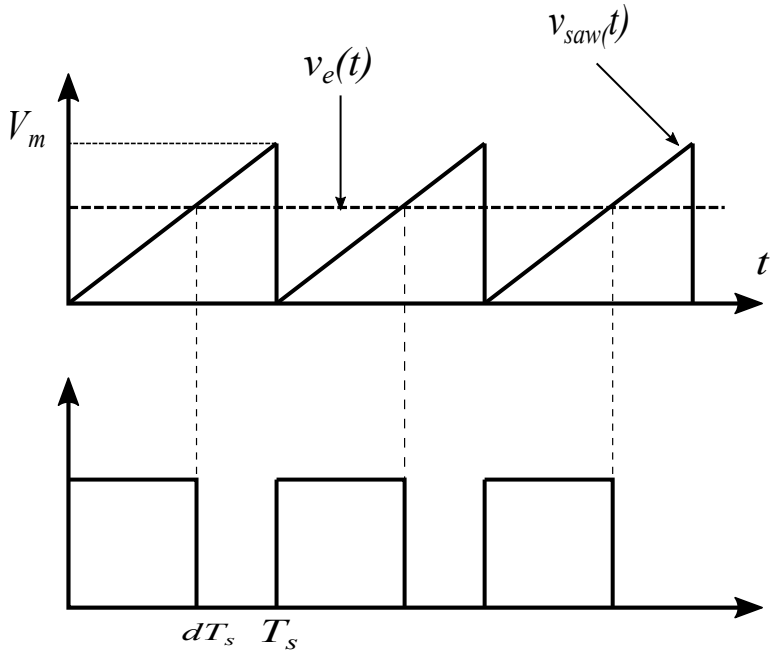


Fig. 5.13: PWM Generator Waveform

This is a non-linear equation and thus should be linearized. The perturbation of signal is given by

$$v_c(t) = V_c + \widehat{v}(t) \tag{5.65}$$

$$d(t) = D + \widehat{d}(t) \tag{5.66}$$

The perturbation of the variables results

$$D + \widehat{d}(t) = \frac{V_c + \widehat{v}(t)}{V_m} \tag{5.67}$$

The DC and AC relationship are given below

$$D = \frac{V_c}{V_m} \tag{5.68}$$

$$\widehat{d}(t) = \frac{\widehat{v_c}(t)}{V_m} \tag{5.69}$$

## 5.3 Introduction to Average Current Mode (ACM) Control

### 5.3.1 Introduction to voltage Mode Control

The Fig (5.14) shows the block diagram of the closed loop voltage control. The output voltage is sensed and scaled. It can be voltage divider and is represented as block (H) in the diagram.The sensed voltage is then compared with a reference voltage $V_{ref}$ and the resultant error signal ($v_e$) is obtained.This error signal is then passed through a compensator. This can be PI or PID one. The s-domain transfer function of the compensator is shown as $G_{cv}$. The compensator output provides the control signal $v_c$. This signal is then compared with a saw-tooth waveform to generate the gate driving signal of required duty cycle. It is labelled as PWM in the block diagram in the given figure (5.14)

The main aim is to design the compensator in frequency domain based on the required phase-margin and cross over frequency. To find the exact design we need to develop the transfer function of each blocks in the closed loop system. In order to model the closed loop system we need to develop the input to output transfer function $(G_{vg})$ and the duty-cycle to output transfer function $(G_{vd})$. Similarly the pulse width modulator should also be modelled. The fig (5.15) gives the brief idea

In-order to develop the converter transfer function we will be using the transformer model of the buck converter which is shown in fig(5.16).The transfer function are given as

$$G_{vd}(s) = \frac{G_{do}}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \tag{5.70}$$

In the case of buck converter the various terms of the standard form is given as

$$G_{do} = \frac{V}{D} \tag{5.71}$$

$$w_o = \frac{1}{\sqrt{LC}} \tag{5.72}$$

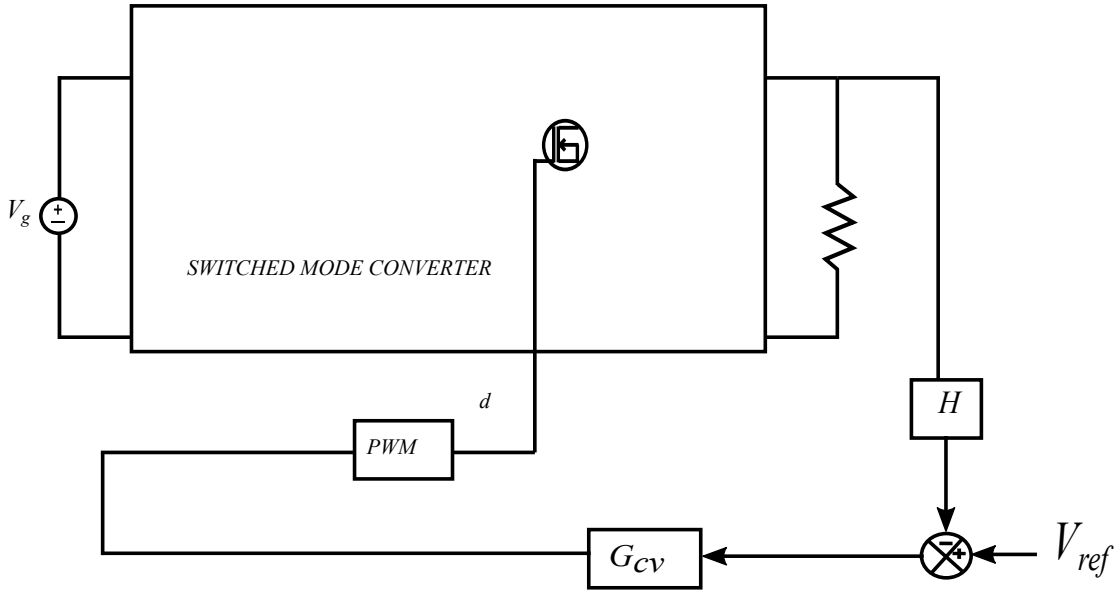


Fig. 5.14: Voltage Mode Control Block Diagram

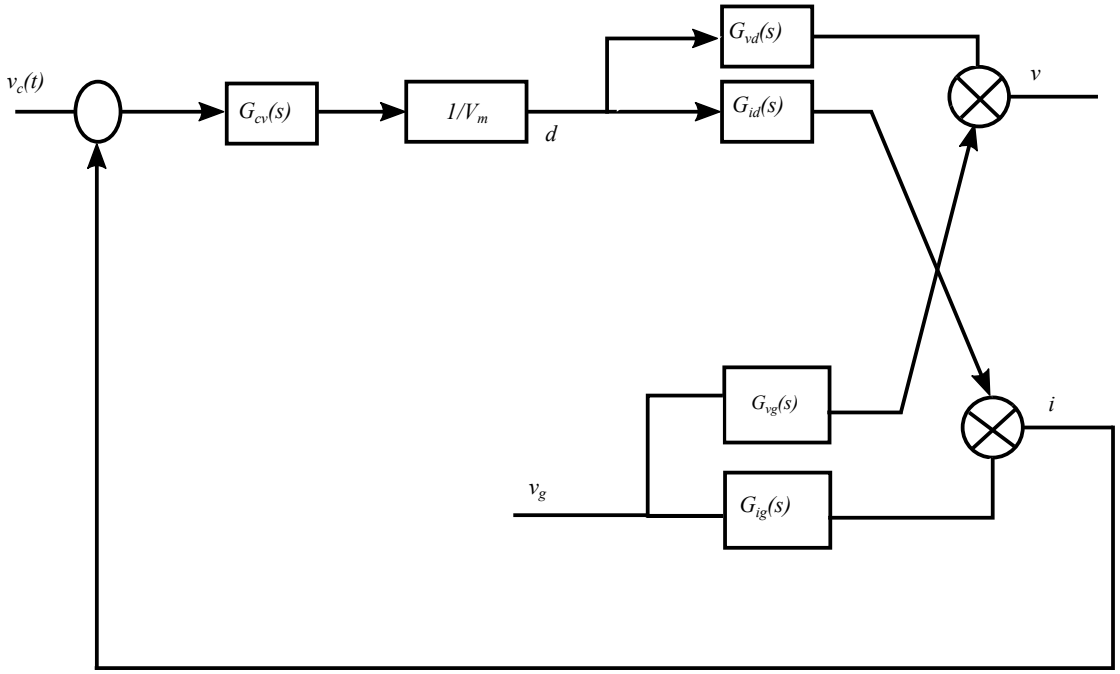


Fig. 5.15: Loop Transfer Function Block Diagram

$$Q = R * \sqrt{\frac{C}{L}} \tag{5.73}$$

$$G_{vg} = \frac{G_{go}}{1 + \frac{s}{Qw_o} + (\frac{s}{w_o})^2} \tag{5.74}$$

Where $G_{go}$ = D in the case of buck converter

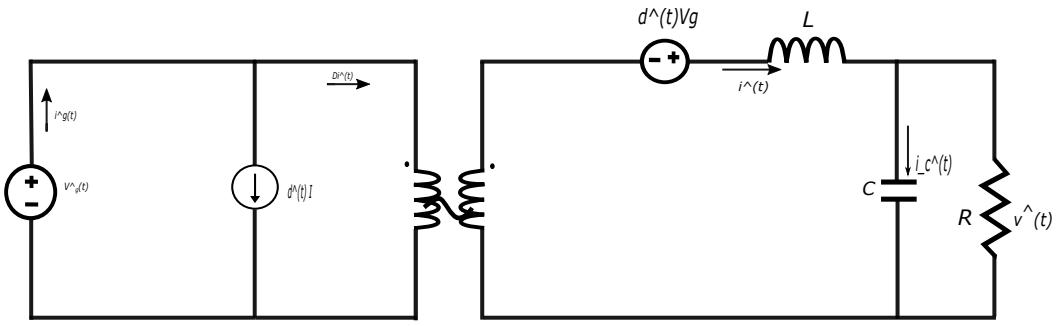


Fig. 5.16: Small Signal Transformer Model Of Buck Converter

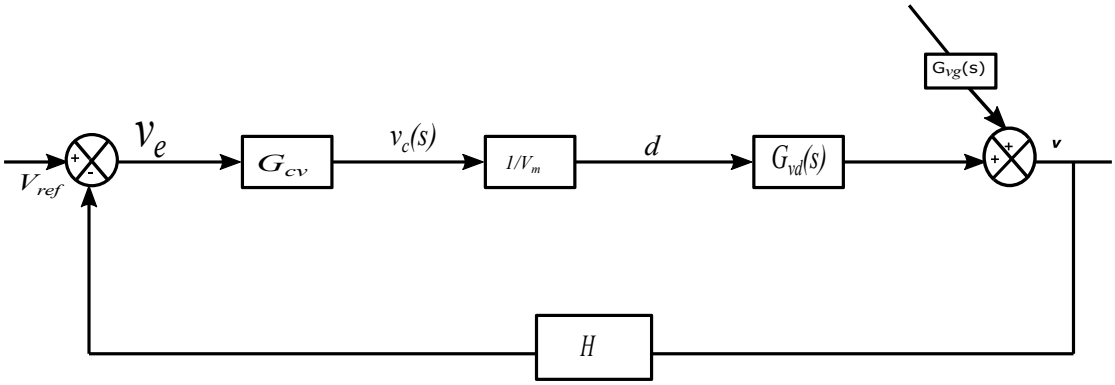


Fig. 5.17: Closed Loop Block Diagram

The fig (5.17) depicts the the closed loop block diagram including the compensator, PWM, converter and the sensor transfer function.

The closed loop transfer function between the $V_{ref}(s)$ and $v(s)$ is developed as below

$$\frac{V(s)}{V_{ref}(s)} = \frac{\frac{1}{H(s)} \cdot G_{vd}(s) \cdot \frac{G_c(s)}{V_m} \cdot H(s)}{1 + G_{vd}(s) \cdot H(s) \cdot \frac{G_{vc}(s)}{V_m}} \tag{5.75}$$

The loop gain $T(s)$ can be defined as

$$T(s) = G_{vd}(s) \cdot \frac{G_c(s)}{v_m} \cdot H(s) \tag{5.76}$$

Thus the eq 5.75 can be rewritten as

$$\frac{V(s)}{V_{ref}(s)} = \frac{1}{H(s)} \cdot \frac{T(s)}{1 + T(s)} \tag{5.77}$$

If we design the compensator such that the low frequency gain is very high i.e $T(0) >>$

1 then the eq (5.77) can be written at low frequency as in eq 5.78

$$\frac{V(s)}{V_{ref}(s)} = \frac{1}{H(0)} \tag{5.78}$$

Thus if the loop gain is very high at low frequency then the output will track the reference value and the desired output can be obtained Similarly the input voltage to output transfer function can be given as

$$\frac{V(s)}{V_g(s)} = \frac{G_{vg}}{1 + T(s)} \tag{5.79}$$

If the loop gain is very high mainly in the low frequency range then the disturbances due to input voltage can be removed as can be pointed out in eq (5.79)

### 5.3.2 Conditions that Need to be Followed While Designing the Compensator

- The desired phase margin should be in the range 30 to 50 degree
- The quality factor(Q) which is function of R,L and C should be less than .5
- The inductor(L) and capacitor (C) are designed based on the ripple requirement.
- The cross-over frequency should be less than the switching frequency
- The bode plot should cut the cross-over frequency at a slope of $20dB/decade$.
- The compensator should be designed such that the low frequency loop gain T(0) should be a large value.

### 5.3.3 Procedure of Design of the Compensator

- First the uncompensated loop gain is considered with the compensator transfer function $G_{cv}(s)$ =1.
- Find the current crossover frequency and phase margin and compare with the required value
- Use lag or lead compensator to get the required steady state error and phase margin
- Lag or PI controller is used to reduce the steady state error

- Lead or PD compensator is used to increase the phase margin

The total loop gain including converter transfer,compensator transfer function is given by

$$T_v(s) = G_{cv}(s) \cdot \frac{1}{V_m} \cdot G_{vd}(s) \cdot H(s) \tag{5.80}$$

The loop gain considering the compensator $G_{cv}$=1

$$T_v(s) = 1 \cdot \frac{1}{V_m} \cdot G_{vd}(s) \cdot H(s) \tag{5.81}$$

**Selection of phase margin**

An equation showing the relationship between the phase margin and quality factor is given as

$$Q = \frac{\sqrt{\cos \phi_m}}{\sin \phi_m} \tag{5.82}$$

| PHASE MARGIN | QUALITY FACTOR | PEAK OVERSHOOT |
|---|---|---|
| 52° | 1=0db | 16.3 % |
| 72° | .5=-6db | 10% |

Table 5.1: Relation Between Peak Overshoot, Phase-margin and Quality-factor

From the table 5.1 it can be concluded that the phase margin should be in the range between 52 to 72 for the peak overshoot to be in the range between 10 and 16.3

**Lead and lag compensator**

Base on the phase-margin requirement whether we need increase or reduce the phase-margin we will be using a lead or lag compensator.

An example for compensator the case of lead compensator is discussed. The transfer of lead compensator with pole frequency $w_p$ zero frequency $w_z$ and gain k is given as

$$G_c = \frac{k(1 + \frac{s}{w_z})}{(1 + \frac{s}{w_p})} \tag{5.83}$$

The pole and zero frequency can be calculated based on the phase margin and cross-over frequency are given as

$$f_p = f_c \cdot \sqrt{\frac{(1+\sin(\phi_m))}{(1-\sin(\phi_m))}} \tag{5.84}$$

$$f_z = f_c \cdot \sqrt{\frac{(1-\sin(\phi_m))}{(1+\sin(\phi_m))}} \tag{5.85}$$

Similarly the low frequency regulation can be further improved by addition of an inverted zero. Thus the PID controller can be defined as

$$G_c(s) = \frac{G_{cm} \cdot (1+\frac{s}{w_z}) \cdot (1+\frac{w_l}{s})}{(1+\frac{s}{w_p})} \tag{5.86}$$

## 5.4 Discussion On Average Current Mode Control

The fig 5.18 shows the total average current loop control block diagram with the inner current control and outer voltage control. The output voltage is sensed and compared with the reference voltage and the error signal is then passed through voltage compensator and the output of this compensator is made as the reference to the current sensed and the signal is passed to the inner current loop and thus produce the required gate signal.

Fig 5.19 shows the inner current loop with loop controller transfer function $G_{ci}(s)$.The compensator acts a low pass filter and controls only the average quantity. In this mode of control the average quantity is controlled rather than the peak value and it compared with a required reference.

The main advantages compared to peak current mode control is that it has better noise immunity due to low pass filter nature of the controller.It also can control average current accurately in wide range of application. The major disadvantage compared to peak current mode control is that it does not provide immediate peak transistor current limit and also does not mitigate transformer saturation problem in push-pull converters

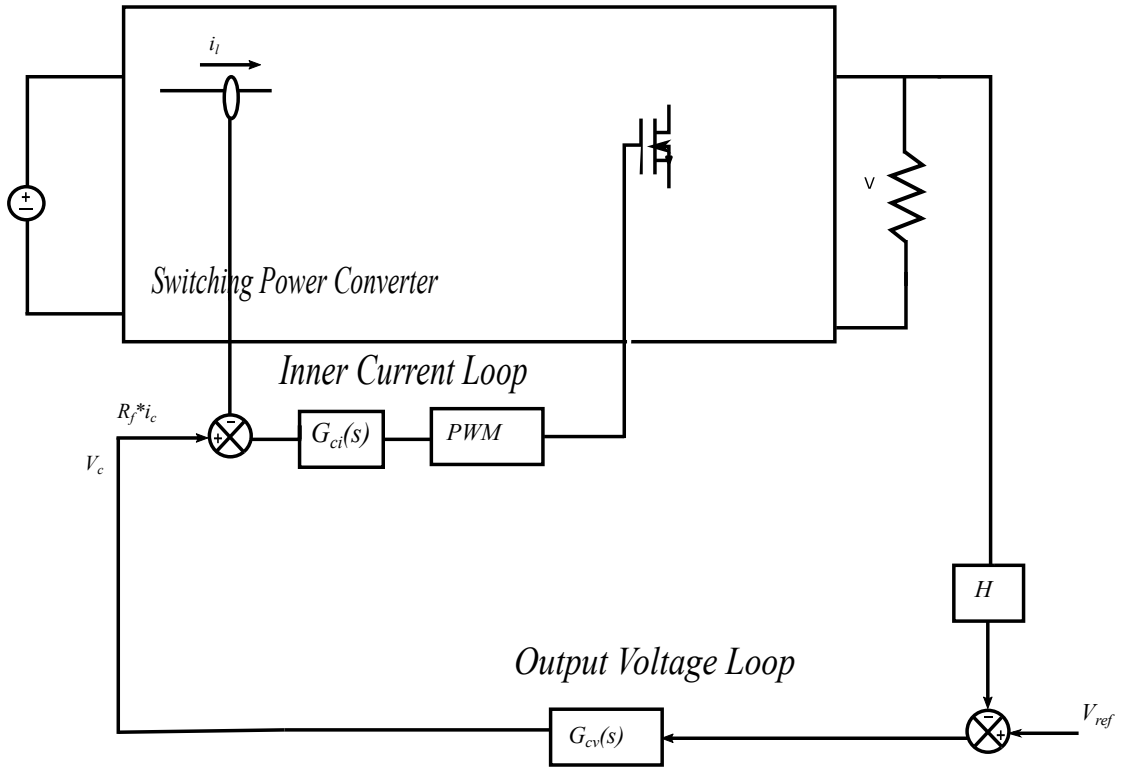


Fig. 5.18: Average Current Model Block Diagram

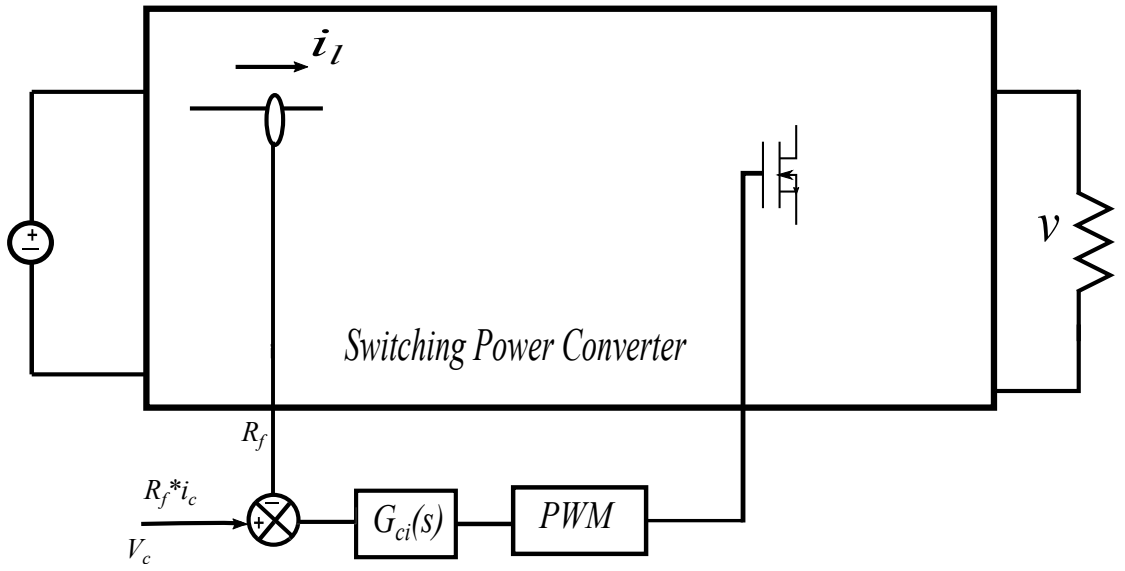


Fig. 5.19: Inner voltage Loop Block Diagram

### 5.4.1 Design of Current Loop compensator

In-order to design the current loop compensator we need the current to output voltage converter transfer function $G_{id}(s)$. The loop gain of the inner current loop is given as

$$T_i(s) = R_f \cdot G_{ic}(s) \cdot \frac{1}{V_m} G_{id}(s) \tag{5.87}$$

First we need to find the frequency response with the uncompensated loop gain to find present phase cross-over frequency and phase margin. In-order for that we need the converter duty-cycle to current transfer function which is given as

$$G_{id}(s) = \frac{i(s)}{d(s)}_{v_g(s)=0} \tag{5.88}$$

From the buck small signal ac model we can derive $G_{id}(s)$ as given below

$$G_{id}(s) = \frac{\frac{V}{D \cdot R} \cdot (1 + sRC)}{1 + s \cdot \frac{L}{R} + s^2 \cdot LC} \tag{5.89}$$

The generalized converter transfer function equation can be given as

$$G_{id}(s) = \frac{G_{ido} \cdot (1 + \frac{s}{w_{zi}})}{1 + \frac{s}{Q.w_n} + \frac{s^2}{w_n^2}} \tag{5.90}$$

$$G_{ido} = \frac{V}{D.R} \tag{5.91}$$

$$Q = R \cdot \sqrt{\frac{C}{L}} \tag{5.92}$$

$$w_n = \frac{1}{\sqrt{L \cdot C}} \tag{5.93}$$

$$w_{zi} = \frac{1}{R \cdot C} \tag{5.94}$$

The compensator design is similar to explained before.The closed loop transfer func-

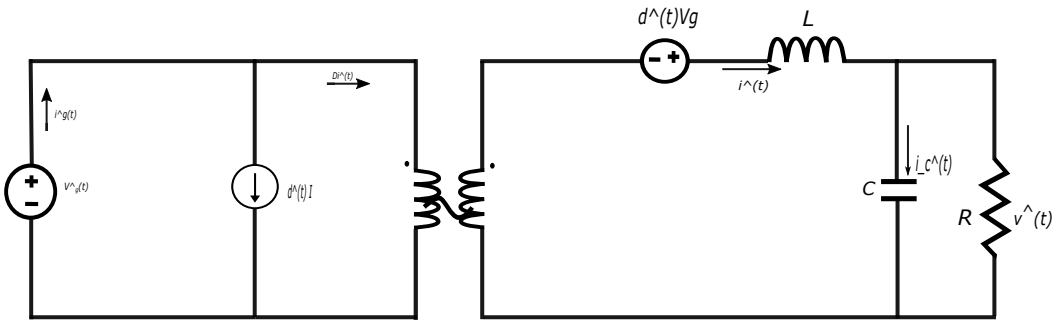


Fig. 5.20: Transformer Model Of Buck Converter

tion frequency response is studied and based on required phase margin either lead or lag compensator is designed.The required compensator $G_{ci}(s)$ is obtained.The uncom-

penasted loop gain is given as

$$T_{iu}(s) = R_f \cdot \frac{1}{V_m} \cdot G_{id}(s) \tag{5.95}$$

$$T_{iu}(s) = T_{iuo} \cdot (\frac{1 + \frac{s}{w_{zi}}}{1 + \frac{s}{Q \cdot w_n} + \frac{s^2}{w_n^2}}) \tag{5.96}$$

$$T_{iuo} = R_f \cdot \frac{1}{V_m} \cdot G_{ido} \tag{5.97}$$

**Asymptotic behaviour of Uncompensated current loop gain around cross-over frequency**

$$T_{iu}(s) = T_{iuo} \cdot (\frac{1 + \frac{s}{w_{zi}}}{1 + \frac{s}{Q \cdot w_n} + \frac{s^2}{w_n^2}}) \tag{5.98}$$

At frequency near the cross-over frequency the eq (5.98) can be approximated as

$$T_{iu}(s) = T_{iuo} \cdot \frac{\frac{s}{w_{zi}}}{\frac{s^2}{w_n^2}} \tag{5.99}$$

$$T_{iu}(s) = T_{iuo} \cdot \frac{w_n^2}{\frac{w_{zi}}{s}} \tag{5.100}$$

$$T_{ius} = \frac{R_f}{V_m} \cdot \frac{V}{L} \cdot . \frac{1}{s} \tag{5.101}$$

Thus the uncompensated current loop equation can be approximated as eq (5.101) around the cross-over frequency and can be used in the entire closed loop design

For the current loop compensator we need only a proportional controller to make the gain 1 at the required crossover frequency But we are using an inverted zero along with an high frequency pole.The inverted zero make sure high low frequency gain to maintain zero steady state error.The high frequency pole behaves more like a low pass filter to attenuate high frequency noise and ripple.

Thus the compensator transfer function can be defined as

$$G_{ci}(s) = G_{cm} \cdot (\frac{1 + \frac{w_z}{s}}{1 + \frac{s}{w_p}}) \tag{5.102}$$

Around cross-over frequency we can reduce the loop gain with compensator as

$$T_i(s) = G_{cm} \cdot \frac{R_f}{V_m} \cdot \frac{V}{L} \cdot \frac{1}{s} \tag{5.103}$$

From these equation we need to find the gain and zero and pole frequency based on the required phase-margin.

**Outer Voltage Loop Design**

The main objective is to design the outer voltage loop compensator $G_{cv}(s)$.The control to current transfer function is given as

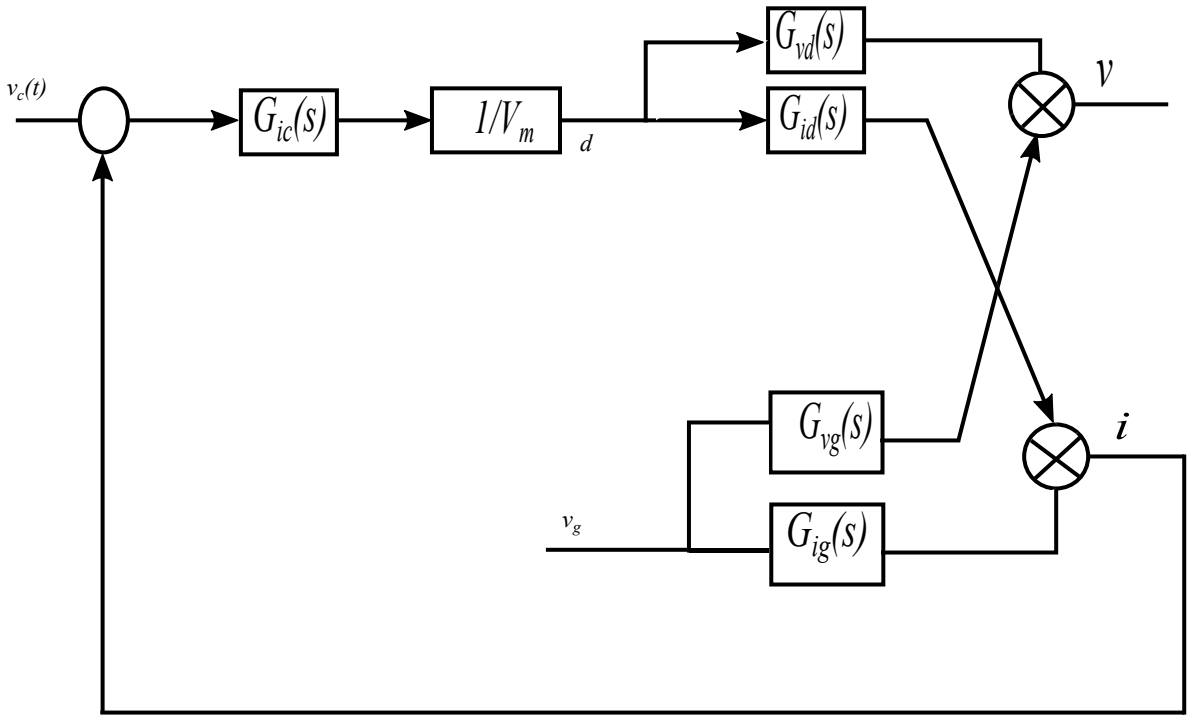


Fig. 5.21: Loop Transfer function Block Diagram

$$T_i(s) = G_{ic}(s) \cdot \frac{1}{V_m} \cdot G_{id} \cdot R_f \tag{5.104}$$

$$G_{ic}(s) = \frac{G_{ci} \cdot \frac{1}{V_m} G_{id}}{1 + G_{ci} \cdot \frac{1}{V_m} \cdot G_{id} \cdot R_f} \tag{5.105}$$

$$G_{ic}(s) = \frac{i}{v_c} \tag{5.106}$$

$$G_{ic} = \frac{(G_{ci} \cdot \frac{1}{V_m} \cdot G_{id} \cdot R_f)}{1 + G_{ci} \cdot \frac{1}{V_m} \cdot G_{id} \cdot R_f} \cdot \frac{1}{R_f} \tag{5.107}$$

$$G_{ic} = \frac{1}{R_f} \cdot \frac{T_i}{1 + T_i} \tag{5.108}$$

For the frequencies well below the cross-over frequency the current loop.

$$G_{ic} = \frac{i}{v_c} \approx \frac{1}{R_f} \tag{5.109}$$

The next step is to find the relationship between the control voltage and the output voltage

$$G_{vc} = \frac{v}{v_c} \tag{5.110}$$

$$i = G_{id} \cdot d \tag{5.111}$$

$$i_c = \frac{v_c}{R_f} \tag{5.112}$$

$$\frac{d}{v_c} = \frac{1}{R_f} \cdot \frac{1}{G_{id}} \tag{5.113}$$

$$G_{vc} = \frac{v}{v_c} = \frac{v}{d} \cdot \frac{d}{v_c} = \frac{1}{R_f} \cdot \frac{G_{vd}}{G_{id}} \tag{5.114}$$

The reduced and approximate loop gain block diagram is shown in fig (5.22). The final

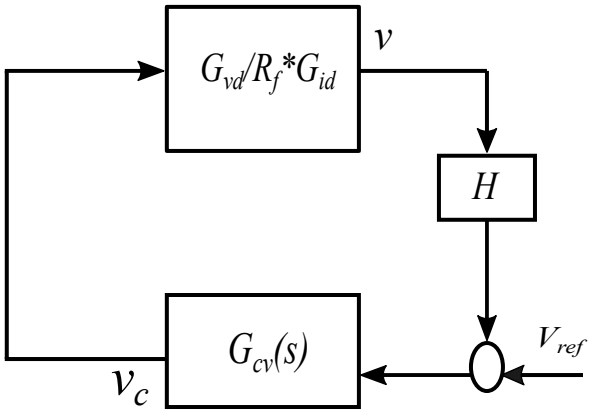


Fig. 5.22: Outer Loop Voltage With Reduced Inner Current Loop

voltage loop gain is given as

$$T_v \approx H \cdot G_{cv}(s) \frac{1}{R_f} \frac{G_{vd}}{G_{id}} \tag{5.115}$$

The uncompensated loop gain is given as

$$T_{vu}(s) = H \cdot G_{vc}(s) \tag{5.116}$$

The uncompensated loop frequency response is plotted and based on required improvement in frequency response the compensator is designed.Determine voltage-loop compensator transfer function Gcv to achieve the desired cross-over frequency (well below the cross-over frequency of current loop) and phase margin

### 5.4.2 Average Current Mode Control Simulation Study And Results

Based on the required converter parameters that is 48 V to 14 V, the inductor and capacitor values were calculated based on the ripple requirements. Thus the obtained parameters are given in table below. The fig 5.23 shows the input to gate of the buck

| **Parameter** | **Value** | **Unit** |
|---|---|---|
| Inductor(L) | 3 | $\mu H$ |
| Capacitor(C) | 6.8 | $\mu F$ |
| Resistor(R) | .916 | $\Omega$ |
| Input/Output Voltage | 48/14 | V |
| Output Power | 1 | kW |

Table 5.2: Parameters And Value For Buck Converter Simulation

switch. It is obtained through closed loop average current mode control by sensing the current in the inner loop and output voltage in outer loop and the duty cycle of the obtained gate pulse is same as required duty cycle $V_o/V_g = 14/48 = .2916$.

The fig 5.24 shows the output voltage obtained. It shows an output voltage of average 14 V with ripple of 2%.

The fig 5.25 shows the output current waveform with average value of 71.3 with a ripple of 10 % as per the design.

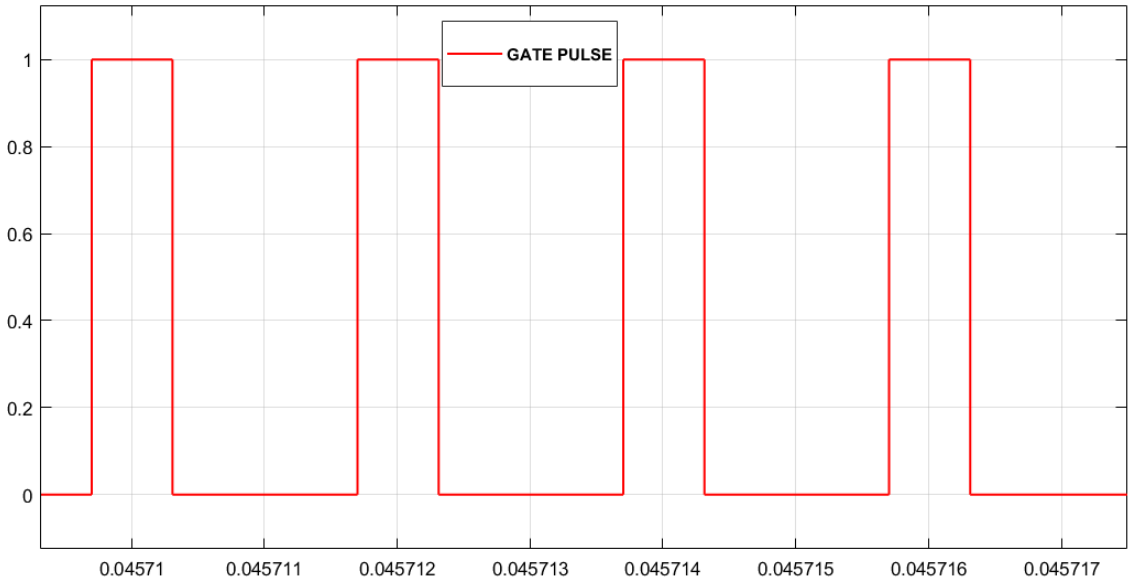


Fig. 5.23: Gate Pulse For Buck Switch

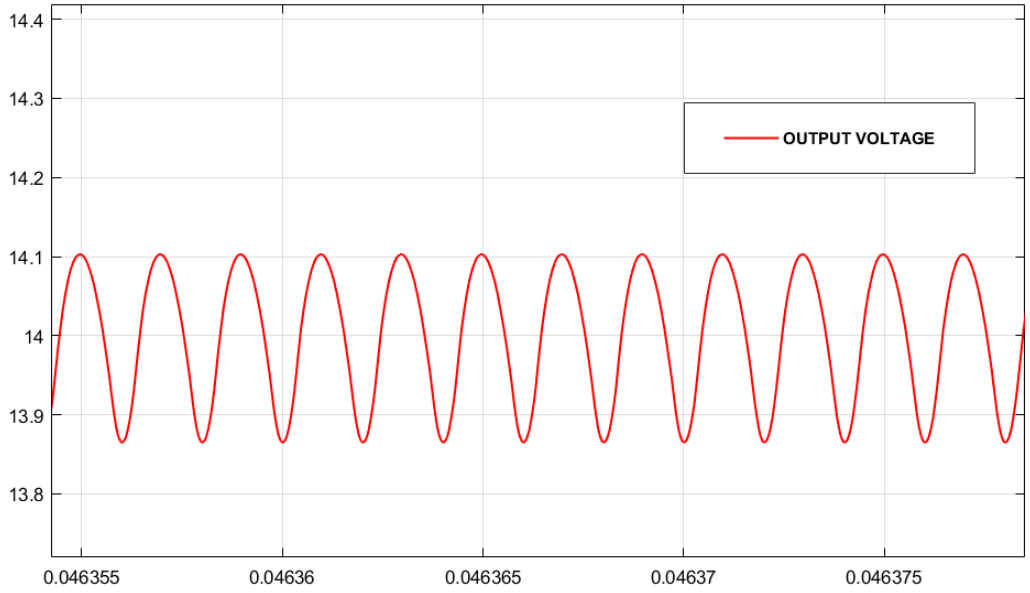


Fig. 5.24: Output Voltage Waveform

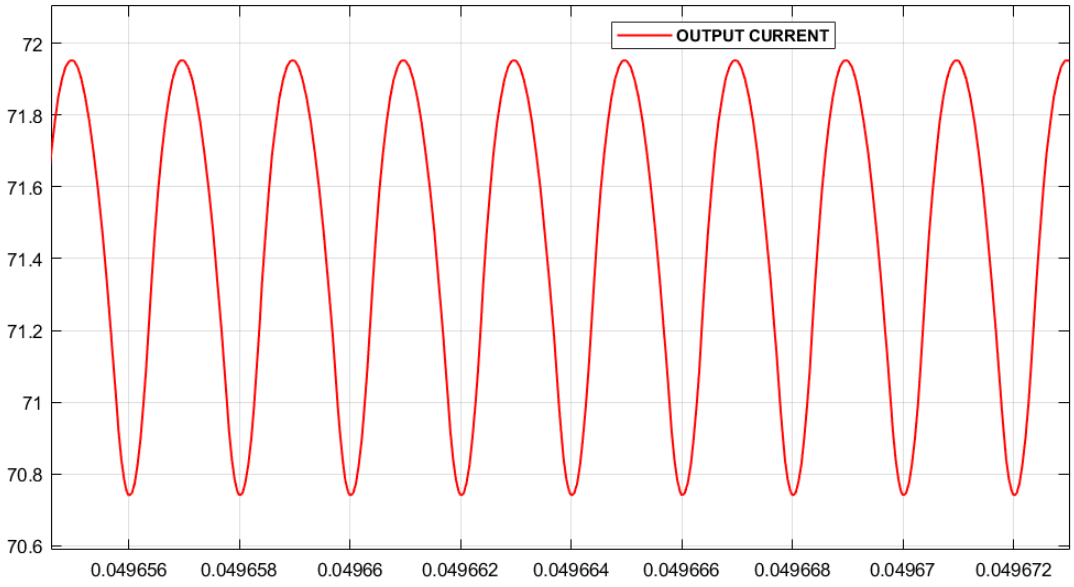


Fig. 5.25: Output Current Waveform

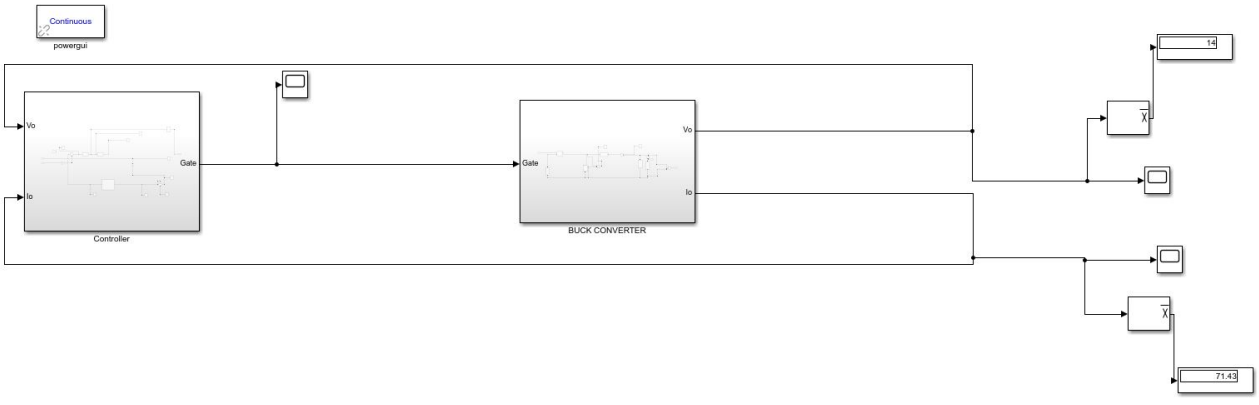


Fig. 5.26: Entire Simulink Model

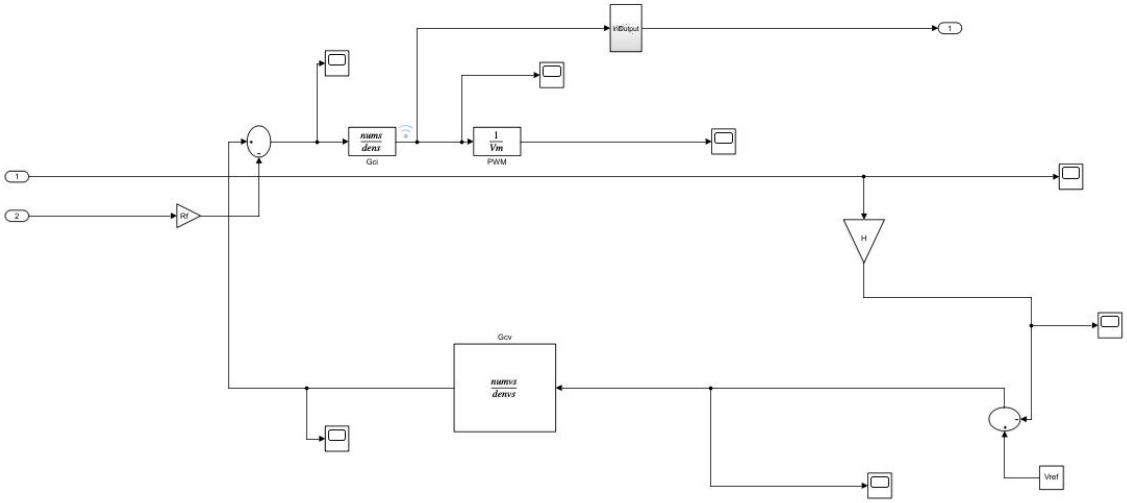


Fig. 5.27: Controller Simulink Model

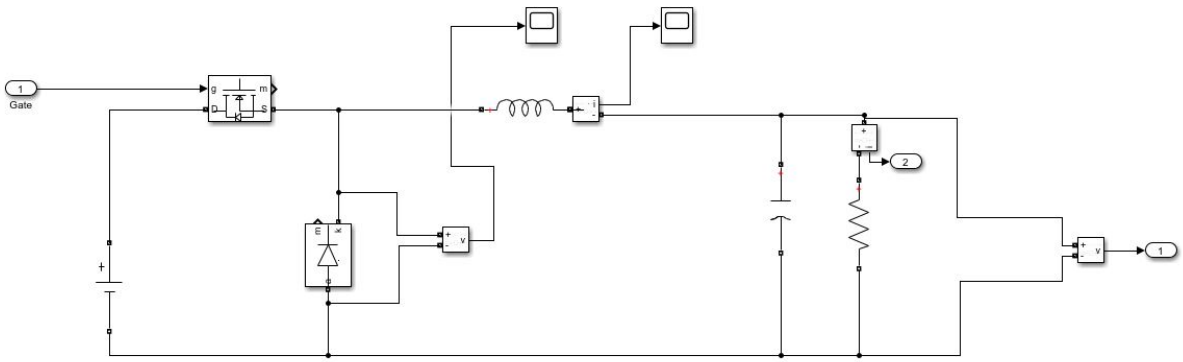


Fig. 5.28: Converter Simulink Model

# CHAPTER 6

# Conclusion And Future Scope

As today's world demands more energy saving and efficiency whether it in case of using renewable resources or moving to fully electric vehicles the need for energy conversion is really important. Power electronic devices and designs plays crucial role in these areas. We need efficient power converter which can be as made as small and with high efficiency. The size of each converter depends on the energy storage elements used for power conversion. To reduce the size of these elements results in the overall reduction in the converter size. One way of attaining this by operating the devices at higher operating frequency.The disadvantage of operating at higher frequency switching loss, which demands for larger heat sinks. This will suppress the reduced size of converter by higher frequency operation. So these switching losses has to be reduced. One way using the principle of soft switching with the help of resonant converters. But proper design must be followed so that the reduction in switching losses won't increases the conduction losses.

The development in the field of silicon devices has reached the limits. The new trend is the use of wide band gap devices like GaN and SiC. These power devices have more advantages compared to previous silicon based devices. Usage of the new power devices results in high frequency operation and reduction in converter size and thus saving the board space.

Another new approach in power converter design is by interleaving or multi-phasing the converter model thus the power flow is divided in different branches in parallel. Thus it helps in the reduction in rating of switches and other energy storage elements and proper control of each branches based on power output requirement,can be controlled.

The normal method of control of converter is usually in the analog doamin with op-amp based PID compensator and other analog blocks.But with the easy availability

of FPGA devices in which hardware can programmed and re-programmed and can add associated software, the usage of digital control is increasing now days like the use of digital compensator digital PWM etc. So more study has to be done in this field also.

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