STUDY AND DEVELOPMENT OF COMPACT HIGH POWER DENSITY CONVERTER FOR BATTERY CHARGER APPLICATIONS

A Project Report

Submitted by

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in partial fulfilment of the requirement for the award

of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY MADRAS

CHENNAI-600 036, INDIA

JUNE 2021

Thesis certificate

This is to certify that the thesis titled STUDY AND DEVELOPMENT OF COMPACT HIGH POWER DENSITY CONVERTER FOR BATTERY CHARGER APPLICATIONS, submitted by G.BHARATH REDDY, to the Indian Institute of Technology, Madras, for the award of the degree of Master of Technology, is a bonafide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 18^{th} june 2021

Acknowledgement

I would like to express my sincerest gratitude to Dr.Kamalesh Hatua for giving me the opportunity to work on a project as ambitious as this one. The experiences I have gathered and the invaluable lessons I have learned while working on this project have endowed me with a renewed interest in the area of High Power Compact Converters and this would not have been possible without him guiding me every step of the way. Research would be a lot harder without well-meaning seniors to help skip a few hurdles. I would be forever grateful to Arunava sir,Surja, Sakthi for sharing with me their insights and experiences, pointing me to useful resources, helping me find new angles to look at the problem and above all, making the lab a much homelier place. I would like to thank my parents for always supporting me no matter what. It is their support that gave me the assurance needed to pursue an M.Tech instead of doing a job. I've been truly blessed to have known all these people and I hope I can make it worthwhile for them as well through my work.

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Chapter 1

Introduction

The large number of automobiles that are in use around the world has created and continues to cause major environmental and human health problems.Pollution, global warming, and the fast depletion of the petroleum reserves are the major issues today. In future, electric vehicles (EVs), hybrid electric vehicles (HEVs), and fuel cell electric vehicles (FCEVs) will replace conventional automobiles. Electric vehicles (EV) have developed rapidly because of its high efficiency and pollution-free advantages. By increasing or chopping the voltage levels, DC-DC converters can be utilised to interface the elements in the electric power train. The power converter construction must be reliable, lightweight, small in volume, high in efficiency, low in electromagnetic interference, and low in current/voltage ripple due to automotive limitations.

1.1 Background

The DC-DC converters used in BEV and PHEV powertrains, primarily use Si-based [1] semiconductors which limits their efficiency to 92–93%, allows for a maximum switching frequency up to 30 kHz and achieve only 3–12 W/in^3 power density. However, due to their physical properties and characteristics, the performance of Si-based semiconductors is limited, and further development of Si-based semiconductors is not considered. Various innovative technical improvements have been introduced through Si-based power transistor technology, but progress has slowed as

the technology matures.New power transistor technologies based on new material systems have received a lot of interest in recent years. Gallium Nitride (GaN) power transistors have emerged as a disruptive technology with great potential, owing to the outstanding material properties of GaN [2],[3], that is the use of Wide Band Gap elements, which has resulted in drastic improvements in power density (50 W/in^3) and efficiency while ensuring better manufacturability at low cost. Due to its capacity to handle large power ranges up to 100 kW, reduced cost, superior packaging, high thermal conductivity, and market availability, recent research into WBGSs has discovered that silicon carbide (SiC) semiconductors are particularly ideal for designing high powered DC-DC converters. GaN semiconductors, on the other hand, have reached commercial maturity, with breakdown voltages of less than 600 V and power ratings of less than 5 kW. More research on GaN-based semiconductors, is needed to develop converter adaptability.

1.2 Goals Of Project

The report mainly discusses the implementation of a high power DC-DC resonant converters and is extended towards Dual Active Bridge(DAB) since a bi-directional converter can move power in either direction, which is useful in applications requiring regenrative braking.Further, Implementation of closed loop control methods to control the output voltage as well as circulating energy is shown.

1.3 Outline of the thesis

In Chapter 2 a very basic description of the superiority of GaN over Si based switches will be discussed, various types of GaNFETs available in today's market and their manufacturers, the use of GaN will be discussed as well.

Chapter 3 explains vividly about the different types of resonant tank circuits based series resonant converters and the gains achevied by respective tanks is studied.

In chapter 4 Dual Bridge series resonant converter(DBSRC) is explained and the used topology is discussed with design calculations and simulation results.In chapter 5 deals with the small signal

modelling of DBSRC and control to ouput transfer functions. In chapter 6 triple phase shift control is implemented to control the circukating energy and simulation results expalined in detail.

Chapter 2

Gallium Nitride (GaN)

2.1 About GaN

"Moore's Law or Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved."Simply put, over the time of electronic circuits, more It's smaller and smaller, which makes the device more compact. In this endless space competition, miniaturization and high power density have become major challenges for modern power electronics converters. We want more compact converters with higher power densities than, so GaN is gradually emerging as a possible alternative. Now I get the question the electron mobility more is the drift velocity, resulting in lower RDSON [7]-[11]. As GaNFET has lower RDSON e.g. the device used has 7mΩ resistance for ratings of 100V and 36A. Therefore, due to lower On resistance, conduction losses are low which results in better efficiency. Another advantage of GaN devices is that GaNFETs have lower device capacitances, i.e. CISS,COSS,CRSS i.e. the Input, Output and Reverse transfer capacitances are in the order of few pF's hence smaller charge is required to charge the device capacitances to turn ON the device resulting in Turn On time of a few ns, resulting in higher f_s. GaN can be switched at a higher switching frequency. Due to this small turn On/Off time of the device we can switch the devices at a very high switching frequency at a few MHz, higher switching frequencies result in the reduction of the size of the magnetics used in the converter. The size of a converter is quite majorly decided by the size of

the inductor and the capacitor used in it. Higher f_s results in decreased size of both capacitors and inductors hence making the converter more compact. GaNFET converters have Lesser FOM (Fifure of Merit) that is the product of $R_{DS_{On}}$ and Q_{On} is less[11], hence losses are less, as a result air cooling is sufficient for such converters. For high power converters new cooling methods can be implemented to make the converter more efficient.

2.2 Working of GaN

GaN is piezoelectric in nature, that is, if we apply pressure on a GaN layer, it will generate a voltage of or electrons. Now if we apply a layer of AlGaN over it, the same strain will generate more electrons, which will generate a two-dimensional electron gas [12], which leads to a higher current passing through it.

2.3 Types Of GaN

1. Depletion mode type: The GaNFET depletion mode type is a naturally enabled type device, but when a negative gate source voltage is applied, the will be disabled. The depletion-mode transistors are impractical because when starting up the power converter the negative bias must first be applied to the source devices as otherwise it will result in a short circuit.

2. Enhancement mode type: In recent times a new technology of GaNET has been developed namely the Enhancement mode type or eGANFETs, in such technology when a zero voltage is applied on the gate, the electrons are wiped off and the device turns off and when a positive voltage is applied to the gate it pulls the electrons to the surface completing the circuit hence turning ON the device.

2.4 Usage of GaN

since GANFET can operate at very high frequencies, those are widely used in Microcontrollers, SSDs, antennas, RF MOSFETs, RF Amplifiers, RF Switch ICs, Power MOSFETs, High Power LEDs and Batteries.

2.5 Conclusion

In short, there have been discussions about GaN in the market today.We also see many reasons that GaN may become a replacement for Si-based devices in the near future. Among the many mentioned uses of GaN in power electronic equipment, field GaNFETs are becoming more and more popular because of their ability to switch to such a high frequency as .Therefore, the development of compact and efficient converters for high power ratings will not Then there is the challenge.

Chapter 3

Resonant Converters

In power converters ,key issues are power density and energy conversion efficiency. The size of passive components must be lowered in order to boost the power density. This is accomplished by using higher frequencies. The major problem in using hard switching converters is switching losses , which has a significant impact on efficiency. Resonant power converters may be a superior approach for limiting these losses. The main benefit of resonant converters is soft switching, which eliminates the difficulty of running at high frequencies [13]. The use of a resonance tank allows turning ON of switches under zero voltage (ZVS)[14] and/or turning OFF under zero current (ZCS) [15], thus switching losses are eliminated and then, efficiency of the converter can be increased.

Fig 3.1 presents the schematic of a DC-DC resonant converter. Both half and full bridge can be used to design the ac/dc or dc/ac converters.The resonant tank is a circuit of different combinations of inductive and capacitive components, which allows soft switching under some considerations. High frequency transformer is used to provide the galvanic isolation between source side and load side.

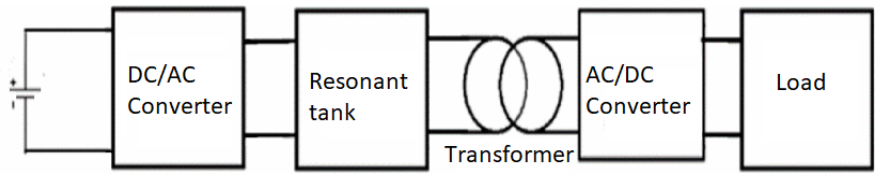

Figure 3.1: Structure of DC-DC resonant converter

The first harmonic approximation (FHA) [16] is used to investigate the features of resonant converters. It's a simplified way for determining the equivalent electrical circuit of a resonant converter by converting the current and voltage forms to a sinusoidal form while ignoring the effects of higher-order harmonics.

3.1 Series Resonant Converter Analysis

3.1.1 Equivalent Circuit

A series resonant converter's (SRC) resonant tank is made up of an inductor L_r linked in series with a capacitor C_r. The topology of SRC is depicted in Figure 3.2. The FHA method is used to determine the equivalent circuit. It is based on the idea that the fundamental harmonic of the Fourier expression of currents and voltages is almost fully associated with the power transfer from the source to the load through the resonant circuit. The switching frequency's harmonics are therefore ignored, and the resonant circuit's waveforms are presumed to be perfectly sinusoidal at the fundamental frequency.

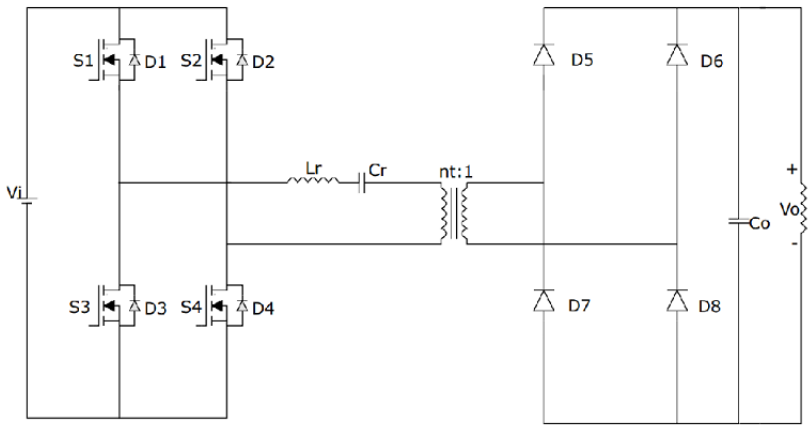

Figure 3.2: Series Resonant Converter

A square voltage V_i is produce at the output of inverter and that can be expressed by the Fourier series in Eqn 3.1 and only its fundamental component given by Eqn 3.2 is injected into the resonant tank.The output voltage V_o is described in Eqn.3.3 and its fundamental component is written in Eqn .3.4.With the capacitive output filter, a DC current I_{out} can be obtained and

injected into the load. The equivalent load resistance R_e is expressed in Eqn 3.5.

$$V_i = \frac{4.V_{in}}{\pi} \sum_{i=1,3,5..} \frac{1}{n} \sin(n\omega_s t) \tag{3.1}$$

$$V_{i1} = \frac{4.V_{in}}{\pi} \sin(\omega_s t) \tag{3.2}$$

$$V_o = \frac{4.V_{out}}{\pi} \sum_{i=1,3,5..} \frac{1}{n} \sin(n\omega_s t - \phi_v) \tag{3.3}$$

$$V_{01} = \frac{4.V_{out}}{\pi} \sin(\omega_s t - \phi_v) \tag{3.4}$$

$$R_e = \frac{8}{\pi^2} R \tag{3.5}$$

3.1.2 Voltage gain

The series resonant converter behaves as a voltage divider and its voltage gain H is given by (3.6). To write the gain in the standard form, the following variables are defined, Q the quality factor (3.7), and f_r the resonance frequency (3.8).

$$H = \frac{V_o}{m.V_i} = \frac{R_e}{R_e + j\omega_s L_r + \frac{1}{j\omega_s C_r}} \tag{3.6}$$

$$Q = \frac{1}{Re} \sqrt{\frac{L_s}{C_r}} \tag{3.7}$$

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{3.8}$$

By readjusting the eqn 3.6, the voltage conversion ratio can be expressed as:

$$H = \frac{1}{1 + jQ(\frac{f_s}{f_r} - \frac{f_r}{f_s})} \tag{3.9}$$

Fig 3.3 shows the schematic of voltage gain module as a function of the normalized frequency $f_n = f_s/f_r$ for different values of Q.

3.1.3 Merits and Demerits

The switching frequency is always kept higher than the resonant frequency because ZVS conditions ($f_n > 1$) is highly preferred than ZCS conditions [17].

The secondary side of the transformer acts as a current source to the load, so only a filter capacitor is sufficient.

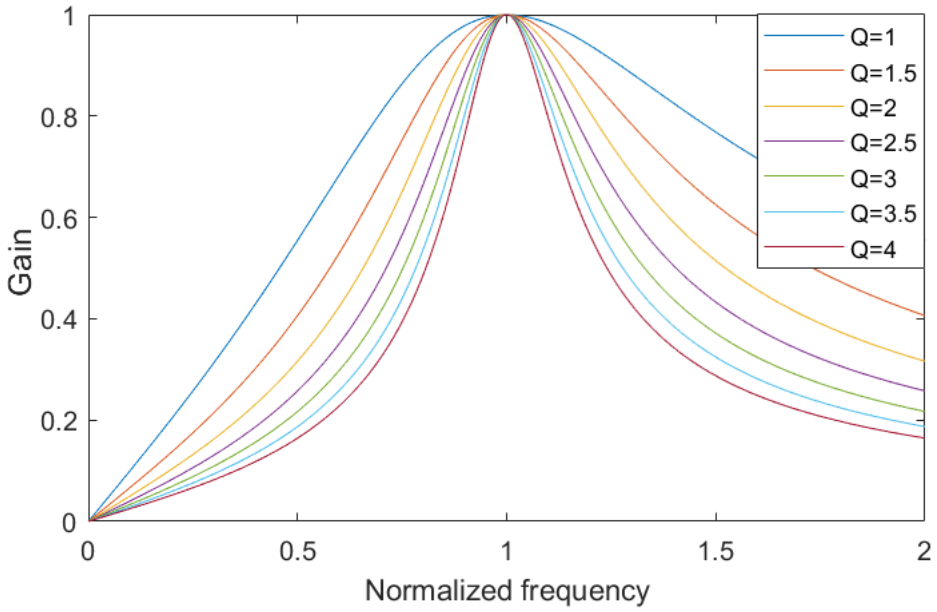

Figure 3.3: Voltage gain of series resonant converter

Conduction losses reduces as the load decreases, so low load efficiency is preserved.

Series resonant converter behaves as a voltage divider, thus the maximum voltage gain is unity

The performance at low load and high input voltage conditions is degraded. As seen in fig.3.3, for light loads, the frequency will be very high if input voltage increases a lot and then efficiency will be degraded.

3.2 Parallel Resonant converter Analysis

3.2.1 Equivalent circuit

The topology of a parallel resonant converter is shown in Fig.3.4 (PRC). The load is connected to the resonant capacitor in series [18]. We get the same input voltage equations using the FHA approach. The difference between the series and parallel topologies is that the parallel capacitor acts as a voltage source on the secondary side, which must be filtered further at the output by an LC filter. Eqn. 3.10 and 3.11 gives the equivalent resistance and output current.

$$R_e = \frac{\pi^2}{8} R \tag{3.10}$$

$$I_{o1} = \frac{4.I_o}{\pi} \sin(\omega_s t - \phi_i) \tag{3.11}$$

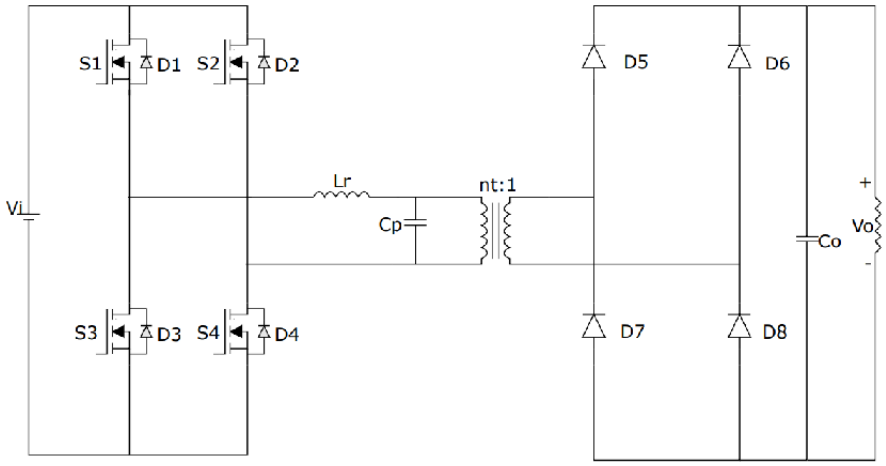

Figure 3.4: Parallel Resonant converter

3.2.2 Voltage Gain

Based on the equivalent circuit, the voltage gain is expressed by the Equation 3.12.

$$H = \frac{R_e||j\omega_s C_r}{j\omega_s L_r + (R_e||j\omega_s C_r)} \tag{3.12}$$

To put the gain under the standard form, the quality factor is defined in Eqn 3.13 and then the voltage gain expression is given in Eqn 3.14. Fig.3.5 shows the schematic of the voltage gain module as a function of the normalized frequency for different values of Q.

$$Q = R_e\sqrt{\frac{C_r}{L_r}} \tag{3.13}$$

$$H = \frac{1}{(1-(\frac{f_s}{f_r})^2) + j\frac{f_s}{f_r Q}} \tag{3.14}$$

3.2.3 Merits And Demerits

The light load problem does not exist because the operating region of the parallel resonant converter is much smaller than series resonant converter The converter is designed to work in ZVS conditions which is achieved on the right zone of the voltage gain(f_n >1). Narrow input voltage range and invariable load applications are more preferred. The resonant tank has small impedance and the resonant current is high, thus the reactive power is high.

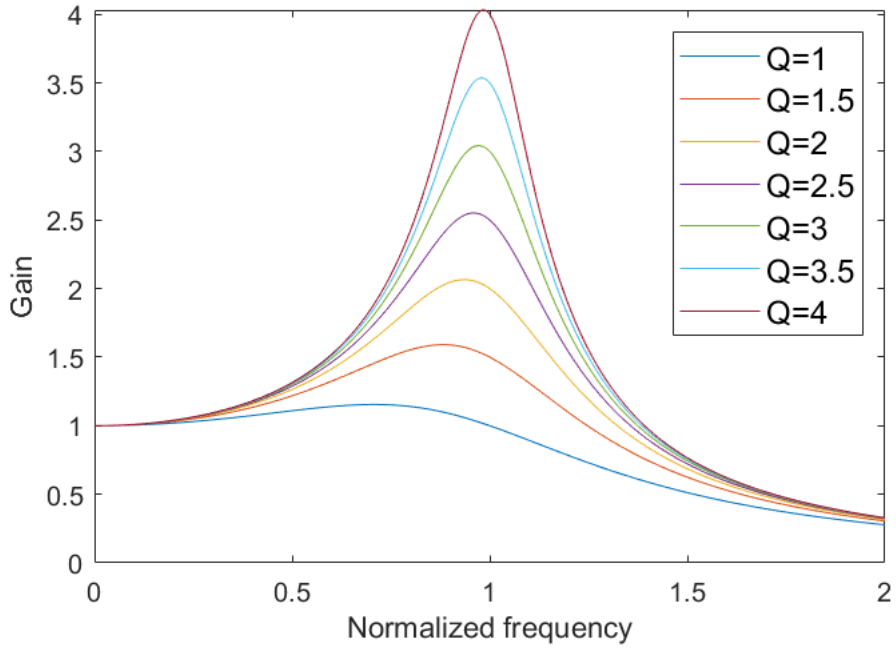

Figure 3.5: Voltage gain of parallel resonant converter

3.3 Series Parallel Resonant Converter Analysis

3.3.1 Equivalent Circuit

The resonant tank is composed of a series inductor L_r series capacitor C_r and a parallel capacitor C_p Fig.3.6 shows the topology of series parallel resonant converter.

3.3.2 Voltage Gain

Based on the equivalent circuit, the voltage gain is given by Eqn 3.15. Quality factor and resonance frequency are given in Eqn 3.16 and 3.17.

$$H = \frac{R_e||j\omega_s C_r}{j\omega_s L_r + \frac{1}{j\omega_s C_r} + (R_e||j\omega_s C_r)} \tag{3.15}$$

$$Q = Re\sqrt{\frac{C_e}{L_r}} \tag{3.16}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_e}} \tag{3.17}$$

where $C_e = C_r||C_p$

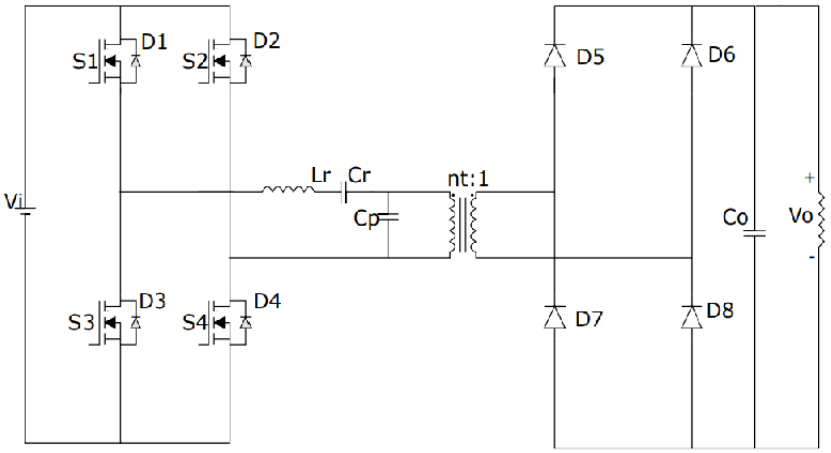

Figure 3.6: Series Parallel Resonant Converter

The gain in standard form is expressed in Eqn 3.18. Fig.3.7 shows the schematic of the voltage gain for different values of Q.

$$H = \frac{1}{[(1+\frac{C_p}{C_r}).(1-(\frac{f_s}{f_r})^2] + [j\frac{1}{Q}(\frac{f_s}{f_r} - \frac{f_r C_p}{f_s(C_p+C_r)})]} \tag{3.18}$$

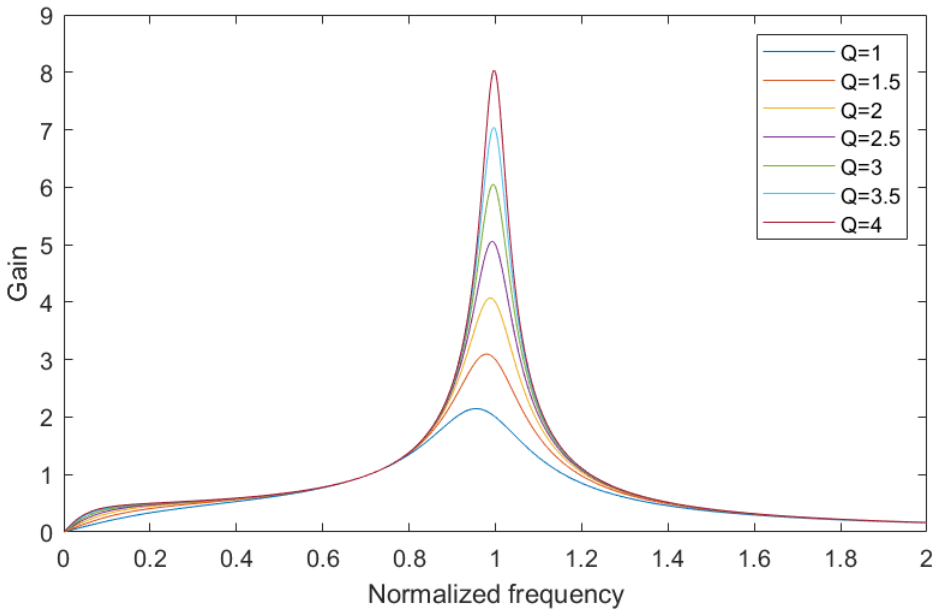

Figure 3.7: Voltage gain of series parallel resonant converter

3.3.3 Merits And Demerits

Smaller circulating energy compared to parallel resonant converter because of the series capacitor. Voltage regulation is achieved at no load conditions, so main drawback of series resonant converter is eliminated. High switching losses for applications with large voltage range and high input voltage.

3.4 LLC Resonant Converter Analysis

3.4.1 Equivalent Circuit

The resonant tank of a LLC resonant converter is composed of three element, a capacitor C_r and two inductors L_m and L_r.The LLC converter behaves as a current source to the load as the series resonant converter,thus by using the FHA method, we obtained same equations for input voltage (3.2), equivalent resistor (3.5) and output voltage (3.4). The topology and the equivalent circuit of LLC converter are illustrated in fig.3.8.

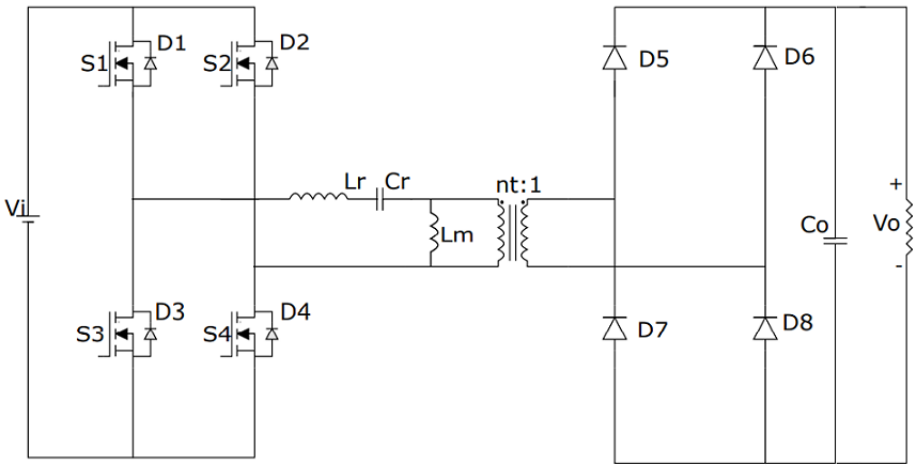

Figure 3.8: LLC Resonant Converter

3.4.2 Voltage Gain

From the equivalent circuit, the voltage gain is given by (3.19).

$$H = \frac{R_e||j\omega_s L_p}{j\omega_s L_r + \frac{1}{j\omega_s C_r} + (R_e||j\omega_s L_p)} \tag{3.19}$$

The following parameters are defined

$$\gamma = \frac{L_r}{L_p} \tag{3.20}$$

$$Q = R_e\sqrt{\frac{L_e}{C_r}} \tag{3.21}$$

where $L_e = L_r + L_p$

$$f_n = \frac{f_s}{f_r} \tag{3.22}$$

where $f_r = \frac{1}{2\pi\sqrt{L_e C_r}}$

The voltage gain can be written as Eqn 3.23. Fig.3.9 shows the schematic of the voltage gain for different values of Q.

$$H = \frac{1}{[1 + \gamma - \frac{1}{f_n^2} + \frac{\gamma}{f_n^2}] + [jQ(\frac{\gamma f_n}{\gamma+1} - \frac{1}{f_n}]} \tag{3.23}$$

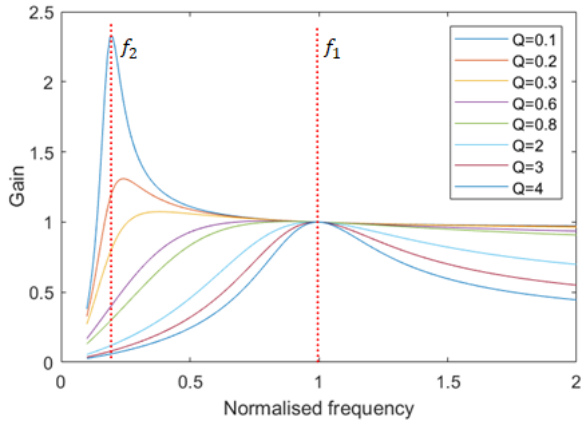

Figure 3.9: Voltage gain of LLC resonant converter

3.4.3 Merits And Demerits

LLC resonant converter has two resonant frequencies f_2, defined by L_r,C_r and L_m and f_1 defined by C_r and L_r. At light loads the voltage peak moves to f_1 and the converter behaves as series

resonant converter, while it behaves as parallel resonant converter in higher loads where the peak moves to f_2.

The main advantage of LLC resonant converter is its capability to reach ZVS for all the load range.

Inductor L_m can be integrated to magnetic core of the transformer.Wide switching frequency variation under large input or output voltage.

Chapter 4

Single Phase DBSRC

The dual-bridge series resonant converter (DBSRC) and standard full-bridge dc/dc series resonant converter(SRC) have some similarities. Besides that DBSRC has some special features due to the active secondary-side bridge, such as the capability of bidirectional power flow.Resonant converters can be operated at higher frequencies due to their advantages of operation [20].Fig.4.1 shows the DBSRC. The inverter and rectifier bridges are connected through a series LC resonant tank and a HF transformer.

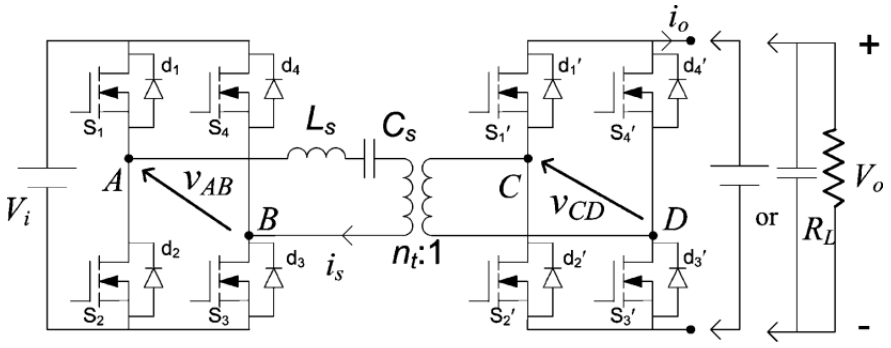

Figure 4.1: Dual Bridge Series Resonant Converter

The circuit symmetry allows it to manage bidirectional power flow. For bidirectional power flow, the output can be another dc source, or a resistive load with a capacitive filter for unidirectional power flow only. A bidirectional dc/dc converter is a two-quadrant converter that uses only ordinary MOSFET or IGBT switches. All of the switches in the two bridges have a 50% duty

cycle, however there is a phase shift between them.The switching frequency is set higher than the LC resonance frequency, thus, the converter works only in continuous current mode. The amount of power transfer is controlled using the phase-shift angle, whereas, the power flow direction is dependent on the polarity of phase shift. Also, only a small variation of the phase shift is needed to regulate the output from full load to almost no load. The HF transformer's leakage inductance is employed as part of the resonant inductance. The resonant tank's series capacitor will also aid in limiting the dc current component emerging from any asymmetry in device drop, etc., preventing the transformer from being saturated. For bidirectional power flow in a real application, Cs can be split into two portions and placed on both sides of the HF transformer (but having the same value of equivalent capacitance as if placed exclusively on the primary side).

4.1 AC equivalent analysis of DBSRC

Two ac equivalent circuit analysis methods are used for dc voltage source load and resistive load with capacitive filter, respectively [21], [22].and resistive load with capacitive filter, respectively [21], [22]. Anyway both methods could be applied for either of the two types of load because the load resistance can be regarded as the equivalent load resistance of a dc voltage source with the designed power at $P_o = V'^2_o/R_L$ where $R'_L = n_t^2(V_o^2/P_o)$ is the primary-side reflected equivalent load resistance.

In ac equivalent circuit analysis or approximate analysis, all harmonics except fundamental component of all voltages and currents are ignored.Switches, diodes, and all other components are assumed to be ideal and lossless. The magnetising inductance of the transformer is considered to be infinite, and the leakage inductance is included in the resonant inductance Ls. The effects of snubbers and dead-gaps used in the gating signals are neglected.All the parameters that have been transferred to primary side,are denoted by using the superscript " ' ".

$$V_B = V_i \qquad Z_B = R'_L \qquad I_B = \frac{V_B}{Z_B} \tag{4.1}$$

where V_i is the input voltage and the converter voltage gain is defined as $M = V'_o/V_i$

The normalized switching frequency is given by

$$F = \frac{f_s}{f_r} \tag{4.2}$$

where $f_r = \frac{1}{2\pi\sqrt{L_s C_s}}$

The normalized values of all reactances are given by

$$X_{L_{s,pu}} = QF \qquad X_{C_{s,pu}} = \frac{-Q}{F} \tag{4.3}$$

$$X_{spu} = Q(F - \frac{1}{F}) \tag{4.4}$$

$$Q = \frac{\omega_r L_s}{R'_L} \tag{4.5}$$

4.1.1 Voltage Source Load

An equivalent circuit is shown in Fig.4.2, using the series (LC) tank circuit separated by fundamental components of two voltage sources v_{AB} and v_{CD} is used for the analysis.$v_{AB,1}$ and $v_{CD,1}$ are the fundamental components of square waves v_{AB} and v_{CD} phase-shifted by an angle ϕ [23]. The normalized fundamental components of v_{AB} and v_{CD} are as follows:

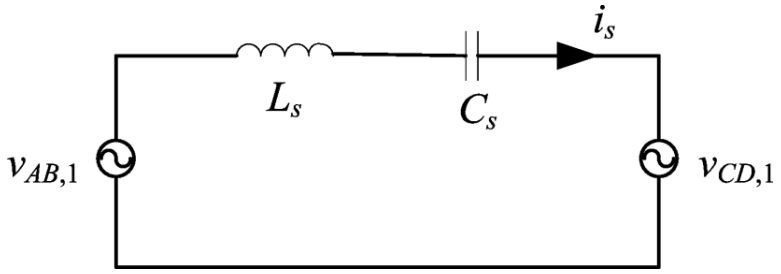

Figure 4.2: Equivalent Circuit for analysis using the fundamental component of voltages v_{AB} and v_{CD}

$$V_{AB,1pu}(t) = \frac{4}{\pi}\sin(\omega_s t) \tag{4.6}$$

$$V'_{CD,1pu}(t) = \frac{4M}{\pi}\sin(\omega_s t - \phi) \tag{4.7}$$

$$i_{spu}(t) = \frac{4}{\pi X_{spu}}(\sin(\omega_s t - 90) - M\sin(\omega_s t - \phi - 90)) \tag{4.8}$$

The transferred power from the primary side to the secondary side could be calculated from either side. Here, the instantaneous power is evaluated from the output side

$$P_{pu}(t) = V_{CD,1pu}(t) * i_{spu}(t) = \frac{16M}{\pi^2 X_{spu}}[\frac{M}{2}(sin2(\omega_s t - \phi) - \cos(\omega_s t)\sin(\omega_s t - \phi)] \tag{4.9}$$

The output active power is the average value of instantaneous power

$$P_{pu} = \frac{8M}{\pi^2 Q(F - \frac{1}{F})}\sin(\phi) \tag{4.10}$$

The above equation can be used to determine the phase-shift angle required to deliver a certain amount of power. It is apparent that the net power flow is positive with $\phi > 0$, while the net power will reverse direction if $\phi < 0$.

4.1.2 Resistive Load

The second modified method is proposed for the case that the output of the DBSRC is a pure resistance with capacitive output filter, Although this is more like the approach proposed for a regular full-bridge resonant converter with capacitive filter [21], [22], in the present case, diode rectifier has been replaced by a controlled rectifier on the secondary side. Therefore, here ac equivalent impedance is derived instead of equivalent ac resistance. Since, the output voltage V_o is constant, the reflected converter input voltage v'_{CD} is a square wave with the amplitude of $\pm V'_o$. Thus, the rms value of fundamental input voltage v'_{CD} can be evaluated as follows:

$$E_o = \frac{4V'_o}{\pi\sqrt{2}} = \frac{\sqrt{8}V'_o}{\pi} \tag{4.11}$$

The resonant input current is is assumed to be near sinusoidal. Due to the active rectifier control, the rectifier current is assumed to lag the voltage by an angle θ. The condition $\theta = 0$ corresponds to the diode rectifier operation. The load current I'_o is the average value of i'_o , which can be obtained by

$$I'_o = \frac{2\sqrt{2}}{\pi} I_{ac}\cos(\theta) \tag{4.12}$$

where I_{ac} is rms value of input current i_s.

Because of the controlled rectifier, output current i_o may go negative in a small portion of each cycle, which means sometime power is fed back to primary side. And, the rectifier output voltage

and current are not always in phase. Thus, it is valid to represent the whole secondary part with an equivalent impedance $Z_{ac} = |Z_{ac}| \angle \theta$ instead of a pure resistance in the case of SRC [21], [22]. Hence, the output power can be expressed as follows:

$$P_o = E_o I_o \cos(\theta) \tag{4.13}$$

The magnitude of equivalent ac impedance is given below.

$$|Z_{ac}| = \frac{8R'_L \cos(\theta)}{\pi^2} \tag{4.14}$$

The converter voltage gain is as follows:

$$M = \frac{8}{\pi^2 Q(F - \frac{1}{F})} \sin(\phi) \tag{4.15}$$

4.2 Design calculations Of DBSRC

The converter is designed for 700V nominal input voltage and 48V nominal output voltage. The input voltage swings between 600V-800V and output swings between 40V-56V. The maximum allowed phase shift between two bridges is 45°. The maximum Power output of converter is 8KW. The transformer turns ratio is taken as 5:1 and leakage inductance of transformer(L_p) is 4μH. Switching and resonant frequencies are taken as 500KHz and 470KHz respectively.

The topology used for DC-AC bridge is half bridge inverter and for AC-DC is full bridge Rectifier.The circuit used for simulation is shown below in fig.4.3

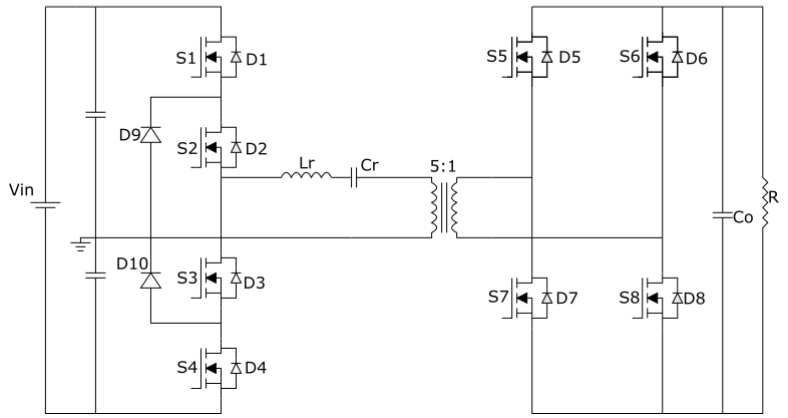

Figure 4.3: Circuit used for simulation

Maximum gain required will be M=0.933 Using Eqn.4.15 Quality factor Q=4.9593

$$L_t = \frac{QR'_l}{\omega_r} = 12.259\mu H \tag{4.16}$$

resonant inductance(L_r) = L_t - L_p = 8.259

$$C_r = \frac{1}{4\pi^2\omega_r^2 L_t} = 9.3538nF \tag{4.17}$$

4.3 Simulation results

The following fig.4.4. shows the output current and voltages of DBSRC and fig.4.5. shows the currents through the resonant tank and input voltage of transformer and output voltage of neutral point clamped inverter. The total harmonic distorsion in the current through resonant tank is shown in fig.4.7

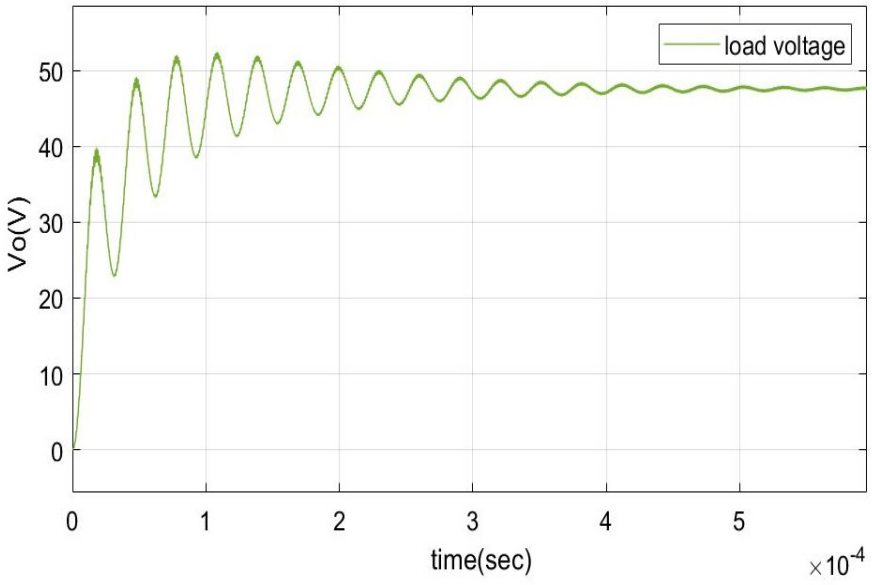

Figure 4.4: Output voltage of DBSRC

The total harmonic distorsion(THD) is appoximately 3.61% with fundamental peak current of 54.93. The input voltage of transformer is high because of the leakage inductance of the transformer.This can be reduced by splitting the resonant capacitance and placing it at the secondary terminal of the transformer.

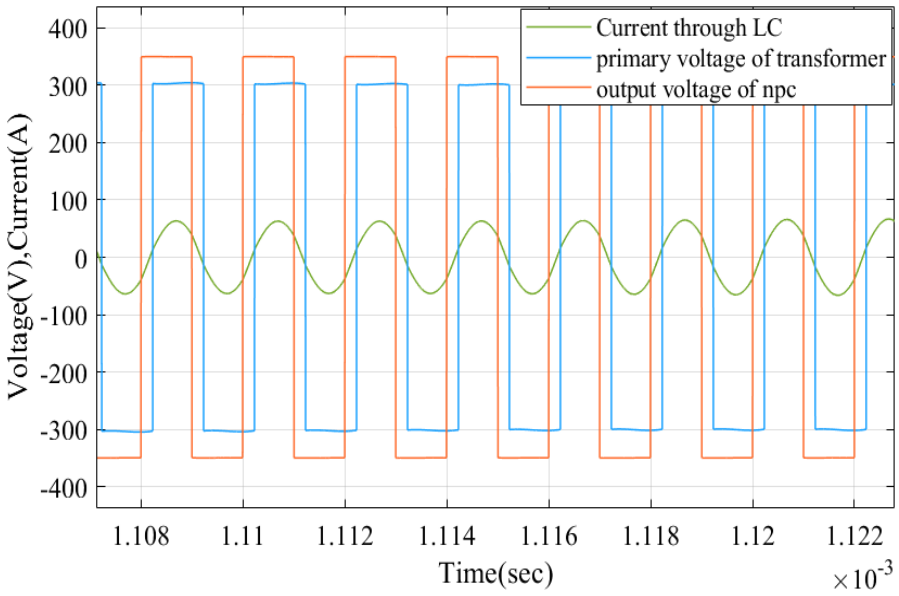

Figure 4.5: Current through resonant tank, output voltage of neutral point converter and primary voltage of transformer.

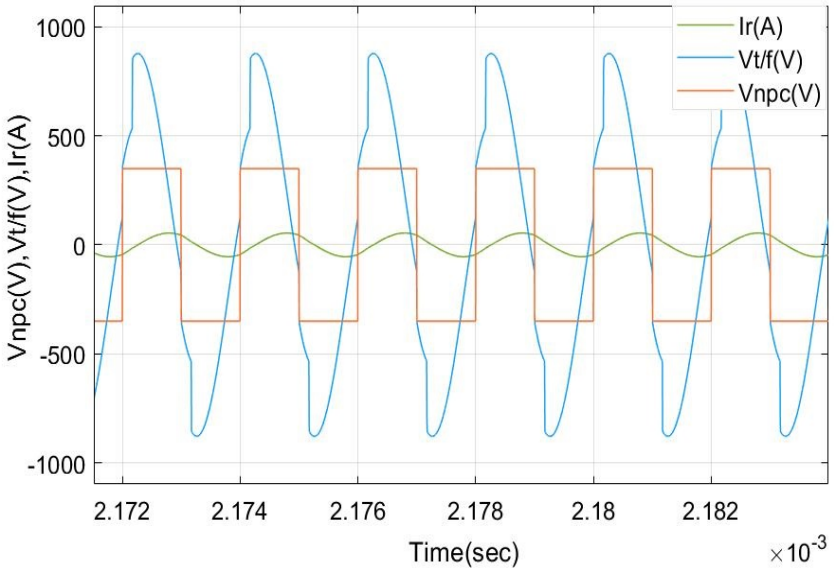

Figure 4.6: Current through resonant tank, output voltage of neutral point converter and primary voltage of transformer with leakage inductance split.

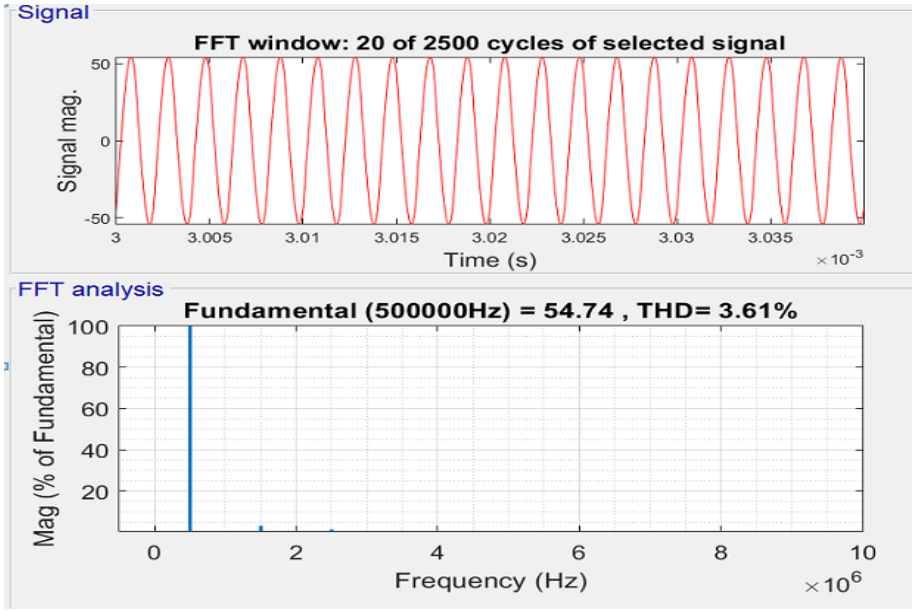

Figure 4.7: FFT analysis of resonant tank current

Chapter 5

Small Signal Modelling of DBSRC

The topology of DBSRC is shown in Fig. 4.1, Compared with the DAB, an additional resonant capacitor C_s is connected in series with the high frequency transformer and inductor. The turns ratio of high frequency transformer is assumed to be 1:N_t. At the normal operation, the switching frequency f_s is set a little higher than the resonant frequency fr to maintain the resonant tank inductive, and the power is transferred due to the phase difference δ between the AC voltage of primary and secondary side V_{ab} and V'_{cd}, where $V'_{cd} = V_{cd}/N_t$ is the secondary AC voltage transferred to primary side. At the steady state, the voltage conversion ratio M is calculated through the ratio between the transferred output DC voltage V'_2 and input DC voltage V1, namely M = V'_2 / V_1. According to the different the different value of M, DBSRC contains three working modes and the mode II, where M is close to 1, is the most popular mode, due to the lower current stress and circulating power. The waveforms at mode II are shown in Fig. 2, where V_{LC} is the sum of resonant capacitor and inductor voltage. Through solving two second-order differential equations, the key resonant current ip, namely the AC current of primary side, can be derived as Eqn.5.1, where $i_p(0)$, $i_p(\delta)$, $v_c(0)$ and $v_c(\delta)$ are the resonant current and capacitor voltage at the beginning and end of phase-shift angle, respectively The current through the inductor and voltage across the series capacitor are given by the following equations.

$$i_p(\omega_s t) = \begin{cases} (-1)^k[i_p(0)cos(\frac{\omega_s t - k\pi}{F}) + \frac{V_1 + V_2' - v_c(0)}{Z_r} sin(\frac{\omega_s t - k\pi}{F})] & ,\omega_s t \in [k\pi, k\pi + \delta] \\ (-1)^k[i_p(\delta)cos(\frac{\omega_s t - \delta - k\pi}{F}) + \frac{V_1 - V_2' - v_c(\delta)}{Z_r} sin(\frac{\omega_s t - \delta - k\pi}{F})] & ,\omega_s t \in [k\pi + \delta, (k+1)\delta] \end{cases} \tag{5.1}$$

where

$$i_p(0) = \frac{V_1}{Z_r}[Msin(\frac{\delta}{F}) + (1 - Mcos(\frac{\delta}{F}))tan(\frac{\pi}{2F})] \tag{5.2}$$

$$i_p(\delta) = \frac{V_1}{Z_r}[sin(\frac{\delta}{F}) + (M - cos(\frac{\delta}{F}))tan(\frac{\pi}{2F})] \tag{5.3}$$

$$v_c(0) = -2V_1 Msec(\frac{\pi}{2F})sin(\frac{\pi - \delta}{2F})sin(\frac{\delta}{2F}) \tag{5.4}$$

$$v_c(\delta) = -2V_1 sec(\frac{\pi}{2F})sin(\frac{\pi - \delta}{2F})sin(\frac{\delta}{2F}) \tag{5.5}$$

$$F = \frac{f_s}{f_r} \tag{5.6}$$

$$Z_r = \sqrt{\frac{L_s}{C_s}} \tag{5.7}$$

The small signal model is formed based on the Fig. 4.1, where the inner impedance of power switches and high frequency transformer are ignored. Taking the resonant current i_p, the resonant capacitor voltage $v_c$and the output voltage v_2 as the state variable, and a third-order state space equation is formed as given below.

$$\begin{bmatrix} \frac{di_p}{dt} \\ \frac{dv_c}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_s} & \frac{1}{L_s N_t} \\ \frac{1}{C_s} & 0 & 0 \\ \frac{-1}{C_s N_t} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_p \\ v_c \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_r} \\ 0 \\ 0 \end{bmatrix} v_1 \quad ,\text{t} \in [0, \frac{\delta}{\pi} T_s] \tag{5.8}$$

$$\begin{bmatrix} \frac{di_p}{dt} \\ \frac{dv_c}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_s} & \frac{-1}{L_s N_t} \\ \frac{1}{C_s} & 0 & 0 \\ \frac{1}{C_s N_t} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_p \\ v_c \\ v_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_r} \\ 0 \\ 0 \end{bmatrix} v_1 \quad ,\mathrm{t} \in [\tfrac{\delta}{\pi} T_s, T_s] \tag{5.9}$$

where Ts is half of the switching period. Due to the periodically symmetry of waveforms, only the states in the half period are considered.

Since the average value of i_p and v_c in a switching cycle are 0,the normal switching cycle average modeling cannot work at this situation.The order of above state space equations are reduced before applying the switching cycle averaging. Considering that the perturbation frequency of input and output voltage v1 and v2 is far smaller than the switching frequency, the system can be divided into a slow variable system and a fast-variable system. For the slow variable system, the fast variable i_p and v_c should be eliminated. By substituting Eqn 5.1 in Eqn 5.9 and 5.10, the state space equations are changed to one-dimension as 5.11.

$$C_2 \frac{dv_2}{dt} = \begin{cases} -\frac{i_p(0)}{N_t} cos(\frac{\omega_s t}{F}) + \frac{V_1 + V_2/N_t - v_c(0)}{Z_r N_t} sin(\frac{\omega_s t}{F}) - \frac{V_2}{R} & ,\mathrm{t} \in [0, \frac{\delta}{\pi} T_s] \\ \frac{i_p(\delta)}{N_t} cos(\frac{\omega_s t - \delta}{F}) + \frac{V_1 - V_2/N_t - v_c(\delta)}{Z_r N_t} sin(\frac{\omega_s t - \delta}{F}) - \frac{V_2}{R} & ,\mathrm{t} \in [\frac{\delta}{\pi} T_s, T_s] \end{cases} \tag{5.10}$$

Apply averaging on Eqn 5.11 through the operator $\langle x(t) \rangle = \frac{1}{2T_s} \int_t^{t+2T_s} x(\tau)\, d\tau$ the large signal model can be obtained as the following equation.

$$C_2 \frac{d \langle v_2 \rangle}{dt} = \frac{2F \langle v_1 \rangle}{\pi Z_\mathrm{r} N_\mathrm{t}} \left(-1 + \cos \frac{\delta}{F} + \sin \frac{\delta}{F} \tan \frac{\pi}{2F} \right) - \frac{\langle v_2 \rangle}{R} \tag{5.11}$$

A small perturbation is added on the variables

$$\langle v_1 \rangle = V_1 + \hat{v}_1, \langle v_2 \rangle = V_2 + \hat{v}_2, \quad \delta = \Delta + \hat{\delta} \tag{5.12}$$

Assume that the perturbation is much small, so that the trigonometric function of δ can adopt the following approximation.

$$\sin \hat{\delta} = 0, \cos \hat{\delta} = 1 \tag{5.13}$$

Substitute Eqn 5.13 and 5.14 to 5.12 and linearize the variable, and the steady state model and small signal model of DBSRC can be obtained as follows.

$$\frac{V_2}{R} = \frac{2FV_1}{\pi Z_r N_t}\left(-1 + \cos\frac{\Delta}{F} + \sin\frac{\Delta}{F}\tan\frac{\pi}{2F}\right) \tag{5.14}$$

$$\begin{aligned}\frac{d\hat{v}_2}{dt} =& \frac{2F\cdot\hat{v}_1}{\pi Z_r C_2 N_t}\left(-1 + \cos\frac{\Delta}{F} + \sin\frac{\Delta}{F}\tan\frac{\pi}{2F}\right) \\ &+ \frac{2V_1\cdot\hat{\delta}}{\pi Z_r C_2 N_t}\left(\cos\frac{\Delta}{F}\tan\frac{\pi}{2F} - \sin\frac{\Delta}{F}\right) - \frac{\hat{v}_2}{C_2 R}\end{aligned} \tag{5.15}$$

The transfer function from phase-shift angle to output voltage (control-to-output) is

$$\left.\frac{\hat{v}_2}{\hat{\delta}}\right|_{\hat{v}_1=0} = \frac{2V_1 R}{\pi Z_r(1+sC_2R)N_t}\left(\cos\frac{\Delta}{F}\tan\frac{\pi}{2F} - \sin\frac{\Delta}{F}\right) \tag{5.16}$$

The control to utput transfer function is for the circuit is gievn is Eqn 5.17

$$\frac{\hat{v}_2}{\hat{\delta}} = \frac{78.44}{2.8 * 10^{-5}s + 1} \tag{5.14}$$

The bode plot for the above transfer function is shown below in figure 5.1. From the figure it is clear that the converter is very stable and has a gain margin and phase margin of infinite and 90° respectively.

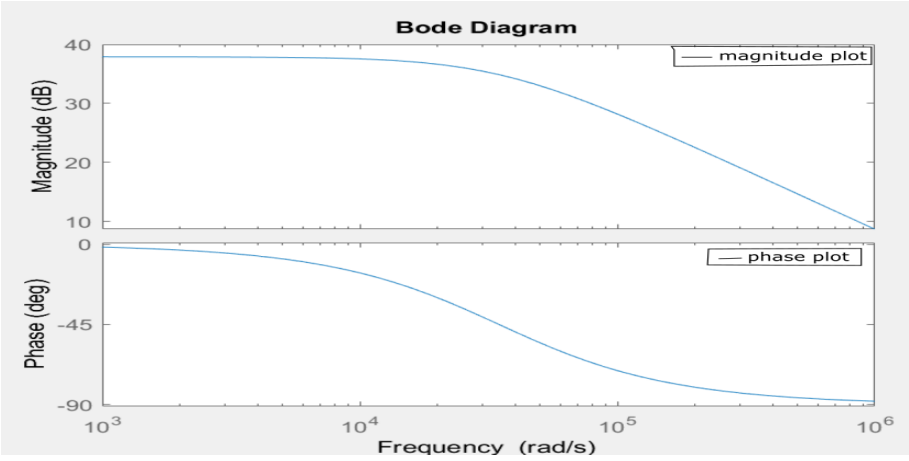

Figure 5.1: Bode plot for control to output transfer function.

A PI controller is designed to adjust phase margin as 60° and bandwidth to 200kHz. The k_p and k_i values are obtained using control system toolbox by adjusting phase margin to 60° as

bandwidth to 200kHz as 0.0452 and 6652.7 respectively .The bode plot for the closed loop control system is shown in figure 5.2.

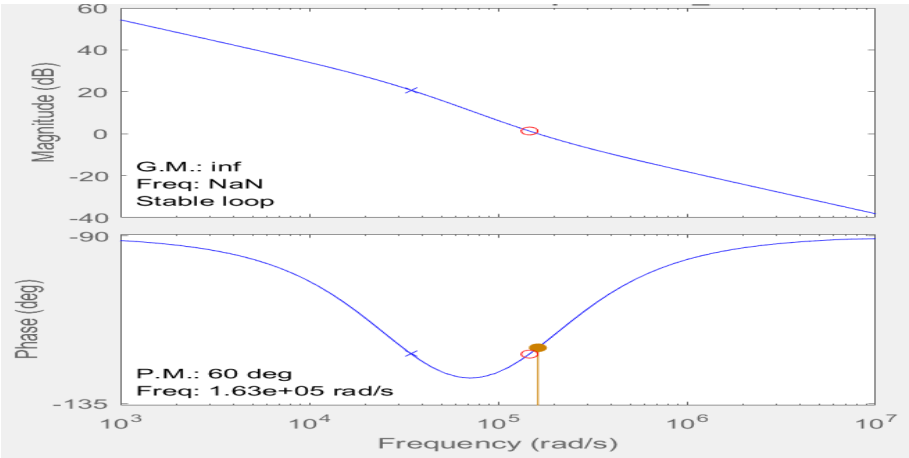

Figure 5.2: Bode plot for closed loop transfer function.

Chapter 6

Triple Phase Shift control to minimise circulating energy

Single Phase Shift (SPS) is a commonly used control technology because has the advantages of a simple controller, easy implementation, and controllable phase shift angle. However, when the voltage gain and load level change, the circulating energy will increase and its efficiency will decrease. The Extended Phase Shift Control (EPS) is an upgraded version with a one more controllable phase shift angle. Compared with SPS control, EPS control can reduce circulating energy and extend smooth switching range. However, when the direction of the power flow changes, the working modes of the two bridges must be interchanged with the to reduce the circulating power. Dual Phase Shift Control (DPS) is easier to implement than EPS control because the internal phase shift angles of the two bridges are equal. Through DPS control, the dynamic performance of the converter can be improved. However, in some operating areas, the efficiency improvement is not significant.Triple phase shift (TPS) is an integrated form of phase shift control, and SPS, DPS, and EPS are also sometimes considered special cases of TPS control. TPS control is complex but most flexible control scheme to control load voltage as well as circulating energy. The typical working waveform under tps control and the required waveform are shown in Figure 6.1 and 6.2 [24].

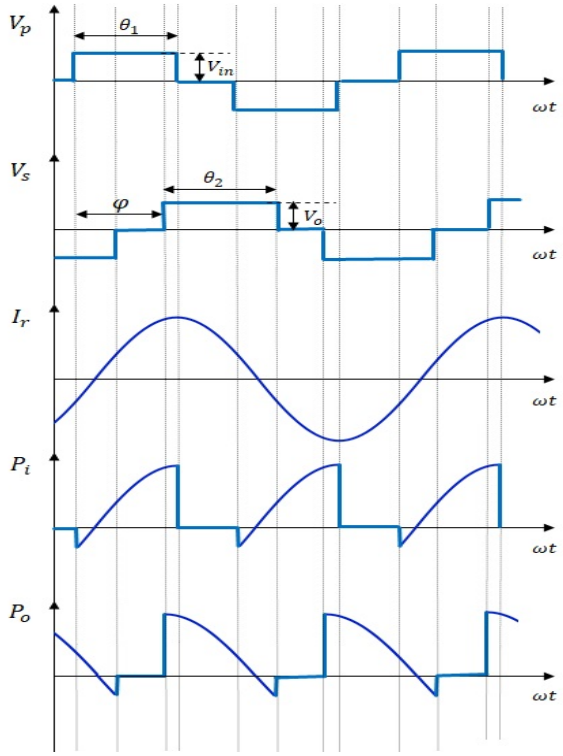

Figure 6.1: Typical operating waveforms of the DBSRC under conventional TPS control

6.1 Steady-state analysis of DBSRC with TPS control

When the switching frequency is close to the resonant frequency, FHA analysis is adopted for the steady state analysis with simplified calculation and acceptable accuracy. The obtained equations can be used for a quick initial converter design with enough accuracy. All parameters have been reflected to the secondary side in the fig 4.1. (denoted by a superscript " ' ",if the parameter is on the primary side). In order to obtain normalized equations, the following base values are chosen:

$$V_B = nV_{in};\ Z_B = \frac{V_o^2}{P_R};\ I_B = \frac{V_B}{Z_B}; \tag{6.1}$$

$$f_B = f_r = \frac{1}{2\pi\sqrt{L_k C_k}};\ P_B = \frac{V_B^2}{Z_B} \tag{6.2}$$

where f_r is the series resonance frequency, P_r is the rated output power.

In Fig.6.3, the fundamental equivalent circuit of DBSRC is given. The normalized two voltage sources of $v'_{p,1}$ and $v_{s,1}$ in time domain with only fundamental components can be expressed as:

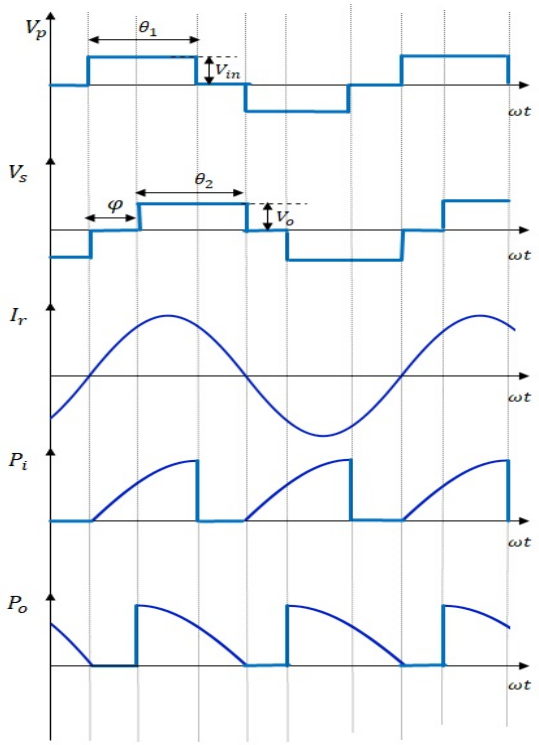

Figure 6.2: Typical operating waveforms of the DBSRC to eliminate circulating energy

$$v'_{p,1pu}(\omega_s t) = \frac{4}{\pi} \sin\frac{\theta_1}{2} \sin(\omega_s t) \tag{6.3}$$

$$v_{s,1pu}(\omega_s t) = \frac{4M}{\pi} \sin\frac{\theta_2}{2} \sin\left[\omega_s t - \left(\varphi + \frac{\theta_2 - \theta_1}{2}\right)\right] \tag{6.4}$$

where the converter gain M is defined as $M = \frac{n_t V_o}{V_{in}}$, ω_s is the switching angular frequency. It is seen from Eqn 6.3. that the fundamental component of v'_p leads that of v_s with a phase-shift angle of $\varphi + \frac{\theta_2 - \theta_1}{2}$.

The normalized impedance of the resonant tank can be written as:

$$X_{s,pu} = \left(\omega_s L_k - \frac{1}{\omega_s C_k}\right) / Z_B = Q(F - 1/F) \tag{6.5}$$

where rated load quality factor Q is defined as $Q = \frac{\omega_r L_k}{Z_B} = \frac{1}{\omega_r C_k Z_B}$, the normalized switching frequency F can be expressed as $F = \frac{\omega_s}{\omega_r}$, and ω_r is the resonant angular frequency.

Then the normalized resonant tank current $i_{LC,pu}$ in time domain with only fundamental component can be found as:

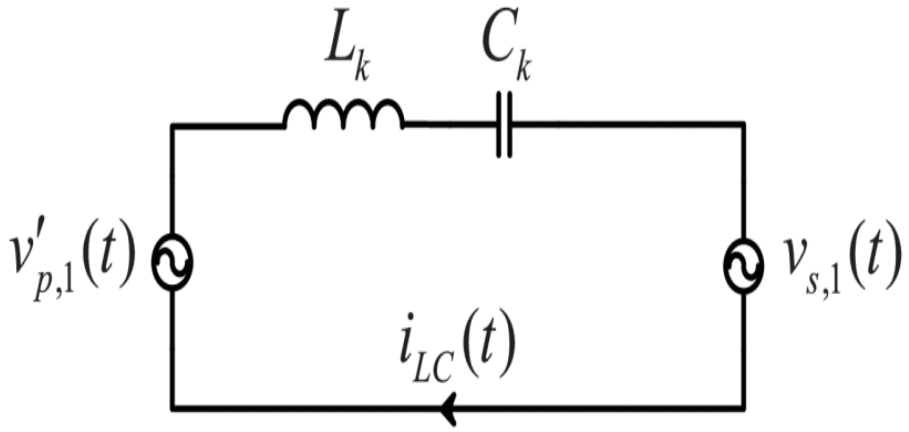

Figure 6.3: Equivalent circuit for fundamental components in time domain.

$$i_{LC,pu}(\omega_s t) = \frac{4\left[M \sin\frac{\theta_2}{2} \cos\left(\omega_s t - \left(\varphi + \frac{\theta_2 - \theta_1}{2}\right)\right) - \sin\frac{\theta_1}{2} \cos(\omega_s t)\right]}{\pi X_{s,pu}} \tag{6.6}$$

By using Eqn 6.6., the normalized root-mean-square (rms) current $I_{LCr,pu}$ is given as:

$$I_{LCr,pu} = \frac{\sqrt{8}\sqrt{M^2 \sin^2\frac{\theta_2}{2} - 2M \sin\frac{\theta_1}{2} \sin\frac{\theta_2}{2} \cos\left(\varphi + \frac{\theta_2 - \theta_1}{2}\right) + \sin^2\frac{\theta_1}{2}}}{\pi X_{s,pu}} \tag{6.7}$$

Ignoring the circuit loss, the normalized average transferred power with TPS control in a switching cycle can be evaluated from either side of the converter, which can be calculated as:

$$P_{o,pu} = \frac{1}{2\pi} \int_0^{2\pi} v'_{p,1pu}(\omega_s t) i_{LC,pu}(\omega_s t) d\omega_s t = \frac{8M}{\pi^2 X_{s,pu}} \sin\frac{\theta_1}{2} \sin\frac{\theta_2}{2} \sin\left(\varphi + \frac{\theta_2 - \theta_1}{2}\right) \tag{6.8}$$

By using Eqn 6.1 and 6.2, the normalized power can also be defined as:

$$P_{o,pu} = \frac{P_o}{P_B} = \frac{P_o}{P_R} \frac{V_o^2}{(nV_{in})^2} = M^2 G \tag{6.9}$$

where P_o is the actual output power, and $G \in [0, 1]$ is the percentage of the power level index at certain voltage gain, which is defined as:

$$G = \frac{P_o}{P_R} = \frac{P_{o,pu}}{M^2} \tag{6.10}$$

Substituting Eqn 6.8 into 6.10, the voltage gain can also be defined as:

$$M = \frac{8}{\pi^2 G X_{s,pu}} \sin\frac{\theta_1}{2} \sin\frac{\theta_2}{2} \sin\left(\varphi + \frac{\theta_2 - \theta_1}{2}\right) \tag{6.11}$$

Equation 6.11. shows the relationship between the power level index and the voltage gain in a DBSRC under TPS modulation. The control phase-shift θ_1 , θ_2 and φ shall be adjusted dynamically with the changes of G and M to keep the balance in Eqn 6.11.

6.2 Determining θ_1 , θ_2 for reducing Circulating energy

The obtained equations Eqn 6.1-6.8 are suitable for unified boundary TPS control with certain boundary conditions. The constraints can be derived as follows.To completely eliminate secondary side circulating energy, the falling edge of v_s (turn-on moments of S_1' and S_2') should move left and finally align with the zero crossing point of resonant tank current i_{LC} as shown in Fig. 4. Since the resonant tank current i_{LC} is a sinusoidal waveform, the first boundary condition of the two angles can be easily written as

$$\pi = \varphi + \theta_2 \tag{6.12}$$

To completely eliminate primary side circulating energy, the rising edge of v_p (turn-on moments of S_1 and S_2) should move right and eventually align with the zero crossing point of resonant tank current i_{LC} as shown in Fig. 4. By using (5), the zero circulating energy condition can be expressed as

$$i_{LC,pu}\left(\frac{\pi - \theta_1}{2}\right) = \frac{4\left[-\sin^2\frac{\theta_1}{2} + M\sin\frac{\theta_2}{2}\sin\left(\varphi + \frac{\theta_2}{2}\right)\right]}{\pi X_{s,pu}} = 0 \tag{6.13}$$

With the help of Eqn 6.12, the secondary boundary condition Eqn 6.13 can be simplified as

$$\sin\frac{\theta_1}{2} = \sqrt{M}\sin\frac{\theta_2}{2} \tag{6.14}$$

Based on the above analysis, the output power can be controlled solely by the external phase-shift φ under the unified boundary TPS control. The other two phase-shift angles (θ_1 and θ_2)

can be represented by φ from Eqn 6.12 and 6.14. Substituting Eqn 6.12 and 6.14 into 6.8, the normalized output power under unified boundary TPS control can be rewritten as

$$P_{o,pu} = \frac{8M^{\frac{3}{2}}}{\pi^2 X_{s,pu}} \cos^2\frac{\varphi}{2} \cos\left[\arcsin\left(\sqrt{M}\cos\frac{\varphi}{2}\right) - \frac{\varphi}{2}\right] \tag{6.15}$$

6.3 Simulation results with closed loop Control

The switching combination for obtaining different levels of voltages at output of neutral point clamped inverter and input of secondary side rectifier for the DBSRC shown in figure 4.3 is given in the table 6.1. and 6.2 respectively.

Table 6.1: Switching combinations for Half bridge NPC Inverter

S1	S2	S3	S4	V_o
1	1	0	0	$+V_{in}/2$
0	1	1	0	0
0	0	1	1	$-V_{in}/2$

Table 6.2: Switching combinations for rectifier

S5	S6	S7	S8	V_o
1	0	0	1	$+V_o/2$
1	1	0	0	0
0	0	1	1	0
0	1	1	0	$-V_o/2$

The output voltage of the DBSRC and Reference voltage is plotted in figure 6.4. The ripple in the steady state output voltage is around 0.4v and is plotted in figure 6.5.

Figure 6.6 shows the instantaneous power flowing through the resonant link and it clearly shows circulating power is zero.

Figure 6.7 shows the output voltage of the inverter,current through the resonant tank and input voltage of the transformer. The current through switch s1 and current through the clamping diodes

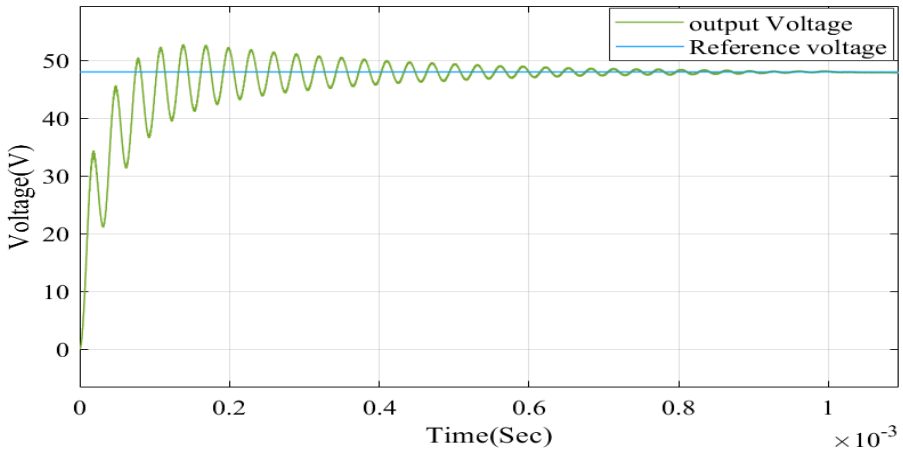

Figure 6.4: Output voltage and reference voltage of DBSRC

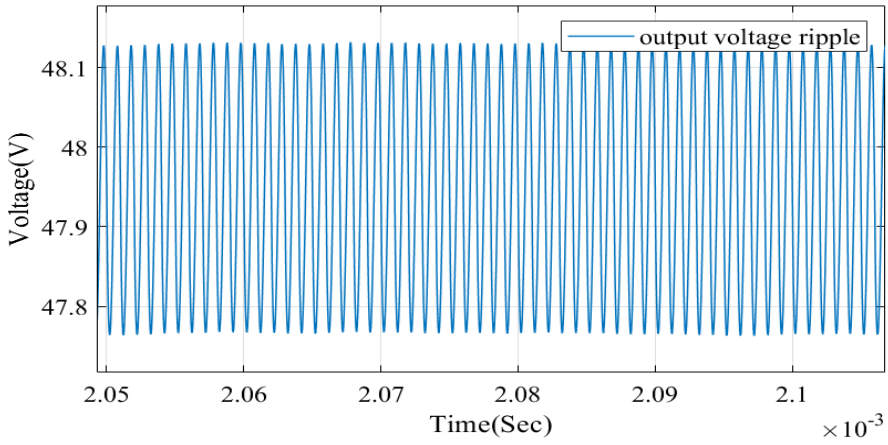

Figure 6.5: Ripple in output voltage.

is shown in figure 6.8 and the the voltage across the switches in the inverter is shown in figure 6.9

when output voltage across the nuetral point clamped inverter is zero one of the clamping diode is turned on depending upon the direction of current in the resonant link. During this time both switches s2 and s3 are turned on.The nuetral point clamped inverter provides the advantage in peak reverse voltage as it is only half compared to full bridge inverter.

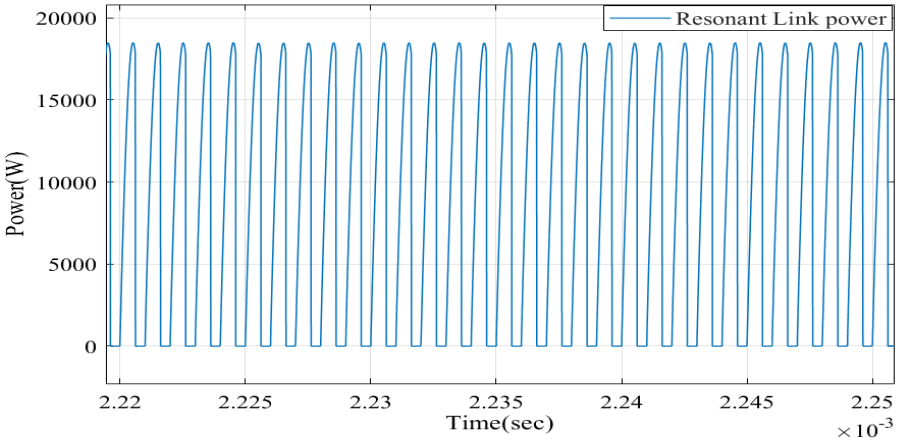

Figure 6.6: Resonant Link Power

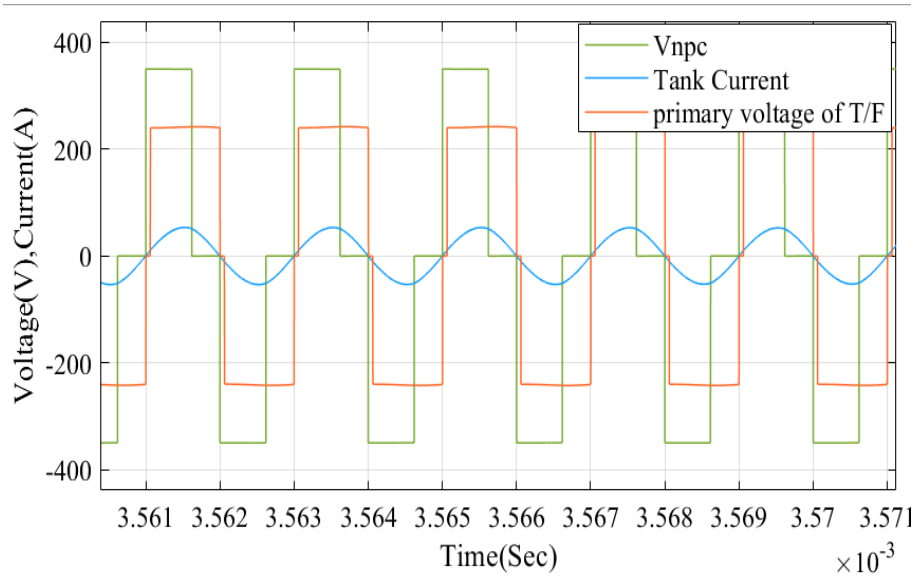

Figure 6.7: Ouput voltage of inverter,current through resonant link and input voltage of transformer

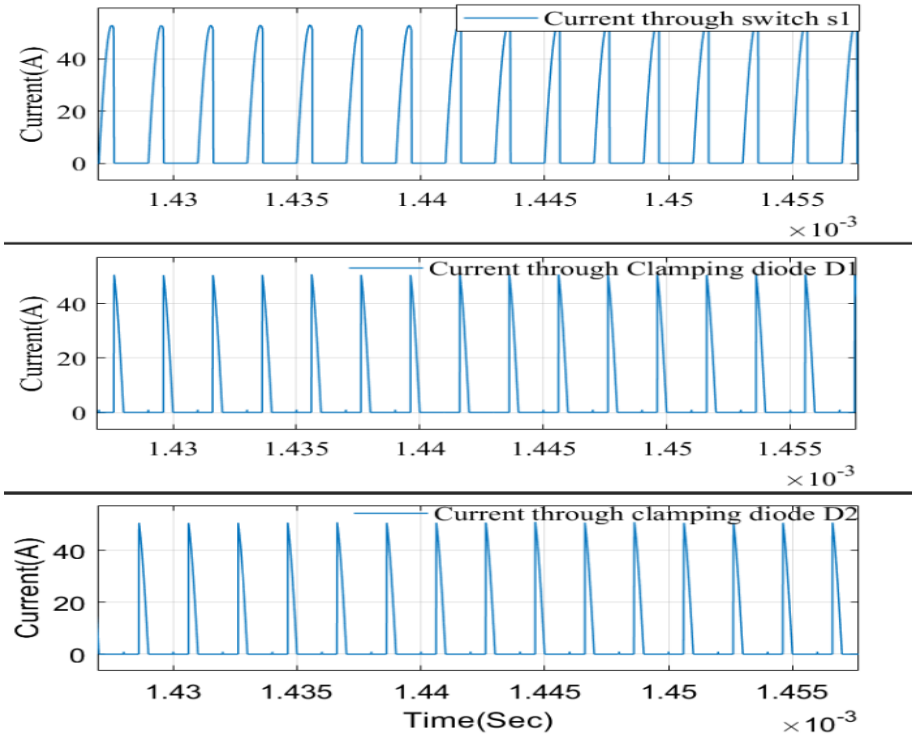

Figure 6.8: Current through switches and diodes

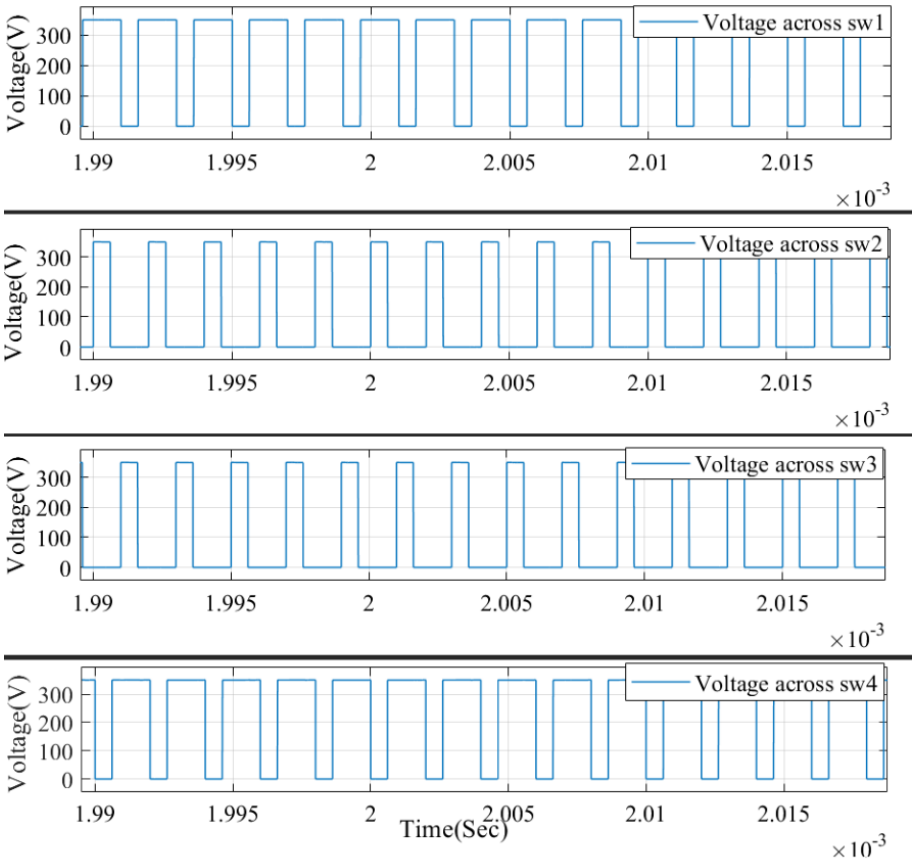

Figure 6.9: Voltages across the switches of inverter

6.4 Conclusions

In this report a detailed study of different types of resonant links and the gains associated with respective resonant links are analysed.A proper analysis of the dual active series resonant converter has been done and a closed loop control method is implemented by using small signal modelling technique to maintain desired output voltage by controlling the phase shift between the input side and output side bridges.Further the circulating energy in the resonant link is reduced by implementing dead times in both the bridges.

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