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Snubber less Series Connection of Silicon Carbide MOSFET using Active Gate Driver

A Thesis

Submitted by

SARAVANAN D

For the award of the degree

Of

MASTER OF SCIENCE

(by Research)

March 2023

THESIS CERTIFICATE

This is to undertake that the Thesis titled **SNUBBER LESS SERIES CONNECTION OF SILICON CARBIDE MOSFET USING ACTIVE GATE DRIVER**, submitted by me to the Indian Institute of Technology Madras, for the award of M.S. is a bona fide record of the research work done by me under the supervision of Dr. Kamalesh Hatua. The contents of this Thesis (or Project report), in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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LIST OF PUBLICATIONS

I. PUBLICATIONS IN CONFERENCE PROCEEDINGS

1. D. Saravanan, V. K. Miryala and K. Hatua "Adaptive Digital Technique Assisted Hard Switching Fault Detection for SiC MOSFETs," *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, Wuhan, China, 2021, pp. 338-343, doi: 10.1109/WiPDAAsia51810.2021.9656023

2. S. S. Chakraborty, D. Saravanan, S. Bhawal and K. Hatua "Design of an Isolated Gate Driver for Medium Voltage Cascaded H-Bridge (CHB) Based Solid State Transformer (SST)," *2022 IEEE Global Conference on Computing, Power and Communication Technologies (GlobConPT)*, New Delhi, India, 2022, pp. 1-6, doi: 10.1109/GlobConPT57482.2022.9938157

3. S, S. S., K. Ghosh, D. Saravanan, K. Hatua, and A. Mitra "A compact sic power module gate driver for high-voltage ev application with spi initialization, fault monitoring and diagnostics," *2022 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, (Accepted not published)

4. Ghosh, K., S. S. S, D. Saravanan, K. Hatua, and A. Mitra "Design of a parasitic inductance based shoot-through protection scheme for sic mosfet gate driver," *2022 IEEE Industrial Electronics Society Annual On-Line Conference (ONCON)*, (Accepted not published)

II. PUBLICATIONS IN JOURNAL PROCEEDINGS

1. V. K. Miryala, S. Dhanasekaran, P. Ganesan, K. Hatua and S. Bhattacharya "Active Gate Driving Technique for Series Connecting SiC MOSFETs in the Presence of Gate Pulse Delay Mismatch" *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12402-12413, Dec. 2022, doi: 10.1109/TIE.2021.3128907.

ACKNOWLEDGEMENTS

I want to thank my research advisor, Dr. Kamalesh Hatua, for all his assistance and guidance. It would not have been easy to complete the research project I was working on without his insights, knowledge, and experience. He has given me enormous independence and the ability to concentrate on my research. I will be eternally grateful to him for his guidance concerning my academic and professional goals. I will try to incorporate myself with his level of kindness.

I want to express my deepest gratitude to Professors Mahesh Kumar Mishra, Shanti Swarup, and G.L. Samuel for reviewing the results of my research project and providing me with helpful feedback in their capacities as members of the General Test Committee (GTC). Professor Nagendra Krishnapura's class on analog circuits provided the foundation for my work, so I would like to express my appreciation.

A debt of gratitude is owed to M/S CDAC-Thiruvananthapuram for the helpful support they provided during the creation of the hardware configuration. I want to extend sincere gratitude to Mr. Ganesan P, who works in the Power Electronics Group at CDAC, for all the technical assistance and direction he and his team have provided.

I want to express my gratitude to Mr. Veera Balaji, Mr. Kothandaraman K, and Mrs. Jayasutha Avudai Thangam R of the Power Electronics and Drives Laboratory for their assistance in the creation of the experimental test equipment.

I want to express my gratitude, particularly to Vamshi and yash. Conversations with both of them helped me gain extremely helpful insights that paved the road for me. I am grateful to my other lab mates, Shekhar Bawal, Shivam Chakraborty, Surja Sekhar Chakraborty, Himanshu Patel, Vibhav Pandey, Sakthi, Sandeep, Hari, Ajay, Kunal, Koushik, Sougata, Pradeep, and everyone else who contributed to my research work. During the time that I have spent at the institute, the people who are a part of the Power Electronics and Drives group have significantly impacted my personal and professional lives.

In conclusion, I would want to express my gratitude to my parents and the other members of my family who have consistently shown their support for me during this time.

ABSTRACT

SiC MOSFETs are fast replacing Si IGBTs due to their superior performance in terms of higher voltage blocking, lower on state resistance, higher thermal conductivity, and higher switching frequency of operation. Commercially available SiC MOSFETs have voltage blocking capabilities ranging from 650V to 1.7kV. One of the most cost effective and efficient ways to take advantage of SiC MOSFETs in MV applications is to connect them in series. Unfortunately, SiC MOSFETs are difficult to connect in series due to the manufacturing process variations, mismatches in the applied input gate control signal, and parasitics in the converter layout. Active Gate Driver based control is one of the solutions that may be utilized to overcome the series connection issue. The current study proposes a simplified switching analysis to understand the problems related to the series connection. The gate current control based Active Gate Driver is used to fully control the transients of series connected devices during turn on and turn off time to achieve minimal voltage imbalance. A closed loop control is also implemented for voltage balancing under varying load current conditions. A new voltage balancing control approach for SiC MOSFET body diodes in a series connected string is also proposed. The proposed control mechanism is examined in Double Pulse Test (DPT) setup with two devices connected in series at 1.2kV dc bus voltage. The experiment is extended to include chopper mode, buck converter mode, and half bridge inverter mode for two devices at 1.2kV dc bus and three devices at 2.1kV dc bus using 1.2kV SiC MOSFETs.

The conventional desaturation protection approach includes a fixed blanking time delay, which introduces uncertainty in device protection. An adaptive blanking time technique for detecting Hard Switched Fault(HSF) is proposed. The proposed method uses only device voltage sensing to detect the HSF status. In contrast to the traditional desaturation technique, which uses a fixed blanking time, the proposed method varies the blanking time during each switching cycle. This ensures faster detection of the

shoot-through event and a reduction in peak fault current. The developed protection method is tested in a Double Pulse Test(DPT) setup.

KEYWORDS: Series connection, Active Gate Driver, Voltage balancing.

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ABBREVIATIONS

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
AGD	Active Gate Driver
CGD	Conventional Gate Driver
DUT	Device Under Test
FPGA	Field Programmable Gate Array
SiC	Silicon Carbide

NOTATION

C_{gs}	Gate to Source capacitance
C_{gd}	Gate to Drain capacitance
C_{ds}	Drain to Source capacitance
C_{iss}	Device input capacitance
C_{oss}	Device output capacitance
$\frac{dv}{dt}$	Device voltage slew rate
$\frac{di}{dt}$	Device current slew rate
C_p	Parasitic capacitance
L_p	Parasitic inductance
I_L	Load current
i_d	Device current
i_{ch}	Channel current
g_m	Transconductance of MOSFET
V_{th}	Device threshold voltage
v_{gs}	Gate to Source voltage
v_{gd}	Gate to Drain voltage
v_{ds}	Drain to Source voltage
V_{dc}	DC bus voltage

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

SiC MOSFETs are suitable for high power density converters operating from 650V to 1.7kV. Their performance is superior to Si devices in terms of the higher switching frequency of operation, lower loss, and higher thermal conductivity. Due to growing consumer demands, SiC MOSFETs price is decreasing. The power density of medium voltage converters (ranging from 1kV to 35kV) can be significantly improved by extending SiC technology to these converters. However, SiC MOSFETs with ratings greater than 1.7kV are not commercially available. Few manufacturers offer 3.3kV SiC MOSFETs, but these devices are much more expensive than Si IGBTs. Several low voltage SiC MOSFETs can be connected in series to achieve higher voltage blocking capability to meet the pressing requirements of medium voltage applications.

Currently, for MV applications Si IGBTs are generally preferred. However, the IGBTs have a maximum voltage blocking capability of 6.5 kV. The switching loss and on-state voltage drop are inherent trade-offs that impede the development of Si IGBTs for higher voltage ratings. Consequently, Medium Voltage Si IGBTs are often restricted to switching frequency lower than 800 Hz. They may not be the optimal solution for new applications in which a higher switching frequency of operation is preferred. These constraints can be greatly reduced by using SiC MOSFETs.

The higher cost due to low production volume is a barrier to their widespread use. It is possible to realize a high voltage switch for medium voltage applications by connecting several low voltage SiC MOSFETs in series. This method is less expensive and more efficient than using a single high voltage switch of comparable rating. However, connecting many devices in series presents several challenges that need to be addressed before they can be used in medium voltage applications. One of the difficult challenges in series connection is to ensure that the voltage is properly balanced in both transient and steady state conditions. Several voltage balancing techniques have

been proposed for series connected Si IGBTs. However, these techniques cannot be directly applied to SiC MOSFETs due to their faster switching speed. This chapter discusses the review of existing techniques for series connecting SiC MOSFETs, which lay the foundation for the proposed active control technique for series connecting SiC MOSFETs. An overview of the proposed active gate control will be discussed in this chapter. The short circuit withstanding time of SiC MOSFET is lesser than the Si devices. As the short circuit withstanding time is lesser, a faster detection circuit is required to detect the short circuit event. An adaptive blanking time-based short circuit detection technique is also proposed in this thesis.

1.2 REVIEW OF SERIES CONNECTION TECHNIQUES

Series connection techniques can be broadly classified into four groups. Passive snubber approach, voltage clamping method, gate pulse delay time control, and active gate control. In the passive snubber approach, the individual gate driver and the passive components like resistor, capacitor, and diode across the device [1], [2]. The passive snubber technique obtains good dynamic voltage balancing but at the price of longer turn off time, and higher turn off loss in the capacitor [3]- [6]. The snubber capacitor current is larger in magnitude, and stored energy during turn off time is dumped back into the power device during turn on time. The device loss increases proportionally as the switching frequency increases. A single gate driver connected to the bottom most device is used to drive the series connected devices with passive components connected to all other series connected devices gate terminal [7], [8]. [9] proposes a series parallel approach based single external gate driver for series connecting SiC MOSFETs with passive components. The above mentioned passive snubber approach increases the cost and size of the solution. Furthermore, due to a significant increase in loss, a higher switching frequency of operation is not possible. Fig.1.1 shows typical RCD snubber technique for series connected IGBTs for DC breaker application. The snubber based solution for power conversion will drastically increases the size and cost of the solution.

In the voltage clamping method, the voltage across the devices is clamped to a predefined voltage through closed loop control. Active voltage control is a popular technique for series connection of Si-IGBTs. To control the device voltage, a high

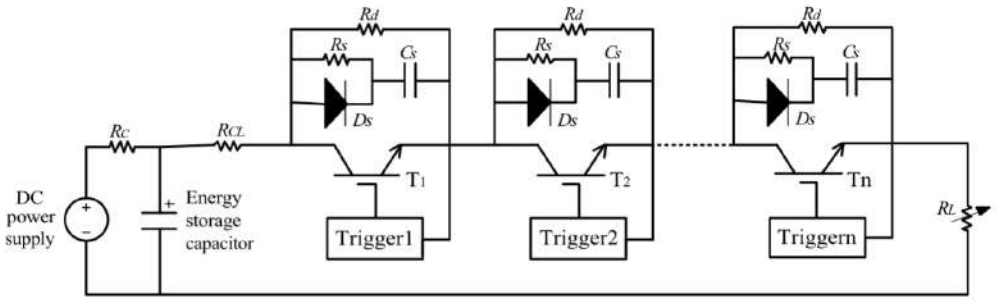

Fig. 1.1: Series connecting SiC MOSFETs with RCD snubber for DC breaker application

bandwidth OP-AMP is used [10]- [13]. Except for the high bandwidth OP-AMP, this method does not require complex circuitry. Feedback gains are critical in this method to achieve any desired voltage balancing. In this method, TVS diodes are used to limit the overvoltages. [25] presents a novel voltage balancing technique in which maximum device voltage is clamped using a capacitor and a diode. Also, the stored energy in the capacitor is recovered for self powering the gate driver. Fig.1.2 shows Active Voltage Control technique for series connected IGBTs. High bandwidth OP-AMP is cascaded to meet the bandwidth requirement for voltage balancing.

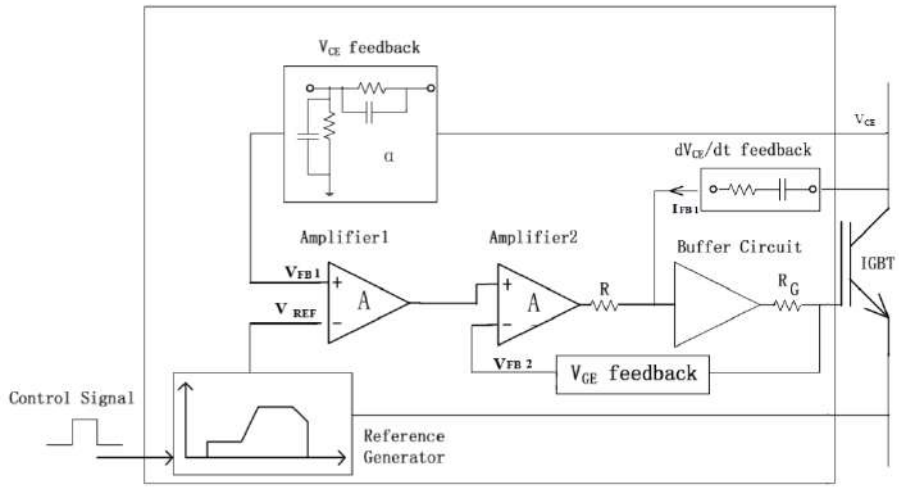

Fig. 1.2: Typical AVC control technique for series connected IGBTs

Gate Pulse Delay (GPD) control [14]- [18] is also a popular control technique. In this method, a simple gate driver is used for voltage balancing. The turn on and turn off instants of the gate signals are delayed based on the voltage mismatch. This

method requires a drain to source voltage sensing circuit, and the central controller uses the sensed signal of all the device voltages to decide the difference in the voltage mismatch. The central controller determines the delay required to achieve the voltage balancing. [19] proposes a magnetic coupling based gate pulse synchronizing technique. The above mentioned method requires a central controller as shown in Fig.1.3 and high-precision delay IC to adjust the gate pulse delay to a few nanoseconds. However, these methods do not address diode voltage balancing control.

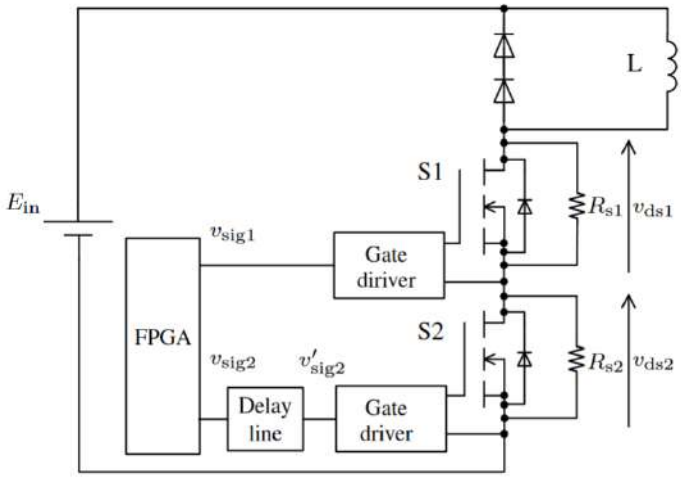

Fig. 1.3: Gate pulse delay control technique

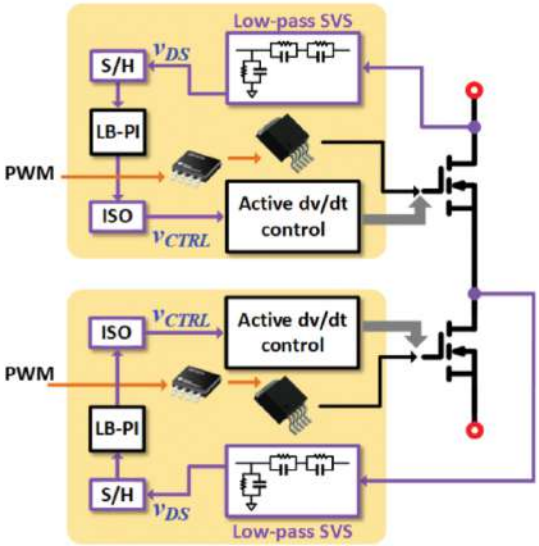

Fig. 1.4: Active Voltage Balancing technique

Active Voltage Balancing is a more popular technique for series connecting SiC MOSFETs. [20] uses a drain side switch, shunt capacitor, and conventional gate driver with the central controller to actively control the device ($\frac{dv}{dt}$) to achieve voltage balancing control. The PWM technique is used with a shunt capacitor for voltage balancing as shown in Fig.1.4. [21] proposes a voltage balancing control method with Active Gate Driver (AGD). A gate resistance modulation method with a signal time delay is adopted for dynamic voltage sharing. [22] proposes an active gate driver with variable gate voltage control in a closed loop fashion to achieve voltage balancing. It uses a single p-channel MOSFET to determine the connection timing of a pre-charged capacitor in series with the input capacitance, in which the voltage balancing is achieved. [23], [24] presents active $\frac{dv}{dt}$ control where the voltage imbalance created is mainly due to the formation of gate to earth capacitance. The $\frac{dv}{dt}$ of the device is controlled by controlling the capacitor current by adding additional Miller capacitance. [26] proposes a hybrid voltage balancing technique by combining active $\frac{dv}{dt}$ control and gate pulse delay control for controlling the active switch voltage in series connected devices. In this method a small compensation capacitor is added for diode voltage balancing.

1.3 REVIEW OF SHORT CIRCUIT PROTECTION TECHNIQUES

Protecting SiC MOSFETs during fault condition is a major challenge [27]. The short-circuit protection is a challenging task for SiC MOSFETs due to their fast switching speed and smaller short-circuit withstand time compared to Si IGBTs. This time further shrinks at higher operating temperature [28]. Thus, a reliable short-circuit detection and quenching method is required for wide adoption of SiC MOSFETs. Several protection schemes are proposed for SiC MOSFETs. The gate charge characteristics shows the variation in determining the normal and short-circuit event [29]. [30] presents Current Transformer (CT) based short-circuit protection, where the CT is used to sense the drain current and a fast comparator is used to detect the short circuit event. Rogowski coil is also used to sense the di/dt and the drain current is reconstructed using the integrator which is compared with fault current reference to detect the short circuit event [31]. The stray inductance between Kelvin and power

source terminal of SiC MOSFETs is used to detect the fault current in [32], [33]. All the above mentioned methods give better short-circuit performance but they are difficult to implement.

Desaturation based protection technique is commonly used for short circuit protection of IGBTs. It has the advantage of easy implementation, lesser complexity, and higher noise immunity. But it cannot be directly used for SiC MOSFETs due to the fixed blanking time [34]- [35]. The blanking time is provided to differentiate between the normal turn on and the short circuit event. [36] discusses adaptive blanking time in IGBTs, where the blanking time is varied by monitoring the collector to emitter saturation voltage and varying the desaturation comparator reference. This method, cannot be directly implemented due to the fast switching speed of SiC MOSFETs. [37], [39] presents a modified desaturation circuit, where an additional resistor is added between the gate and desaturation sensing circuit to minimise the charging time of the blanking capacitor.

1.4 BRIEF DESCRIPTION OF THE PRESENT WORK

The present work aims to address the voltage imbalance in series connected SiC MOSFETs due to the presence of gate pulse mismatch, process variation and layout parasitics. Gate Current Control based Active Gate Driver(AGD) is used for controlling the switching transients during turn on and turn off time. The gate current control leads to the constant rate of gate to source voltage (v_{gs}) change compared to the voltage source driven control [38], [40]. Miller current for the ($\frac{dv}{dt}$) control can be effectively controlled through current source. The sensitivity of the current control is much lower than that of the voltage control, which is very immune to gate loop parasitics. Fig.1.5 shows the block diagram unit of single Active Gate Driver connected to SiC MOSFET. Several such units can be connected in series to realise the series connection of SiC MOSFETs. Ideally, there is no limitation on the number of units that can be series connected, but limitations may come due to the complexity of the circuit. The key building blocks of Active Gate Driver(AGD) are FPGA, Power Supply Unit(PSU), turn on and turn off stages for gate current control, voltage sensing, and signal conditioning units. Each AGD in the series connected string receives a gate pulse and transmits the

fault information.

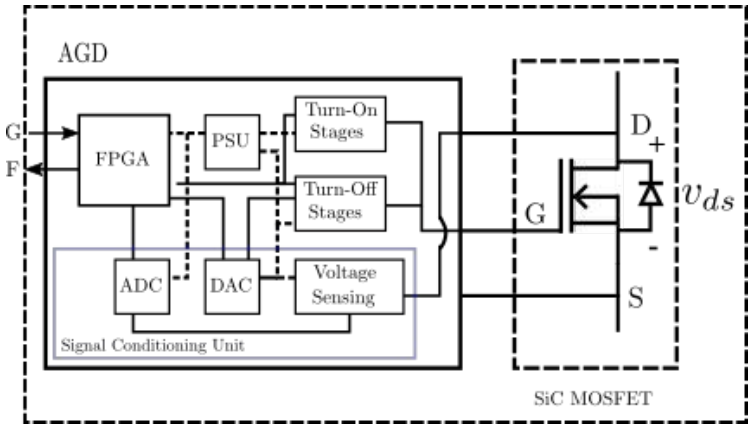

Fig. 1.5: Block diagram representation of proposed AGD for series connecting SiC MOSFETs

The present work address the issues related to series connection implementation. Some of them are mismatches in the input gate pulse timing received by the gate drivers, variations in parasitic capacitance of SiC MOSFETs due to process variation, and parasitic inductance and capacitance formation due to the circuit layout. These issues are addressed using AGD based control with no communication to the central controller. Each individual SiC MOSFET in the series connected string contains a dedicated Active Gate Driver(AGD). AGD requires only the device voltage (v_{ds}) information to perform active control to achieve voltage balancing in both the transient and steady state. The present work also proposes a low frequency closed loop control for voltage balancing of series connected SiC MOSFETs for varying load conditions, the device ($\frac{dv}{dt}$) variation also depends on the magnitude of the load current. At lower load conditions, the active control cannot achieve good voltage balancing. The low frequency control, in conjunction with the active control, is used to achieve voltage balancing at varying load current operations. The present work also proposes a novel active diode voltage balancing technique for balancing the body diode voltages of SiC MOSFETs when the diodes are turned off. The body diode which blocks the higher voltage is discharged by partially turning on the respective MOSFET. Excess charge in the diode reverse capacitance is discharged to the device until it reaches the set reference voltage. The experimental verification of the proposed technique are performed at 1.2kV dc bus voltage with two devices in series and 2.1kV dc bus voltage with three devices in series.

The present work proposes an adaptive blanking time based Hard Switch Fault(HSF) or shoot through detection technique for detecting the shoot through event in SiC MOSFETs. The adaptive blanking technique makes use of the AGD's FPGA to change the blanking time as the load current varies. This eliminates the fixed blanking time used in the conventional desaturation technique. The proposed adaptive blanking time technique is experimentally verified and validated in a Double Pulse Test (DPT) setup.

1.5 ORGANIZATION OF THE THESIS

The thesis is organised as follows:

Chapter 2 includes modeling of the switching transients of series connected SiC MOSFETs. The analysis captures the issues associated with series connected SiC MOSFETs. The transients during turn on and turn off are analyzed and modeled. The steady state $\frac{di}{dt}$ and $\frac{dv}{dt}$ of the series connected devices are derived, which can be used for controlling the switching transients. The steady state analysis captures the effect of various circuit parameters that contribute to voltage unbalance. The variation of load current in series connected SiC MOSFETs is presented. The issue of body diode voltage imbalance is also discussed.

Chapter 3 discusses the proposed active gate driving control technique for series connected SiC MOSFETs. Using the analytical model, current source based turn on and turn off control stages are presented. The operation of each switching stage and its impact on voltage balancing in the device are discussed. The need for closed loop control for voltage balancing during low load current conditions, along with the control loop design are explained. The body diode voltage control is presented for voltage balancing during diode turn off transients.

Chapter 4 focuses on the hardware implementation and realisation of the proposed active control switching stages for turn on and turn off. The current source stages are realised using NMOS and PMOS switches. This chapter also includes the hardware results of the proposed control technique.

Chapter 5 discusses the proposed adaptive digital blanking time technique for detecting the HSF or Shoot through event in SiC MOSFET. The working methodology

and practical implementation along with the experimental hardware results are also presented in this chapter.

Chapter 6 concludes the thesis.

CHAPTER 2

Modelling and Analysis of Switching Transient of Series Connected SiC MOSFETs

2.1 INTRODUCTION

Series connecting several low voltage SiC MOSFETs is one of the optimal solution for medium voltage applications. However, SiC MOSFETs switch at a much faster rate than the Si IGBTs. The effects of converter parasitic inductance and MOS capacitance play a dominant role during the switching transient. It has a direct impact on the voltage balancing of series connected SiC MOSFETs in both transient and steady state conditions. The series connected SiC MOSFETs must be modelled and analysed in order to control the voltage balancing problem. In this chapter, the turn on and turn off switching transients of series connected SiC MOSFETs are analysed and mathematically modelled. The switching dynamics are modelled using a current source. The relationship between the device turn on and turn off behaviour with gate current (i_g) is established. The effects of parasitics in MOS devices have been considered in the modelling. In addition, the effects of load current on voltage balancing in series connected SiC MOSFETs are also discussed. SPICE simulation is used to validate the modelling and analysis. The simulation results are presented to validate the switching transient analysis.

2.2 TURN ON SWITCHING TRANSIENT ANALYSIS

The mathematical modelling of switching dynamics using a voltage source and series gate resistor approach yields complex equations with little intuitive insight. Furthermore, switching parameters such as $\frac{di}{dt}$ and voltage overshoot are affected by the threshold voltage (V_{th}) and common source inductance (L_s). The switching dynamics varies with the threshold voltage (V_{th}). The variation in threshold voltage due to the junction temperature (T_j) variation is also significant, thus making control even more

difficult[20]. However, using a current source based approach, the device $\frac{di}{dt}$ and $\frac{dv}{dt}$ become a linear function of gate current(i_g) thus simplifies the control technique. The turn on and turn off switching transient are analysed with double pulse test(DPT) setup with clamped inductive load as shown in Fig.2.1.

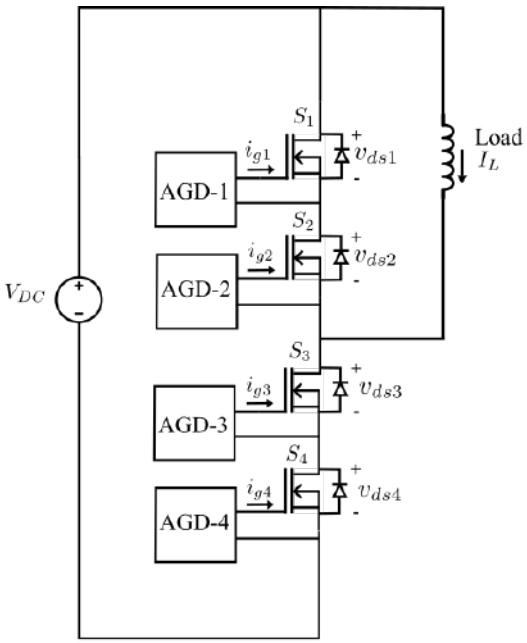

Fig. 2.1: Double pulse test setup for analysing series connected SiC MOSFETs

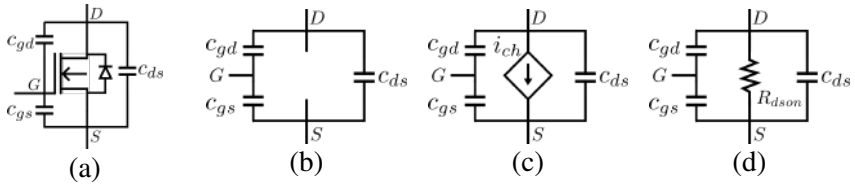

Fig. 2.2: Simplified circuit model of SiC MOSFET at various switching stage

The simplified circuit model of SiC MOSFET is shown in Fig.2.2. Fig.2.2a shows the equivalent circuit symbol of SiC MOSFET with parasitic capacitance, where C_{gs} is gate to source capacitance, C_{gd} is gate to drain capacitance and C_{ds} is drain to source capacitance. The gate to source voltage(v_{gs}) decides the mode of operation. If the gate to source voltage(v_{gs}) is less than threshold voltage ($v_{gs} < V_{th}$), the device operates in cut-off region and the equivalent circuit model is shown in Fig.2.2b. When the drain to source voltage(v_{ds}) is greater than gate to source voltage(v_{gs}) and threshold voltage(V_{th}), the device operates in the saturation region ($v_{ds} > v_{gs} > V_{th}$). Fig.2.2c

depicts the equivalent circuit model, where i_{ch} represents the channel current. If the gate to source voltage(v_{gs}) is greater than threshold voltage(V_{th}) and device drain to source voltage (v_{ds}), the device operates in the triode or linear region ($v_{gs} > V_{th} > v_{ds}$). The equivalent model is shown in Fig.2.2d, R_{dson} represents the on-state resistance of the device. These models will be often used in analysing the switching transients of series connected SiC MOSFETs.

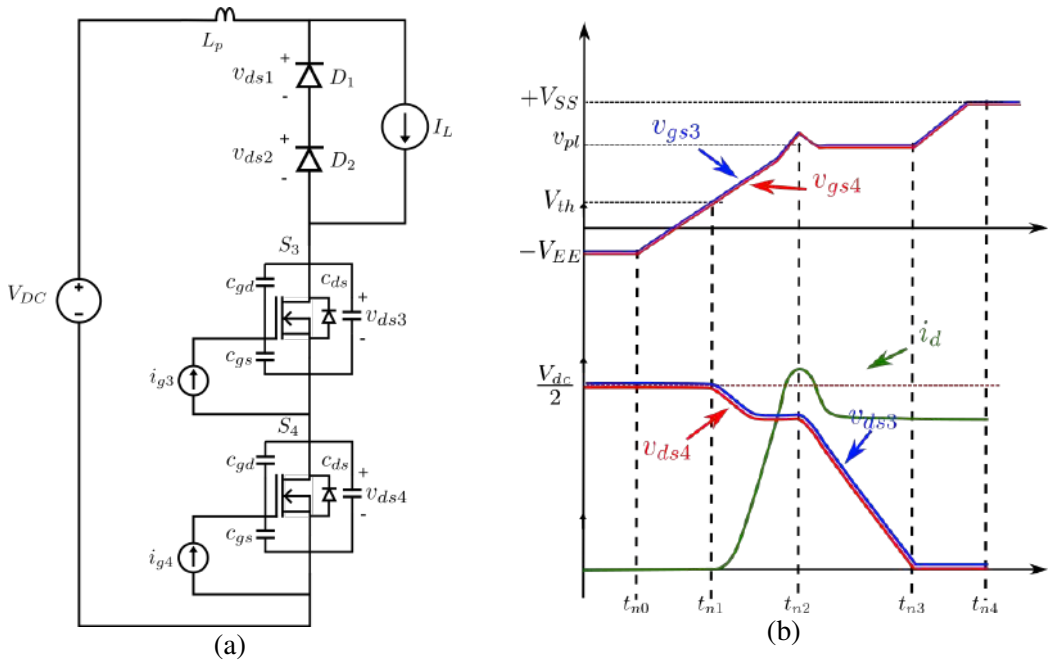

Fig. 2.3: (a) DPT test setup driven with current source (b) Ideal turn on switching transient

The Fig.2.3a shows the DPT setup with top series connected SiC MOSFETs S_1 and S_2 in Fig.2.1 are replaced with their body diode D_1 and D_2 respectively. The gate of the device S_3 and S_4 are driven by the current source of magnitude i_{g3} and i_{g4}. Prior to the turning on of the device S_3 and S_4, the load current I_L is assumed to be free-wheeling through D_1 and D_2. Fig.2.3b shows the ideal turn on transient of series connected SiC MOSFETs, where the gate voltage and the device parameters are exactly matched. The body diode D_1 and D_2 drop are assumed to be zero (ideal condition) when it is forward biased.

$$V_{DC} = V_{TOP} + V_{BOT} \tag{2.1}$$

where V_{TOP} and V_{BOT} is given by

$$V_{TOP} = v_{ds1} + v_{ds2} \tag{2.2}$$

$$V_{BOT} = v_{ds3} + v_{ds4} \tag{2.3}$$

For series connected devices, the turn off blocking voltage is decided by the number of devices connected in the series string. In case of two devices in series connection, the blocking voltage of device S_3 and S_4 is $\frac{V_{DC}}{2}$.

The turn on transient of ideal series connected SiC MOSFETs is identical to the single device turn on switching waveform shown in Fig.2.3b. However, due to IC time delays and parasitic earth capacitance formation from the switching node, the input gate pulse and parasitic capacitance of series connected SiC MOSFETs cannot be precisely matched in practice. The gate pulse instant of device S_4 is delayed from that of S_3 to analyse the turn on transient of series connected SiC MOSFETs under real world conditions.

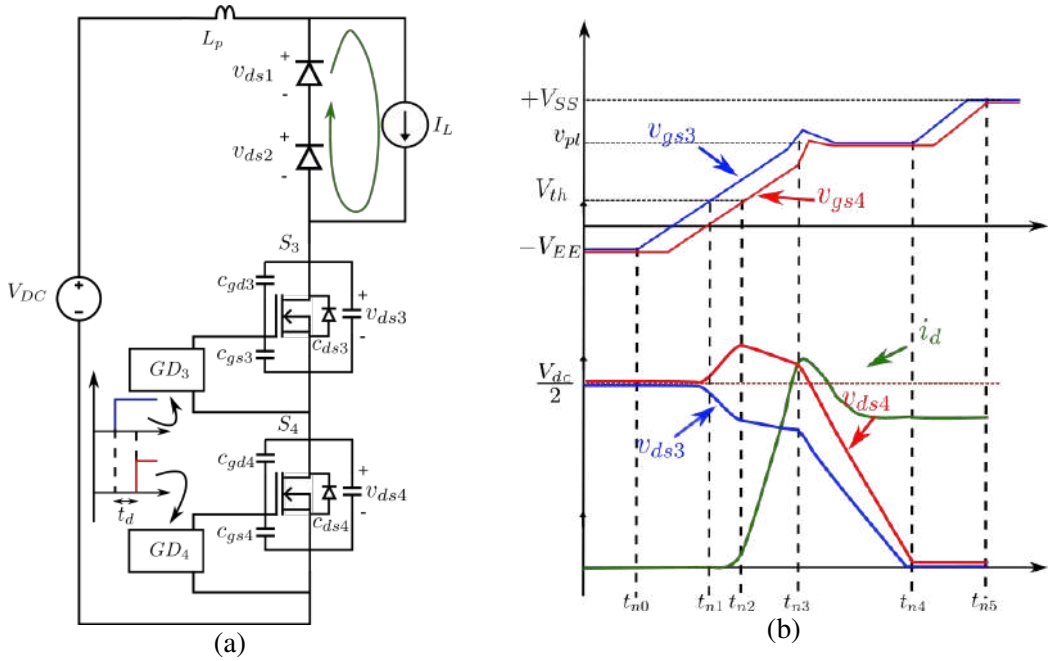

Fig. 2.4: (a) DPT test setup with input gate pulse delayed (b) Practical turn on switching transient of two device series connection

The gate pulse instant of device S_4 Gate driver GD_4 is delayed by delay time (t_d) with respect to the device S_3 Gate driver GD_3. The load current I_L is assumed to be

free-wheeling through the top diode D_1 and D_2. The turn on transient can be subdivided into delay time, turn on over voltage time, current rise time and voltage fall time.

2.2.1 Delay time interval

Fig.2.5 shows the equivalent circuit model of series connected device S_3 and S_4 driven with current source of magnitude i_{g3} and i_{g4}. For simplicity, the top diodes D_1 and D_2 are replaced with a single diode. The load current I_L is assumed to be free wheeling through it. As per the assumption in Fig.2.4a, the device S_3 receives the gate pulse much earlier than device S_4. The time interval ($t_{n0} \rightarrow t_{n1}$) in Fig.2.4b represents the turn on delay time which signifies the amount of time required to rise the gate to source voltage (v_{gs}) from negative voltage ($-V_{EE}$) to threshold voltage (V_{th}). During

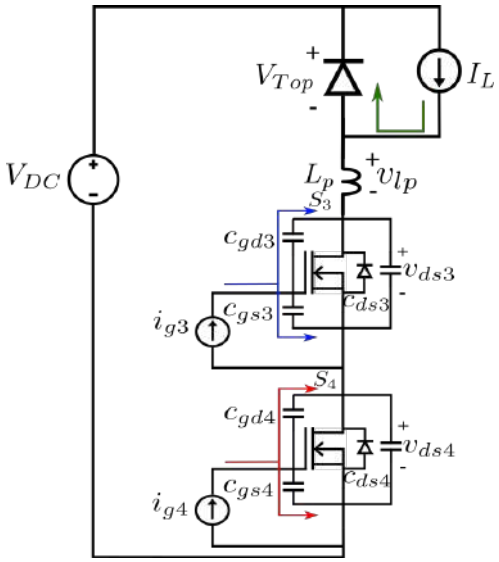

Fig. 2.5: Equivalent Circuit model during delay time

this interval, the current source i_{g3} and i_{g4} charges the input capacitance of device S_3 and S_4. Where the input capacitance C_{iss3} and C_{iss4} of device S_3 and S_4 are given by Eq.(2.4) and Eq.(2.5)

$$C_{iss3} = C_{gs3} + C_{gd3} \tag{2.4}$$

$$C_{iss4} = C_{gs4} + C_{gd4} \tag{2.5}$$

Applying KCL at the gate node of device S_3 and S_4 is given by Eq.(2.6) and Eq.(2.7)

$$i_{g3} = C_{gs3}\frac{dv_{gs3}}{dt} + C_{gd3}\frac{dv_{gd3}}{dt} \tag{2.6}$$

$$i_{g4} = C_{gs4}\frac{dv_{gs4}}{dt} + C_{gd4}\frac{dv_{gd4}}{dt} \tag{2.7}$$

Similarly KVL across the capacitance of device S_3 and S_4 is given by Eq.(2.8) and Eq.(2.9)

$$v_{gd3} = v_{gs3} - v_{ds3} \tag{2.8}$$

$$v_{gd4} = v_{gs4} - v_{ds4} \tag{2.9}$$

During this time, device drain to source voltage v_{ds3} and v_{ds4} is blocking $\frac{V_{DC}}{2}$. Substituting Eq.(2.8) and Eq.(2.9) in Eq.(2.6) and Eq.(2.7), the gate voltage of series connected SiC MOSFETs S_3 and S_4 is obtained as given in Eq.(2.10) and Eq.(2.11). The gate can be equivalently represented as current source connected in parallel with SiC MOSFET input capacitance (C_{iss}). At the end of time interval(t_{n1}) the device S_3 which is turned on earlier than the device S_4 reaches the threshold voltage(V_{th}) and enters into turn on over voltage interval.

$$v_{gs3} = \frac{1}{C_{iss3}}\int_0^t i_{g3}dt \tag{2.10}$$

$$v_{gs4} = \frac{1}{C_{iss4}}\int_0^t i_{g4}dt \tag{2.11}$$

2.2.2 Turn on over voltage interval

The time interval ($t_{n1} \rightarrow t_{n2}$) in Fig.2.4b represents the turn on over voltage period. Due to the presence of delay time (t_d), the device S_3 turns on earlier than the device S_4. The gate to source voltage (v_{gs3}) of device S_3 reaches the threshold voltage (V_{th}) much earlier than the device S_4. As the device S_3 crosses threshold voltage, the device enters into saturation region. The channel is formed to conduct the load current. The expression for channel current is given by Eq.(2.12).

$$i_{ch3} = g_{m3}v_{gs3} \tag{2.12}$$

where g_{m3} represents the transconductance of device S_3. However, device S_3 cannot conduct the load current as gate to source voltage(v_{gs4}) of S_4 has not reached the threshold voltage. Fig.2.6 shows the equivalent circuit during the turn on overvoltage interval. The device S_3 channel current i_{ch3} cannot take the full load current as the device S_4 has not reached the threshold voltage. A small channel current i_{ch3} flows through the output capacitance(C_{oss4}) of the device S_4, thus increasing the device drain to source voltage(v_{ds4}). The increase in the drain to source voltage (v_{ds4}) of S_4 causes the drain to source voltage (v_{ds3}) of S_3 to decrease to balance the KVL. The current rise $\frac{di}{dt}$ during this interval will mainly depend on the magnitude of the applied gate current. Smaller magnitude of i_{g3} causes lower $\frac{di}{dt}$. This in turn reduces the turn on over voltage of device S_4 by slowly charging the output capacitance(C_{oss4}). This phenomenon happens until the gate voltage of S_4 reaches the threshold voltage.

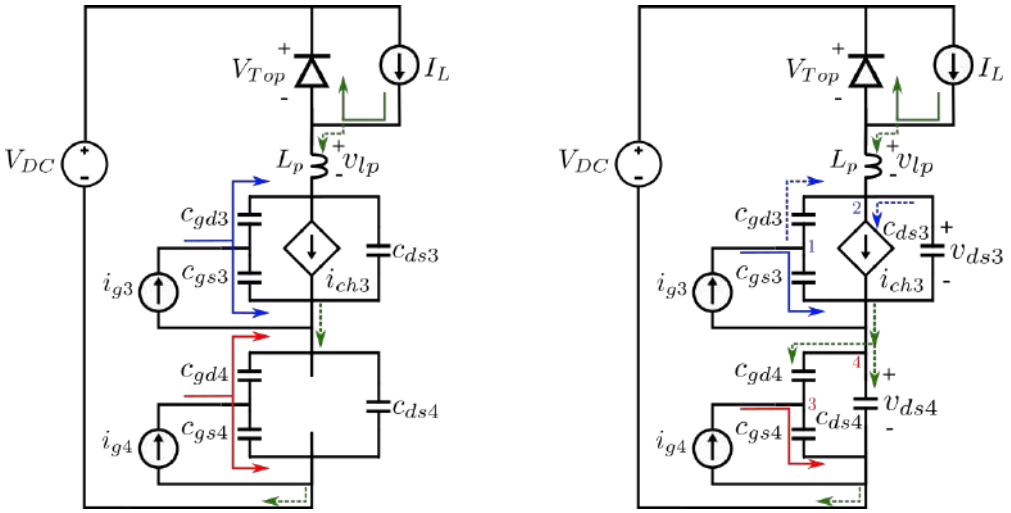

Fig. 2.6: (a) Equivalent circuit model during turn on over voltage interval (b) Over voltage increase in device S_4

Applying KCL at gate node 1 of Fig.2.6b,

$$i_{g3} = C_{gs3}\frac{dv_{gs3}}{dt} + C_{gd3}\frac{dv_{gd3}}{dt} \tag{2.13}$$

Simplifying Eq.(2.13) with $v_{gd3} = v_{gs3} - v_{ds3}$

$$i_{g3} = C_{iss3}\frac{dv_{gs3}}{dt} - C_{gd3}\frac{dv_{ds3}}{dt} \tag{2.14}$$

Where $C_{iss3} = C_{gs3} + C_{gd3}$ is the equivalent input capacitance of device S_3. Similarly applying KCL at node 3,

$$i_{g4} = C_{iss4}\frac{dv_{gs4}}{dt} - C_{gd4}\frac{dv_{ds4}}{dt} \tag{2.15}$$

Applying KCL at the drain node 2 of device S_3, the drain node 4 of device S_4 and outer KVL loop (by neglecting the v_{lp} drop as $\frac{di}{dt}$ is very low) is

$$i_{ch3} = i_d + i_{Cgd3} + i_{Cds3} \tag{2.16}$$

$$i_d = i_{Cgd4} + i_{Cds4} \tag{2.17}$$

$$V_{DC} = v_{ds3} + v_{ds4} \tag{2.18}$$

Simplifying the Eq.2.14, Eq.2.15, Eq.2.16 and Eq.2.17

$$K_1\frac{dv_{ds4}}{dt} - K_2\frac{dv_{ds3}}{dt} = i_{ch3} - \frac{C_{gd3}}{C_{iss3}}i_{g3} - \frac{C_{gd4}}{C_{iss4}}i_{g4} \tag{2.19}$$

Differentiating Eq.2.18

$$\frac{dv_{ds3}}{dt} + \frac{dv_{ds4}}{dt} = 0 \tag{2.20}$$

Substituting the Eq.2.20 in Eq.2.19, the rise in the device drain to source voltage ($\frac{dv_{ds4}}{dt}$) can be expressed as

$$\frac{dv_{ds4}}{dt} = \frac{(\frac{g_{m3}-C_{gd3}}{C_{iss3}})i_{g3} - \frac{C_{gd4}}{C_{iss4}}i_{g4}}{K_1 + K_2} \tag{2.21}$$

Where $K_1 = (C_{oss4} - \frac{C_{gd4}^2}{C_{iss4}}) \simeq C_{oss4}$ and $K_2 = (C_{oss3} - \frac{C_{gd3}^2}{C_{iss3}}) \simeq C_{oss3}$,where C_{oss3} and C_{oss4} are the equivalent output capacitance of device S_3 and S_4. The Eq.2.21 can be modified as

$$\frac{dv_{ds4}}{dt} = \frac{(\frac{g_{m3}-C_{gd3}}{C_{iss3}})i_{g3} - \frac{C_{gd4}}{C_{iss4}}i_{g4}}{C_{oss3} + C_{oss4}} \tag{2.22}$$

From Eq.2.22, the rise in the device S_4 drain to source voltage ($\frac{dv_{ds4}}{dt}$) is directly dependent on the magnitude of the gate current i_{g3} and i_{g4}. Higher i_{g3} current results in larger ($\frac{dv_{ds4}}{dt}$). Similarly, the sum of the device voltage v_{ds3}, v_{ds4} during this interval will always be equal to the applied DC bus voltage (V_{DC}) to satisfy the KVL.

2.2.3 Current rise interval

The time interval ($t_{n2} \rightarrow t_{n3}$) in Fig.2.4b is termed as the current rise ($\frac{di_d}{dt}$) region. The device S_3 channel has already formed and it is in saturation region. Despite the channel has formed, ($\frac{di_d}{dt}$) will be very less as the other series connected device channel has not formed yet. The current rise of series connected devices starts as soon as the gate voltage (v_{gs4}) of device S_4 reaches the threshold voltage. During this interval, the device channels are formed, and both devices are in saturation, ensuring their readiness to take the load current. Fig.2.7 shows the equivalent circuit model when both the device are in saturation.

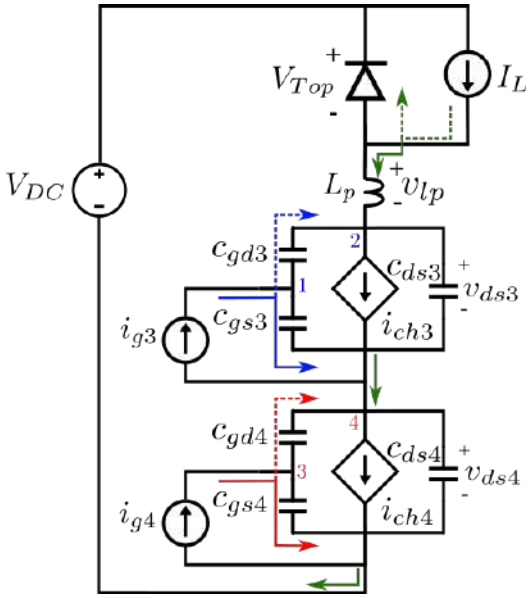

Fig. 2.7: Equivalent Circuit model during Current rise Interval

Applying KCL at the gate node 1 and 3 results in Eq.2.23 and Eq.2.24 respectively.

$$i_{g3} = C_{iss3}\frac{dv_{gs3}}{dt} - C_{gd3}\frac{dv_{ds3}}{dt} \tag{2.23}$$

$$i_{g4} = C_{iss4}\frac{dv_{gs4}}{dt} - C_{gd4}\frac{dv_{ds4}}{dt} \tag{2.24}$$

Taking Laplace transformation of Eq.2.23 Eq.2.24 results in Eq.2.25 and Eq.2.26

$$I_{g3}(s) = sC_{iss3}V_{gs3}(s) - sC_{gd3}V_{ds3}(s) \tag{2.25}$$

$$I_{g4}(s) = sC_{iss4}V_{gs4}(s) - sC_{gd4}V_{ds4}(s) \tag{2.26}$$

Similarly, applying KCL at drain node 2 and 4 and taking Laplace transformation results in Eq.2.27 and Eq.2.28

$$I_d(s) = sC_{oss3}V_{ds3}(s) + (g_{m3} - sC_{gd3})V_{gs3}(s) \tag{2.27}$$

$$I_d(s) = sC_{oss4}V_{ds4}(s) + (g_{m4} - sC_{gd4})V_{gs4}(s) \tag{2.28}$$

The KVL at the outer loop is given by Eq.2.29

$$V_{DC} = v_{lp} + v_{ds3} + v_{ds4} \tag{2.29}$$

The rate of rise of i_d as a function of both the gate current is described from Eq.2.30. It should be noted that the higher order s^3 term has been ignored as the relative magnitude is very small.

$$sI_d(s) = \frac{I_{g3}(s)(1 - s(\frac{C_{gd3}}{g_{m1}} - \frac{K_2}{g_{m2}})) + I_{g4}(s)(1 - s(\frac{C_{gd4}}{g_{m2}} - \frac{K_1}{g_{m1}}))}{s^2L_p(\frac{K_1g_{m2}+K_2g_{m1}}{g_{m1}g_{m2}}) + s(L_p + \frac{C_{iss3}K_2}{g_{m1}g_{m2}} + \frac{C_{iss4}K_1}{g_{m1}g_{m2}}) + (\frac{C_{iss3}}{g_{m3}} + \frac{C_{iss4}}{g_{m4}})} \tag{2.30}$$

where $K_1 = C_{iss3}C_{oss3} - C_{gd3}^2$ and $K_2 = C_{iss4}C_{oss4} - C_{gd4}^2$ and in the steady state the $(\frac{di_d}{dt})$ of drain current is given by Eq.2.31

$$\frac{di_d}{dt} = \frac{i_{g3} + i_{g4}}{\frac{C_{iss3}}{g_{m3}} + \frac{C_{iss4}}{g_{m4}}} \tag{2.31}$$

From the Eq.2.31, the current rise $(\frac{di_d}{dt})$ directly depends on the applied gate current, transconductance and input capacitance of the SiC MOSFETs. The $\frac{di_d}{dt}$ of the series connected SiC MOSFETs can be controlled by directly controlling the input gate current.

$$v_{ds3} + v_{ds4} = V_{DC} - v_{lp} \tag{2.32}$$

Due to the $\frac{di_d}{dt}$, there will be a $L_p\frac{di_d}{dt}$ drop across the parasitic inductance (L_p) as described in Eq.2.32. This leads to slight reduction in the device voltage during the current rise interval as shown in Fig.2.4b.

2.2.4 Voltage fall interval

The time interval ($t_{n3} \rightarrow t_{n4}$) in Fig.2.4b is termed as voltage fall ($\frac{dv_{ds}}{dt}$) interval. As the drain current reaches the load current, the device enters into the voltage fall interval. The top diode will be entering into the reverse recovery mode and an overshoot is observed in the drain current. During the voltage fall interval, the device gate voltage reaches the plateau voltage (v_{pl}) and most of the gate current will be flowing into the Miller capacitance of the device. The equivalent circuit model has been presented in Fig.2.8. The relation between the ($\frac{dv_{ds}}{dt}$) and the applied input current can be derived as follows.

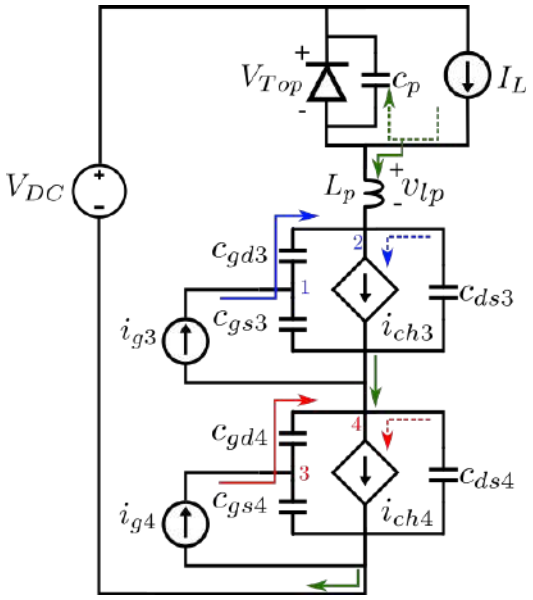

Fig. 2.8: Equivalent Circuit model during Voltage fall Interval

Similarly, applying KCL at the drain node 2 and 4 in Fig.2.8 results in Eq.2.33 and Eq.2.34.

$$i_d + i_{Cgd3} = i_{ch3} + i_{Cds3} \tag{2.33}$$

$$i_d + i_{Cgd4} = i_{ch4} + i_{Cds4} \tag{2.34}$$

Taking Laplace transform

$$I_d(s) + I_{Cgd3}(s) = I_{ch3}(s) + I_{Cds3}(s) \tag{2.35}$$

$$I_d(s) + I_{Cgd4}(s) = I_{ch4}(s) + I_{Cds4}(s) \tag{2.36}$$

Eq.2.25, Eq.2.26, Eq.2.35 and Eq.2.36 can be simplified as

$$sV_{ds3}(s) = \frac{sI_d(s)C_{iss3} + (sC_{gd3} - g_{m3})I_{g3}(s)}{s(C_{iss3}C_{oss3} - C_{gd3}^2) + g_{m3}C_{gd3}} \tag{2.37}$$

$$sV_{ds4}(s) = \frac{sI_d(s)C_{iss4} + (sC_{gd4} - g_{m4})I_{g4}(s)}{s(C_{iss4}C_{oss4} - C_{gd4}^2) + g_{m4}C_{gd4}} \tag{2.38}$$

The outer loop KVL, considering the input excitation alone is given by Eq.2.39

$$V_{ds3}(s) + V_{ds4}(s) = -(sL_p + \frac{1}{sC_p})I_d(s) \tag{2.39}$$

The voltage fall of entire series connected device can be simplified by solving Eq.2.39

$$sV_{BOT}(s) = \frac{(1 + s^2L_pC_p)(I_{g3}(s)(sC_{gd3} - g_{m3})(M_2) + I_{g4}(s)(sC_{gd4} - g_{m4})(M_1))}{(M_1)(M_2)(s^2L_pC_p + 1) + sC_p[C_{iss3}(M_2) + C_{iss4}(M_1)]} \tag{2.40}$$

where

$$M_1 = sK_1 + g_{m3}C_{gd3}$$

$$M_2 = sK_2 + g_{m4}C_{gd4}$$

$$K_1 = C_{iss3}C_{oss3} - C_{gd3}^2$$

$$K_2 = C_{iss4}C_{oss4} - C_{gd4}^2$$

The steady state $\frac{dv_{ds}}{dt}$ of the series connected device is given by

$$\frac{dv_{BOT}}{dt} = \frac{dv_{ds3}}{dt} + \frac{dv_{ds4}}{dt} = -\frac{i_{g3}}{C_{gd3}} - \frac{i_{g4}}{C_{gd4}} \tag{2.41}$$

From Eq.2.41, the voltage fall region are mainly decided by the applied gate current (i_g) charging the Miller capacitance (C_{gd}) of the series connected device. The rate of voltage fall ($\frac{dv_{ds}}{dt}$) for device S_3 and S_4 is given by Eq.2.42 and Eq.2.43.

$$\frac{dv_{ds3}}{dt} = -\frac{i_{g3}}{C_{gd3}} \tag{2.42}$$

$$\frac{dv_{ds4}}{dt} = -\frac{i_{g4}}{C_{gd4}} \tag{2.43}$$

The applied gate current and Miller capacitance primarily determine the device's rate of voltage fall. Miller capacitance, on the other hand, varies with the operating region of drain to source voltage. The change in the Miller capacitance of one of the device causes the ($\frac{dv_{ds}}{dt}$) of S_4 to be sightly different than of S_3. During the voltage fall interval, the top diode will be in the reverse recovery region. This reverse recovery charge will appear as current overshoot in this interval. After the voltage fall region, the gate to source voltage v_{gs} further increases and reaches the maximum applied voltage (recommended for minimum R_{dson}) and gets clamped to that value.

2.2.5 Simulation results of turn on switching transient

To simulate the transients of series connected SiC MOSFETs, the LTspice environment is used. The turn on transient is simulated here using two cases, one with no delay in the applied gate pulse and one with delay in the applied gate pulse. This will help to understand the issue of turn on transients in series connected SiC MOSFETs.

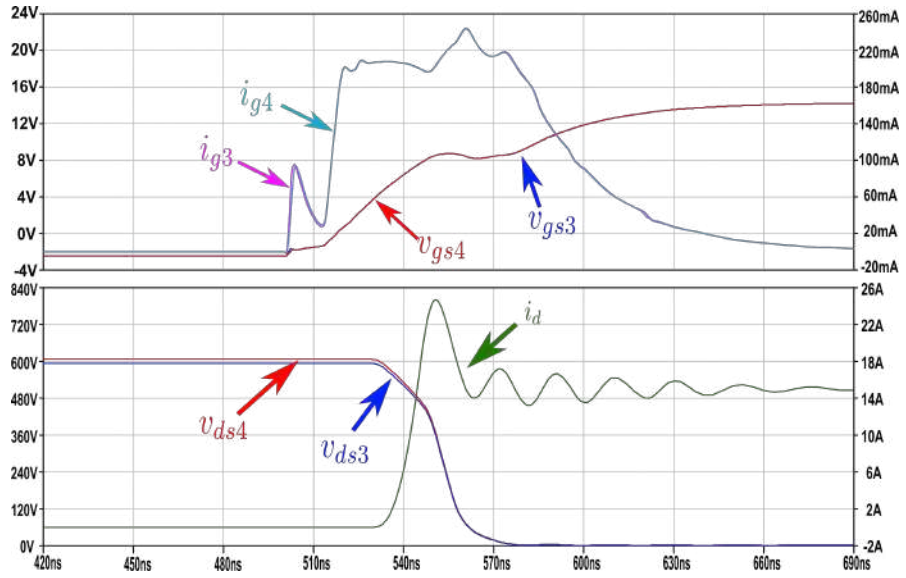

Fig. 2.9: Simulation result of turn on transient without delay (Voltage scale: 120V/div, Current scale: 4A/div and time scale: 30ns/div)

Fig.2.9 shows the ideal simulation results without any delay in the gate pulse. The device voltage v_{ds3} and v_{ds4} are identical and overlapping with each other. Now the input gate pulse is delayed by 10ns, Fig.2.10 shows the device voltage (v_{ds3}) increases due to the delay time. Due to the delay in the input gate pulse, device voltage v_{ds3} experiences over voltage of 90V from the reference voltage ($\frac{V_{DC}}{2} = 600V$). As the

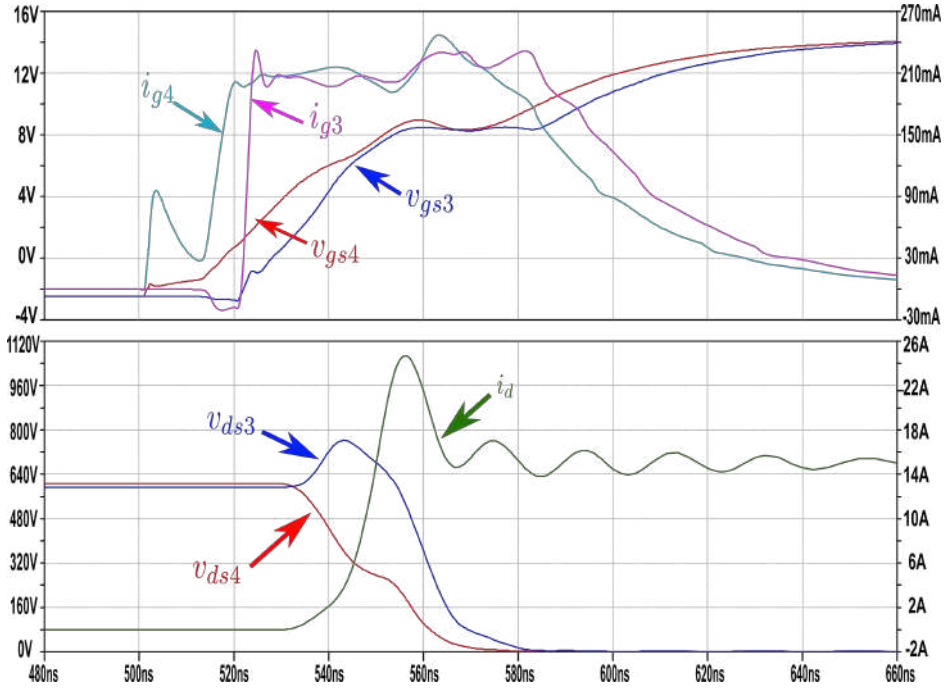

Fig. 2.10: Simulation result of turn on transient with delay (Voltage scale: 140V/div, Current scale: 4A/div and time scale: 20ns/div)

delay time between the gate pulse instants of series connected devices increases, the over voltage of the particular device also increases. This leads to the higher switching loss during the turn on and it may cause device failure if it exceeds the rated voltage.

2.3 TURN OFF SWITCHING TRANSIENT ANALYSIS

Fig.2.11a shows the Double Pulse Test(DPT) setup. Before the turn off transient, the device S_3 and S_4 is assumed to be conducting the full load current (I_L) and device is operating in the triode or ohmic region. Fig.2.11b shows the ideal turn off switching transient. In ideal turn off condition, the applied gate pulse instants are exactly matched and the turn off transient of series connected SiC MOSFET looks exactly similar to the single device turn off transient. The two device voltage v_{ds3} and v_{ds4} will be exactly blocking ($\frac{V_{DC}}{2}$) in the steady state.

The voltage imbalance can occur in the presence of delay in the applied gate pulse instant, parameter mismatch due to process variation, and the formation of earth capacitance from the switching node. Because of these variations, when considering the practical turn off switching transient, the device voltage of a series connected SiC MOSFETs cannot be precisely balanced or matched in the same way that an ideal turn

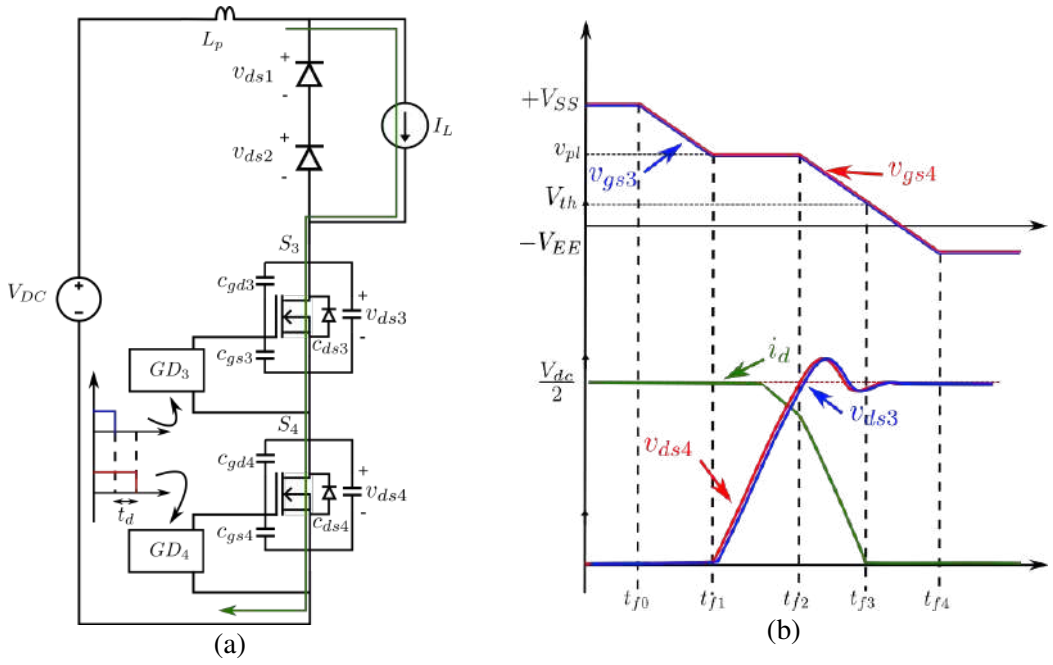

Fig. 2.11: (a) DPT test setup with input gate pulse delayed (b) Ideal turn off switching transient

off switching transient. In order to analyse the turn off transient of series connected device, the turn off gate pulse instant of device S_4 is delayed by delay time (t_d) compared to device S_3. Due to this delay time, mismatch is created in the switching transient as shown in Fig.2.12 and this mismatch can be analyzed and modelled by considering each time interval and their equivalent circuit model in that transition period.

2.3.1 Turn off delay time

Fig.2.13 shows the equivalent circuit model of series connected device S_3 and S_4 driven with current source of magnitude i_{g3} and i_{g4}. For simplicity, the top series connected device S_1 and S_2 are replaced with equivalent single diode. The load current I_L is conducting through device S_3 and S_4. Here, R_{dson3} and R_{dson4} are on-state resistances of device S_3 and S_4 respectively. As per the assumption in Fig.2.12, the device S_3 receives the gate pulse earlier than device S_4. The time interval ($t_{f0} \rightarrow t_{f1}$) in Fig.2.12 represents the turn on delay which signifies the amount of time required to bring the gate to source voltage (v_{gs}) from positive voltage ($+V_{SS}$) to Miller plateau voltage (v_{pl}). During this region, the input capacitance of the device S_3 and S_4 starts

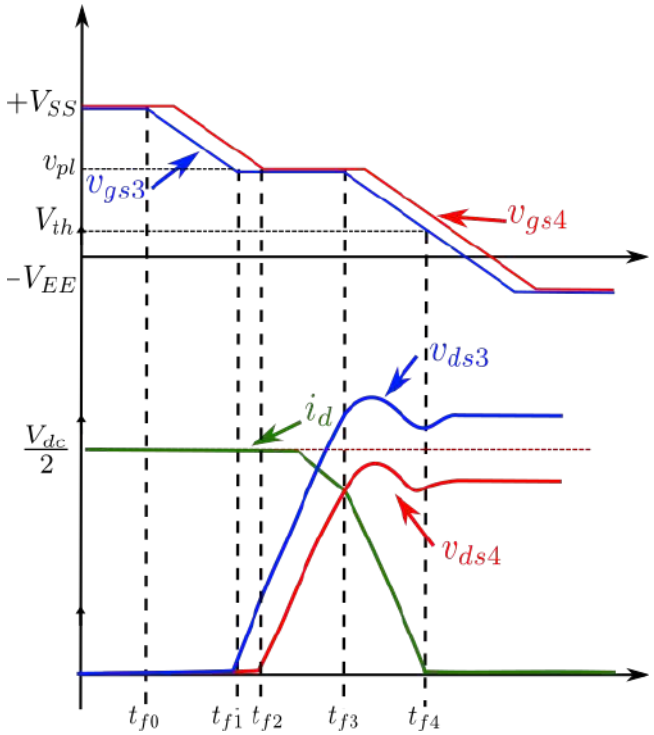

Fig. 2.12: Practical Turn-Off switching transient of two device series connection

discharging by the current source. However, there are no change in the device current (i_d) and drain to source voltage (v_{ds}) of both the series connected devices. Fig.2.13 shows the equivalent circuit model during the turn off delay time interval, where the input capacitor starts discharging from both the series connected SiC MOSFETs in accordance with the applied current source at the gate terminal.

Applying KCL at the gate node of device S_3 and S_4 Eq.(2.44) and Eq.(2.45) are obtained.

$$i_{g3} = -C_{gs3}\frac{dv_{gs3}}{dt} - C_{gd3}\frac{dv_{gd3}}{dt} \tag{2.44}$$

$$i_{g4} = -C_{gs4}\frac{dv_{gs4}}{dt} - C_{gd4}\frac{dv_{gd4}}{dt} \tag{2.45}$$

Substituting Eq.(2.8) and Eq.(2.9) in Eq.(2.44) and Eq.(2.45), gate voltages of series connected SiC MOSFETs S_3 and S_4 are obtained as Eq.(2.46) and Eq.(2.47). The gate can be equivalently represented as a current source connected in parallel with SiC MOSFET input capacitance (C_{iss}). At the end of the time interval(t_{f1}), the device S_3 which is turned off earlier than the device S_4 reaches the Miller plateau voltage(v_{pl}) and

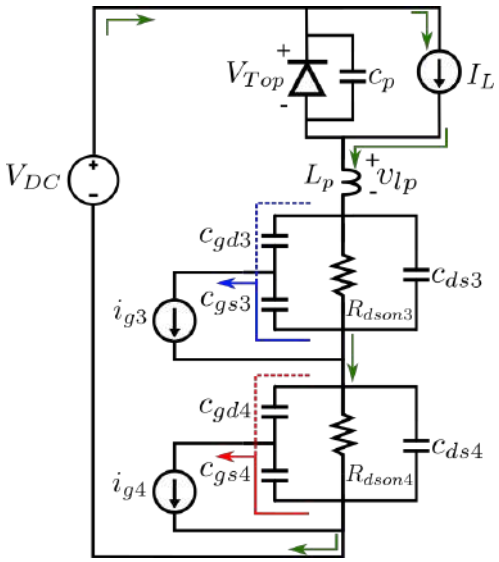

Fig. 2.13: Equivalent circuit model during delay time

enters into turn off voltage rise interval.

$$v_{gs3} = -\frac{1}{C_{iss3}} \int_0^t i_{g3} dt \tag{2.46}$$

$$v_{gs4} = -\frac{1}{C_{iss4}} \int_0^t i_{g4} dt \tag{2.47}$$

2.3.2 Voltage rise interval

The time interval ($t_{f1} \rightarrow t_{f3}$) in Fig.2.12 represents the voltage rise ($\frac{dv}{dt}$) period. At first, the gate to source voltage (v_{gs3}) of S_3 reaches the Miller plateau (v_{pl}) at t_{f1} time instant. The reduction in the gate to source voltage (v_{gs3}) causes the reduction in the current flowing through the device. As soon as the gate to source voltage (v_{gs3}) reaches the Miller plateau voltage (v_{pl}), voltage rise ($\frac{dv_{ds3}}{dt}$) of S_3 begins. But S_4 gate to source voltage (v_{gs4}) has not reached the Miller plateau voltage (v_{pl}) due to the delay present in the applied gate pulse instant. The equivalent circuit model during this region can be seen in Fig.2.14.

Applying KCL at node 1 and 2 is given by Eq.2.42 and Eq.2.43.

$$i_{g3} = C_{iss3} \frac{dv_{gs3}}{dt} - C_{gd3} \frac{dv_{ds3}}{dt} \tag{2.48}$$

$$i_d = i_{ch3} + i_{Cdg3} + i_{Cds3} \tag{2.49}$$

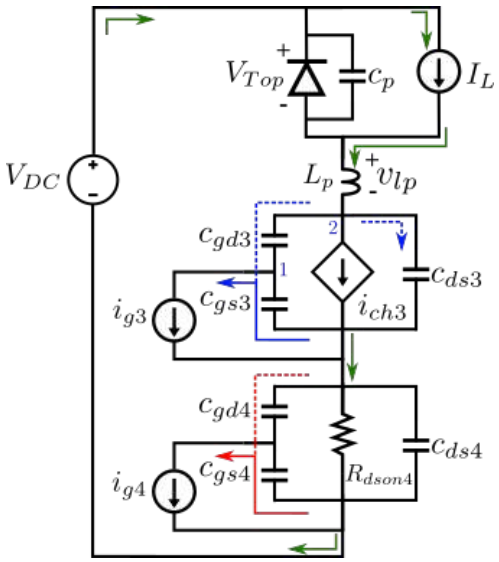

Fig. 2.14: Equivalent circuit model during voltage rise interval

Taking Laplace transform and further simplification is obtained by Eq.2.50 and Eq.2.51.

$$I_{g3}(s) = sC_{iss3}V_{gs3}(s) - sC_{gd3}V_{ds3}(s) \tag{2.50}$$

$$I_d(s) = sC_{oss3}V_{ds3}(s) + (g_{m3} - sC_{gd3})V_{gs3}(s) \tag{2.51}$$

From the outer KVL loop , the $i_d(s)$ can be obtained as

$$I_d(s) = -\frac{V_{ds3}(s)}{(sL_p + \frac{1}{sC_p} + R_{dson4})} \tag{2.52}$$

Solving Eq.2.50, Eq.2.51, Eq.2.52 and neglecting the higher order s^3 term, the voltage rise ($\frac{dv_{ds3}}{dt}$) can be expressed as

$$sV_{ds3}(s) = \frac{[(g_{m3} - sC_{gd3}) + (s^2(L_p g_{m3} - C_p R_{dson4} C_{gd3}))]I_{g3}(s)}{s^2(g_{m3}C_{gd3} + KC_p R_{dson4}) + S(K + C_p C_{iss3} + g_{m3}C_{gd3}) + g_{m3}C_{gd3}} \tag{2.53}$$

Where $K = C_{iss3}C_{oss3} - C_{gd3}^2$. The steady state ($\frac{dv_{ds3}}{dt}$) can be obtained from above Eq.2.53

$$\frac{dv_{ds3}}{dt} = \frac{i_{g3}}{C_{gd3}} \tag{2.54}$$

Similarly at t_{f2} instant, the gate to source voltage (v_{gs4}) of S_4 reaches the Miller plateau

(v_{pl}). Fig.2.15 shows the equivalent circuit model, when both the devices enter into the Miller plateau region. The dynamics of turn off at this interval is same as the voltage fall interval in the turn on instant of the series connected devices. Here, the equivalent circuit model represented in the both the conditions remains the same.

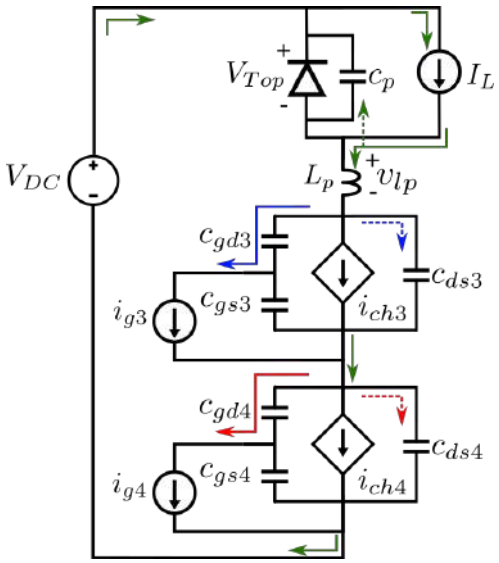

Fig. 2.15: Equivalent circuit model during voltage rise interval

The voltage rise of entire series connected device can be given by

$$sV_{BOT}(s) = \frac{-I_{g3}(s)(sC_{gd3} - g_{m3})(M_2) - I_{g4}(s)(sC_{gd4} - g_{m4})(M_1)}{(M_1)(M_2)(s^2L_pC_p + 1) + sC_p[C_{iss3}(M_2) + C_{iss4}(M_1)]} \tag{2.55}$$

where

$$M_1 = sK_1 + g_{m3}C_{gd3}$$

$$M_2 = sK_2 + g_{m4}C_{gd4}$$

$$K_1 = C_{iss3}C_{oss3} - C_{gd3}^2$$

$$K_2 = C_{iss4}C_{oss4} - C_{gd4}^2$$

The steady state $\frac{dv_{ds}}{dt}$ of the series connected device is given by

$$\frac{dv_{BOT}}{dt} = \frac{dv_{ds3}}{dt} + \frac{dv_{ds4}}{dt} = \frac{i_{g3}}{C_{gd3}} + \frac{i_{g4}}{C_{gd4}} \tag{2.56}$$

Due to the mismatch in the gate pulse instant from Fig.2.12, it can be seen that there

exist a finite static unbalance in the steady state voltage balancing. The static imbalance in the series connected devices can be represented by Eq.2.57.

$$\Delta V = V_{ds3} - V_{ds4} = \frac{I_{g3}}{C_{gd3}} t_1 - \frac{I_{g4}}{C_{gd4}} t_2 \tag{2.57}$$

where $t_1 = t_{f3} - t_{f1}$ and $t_2 = t_{f3} - t_{f2}$ are the instant at which the channel current is formed and mainly depends on the applied gate pulse instant. Either the applied gate current can be controlled or the delay time can be controlled to minimise the static imbalance in the voltage.

2.3.3 Current fall interval

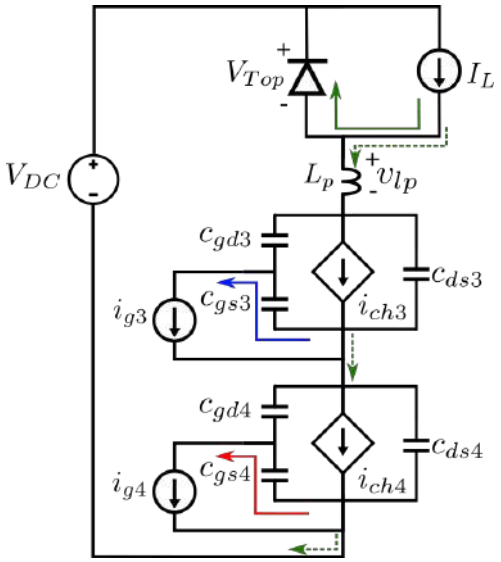

Fig. 2.16: Equivalent circuit model during current fall interval

The time interval ($t_{f3} \rightarrow t_{f4}$) in Fig.2.12 is termed as the current fall ($\frac{di_d}{dt}$) region. The current fall region begins when the sum of the device voltages exactly equals the total DC bus voltage. As the bottom series connected device blocks the entire applied DC bus voltage (V_{DC}), the diode changes its state from reverse blocking mode to conduction mode and starts taking the load current (I_L). This initiates the current fall with reduction in the gate to source voltage(v_{gs}) of the device. The equivalent circuit model during current fall interval is shown in Fig.2.16. The equivalent circuit model looks exactly same as the current rise interval of turn on transient. The current fall

expression is given by Eq.2.58.

$$sI_d(s) = -\frac{I_{g3}(s)(1 - s(\frac{C_{gd3}}{g_{m1}} - \frac{K_2}{g_{m2}})) - I_{g4}(s)(1 - s(\frac{C_{gd4}}{g_{m2}} - \frac{K_1}{g_{m1}}))}{s^2 L_p(\frac{K_1 g_{m2} + K_2 g_{m1}}{g_{m1} g_{m2}}) + s(L_p + \frac{C_{iss3} K_2}{g_{m1} g_{m2}} + \frac{C_{iss4} K_1}{g_{m1} g_{m2}}) + (\frac{C_{iss3}}{g_{m3}} + \frac{C_{iss4}}{g_{m4}})} \quad (2.58)$$

where $K_1 = C_{iss3}C_{oss3} - C_{gd3}^2$ and $K_2 = C_{iss4}C_{oss4} - C_{gd4}^2$ and in the steady state the $(\frac{di_d}{dt})$ of drain current is given by Eq.2.59

$$\frac{di_d}{dt} = \frac{-(i_{g3} + i_{g4})}{\frac{C_{iss3}}{g_{m3}} + \frac{C_{iss4}}{g_{m4}}} \quad (2.59)$$

Due to the $\frac{di_d}{dt}$, there will be a $L_p \frac{di_d}{dt}$ drop across the parasitic inductance (L_p) given by Eq.2.60. This leads to overshoot in the device voltage during the current fall interval as shown in Fig.2.12.

$$v_{ds3} + v_{ds4} = V_{DC} + v_{lp} \quad (2.60)$$

Once the current falls to zero and the load current (I_L) is completely transferred to the top diodes, the turn off transient is completed. The gate to source voltage (v_{gs}) of the series connected SiC MOSFETs reach to the negative clamp voltage ($-V_{EE}$) as shown in Fig.2.12.

2.3.4 Turn off switching transient at lower load current

Fig.2.17 shows the turn off transient of series connected SiC MOSFETs at lower load current condition. In low load current condition, the channel current reduces to zero before the current fall region starts. Due to the reduction in the channel current, the voltage rise entirely depends on the load current flowing through the output capacitance of the device. This phenomenon can be explained through equivalent circuit model as shown in Fig.2.18. After the delay time at t_{f1} instant, the gate to source voltage (v_{gs3}) of S_3 reaches the Miller plateau region and the voltage rise ($\frac{dv}{dt}$) begins. At t_{f2} instant, the gate to source voltage (v_{gs4}) of S_4 reaches the Miller plateau region and the ($\frac{dv}{dt}$) of S_4 begins. It can be seen from Fig.2.18, the miller current i_{Cgd3} and i_{Cgd4} take part of the load current(I_L). The other part of the current i_{Cds3} and i_{Cds4} charge the output capacitance. Due to this, the channel current i_{ch3} and i_{ch4} reduce and fall to a very low value at the beginning of the voltage rise ($\frac{dv}{dt}$) region. The voltage rise ($\frac{dv}{dt}$), in this

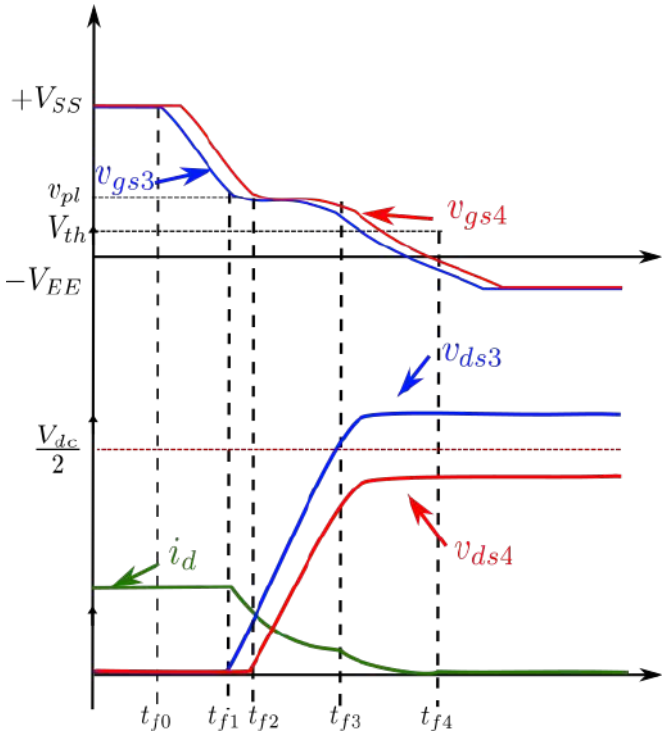

Fig. 2.17: Turn off transient at lower load current

region can be derived by applying KCL at the drain node.

$$I_L = C_{oss3}\frac{dv_{ds3}}{dt} + C_p\frac{d(v_{ds3} + v_{ds4} - V_{DC})}{dt} \tag{2.61}$$

$$I_L = C_{oss4}\frac{dv_{ds4}}{dt} + C_p\frac{d(v_{ds3} + v_{ds4} - V_{DC})}{dt} \tag{2.62}$$

Also

$$C_{oss3}\frac{dv_{ds3}}{dt} = C_{oss4}\frac{dv_{ds4}}{dt} \tag{2.63}$$

From Eq.2.61, Eq.2.62 and Eq.2.63 the voltage rise of the device S_3 and device S_4 is give by

$$\frac{dv_{ds3}}{dt} = \frac{I_L}{C_{oss3} + C_p(1 + \frac{C_{oss3}}{C_{oss4}})} \tag{2.64}$$

$$\frac{dv_{ds4}}{dt} = \frac{I_L}{C_{oss4} + C_p(1 + \frac{C_{oss4}}{C_{oss3}})} \tag{2.65}$$

Eq.2.64. and Eq.2.65 show the voltage rise of device S_3 and S_4. Voltage rise ($\frac{dv}{dt}$) of both devices directly depends on the magnitude of the load current. It is inversely related to its output capacitance and parasitic capacitance of the top diode. Apart from the input

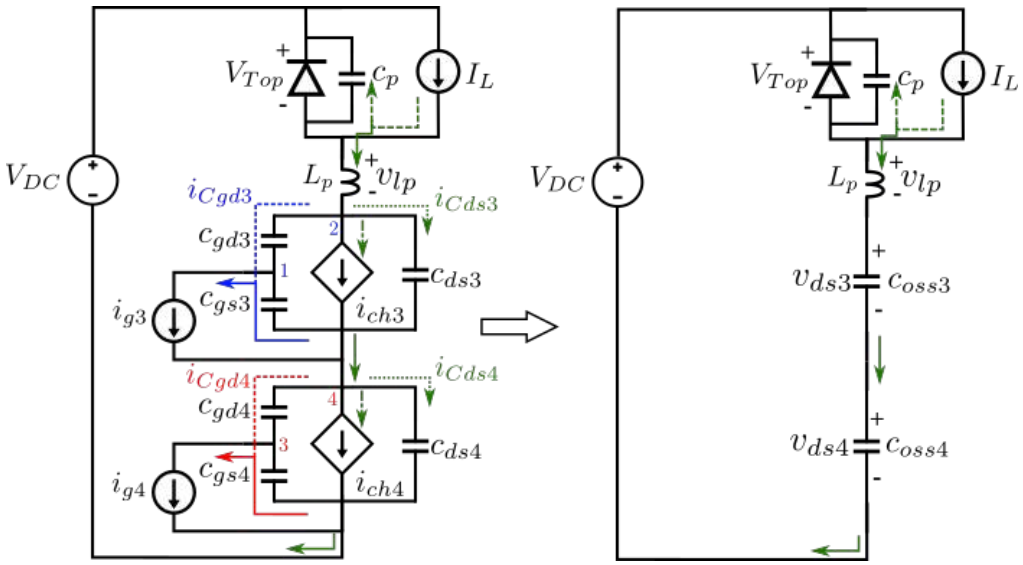

Fig. 2.18: Equivalent circuit model at lower load current

gate pulse delay, the capacitance mismatch among the series connected SiC MOSFETs is critical in determining the slew rate and unbalance during the steady state.

2.3.5 Top diode voltage sharing transient analysis

The top diode is assumed to be ideal in the earlier analysis of turn on and turn off switching transient. But in the practical condition, top device S_1 and S_2 shown in Fig.2.1 has different anti-parallel diode parasitic capacitance C_{p1} and C_{p2}. Due to the difference in the parasitic capacitance, voltage sharing of the diodes will have a steady state voltage difference proportional to the ratio of the capacitance mismatch among the diodes.

The top diode turn off is induced by the turn on transient of bottom series connected device S_3 and S_4. The time interval ($t_{n1} \rightarrow t_{n3}$) is the current rise interval where the load current (I_L) is transferred from diode to the bottom series connected devices. At the end of the interval, the load current is completely transferred to bottom active devices S_3 and S_4. The body diode current of S_1 and S_2 enters into the reverse recovery region. It appears as the current overshoot for the bottom device current. The time interval ($t_{n3} \rightarrow t_{n4}$) is the voltage fall region of the bottom series connected device. During this time the bottom device voltage decreases and the diode enters into the reverse blocking mode and the body diode voltage increases and blocks the entire V_{DC} voltage. As

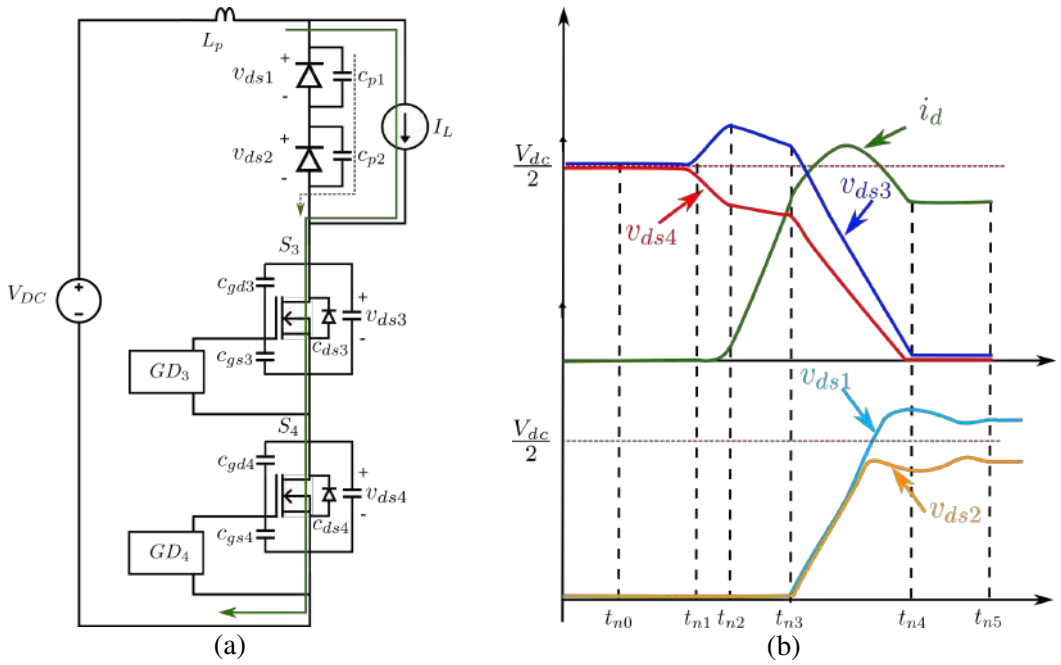

Fig. 2.19: (a) DPT test setup (b) Top diode turn off voltage sharing

mentioned above, the body diode static voltage balancing is mainly decided by the parasitic capacitance of the top series connected devices.

2.3.6 Simulation results of turn off switching transient

The LTspice environment is used to simulate the transients of series connected SiC MOSFETs. Fig.2.20 shows the ideal turn off transient of series connected SiC MOSFETs without gate pulse delay, which is similar to that of single device turn off transient. Here, each series connected device will be blocking ($\frac{V_{DC}}{2}$) during the steady state. The power loop inductance(L_p) is considered to be 100 nH. In order to simulate the practical turn off transient, the gate pulse instant of one of the device is delayed by 10ns. Due to the delay time, device (S_3) reaches the Miller plateau voltage much earlier than the device (S_4). The device drain to source voltage (v_{ds3}) rises by the time the other device gate voltage reaches the plateau voltage. Now, there exists a difference in the transient rise region which will lead to steady state difference in the voltage. Fig.2.21 shows the simulation result of turn-off transient with delay time. It can be observed a static difference of 260V in the steady state.

Fig.2.22 shows the turn off transient with lower load current. It can be seen that as the load current (I_L) is low and the voltage rise ($\frac{dv}{dt}$) of the device S_3 and S_4

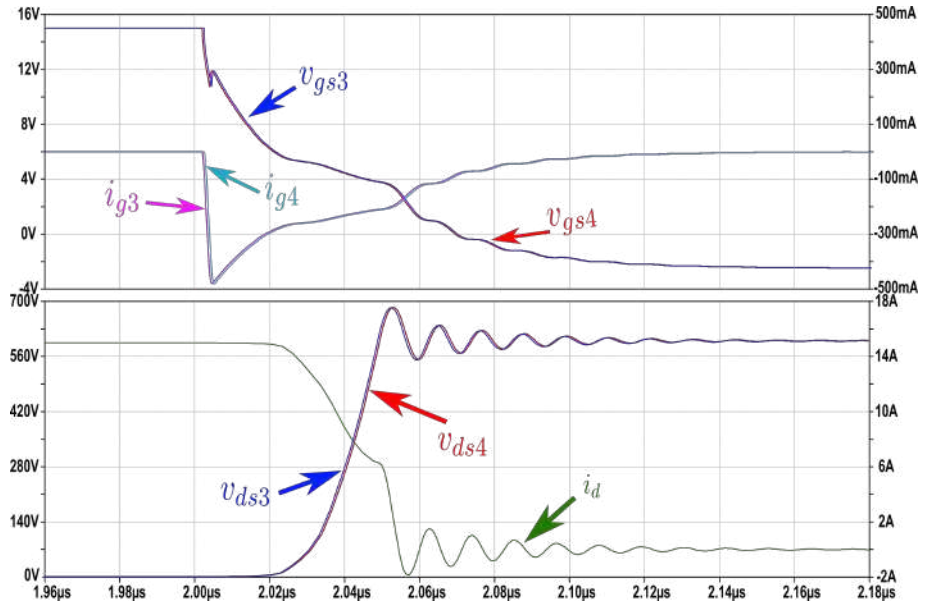

Fig. 2.20: Simulation result of turn off transient without delay(Voltage scale: 140V/div, Current scale: 4A/div and time scale: 20ns/div)

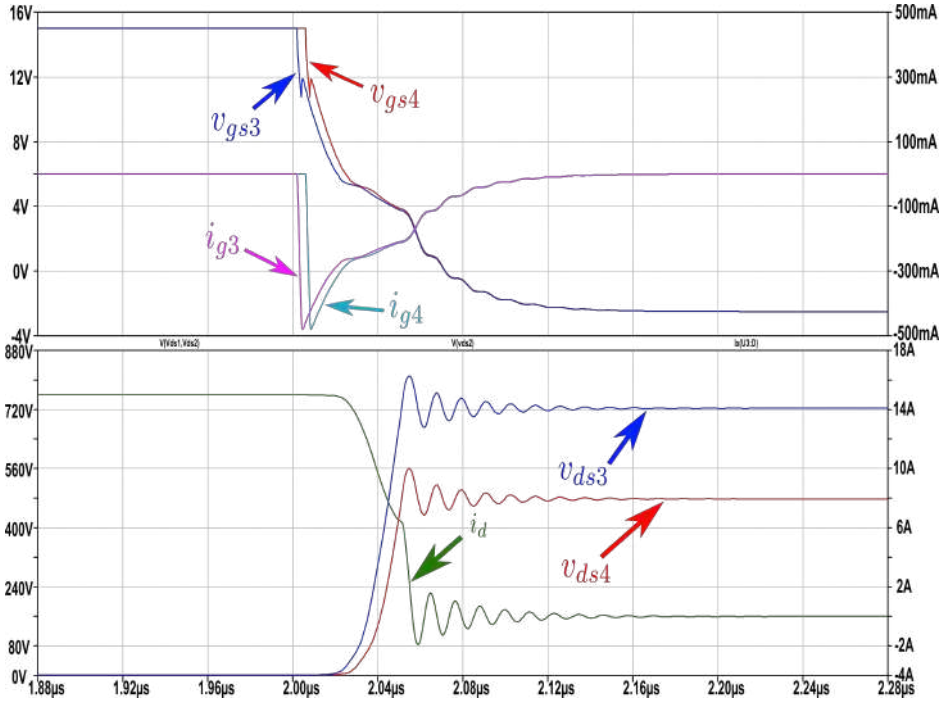

Fig. 2.21: Simulation result of turn off transient with delay (Voltage scale: 160V/div, Current scale: 4A/div and time scale: 40ns/div)

are naturally slowed down as shown from the analysis. The device current (i_d) also reduces in the voltage rise region. The static difference in the steady state voltage balancing is observed to be 90V. Fig.2.23 shows the body diode voltage balancing. In order to simulate the practical condition, the parasitic capacitance across the top series

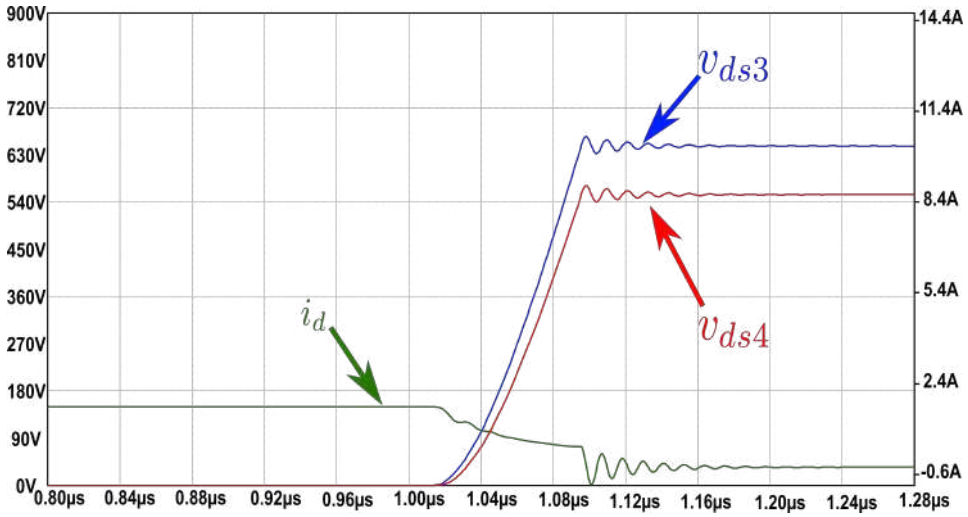

Fig. 2.22: Simulation result of turn off transient with low current (Voltage scale: 90V/div, Current scale: 3A/div and time scale: 40ns/div)

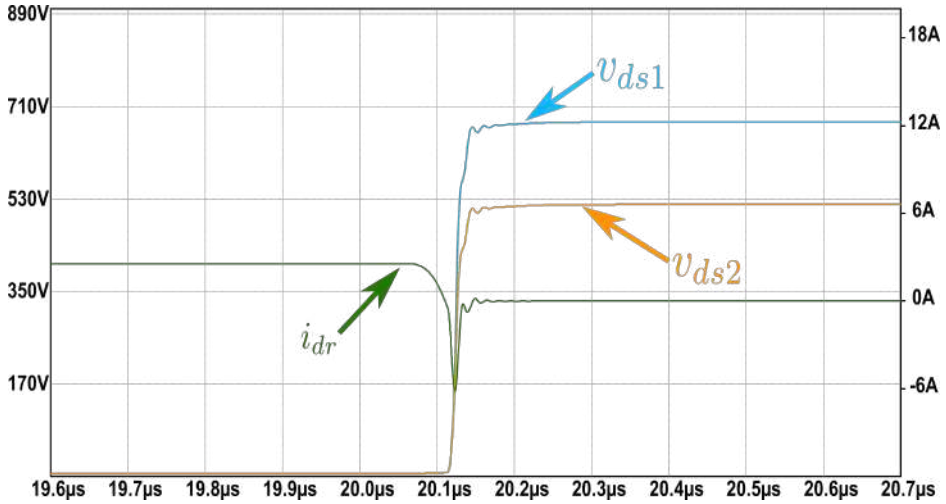

Fig. 2.23: Simulation result of turn off transient of body diode (Voltage scale: 180V/div, Current scale: 6A/div and time scale: 100ns/div)

connected device is added in the ratio of 1:3. This simulates the practical condition and the body diodes voltage of the device S_1 and S_2 are presented. The body diode capacitance of device S_1 is lesser compared to the device S_2. The static difference of 140V is observed between v_{ds1} and v_{ds2}, i_{dr} is the current flowing through the top series connected devices body diode.

2.4 CONCLUSION

This chapter explains the modelling and analysis of switching transients in series connected SiC MOSFETs. The simulation was carried out using a series connected SiC

MOSFET as the Device Under Test (DUT) in a Double Pulse Test(DPT) setup. The turn on modelling and analysis include gate pulse delay and device parameters mismatch. A turn on over voltage will be present in one of the series connected SiC MOSFETs. The relationship between turn on over voltage and input gate current is also established to gain insight into the over voltage phenomenon. Similarly, turn off modelling and analysis reveal the voltage imbalance among series connected devices and the variation of load current influencing the voltage imbalance. Under light load conditions, the device voltage rise is solely determined by the device output capacitance. In addition, the equivalent model for the light load condition is also presented. A series connected SiC MOSFETs body diode voltage imbalance occurs when the complementary switch in the same phase leg is turned on. As a result, the body diodes that share unequal capacitance among the series connected devices will exhibit voltage imbalance.

CHAPTER 3

Active Gate Control Technique for series connected SiC MOSFETs

3.1 INTRODUCTION

This chapter discusses the control of turn on and turn off transients in series connected SiC MOSFETs. An active gate driver based gate current control is presented to resolve the problem of voltage imbalance in series connection. This chapter includes separate turn on and turn off control for voltage balancing. The proposed control techniques for voltage balancing require only device drain to source (v_{ds}) voltage information. The proposed control method achieves the least static voltage imbalance. A closed loop control technique for varying load current conditions is proposed to achieve minimum static imbalance among series connected devices operating at low load current conditions. The voltage balancing of SiC MOSFET body diodes is also critical for the operation of any converter. A partial turn on based active gate control is proposed to control the voltage imbalance of the body diode.

3.2 PROPOSED TURN ON CONTROL TECHNIQUE

In order to explain the proposed turn on control, the gate pulse of AGD_4 is delayed by t_d with respect to AGD_3 in Fig.3.1. Due to this delay in the gate pulse instant, one of the device S_3 turns on much earlier than the other device S_4. The turn on of device S_3 causes the channel to form, which will induce an additional overshoot in S_4. In order to restrict the voltage rise due to the mismatch in the gate pulse instant, the proposed control technique consists of three switching stages namely ON Stage-1, ON Stage-2 and ON Stage-3 as shown in Fig.3.2. ON Stage-1 and ON Stage-2 are switched current source stages driven by S_{on1} and S_{on2} control signals. ON Stage-3 is the switched voltage source stage driven by S_{on3} control signal. I_{on1} and I_{on2} are the magnitude of the switched current source (ON Stage-1 and ON Stage-2) and R_{g_on} is the resistance of

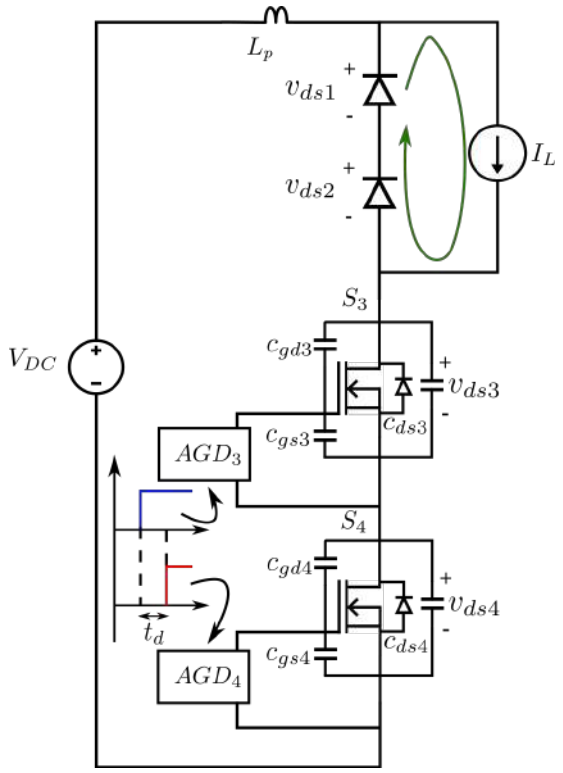

Fig. 3.1: DPT setup of series connected SiC MOSFET with delay

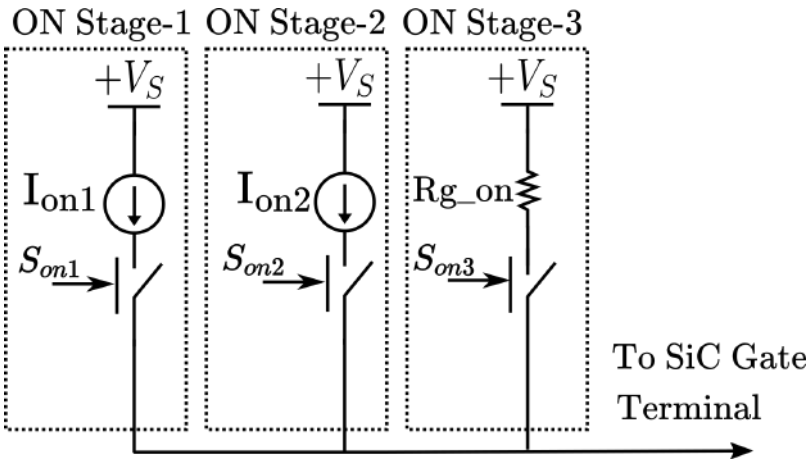

Fig. 3.2: Proposed turn on control stages

the switched voltage source (ON Stage-3) stage. Fig.3.3a shows the switching transient of the proposed turn on control.

Operation during N1 subinterval($t_{n0} - t_{n4}$): Fig.3.3a shows the switching transient of the proposed turn on control. The load current is assumed to be freewheeling through the top diode. The AGD_3 of device S_3 and AGD_4 of device S_4 receives the gate pulse at t_{n0} and t_{n1} instant respectively. Upon receiving the turn on signal, the AGDs start

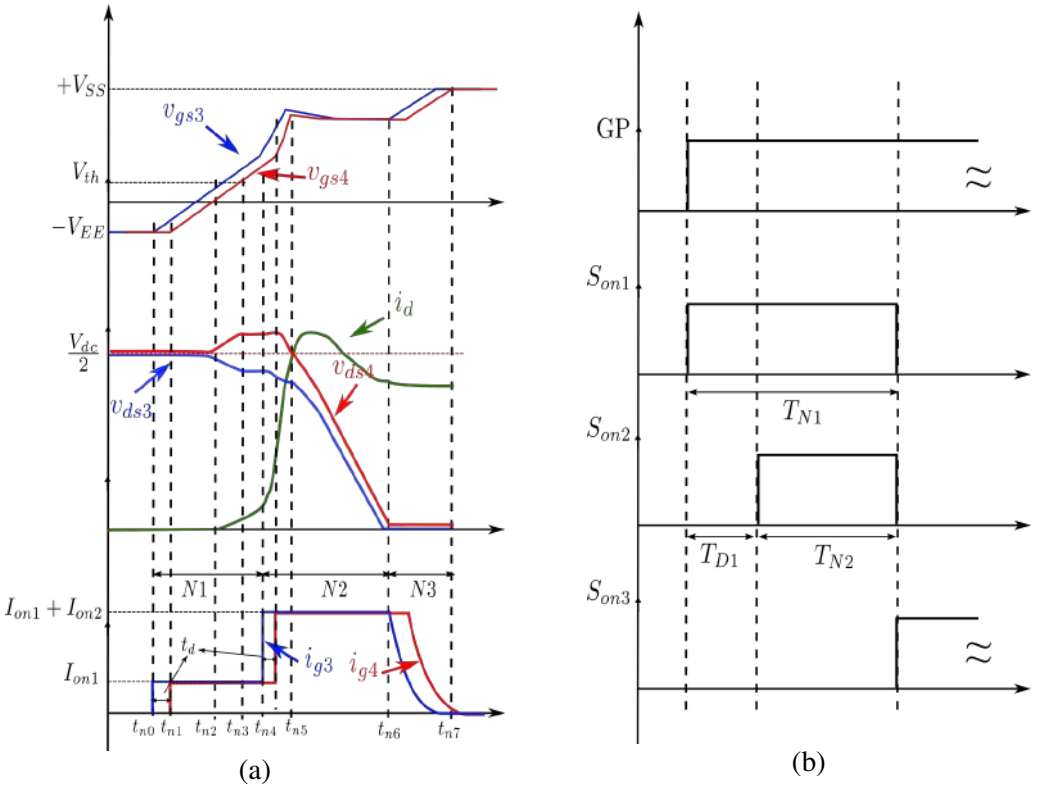

Fig. 3.3: (a) Switching transient of proposed turn on control stage (b) Control signal to the turn on switching stages

charging their respective input gate capacitance (C_{iss}) with a constant gate current I_{on1} of On Stage-1 (t_{n0} and t_{n1} instants in Fig.3.3a). At t_{n2} instant, the device S_3 reaches the threshold voltage, and the device channel current is formed. Due to this, the drain to source voltage (v_{ds4}) of S_4 starts increasing, as explained in the previous chapter. The increase in drain to source voltage v_{ds4} of S_4 causes the drain to source voltage v_{ds3} of S_3 to reduce (as per the KVL). Also, the sum of the device voltages will always be equal to the DC bus voltage (V_{DC}). The maximum allowable overvoltage mainly decides the magnitude of I_{on1} (V_{onov} above the blocking voltage $\frac{V_{dc}}{2}$) across the device. The Miller charge Q_{gd} is responsible for the overvoltage in this region. Lower Q_{gd} charge results in lesser overvoltage.

$$I_{on1}T_{N1} = C_{gd}V_{onov} \tag{3.1}$$

From the above equation, the time duration of On Stage-1 is controlled by S_{on1} control signal as shown in Fig.3.3b. The time duration T_{N1} and maximum allowable over voltage (V_{onov}) are selected such that maximum delay time is accommodated. The

magnitude of the current source of On Stage-1 is driven low to limit the overvoltage caused by the delay in channel current formation. At t_{n3} instant, device S_4 also reaches the threshold voltage and further increases in the device drain to source voltage (v_{ds4}) is restricted by its channel formation. During this region, both devices are in On Stage-1. After fixed duration time T_{D1} shown in Fig.3.3b, the AGD_3 of device S_3 switches to On Stage-2 at the end of t_{n4} instant and concludes the operation of N1 subinterval.

Operation during N2 subinterval($t_{n4} - t_{n6}$): At t_{n4} instant, AGD_3 of device S_3 switches to On Stage-2 with higher current magnitude of I_{on2}. During this time, the gate to source voltage v_{gs3} of S_3 increases at a faster rate with applied higher current magnitude of I_{on2}. The increase in the gate to source voltage v_{gs3} causes the channel resistance of device S_3 to reduce. However, the device S_4 has not switched to On Stage-2 and still has the higher channel resistance and makes the current rise ($\frac{di}{dt}$) slower in this delay time t_d. After the delay time t_d, the AGD_4 of device S_4 also switches to On Stage-2 with higher current magnitude of I_{on2}. The magnitude of I_{on2} is selected based on the required current rise ($\frac{di}{dt}$) and voltage fall ($\frac{dv}{dt}$) of the device.The gate current injected by AGD_3 of device S_3 and AGD_4 of device S_4 is given by

$$i_{g3} = I_{on1} + I_{on2} \tag{3.2}$$

$$i_{g4} = I_{on1} + I_{on2} \tag{3.3}$$

The steady state $\frac{di}{dt}$ of the series connected SiC MOSFETs (from chapter 2 turn on analysis) is given by Eq.3.4

$$\frac{di}{dt} = \frac{i_{g3} + i_{g4}}{\frac{C_{iss3}}{g_{m3}} + \frac{C_{iss4}}{g_{m4}}} \tag{3.4}$$

If C_{iss3} = C_{iss4} = C_{iss} and g_{m3} = g_{m4} = g_m, then the above equation can be represented as

$$\frac{di}{dt} = (i_{g3} + i_{g4})\frac{g_m}{2C_{iss}} \tag{3.5}$$

During the current rise region, the drain to source voltage (v_{ds}) of S_3 and S_4 are

slightly reduced due to the leakage inductance $L_p\frac{di}{dt}$ drop. At t_{n5} instant, the device current reaches the load current I_L and top diodes will be entering into the reverse blocking mode. This will initiate the voltage fall region of the device. The voltage fall of the device is completed at t_{n6} instant.

The steady state $\frac{dv}{dt}$ of the series connected SiC MOSFETs (from chapter 2 turn on analysis) is given by Eq.3.6

$$\frac{dv}{dt} = -\frac{(i_{g3} + i_{g4})}{C_{gd}} \tag{3.6}$$

From Eq.3.5 and Eq.3.6 the magnitude of I_{on2} and time duration T_{N2} is selected to get the desired current rise $\frac{di}{dt}$ and voltage fall $\frac{dv}{dt}$ in the series connected devices.

Operation during N3 subinterval$(t_{n6} - t_{n7})$: During this subinterval, after the fixed turn on time duration (T_{N2}) (On Stage-2 operation shown in Fig.3.3b), the On Stage-3 which is a switched voltage source is applied for the remaining turn on gate pulse duration. This stage helps in clamping both the device gate to source voltage (v_{gs}) to recommended clamping voltage of +V_{SS}, which in turn helps in reducing the on state resistance of the device.

3.2.1 Simulation results of proposed turn on control

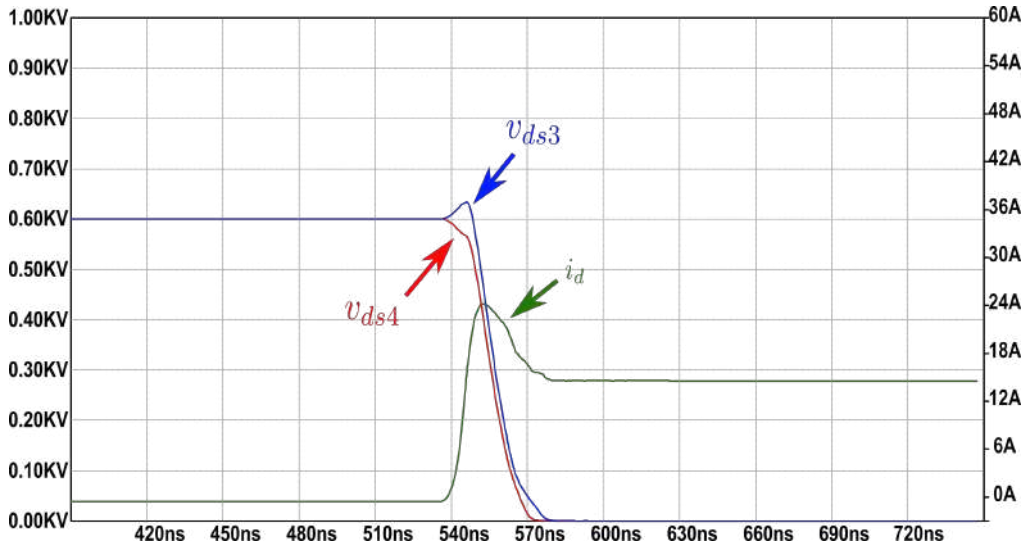

Fig. 3.4: Simulation results of proposed turn on control with lower current (Voltage scale:100V/div, Current scale: 6A/div and time scale: 30ns/div)

The proposed turn on control technique is simulated using LTspice simulation to

validate the proposed control technique. The proposed turn on stages are modelled as ideal current sources. Two cases are considered to ensure validity of the proposed control technique at all load conditions. In the first case, the load current is set at 15A. In the second case, the load current is set at 25A. From Eq.3.1, Eq.3.5 and Eq.3.6 the desired $\frac{di}{dt}$, $\frac{dv}{dt}$ is selected to be 1.3A/ns and 21V/ns. Based on this, the average value of gate current can be calculated. By using the average value, the magnitude for ON Stage-1 and ON Stage-2 can be selected. Fig.3.4 shows the simulation results of proposed turn on control with lower load condition. Delay between gate pulse instant of series connected devices are assumed to be 10ns in this case. As per the proposed control technique, at first the device S_4 turns on. Due to the gate pulse mismatch, the drain to source voltage (v_{ds3}) of S_3 increases. As the turn on stage current magnitude for ON Stage-1 is kept low (110mA), the drain to source voltage (v_{ds3}) of S_3 is also limited to 60V peak. The second stage, ON Stage-2 is applied with higher current magnitude (120mA). This current will be responsible for the current rise ($\frac{di}{dt}$) and voltage fall ($\frac{dv}{dt}$) during the turn on transients.

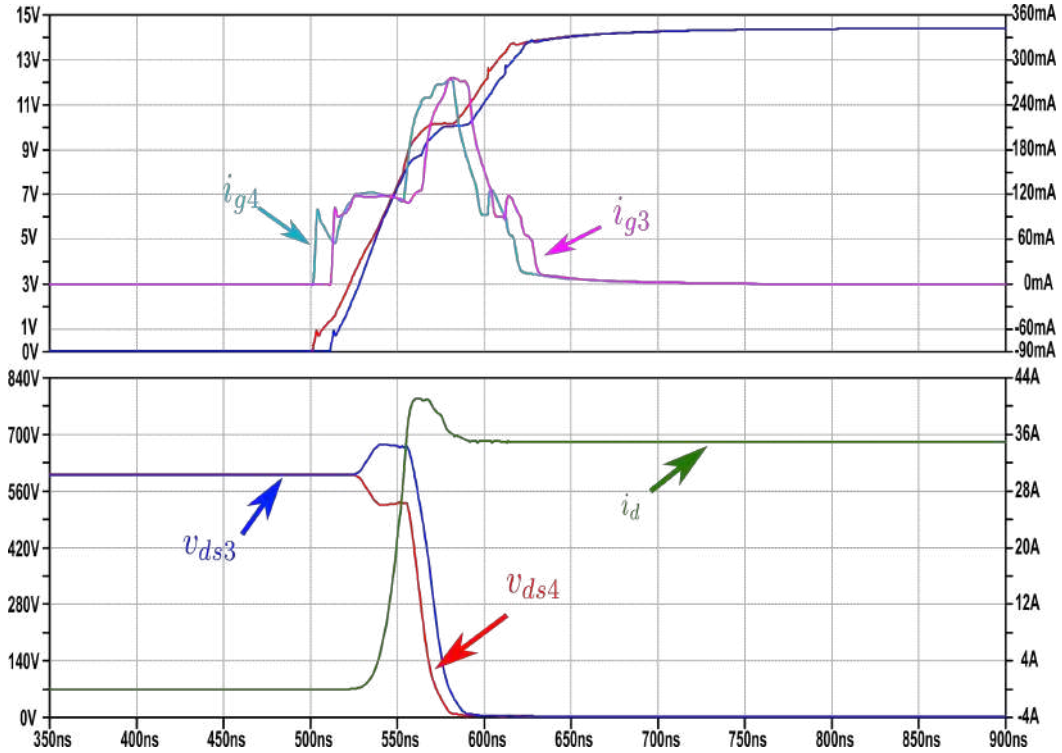

Fig. 3.5: Simulation results of proposed turn on control with higher current (Voltage scale:100V/div, Current scale: 6A/div and time scale: 30ns/div)

The proposed turn on control achieves total turn on switching time of 45ns. The simulation results of turn on transient of series connected SiC MOSFET at higher load current are shown in Fig.3.5. In this case, only the load current is increased while all other control parameters of turn on stage remain unchanged. The results show that the peak overvoltage clamping of 60V and the total turn on switching time of 50ns. The simulation results presented above validate the proposed turn on control technique for series connected SiC MOSFETs.

3.3 PROPOSED TURN OFF CONTROL TECHNIQUE

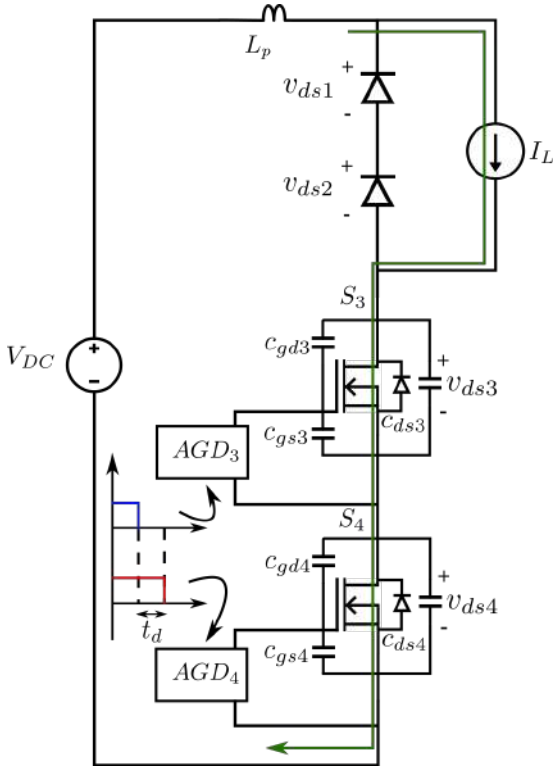

Fig. 3.6: DPT setup of series connected SiC MOSFET with delay

In order to demonstrate the proposed turn off control, gate pulse instant of AGD_4 is delayed by time (t_d) as compared to AGD_3. Fig.3.6 shows the Double Pulse Test (DPT) circuit of series connected SiC MOSFETs. Device S_3 and S_4 are turned off simultaneously without any delay. The device drain to source voltage (v_{ds}) exactly blocking at $\frac{V_{DC}}{2}$. In case of 'n' devices connected in series, the blocking voltage will be $\frac{V_{DC}}{n}$. Due to the presence of delay in the turn off instant of the device S_4, the device S_3 turns off much earlier than the device S_4, which causes the device S_3 to block

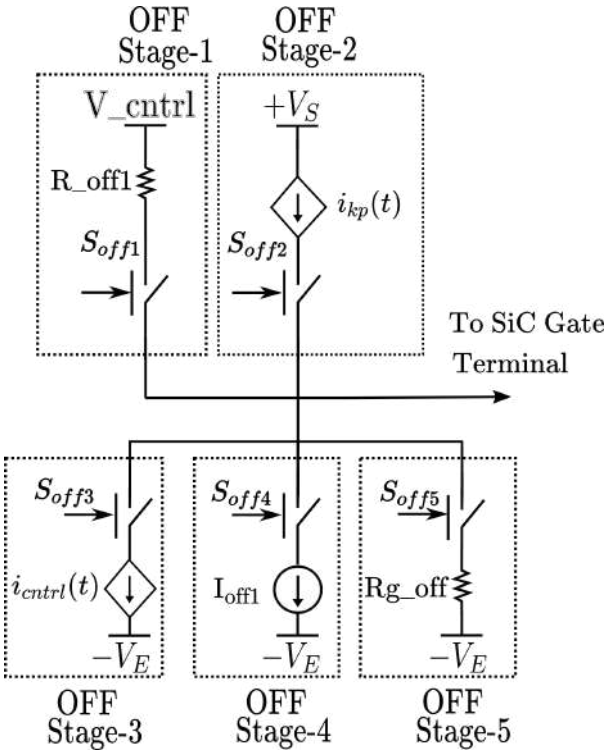

Fig. 3.7: Proposed turn off control stages

higher voltage (more than $\frac{V_{DC}}{2}$). This can lead to considerable amount of power loss. The blocking voltage may exceeds higher than the device rated voltage and can lead to failure. The main objective of the turn off control is to achieve minimum voltage imbalance in static as well as in the dynamic condition. Also, the proposed control should limit the device blocking voltage (In case of large mismatch in the gate pulse instants) well below the breakdown voltage. Fig.3.7 shows the proposed turn off control stages. They are mainly classified into three sub-control stages namely low frequency control, high frequency control and diode voltage balancing control.

3.3.1 High frequency turn off control technique

High frequency control stage is delicately used for higher load current conditions (greater than 5A). The Off Stage-2 and Off Stage-4 are operated together for high frequency control. The Off Stage-2 is the switched controlled current source. The magnitude of the current source i_{Kp} is decided by the device drain to source voltage (v_{ds}). The Off Stage-4 is the switched current source of constant magnitude I_{off1}. The effective applied gate current during the high frequency control for device S_3 and S_4 is

given by Eq.3.11.

where i_{Kp} for device S_3 and S_4 is given by

$$i_{Kp3} = \begin{cases} K_p\left(v_{ds3} - \frac{V_{DC}}{2}\right) & \text{for} \quad v_{ds3} \geq \frac{V_{DC}}{2} \\ 0 & \text{otherwise} \end{cases} \tag{3.7}$$

$$i_{Kp4} = \begin{cases} K_p\left(v_{ds4} - \frac{V_{DC}}{2}\right) & \text{for} \quad v_{ds4} \geq \frac{V_{DC}}{2} \\ 0 & \text{otherwise} \end{cases} \tag{3.8}$$

$$i_{g3} = -I_{off1} + i_{Kp3} \tag{3.9}$$

$$i_{g4} = -I_{off1} + i_{Kp4} \tag{3.10}$$

$$\begin{aligned} i_{g3} &= -\left[I_{off1} - K_p\left(v_{ds3} - \frac{V_{DC}}{2}\right)\right] \quad \text{during} \;\; t_{f4} \leq t \leq t_{f6} \\ i_{g4} &= -\left[I_{off1} - K_p\left(v_{d42} - \frac{V_{DC}}{2}\right)\right] \quad \text{during} \;\; t_{f5} \leq t \leq t_{f6} \end{aligned} \tag{3.11}$$

The high frequency control can be explained from the switching transient of the proposed turn off control. The turn off transient can be divided into three subinterval namely F1, F2 and F3 shown in Fig.3.8a.

Operation during F1 subinterval$(t_{f0} - t_{f4})$: The AGD_3 of device S_3 and AGD_4 of device S_4 receive gate pulses at t_{f0} and t_{f1} instants respectively. The Off Stage-2 and Off Stage-4 are simultaneously turned on with S_{off2} and S_{off4} control signal as shown in Fig.3.8b. From Eq.3.7 it is clear that the i_{Kp3} and i_{Kp4} current are valid only if the respective device crosses $\frac{V_{DC}}{2}$. Below $\frac{V_{DC}}{2}$, the value of i_{Kp3} and i_{Kp4} is 0. Substituting the value of i_{Kp3} and i_{Kp4} in Eq.3.9 and Eq.3.10, the value of gate current can be obtained as

$$i_{g3} = -I_{off1} \tag{3.12}$$

$$i_{g4} = -I_{off1} \tag{3.13}$$

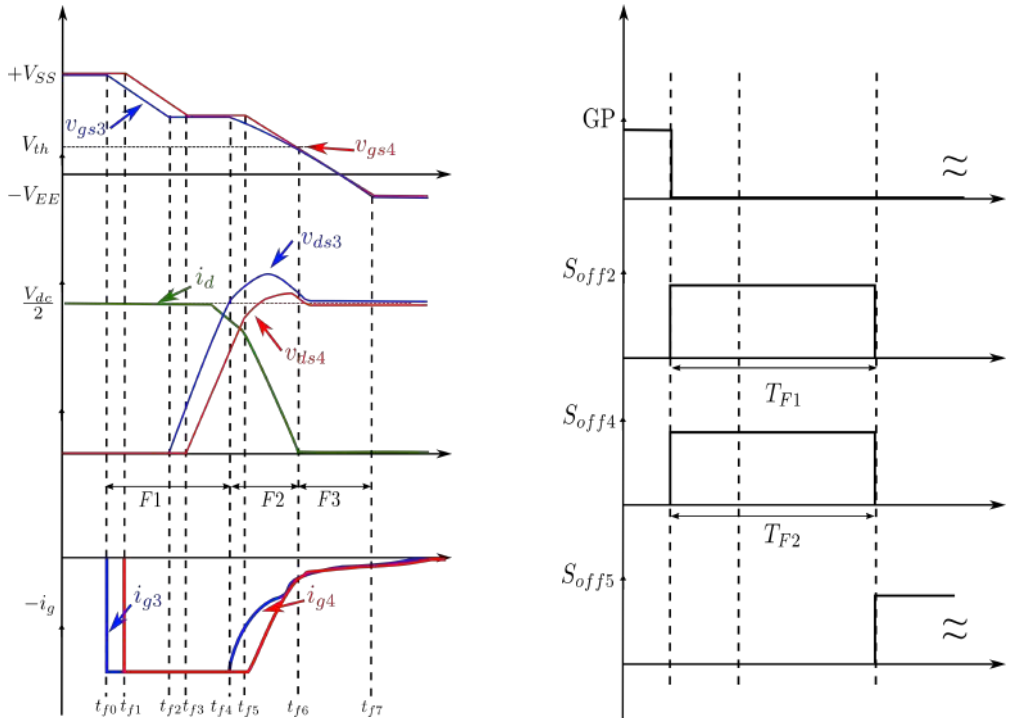

Fig. 3.8: (a) Switching transient of proposed turn off high frequency control (b) Stage control signal to the turn off switching stages

From Eq.3.12 and Eq.3.13 it is clear that upon receiving the turn off signal, both the AGDs start discharging their respective input gate capacitance with a constant gate current I_{off1} by applying Off Stage-4 (t_{f0} and t_{f1} instants in Fig.3.8a). The device S_3 and S_4 reach the Miller plateau voltage and start experiencing voltage rise at t_{f2} and t_{f3} instants respectively. The turn off process of S_4 is delayed compared to device S_3, the drain to source voltage v_{ds3} of device S_3 reaches $\frac{V_{DC}}{2}$ at t_{f4} instant much earlier than device S_4. This is the end of F1 subinterval.

Operation during F2 subinterval$(t_{f4} - t_{f6})$: In the F1 subinterval, device S_3 reaches $\frac{V_{DC}}{2}$ and as per the Eq.3.7, the Off Stage-2 stage current(i_{Kp3}) of device S_3 is activated. At t_{f4} instant, as the device voltage v_{ds3} increases, the Off Stage-2 current also increases. This results in reduction of net gate current i_{g3} as shown in Eq.3.9. The steady state relationship between gate current and $\frac{dv}{dt}$ from chapter 2 is given by Eq.3.14.

$$\frac{dv}{dt} = \frac{i_g}{C_{gd}} \tag{3.14}$$

From Eq.3.14, it is clear that the reduction in the gate current results in reduction

on the $\frac{dv}{dt}$ of the device voltage v_{ds3} as shown in Fig.3.8a. At t_{f5} instant, the device S_4 reaches close to $\frac{V_{DC}}{2}$. By that time sum of device voltages reach V_{DC}, the top diodes turn on and the current fall region starts. The device S_4 also enters into Off Stage-2 stage after crossing $\frac{V_{DC}}{2}$. The i_{Kp4} current of device S_4 is activated in this duration. During $t_{f4} - t_{f6}$ interval, both the device gate current are controlled by Off Stage-2 and Off Stage-4 as given by Eq.3.11. Further increase in the device voltage is restricted by i_{Kp} current, injected by both the AGDs. The current fall ($\frac{di}{dt}$) causes additional parasitic leakage drop, which appears as the voltage overshoot across the series connected devices. The value of K_p and I_{off1} is selected in such a way that it limits the peak voltage (v_{ds_peak}), and desired voltage rise and current fall are achieved with voltage balancing. In any given condition, the peak voltage stress across each switching device is determined by the values of I_{off1} and K_p. The relationship between Off Stage-2, Off Stage-4, and gate current is as follows.

$$i_g = -\left[I_{off1} - K_p\left(v_{ds\_peak} - \frac{V_{DC}}{2}\right)\right] \tag{3.15}$$

As per Eq.3.15, the peak voltage stress v_{ds_peak} occurs when the gate current becomes zero (as v_{ds} cannot increase when $i_g = 0$). The value of peak voltage can be obtained by setting the value of $i_g = 0$ in Eq.3.15. The corresponding expression for v_{ds_peak} is as follows.

$$v_{ds\_peak} = \frac{I_{off1}}{K_p} + \frac{V_{DC}}{2} \tag{3.16}$$

Using Eq.3.16, the values of I_{off1} and K_p are selected such that the peak voltage stress is within the rated voltages of the switching devices. In addition to this, I_{off1} and K_p values are also responsible for determining the $\left(\frac{di}{dt}\right)$ value during turn off transient (current fall region). Current fall $\left(\frac{di}{dt}\right)$ from steady state relationship is expressed in Eq.3.17.

$$\frac{di}{dt} = \frac{g_m i_g}{C_{iss}} \tag{3.17}$$

The device drain to source voltage reaches above $\frac{V_{DC}}{2}$ during the current fall region $\frac{di}{dt}$. The parasitic inductance L_p is responsible for the peak voltage as given in Eq.3.18.

$$i_g = -\left[I_{off1} - K_p\left(v_{ds\_peak}\right)\right] \tag{3.18}$$

The relationship between $\frac{di}{dt}$, I_{off1} and K_p values can be expressed in Eq.3.19 using Eq.3.17 and Eq.3.18.

$$I_{off1} - K_p L_p\left(\frac{di}{dt}\right) = \left(\frac{di}{dt}\right)\frac{C_{iss}}{g_m} \tag{3.19}$$

Using Eq.3.16 and Eq.3.19 the values of I_{off1} and K_p can be estimated.

$$K_p = \frac{C_{iss}\left(\frac{di}{dt}\right)}{g_m\left(v_{ds\_peak} - 0.5V_{DC} - L_p\left(\frac{di}{dt}\right)\right)} \tag{3.20}$$

$$I_{off1} = \frac{2C_{iss}\left(\frac{di}{dt}\right)\left(v_{ds\_peak} - 0.5V_{DC}\right)}{g_m\left(L_p\left(\frac{di}{dt}\right) + 0.5V_{DC} - v_{ds\_peak}\right)} \tag{3.21}$$

Operation during F3 subinterval($t_{f6} - t_{f7}$): At the end of F2 subinterval both the device S_3 and S_4 are in Off Stage-2. As one of the device voltage v_{ds3} decreases due to Off Stage-2 current, the other device voltage v_{ds4} increases and helps in balancing the device voltage. The time duration T_{F1} and T_{F2} are selected at least twice the desired turn off transient duration. At t_{f6} instant, Off Stage-5 is applied, which will clamp the gate voltage of both the device to negative voltage ($-V_{EE}$) through minimum gate resistance(Rg_off). The Off Stage-5 is turned on after T_{F2} duration and kept on till the end of turn off gate pulse. At higher load currents, the channel current is sufficient enough and the Miller discharge can be controlled from the gate side. By controlling the i_{kp} current combined with I_{off1} current, the effective gate current can be controlled with proportional to the device drain to source voltage. The gate current (i_g) is controlled during the transient time hence the control is termed as high frequency control. In this method, the static voltage difference can exist(i.e. very minimum) in case if large mismatch in the gate pulse instants occurs.

3.3.2 Low frequency turn off control technique

Fig.3.9 shows the turn off transient with the proposed high frequency control for the lower load current conditions. In low load current condition, the device S_3 and

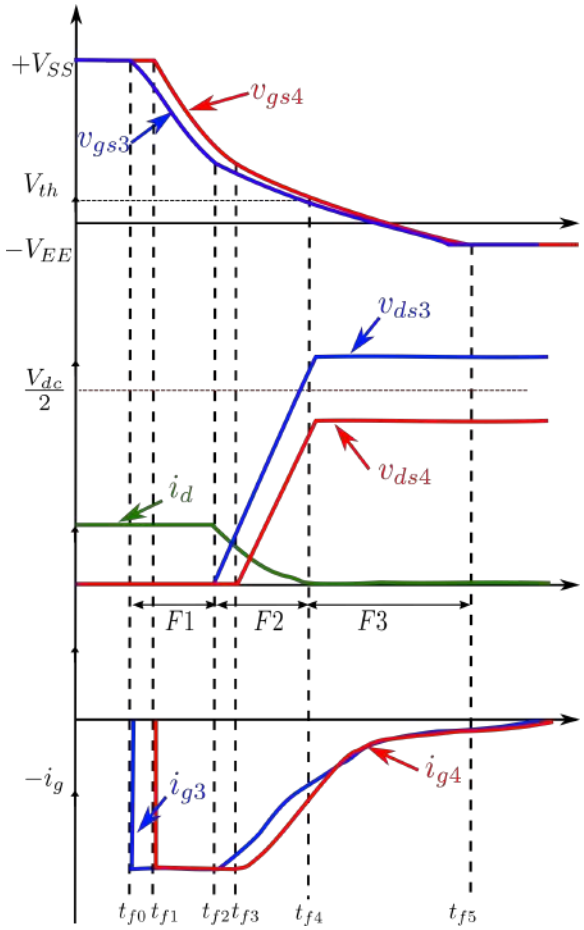

Fig. 3.9: Switching transient of turn off transient during lower current condition

S_4 is turned off at t_{f0} and t_{f1} instant. The gate capacitor of the individual device starts discharging and reaches to the Miller plateau voltage. The device S_3 reaches the Miller plateau at t_{f2} instant and device S_4 reaches the Miller plateau at t_{f3} instant. The voltage rise ($\frac{dv}{dt}$) of the device starts increasing and simultaneously the channel current of the device starts reducing. Due to this, the effective gate current control by the high frequency control stages (Off Stage-2 and Off Stage-4) does not have much effect in the lower current conditions. Low frequency control technique is delicately used for low load current conditions (less than 5A) where the gate does not have tight control over the device ($\frac{dv}{dt}$). The Off Stage-3 is the switched current source used for low frequency control, the $i_{cntrl}(t)$ magnitude is decided by the closed loop controller. The controller senses the static deviation of the device voltage from the reference voltage of ($\frac{V_{DC}}{2}$) during the turn off steady state condition. The error voltage corresponding to the device static difference is fed to the controller to compute the $i_{cntrl}(t)$ magnitude. Once in

every switching cycle, the sample voltage is taken and the bandwidth of the system will be chosen less than the switching frequency. This ensures good steady state response and the control technique is termed as low frequency control. The control signals shown in Fig.3.10b for low load current condition contains the high frequency control signals and the Off Stage-3 is operated along with the other switching stages.

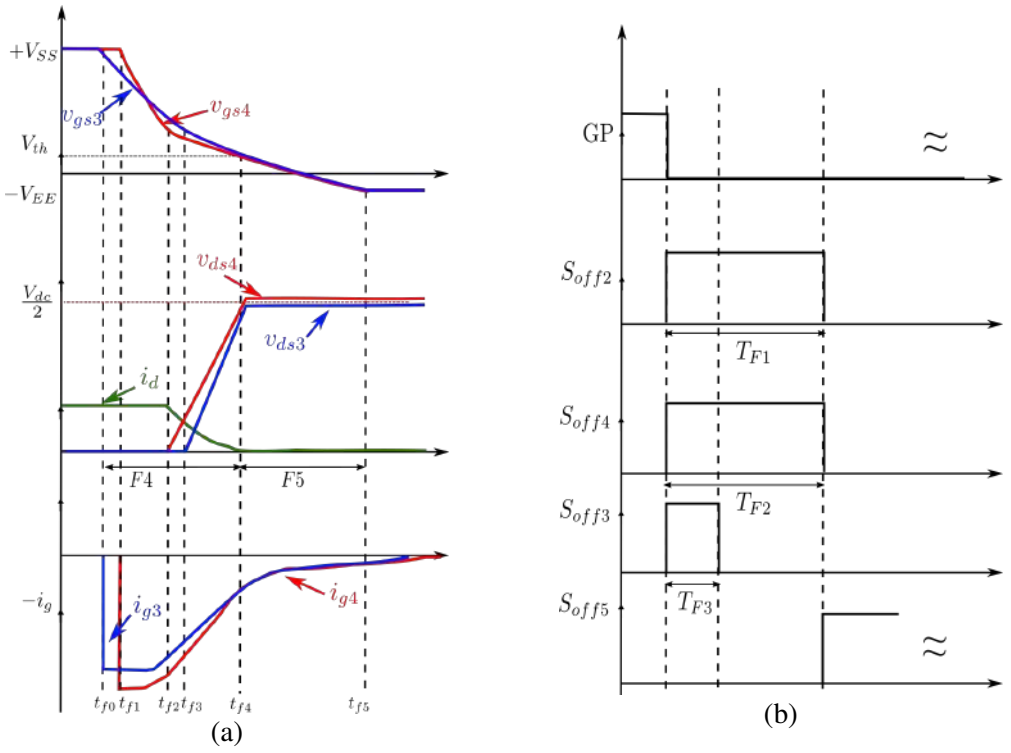

Fig. 3.10: (a) Switching transient of proposed turn off low frequency control (b) Stage control signal to the turn off switching stages

Operation during F4 subinterval$(t_{f0} - t_{f4})$: The AGD_3 of device S_3 and AGD_4 of device S_4 receives gate pulse at t_{f0} and t_{f1} instants respectively. Upon receiving the turn off signal, both the AGDs start discharging their respective gate capacitors with a constant gate current I_{off1} by applying Off Stage-4 at t_{f0} and t_{f1} instant. The controller computes the static voltage difference in every cycle. Based on the deviation in the voltage, the controlled current source $i_{cntrl}(t)$ is applied in the present cycle for T_{F3} duration as shown in Fig.3.10b. This will effectively increase the gate current of device S_4 which can be observed at the beginning of this subinterval. The increase in the gate current causes the gate voltage (v_{gs4}) of S_4 to reach Miller plateau voltage much earlier than the gate voltage (v_{gs3}) of S_3. Due to this, device S_4 turns off earlier than the

device S_3 which will eventually helps in balancing the voltages among the devices.

Operation during F5 subinterval($t_{f4}-t_{f5}$): At t_{f4} instant, the device S_3 and S_4 gate to source voltage will be reaching close to threshold voltage. The effectiveness of the Off stage-2 and Off stage-4 has no significant impact in the low current duration due to the absence of the channel current. At t_{f5} instant, the Off Stage-5 is applied which will clamp the gate voltage of both the device to negative voltage ($-V_{EE}$) through minimum gate resistance(Rg_off).

3.3.3 Closed loop control design

The low frequency control mentioned above is achieved through the proposed closed loop control. Fig.3.11 shows the control block diagram of the proposed closed loop control. $G_c(s)$ represents the PI controller transfer function, $G_{vi}(s)$ represents device transfer function and $H(s)$ represents the feedback gain of the system.

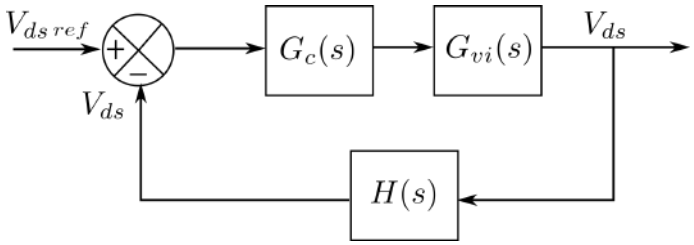

Fig. 3.11: Block diagram of the proposed low frequency control

Detailed derivation of the plant transfer function is given in the Appendix A. The plant transfer function $G_{vi}(s)$ represents the input gate current i_g to device voltage v_{ds} of SiC MOSFET.

$$G_{vi}(s) = \frac{v_{ds}(s)}{i_g(s)} = \frac{a_1 s^3 + b_1 s^2 + c_1 s + d_1}{a_2 s^4 + b_2 s^3 + c_2 s^2 + d_2 s}$$

where the coefficients of the s terms are given below

$a_1 = -L_p C_p C_{gd}$

$b_1 = L_p C_p g_m$

$c_1 = -C_{gd}$

$d_1 = g_m$

$a_2 = K L_p C_p$

$b_2 = L_p C_p g_m C_{gd}$

$c_2 = C_p C_{iss} + K$

$d_2 = g_m C_{gd}$

$K = C_{iss} C_{oss} - C_{gd}^2$

From the above transfer function, the coefficients of the higher order 's' terms which are negligible compared to the other coefficient terms are neglected. The transfer function can be reduced to a lower order which can be used for the simplified analysis.

$$G_{vi}(s) = \frac{c_1 s + d_1}{d_2 s}$$

The above transfer function can be modified as

$$G_{vi}(s) = \frac{\tau_{m1} s + 1}{\tau_{m2} s}$$

where $\tau_{m1} = \frac{c_1}{d_1}$ and $\tau_{m2} = \frac{d_2}{d_1}$

The PI controller transfer function can be represented as

$$G_c(s) = K_p \frac{(1 + \tau_{pi} s)}{\tau_{pi} s}$$

The sensing or the feedback gain is given by

$$H(s) = \frac{1}{1 + \tau_d s}$$

The stability analysis of the closed loop system is mainly decided by the phase margin and bandwidth of the system. If the switching frequency of the system is f_s, then the desired gain cross over frequency can be chosen as $f_c = \frac{f_s}{10}$. The phase angle at the desired gain cross over frequency of the uncompensated system can be estimated or selected from the Bode plot. Let $T_{cu}(s) = G_{vi}(s)$ be the uncompensated transfer function of the plant. The phase margin is given by Eq.3.22.

$$\angle \phi_m = 180^\circ + \angle T_{cu} \tag{3.22}$$

The required phase from the PI controller is calculated by

$$\angle\phi_m - 180^\circ = \angle T_{cu} + \angle G_c \tag{3.23}$$

$$\angle G_c = \angle\phi_m - 180^\circ - \angle T_{cu} \tag{3.24}$$

The phase of the PI compensation can be calculated from Eq.3.25

$$\angle G_c = -90^\circ + \arctan \omega\tau_{pi} \tag{3.25}$$

Combining the Eq.3.24 and Eq.3.25 the value of τ_{pi} can be estimated from Eq.3.26. Here, ω is the required gain cross over frequency.

$$\omega\tau_{pi} = \tan(\angle\phi_m - 90^\circ - \angle T_{cu}) \tag{3.26}$$

The value of K_p can be calculated by setting the loop gain of the system to be 1 at the gain cross-over frequency.

$$|G(s)H(s)| = |T_{cu}(s)||G_c(s)||H(s)| = 1$$

Upon solving the above expression the gain K_p can be determined as

$$K_p = \frac{\omega^2\tau_{pi}\tau_{m2}\sqrt{1+\omega^2\tau_d^2}}{\sqrt{1+\omega^2\tau_{pi}^2}\sqrt{1+\omega^2\tau_{m1}^2}} \tag{3.27}$$

The values of K_p and τ_{pi} are used in the controller design to control the Off stage-3 controlled current $i_{cntrl}(t)$. As demonstrated above controlling the Off stage-3 current, voltage balancing among the series connected devices can be achieved.

Stability of the control loop is investigated in the Matlab simulink environment. The system switching frequency is set to 5 kHz. The model of the derived transfer function is imported into the simulink model. The device data sheet gives device parameters such as input capacitance, output capacitance, and trans conductance (C3M0065100K). The open loop transfer function is plotted and shown in Fig.3.12. As per the above

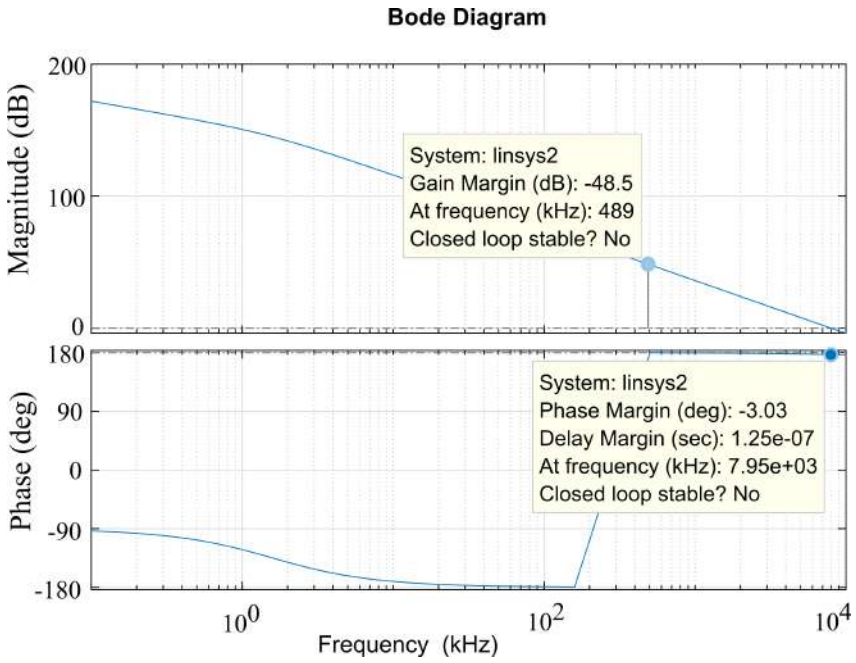

Fig. 3.12: Uncompensated bode plot of open loop transfer function from matlab

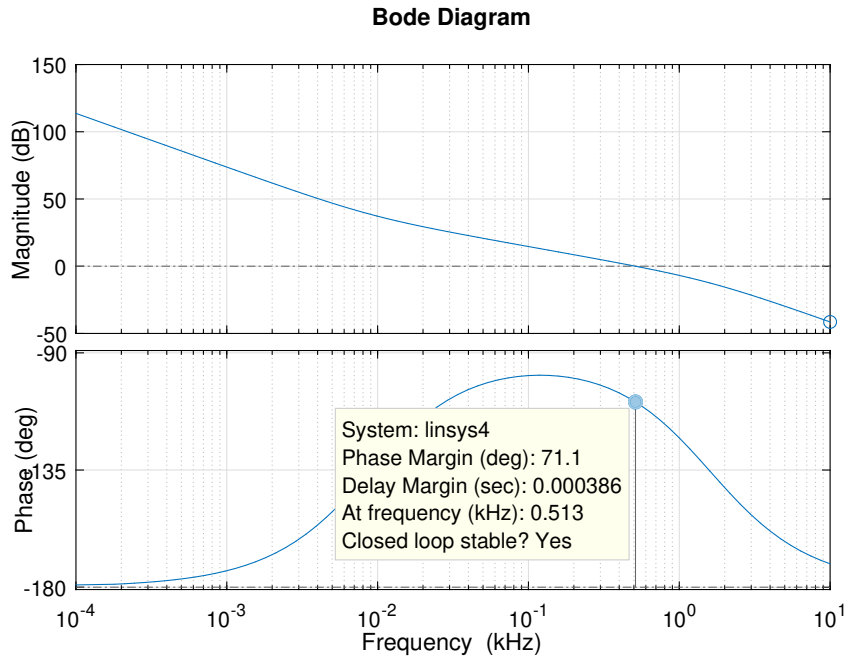

Fig. 3.13: Compensated bode plot of open loop transfer function from matlab using PI tuner

control loop design the required gain cross over frequency is chosen as 500 Hz for the 5 kHz switching frequency of the converter. The phase margin must be above 45° to achieve the minimal overshoot and damping. Based on these criteria, PI controller parameters are tuned to get the compensated Bode plot of open loop transfer function

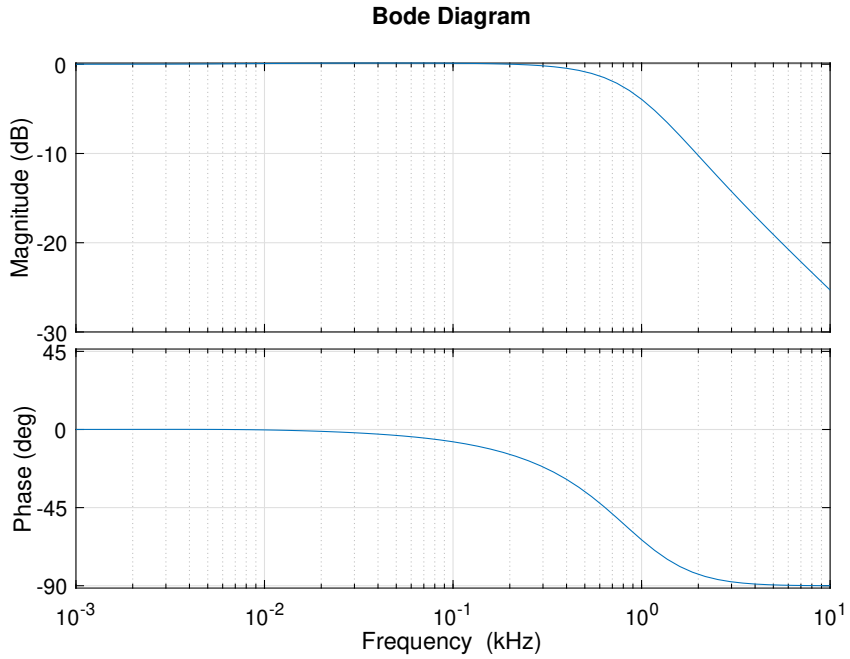

Fig. 3.14: Compensated bode plot of closed loop transfer function from matlab using PI tuner

as shown in Fig.3.13. The compensated system has the phase margin of 71° and cross over frequency at 513 Hz. This ensures the closed loop system is stable. Above 513 Hz, the controller offers attenuation for high frequency signals.

3.3.4 Diode turn off control technique

Body diode conduction occurs when the load current transfers from the device to its body diode during freewheeling time. The device is already turned off with the gate voltage held at a negative maximum. After the dead time, when the other device in the same phase leg is turned on, the body diodes of the series connected devices will go to the reverse blocking mode. During this condition, body diode voltages of the series connected SiC MOSFETs share unequal voltages. The voltage sharing mainly depends on the capacitance formation among the series connected string. Fig.3.15a shows the diode voltage imbalance due to the different parasitic capacitance c_{p1} and c_{p2} of D_1 and D_2 respectively. Off Stage-1 and Off stage-5 are switched voltage source stages which are used to actively control the body diode voltage. The proposed diode control can be subdivided into two region namely D1 and D2 as shown in Fig.3.16a.

Operation during D1 subinterval$(t_{d0} - t_{d2})$: At t_{d0} instant, AGD_1 and AGD_2 of

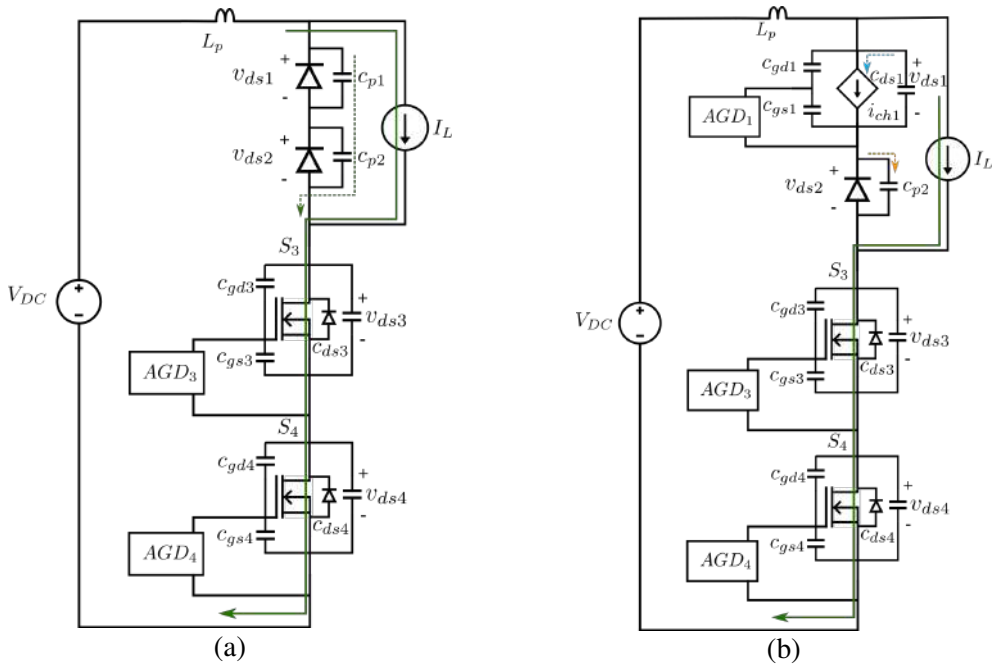

Fig. 3.15: (a) Body diode turn off without control (b) Body diode turn off with proposed control

the device S_1 and S_2 are turned off and the devices start conducting the freewheeling current through its body diode. At t_{d1} instant, the S_3 and S_4 are turned on and the diode current i_{dr} decreases nearly to zero current and enters into the reverse recovery region.

Operation during D2 subinterval$(t_{d2} - t_{d4})$: At t_{d2} instant, the diode enters into reverse blocking mode and the diode voltage of device S_1 and S_2 starts increasing as shown in Fig.3.16a. The steady state voltage of the device v_{ds1} and v_{ds2} is purely decided by the ratio of the capacitance formation across the devices. In this case, device S_1 is assumed to have lower capacitance compared to device S_2. The drain to source voltage v_{ds1} of S_1 blocks higher voltage (more than $\frac{V_{DC}}{2}$) than the device v_{ds2}. In order to balance the diode voltage, the device v_{ds1} and v_{ds2} are compared to the reference voltage $\frac{V_{DC}}{2}$. The device which blocks more than the reference voltage $\frac{V_{DC}}{2}$, is partially turned on to discharge the excess charge into the channel of the same device. The amount of charge to be discharged from the output capacitor can be calculated as follows

The charge stored in the capacitor C_{p1} can be represented as

$$Q_{actual} = C_{p1} V_{actual} \tag{3.28}$$

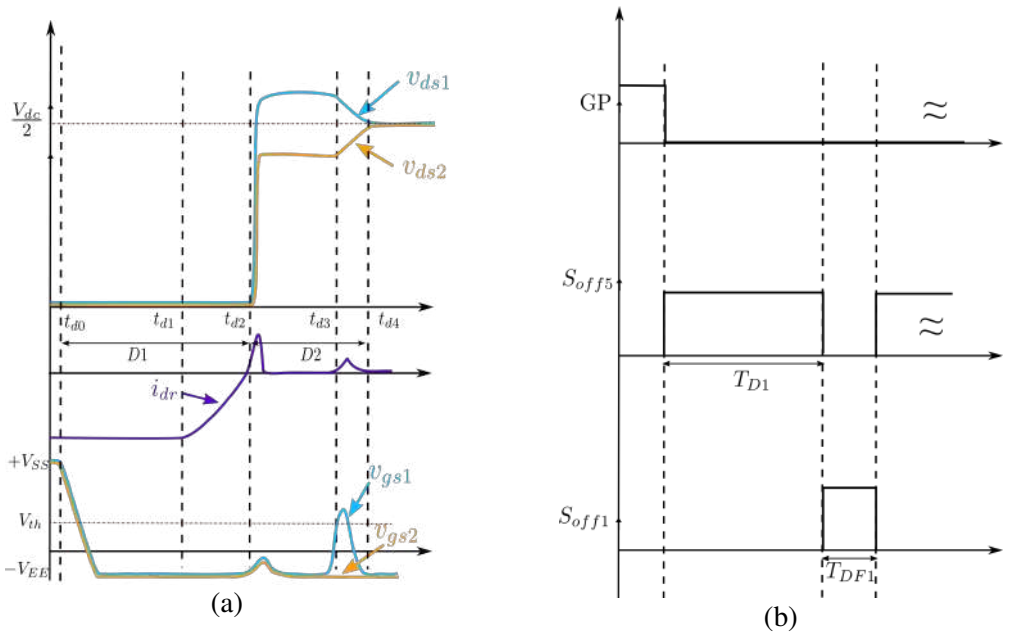

Fig. 3.16: (a) Proposed turn off control of body diode (b) Control signal for body diode turn off stage

where Q_{actual} is the actual charge stored in the C_{p1} capacitor and V_{actual} is the over voltage experienced by the diode of device S_1.

$$Q_{required} = C_{p1} V_{required} \tag{3.29}$$

where $Q_{required}$ is the required charge in the C_{p1} capacitor to maintain or bring the voltage to $V_{required}$ which is nothing but $\frac{V_{DC}}{2}$.

$$Q_{difference} = Q_{actual} - Q_{required} \tag{3.30}$$

where $Q_{difference}$ is the charge to be discharged from C_{p1} to bring the voltage from $V_{actual}(v_{ds1})$ to $V_{required}(\frac{V_{DC}}{2})$. This extra charge $Q_{difference}$ can be discharged through the device channel by partially turning on the device S_1. The channel current of the device in saturation is given by

$$i_{ch1} = g_m(V_{gs} - V_{th}) \tag{3.31}$$

Similarly, difference in the charge to be discharged in the channel is given by Eq.3.32

and Eq.3.33.

$$Q_{difference} = i_{ch1} T_{DF1} \tag{3.32}$$

$$Q_{difference} = g_m (V_{gs} - V_{th}) T_{DF1} \tag{3.33}$$

The required gate voltage to discharge the excess charge can be calculated from Eq.3.34

$$V_{gs} = V_{th} + \frac{Q_{difference}}{g_m T_{DF1}} \tag{3.34}$$

From the $Q_{difference}$, the channel current i_{ch1} is calculated and using Eq.3.31 the required V_{gs} above the threshold voltage can be estimated from Eq.3.34 . At t_{d3} instant, Off Stage-1 of S_1 is turned on and at the same time Off Stage-5 is turned-off. The required v_{gs} is applied through V_{cntrl} voltage for a fixed time duration of T_{DF1}. During this time, the drain to source voltage v_{ds1} of S_1 discharges to $\frac{V_{DC}}{2}$. This automatically forces the other drain to source voltage v_{ds2} of S_2 to be charged to $\frac{V_{DC}}{2}$ by KVL action. At t_{d4} instant the diode voltages of both the devices are completely balanced.

3.3.5 Simulation results of proposed turn off control

In order to verify the proposed turn off control technique, the simulation in LTspice environment is carried out. The proposed control stages are realised using ideal current sources. The simulation results for the proposed turn off control can be divided into low load and high load current condition. In low load condition, the parameters of Off Stage-2, Off Stage-3 and Off Stage-4 are decided by the above mentioned conditions. The parameters also depends on the maximum voltage clamping for the high frequency control. From Eq.3.14, Eq.3.15, Eq.3.19, Eq.3.21 and Eq.3.20 the v_{ds} peak at which i_{kp} reaches close to zero is set at 810V. The required $\frac{di}{dt}$ and $\frac{dv}{dt}$ is set at 1.5A/ns and 20V/ns. By setting this, the Off Stage-4 magnitude can be selected. The value of L_p used in the calculation is 60nH. The control parameters are fixed and the Fig.3.17 shows the simulation results of turn off transient at lower load current of 5A. Off Stage-4 has a magnitude of 190mA. The high frequency proportional controller Off stage-2 is chosen so that the net current injected to the gate is close to 0A at 600V DC bus to clamp the

device voltage as proposed. However, at lower loads, the high frequency control has little effect. Off Stage-3, which is carefully designed for low load current conditions, will inject current to the gate based on the static voltage difference over the switching frequency in order to minimise static imbalance. Fig.3.18 shows the turn off transient at low load current condition.

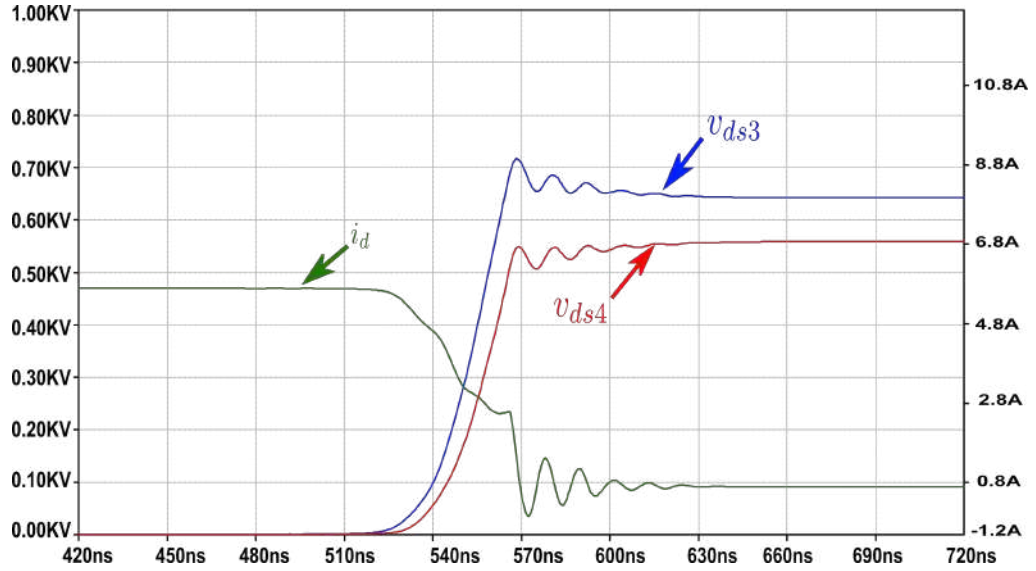

Fig. 3.17: Turn off at lower load current (Voltage scale:100V/div, Current scale: 2A/div and time scale: 30ns/div)

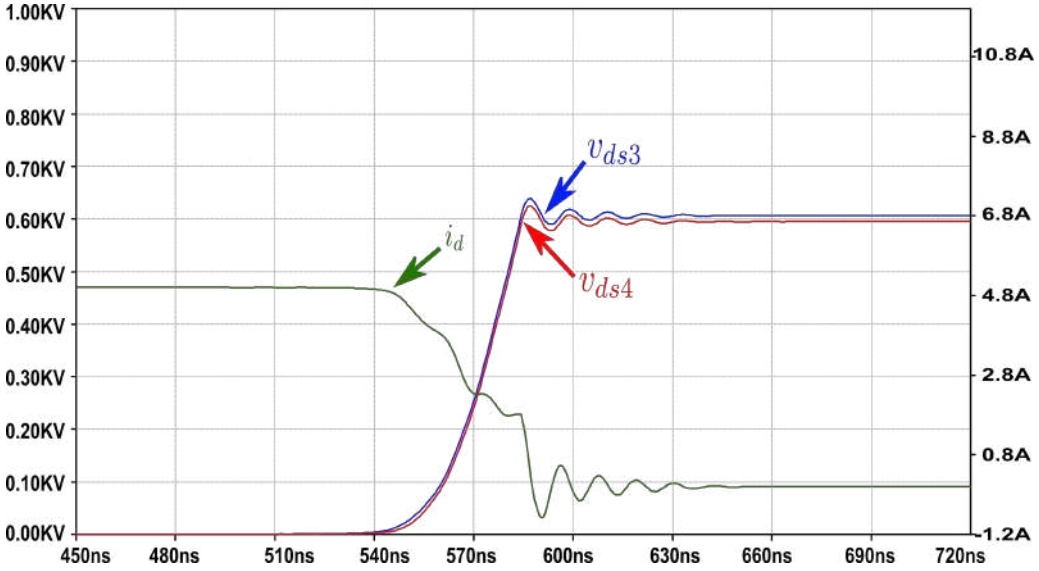

Fig. 3.18: Turn off at lower load current with proposed control (Voltage scale:100V/div, Current scale: 2A/div and time scale: 30ns/div)

Similarly, at higher load current conditions, where the device channel has enough

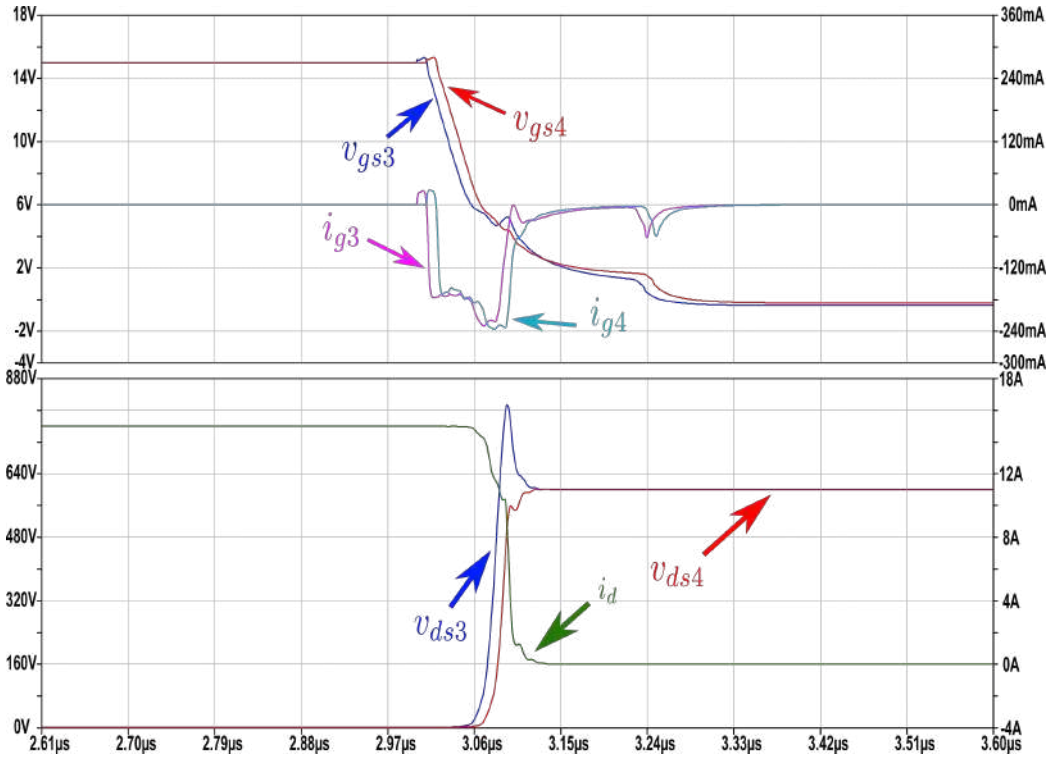

Fig. 3.19: Turn off at higher load current (Voltage scale:160V/div, Current scale: 4A/div and time scale: 90ns/div)

current to turn off, the high frequency control is very effective. It is important to note that both controls are enabled regardless of load current. Fig.3.19 demonstrates the turn off transient under higher load current conditions. Despite the clamp limit of 690V, the voltage is clamped at 770V due to the faster voltage rise and the propagation delay of the designed analog stage. The positive current injected into the gate for over voltage clamping greatly influences the dynamic response of the system. Lowering the clamping voltage increases damping and switching loss in the system.

3.4 CONCLUSION

The design of current source based gate driving stages for series connecting SiC MOSFETs is described in this chapter. The driving stages are divided into two categories namely turn on and turn off control. The turn on control is divided into three stages ON Stage-1, ON Stage-2, and ON Stage-3. During the turn on transient, each stage is controlled to achieve lower overvoltage and faster switching speed. The proposed method uses only two current source stages to limit the excess voltage during

the turn on transient. Furthermore, simulation results to validate the suggested turn-on control technique are also presented. Off Stage-1, Off Stage-2, Off Stage-3, Off Stage-4, and Off Stage-5 are the five stages for proposed turn off control. Off Stage-1 is the switched voltage source stage. This stage is dedicated for body diode voltage balancing. Off Stage-2, Off Stage-3 and Off Stage-4 are the switched current source stages dedicated for voltage balancing at light load and higher load conditions. The Off Stage-5 is the switched voltage source stage responsible for clamping the gate voltage to a negative value. This aids in avoiding the Miller from false turn on. The proposed turn off low frequency control as well as high frequency control techniques are discussed in detail in this chapter. The parameter selection for each control stages are also derived in this chapter. Low frequency control system modelling are also presented. The closed loop system dynamics and PI control model are validated through MATLAB. In addition, simulation results are shown to validate the suggested turn off control technique. According to the simulation results, the proposed control technique exhibits less static voltage imbalance and faster switching speed.

CHAPTER 4

Hardware Implementation of proposed AGD for Series Connected SiC MOSFETs

4.1 INTRODUCTION

This chapter will discuss the hardware implementation of the proposed control technique for series connected SiC MOSFETs. The hardware implementation consists of an on/off control section, a digital controller (FPGA), and signal conditioning units. In order to achieve voltage balancing and faster switching speed, the switching components in each control stage must be selected considering the minimum propagation delay and the minimum gate charge. This chapter also includes a detailed procedure for selecting the critical components of the proposed Active Gate Driver (AGD). The proposed control technique is validated experimentally using a Double Pulse Test (DPT) setup. The proposed control technique has been extended and applied to various phase leg configurations, which can be used in any power electronics converter topology. The first configuration is a chopper mode of operation with two device at 1.2kV DC bus and three devices at 2.1kV DC bus. The proposed series connection method is tested for various DC load current operating point. The second configuration is the high voltage buck converter at 1.2kV DC bus to validate the body diode voltage balancing. The third configuration is half bridge inverter at 1.2kV DC bus for two device and 2.1kV DC bus for three device in series connection. This helps to validate the proposed series connection control at AC load current conditions. The experimental hardware results are also presented for all the above mentioned configuration.

4.2 HARDWARE REALISATION OF PROPOSED SERIES CONNECTION TECHNIQUE

Fig.4.1 shows the functional block diagram of the proposed AGD. The turn on and turn off stages consist of switched voltage sources and current sources. The

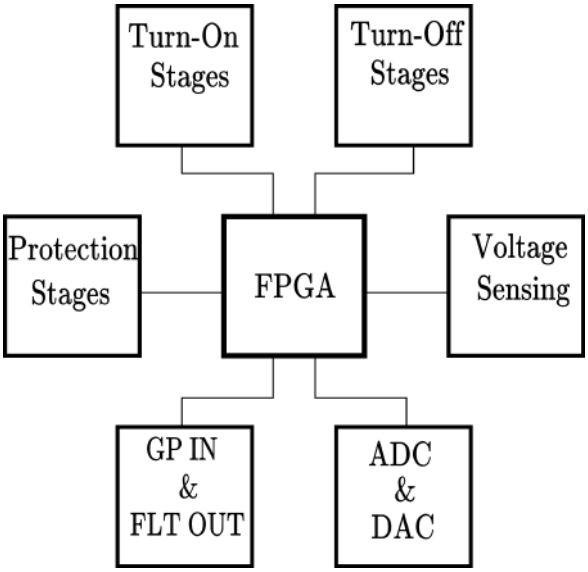

Fig. 4.1: Functional block diagram of proposed AGD

control command for the switching stages are controlled by an FPGA. Apart from the switching stages, the AGD has voltage sensing section for both protection and closed loop operation. ADC and DAC sections are used to sense the device voltage and to control the current reference of current sources respectively. GP IN (Gate Pulse IN) is used to receive the gate pulse from the central controller and FLT OUT (Fault OUT) is used to send fault signal to the controller. Finally Protection Stage is used to protect the device during over voltage and over current conditions.

4.2.1 Design of Voltage Controlled Current Source

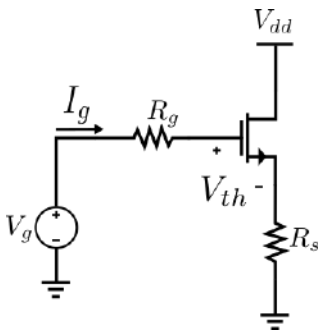

Fig. 4.2: Realising voltage controlled current source

The switching stages used in the Active Gate Driver are realised by configuring NMOS and PMOS transistors in the saturation region to realise the voltage controlled current source. In Fig.4.2, NMOS transistor is used to build the voltage controlled

current source. If the gate to source voltage (v_{gs}) is greater than the threshold voltage ($v_{gs} > V_{th}$), the drain current of the MOS transistor is given by Eq.4.1

$$I_d = g_m(v_{gs} - V_{th}) \tag{4.1}$$

The value of v_{gs} at steady state can be obtained by applying KVL in the gate loop as given by

$$I_d = g_m(V_g - I_g R_g - I_d R_s - V_{th}) \tag{4.2}$$

Rearranging the terms in Eq.4.2

$$I_d = \frac{V_g - I_g R_g - V_{th}}{\frac{1}{g_m} + R_s} \tag{4.3}$$

where, $R_s \gg \frac{1}{g_m}$ and steady state gate current I_g is 0. Simplifying the above equation, the drain current is given by Eq.4.4

$$I_d = \frac{V_g - V_{th}}{R_s} \tag{4.4}$$

From the above equation, it is clear that the drain current is directly proportional to the applied gate voltage (V_g) and inversely proportional to the source resistance (R_s). The above condition are valid only when the MOS transistor operates in the saturation region.

4.2.2 Hardware Realisation of Turn On Stage

Turn on control has three stages. They are designated as ON Stage-1, ON Stage-2, and ON Stage-3 respectively. ON Stage-1 and ON Stage-2 are the voltage controlled current sources, often referred as switched current source. ON Stage-3 is the switched voltage source that makes use of a PMOS transistor. In order to control the current rise ($\frac{di}{dt}$) and voltage fall ($\frac{dv}{dt}$) during the turn on switching interval, the resistors R_1 and R_2 are employed to determine the magnitude of I_{on1} and I_{on2}. When the SiC MOSFET is completely turned on, the resistor R_3 is utilised to clamp the gate voltage of the SiC MOSFET to the required gate voltage ($+V_{SS}$) to achieve the lowest possible on-state resistance. Turn on control signals from the controller (FPGA) are denoted by S_{on1},

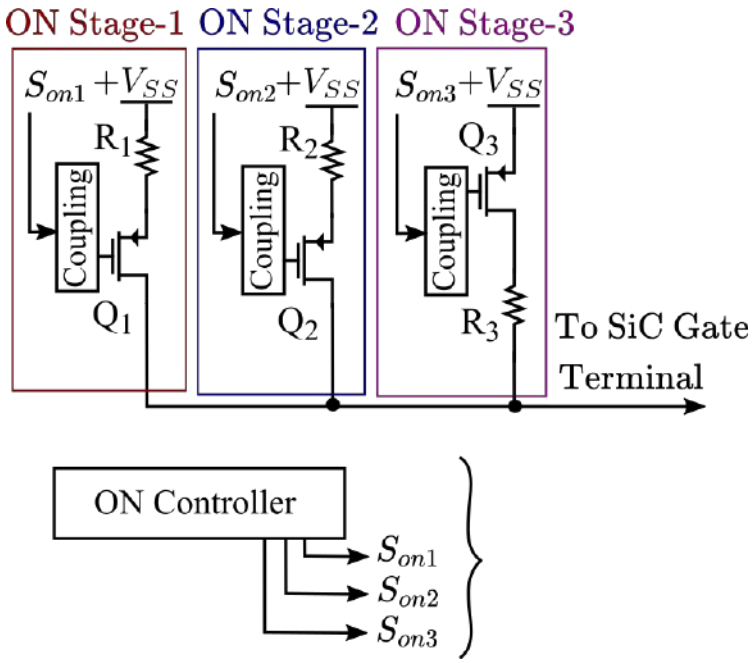

Fig. 4.3: Hardware realisation of proposed turn on stage

S_{on2}, and S_{on3} respectively. The net propagation delays of the switching stages need to be kept as minimum as possible to ensure effective performance of the switching stages. The term "Propagation delay" in the switching stage refers to the time between the instant switching command is given and the instant switching stage has completed its switching action. All the switching command signals S_{on1}, S_{on2}, and S_{on3} come directly from the FPGA via voltage buffer section. This is done to prevent the FPGA from loading. The voltage buffer (model number SN74LVC1T) was chosen in such a way that it would have a minimum delay (3ns to 5ns). The control signal is then sent to the coupling stage, where the control signals are AC coupled to drive the PMOS transistors. PMOS transistors are chosen such a way that it has extremely low total gate charge (Q_g) that needs to be supplied by the gate. At the same time, transconductance of the PMOS transistor needs to be sufficiently high so that it can switch very quickly. The part number of the PMOS transistor that was used in the turn on stage are given in table 4.1.

Designator	**Component**	**Part No**	**Main Specification**
Q1, Q2, Q3	PMOS Transistor	BSS84P	$Q_g = 1nC$ at $v_{gs} = -10V$

Table 4.1: PMOS used in the AGD for Turn-On Stage

4.2.3 Hardware Realisation of Turn off Stage

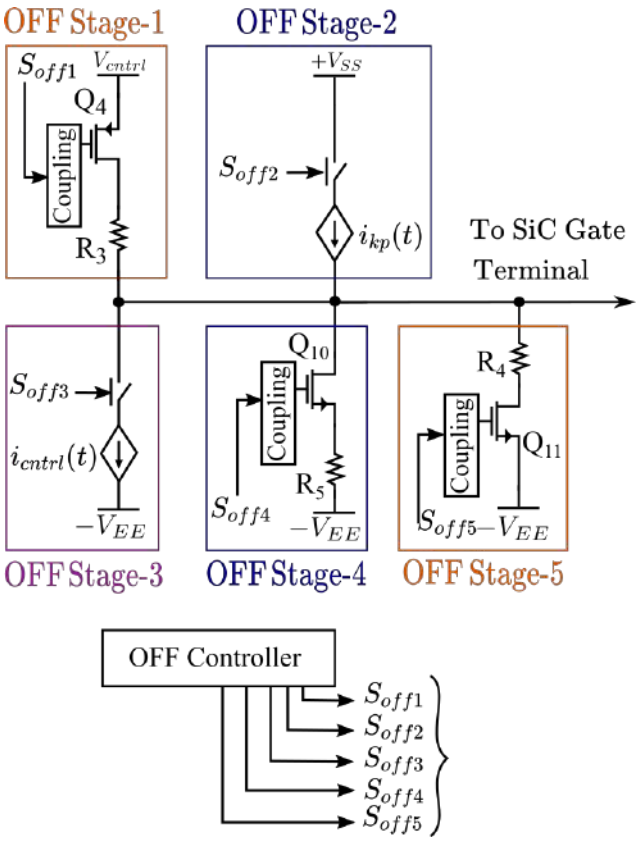

Fig. 4.4: Hardware realisation of proposed turn off stage

Turn off control has total five stages. They are referred as Off Stage-1, Off Stage-2, Off Stage-3, Off Stage-4 and Off Stage-5. The switched voltage source stages known as Off Stage-1 and Off Stage-5 are used for diode voltage balancing. Off Stage-2 and the Off Stage-3 are controlled current source stages. Off Stage-3 is the digitally controlled current source stage. A DAC is employed to control the amount of current flowing through the MOS transistor. Off Stage-2 is the analog controlled current source. The current flowing through the MOS transistor is controlled by the measured device voltage (v_{ds}), which is coupled to the gate bias of Off Stage-2. Off Stage 4 is a switched current source stage of constant magnitude directly controlled by the command signal from the FPGA. Following discussion provides a more detailed explanation of the implementation and operation of each off stage, along with the proposed control technique.

4.2.4 High frequency control realisation

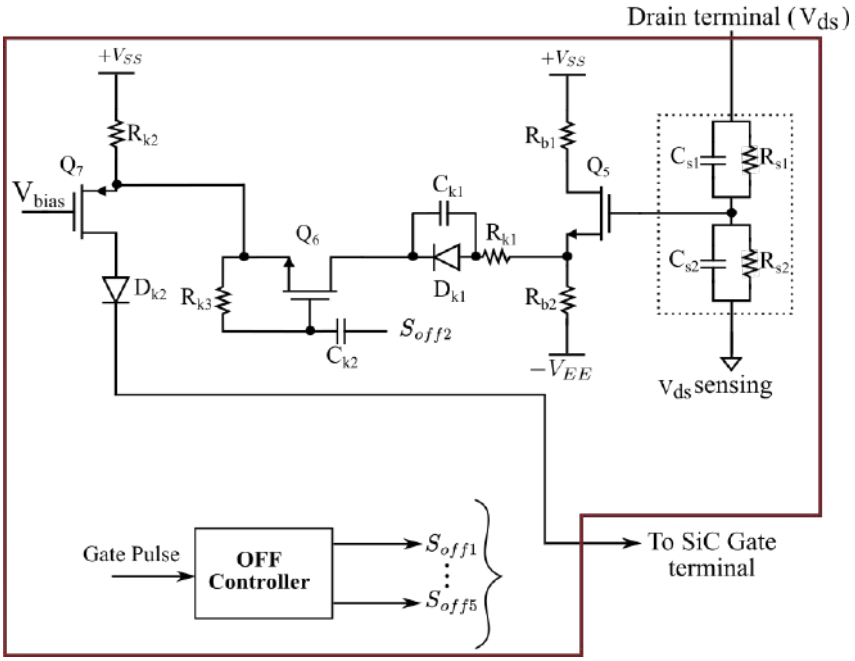

Fig. 4.5: Hardware realisation of high frequency control stage

The main objective of the high frequency control is to limit the device voltage (v_{ds}). The control equation from chapter 3 is reproduced here for better understanding. Eq.4.5 and Eq.4.6 shows relationship between the gate current i_g and the control current i_{Kp}.

$$i_g = -I_{off1} + i_{Kp} \tag{4.5}$$

$$i_{Kp} = \begin{cases} K_p\left(v_{ds} - \frac{V_{DC}}{2}\right) & \text{for} \quad v_{ds} \geq \frac{V_{DC}}{2} \\ 0 & \text{otherwise} \end{cases} \tag{4.6}$$

The high frequency control consists of two stages. They are Off Stage-2 and Off Stage-4 respectively. Off Stage-4 is a switched current source stage of magnitude I_{off1}. Q_{10} is an NMOS transistor used for sinking the current from the gate of the SiC MOSFET as shown in Fig.4.4. The schematic implementation of the i_{Kp} circuit is shown in Fig.4.5. In order to realize Eq.4.6, the circuit consists of a sensing branch v_{ds} sensing, where R_{s1} and R_{s2} are the sensing resistors that are placed across the device drain and the source terminal. In order to provide lead compensation, capacitors C_{s1} and C_{s2} are kept parallel to R_{s1} and R_{s2} respectively. The device voltage is connected

directly to the gate of the Q_5 NMOS transistor in Fig.4.5. The values of R_{b1} and R_{b2} are chosen carefully to ensure the NMOS is biased in the voltage follower configuration. As a result, the source voltage will follow the gate voltage from the sensing circuit. The other side of the circuit consists of a Q_7 PMOS transistor which is used to set the reference voltage (i.e $\frac{V_{DC}}{2}$) through V_{bias} voltage. The source voltage of a Q_7 PMOS transistor follows the applied gate voltage, which is denoted by V_{bias}. The drain of Q_7 PMOS transistor is connected with gate of SiC MOSFET through diode D_{k2}. The Q_6 NMOS transistor along with the AC coupling network (C_{k2} and R_{k3}) gets connected to the FPGA control signal S_{off2}. The effective voltage ($K_p\left(v_{ds} - \frac{V_{DC}}{2}\right)$) is applied across the resistor R_{k1} and the associated current is injected into the gate of the SiC MOSFET whenever the switch Q_6 is turned on. The diode D_{k1} is utilised so that the gate of the SiC MOSFET receives only the positive current. As the voltage of the device v_{ds} rises, the capacitor C_{k1} is connected to supply the lead current. This ensures that the device has a faster dynamic response. This analog controlled current stage is employed in conjunction with the Off Stage-4 current stage to restrict the voltage output of the device to the required level. The transistors are chosen in such a way that they have an extremely low total gate charge (Q_g) that needs to be supplied by the gate. At the same time, transconductance of the transistor needs to be sufficiently high so that it can switch very quickly. The part number of the NMOS&PMOS transistor that was utilised in the turn-off stage operation is given in table 4.2.

Designator	**Component**	**Part No**	**Main Specification**
Q5, Q6	NMOS Transistor	T2N7002	$Q_g = 0.39nC$ at $v_{gs} = 4.5V$
Q7	PMOS Transistor	BSS84P	$Q_g = 1nC$ at $v_{gs} = -10V$

Table 4.2: MOS transistor used in the AGD for Turn-Off Stage

4.2.5 Low frequency control realisation

Fig.4.6 illustrates the hardware implementation of the low frequency control algorithm. To achieve voltage balancing of series connected SiC MOSFET operating at lower current, the low frequency control technique is used. A switched voltage controlled current source Off-Stage-3 is used to achieve voltage balancing at lower load current. The hardware consists of two NMOS transistors, namely Q_8 and Q_9.

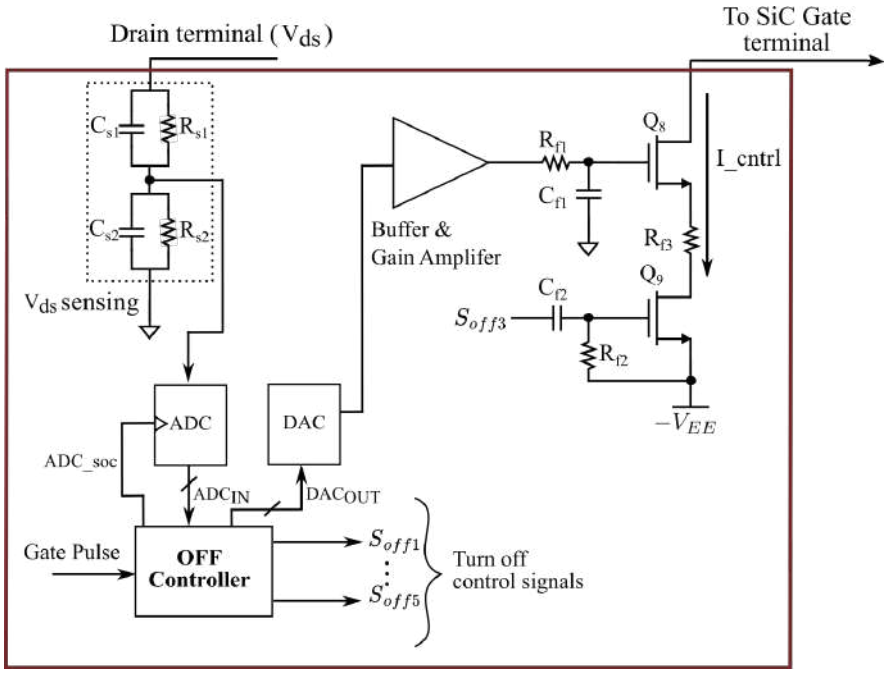

Fig. 4.6: Hardware realisation of low frequency control stage

Q_9 transistor is used as a switch to connect the R_{f3} resistor to the negative supply $-V_{EE}$. Q_9 transistor gate is biased with an AC coupling network (C_{f2} and R_{f2}) through FPGA control signal S_{off3}. Assuming the transistor Q_9 is turned on, the negative supply voltage $-V_{EE}$ gets connected to one end of the resistor R_{f3}. The other end of the resistor R_{f3} is connected to the source of Q_8 NMOS transistor. Through the gain amplifier and the voltage buffer, the gate voltage of Q_8 NMOS transistor is connected to the DAC. Sensing resistors R_{s1} and R_{s2} are kept across the device drain and the source terminal with capacitors C_{s1} and C_{s2} in parallel to the sensing resistor branch. This placement helps to realize lead compensation.

The dedicated ADC module is used to sense the device voltage of each SiC MOSFETs that are connected in series. Sensed voltage is compared to the internal reference voltage, and the closed loop digital PI controller generates the reference based on the error to minimise the voltage difference. The reference voltage is fed directly into the DAC module, and a gain amplifier is used to adjust the calculated voltage to provide the necessary gain. The device voltage is measured during the current switching cycle, but any adjustments are made during the next switching cycle. R_{f1} and C_{f1} are connected at the DAC voltage to filter the ripple. DAC controlled voltage is connected to the gate of Q_8 transistor, and the corresponding current I_{cntrl}

flows through the R_{f3} resistor. The gate current of the SiC MOSFET is sinked by Q_8 NMOS transistor. The propagation delay must be kept as short as possible to ensure that the low frequency control operates reliably. The crucial parameter is the precise Start Of Conversion(ADC_{SOC}) instant signal to the ADC module. The delay in the control signal from the FPGA causes the transistor Q_9 to switch on should be as small as possible. The NMOS transistors are chosen to have an extremely low total gate charge (Q_g) that needs to be supplied by the gate. At the same time, the transconductance of the NMOS transistor needs to be sufficiently high, so it can switch very quickly. The part number of the NMOS transistor utilized in the turn off stage operation is given in table 4.3.

Designator	Component	Part No	Main Specification
Q8, Q9	NMOS Transistor	T2N7002	$Q_g = 0.39nC$ at $v_{gs} = 4.5V$

Table 4.3: NMOS used in the AGD for low frequency control Stage

4.2.6 Diode voltage control realisation

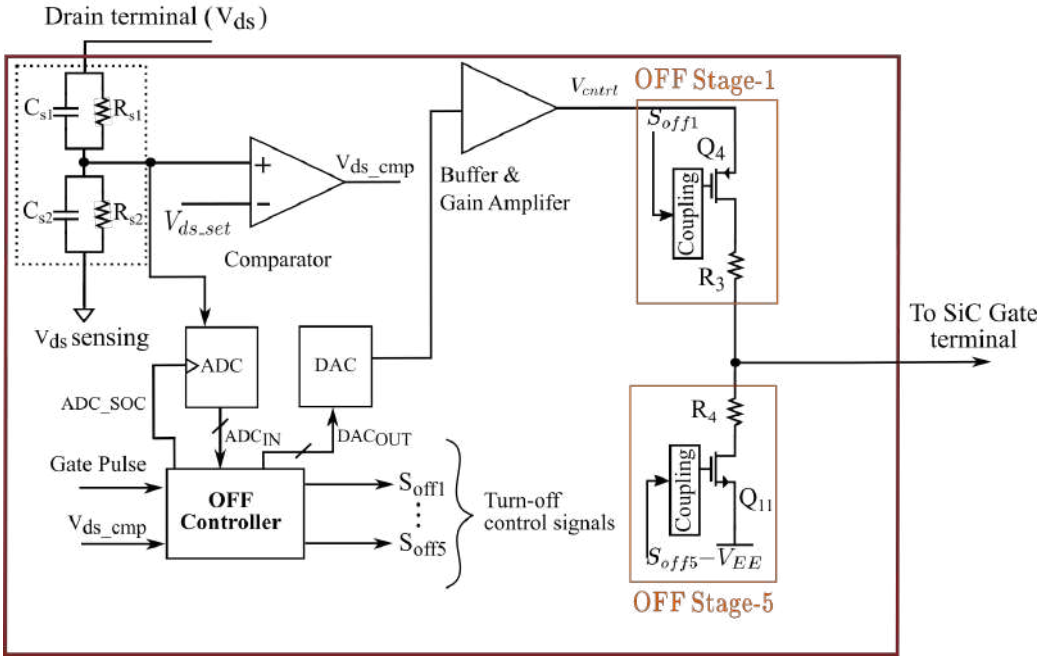

Fig. 4.7: Hardware realisation of Diode voltage control stage

When switching devices are connected in series, the load current can either flow through the channel or through the body diode. The gate voltages of diode conducted

devices will remain in the negative clamping voltage range, while the body diode will continue to conduct until the other switch from the same leg are turned on. As the gate voltage is already negative, the body diode turn off voltage cannot be controlled. The switching devices that are connected in series will have imbalance in the voltage. The reverse capacitance of the diode and the formation of parasitic earth capacitance across the series connected switching devices solely govern the voltage imbalance in the body diode. Both of these factors contribute to the voltage imbalance in the body diode.

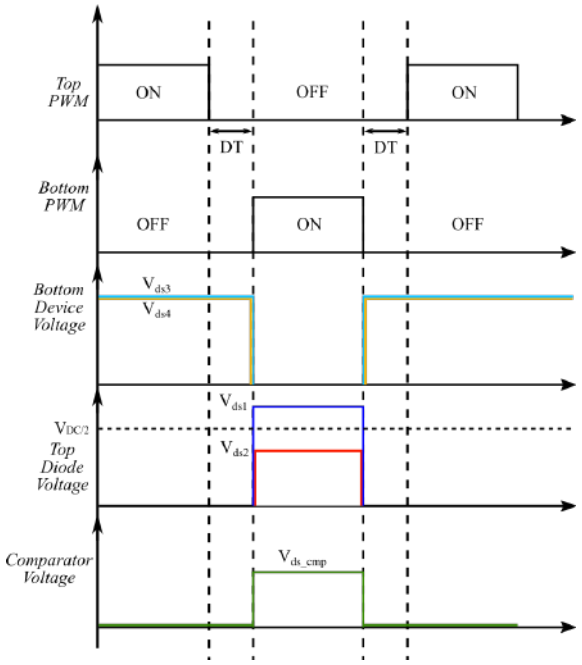

Fig. 4.8: Diode turn off detection signal

It is necessary to distinguish the turn off of the diode from the normal turn off to accomplish diode voltage balancing. Fig.4.8 shows a timing diagram that illustrates the differentiation between a regular turn off event and diode turn off. Device voltage sensing with a comparator and gate pulse information are required to differentiate the diode turn off event. Normal turn off transient occurs when the gate voltage transitions from positive($+V_{SS}$) to negative voltage($-V_{EE}$), and the switching device voltage rises when the gate voltage reaches the Miller pleatue voltage. If the gate voltage of switching devices is already at the negative clamping voltage ($-V_{EE}$). The complementary switching device in the same leg turns on, the diode voltage rises and enters reverse blocking mode. When the gate voltage is clamped negatively, the change in the voltage of the body diode indicates that the body diode is about to turn off. As a result, a v_{ds}

sensing circuit is used with the comparator to sense the rise in switching device voltage to identify the diode turn off event. Fig.4.8 shows the comparator signal will go high whenever the sensed v_{ds} signal crosses the specified reference voltage.

V_{ds}_cmp signal is used by the FPGA to determine the diode event. The control signal S_{off1} and S_{off5} are used to control the diode voltage. Off Stage-1 has a Q_4 PMOS transistor and the drain voltage V_{cntrl} is adjusted above threshold voltage of the SiC MOSFET. This ensures the stage to clamp the gate voltage above the threshold voltage to turn on the device for diode voltage balancing. Off Stage-5 has a Q_{11} NMOS transistor and the source voltage is connected to $-V_{EE}$ voltage. During a diode event, the Off Stage-5 is turned off first to release the gate from the negative clamping voltage. Off Stage-1 is turned on to partially turn on the device to control the diode voltage. By minimising the propagation delay in the switching of Off Stage-1 and Off Stage-5, the diode control can be used more effectively. The selection of transistors must ensure fast switching. The below table 4.4 shows the MOS transistor used for the diode voltage balancing.

Designator	**Component**	**Part No**	**Main Specification**
Q11	NMOS Transistor	T2N7002	$Q_g = 0.39nC$ at $v_{gs} = 4.5V$
Q4	PMOS Transistor	BSS84P	$Q_g = 1nC$ at $v_{gs} = -10V$

Table 4.4: MOS transistor used in the AGD for diode Turn-Off Stage

4.3 HARDWARE SETUP

The proposed series connection of SiC MOSFETs consists of three major hardware components. They are isolated power supply board, an optical isolator board, and an Active Gate Driver(AGD) board. One of the most important requirement for series connection is an isolated power supply. The isolated power supply takes a +15V DC input and provides +20V, +5V, and -5V output voltages for AGD operation. A fixed frequency of 50 kHz Half bridge isolated supply with secondary side rectifiers are designed. The isolation transformer is a critical component of power supply design. The power supply transformer core is designed to withstand 5kV isolation and has cmmon mode capacitance of less than 5pF. The power supply is also designed to withstand maximum power rating of 20W. Fig.4.9 and Fig.4.10 shows the designed power supply.

Fig. 4.9: Isolated Power Supply for AGD

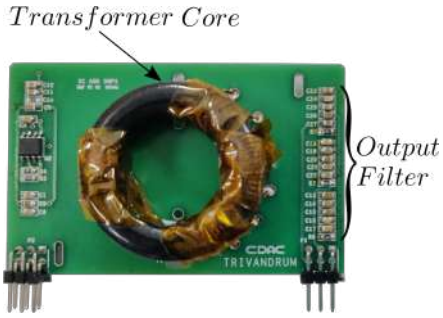

Fig. 4.10: Isolated Power Supply transformer core

The isolation of the power supply is primarily required to drive switches with floating potential. Broadcomm's optical isolator HFBR is used to provide signal isolation for gate pulse signals sent from the controller. Fig.4.11 shows the optical isolator board.

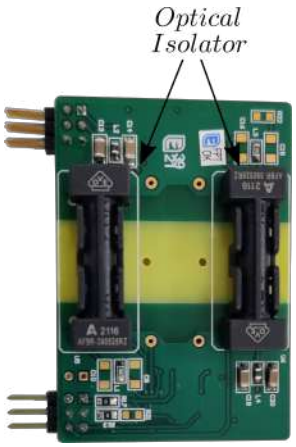

Fig. 4.11: Optical Isolator

Fig.4.12 shows the designed Active Gate Driver. The main components of AGD are FPGA (MAX 10 from Intel), switching stages and voltage sensing section. The

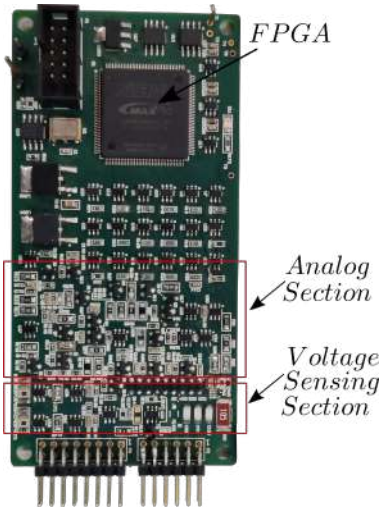

Fig. 4.12: Designed Active Gate Driver

Fig. 4.13: Designed load inductor

AGD is made of 6 layer PCB for better signal integrity. The AGD has a 250MHz onbard clock which provides 4ns time period for the control signals. ADC and DAC are also provided for the proposed control technique implementation. Fig.4.13 shows the designed ferrite core load inductor of value 2.5mH and maximum current rating of 10A. Fig.4.14 shows the assembled hardware setup consisting of AGD board, Power board, Power supply board and optical board connected. The input DC bus capacitance of (560uF, 3kV) is placed. The DC link flim capacitor of capacitance (22uF, 3.6kV) is placed close to the switching devices to provide the ripple current requirement. Lecroy voltage probe (HVD 3605A) and current probe (N2782B) are used for capturing the switching transients.

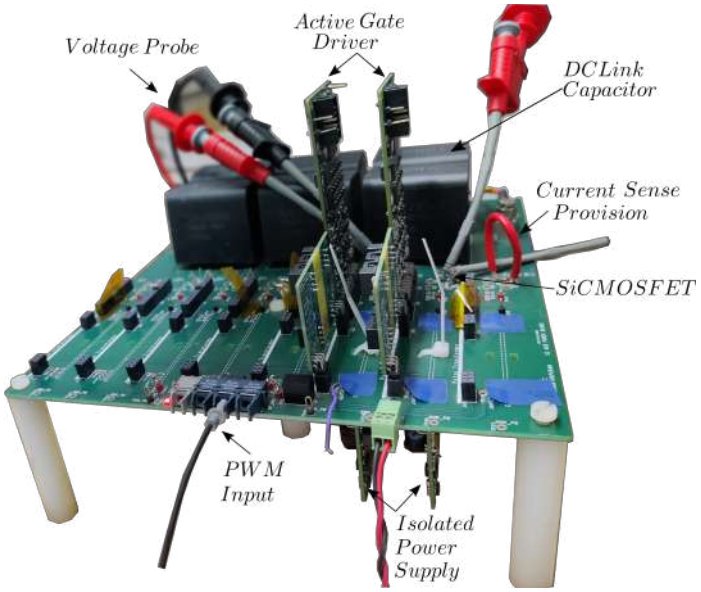

Fig. 4.14: Series connection Hardware setup

4.4 EXPERIMENTAL RESULTS

4.4.1 Two device series connection results

Chopper mode of operation

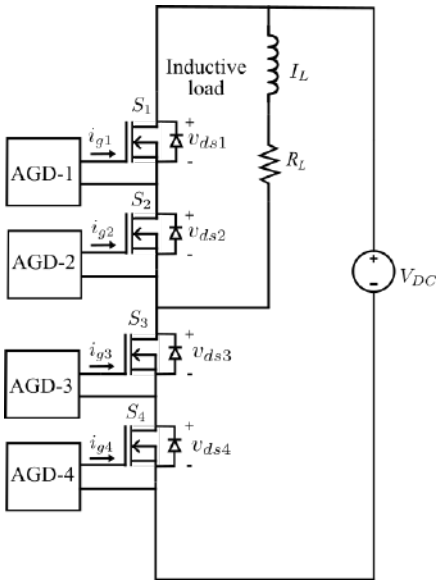

Fig. 4.15: Series connected devices in chopper mode configuration

The proposed control technique can be used for all the converter configuration. The chopper mode topology is chosen to verify the voltage balancing of the series connected devices as well as the diodes. Here, the proposed low frequency control

technique can be easily verified through the experimental results. Fig.4.15 shows the two device in series connection for the chopper mode converter configuration. The device S_1 and S_2 are the top series connected devices working as free wheeling diode for the inductor current. The device S_3 and S_4 are the bottom series connected devices as the main device for load current conduction. The value of the inductor is 2.5mH. A load resistor R_L is placed in series with inductor for loading the converter. The value of load resistance is changed to vary the load current. Switching frequency of the converter is kept at 5kHz. The duty ratio is fixed at 30% and the input DC bus voltage is maintained at 1200V.

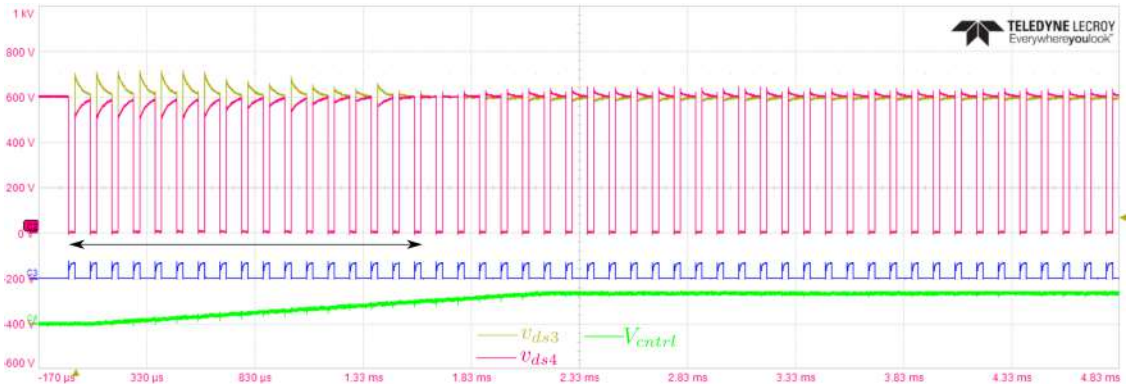

Fig. 4.16: Chopper output at low load current (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div and time-500us/div)

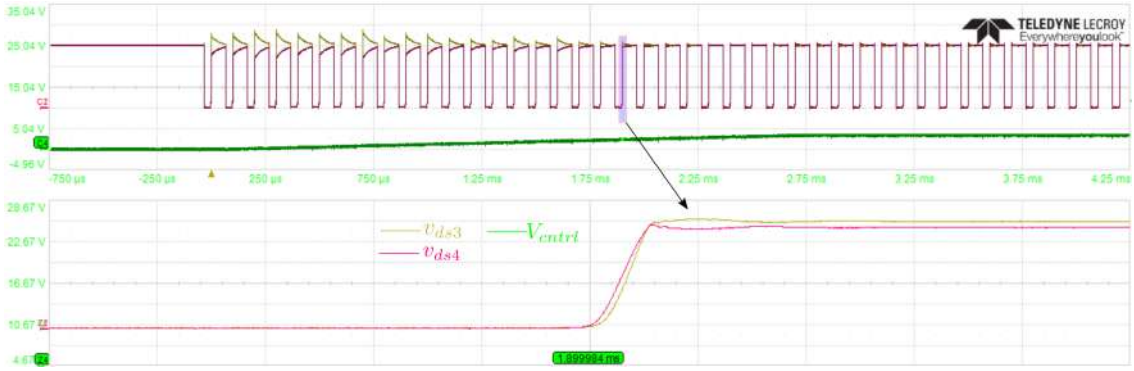

Fig. 4.17: Chopper output at low load current transient (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div and time-100ns/div)

Fig.4.16 shows the chopper mode of operation at a fixed load current of 5A peak. The initial voltage differences among the switching devices are high as expected in the low load current conditions. The steady state settling time is mainly determined

by the controller dynamics. In this case, the PI controller is tuned to achieve the response time of 2ms. The V_{cntrl} voltage can be seen increasing slowly to reduce the voltage difference. Fig.4.17 shows zoomed version of turn off transient and the voltage imbalance among the series connected devices. The voltage imbalance is below 50V.

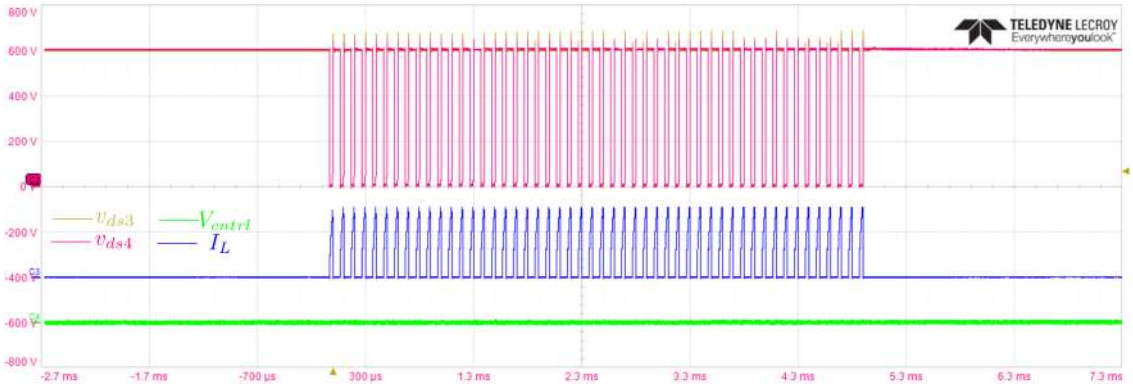

Fig. 4.18: Chopper output at high load current (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div,I_L-10A/div and time-1ms/div)

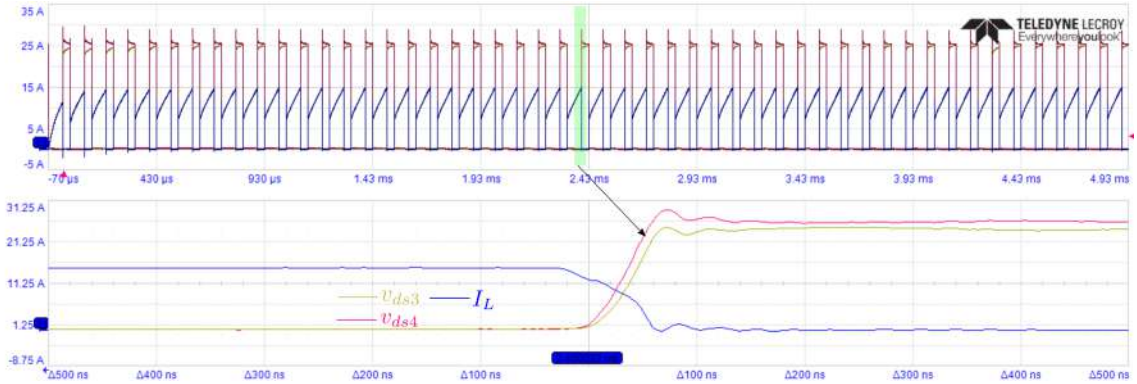

Fig. 4.19: Chopper output at high load current transient (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div,I_L-10A/div and time-100ns/div)

Fig.4.18 shows the chopper mode of operation at fixed load current of 15A peak. In this mode, the load current is high and it is sufficient for the channel formation at the very first turn off instant. This will enable the high frequency control stage to correct the voltage imbalance in the very first switching cycle itself. Thus the sensed error will be very low and this makes the controller output to be low. This means the low frequency control at the higher load current has very minimum impact. Fig.4.19 shows the turn off transient at higher drain current. The turn off transient is within 60ns which ensures fast switching speed of the proposed control.

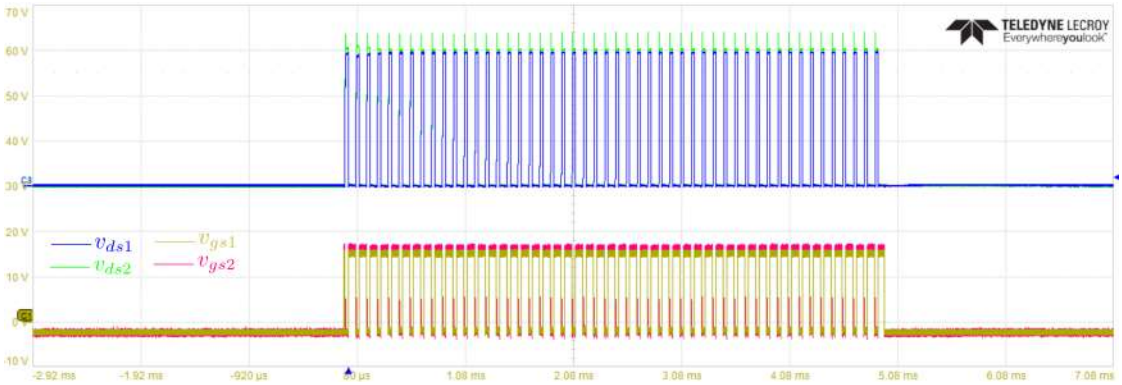

Fig. 4.20: Chopper diode voltage balancing (v_{ds1}-200V/div, v_{ds2}-200V/div, v_{gs1}-10V/div, v_{gs2}-10V/div and time-1ms/div)

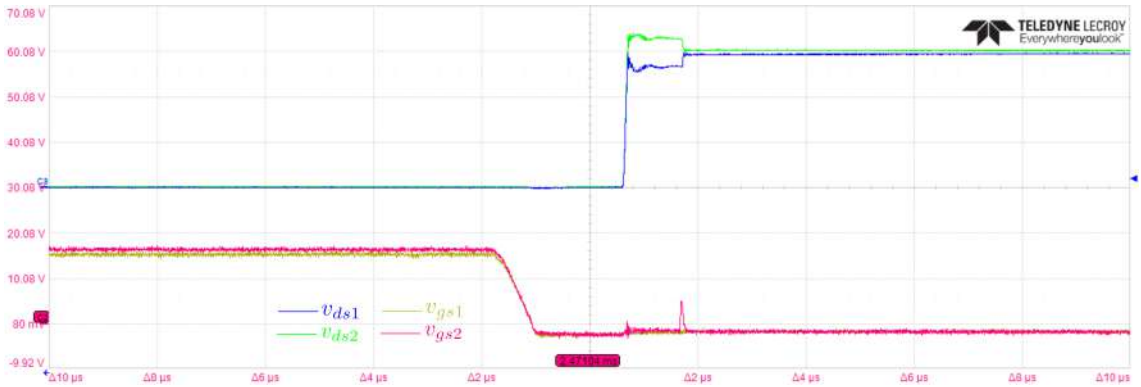

Fig. 4.21: Chopper diode voltage balancing transient (v_{ds1}-200V/div, v_{ds2}-200V/div, v_{gs1}-10V/div, v_{gs2}-10V/div and time-2us/div)

Fig.4.20 shows the freewheeling diode voltage balancing of S_1 and S_2. During the inductor current freewheel time, the anti parallel diode of S_1 and S_2 will be conducting. After the freewheel time, the device S_3 and S_4 will start conducting. Anti parallel diode of S_1 and S_2 will be into reverse blocking mode. This event will be detected from the device voltage sensing as explained in the diode control hardware implementation. As the gate voltage of the devices is already below the threshold voltage. The proposed diode control is used to balance the diode reverse voltages. The verification of the proposed diode voltage balancing technique is shown in Fig.4.20 and Fig.4.21. Here, the device that crosses the set reference voltage is turned on to discharge the excess charge into the channel and balances the diode voltage.

In order to verify the low frequency control for the low load current conditions, the load current is fixed at 5A and duty of the PWM pulse is varied. Fig.4.22 shows the chopper mode of operation at 10% duty cycle. Fig.4.23 shows the chopper mode

Fig. 4.22: Chopper output voltage at 10% duty (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div,I_L-10A/div and time-200us/div)

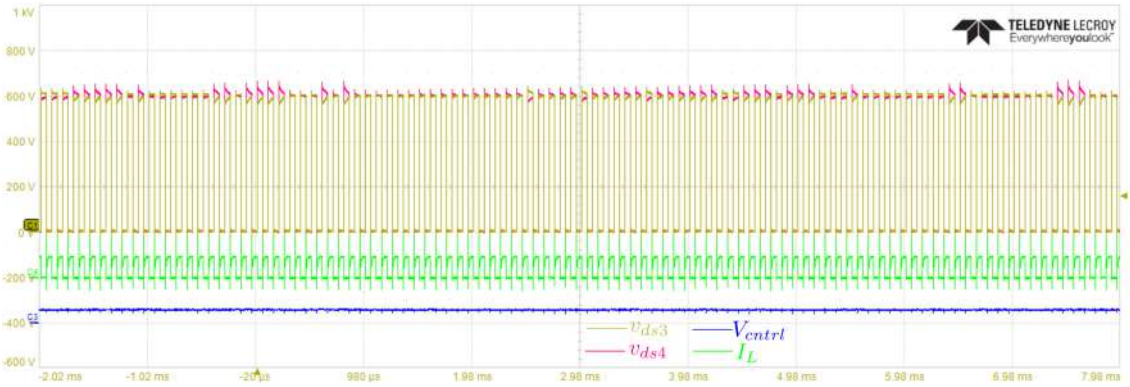

Fig. 4.23: Chopper output voltage at 50% duty (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div,I_L-10A/div and time-1ms/div)

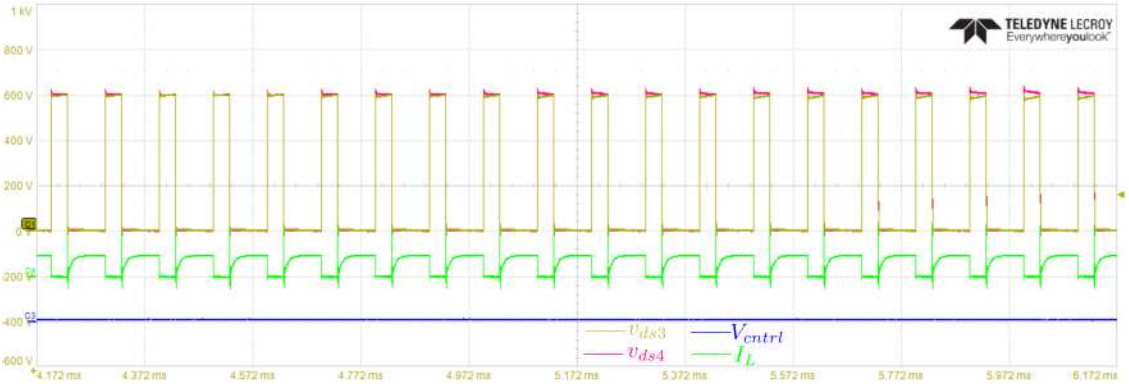

Fig. 4.24: Chopper output voltage at 70% duty (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{cntrl}-5V/div,I_L-10A/div and time-200us/div)

of operation at 50% duty cycle. Here, the steady state has slight unbalance with small static difference in some cycles. This is due to the decentralised control from the central controller. As the gate pulses received by the AGD's have different clock sampling, the static difference occurs at some switching cycle even though the steady state is reached.

DC-DC buck converter configuration

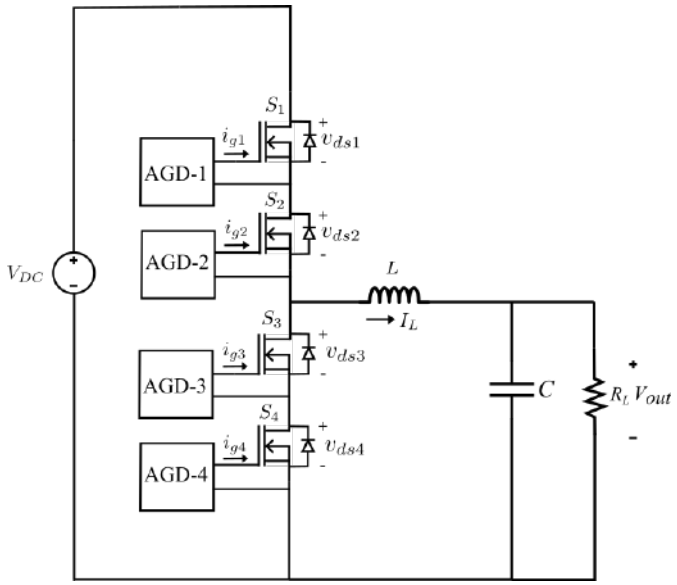

Fig. 4.25: Series connected devices in buck converter configuration

In order to show that the proposed control technique can be applied for all the converter configuration, the buck converter topology is chosen to verify the voltage balancing of the series connected devices as well as the diodes. Fig.4.25 shows the two device series connection in the buck converter configuration. The device S_1 and S_2 are the top series connected device and acts as the main device for the buck converter configuration. The device S_3 and S_4 are the bottom series connected device and acts as free wheeling diode for the inductor current. The value of the inductor is 2.5mH and the value of capacitor is 5uF. The resistive load R_L is placed for loading the converter. Switching frequency of the buck converter in open loop configuration is chosen to be at 10KHz. The duty ratio is fixed at 30% and the input DC bus voltage is kept at 1200V.

Fig.4.26 shows the voltage balancing of S_1 and S_2 in the steady state. The steady state voltage difference is very low. Fig.4.27 and Fig.4.28 shows the turn off and turn on transient.

Fig.4.29 and Fig.4.30 shows the steady state and transient voltage balancing of body diode with the proposed control technique.

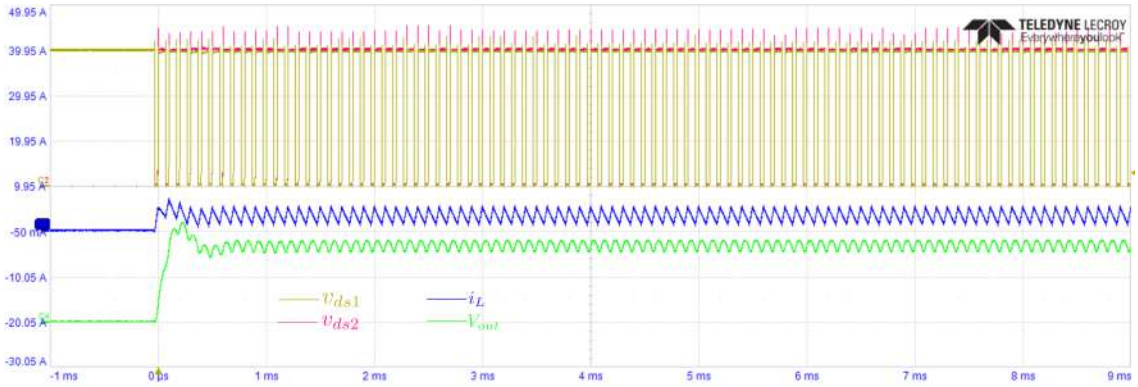

Fig. 4.26: Buck converter output waveform (v_{ds1}-200V/div, v_{ds2}-200V/div, V_{out}-200V/div, I_L-10A/div and time-1ms/div)

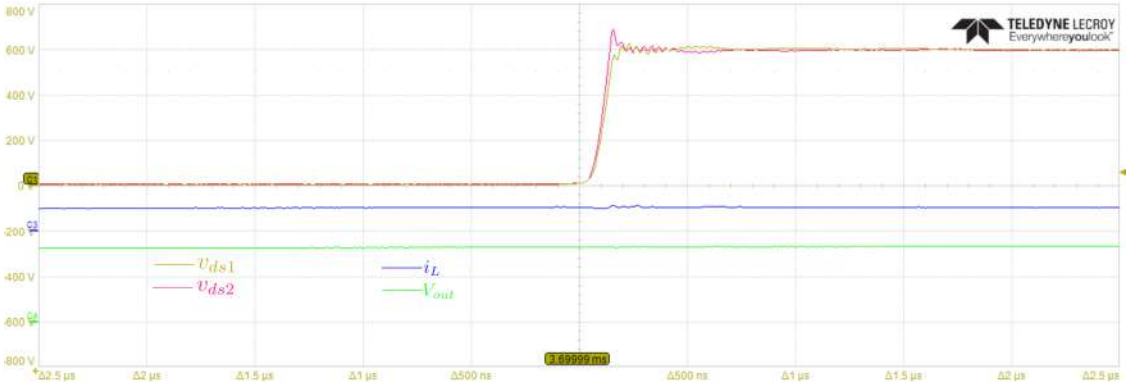

Fig. 4.27: Turn off transient of series connected devices in buck converter (v_{ds1}-200V/div, v_{ds2}-200V/div, V_{out}-200V/div, I_L-10A/div and time-500ns/div)

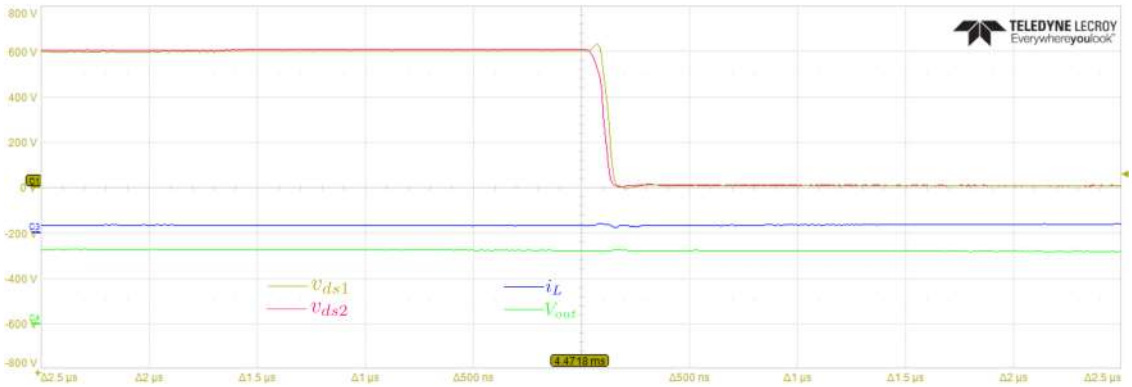

Fig. 4.28: Turn on transient of series connected devices in buck converter (v_{ds1}-200V/div, v_{ds2}-200V/div, V_{out}-200V/div, I_L-10A/div and time-500ns/div)

Half bridge inverter operation

The experiment is extended for half bridge inverter configuration to show the effectiveness of the proposed control in AC load current conditions. Fig.4.31 shows the series connected SiC MOSFET in half bridge inverter configuration. The device

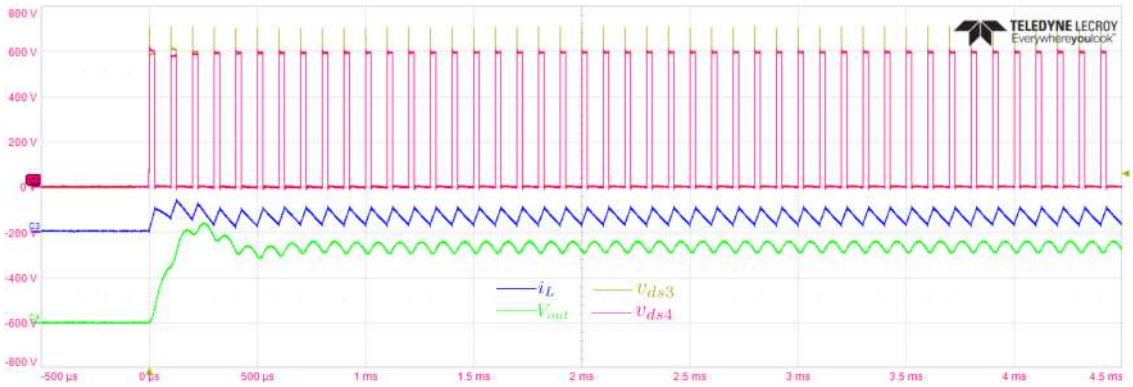

Fig. 4.29: Anti-parallel diode voltage balancing of series connected devices in buck converter (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{out}-200V/div, I_L-10A/div and time-500us/div)

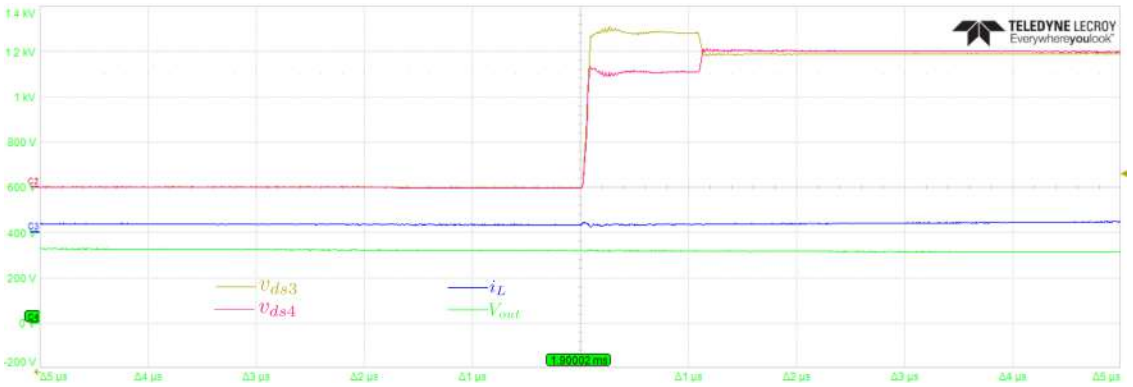

Fig. 4.30: Transient diode voltage balancing of series connected devices in buck converter (v_{ds3}-200V/div, v_{ds4}-200V/div, V_{out}-200V/div, I_L-10A/div and time-1us/div)

S_1 and S_2 represents top series connected device. Device S_3 and S_4 represents bottom series connected device. The DC split capacitor C_1 and C_2 of each 2200uF capacitance and voltage rating of 1.7kV are used. The RL load of inductance 3mH and resistance of 20 ohm are placed considering the fundamental sine frequency of 300Hz. The switching frequency and modulation index are kept at 10KHz and at 0.3 respectively.

Fig.4.32 shows the voltage balancing of top series connected devices S_1 and S_2. The load current I_L varies sinusoidally at 300Hz. During the positive cycle of the load current, the series connected device will have hard turn off. From Fig.4.33 it can be seen at zero crossing of the load current, the voltage imbalance is considerably large. This is due to the fact that the closed loop control has a limited number of switching cycles available to balance voltages at low load current. As the load current goes to

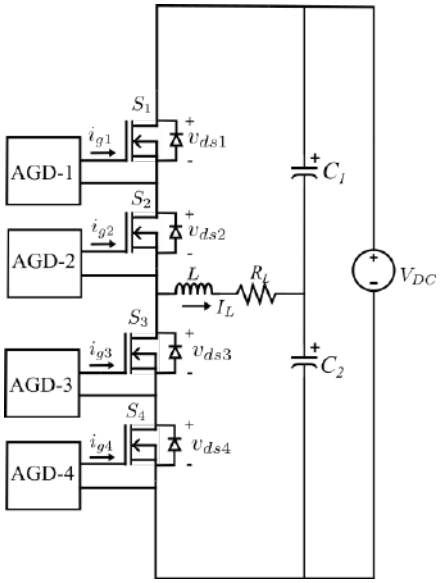

Fig. 4.31: Series connected devices in half bridge mode configuration

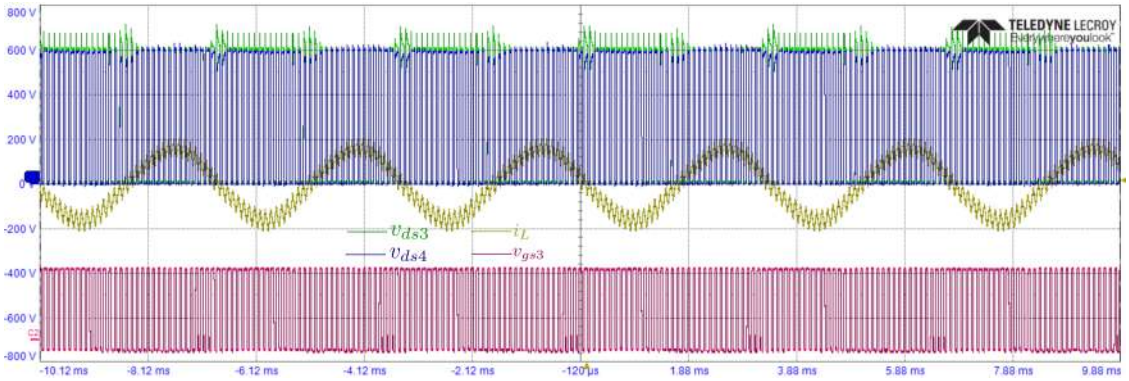

Fig. 4.32: Half bridge inverter top series connected devices (v_{ds1}-200V/div, v_{ds2}-200V/div, v_{gs2}-10V/div,I_L-10A/div and time-2ms/div)

Fig. 4.33: Half bridge inverter bottom series connected devices (v_{ds3}-200V/div, v_{ds4}-200V/div, v_{gs3}-10V/div,I_L-10A/div and time-1ms/div)

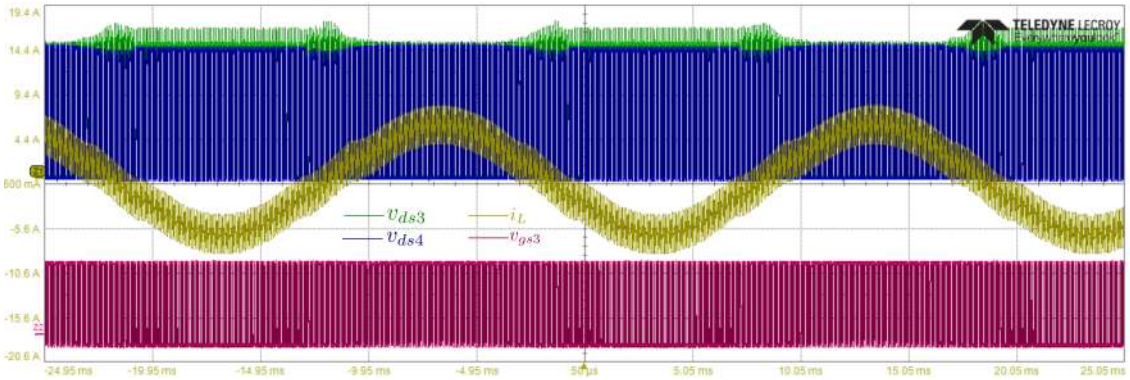

Fig. 4.34: Half bridge inverter at 50Hz fundamental frequency (v_{ds3}-200V/div, v_{ds4}-200V/div, v_{gs3}-10V/div,I_L-10A/div and time-5ms/div)

the positive cycle, the voltage imbalance is corrected by the high frequency control and voltage difference is very minimum. In the negative half cycle of the load current, the diode of the top series connected device will be soft turn off and the proposed diode voltage balancing control is activated for the voltage balancing. Similarly Fig.4.33 shows the voltage balancing of bottom series connected devices S_3 and S_4. Fig.4.33 shows the experimental result of half bridge inverter with series connected device at 50Hz fundamental frequency.

4.4.2 Three device series connection results

Chopper mode of operation

The proposed control technique can be extended for more than two devices in series connection. In order to verify that, three devices are connected in series for chopper mode configuration. The chopper mode topology is chosen to verify the voltage balancing of the series connected devices as well as for the diodes. Here, the proposed low frequency control can be easily verified for three device in series connection with the experimental results. Fig.4.35 shows the three device in series connection for the chopper mode converter configuration. S_1, S_2 and S_3 are top series connected devices as free wheeling diodes for the inductor current. S_3, S_4 and S_5 are bottom series connected devices for the load current conduction. Value of the load inductor is 2.5mH and the load resistor R_L is placed for loading the converter. The switching frequency of the converter is kept at 10kHz. The duty ratio is fixed at 30% and the input DC bus voltage is kept at 2.1kV.

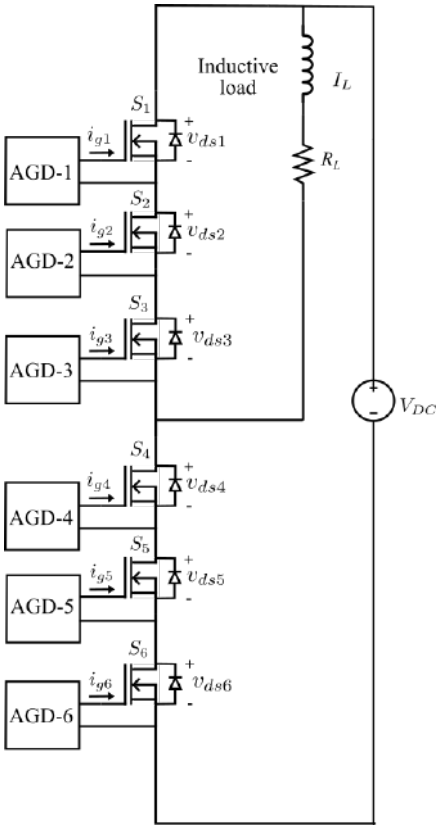

Fig. 4.35: Series connected devices in chopper mode configuration

Fig. 4.36: Without low frequency control of three device series connection (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-500us/div)

Fig.4.36 shows the voltage balancing of three devices in series connection. Here, the low frequency control is disabled at the load current of 5A. The voltage imbalance can be seen in the waveform where each device are expected to be sharing 700V for 2.1kV DC bus voltage. Due to the absence of the low frequency control, one of the series connected device experiences a maximum blocking voltage of 900V.

The low frequency control is activated and shown in Fig.4.37. The voltage

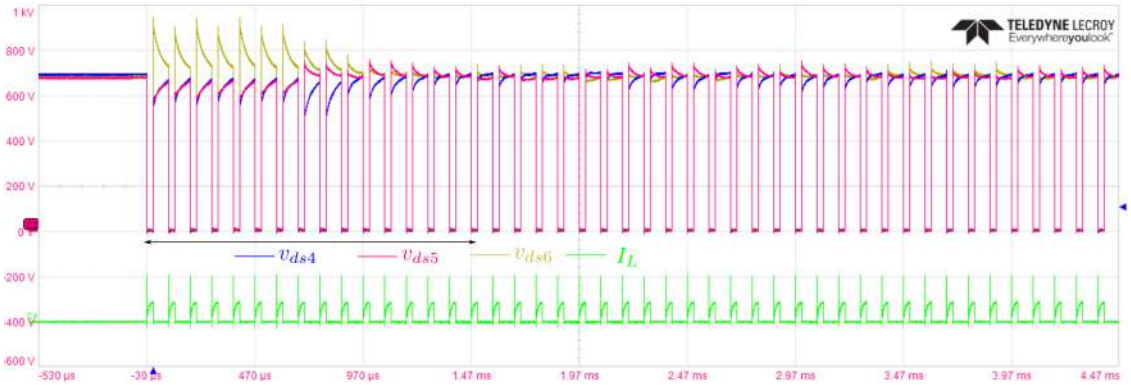

Fig. 4.37: With low frequency control of three device series connection (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-500us/div)

imbalance minimises in the consecutive switching cycles. The steady state settling time is mainly determined by the controller dynamics. The PI controller is tuned to get the response time of 1.5ms. After 1.5ms, the steady state voltage unbalance is very low. Fig.4.37 shows the transient of the steady state voltage balancing.

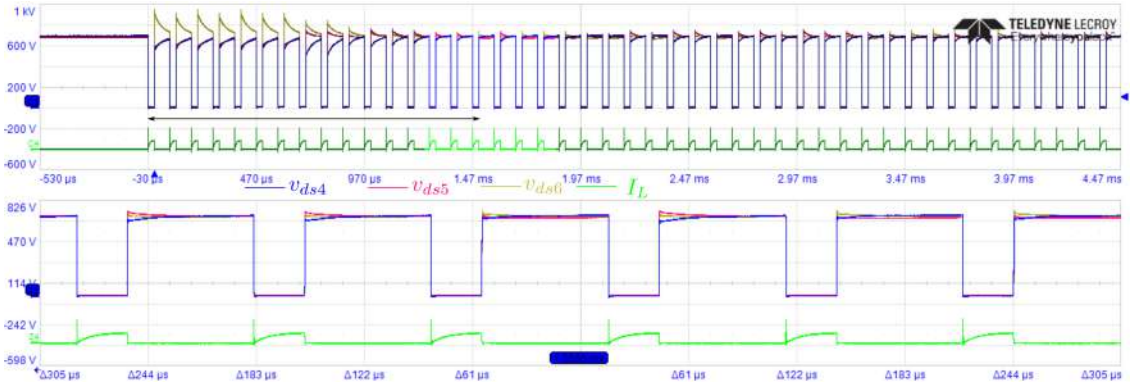

Fig. 4.38: With low frequency control of three device series connection transient (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-500us/div)

The higher load current operation is also performed to show the effectiveness of the proposed high frequency control. Fig.4.39 and Fig.4.40 shows the voltage balancing of three device in series connection at higher load current. As the load current is high enough for the channel current formation, the high frequency control takes care of voltage balancing. The high frequency control stage will correct the voltage imbalance at very first switching cycle itself. The sensed error will be very minimum and this makes the controller output to be low.

Fig.4.41 shows the freewheeling diode voltage imbalance of the top series connected

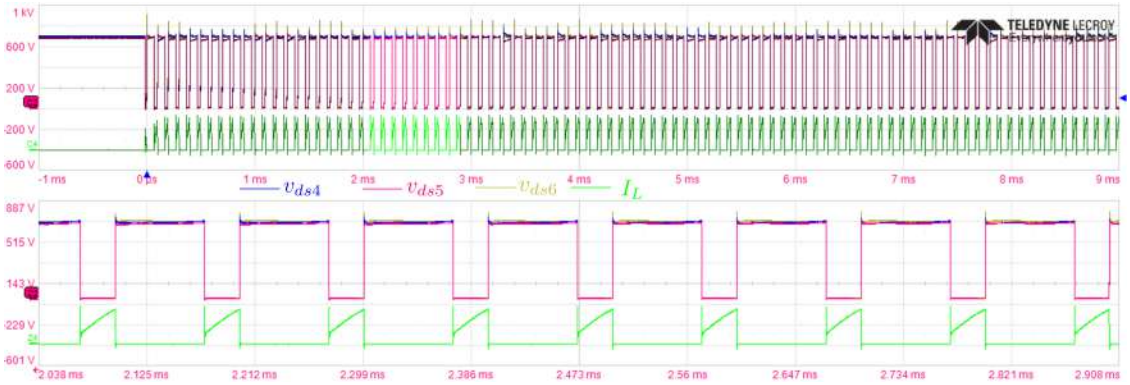

Fig. 4.39: Three device series connection at higher load current (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-1ms/div)

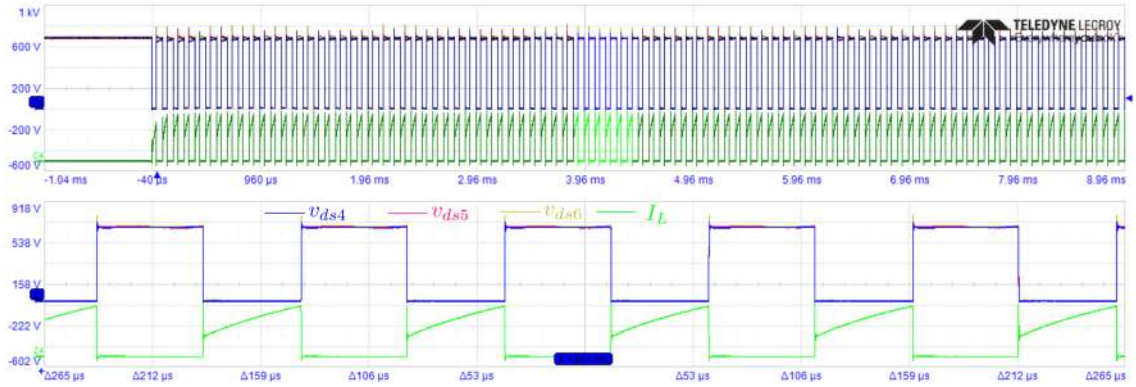

Fig. 4.40: Three device series connection at higher load current (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-1ms/div)

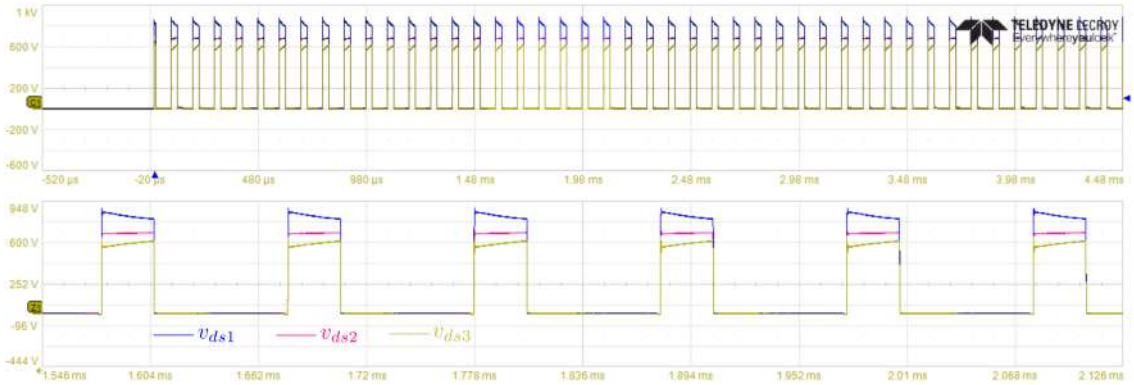

Fig. 4.41: Diode voltage unbalance of three device series connection (v_{ds1}-200V/div, v_{ds2}-200V/div, v_{ds3}-200V/div, and time-500us/div)

devices when diode balancing control is disabled. During the inductor current freewheeling time, anti parallel diodes S_1, S_2 and S_3 will be conducting. Once the freewheel duration is over, the devices S_4, S_5 and S_6 will start conducting. Anti parallel diodes S_1, S_2 and S_3 will be into reverse blocking mode. This event will be

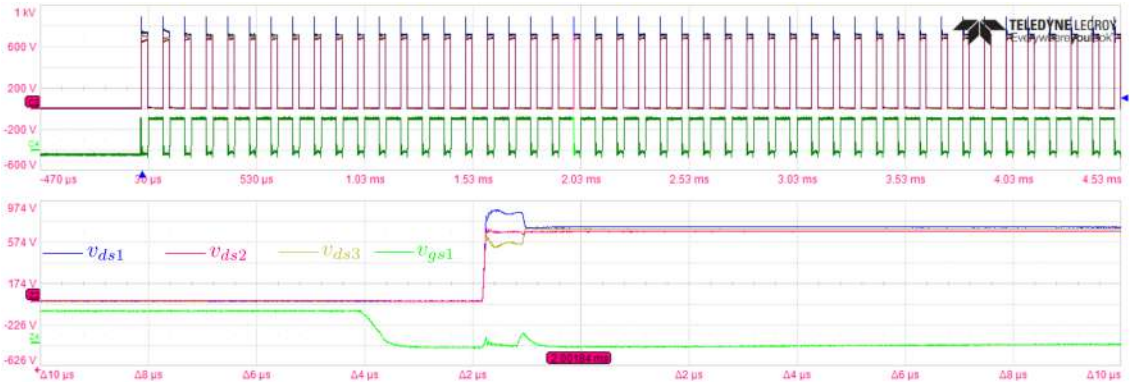

Fig. 4.42: Diode voltage balancing of three device series connection (v_{ds1}-200V/div, v_{ds2}-200V/div, v_{ds3}-200V/div,v_{gs1}-10V/div and time-1ms/div)

detected from the device voltage sensing as explained in the diode control hardware implementation stage. Since the gate voltage of the device is already below the threshold level, the proposed diode control is implemented to balance the diode reverse voltage. For three device in series connection, two over voltage limits are set. The device which crosses the limit will be partially turned on for active diode voltage balancing. Fig.4.42 shows the verification of the proposed diode voltage balancing technique.

Half bridge mode configuration

The experiment is further extended for half bridge inverter configuration to show the effectiveness of the proposed control in AC load current conditions. Fig.4.43 shows the series connected SiC MOSFETs in half bridge inverter configuration. Device S_1, S_2 and S_3 represents top series connected device and device S_4, S_5 and S_6 represents bottom series connected device.

The DC split capacitor C_1 and C_2 of each 2200uF capacitance and 2.5kV rated voltage is placed. The RL load of inductance 3mH and resistance of 10 ohm are used considering the fundamental sine frequency of 300Hz. The switching frequency and modulation index are 20kHz and 0.3 respectively. Fig.4.44 shows the voltage balancing of series connected devices. The load current I_L varies sinusoidally at 300Hz. During the positive cycle of the load current, series connected device will have hard turn off. From the waveform it can be seen at zero crossing of the load current the voltage imbalance is considerably large. This is due to the fact that very less switching

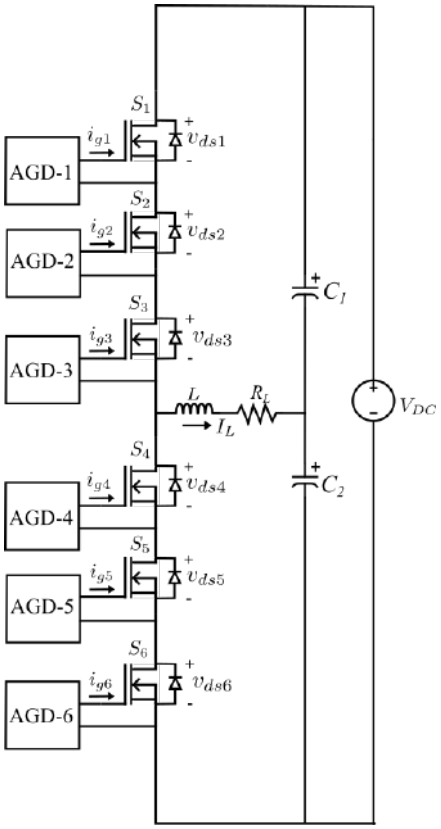

Fig. 4.43: Series connected devices in half bridge mode configuration

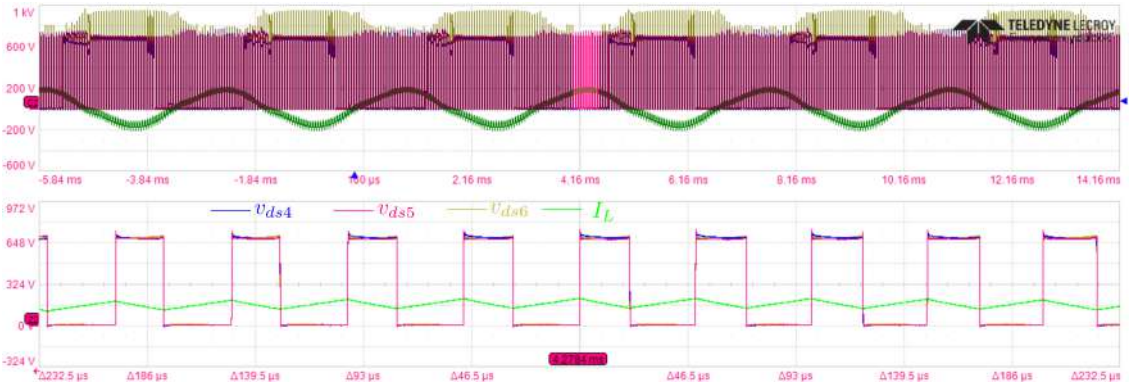

Fig. 4.44: Half bridge operation of three device series connection (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-2ms/div)

cycle are available for the closed loop control to balance at the low load current. As the load current goes to the positive cycle, the voltage imbalance is corrected by the high frequency control and difference becomes low. In the negative half cycle of the load current, diode of the top series connected device will undergo soft turn off and the proposed diode voltage balancing control is activated for the voltage balancing. Similarly Fig.4.45 and Fig.4.46 shows the transients results.

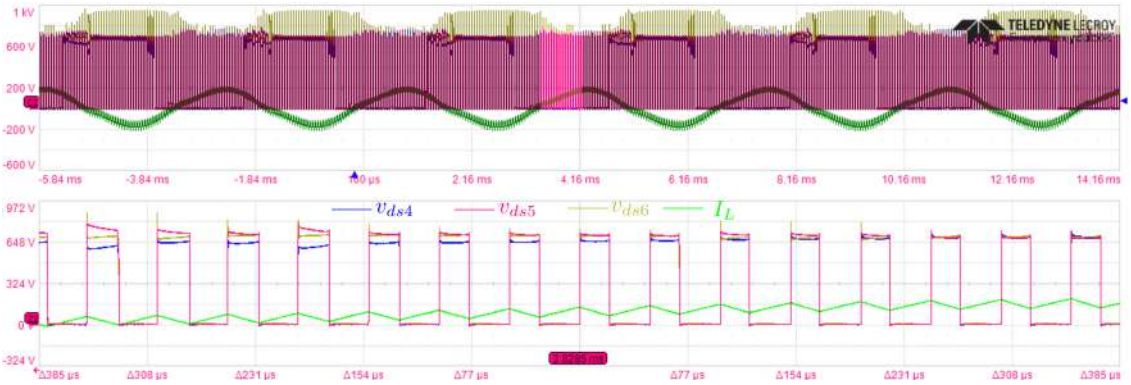

Fig. 4.45: Half bridge operation of three device series connection (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-2ms/div)

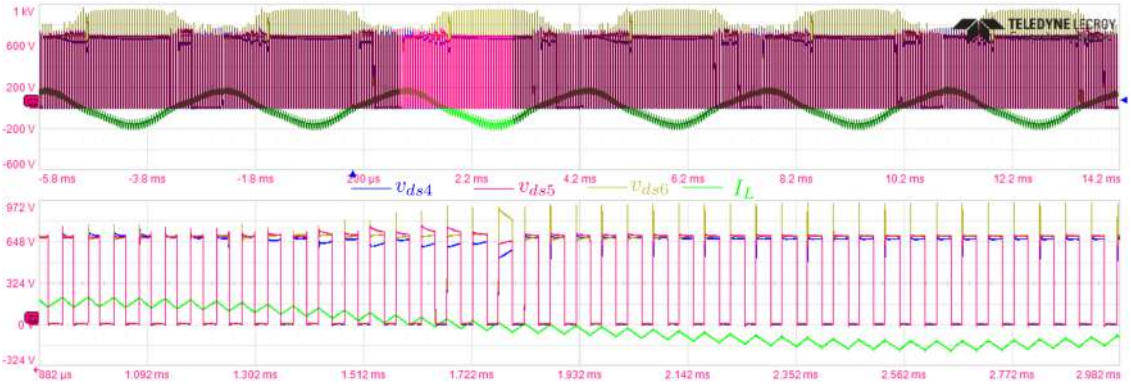

Fig. 4.46: Half bridge operation of three device series connection (v_{ds4}-200V/div, v_{ds5}-200V/div, v_{ds6}-200V/div,I_L-10A/div and time-2ms/div)

4.5 CONCLUSION

This chapter describes the detailed hardware implementation of the proposed SiC MOSFET series connection control technique. Implementation of turn on and turn off control, as well as considerations for selecting the component, are also presented. This chapter also discusses the hardware organisation of the proposed series connection as well as various hardware interconnections. The implementation is carried out with the help of an FPGA. The proposed Active Gate Driver has been extensively tested in a variety of power topologies. The chopper mode of operation is carried out at 1.2kV for two devices in series and 2.1kV for three devices in series at 5kHz. The results show that voltage balancing can be accomplished with a settling time of 2ms. In 1.2kV DC bus operation, the static imbalance is approximately 50V. It is less than 5% of the DC bus voltage. Similarly, steady state voltage difference of 60V is achieved at 2.1kV DC bus operation. The proposed diode voltage balancing technique also corrects the diode

voltage imbalance. The steady state voltage difference of the diode is maintained at 20V. The similar operations are carried out for buck converter mode and half bridge inverter mode. The buck converter operates in open loop configuration with 1.2kV DC bus and the output voltage is designed at 380V. This chapter presents the experimental results of the aforementioned operations. The half bridge inverter runs at 1.2kV for two devices and 2.1kV for three devices. Switching frequency of the converter is set at 10kHz. Based on the load requirement, fundamental sine frequency is set at 300Hz for three device in series connection. Results demonstrate the operation of the proposed control technique under various load current conditions.

CHAPTER 5

Short Circuit Protection Technique

5.1 INTRODUCTION

Under short circuit conditions, the reliability of SiC MOSFETs is critical for operation of a converter. Short-circuit withstanding time of SiC MOSFETs are significantly lower than Si devices. This chapter introduces a new adaptive blanking time based shoot through detection technique. The proposed method takes advantage of an active gate driver controller. It requires only device voltage sensing and gate pulse information as input to determine the shoot through condition. This chapter describes operation of the proposed shoot through detection method. The proposed technique reduces fault peak current magnitude with active turn off control by minimising the shoot through detection time. The proposed short circuit detection technique hardware results are also presented.

5.2 ADAPTIVE BLANKING TIME BASED SHOOT THROUGH DETECTION METHOD

The proposed method is based on the fact that the nature of the turn on switching transient differs from that of a short circuit event and can be easily identified by the device drain to source voltage transient. The normal turn on conditions and Hard Switched Fault (HSF) conditions are compared in this section. The HSF event can be detected simply by examining the HSF transient of the device drain to the source voltage. Based on this, working principle of the proposed method is explained. Fig.5.1 shows the test circuit in which S_1 and S_2 are two active switches. L_p represents the layout inductance of the power circuit. In order to create the short circuit event, switch S_1 is turned on first and after a time delay t_d the switch S_2 is turned on. Thus short-circuit event during turn on of switch S_2 is created. Fig.5.2 shows the gate pulse signal applied to the two switches. V_{GP1} and V_{GP2} are the two gate pulse signals applied to switch S_1 and S_2 respectively.

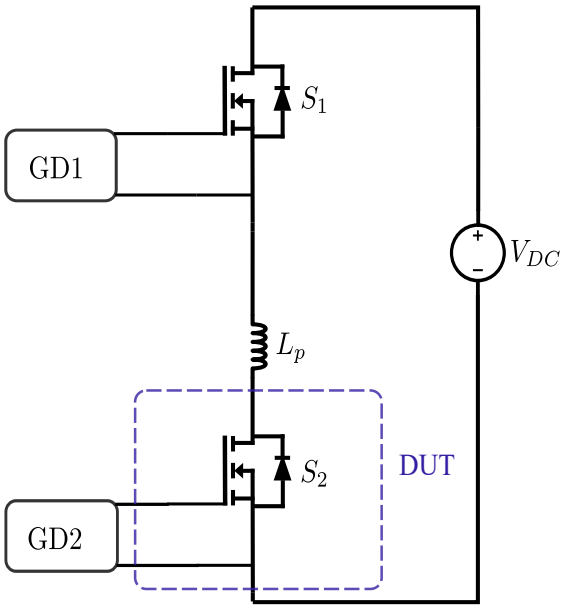

Fig. 5.1: Test condition for proposed protection method

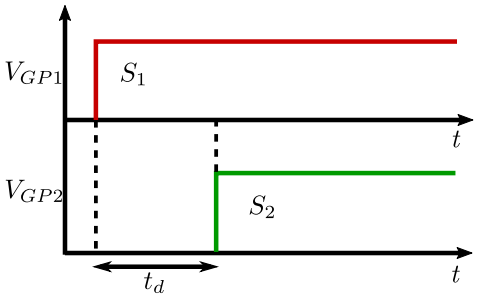

Fig. 5.2: Gate signal for the switches

Fig.5.3 shows the normal turn on transient where the device current increases first after the gate voltage crosses the threshold voltage. The voltage fall begins once the device reaches the Miller plateau voltage and the device eventually reaches to the on-state drop voltage as the gate increases towards the positive clamp voltage.

However, during the short circuit condition, the device conducts in saturation and drain current i_d increases. Due to this, the junction temperature increases and considerable power loss happens. The increase in temperature further reduces the channel carrier mobility charges, which slows down the increase of device current and stays at maximum saturation current. It can be seen that, the device voltage alone is enough to differentiate the HSF event from normal turn on transient.

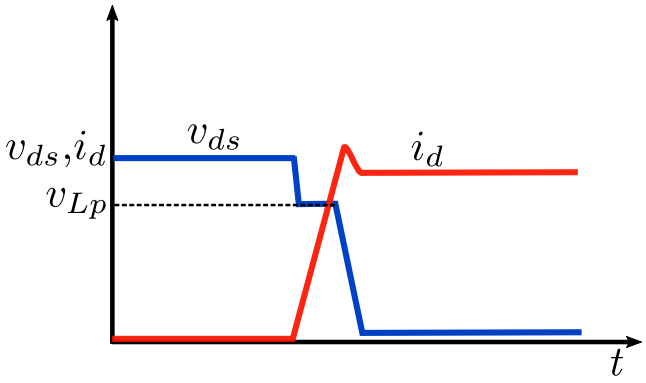

Fig. 5.3: Normal Turn-On switching transient

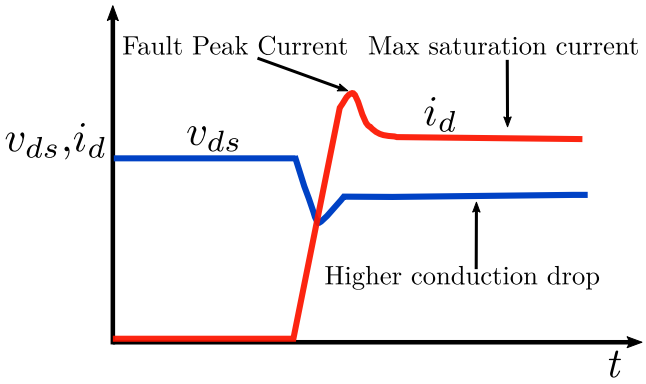

Fig. 5.4: HSF Turn-On switching transient

5.2.1 Working principle of the proposed method

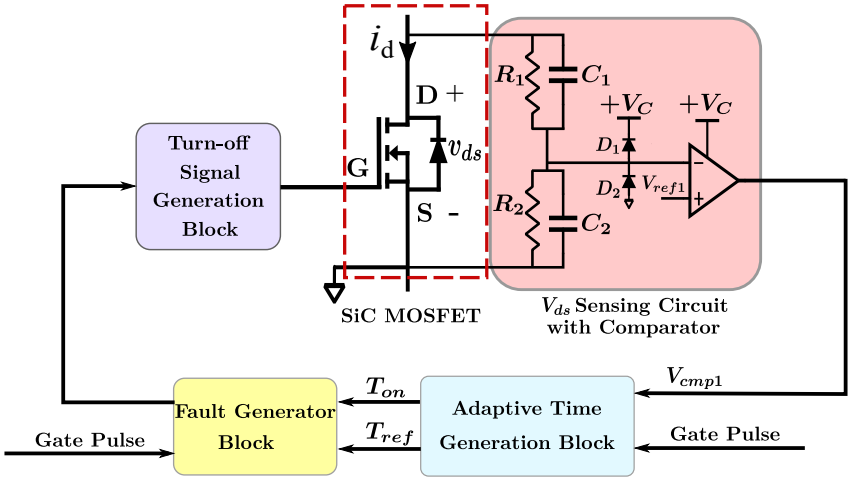

Fig. 5.5: Functional block diagram of proposed HSF detection method

The proposed method consists of v_{ds} Sensing circuit with a comparator, Adaptive time generation block, Fault generation block, and Turn off switching stage signal generation block as shown in Fig5.5. The v_{ds} sensing circuit consists of a resistor

divider with a lead compensated capacitor. The gain of the sensing stage can be adjusted by choosing proper value of R_1, R_2 and C_1 , C_2. The sensed v_{ds} signal is compared with V_{ref1}. The V_{ref1} selection will be discussed in the subsequent sections. Based on the comparator signal, adaptive time generation circuit is used to compute the turn-on switching time T_{on} at each switching cycle and the reference time T_{ref}. The T_{ref} time contains the information of the previous turn-on time as well as the maximum allowable load current change.

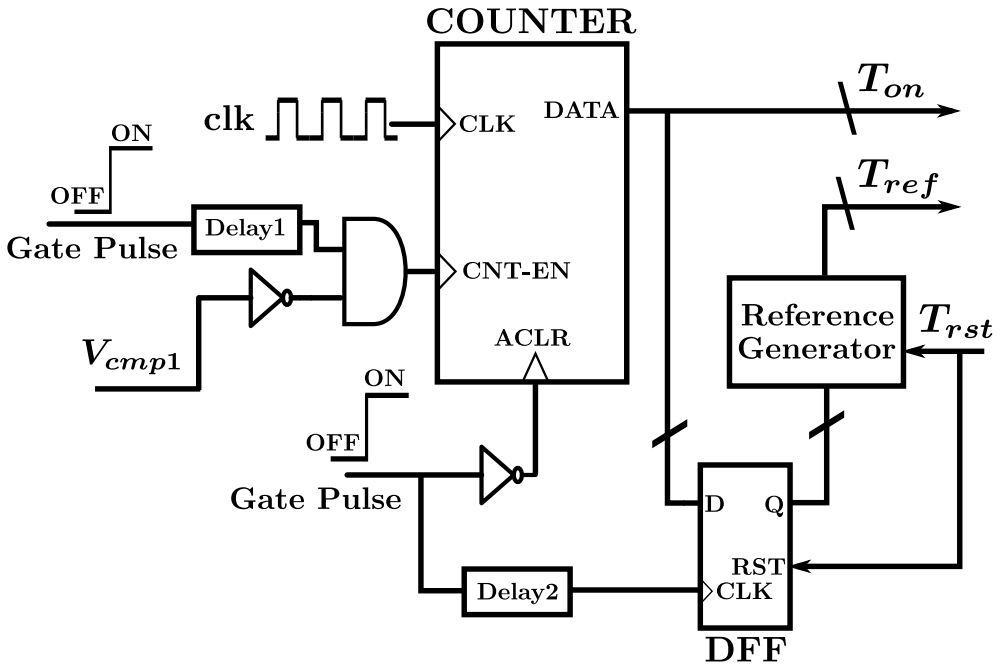

Fig. 5.6: Functional block diagram of proposed AGD

In each switching cycle, T_{ref} gets updated with the new value of turn on switching time T_{on}. In fault generation block, the turn on switching time T_{on} is compared with the reference time T_{ref} at the same switching cycle to detect the Hard Switching Fault (HSF) event. During normal turn on condition, the computed turn on switching time T_{on} at that switching cycle will always be lesser than the reference time T_{ref}. In the case of the HSF event, the computed turn on switching time T_{on} will be higher than the reference time T_{ref}. Hence, the fault is generated and the turn off stage is initiated.

The on board FPGA controller is used to implement the Adaptive time generation block. Fig.5.6 shows the computation of turn on switching time T_{on} and the reference time T_{ref}. Fig.5.7 shows the typical turn on transient under normal condition. As soon

as the Gate pulse V_{GP} is received, the current rise i_d starts after a turn on delay time (time interval t_1 to t_2) $t_{d(on)}$. The turn on delay time $t_{d(on)}$ can be expressed by (5.1) [14].

$$t_{d(on)} = \tau \ln(\frac{V_{GS}}{V_{GS} - V_{th}}) \tag{5.1}$$

Where τ represents time constant $R_g C_{iss}$. The delay1 block shown in Fig.5.6 contains the information of pre calculated turn on delay time T_{delay1}(as shown in Fig.5.7). This block is used to deduct the turn on delay time $t_{d(on)}$ from the instant the gate pulse V_{GP} is received. The time interval t_2 to t_4 shows the current rise time t_{ir} and voltage fall time t_{vf}. The V_{ref1} is selected such that the v_{ds} falls below 10% of the DC bus voltage (V_{DC}). When v_{ds} falls below the V_{ref1}, the output of the comparator signal V_{cmp1} (as shown in Fig.5.5) becomes high. The counter module is enabled at the rising edge of the gate pulse V_{GP} and disabled at the rising edge of the comparator signal V_{cmp1}. By this, the turn on switching time T_{on} is measured at the each turn on switching cycle. The counter is cleared at the falling edge of the gate pulse V_{GP}. This ensures the proper T_{on} measurement in the next switching cycle (t_2 to t_4). The reference time T_{ref} can be realised as following (5.2).

$$T_{ref}(N) = T_{on}(N-1) + T_{sf} \tag{5.2}$$

At any instant, the reference time of the current switching cycle T_{ref} contains the information of previous turn on switching time T_{on} and the safety factor time T_{sf}. T_{sf} represents the maximum allowable change in turn on switching time from previous switching cycle to current switching cycle. This accounts for maximum possible variation in drain current that occurs during consecutive turn on switching cycles. The computed turn on switching time T_{on} should be updated to the reference time T_{ref}. In normal turn on condition, the measured T_{on} time at each switching cycle remains constant after completion of the turn on switching transient. The D-Flip Flop (DFF) is used to sample the T_{on} time with Delay2 block. The Delay2 block contains the delay time T_{delay2} (in Fig.5.7) higher than the switching transient time (i.e higher than the reference time). The higher delay time T_{delay2} is provided for the proper update of T_{on}

switching time to generate T_{ref} time for next switching cycle. In case of HSF event, the T_{rst} signal is used to reset to the initial conditions. During the first switching cycle (N=1 in (5.2)), where $T_{on}(0)$ represents turn on switching time at 0A load current and it can be pre calculated using data sheet values or it can be measured experimentally at 0A load current.

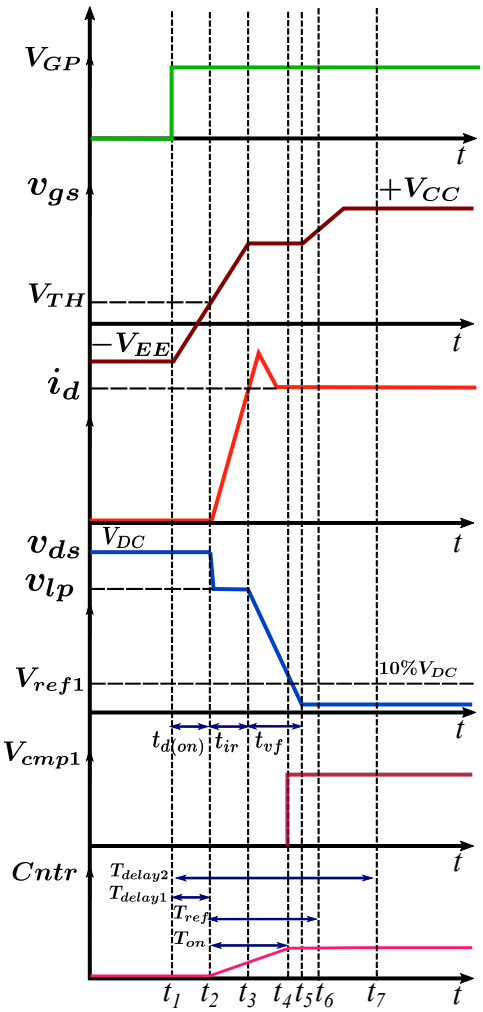

Fig. 5.7: Turn on switching waveform with proposed method

5.2.2 Fault generation Block

The Fault generation Block in Fig.5.8 consist of a digital comparator in which the turn on switching time T_{on} is compared with the reference time T_{ref}. If the turn on switching time T_{on} is lesser than the reference time T_{ref}, the output of the comparator becomes low (i.e normal turn on event). If the turn on switching time T_{on} is greater

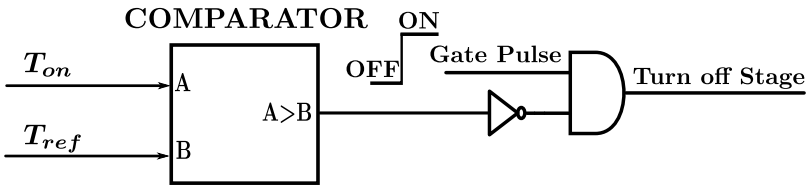

Fig. 5.8: Functional block diagram of proposed AGD

than the reference time T_{ref}, the output of the comparator becomes high. It indicates the current is still increasing and the Hard Switching Fault (HSF) has occurred.

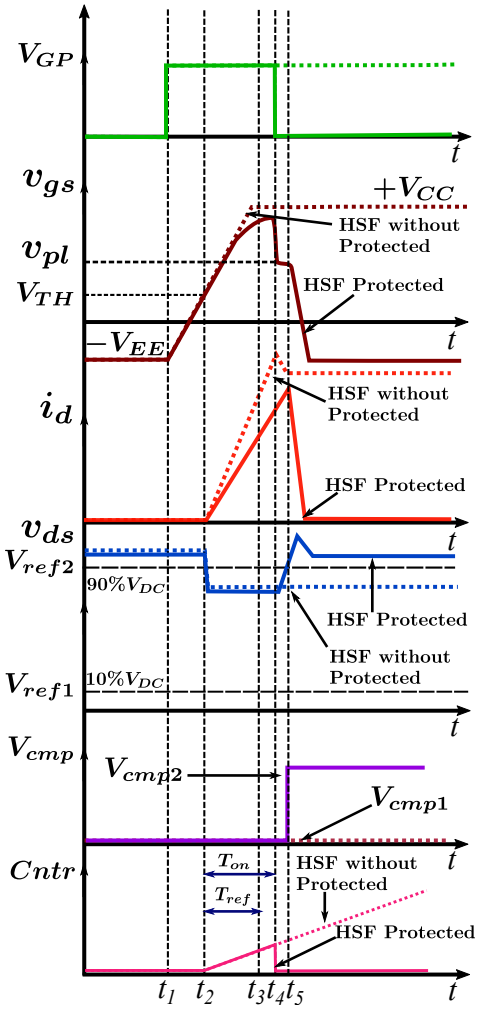

Fig. 5.9: Turn on waveform with HSF event

Fig.5.9 shows the turn on switching waveform during Hard Switched Fault (HSF) condition. In normal turn on switching cycle, the drain to source voltage v_{ds} falls below the V_{ref1} and the comparator output goes from low to high, the T_{on} time is estimated. The measured T_{on} time is instantly compared with T_{ref} time. During HSF

event the drain current i_d increases and the drain to source voltage v_{ds} will have a higher conduction drop and never reaches the set reference voltage V_{ref1}. Due to this, the comparator output stays at low and the counter used to measure T_{on} time will not be disabled. As the T_{on} time increases above the the reference time T_{ref}, the comparator output becomes high and the turn off is initiate. From the Fig.5.9 the time interval t_2 to t_3 shows the computed T_{ref} and at t_3 instant the T_{on} time exceeds the T_{ref}. The turn off is initiated at t_4 instant. Due to the faster detection, the turn off delay time is reduced and fast turn off can be achieved.

5.3 SIMULATION RESULTS

The proposed method is verified in LTspice simulation environment. Fig.5.10 shows the Hard Switching Fault result taken at 0A load current condition. The practical delays (Process delay time and Comparator delay) are not included in the simulation. However, the turn off delay time of the turn off stage is included in the simulation. The current limit is set at 25A. The total fault handling time is 60ns and the fault peak current is limited to 50A. Fig.5.11 shows the Hard Switching Fault result taken with varying DC

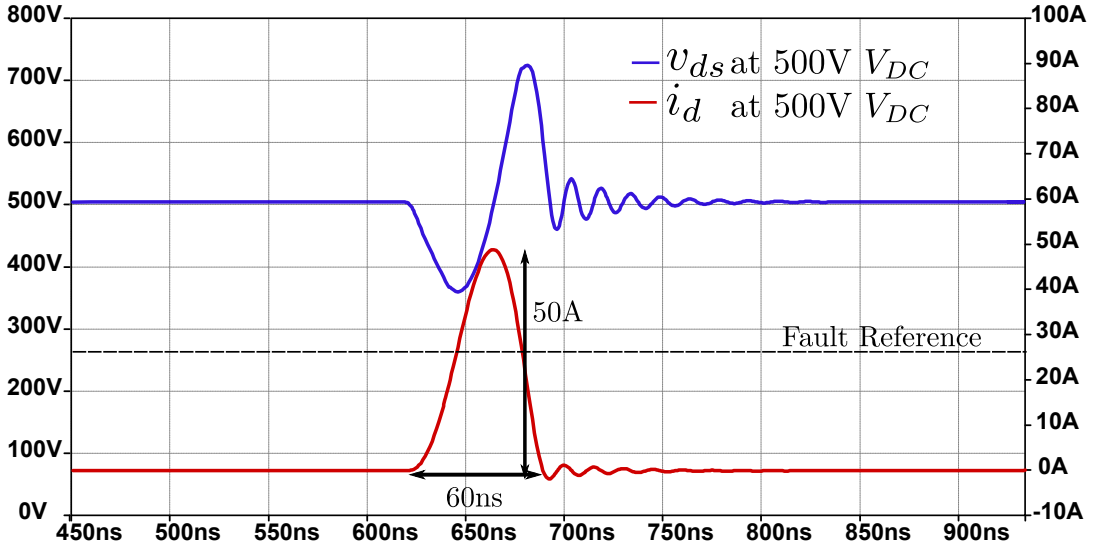

Fig. 5.10: Hard Switched Fault (HSF) Result at 0A Load Current (Voltage Scale:100V/div, Current Scale:10A/div, Time Scale: 50ns)

bus voltage. The lower the DC bus voltage, the lower the fault peak current. As the DC bus voltage increases, the magnitude of the fault peak current also increases. It is important to note that, the reference time calculation will also include the DC bus

voltage variation. The safety factor time T_{sf} can be varied to include the maximum deviation in the DC bus voltage and the junction temperature. Fig.5.12 shows the HSF event at different Junction temperature.

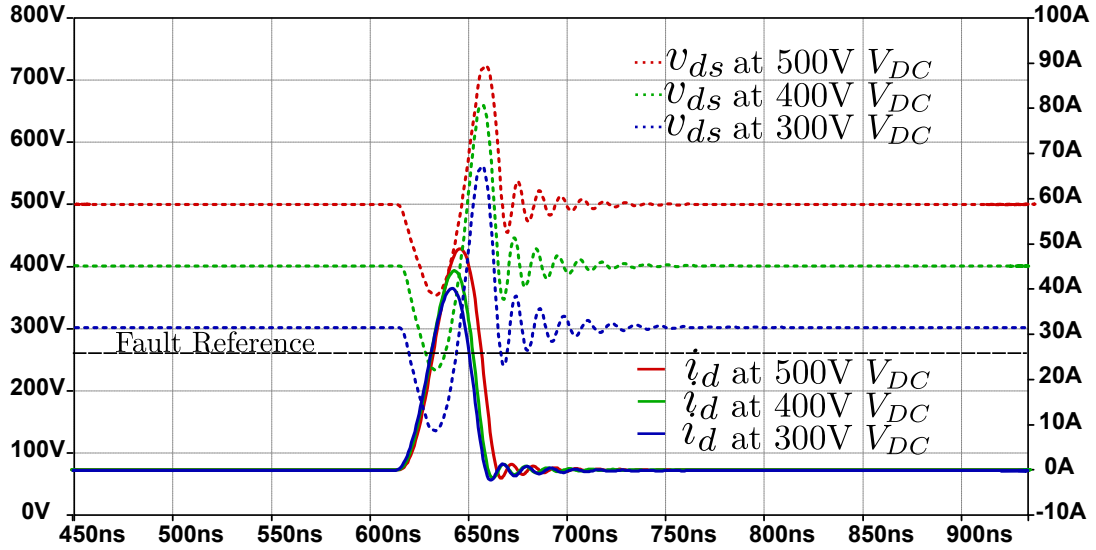

Fig. 5.11: HSF Result at varied DC bus voltage(Voltage Scale:100V/div, Current Scale:10A/div, Time Scale: 50ns)

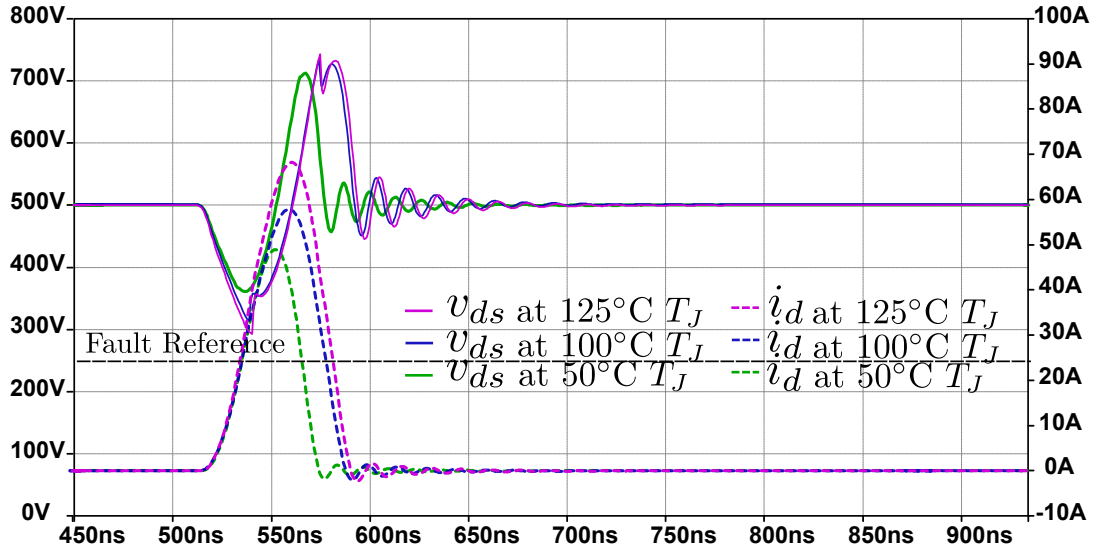

Fig. 5.12: HSF Result at varied Junction temperature(Voltage Scale:100V/div, Current Scale:10A/div, Time Scale: 50ns)

5.4 EXPERIMENTAL RESULTS

The proposed method is tested in Double Pulse Test (DPT) setup at 500V DC bus voltage as shown in Fig.5.13. CREE make part number C3M0065100K (1000V, 32A)

SiC MOSFET is used with 130nH layout inductance. The CPLD controller is operating with a clock frequency of 100MHz. The switching transient of the proposed method during Hard Switched Fault (HSF) is presented here.

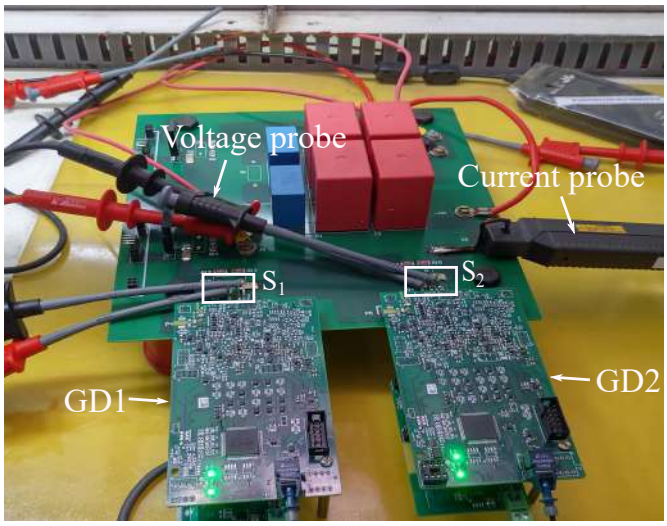

Fig. 5.13: Photo of Hardware test setup

The turn on switching time T_{on} is pre-calculated by data sheet values or by measuring experimentally. The calculated value of $T_{on}(0)$ at 0A load current is around 20ns. Fig.5.14 shows the measured turn-on time for 20A load current is 40ns. From this, the safety factor time T_{sf} can be estimated, which is around 40ns. The safety factor time includes the maximum change in the load current and the comparator signal delay time.

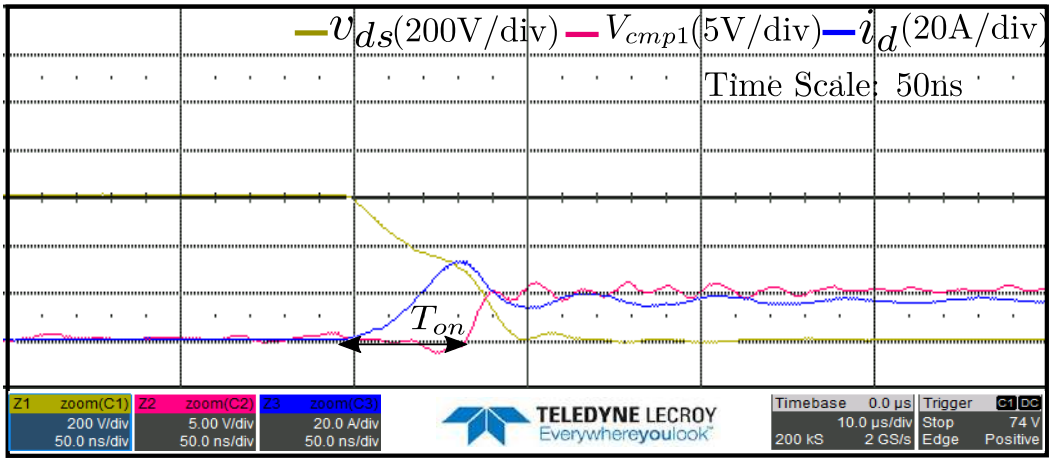

Fig. 5.14: Estimation of Turn-on time

Hence the total reference time T_{ref} can be calculated as 60ns. Fig.5.15 shows the

Hard Switched Fault (HSF) Result taken at 0A load current. The Fault current limit is set at 15A. T_{doff} represents the turn-off delay time which includes the comparator delay time and process delay time for generating the turn-off control signals. Due to the finite process delay time, the fault peak current is limited to 45A, and the total HSF time is 130ns (detection time, process time, and total turn off delay time)

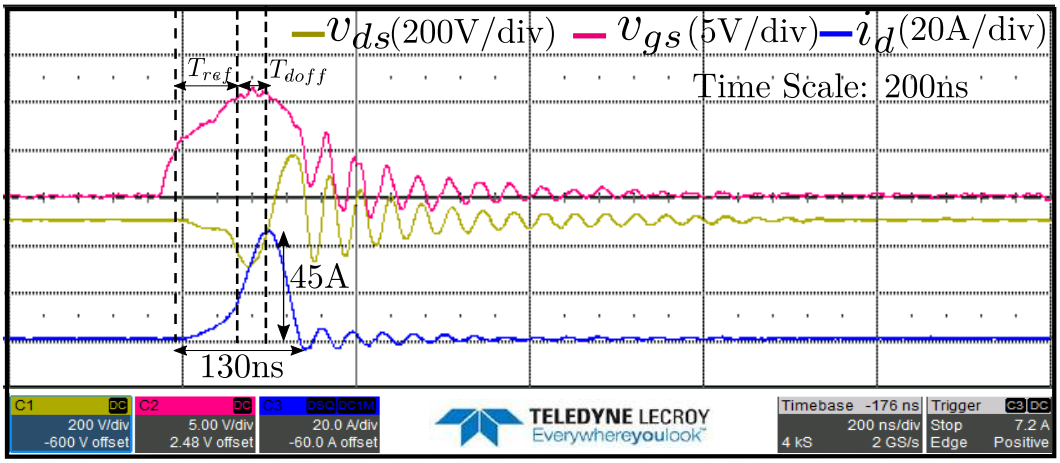

Fig. 5.15: Hard Switched Fault (HSF) Result at 0A Load Current

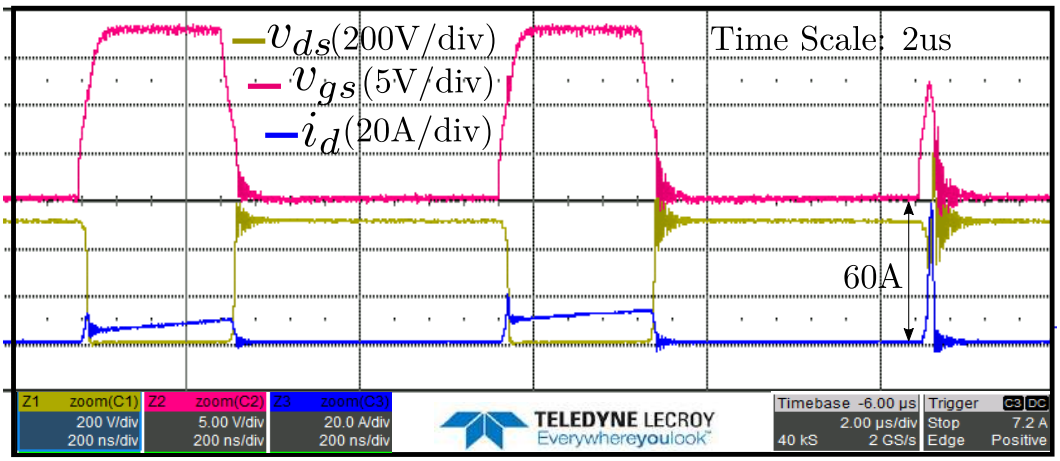

Fig. 5.16: Hard Switched Fault (HSF) Result at 15A Load Current

The Hard Switching Fault (HSF) event can happen at any load current. In order to show the effectiveness of the proposed method, HSF event is created at 15A load current. Fig.5.16 shows the HSF event at 15A load current. The Fault current limit is changed to 25A. It can be seen that, the maximum fault peak current is limited to 60A (as shown in Fig.5.17), which is within the safe operating area of the device. The results also show that the proposed method does not trigger false trip during the normal turn

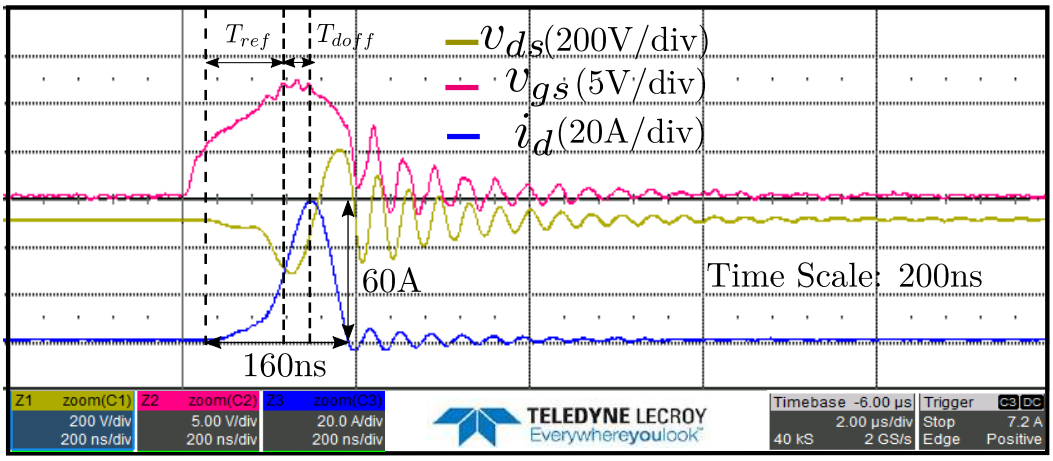

Fig. 5.17: Transient of Hard Switched Fault (HSF) Result at 15A Load Current

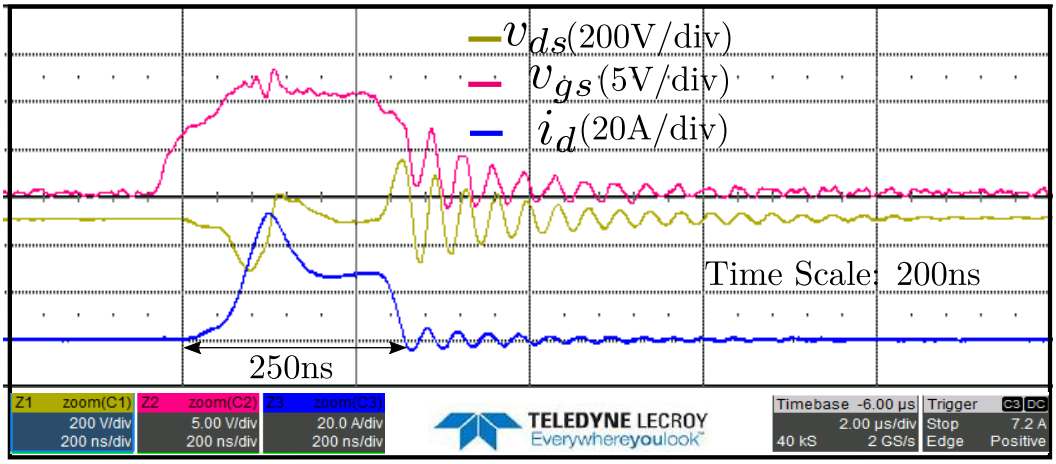

Fig. 5.18: Conventional 2-Level Turn-off

on switching. Fig.5.18 shows the proposed method with conventional 2- level turn off (2LTO) for 0A load current. During the turn off transient, an additional voltage level is introduced at the gate side using this method. The first voltage level is used to limit the fault current, and the gate voltage is clamped for a predetermined period of time. This limits the SiC MOSFET channel current and greatly reduces the drain to source voltage overshoot. The gate voltage is clamped to the recommended negative voltage after the fixed duration time. The total HSF time is 240ns which is higher than the active turn off, where the turn off delay time is significantly reduced.

5.5 CONCLUSION

This chapter explains how the proposed adaptive blanking time based shoot through fault detection technique. The proposed method only uses device voltage information to distinguish between a short circuit and a normal operating condition. To compute the blanking time, the proposed method employs digital logic within the FPGA. A timer based blanking time calculation logic is implemented inside the controller. This blanking time varies with each turn on time. This clearly distinguishes the blanking time required for low load current from that required for high load current. This eliminates the fixed blanking time present in the conventional desaturation technique for all load current operations. Both simulation and hardware experimentation are used to validate the proposed technique. The proposed method was primarily based on the turn on time that would be fed into the blanking time calculation model. As a result, before performing the short circuit test, the turn on time must be pre-calculated or experimentally calculated. The hardware results show a faster detection time of 50ns and a fault peak current limit of 45A with a total short circuit time of 130ns.

CHAPTER 6

Conclusion

6.1 SUMMARY AND CONCLUSION

The advantages of SiC MOSFETs over Si devices are well known. There is a pressing need for series connection for high voltage devices in medium power conversion. To meet the immediate need, a series connection of several low voltage SiC MOSFETs can be used instead of a single high voltage SiC MOSFET. On the other hand, series connection of several low voltage SiC MOSFETs introduces inherent difficulty of voltage balancing during turn off transients as well as in the steady state. The formation of parasitic capacitance in the switching node, as well as part-to-part parameter variation in SiC MOSFETs, causes these difficulties. Parasitics in the converter layout will play a larger role in voltage balancing. These are the primary drawbacks of series connecting SiC MOSFETs. Many techniques exists in the literature which takes an unique approach to solve the aforementioned problem. However, each method has its own advantages and disadvantages. An Active Gate Driver based approach is presented in this thesis to overcome the difficulties associated with series connections. Taking the benefits of an active gate driver, the reliability of SiC MOSFETs are improved by proposing an adaptive blanking time-based short circuit detection technique. This helps in faster detection of short circuit event in SiC MOSFET.

In this thesis, problems of series connection of SiC MOSFETs are thoroughly investigated. The switching transient model is provided for turn on and turn off transients. Analytical expressions for the series connected SiC MOSFET at turn on and turn off conditions are presented. In the modelling, the SiC MOSFET gate is assumed to be driven by a constant current source. If the device has a parameter mismatch or a gate pulse delay, there is an over voltage period in the turn on transient. Overvoltage causes more switching loss and can damage the device if it is not limited below the rated voltage. The turn off transient modelling is presented, and the analysis yields the

voltage imbalance parameters. According to the analysis, load current variation has a significant impact on voltage balancing. The device ($\frac{dv}{dt}$) is mainly decided by the gate current as well as the load current. The lower load current leads to lower ($\frac{dv}{dt}$) and higher load current leads to higher ($\frac{dv}{dt}$) for the same applied gate current i_g. The analysis of voltage balancing of body diodes due to unequal parasitic capacitance formation is also presented.

A three-stage control (two switched current source stages and one switched voltage source stage) has been proposed to independently control the turn on transients. The first two switched current source stages are operated to minimise the turn on over voltage. The third stage clamps the gate voltage to the recommended turn on gate voltage to reduce the on-state resistance. Similarly, the turn off transient is controlled by five stages. For diode voltage balancing, Off Stage 1 and 5 are coordinately operated. Off Stage-2, Off Stage-3, and Off Stage-4 are used to address voltage balancing for varying load current conditions. The detailed design and hardware implementation of the proposed control technique are also presented. The proposed series connection control techniques are validated experimentally. Experiment results for two device series connections at 1.2kV DC bus voltage and three device series connections at 2.1kV DC bus voltage are shown. The experimental results demonstrate the effect of the proposed voltage balancing control technique under various load current conditions. At 1.2kV and 2.1kV DC bus voltages, the results shows a maximum static voltage difference of 50V and 60V. This corresponds to less than 5% of the total DC bus voltage.

In the presence of short circuit conditions, reliability of SiC MOSFETs is critical for the converter's operation. SiC MOSFETs have a significantly lesser short circuit withstanding time than Si devices. The proposed method takes advantage of the benefits of an active gate driver controller and requires only device voltage sensing and gate pulse information as input to determine the shoot through condition. A timer based blanking time calculation logic is implemented inside the controller. This blanking time varies with every turn on time. This clearly distinguishes the blanking time required for lower load current from higher load current. This eliminates the fixed blanking time present in the conventional desaturation technique for all load current operations. Here, the reference time is compared with previous calculated turn on time. Based on this,

shoot through event can be detected instantly. The experimental verification of the proposed technique is implemented. The hardware results shows a faster detection time of 50ns and a fault peak current limit of 45A with a total short circuit time of 130ns.

6.2 THESIS CONTRIBUTIONS

The following are major contributions of this thesis.

(a) The thesis provides analytical expressions and switching transient behaviour of series connected SiC MOSFETs. The analytical expressions are approximated to second order and steady state terms are also derived.

(b) A separate turn on and turn off control stages are proposed to address the voltage balancing issues. Each stages are driven to control the $\frac{di}{dt}$, $\frac{dv}{dt}$ of the series connected SiC MOSFETs with voltage balancing.

(c) A low frequency control for series connection is proposed to address the varying load current conditions.

(d) Voltage balancing control technique of body diode of SiC MOSFETs are also presented and experimentally verified.

(e) An adaptive blanking time based shoot through detection technique has been developed and tested experimentally. The on-board detection uses only voltage sensing information to differentiate the shoot through from normal operation.

6.3 FUTURE SCOPE AND WORK

The following activities can be considered for continuation of the present work.

- Extending the series connection to multiple device for higher blocking voltage requirements.
- Extending the AGD to Asymmetric series connection of SiC MOSFETs.

APPENDIX A

SiC MOSFET Model

The mathematical model of SiC MOSFET presented in Chapter 3 is derived in detail in this appendix. Fig.A.1 represents equivalent circuit model for SiC MOSFET under parasitics.

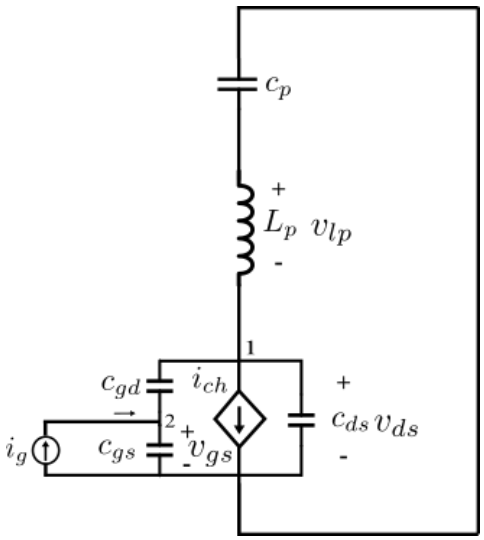

Fig. A.1: Equivalent circuit of SiC MOSFET

The SiC MOSFET is excited with current source and all the other sources are forced to zero (Voltage source are short circuited and current sources are open circuited). L_p represents equivalent layout inductance and C_p represents equivalent parasitic capacitance of the diode. The KCL is applied at node 2 to obtain the Eq.A.1

$$i_g = C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\frac{dv_{gd}}{dt} \tag{A.1}$$

The KVL at the outer loop of SiC MOSFET model is given by Eq.A.2

$$v_{gs} = v_{gd} + v_{ds} \tag{A.2}$$

Similarly, the KCl at node 1 is given by Eq.A.3

$$i_d = i_{ch} + i_{Cgd} + i_{Cds} \tag{A.3}$$

Differentiating the Eq.A.2 and substituting in Eq.A.1 is given by Eq.A.4

$$i_g = C_{iss}\frac{dv_{gs}}{dt} - C_{gd}\frac{dv_{ds}}{dt} \tag{A.4}$$

Applying Laplace transformation on Eq.A.4 is given by

$$I_g(s) = sC_{iss}V_{gs}(s) - sC_{gd}V_{ds}(s) \tag{A.5}$$

Eq.A.3 is expanded and Laplace transformation is applied.

$$I_d(s) = sC_{oss}V_{ds}(s) + (g_m - sC_{gd})V_{gs}(s) \tag{A.6}$$

From Eq.A.5, the expression for v_{gs} is given by

$$V_{gs}(s) = \frac{sC_{gd}V_{ds} - I_g(s)}{sC_{iss}} \tag{A.7}$$

Upon solving Eq.A.5 and Eq.A.6. The device drain to source voltage (v_{ds}) in terms of device drain current (i_d) and input gate current (i_g) is obtained.

$$V_{ds}(s) = \frac{sI_d(s)C_{iss} + I_g(s)[g_m - sC_{gd}]}{s[sC_{iss}C_{oss} + C_{gd}(g_m - sC_{gd})]} \tag{A.8}$$

The KVL in outer loop is given by

$$V_{ds}(s) = -(sL_p + \frac{1}{sC_p})I_d(s) \tag{A.9}$$

Solving Eq.A.9, Eq.A.8, and Eq.A.5. The device input to output transfer function can be obtained as

$$\frac{V_{ds}(s)}{I_g(s)} = \frac{g_m - sC_{gd} + s^2 g_m L_p C_p - s^3 L_p C_p C_{gd}}{S^4 K L_p C_p + S^3 C_{gd} L_p C_p + S^2(K + C_p C_{iss}) + s g_m C_{gd}} \tag{A.10}$$

The above transfer function can also be represented as

$$G_{vi}(s) = \frac{a_1 s^3 + b_1 s^2 + c_1 s + d_1}{a_2 s^4 + b_2 s^3 + c_2 s^2 + d_2 s}$$

where the coefficients of the s terms are given below

$a_1 = -L_p C_p C_{gd}$

$b_1 = L_p C_p g_m$

$c_1 = -C_{gd}$

$d_1 = g_m$

$a_2 = K L_p C_p$

$b_2 = L_p C_p g_m C_{gd}$

$c_2 = C_p C_{iss} + K$

$d_2 = g_m C_{gd}$

$K = C_{iss} C_{oss} - C_{gd}^2$

The above transfer function is used in the control modelling to design the PI controller for the proposed low frequency control operation.

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