HARDWARE IMPLEMENTATION OF CHANNEL DECODER FOR 5G NR

A project report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Hardware implementation of Channel Decoder for 5G NR**, submitted by **K JITHENDRA**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Data transmission using the 5G New Radio (NR) standard, from a transmitter to a receiver through a channel may introduce some bit errors in the received data due to noise and interference in the channel. But to get more reliable information from the data received at the receiver, the data needs to be error free. This raises a need to detect and correct errors present in the data received at the receiver. In 5G NR standard, Low Density Parity Check (LDPC) decoding is used to detect and correct the errors present in the received data in receiver.

This thesis work concentrates on the hardware implementation of Channel Decoder for 5G NR standard. Channel Decoder for Uplink Receiver in 5G NR is designed using Vivado High Level Synthesis (HLS). The verification and implementation of Channel Decoder is done in Vivado IP Integrator. Testing of Channel Decoder is done using Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit from Xilinx.

Due to confidentiality, only abstract is submitted. The complete thesis was submitted to Dr. Radha krishna Ganti. Please contact **rganti@ee.iitm.ac.in** to get access to full thesis.