Design of an 800 MHz Clock Generator for High-Speed $\Delta\Sigma$ ADC

A Project Report

submitted by

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in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY MADRAS

JULY 2020

CERTIFICATE

This is to certify that the thesis (or project report) titled **Design of an 800 MHz Clock Generator for High-Speed $\Delta\Sigma$ ADC**, submitted by **JOSE K SEBASTIAN**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis (or project report), in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 10th Aug 2020

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ACKNOWLEDGEMENTS

First of all I offer my sincere gratitude to my mentor Dr. Nagendra Krishnapura for providing me an opportunity to work under him. The way he made me analyze the problem kept me interested with the work. The feedbacks he provided kept me engaged all the time.

I convey my gratitude to Aditya Narayanan for his support during the entire course of the project. The discussions we had for the design was helpfull throughout. I would like to thank Ashwin, Ashish, Aswani, Chithra, Naveen, Sumit for helping with the design tools. I thank my parents and sister for all their support.

ABSTRACT

This work presents a design topology for implementing high-speed clocks. Here an 800 MHz clock is designed in UMC180nm technology. The clock is made using a PLL with 5 MHz reference frequency. The total power consumed by the PLL is 8.8mW. The nearest spur(at 5 MHz) has an attenuation of 68 dB and the estimated jitter is 4.2ps. This clock was used to drive a $\Delta\Sigma$ ADC,(which had an SNR of 118dB with ideal clock) and the SNR obtained is 110.3dB.

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ABBREVIATIONS

PLL	Phase Locked Loop
VCO	Voltage controlled oscillator
PFD	Phase frequency detector
LF	Loop filter
CP	Charge pump
DFF	D-Flipflop
PSD	Power Spectral Density
HB	Harmonic Balance

NOTATION

$g_{m\,n}$	Transconductance of nMOS
$g_{m\,p}$	Transconductance of pMOS
g_{ds}	Drain to source conductance
ω_{UGF}	Unity gain frequency

CHAPTER 1

Introduction

1.1 Motivation

A PLL synthesizer can generate stable output frequency from a lower frequency input. This can be used as a clock for high-speed circuits. This work describes the design of an 800 MHz clock used to drive a $\Delta\Sigma$ ADC.

1.2 Principle of operation

The PLL is implemented using the block diagram given in Fig. 1.1. It consists of a reference frequency generator, phase-frequency detector(PFD), loop filter, VCO, and a reference divider. The voltage across the loop filter acts as the control voltage for the VCO. With this control voltage, the VCO oscillates at a certain frequency. The frequency thus generated then passes through the divider and the phase is then compared with the phase of reference frequency using the PFD. The corresponding output from the PFD drives the charge pump, which drives the loop filter. The entire system acts as a negative feedback system and the output phase of the VCO locks with the phase of the reference frequency.

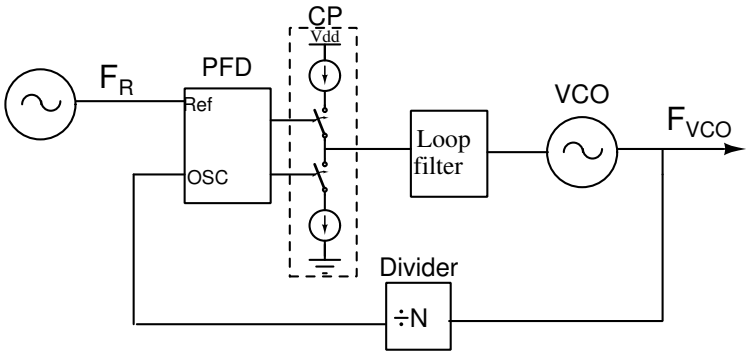


Fig. 1.1: PLL block diagram

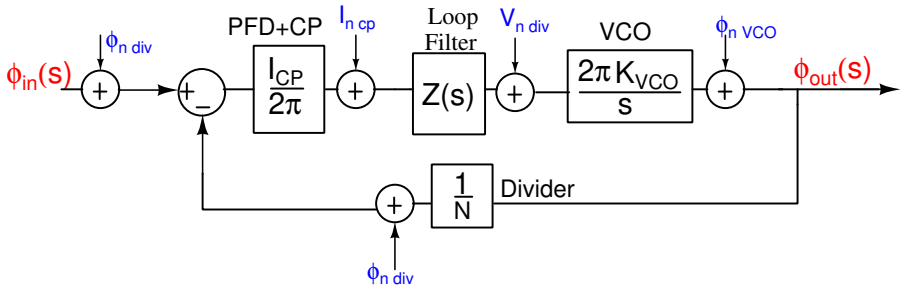


Fig. 1.2: PLL phase domain model

1.3 Performance parameters

The quality of a PLL can be measured using the following parameters.

1.3.1 Phase noise

Different components in the PLL contributes the noise to PLL. Fig.1.2 shows the phase model of the PLL. The phase noise at the output will decide the jitter in the clock.
The transfer functions from different noise sources to output are :

$$TF_{inp} = \phi_{out}/\phi_{n\,in} = \frac{NI_{cp}K_{VCO}Z(s)}{Ns + I_{cp}K_{VCO}Z(s)} \tag{1.1}$$

$$TF_{div} = \phi_{out}/\phi_{n\,div} = \frac{NI_{cp}K_{VCO}Z(s)}{Ns + I_{cp}K_{VCO}Z(s)} \tag{1.2}$$

$$TF_{CP} = \phi_{out}/I_{n\,CP} = \frac{2\pi N K_{VCO} Z(s)}{Ns + I_{cp} K_{VCO} Z(s)} \tag{1.3}$$

$$TF_{LF} = \phi_{out}/V_{n\,LF} = \frac{2\pi N K_{VCO}}{Ns + I_{cp} K_{VCO} Z(s)} \tag{1.4}$$

$$TF_{VCO} = \phi_{out}/\phi_{n\,VCO} = \frac{Ns}{Ns + I_{cp} K_{VCO} Z(s)} \tag{1.5}$$

Where N is the divider ratio, I_{cp} is the charge pump current, $Z(s)$ is the loop filter impedance, K_{VCO} is the oscillator gain. Also, ϕ_{in} is the phase noise from the reference generator, $\phi_{n\,div}$ is the phase noise due to the divider, ϕ_{nVCO} is the phase noise due to VCO. $I_{n\,CP}$ is the noise current from PFD and CP, $V_{n\,LF}$ is the noise from the loop filter.

Therefore the PSD of the noise at the output will be the PSD of noise at input multiplied by the magnitude square of the transfer function. From the equations, it is clear that the noises from the divider, reference frequency generator, PFD and the charge pump are having the low pass behaviour and the VCO noise at the output will have a high pass behaviour. By adjusting the bandwidth of the PLL loop, we can minimize the total noise.

1.3.2 Reference spur level

The voltage across the loop filter will be periodic at the reference frequency. This introduces spurs at the output with the reference frequency and its harmonics.

1.3.3 Stability of the PLL

The phase margin of the loop should be adjusted to obtain good stability. Since the K_{VCO} changes with respect to VCO's input voltage, the phase margin should be evaluated for different values of K_{VCO}.

CHAPTER 2

VCO Design

2.1 VCO Architecture

Several topologies are available for voltage-controlled oscillators, namely ring oscillators, relaxation oscillators, and LC oscillators. The ring oscillator can be made by cascading an odd number of single-ended inverters. Even though a more extensive range can be obtained using ring oscillators, the poor phase noise performance makes them unsuitable for a low jitter PLL. On the other hand, LC oscillators come with excellent phase noise performance making them suitable for PLL applications. However, the size of inductors and capacitors makes the circuit bulky compared with a ring oscillator.
An LC VCO can be made using differential cross-coupled pairs with a current mirror. A complementary cross-coupled pair (contains both nMOS and pMOS cross-coupled pairs) helps in increasing the amplitude of oscillation for the same current as in nMOS or pMOS cross-coupled pairs.
The quality of VCO can be estimated by a figure of merit

$$FOM = -L\left(\Delta f\right) + 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1mW}\right) \tag{2.1}$$

Where Δf is the offset frequency, $L(\Delta f)$ is the phase noise at the offset frequency, f_0 is the oscillation frequency and P_{dc} is the power consumed in mW.

2.2 Complementary CMOS LC Oscillator

Figure 2.1 shows an LC VCO using nMOS cross-coupled transistors, inductors and varactors, biased using a tail current source. The parasitics resistance present in the LC

tank contributes to the losses in the tank. The negative resistance given by the cross-coupled pair compensates for these losses. The drain current of the transistors swings between 0 and I_0, as shown in the Figure 2.1. So amplitude of oscillation produced will be I_0 time impedance seen from the source, which is R/2 in parallel with L/2 and 2C. In the case of a complementary cross-coupled pair Figure 2.2, the effective impedance seen by the current will be R in parallel with the L and C, thereby increasing the amplitude of oscillation for the same current [2]. The latter configuration is used as it gives more amplitude of oscillation for the same current.

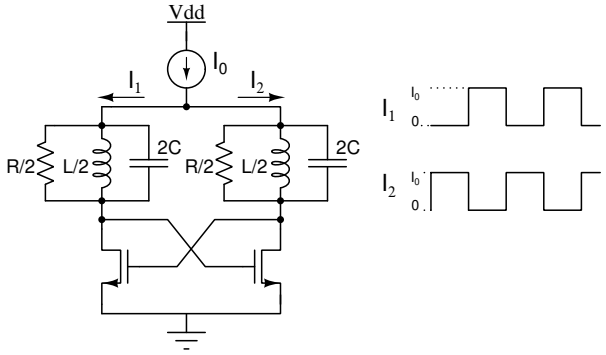


Fig. 2.1: LC VCO using nMOS cross-coupled pair

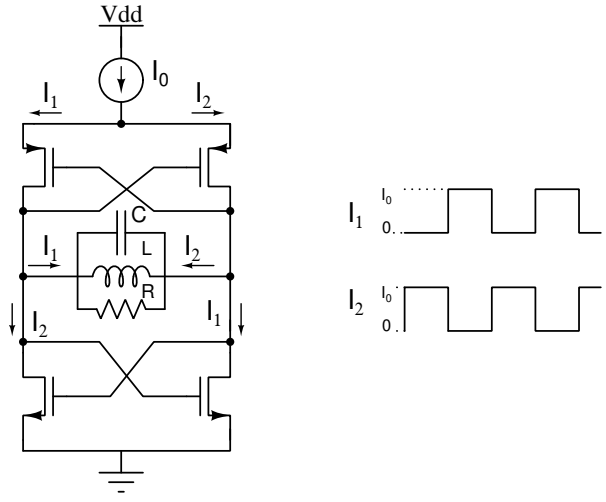


Fig. 2.2: LC VCO using nMOS and pMOS cross-coupled pair

2.3 Design

The frequency of oscillation was chosen to be f_{osc} = 800 MHz . The oscillation should have an appreciable amplitude and frequency range. The VCO should also have a good phase noise performance. Figure 2.3 shows the different components in the VCO.

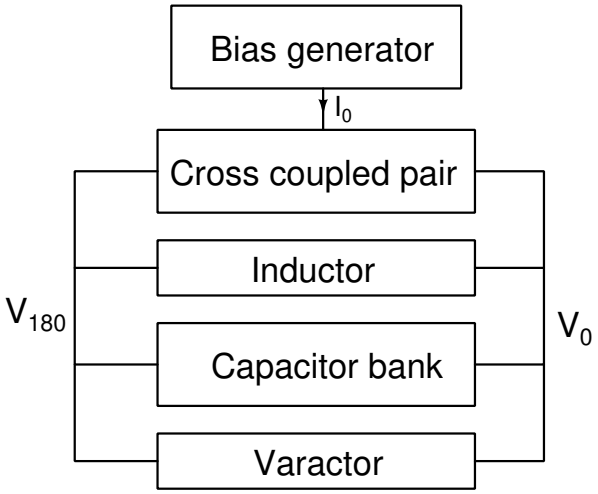


Fig. 2.3: VCO block diagram

2.3.1 Inductor

For better phase noise performance, the LC tank should have a high quality factor(Q). At 800 MHz the Q of the tank is dominated by the inductor. The Q of the inductor is proportional to the inductance value. However, high inductance value will consume a large area and use a long wire, which will have a higher resistance. The inductor was laid out, as shown in Figure 2.4. The width and spacing between the turns should be adjusted to increase the Q of the inductor. The inductor value was extracted using the EMX tool and the values were measured using a port.

Inductance value = 12.366 nH

Q = imaginary part of voltage / real part of voltage = 6.7

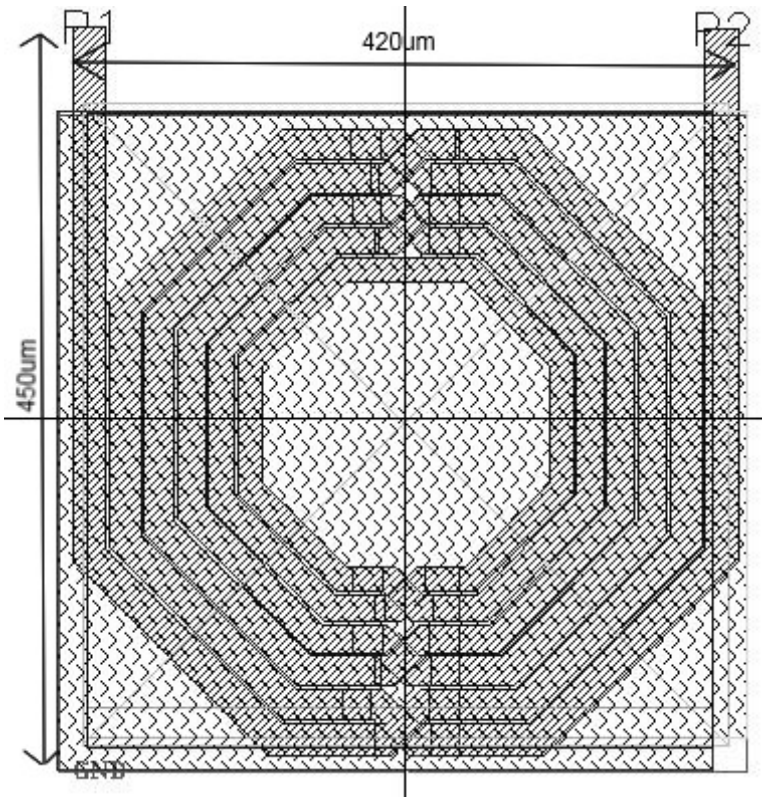


Fig. 2.4: Inductor Layout

2.3.2 Capacitor bank

From the obtained value of L, the capacitor value required was found to be 3.208 pF. To account for the variations in capacitor values, the total capacitance is implemented using a fixed capacitor of value 1.8 pF and a 3 bit capacitor bank of LSB corresponding to 200 fF . The switches sizes were adjusted to produce a high Q capacitor bank during turn on and OFF condition. If the control bit ct1 is low, since ct1b is high, turns the MOSFET M1 M2 'ON'. Therefore it introduces a capacitor C3 series with C4 across the terminals, changing the terminals effective capacitance. The other switches are off introduces large resistance and low capacitance(very less compared to the total capacitance) to be added in parallel across the terminal. The mimcap was used for the implementation of the capacitor bank.

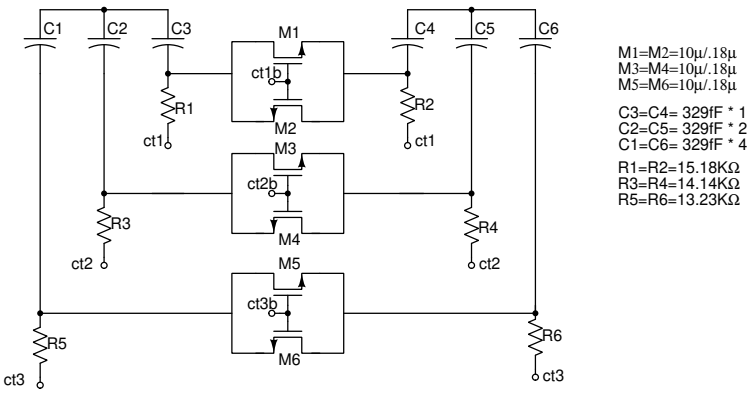


Fig. 2.5: Capacitor bank circuit

2.3.3 Cross-coupled pair

The LC tank will introduce a parallel resistance to the circuit, thereby damping the oscillations. To compensate for the losses, a negative resistance is added using a cross-coupled pair, as shown in Figure 2.6. The LC tank introduces approx. 390 Ω to the circuit. The cross-coupled pair should produce a negative resistance of R_{neg} such that its magnitude is less than 390 Ω , so that the effective resistance is negative.
The negative impedance provided by the cross-coupled pair,

$$R_{neg} = \frac{-2}{g_{mn} - g_{ds}} || \frac{-2}{g_{mp} - g_{ds}} \tag{2.2}$$

The g_{mn} and g_{mp} were adjusted to give the R_{neg} to -140Ω

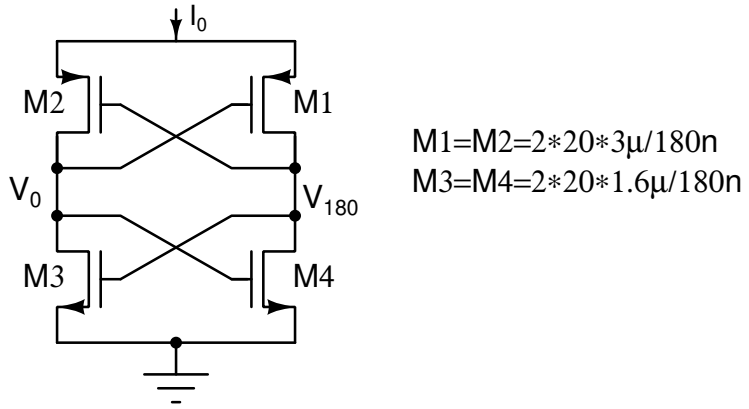


Fig. 2.6: Cross-Coupled pair

2.3.4 Varactor

As we need to change the oscillation frequency with a control voltage, a varactor is placed in parallel with the capacitor. The varactor tunes the value of capacitor to the applied voltage. The minimum change in the capacitor value of the varactor should be higher than the LSB of the capacitor bank. The common voltage of the circuit should be adjusted to make the varactor functional with the control voltage. The common-mode voltage can be adjusted by tweaking the size of lower nMOS transistors.

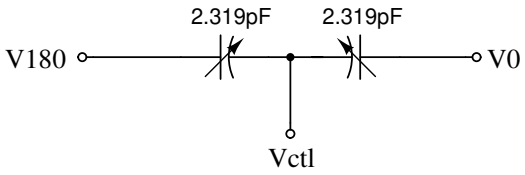


Fig. 2.7: Varactor

2.4 Results

HB simulations were run on the designed VCO to verify the operation of the VCO at different PVT variations.

The following values for the respective were obtained from the schematic:

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise@ offset of 100kHz(dBc/Hz)	Tunning Range (MHz)
TT	1.8	0	0	360	6.14	954.5	-108.0	728 - 934
	0	1.8	1.8	598	6.14	948	-106.7	
	0	1.8	0	807	6.14	946	-104.8	
	0	0	1.8	1140	6.12	955	-104.8	
SS	1.8	1.8	0	301	4.7	842	-108.54	691 - 904
	1.8	0	1.8	546	4.77	837	-105.8	
	1.8	0	0	761	4.76	842	-107.6	
	0	1.8	1.8	1131	4.76	838	-107.6	
FF	0	1.8	0	439	7.97	1085	-104.8	764 - 949
	0	0	1.8	677	7.96	1085	-105.0	
	0	0	0	888	7.91	1099	-103.9	

Table 2.1: Schematic simulation results of VCO

So the worst case results are :

$$\text{Tunning Range} = 764\,\text{MHz} \;\; to \;\; 904\,\text{MHz}$$

$$\text{Power consumption} = 7.97mW$$

$$\text{Amplitude} = 418mV$$

The Schematic results are as given below :

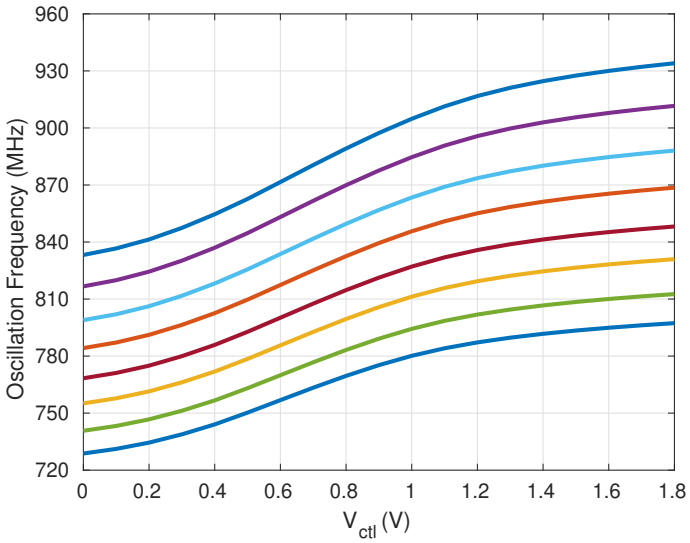


Fig. 2.8: Frequency characteristics in TT corner at 50^oC

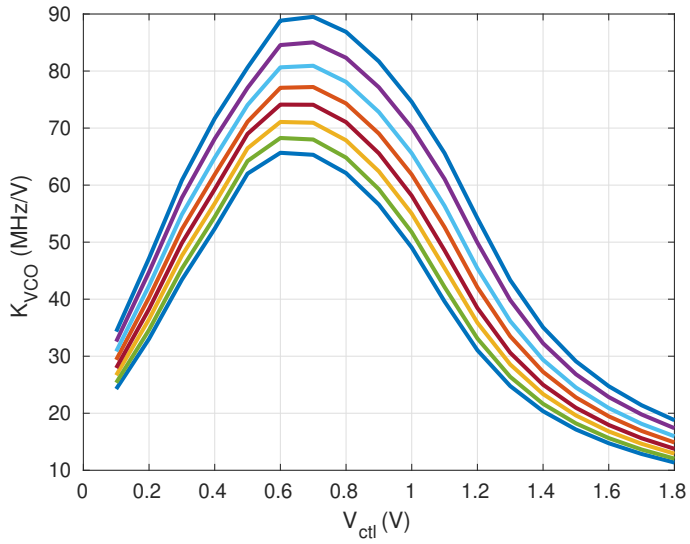


Fig. 2.9: K_{VCO} characteristics in TT corner at 0^oC

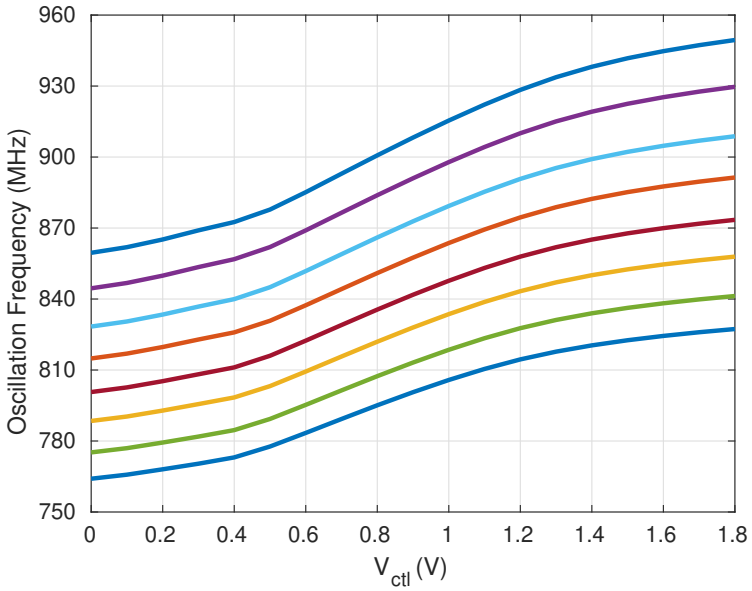


Fig. 2.10: Frequency characteristics in FF corner at 0^oC

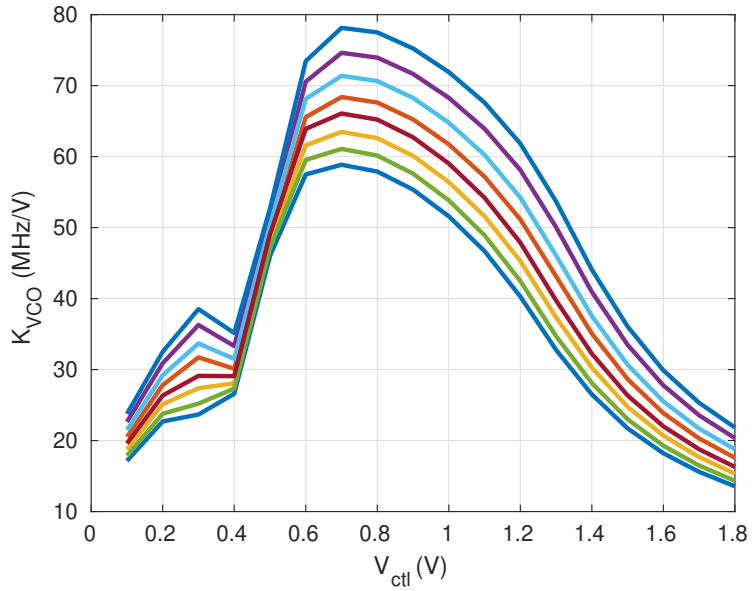


Fig. 2.11: K_{VCO} characteristics in FF corner at 0^oC

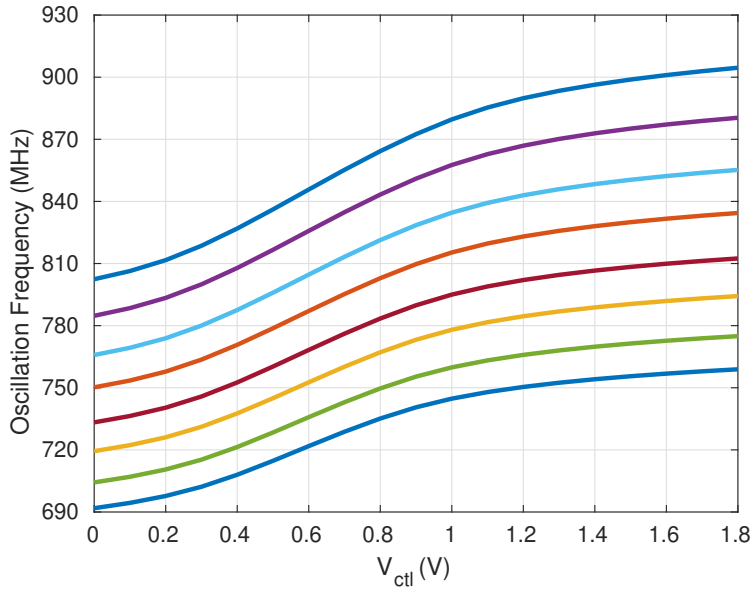


Fig. 2.12: Frequency characteristics in SS corner at 100^oC

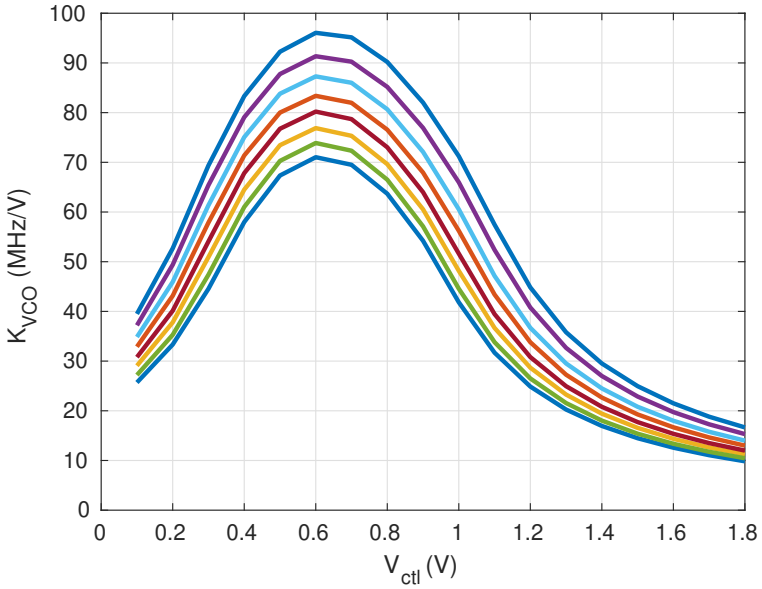


Fig. 2.13: K_{VCO} characteristics in SS corner at 100^oC

The layout simulation gave the following results :

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise @ 100kHz offset (dBc/Hz)	FOM (dB)	Tunning Range (MHz)
TT	1.8	1.8	0	254	6.29	939	-107.8	177.8	712 - 896
	1.8	0	1.8	512	6.3	933	-105.1	175.16	
	1.8	0	0	687	6.28	929	-104.8	174.87	
	0	1.8	1.8	948	6.29	955	-106.1	176.1	
	0	1.8	0	1313	6.27	940	-108.4	178.4	
SS	1.8	1.8	1.8	456	4.9	828	-102.0	175.8	676 - 865
	1.8	1.8	0	640	4.9	828	-101.5	176	
	1.8	0	1.8	901	4.9	824	-103.6	175.4	
	1.8	0	0	1343	4.89	830	-108.3	175	
FF	0	1.8	1.8	555	8.17	1057	-106.9	173.1	749 - 919
	0	1.8	0	721	8.15	1057	-107.1	172.6	
	0	0	1.8	952	8.15	1064	-106.5	174.75	
	0	0	0	1195	8.09	1078	-106.1	179.4	

Table 2.2: Layout simulation results of VCO

So the worst case results are :

$$\text{Tunning Range} = 749\,\text{MHz} \;\; to \;\; 865\,\text{MHz}$$

$$\text{Power consumption} = 8.17mW \text{ (including buffers)}$$

$$\text{Amplitude} = 400mV$$

$$\text{FOM} = \;\; 172dB$$

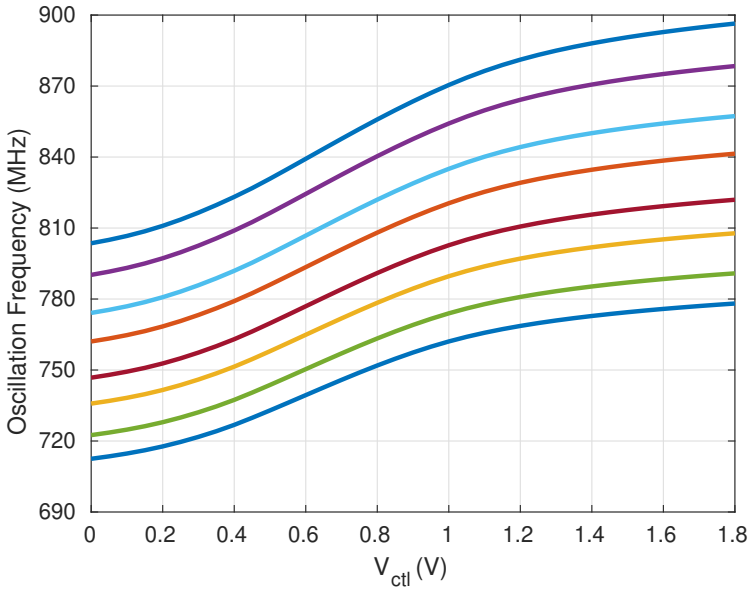


Fig. 2.14: Frequency characteristics in TT corner at 50^oC

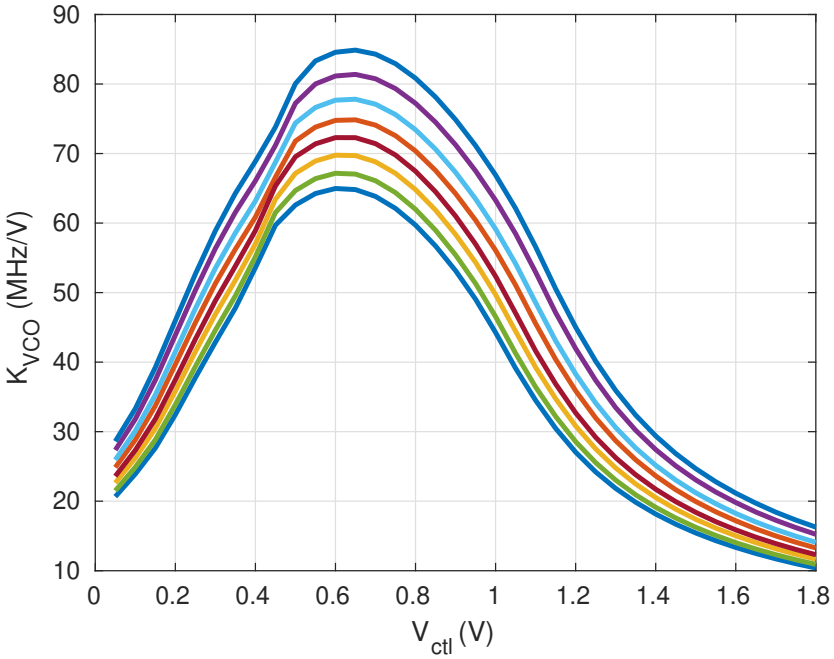


Fig. 2.15: K_{VCO} characteristics in TT corner at 0^oC

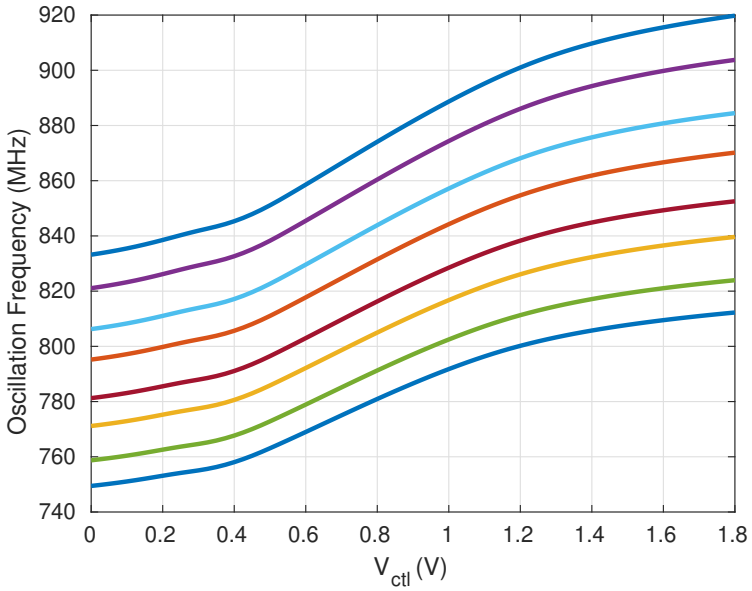


Fig. 2.16: Frequency characteristics in FF corner at 0^oC

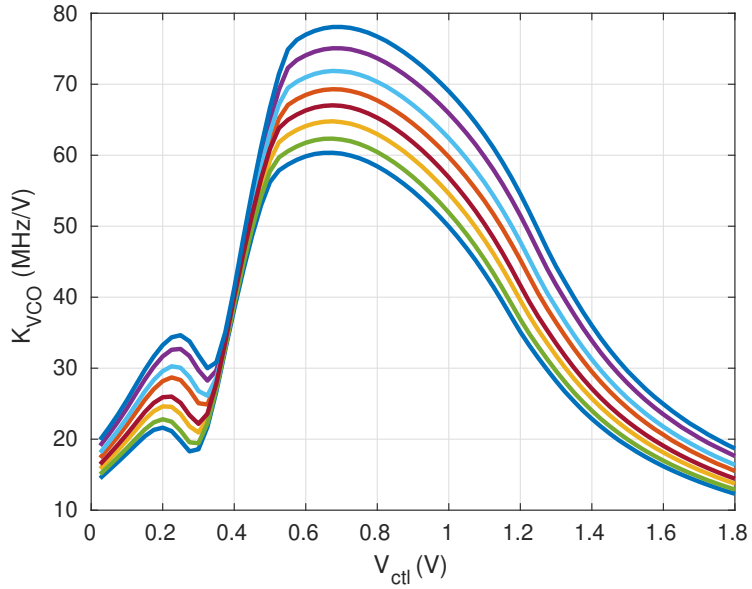


Fig. 2.17: K_{VCO} characteristics in FF corner at 0^oC

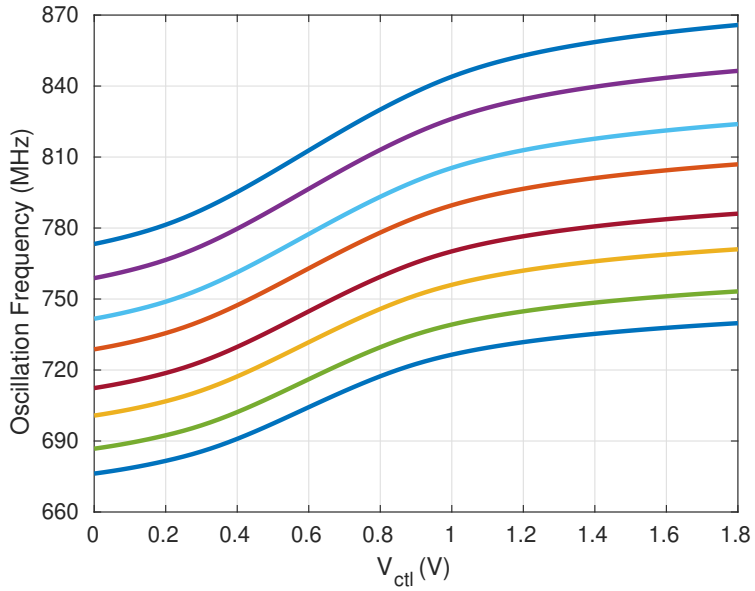


Fig. 2.18: Frequency characteristics in SS corner at 100^oC

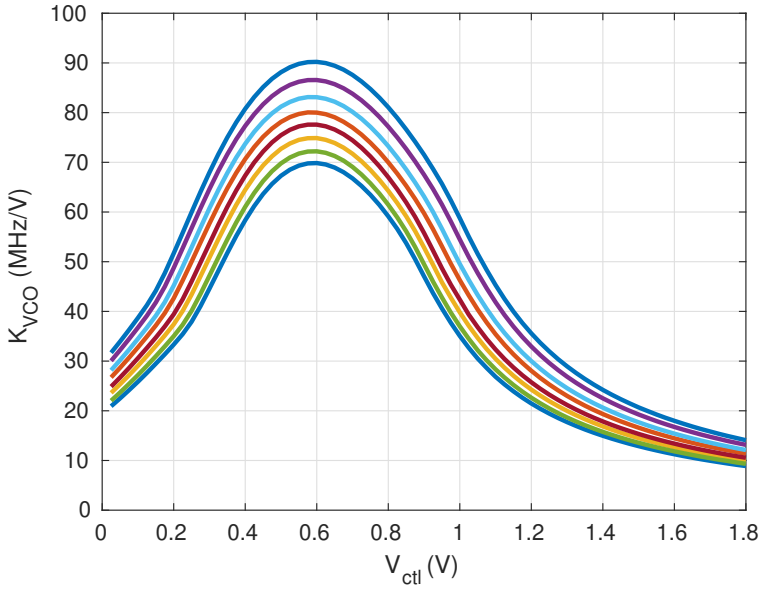


Fig. 2.19: K_{VCO} characteristics in SS corner at 100^oC

2.5 VCO Noise

Figure 2.20 shows the different noise contributions for different operating point.

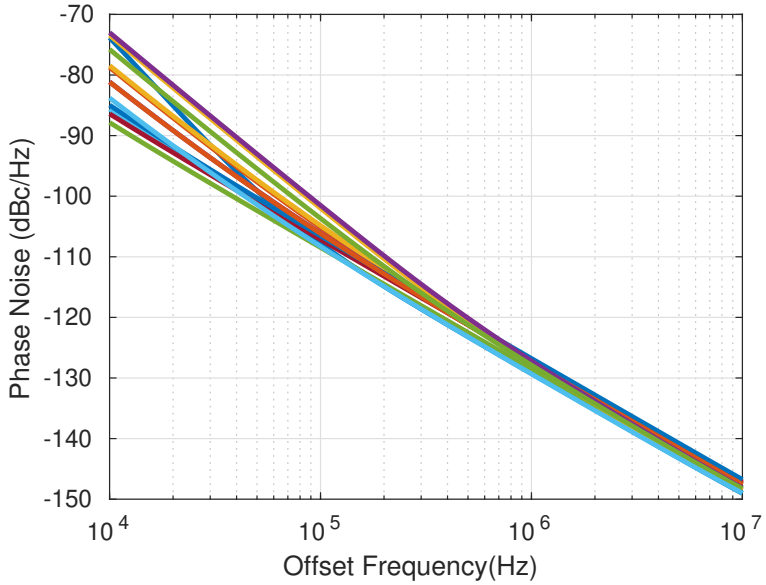


Fig. 2.20: Phase Noise of VCO

This noise profile is multiplied by the magnitude square of eq. 1.5 to get the noise at the output of the PLL.

CHAPTER 3

Divider circuit

The frequency of oscillations from the VCO is stepped down to 5MHz by using the divider of ratio 160. For this purpose, 7 MOD-2/3 dividers are cascaded. Since the input frequency of dividers near to the VCO are high (till 400MHz), Mod 2/3 divider are made using TSPC logic. As the divider moves closer to the reference frequency, the TSPC will not be able to contain the voltage level, so the dividers close to the reference frequency are made by CMOS logic.

3.1 Mod 2or3 dividers

Figure 3.1 [1] shows the logic of the operation of Mod 2 or 3 dividers. If T=0, then $\overline{Q}$ will be feed into the D terminal of the second FlipFlop making it operate in the divide by two mode. Suppose we can make the T=1, then the D input will not depend on the $\overline{Q}$ making the output constant. To make T=1, D input of first flop should be 1, therefore Trig and $\overline{Q}$ should be 1. Since there is a delay of one clock cycle from first flip flop, when OUT=1, T=1 therefore in the next clock cycle, OUT will be remained at 1; this gives an extra cycle for frequency division.

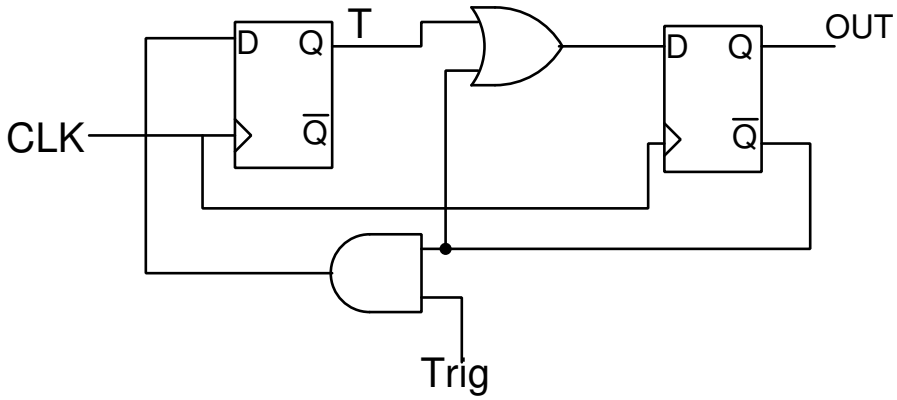


Fig. 3.1: Mod 2or3 divider logic

The mod2or3 dividers can be cascaded and if the Trig signal is adjusted, then a continuous division ratio can be obtained. An example is depicted in figure 3.2 [1]. Frequency division range is obtained as $8 + P0 * 2^0 + P1 * 2^1 + P2 * 2^2$. The mod_{out} signal is the and value of mod_{in} and $\overline{Q}$ of the current stage.

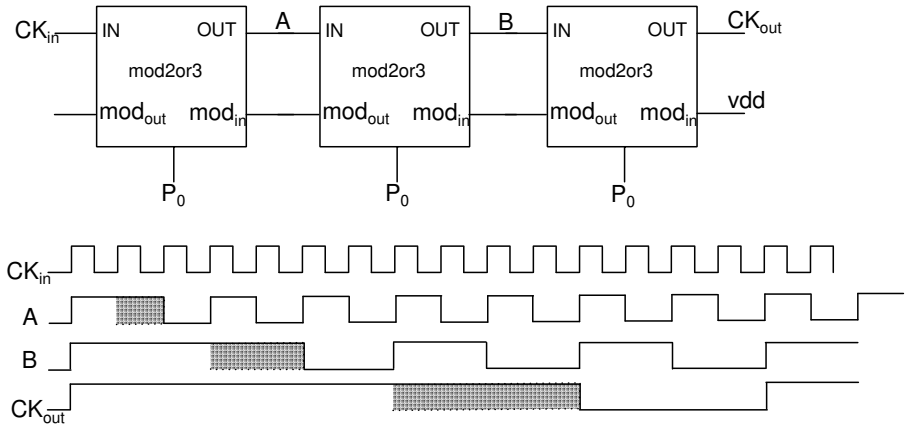


Fig. 3.2: cascaded operation for suitable ratio

The above mod 2or3 dividers can be cascaded and the required frequency division can be obtained. In our case, the division ratio is 160. So we need to cascade seven mod 2or3 dividers.

3.2 High-speed divider

From figure 3.1, it is clear that to obtain a division ratio of 3, two DFFs must be cascaded with some combinational logic. For high-frequency operations, the TSPC DFFs can be used. However, the introduction of logic could slow down the operation. Figure 3.3 shows an improved design for the implementation of TSPC divider[3].

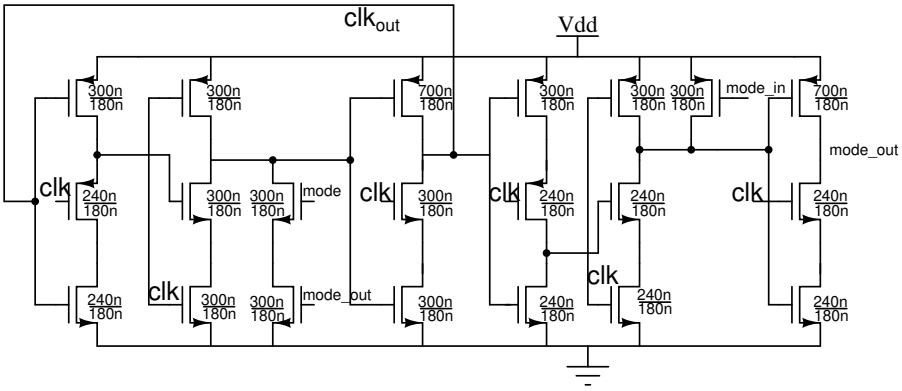


Fig. 3.3: TSPC 2or3 Divider

In divide by 2 operation (mode = 0, assuming node C at Q initially) after the negative triggering of the clock node A will contain $\overline{Q}$, when the clock becomes high, node B contains Q and the node C will move to $\overline{Q}$. Thus in a cycle the Q value changes its value. In divide by 3 mod (mode = 1) the node B settles at zero for an extra cycle, as the DFF2 skips one cycle of value.

3.3 Low-speed dividers

The TSPC latch operation fails for the lower frequencies as the node will not be able to hold charges due to leakages. So for low frequency of operation DFFs used will be using CMOS logic. Figure 3.4 shows the circuit implementation of the DFF.

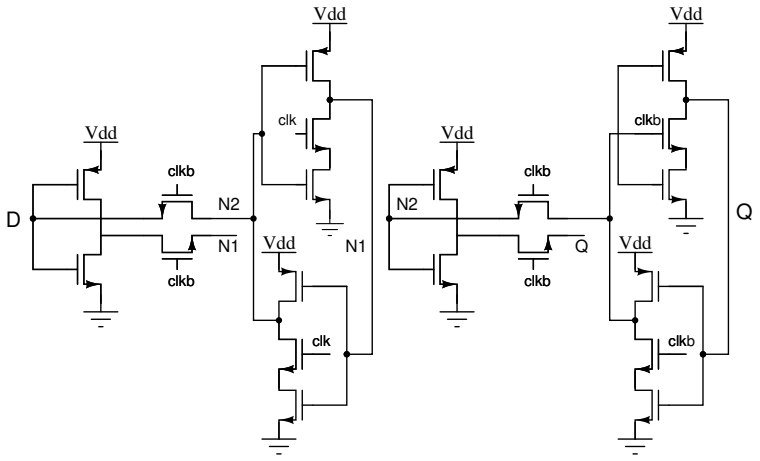


Fig. 3.4: CMOS DFF

3.4 Noise simulations

Since the division ratio is high(here N=160), the HB simulations will not converge with a lower number of harmonics. So the following method is used to obtain the noise contribution from the divider. Two consecutive dividers are taken at a time and are cascaded. The dividers are given the corresponding mode values as in PLL. The output from the VCO should be given to the input clk of the first divider. The HB and HBnoise simulations are run for this combination. The phase noise is obtained after the first stage. This phase noise is being propagated to the divider output after passing through the other stages(as the phase noise pass through the dividers, it repeats at fin/N frequencies and magnitude gets divided by N_2). The rise time and fall time after the first stage are also noted and used as the next stage input. The process is continued until the last stage. Figure 3.5 shows the process for a division ratio of 2, i.e., $f_2 = 2\, f_1$(Here it is shown with jitter spectral density).

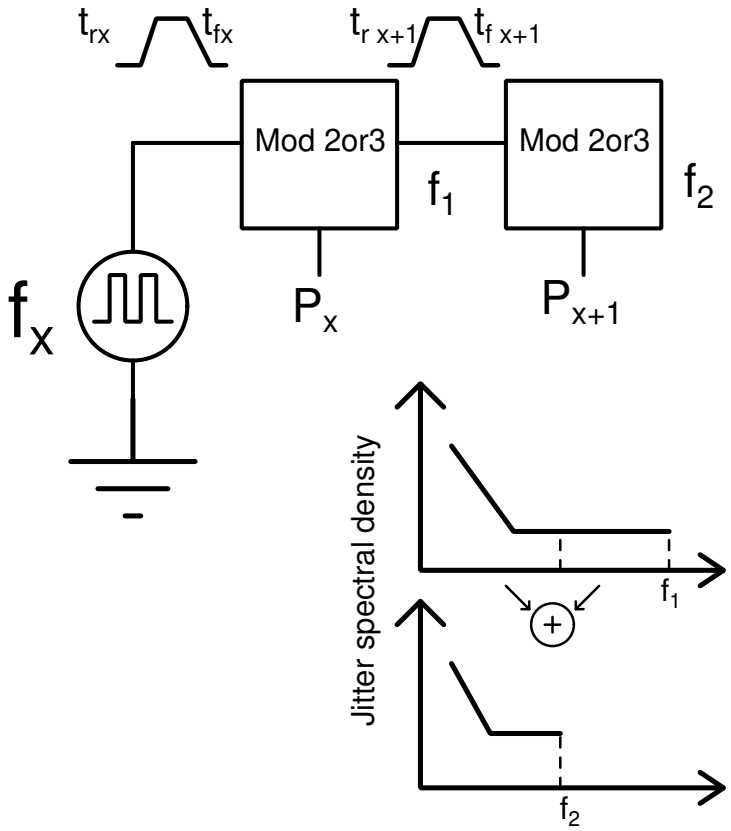


Fig. 3.5: Divider noise analysis configuration [4]

CHAPTER 4

Other components in the PLL

4.1 Phase detector

As shown in Figure 4.1 the 3 state PFD takes two periodic signals and converts the difference in the phases of the two signals to the average value of the difference in UP and DN signals. The signals UP and DN are then passed into the charge pump for obtaining a proportional current.

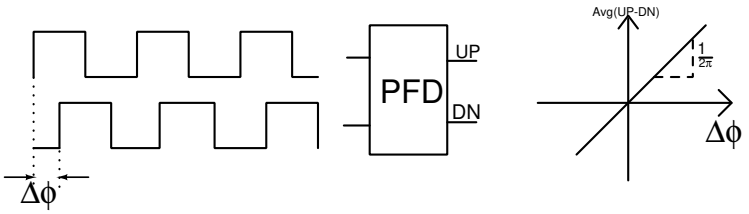


Fig. 4.1: PFD characteristics

The circuit for the same is implemented as in Figure.4.2. The inputs to the phase detector are the reference clock pulse and the oscillator output after passing through the divider of ratio 160. With CP_{En} as 'high', if reference is having an earlier positive edge triggering compared to feedback, then the UP signal becomes 'High' and when the feedback becomes high the RST signal to flipflops becomes high. The delay of the AND gate was adjusted to be 400ns. The slope is of value $\frac{1}{2\pi}$. The sizes of the buffers were adjusted to have equal delay time between the UP and Down pulses.

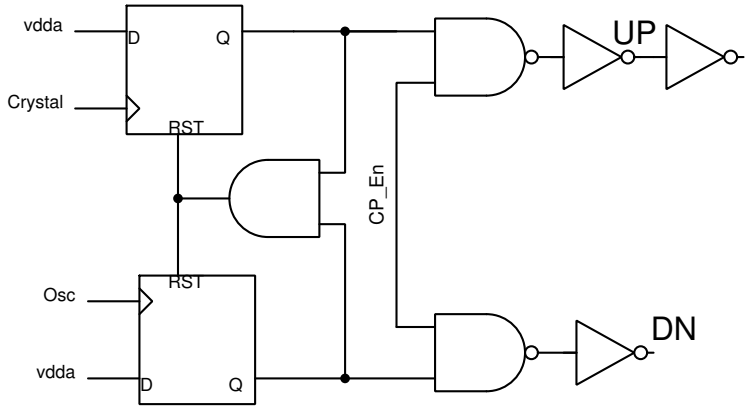


Fig. 4.2: 3 state PFD

4.2 Charge pump

Figure 4.3 shows the implementation of the charge pump. The UP and DN signals are obtained from the 3 state PFD. A current of 2μA was mirrored from the current source into the circuit. This current is amplified by ten times and the driven in(out) with respect to the control UP=0 (DN=1). The CMFB circuit was inserted to make the voltages the same at both the ends of opamp so that UP and DN currents are equal at any voltage Vo. This will reduce the amplitude of the Vctl, thus decreasing the spur level.

The opamp is a folded cascoded structure, as shown in Figure. 4.4 with DC gain of atleast 400 for V_{cm} varying between 300mV to 1.5V(operating voltage range) and Vo kept at 1V to 1.3V(Possible values to gate of pMOS).

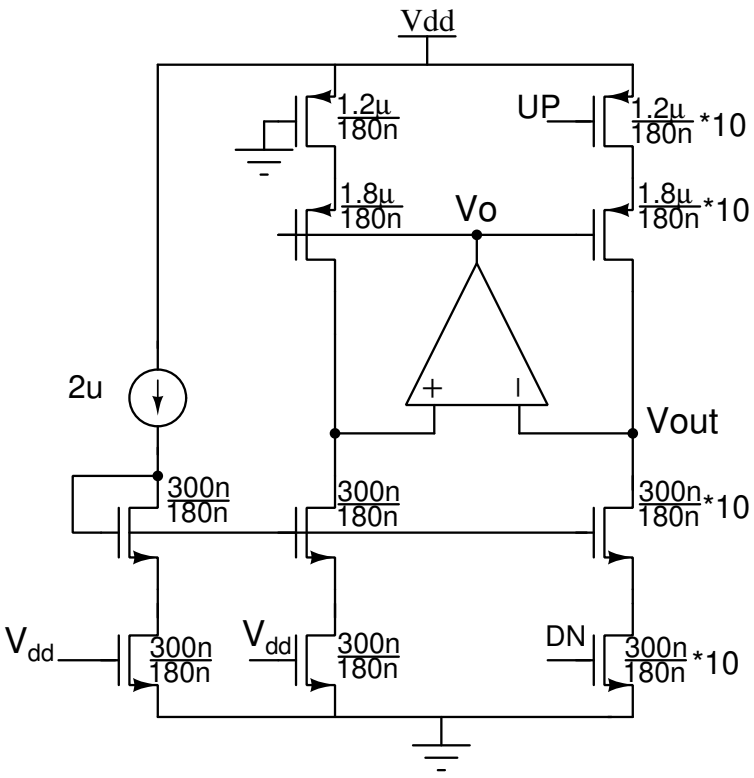
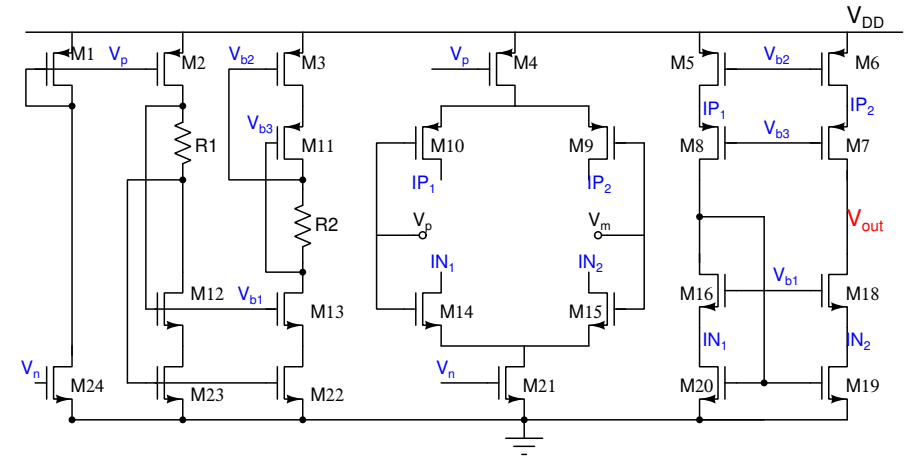


Fig. 4.3: Charge pump



M24= .5µ/400n
M1 = 1.6µ/400n*2
R1= 5KΩ
R2= 5KΩ

M12 = M23 = .5µ/300n * 10
M22 = M13 = .5µ/300n * 8
M3 = M11 = 1.8µ/300n * 2
M3= 1.8µ/300n * 2

M4= 1.6µ/400n
M9 = M10 = .8µ/400n * 2
M14 = M15 = .8µ/400n
M21= .5µ/400n

M5 = M6 = 1.8µ/300n * 2
M7 = M8 = 1.8µ/300n * 3
M16 = M17 =.5µ/300n * 3
M19 = M20 =.5µ/300n * 2

Fig. 4.4: Folded cascode opamp structure

4.3 Loop filter

The loop filter is made as shown in Figure.4.5. The values are obtained to get a loop bandwidth of 100KHz. A lower value of bandwidth reduces the spur level (Which is produced by the periodic addition of UP and DN currents in the Loop Filter.

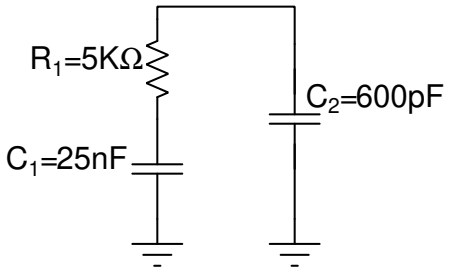


Fig. 4.5: Loop Filter

The impedance provided by the arrangement will be

$$Z(s) = \frac{R_1 C_1 s + 1}{s(C_1 + C_2) + R_1 C_1 C_2 s} \tag{4.1}$$

The peaking of the transfer function from input to output (eq.1.1) should be kept low. The loop gain for the PLL is evaluated for different possible combinations of K_{VCO} and I_{cp}. From simulations the for 800 MHz the K_{VCO} varies from 90 MHz /Vto 20 MHz /V. And I_{cp} is assumed to be varied from 25μ A to 20μ A . For a good phase margin, the zero of the TF should be atleast 5 times below the W_{UGF} and pole greater W_{UGF}. So minimum W_{UGF} will calculated for the 20 MHz /Vand 20μ A will yield to be 67.8 kHz, so the zero should be placed below 5kHz and Maximum W_{UGF} be so the second pole should be placed at 300kHz. The zero provided by the impedance will be at $\frac{1}{R1C1}$ and the pole will be at $\frac{1}{R1C2}$.

The phase transfer function is also evaluated with the the obtained values of R1 C1 C2 and fine adjustments are made to reduce the peaking. Finally the obtained values are as: R_1 = 15 kΩ; C_1 =26nF ; C_1 =600pF ;

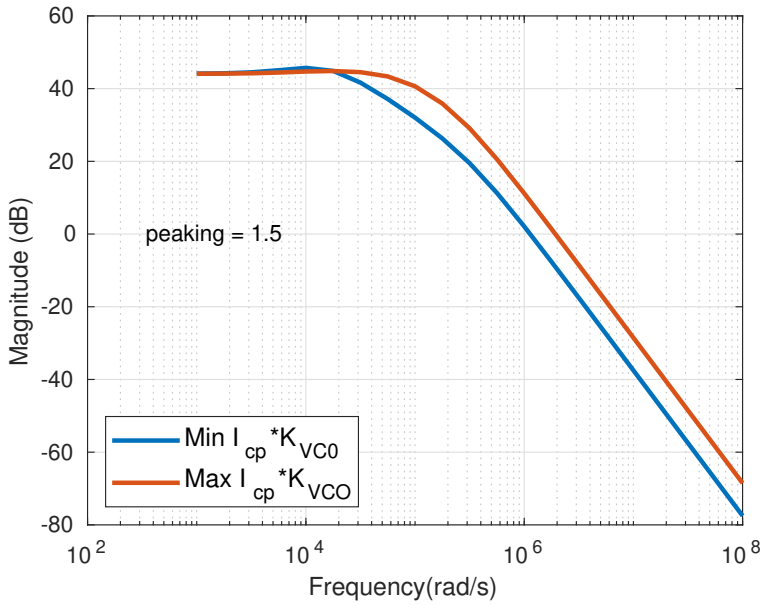


Fig. 4.6: PLL Input Jitter TF

Also, the charging and discharging time of loop filter due to rectangular pulse of current from charge pump will depend on the time constant of loop filter(time constant should be less compared to the reference clock period).

4.4 Noise simulation of PFD and Charge Pump

The noise contribution of PFD and charge pump is found as follows: The PFD and charge pump are taken separately and the charge pump is terminated by a voltage source (Vctl for which the PLL locks) as shown in Fig. 4.7. The inputs to the PFD are two square waves with a phase difference of $\delta\phi$. This phase difference should be the one that gives a total of zero charge injection to the output voltage source. Then PSS and PNOISE analysis are carried out and i_{out} is determined.

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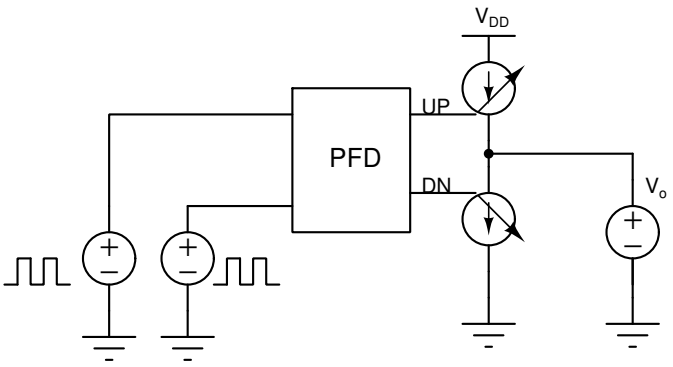

Fig. 4.7: Setup for PFD CP noise simulation

The PSD of the current noise is multiplied by the magnitude square of the transfer function to output (1.3).

CHAPTER 5

PLL Simulation Results

5.1 Layout

The total size of the layout accounts, excluding the inductor, is 225μm * 512μm. The inductor area accounts to 450μm * 420μm.

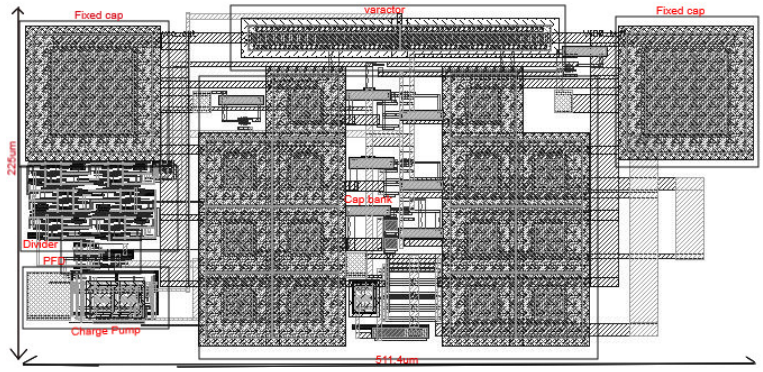

Fig. 5.1: PLL Layout

5.2 Spur

The transient simulations of the PLL circuit was run for 200 μs and the last 40 μs were used to obtain the spectrum of the clock signal.

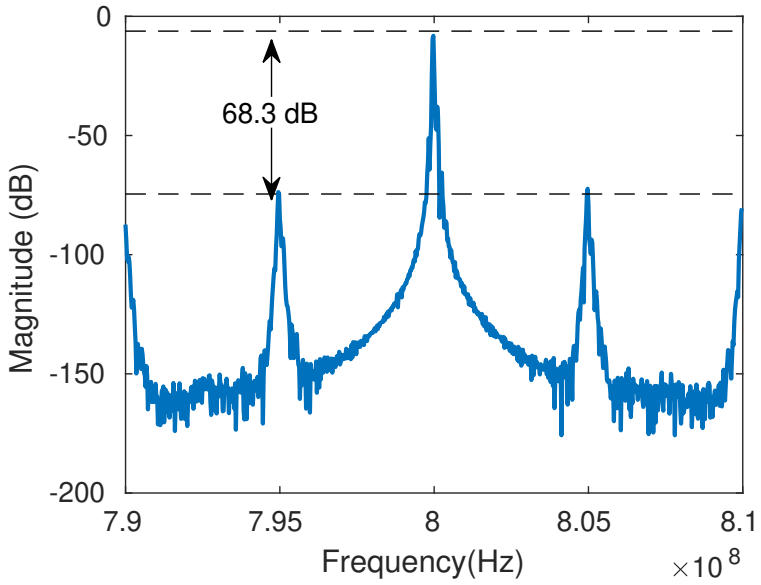

Fig. 5.2: VCO Spur in FF corner

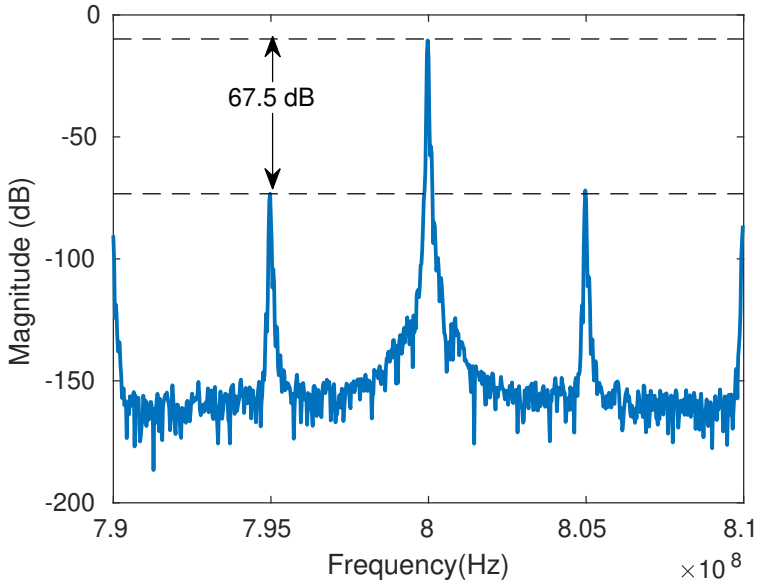

Fig. 5.3: VCO Spur in SS corner

5.3 Noise contributions

As discussed in section 1.3.1, the noise PSD from different sources was obtained and multiplied by magnitude square of the transfer functions to obtain the noise at the output of VCO. The obtained results are as shown.

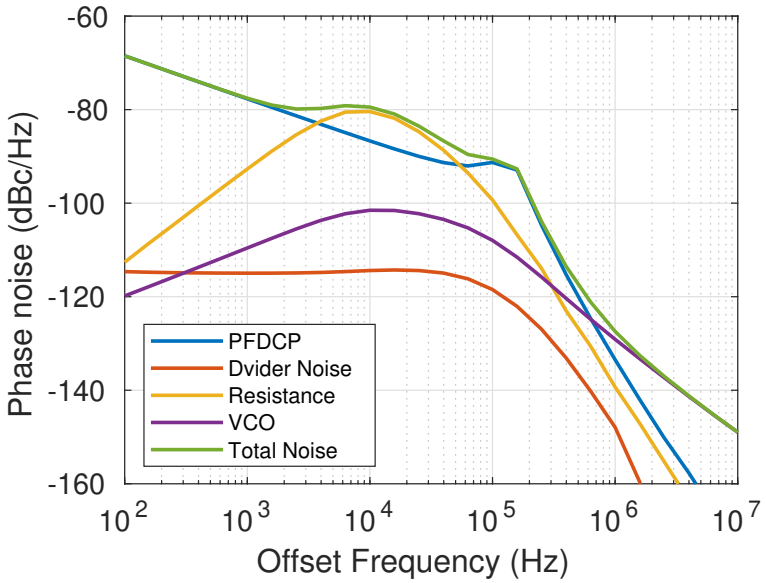

Fig. 5.4: VCO phase noise

The jitter at the output is obtained by as follow :

$$T_{jitter} = \sqrt{Area\ under\ PSD}/(2\pi f_0)$$
$$= 4.2\,ps$$

5.4 ADC simulation

The clock obtained from the circuit is passed through a divider of ratio 4 and then used to drive a $\Delta\Sigma$ ADC. The characteristics of the ADC using an ideal clock and the real clock were noted.

For the ADC simulation with a real clock, a cycle of PLL control voltage was extracted after settling. This voltage was given to the VCO and the output of the VCO was used to drive the divider. However while driving the ADC the clock frequency and the strobe period's precision is the main concern. If the strobe period differs from the clock period then there is a chance for the loss of samples. As shown in figure 5.5 after a long time, the sampling will lose one cycle and degrade the SNR. This issue is solved by excess sampling a cycle of ADC output (this is not the same as OSR) and then comparing a sample with its previous and successive values, if the values are same then the sample is taken and then advanced by the excess sampling ratio. If they are not the same then

it implies that we are missing a sample in this cycle, so if the sample is not same as its previous value then the samples are advanced by the excessive sampling ratio/2 times. If the successive value is not same then the samples are delayed excessive sampling ratio/2 times. The obtained samples are multiplied by Blackmann Harris window (this is due to the precision of sampling and input sinusoidal frequency) and SNR is calculated.

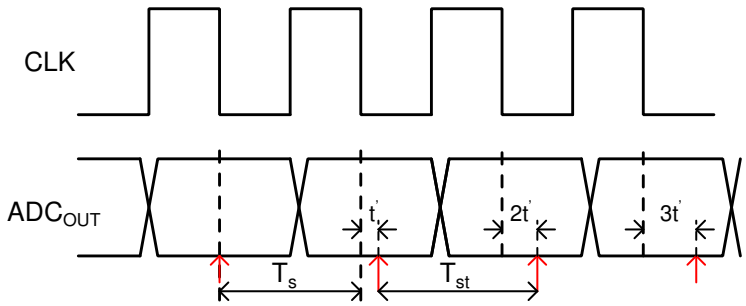

Fig. 5.5: Strobing issue in ADC simulation

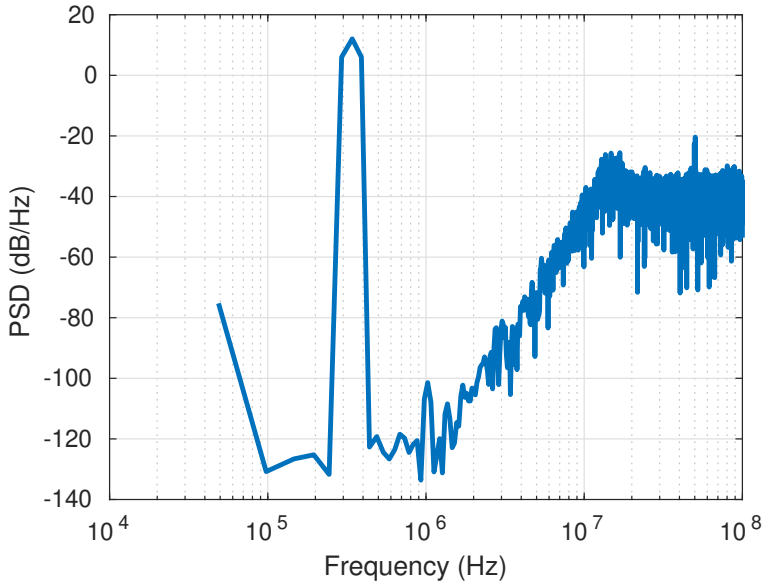

Fig. 5.6: PSD for ideal clock

With ideal Clock :

$$SNR = 118\,dB$$

$$SNDR = 112\,dB$$

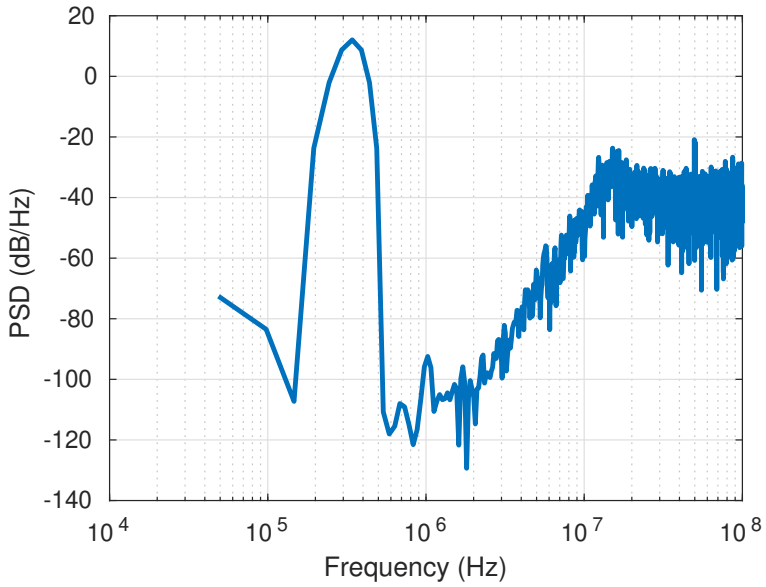

Fig. 5.7: PSD for designed PLL

With designed Clock :

$$SNR = 110.32\,dB$$

$$SNDR = 103.6\,dB$$

REFERENCES

[1] M.H Perroltt, *"Advanced Analog Frequency Synthesizers, Clock and Data Recovery"*. Available: https://www.cppsim.com/PLL_Lectures/day1_pm.pdf

[2] S Aniruddhan, *"RF Integrated Circuits"*. Available: http://www.ee.iitm.ac.in/vlsi/courses/ee6320_2020/start

[3] DIPTI RANJAN TRIPATHY, *"Design of Low power Dividers for Bluetooth Frequency Synthesizer"*

[4] Aditya Narayanan, *"Private Communication"*