Charge based Receiver Front-end for 28Gb/s SERDES

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Charge based receiver front-end for 28Gbp/s SERDES**, submitted by **VIVEK PALA**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

In the current world, there is a demand for a large amount of data to be communicated between the transmitter and receiver. It requires the data to be processed at a very high speed and with low power consumption. Following Moore's law, the circuits are scaled-down, thereby reducing the supply voltages. It helps for faster data processing with reduced power consumption. But the technology scaling benefits are limited with little scaling in supply voltages for technology nodes lower than 90 nm CMOS technology. Parallelism in storage and processing is exploited to overcome the challenges of processing, storing and transferring data at a single peak data rate. It is preferred to have the data transfer between two nodes at the maximum data rate to reduce the number of pins. The bits have to be serialized and deserialized to meet the lower data rate demand for processing and storing the information.

This thesis work concentrates on the front-end part for the receiver of the SERDES, which is having a data rate of 28 Gb/s. Here Charge Steering Logic (CSL) is used instead of Current Mode Logic (CML) or CMOS Logic. The receiver front-end employs a track and hold circuit followed by the 14 GS/s 4-bit charge based Flash ADC with integrated 1:2 demultiplexer (DeMux). The deserializer of the receiver will follow the DeMux. Designed in 28-nm CMOS, the charge-based Flash ADC achieves 23-25 dB SNDR with sinusoidal inputs over a 0.1-7GHz frequency range. The ADC consumes 13.5 mW at 0.9 V supply voltage. The charge-based 1:2 demultiplexers deserialize ADC's outputs.