IIT Madras 5G TestBed

IMPLEMENTATION OF PRACH RECEIVER CHANNEL DESIGN ON HARDWARE

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Abstract

In this project report, The design for PRACH Receiver in the Uplink chain is discussed. The main objective of the design is to estimate a parameter called Timing Advance to achieve Uplink synchronization. This is achieved by correlating the local preamble root sequence with the received RACH sequence. Two algorithms are devised to do this correlation process . One method is to do the frequency shift and downsampling in time domain and the other one is to do RACH sequence extraction after taking FFT. The report presents the hardware designs for both the algorithms and both the designs are optimized for minimal hardware and timing as well. It also talks about certain design choices being made based on the analysis. The designs are implemented and tested on Xilinx Ultrascale (ZCU28) FPGA Board. Based on their hardware implementation results, the two designs are compared to choose the better design option between them for further integration and testing with L1 controller and ORAN (RRH chain and BBU chain).

Note : The contents of the project cannot be described here as this project report is a Confidential property of 5G Testbed lab, IIT Madras.