STUDY AND DEVELOPMENT OF COMPACT HIGH POWER DENSITY CONVERTER FOR AUTOMOTIVE APPLICATION

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **STUDY AND DEVELOPMENT OF COMPACT HIGH POWER DENSITY CONVERTER FOR AUTOMOTIVE APPLICATION**, submitted by **MRINMOY SAHA**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I've been truly blessed to have known all these people and I hope I can make it worthwhile for them as well through my work.

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ABBREVIATIONS

SiC	Silicon Carbide
GaN	Gallium Nitride
AlGaN	Aluminium Gallium Nitride
SRC	Series Resonant Converter
DAB	Dual Active Bridge
1ϕ	Single Phase
3ϕ	Three Phase
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
Q	Quality Factor
$\mathbf{L_r}$	Resonant Inductor
$\mathbf{L_{lk}}$	Leakage Inductance of Transformer
$\mathbf{C_r}$	Resonant Capacitor
$\mathbf{C_o}$	Output Capacitor
L	Inductor
C	Capacitor
R	Resistor
$\mathbf{R_c}$	Core loss Resistance
$\mathbf{R_w}$	Winding loss of Transformer
$\mathbf{R_{DS_{ON}}}$	On-Resistance of FET
$\mathbf{f_s}$	Switching Frequency
$\mathbf{f_r}$	Resonant Frequency
$\mathbf{V_{AN,BN,CN}}$	Primary phase A,B,C to primary Neutral Voltage
$\mathbf{V_{an,bn,cn}}$	Secondary phase a,b,c to secondary Neutral Voltage
DUT	Device Under Test

Chapter 1

Introduction

A large number of automobiles in use around the world has caused and continues to cause serious problems on the environment and human life. Air pollution, global warming, and the rapid depletion of the earth's petroleum resources are now serious problems. Electric Vehicles (EVs), Hybrid Electric Vehicles (HEVs) and Fuel Cell Electric Vehicles (FCEVs) have been typically proposed to replace conventional vehicles in the near future Electric vehicles (EV) have developed rapidly because of its high efficiency and pollution-free advantages. DC-DC converters can be used to interface the elements in the electric power train by boosting or chopping the voltage levels. Due to the automotive constraints, the power converter structure has to be reliable, lightweight, small volume, with high efficiency, low electromagnetic interference, and low current/voltage ripple.

1.1 Background

Presently, the DC-DC converters utilized in BEV and PHEV powertrains primarily use Si-based [1] semiconductors which limits their efficiency to 92–93%, allows a maximum switching frequency up to 30 kHz and attains only 3–12 W/in^3 power density. However, the performance of Si-based semiconductors is limited due to their physical properties and characteristics and further development of Si-based semiconductors is not thought of also various innovative technical improvements have been introduced through Si-based power transistor technology but nowadays their progress has slowed down as it becomes a matured technology. In the last few years, a great deal of attention has been given to new power transistor technologies based on new material systems. Gallium Nitride (GaN) power transistors have emerged as a disruptive technology with great potential that arises from the outstanding material properties of GaN [2],[3] that is use of Wide Band Gap elements have brought about drastic improvements in the power density (50 W/in^3) as well as efficiency while ensuring better manufacturability at minimal cost. Contemporary research into WBGSs have found that silicon carbide (SiC) semiconductors are highly suitable for designing high powered DC-DC converters

due to its capability for handling vast power ranges up to 100 kW, lower cost, better packaging, high thermal conductivity, and availability on the market. On the other hand, GaN semiconductors are at a mature level for commercial use with breakdown voltages of less than 600 V and power ratings of less than of 5 kW . However, more research needs to be conducted on GaN-based semiconductors to advance adaptation in the converters.

1.2 Goals of the project

The report mainly discusses the use of GaN semiconductor that will mostly replace SiC soon for high frequency DC-DC converters. Implementation of a high power DC-DC converter has been shown , the used topology has been extended towards Dual Active Bridge(DAB) since a bi-directional converter can move power in either direction, which is useful in applications requiring regenerative braking. Before moving on to the Three phase Topology study of Single phase SRC based DAB shall be studied.

Development of a single phase PCB of AC-DC module using GaN switches will be done with board layout inductance keeping to as little as possible. The developed module will be run as an Inverter at frequencies upto 1MHz. To characterize dynamics of the switches used DP Test will be conducted. A detailed analysis of a single phase DAB will be done and similarly a comparative analysis shall be studied among an SRC and DAB for high switching frequencies. The comparative analysis shall be validated with experimental results and also mathematical expressions.

1.3 Outline Of the Thesis

In **Chapter 2** a very basic description of the superiority of GaN over Si based switches will be discussed, various types of GaNFETs available in today's market and their manufacturers, the use of GaN will be discussed as well.

Chapter 3 start off with the evolution of the three phase topology, vivid description of a resonant converter will be presented also the importance of various components in the topology will be thoroughly explained.

The simulation of the above derived converter will be done in **Chapter 4** operated as both in ideal as well as non-ideal conditions.

Before moving onto building the 3ϕ topology **Chapter 5** would deal with the operation 1ϕ SRC operated in Buck and Boost Mode. Various Conditions will be derived that will ensure minimum switching losses in the converter by letting ZVS in both the input and the output bridge.

Chapter 6 will explain vividly the operation of 1ϕ DAB, harmonic analysis in a DAB will be done and hence various essential parameters of the converter will be derived. Similar to SRC here too conditions would be derived that will ensure ZVS in the input and output bridges ensuring least switching losses.

After discussion of the DAB, in **Chapter 7** an AC-DC module will be developed using GaNFETs. The dynamic properties of the used FET shall be checked in LT-SPICE. The used Gate driver shall also be shown and the various key factors kept in mind while designing the PCB layout will be clearly explained such that a PCB with least layout inductance can be made.

Chapter 8 deals with the hardware results of the above designed PCB working as an inverter with an inductive load at frequencies up to 1MHz. Later the switching dynamics of the GaNFETs used shall be tested by performing Double Pulse Test on a device and hence proper conclusions shall be drawn that would let us decide upon the selection of proper R_g to ensure least overshoot across the Gate-Source of a device.

Finally **Chapter 9** presents a summary of the most important results and conclusions of the thesis. Suggestions for possible future work in the area of the dc-dc converters for high power and compact converter applications are also given that can be used for Electric Vehicles in the near future.

Chapter 2

Gallium Nitride (GaN)

2.1 About GaN

"Moore's Law or Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved." In simple words, as time passes on electronic circuitry shall be smaller and smaller and hence making the devices more compact. In this never-ending race for space, compactness and high power density have become the major challenges for modern power electronic converters.

Since we want more and more compact converters with higher power density, gradually **GaN** is emerging as the probable substitute. Now the question comes "What are the factors that make GaN a better alternative?"[11] GaN is a Wide Bandgap Element Semiconductor. GaN has a band-gap of 3.3 MV/cm, which results in high breakdown field around 10 times greater than Si[4]-[6], which results in bringing the pads of the device too close to each other resulting in a more compact device for a converter with high power density. GaN has high Electron Mobility μ, GaN has a μ of 2000 cm^2/Vs. Higher the μ , as we know more will be the electron mobility more is the drift velocity, resulting in lower $R_{DS_{ON}}$.[7]-[11]. As GaNFET has lower $R_{DS_{ON}}$ e.g. the device used has $7m\Omega$ resistance for ratings of 100V and 36A. Therefore, lower the On resistance, lesser the conduction loss resulting in better-operating conditions and better efficiency of the converter. Another advantage of GaN devices is that GaNFETs have lower device capacitances, i.e. C_{ISS},C_{OSS},C_{RSS} i.e. the Input, Output and Reverse transfer capacitances are in the order of few pF's so smaller charge is required to charge the device capacitances to turn ON the device resulting in Turn On time of a few ns, resulting in higher f_s. GaN can be switched at a higher switching frequency. Due to this small turn On/Off time of the device we can switch the devices at a very high switching frequency at a few MHz, higher switching frequencies result in the reduction of the size of the magnetics used in the converter. The size of a converter is quite majorly decided by the size of the inductor and the capacitor used in it. Higher f_s results in decreased size of both capacitors and inductors hence making the

converter more compact. GaNFET converters have Lesser FOM (Fifure of Merit) that is the product of $R_{DS_{On}}$ and Q_{On} is less[11], hence losses are less, as a result air cooling is sufficient for such converters. For high power converters new cooling methods can be implemented to make the converter more efficient.

2.2 Working of GaN

GaN is inherently piezoelectric that is if we apply pressure on a layer of GaN, it produces voltage or electrons. Now if we apply a layer of AlGaN on it, more electrons are produced off the same strain, this produces a 2D-electron gas[12] resulting in higher current through it.

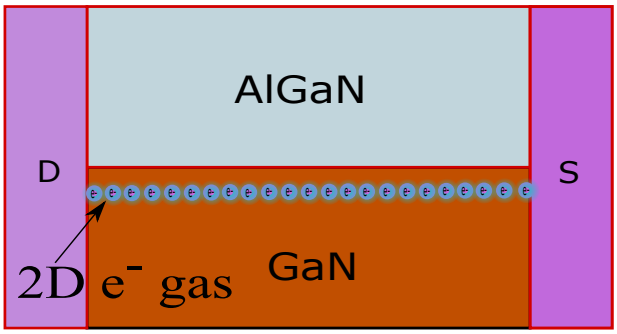


Figure 2.1: Production of 2D e⁻ gas

2.3 Type of GaN

1. **Depletion mode type:** A Depletion Mode type GaNFET is a naturally ON type device but when a negative gate-source voltage is applied it is turned OFF. Depletion mode transistors are inconvenient because, at start-up of a power converter, a negative bias must first be applied to the power devices or a short circuit will result.

2. **Enhancement mode type:** In recent times a new technology of GaNET has been developed namely the Enhancement mode type or eGANFETs, in such technology when a zero voltage is applied on the gate, the electrons are wiped off and the device turns off and when a positive voltage is applied to the gate it pulls the electrons to the surface completing the circuit hence turning ON the device.

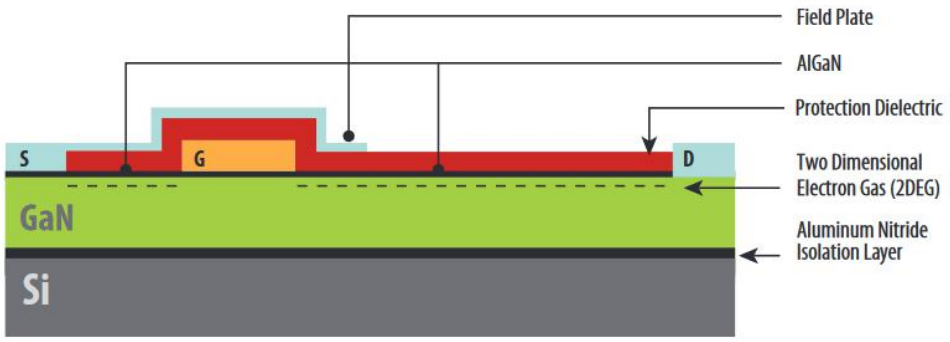


Figure 2.2: Enhancement mode GaN[11]

2.4 Manufacturers of GaN

Few manufacturers of GaN devices in today's market are[11]:
Exagan, EPC, Transphorm, Infineon, Cree, e-Front Runners, Global Power Technologies, Panasonic, Fairchild Semiconductors, Rohm, GaN Systems, ON Semiconductor, Avago Technologies.
Among the above stated manufacturers the leading vendors[11], Infineon uses CoolGaN Technology, EPC uses eGaN Technology and Transphorm uses Cascode Technology.

2.5 Usage of GaN

Due to their capability of handling very high frequencies, GaNs can potentially be used in Microcontrollers, SSDs, antennas, RF MOSFETs, RF Amplifiers, RF Switch ICs, Power MOSFETs, High Power LEDs and Batteries.

2.6 Conclusion

In summary, a discussion has been done on GaN in today's market. We also see the amny reasons making GaN as the probable substitute to Si based devices in the near future. Out of the many mentioned uses of GaN in Power Electronics Field GaNFET's are gaining more popularity due to there ability to switch at such high frequencies hence developing a compact and efficient converter for high power ratings shall remain no longer a challenge.

Chapter 3

Three Phase Multilevel Series Resonant Converter

3.1 Resonant Converter

One of the major losses in a converter is its switching loss, by using a resonant converter we can eliminate these switching losses to a great extent by making a ZVS turn ON for both the bridges for a given amount of phase shift that shall be discussed later.

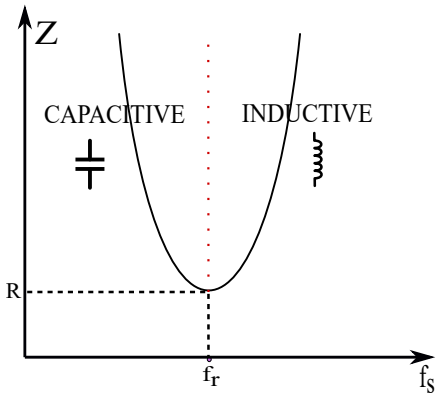


Figure 3.1: Impedance Curve for series Resonance

Presented above is the impedance curve of a series RLC network versus f_s. Series Resonance simply means that when $f_s = \frac{1}{2\pi\sqrt{LC}}$ then $X_L = X_C$ then the net impedance offered by the RLC network is simply R. So the current will be in phase with the voltage waveform hence making soft switching of the MOSFETs, reducing switching losses and also reducing the voltage overshoots during switching too.

As we can see in Figure 3.1, when $f_s = f_r$ then its resonance, $f_s > f_r$ then its an inductive circuit and when $f_s < f_r$ then it behaves as a capacitive circuit. In case we need a net power transfer then always run the converter at $f_s > f_r$ so that the RLC network behaves as an inductive circuit.[27],[29] The impedance curves for varying Quality factor has been displayed on the next page.

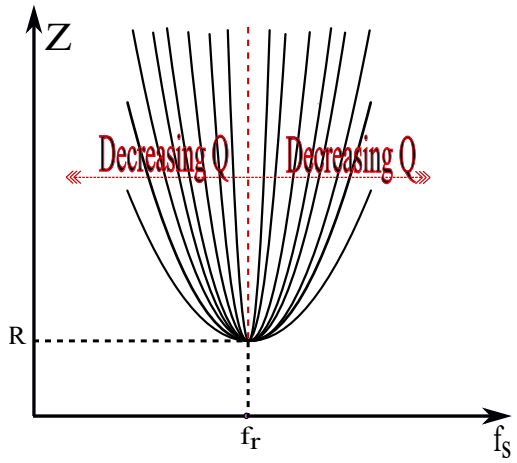


Figure 3.2: Impedance Curve for series Resonance with varying Q

A resonant circuit simply behaves as a notch filter which should ideally allow only a single frequency to pass through it if the Quality factor is very high. As we can see from Fig 3.2, for lower quality factors near f_r very few frequencies get filtered out making the current less of a sinusoid and creeping more harmonics into the system which means the efficiency of the converter reduces. So it is recommended to operate SRC at higher Qs of around 25-30. [30]

3.2 Evolution of the Topology

As discussed earlier the advantages of GaNFETs, making this a very suitable candidate for DC-DC converters for automotive applications. A DC battery serves as the source for the converter, and the output DC can be used for multiple purposes like for the headlights, automated windows also for the gear train as well as the source for the BLDC motor or PMSM's inverter.

A conventional full bridge SRC looks like :-

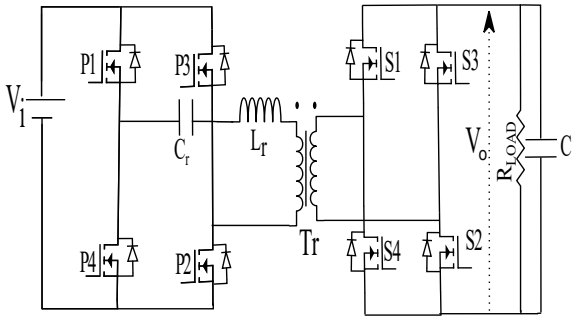


Figure 3.3: Conventional Full Bridge SRC

Since we go for higher power rating, if we use such topology it would lead us to choose devices with higher current ratings which increase the device cost. Since GaN is a completely new technology the paralleling of GaN without any prior tests might result in uneven current sharing resulting in unexpected device failure. Also in such a topology the output current ripple will be $2f_s$ so we would require a larger filter capacitor to filter the ripple currents. For the stated reasons we use a three phase topology resulting in reduced current stresses through the device and also the output current will have a ripple of $6f_s$ so smaller capacitors would be required [13]-[14].

Among numerous resonant circuits like LC series, LC parallel, LLC and LCC, half-bridge, full-bridge, and three phase converter [20]-[26]. Series LC resonant type DC-DC converter is chosen [20].

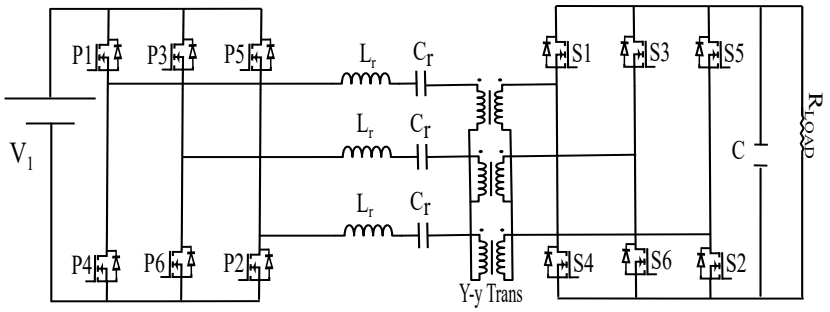


Figure 3.4: Conventional 3ϕ Full Bridge SRC

For higher power as well as high voltage applications we need to put two MOSFETs so we put two switches in series to block the input voltage V1, therefore the topology gets modified to

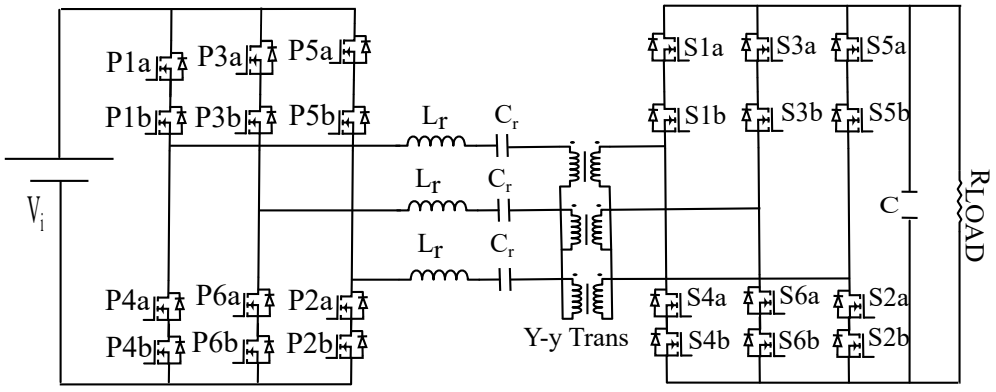


Figure 3.5: Conventional 3ϕ Full Bridge with Series Switches

In the above topology, the problem persists that when we are using 2 switches, there combined $R_{DS_{ON}}$ becomes more, resulting in more conduction loss and hence decreasing its efficiency also in such a configuration since we are using 12 switches the cost goes drastically up. Since there is a series connection of switches both of them might not switch ON /OFF together.

Due to the above disadvantages, we move to multilevel topologies where the stress in every switch is $\frac{v}{n-1}$ where n is the number of switches hence reducing the stress [15]-[17]. A similar approach is taken for three phase systems too as three phase three level converters [18],[19]. Similarly three phase three level resonant converters have been presented in [20]-[27] with several topologies like LLC, LCC, half-bridge, full-bridge etc. The Multilevel topology that has been shown in [28], is shown below and will be further used in the project.

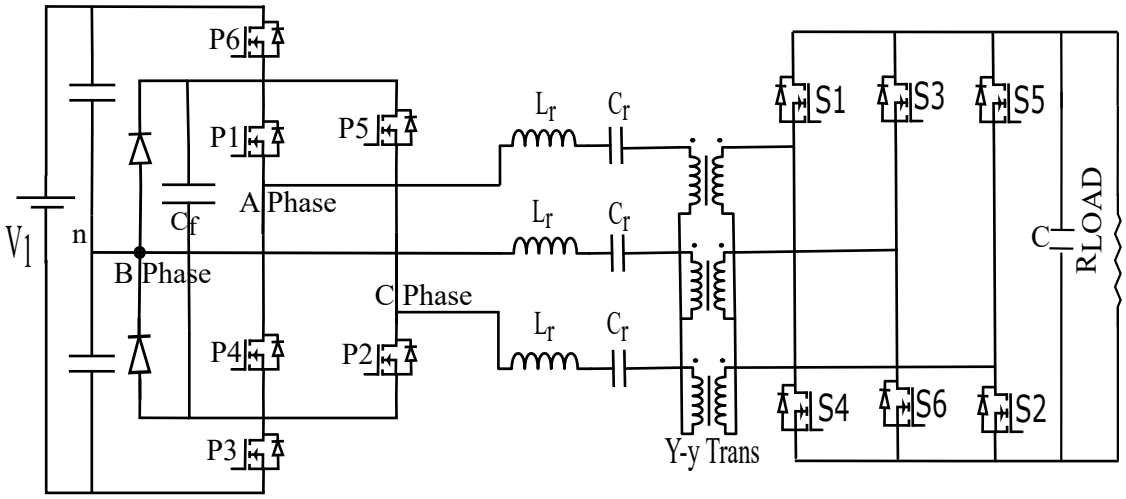


Figure 3.6: Multi-Level Three phase Series Resonant Converter

As earlier mentioned the input to the converter will be of a high voltage DC as it represents the battery/cell package of the EV and the output of the converter is connected to either the inverter to the BLDC or PMSM. In the coming few sections the converter above used shall be explained in detail.

3.3 Switching of the 3ϕ Multilevel SRC

The new topology can be thought of the conventional 3ϕ full bridge where P1 and P4 serve as the switches for Leg A, P6 and P3 serve as the switches for Leg B, P5 and P2 serve as the switches for Leg C. The switching waveforms have been shown in the figures below are at $f_s = 100kHz$,

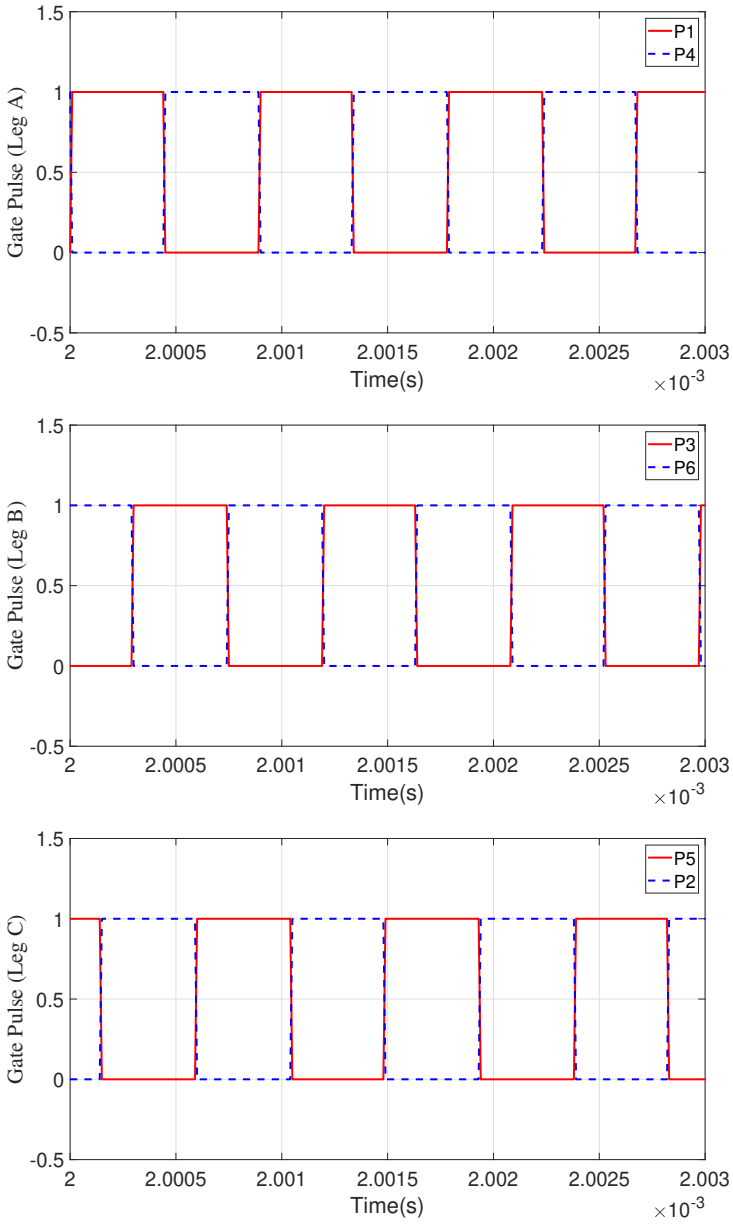


Figure 3.7: Switching of the 3ϕ Multilevel SRC at 1MHz. *(Scale: Y-Axis : 0.5 unit/div, X-axis : 0.5μs/div)*

(The dead-bands haven't been shown here but will be included during the hardware run.)

3.4 Use of Star-star transformer

In [28], the three phase transformer used is a Star-delta transformer. On simulations and observation, it is found out that when Star-delta transformer is used instead of a Star-star transformer, for the same output greater turns ratio is required by a factor of $\sqrt{3}$, now for a similar performance greater Quality factor is required so bigger inductor is required, making the converter bulky one. Finally since the secondary is delta the third harmonics circulate in the secondary winding which get reflected in the star side making the current non sinusoidal. For these mentioned reasons it is recommended to use a Star-star Transformer.

3.5 Use of C_f

In Fig.3.6 the capacitor C_f used is pretty similar to the clamping/flying capacitor in a multilevel converter. The two main use of this capacitor is, firstly the capacitor provides a path for the current when it is not operating in a unity power factor, that is:

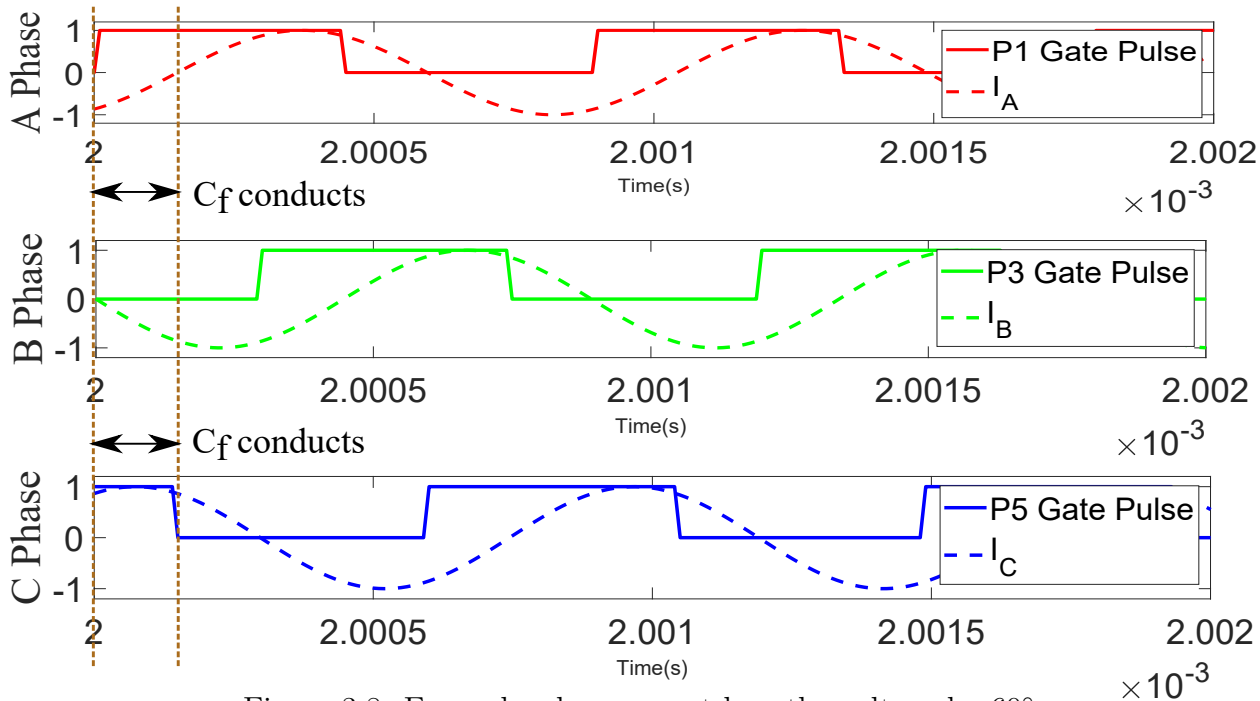


Figure 3.8: Example when current lags the voltage by 60°

As shown above when the current is lagging the voltage by e.g. 60 degrees, for the first 60° P1 is turning On whereas current I_A is negative so the current flows through the body diode of P1, similarly, for phase B switch P6 is ON and

current I_B is negative, the current I_B is always meant to flow through the 'n'. Now for phase C switch P5 is ON and the current I_C is positive. The direction of the current paths has been shown in the figure below:-

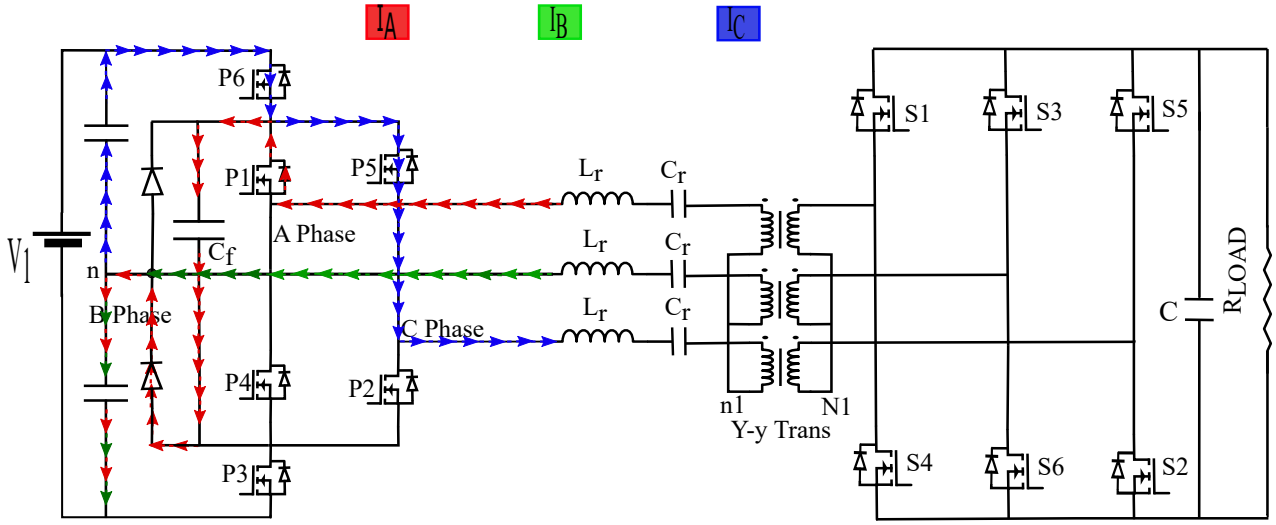


Figure 3.9: Current paths showing importance of C_f

As we can see whenever there is non-unity power factor operation then the current I_A needs a path to flow, this path is provided by the C_f. Consequently the capacitor functions as a coupling capacitor for phase A to the DC bus neutral 'n'. Another significant use of Capacitor C_f is in favor of decoupling the switching transition of all switches, such that when there is switch over from A$\overline{B}$C to ABC to reduce those transitions this acts also as a snubber capacitor [28].

3.6 Effect of L_m

Addition of the Series Resonance to the converter at a certain Q makes the current sinusoidal but the voltage appearing across the transformer is still a square wave so the transformer's magnetizing inductance L_m that appears parallel to this voltage draws a triangular current since $V = L\frac{di}{dt}$, that results in the primary current to be non sinusoidal since it becomes the summation of a triangular and a sinusoidal current,so for simulation purposes to study the behavior of the converter, it is recommended to keep the L_m as high as possible to minimize this effect. This is why ideally a transformer's L_m is supposed to be infinite.

3.7 Load Dependency

As the load resistance is increased, the output voltage increases but output current is decreased so the primary current too gets reduced now, at this time the third harmonics in the primary current get dominant resulting in a non-sinusoid current so this should be taken care of while simulations, very high output resistance must be avoided to avoid such situations or better use an inductor of high Q.

3.8 Equivalence of this topology to the conventional 3ϕ SRC

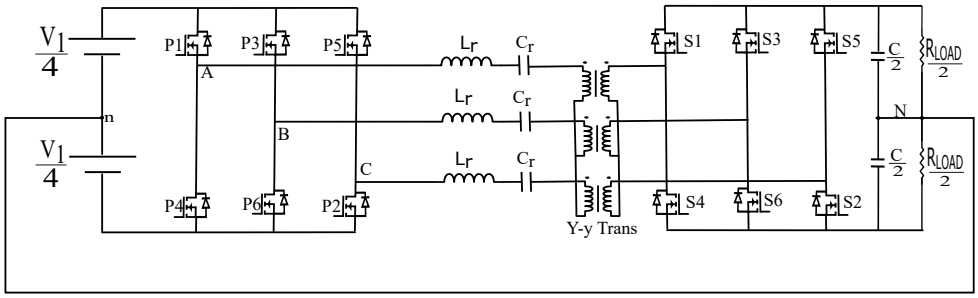


Figure 3.10: Equivalent three-phase circuit by fundamental harmonic analysis

As we can see the gain becomes half [28] to that of the conventional 3phase SRC so we require a 1:2 Star:star transformer to obtain the same voltage at the output. This is an apparent drawback for the converter design but the afore mentioned advantages compensate for the use of a 1:2, Y:y Transformer.

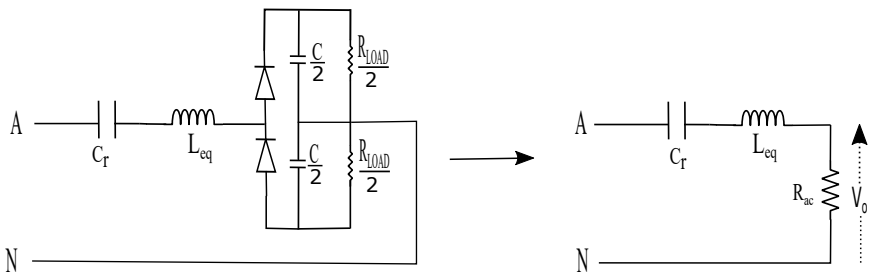


Figure 3.11: Per phase equivalent(line-neutral)

This equivalent three phase topology can be simplified to single phase equivalent due to the symmetrical structure, where $L_{eq} = L_r + L_{lk}$ and $R_{ac} = \frac{6}{\pi^2} R_{LOAD}$.[28]

3.9 Pole and Line Voltages

Shown below are the line voltages V_{AB}, V_{BC}, V_{CA} which can be easily inferred when referred to switching states in Section 3.2. But finding out the pole voltages is a bit difficult since the Transformer primary Neutral(N) is floating. We know

$$V_{AB} = V_{AN} - V_{BN} \tag{3.1}$$

$$V_{BC} = V_{BN} - V_{CN} \tag{3.2}$$

$$V_{CA} = V_{CN} - V_{AN} \tag{3.3}$$

From the above equations it can be derived that

$$V_{AN} + V_{BN} + V_{CN} = 0 \tag{3.4}$$

Using (3.1),(3.2)(3.4) we get

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \begin{bmatrix} V_{AB} \\ V_{BC} \\ 0 \end{bmatrix} \tag{3.5}$$

From (3.5) we get the pole voltages as:-

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ -\frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ -\frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} V_{AB} \\ V_{BC} \\ 0 \end{bmatrix} \tag{3.6}$$

3.10 Calculation of Quality Factor

Quality factor of the SRC is calculated as $Q = \frac{\omega_o L}{R}$ where L is equal to the total inductance in a phase $(L_r + L_{lk_1} + n^2 L_{lk_2})$, where L_r is the resonant inductor, L_{lk_1} refers to the leakage inductance of the primary winding of transformer, L_{lk_2} refers to the leakage inductance of the secondary winding of transformer, R is the series resistance in SRC and not the equivalent AC resistance,and ω_o equals to the resonant frequency in rad/sec and n is the turns ratio [30]. The Quality factor calculation has been done on the assumption that the magnetizing inductance of the transformer is very high. When we consider the converter to be ideal during simulations the Q of the coil is ∞ since R=0.

3.11 Conclusion

In this chapter, a vivid discussion on the Multilevel 3ϕ converter has been made. The importance of its various circuit components has been explained along with the appropriate choice of Q of the converter.

The objective of using this converter is to make a Dual active bridge out of the Series resonant converter i.e when the SRC is switched at $f_S > f_r$ then $X_L > X_C$ making the circuit behaves as a simple inductor. And upon doing the fundamental harmonic analysis since the Quality factor is quite high, it is a pure sinusoid when f_s is close to f_r so our assumption of doing the Fundamental Harmonic Approximation is quite valid. As we already know that power flows from leading to lagging voltage. On doing the Fundamental Harmonic Approximation the very well-known equation of power transfer between two voltage sources can be applied $P = \frac{V_{1_i} V_{2_i}}{X}\ sin\delta$; where V_{1_i} stands for the fundamental of the input side voltage; $V_{1_i} = \frac{4V_1}{\pi\sqrt{2}}$. V_{2_i} stands for the fundamental of the output side voltage; $V_{2_i} = \frac{4V_2}{\pi\sqrt{2}}$. X stands for the equivalent inductive impedance; X=$\omega L - \frac{1}{\omega C}$. δ stands for the phase lead/lag between the voltage sources [27], [29]. Hence the power flow can be controlled by varying the f_s or δ. In the forthcoming chapter, the discussed converter shall be simulated at various frequencies and at various conditions to have a better understanding of the converter.

Chapter 4

Simulation of the Multilevel 3ϕ SRC

4.1 Simulation of the Converter (Ideal)

The converter is designed for 600V-DC(input) to 40V-DC(output). Refer to Fig 3.6. The converter specifications are $V_1 = 550V - 600V$DC, $V_o = 40V$DC, $I_o = 8A$, Turns ratio=10:1, $L_{lk} = 13\mu H$, $f_r = 800kHz$, $L_r = 200\mu H$, $C_r = 180pF$ and $C_o = 30\mu F$.

The following simulations have been done in MATLAB/SIMULINK Environment. The switching waveforms of the devices have been shown in the earlier sections. For the simulations it has been assumed that the transformer, the switches, capacitors, and inductors used are lossless and perfectly ideal that is no saturation and zero losses. The transformer is assumed to take zero magnetization current due to infinite L_m. The assumptions are necessary to ease the analysis hence we omit the aforementioned parameters. The simulation results are only shown for phase A, the same applies to all the other phases too just they are shifted by 120°s.

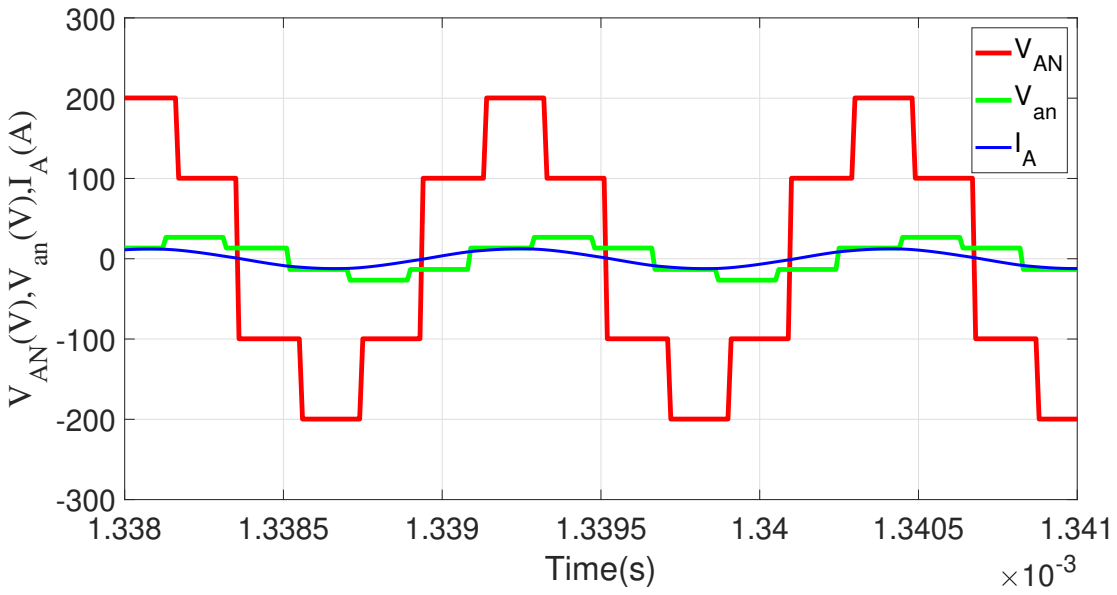


Figure 4.1: V_{AN}, V_{an}, I_A. *(Scale: Y-axis : 50 V,A/div, X-axis : 0.5µs/div)*

There exist several possible values of the phase shift δ and f_s for which the power flow can be adjusted to obtain 40V at the output. Here δ, f_s is chosen to be 47° and $862.63kHz$ respectively, the reason shall be explained in the chapter following.

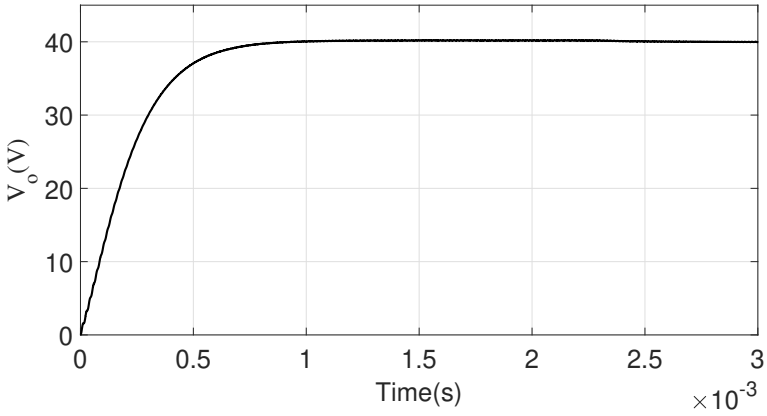


Figure 4.2: V_o. *(Scale : Y-axis : 10V/div, X-axis: 0.5ms/div)*

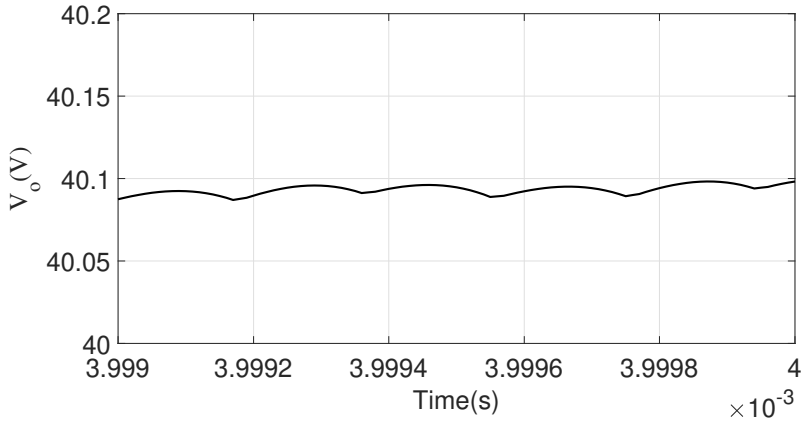


Figure 4.3: $V_{o_{magnified}}$. *(Scale: Y-axis : 50mV/div, X-axis : 0.2μs/div)*

The output of the converter is shown above. The output voltage ripple is less than 1mV and rises within 0.6ms.

As earlier mentioned δ and f_s are such chosen that the current I_A lags V_{AN} but leads V_{an}. As per the current direction for the input bridge when the current is negative, voltage is positive the diode conducts, and later the switch turns on hence it is ZVS during turn ON. Whereas for the output bridge the current direction is opposite to that of the conventional current direction, hence ZVS during turn ON for the output bridge too. Whereas the turn Off is hard switching hence we reduce the switching losses to half. Guaranteeing ZVS not only assures zero switching losses but additionally limits overshoots during the switching ON which may cause device failure if not suppressed.

As seen in Section 3.5, C_f plays an important role in the converter. Shown below is the simulation result explaining the above. For confirming the importance,

f_s was increased so that the current lags the input voltage by around 12° and the turns ratio is changed to 1:5 to increase the primary current making the importance prominent.

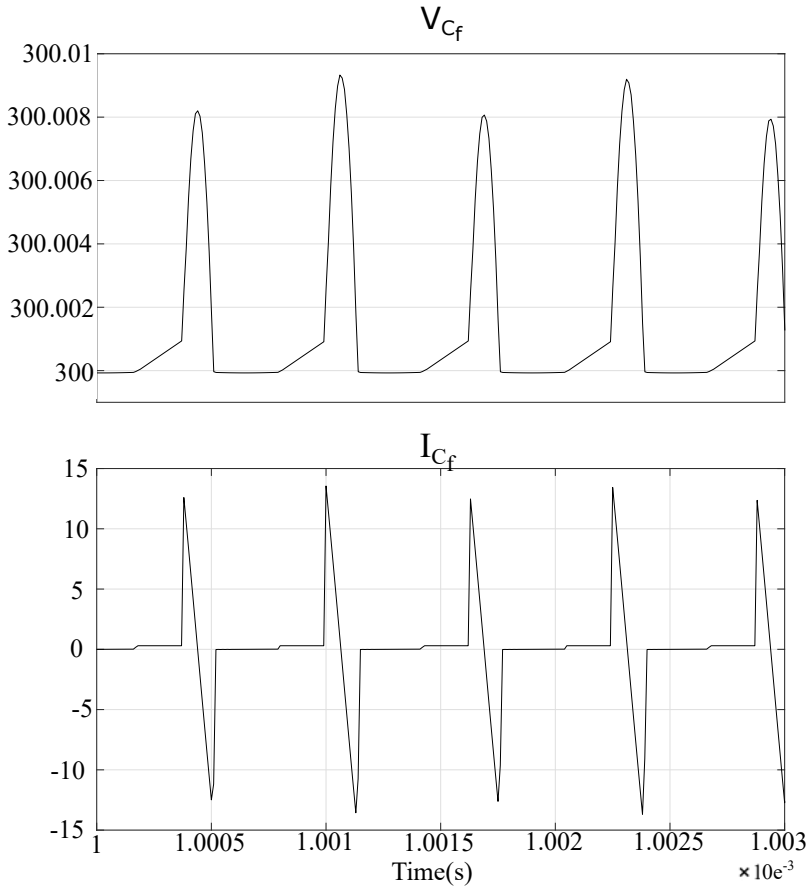


Figure 4.4: V_{C_f}, I_{C_f}. *(Scale: Y-axis : 2 mV, 5A/div, X-axis : 0.5μs/div)*

At the zero crossing of V_{AN}, I_A is -12.5A. This current is being supplied by the freewheeling capacitor hence voltage of the C_f increases first and then decreases when the current goes negative.

As per the specifications the input voltage might vary from 550V to 600V, simulations have been already done for 600V. For getting the same output voltage when $V_1 = 550V$ control algorithms shall be implemented on the converter to reduce the switching frequency and adjust the phase shift so as to adjust the power flow to maintain the ZVS condition as above mentioned. Till now the converter has been operated considering all elements to be ideal, in the coming section working of the converter with non idealities shall be explained.

4.2 Simulation Results of the Converter (Non-Ideal)

As shown in the earlier section are the results for the converter when operated in ideal conditions, here all the parameters are similar to the earlier run but here we include all the non-idealities like L_m, R_c, $R_{DS_{ON}}$, R_w and inductor's coil resistance. Here we consider the sum of all series resistance to be R per phase =5Ω as the chosen resonant inductor is pretty bulky and must have many turns.

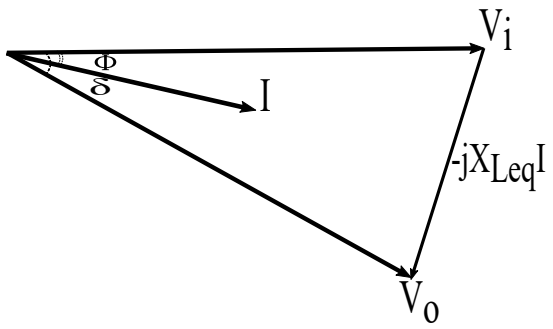


Figure 4.5: Ideal Converter Phasor Diagram

Here V_i represents the fundamental rms of the input side Line to Neutral voltage of any single phase where $V_i = \frac{4\frac{V_1}{2}}{\pi\sqrt{2}}$, V_0 represents the fundamental rms value of the output side Line to Neutral voltage of a single phase where $V_0 = \frac{4V_o}{\pi\sqrt{2}}$ reflected to transformer primary, I represents per phase rms of transformer primary current and $X_{L_{eq}} = \omega L_r + \omega L_{lk} - \frac{1}{\omega C_r}$. As we adjust δ of the output bridge, the output $V_0 \angle \delta$ is produced as per the phase difference between I and V_i, and the chosen f_s. Refer to the per phase equivalent circuit (Sec 3.8) for clarity. Now if we include the non-idealities that have been mentioned earlier.

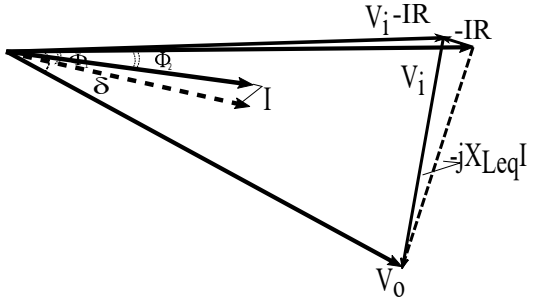


Figure 4.6: Non-Ideal Converter Phasor Diagram

Out of the many possible values of the phase shift δ and f_s for which the power flow can be adjusted to obtain 40V at the output. Here δ is chosen to be 48° and $f_s = 861.9kHz$, now the effect of adding the resistances will be explained using phasor diagrams.

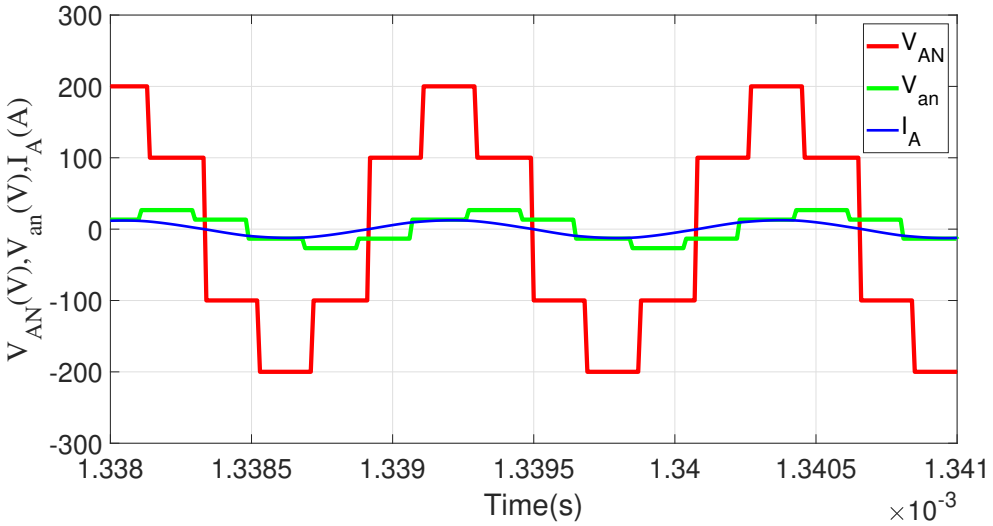


Figure 4.7: V_{AN}, V_{an}, I_A. *(Scale : Y-axis : 50 V,A/div, X-axis : 0.5μs/div)*

As explained earlier, after the introduction of $R = (R_{DS_{ON}} + R_w)$ to get the same $V_o\angle\delta$ the angle ϕ has to be reduced that is $\phi_1 < \phi$, therefore to decrease ϕ, f_s needs to be reduced so that $X_{L_{eq}}$ gets reduced allowing more power flow in order to compensate the losses.

The output of the converter is illustrated below.

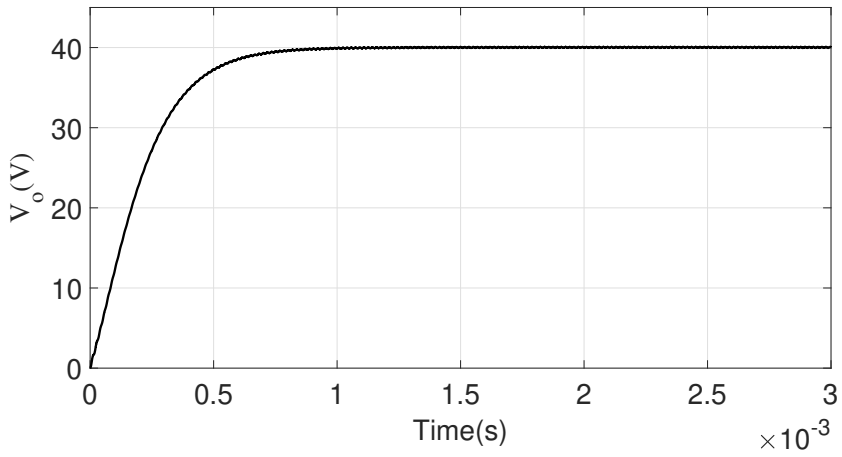


Figure 4.8: V_o. *(Scale: Y-axis : 5 V/div, X-axis : 0.5ms/div)*

As seen from the above output, the voltage rises within 1ms to attain the desired 40V.

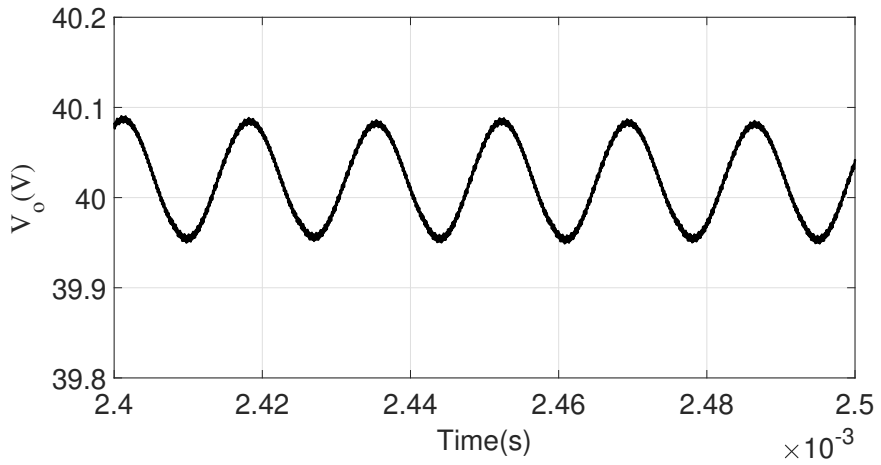


Figure 4.9: $V_{o_{magnified}}$. *(Scale: Y-axis : 5mV/div, X-axis : 0.02ms/div)*

Hence the converter output is 40V with a ripple of 0.1V that is within the converter specifications. Rise time of V_o changes in μs so its change is not significant enough. As we have already seen the behavior of the converter when operated with passive load, the above designed converter is also used for recharging of a battery that is an active source on the output.

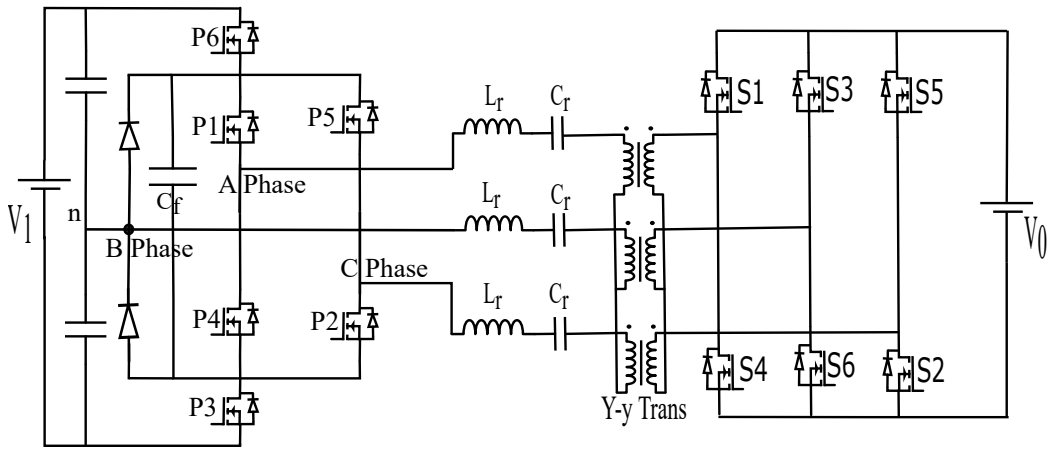


Figure 4.10: Multi-Level Three phase Series Resonant Converter with Active source at the output

Now the converter's output current is required to be 8A as for a passive load already discussed. The converter specifications are $V_1 = 600V$DC, $V_o = 40V$DC, Turns ratio=1:5, $L_{lk} = 13\mu H$, $f_r = 1MHz$, $L_r = 100\mu H$, $C_r = 224pF$, $I_{oavg} = 8A$ To achieve the required, we adjust $\delta = 47°$ and $f_s = 1.12MHz$ assuming everything ideal. The simulation results for the above converter will be shown in the following page.

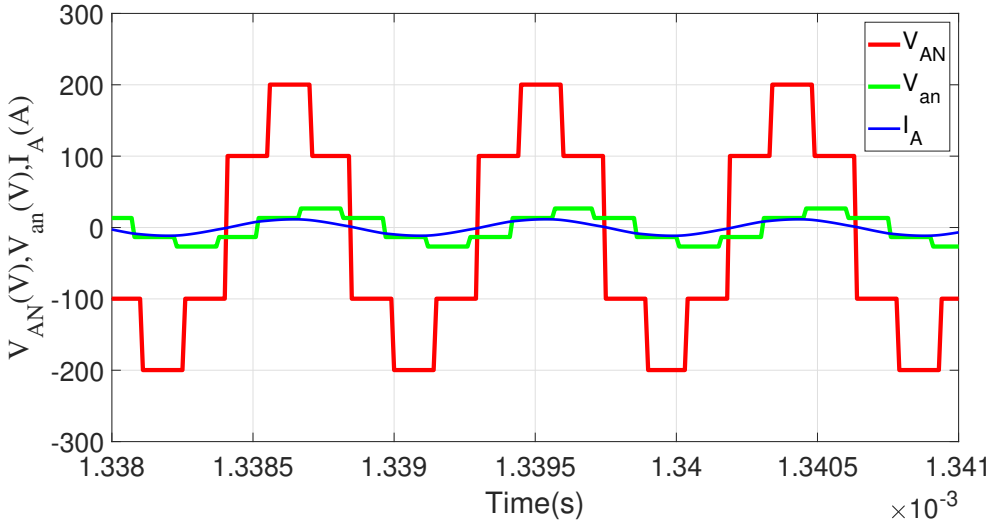


Figure 4.11: V_{AN}, V_{an}, I_A.*(Scale: Y-axis : 50 V,A/div, X-axis : 5µs/div)*

4.3 Line and Phase voltages of the converter at $f_r = 1MHz$

The magnitude of the phase and line voltages remain the same irrespective of the f_s, so it has been shown only once. Their derivation has been presented in Section 3.9.

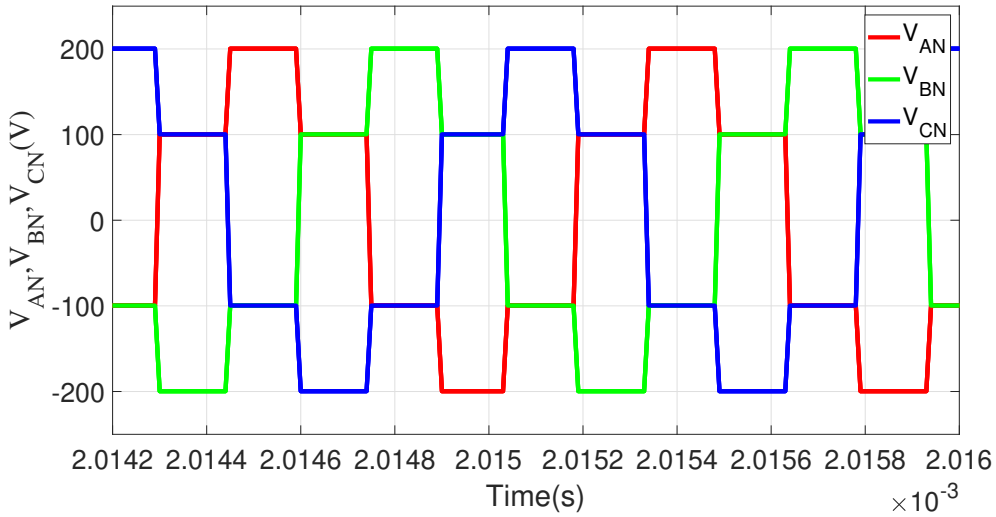


Figure 4.12: Phase Voltages at the primary side.*(Scale: Y-axis : 100 V/div, X-axis : 0.2µs/div)*

Shown above are the phase voltage waveforms, which is a four level waveform with steps of $\pm\frac{V_{DC}}{3}$ and $\pm\frac{V_{DC}}{6}$.

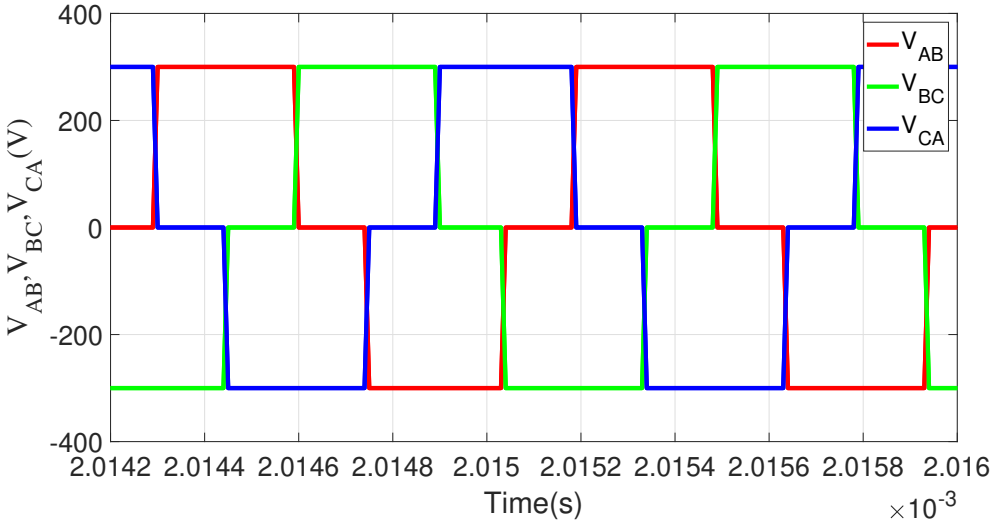


Figure 4.13: Line Voltages at the primary side. *(Scale: Y-axis : 200 V/div, X-axis : 0.2μs/div)*

Shown above are the line voltage waveforms, which is a three level waveform with steps of $\pm\frac{V_{DC}}{2}$ and 0. The relationship between the line and phase voltages can be verified using eq.(3.6).

4.4 Conclusion

In this chapter, the earlier discussed Three Phase Three Level converter has been simulated with the given specifications of 600-40V DC-DC converter with output current. The converter has been simulated as both an ideal and with non-idealities. The effect of various series resistances in the converter has been pointed out precisely. Simulations have been done at 800KHz and 1MHz both with passive load and with an active source at the output. Conditions have been met to satisfy ZVS during turn ON which significantly reduces the switching losses to half. Hence with this chapter, we get a good idea of how the converter works and the various parameters that affect its working. In the upcoming chapter study of single phase SRC will be presented which shall remove any uncertainties before moving towards the actual development of the three phase SRC prototype.

Chapter 5

Single Phase SRC

Before moving on to the three phase multilevel topology, it would be better if we first analyze single phase. Later we develop a protoype to validate our analysis. Fig.5.1 is a Single phase SRC which will be operated as DAB to facilitate power flow between the two bridges.

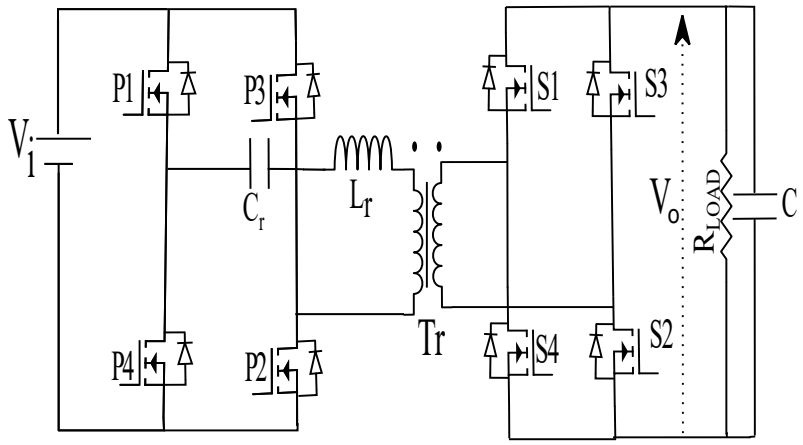


Figure 5.1: 1ϕ SRC

where $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$, the SRC is operated with $f_s > f_r$. As shown in the Fig.3.1 the SRC behaves as an inductor hence the equivalent inductive impedance will be equal to $X_{L_{eq}} = \omega L_r + \omega L_{lk} - \frac{1}{\omega C_r}$. The respective phasor has been shown beneath

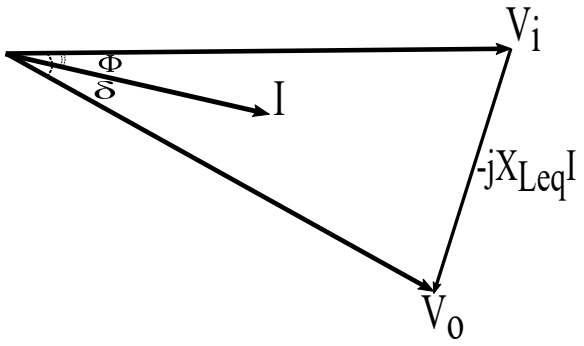


Figure 5.2: Ideal Converter Phasor Diagram

Here V_1 denotes the input DC voltage, V_o denotes the output DC voltage. V_i represents the fundamental rms of the input side bridge voltage where $V_i = \frac{4V_1}{\pi\sqrt{2}}$, V_0 represents the fundamental rms of the output side bridge voltage where $V_0 = \frac{4V_o}{\pi\sqrt{2}}$

reflected to transformer primary, and I represents rms of the current in primary of the transformer.

As mentioned in the earlier chapter the selection of the converter parameters and its operating conditions depend upon the gain to be provided by the converter and also satisfying criteria like ZVS while turning ON. The phasor relation stands as:

$$V_i - V_o\angle{-\delta} = jXI\angle{-\phi}$$

$$or, \quad \frac{4V_1}{\pi\sqrt{2}} - \frac{4V_0}{\pi\sqrt{2}}\angle{-\delta} = IX\angle{90} - \phi \tag{5.1}$$

Separating the real part and the imaginary parts from eq.5.1

$$or, \quad \frac{4V_1}{\pi\sqrt{2}} - \frac{4V_0}{\pi\sqrt{2}}\cos\delta = IX\sin\phi \tag{5.2}$$

$$or, \quad \frac{4V_0}{\pi\sqrt{2}}\sin\delta = IX\cos\phi \tag{5.3}$$

Dividing eq.5.2 by eq.5.3 we get:

$$\tan\phi = \frac{V_1 - V_0\cos\delta}{V_0\sin\delta} \tag{5.4}$$

For achieving a ZVS, the condition that needs to be satisfied is

- $\phi > 0$ to achieve ZVS during turn ON of the input side bridge.
- $\phi < \delta$ to achieve ZVS during turn ON of the output side bridge.

Hence
$$\tan\phi > 0 \tag{5.5}$$

and
$$\tan\phi < \tan\delta \tag{5.6}$$

Putting the value of $\tan\phi$ from eq.5.4 in eq.5.5 we get;

$$\frac{V_1 - V_0\cos\delta}{V_0\sin\delta} > 0$$

$$or, V_1 > V_0\cos\delta$$

$$or, \boxed{\cos\delta < \frac{V_1}{V_0}} \tag{5.7}$$

Now putting the value of $\tan\phi$ from eq.5.4 in eq.5.6 we get;

$$\frac{V_1 - V_0\cos\delta}{V_0\sin\delta} < \tan\delta$$

$$or, V_1 - V_0\cos\delta < \frac{V_0\sin^2\delta}{\cos\delta}$$

$$or, V_0 > V_1 \cos\delta$$

$$or, \boxed{\cos\delta < \frac{V_0}{V_1}} \tag{5.8}$$

Therefore by the above two conditions, we satisfy ZVS for both the bridges of the converter. When the SRC is operated in Buck mode that is $V_0 < V_1$ then eq.5.7 is already satisfied since any $\cos\delta$ is always less than 1, hence only eq.5.8 needs to be satisfied. Similarly when operated in Boost mode that is $V_0 > V_1$ then eq.5.8 is already satisfied since any $\cos\delta$ is always less than 1, hence only eq.5.7 needs to be satisfied. Hence we get a condition for which ZVS can be achieved for both the bridges.By using the the above relations we can find the working parameters for the converter. Referring to the ZVS conditions we find δ and by eq.6.3.4 we can find the f_s to operate the converter at.

For example in our converter design the specifications being $V_o = 30VDC$, $V_i = 40VDC$, $f_r = 800kHz$, $R_{load} = 5\Omega$, turns ratio = 1:1.
Hence the converter parameters can be calculated as
STEP 1 Since $f_r = 800kHz$, we choose $L_r = 10\mu H$ and assuming the transformer has $L_{lk} = 2\mu H$. Hence on computing $C_r = 3.3nF$
STEP 2 Since this is a Buck operations so as per eq.5.8, phase shift($\delta > 41.4°$). Hence we choose $\delta = 45°$.
STEP 3 Referring to eq.6.3.4, on substituting the values, the switching frequency f_s is found to be 825.5kHz.
By following the above few steps one can easily operate the converter to obtain the desired output power making sure the switching losses in the converter are also minimized to the least possible.

With the above obtained parameters the simulations have been done in the coming sections to validate the selection procedure and the ZVS criterion.

5.1 Buck Mode (Ideal)

The converter is designed for 40VDC(i/p) to 30VDC(o/p). The converter specifications are $f_r = 800kHz$, $L_r = 10\mu H$, $L_{lk} = 2\mu H$, $C_r = 3.3nF$, $C_{out} = 66\mu F$ $f_s = 825.5kHz$, $\delta = 45°$, turns ratio= 1:1, $I_o = 6A$. The assumptions considered are that the transformer requires zero magnetization current that is infinite L_m, and infinite R_c and all the lossy components in the converter are considered to be zero.

The simulation results for the deigned converter in ideal conditions will be shown below. In both the conditions the converter is operated in 180° conduction mode.

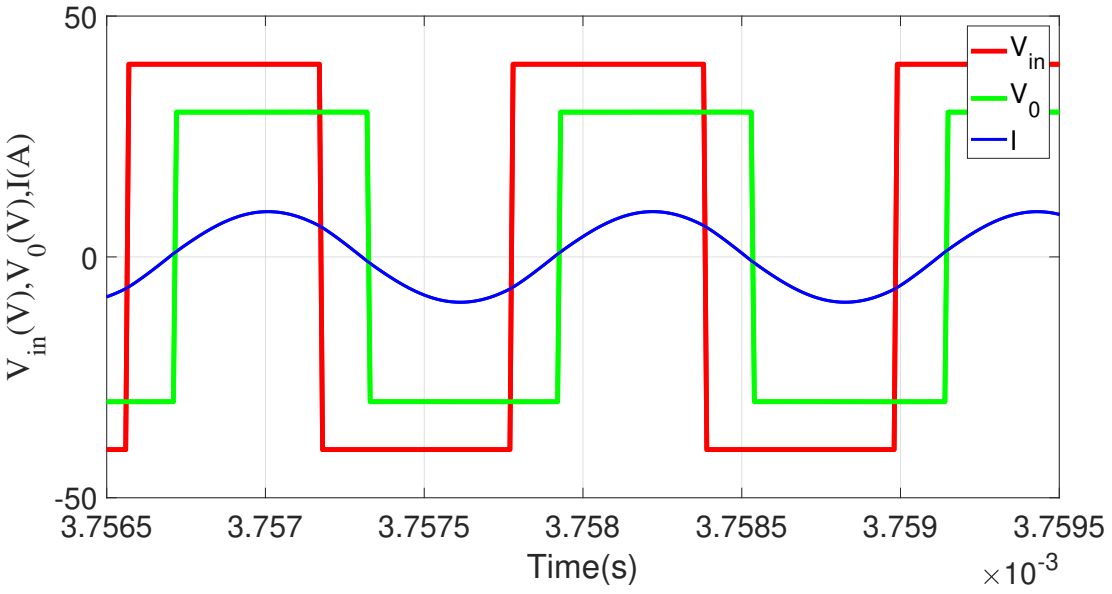


Figure 5.3: Voltages, Current at primary side of 1ϕ SRC *(Scale: Y-axis : 50 V/div, X-axis : 0.5μs/div)*

As seen in the above simulation result the ZVS condition has been satisfied. Interestingly there is ZVS during turn On for both side bridges whereas during turn Off too the output bridge experiences ZVS. V_{in} is of two levels $\pm V_{DC}$ and the output side bridge voltage is of two levels $\pm V_o$.

Below shown are the output voltage of the converter.

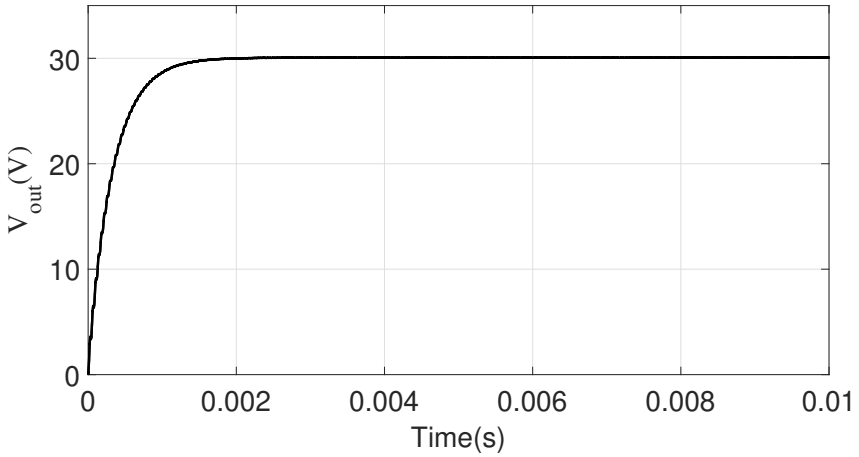


Figure 5.4: *V_o (Scale: Y-axis : 10V/div, X-axis : 2ms/div)*

We can see that the output voltage settles within $2\mu s$ as compared to the three phase topology where it takes around 0.5ms for settling. This subtle difference is due to the reason that in the three phase multilevel SRC bulky capacitors have been chosen so making the time constant larger than that of the single phase SRC.

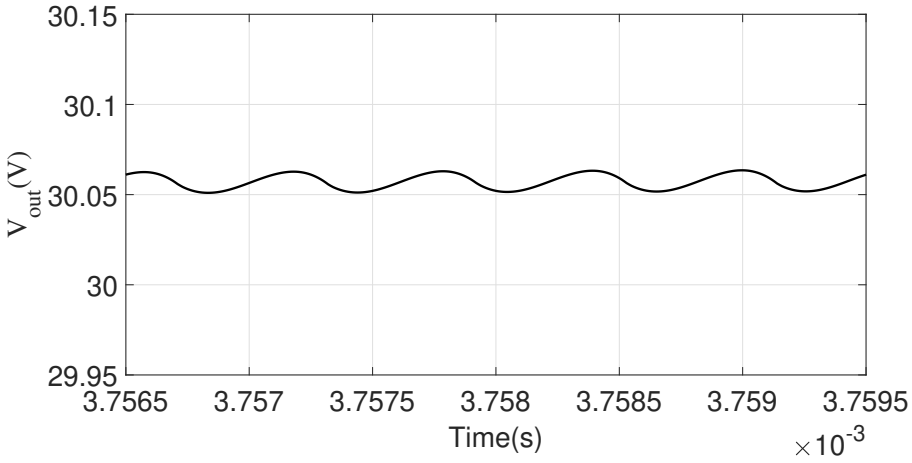
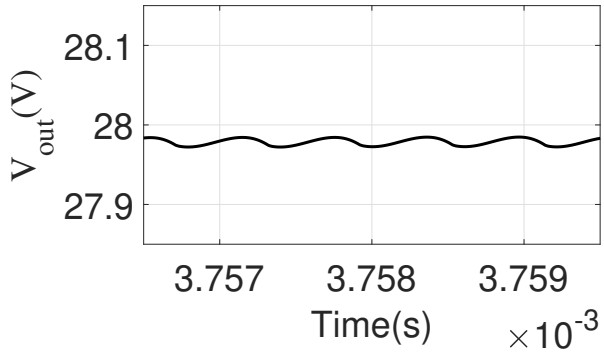


Figure 5.5: *$V_{o_{magnified}}$. (Scale: Y-axis : 0.05V/div, X-axis : 0.5μs/div)*

The above figure illustrates the magnified version of the output voltage, clearly the voltage ripple is less than 10mV that is less than 0.5% of the output voltage, the ripple can be further reduced by increasing the output capacitance. The frequency of the output voltage ripple is observed to be equal to twice the switching frequency.

5.2 Buck Mode(Non Ideal)

As already mentioned in the Sec.4.2 with the phasor diagram Fig.4.6, similarly here too we shall include all the non linearities into the converter like L_m, R_c, $R_{DS_{ON}}$, R_w and coil resistance. The total series resistance is considered to be $50m\Omega$, L_m is considered to be 20 times of L_{lk}, $R_c = 100\Omega$. When run at the same converter parameters it is observed that $V_o < 30V$ shown in the figure below.



Assuming $R_{loss} = 1\Omega$. As seen in the above output, there is a drop in the output voltage due to the presence of the series loss resistances, hence to compensate this loss we can either increase the δ, decrease the f_s as explained in Sec.4.2. Hence we increase δ from 45° to 47° and f_s is decreased to 823kHz. Since L_m is 20 times of L_{lk} so it has a negligible effect on the output which is shown below.

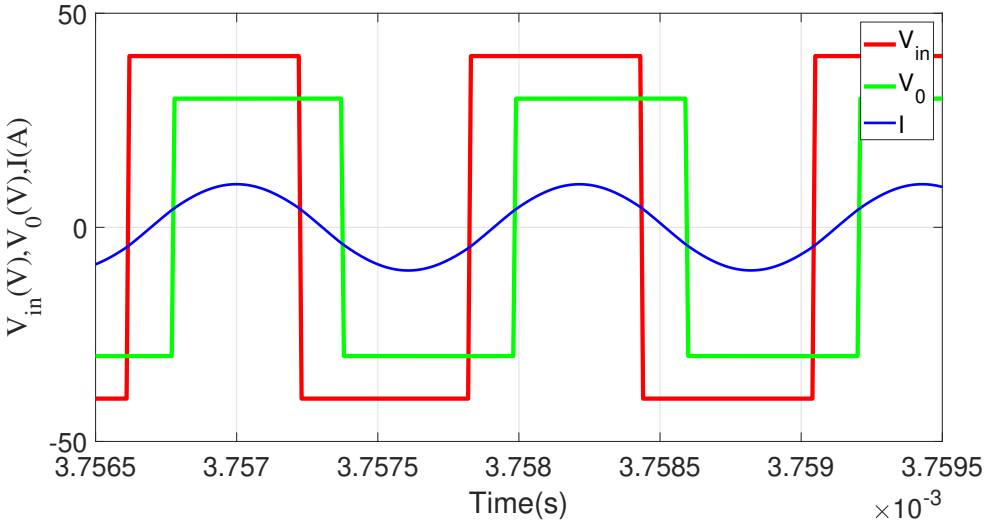


Figure 5.6: Voltages, Current at primary side of 1ϕ SRC. *(Scale: Y-axis : 50 V/div, X-axis : 0.5μs/div)*

Hence by adjusting f_s and δ the output is again achieved as desired. The analysis with non-idealities has been avoided as the equations become too complicated and tough to solve.

5.3 Boost Mode

As already mentioned before the ZVS range can be found out using the eqn.5.7. Now the converter is operated as 40V DC(i/p)- 60V DC(o/p). The converter parameters remain the same as mentioned in the Sec.5.1 only $f_s = 814kHz$ and $\delta = 55°$. Shown below are results of the SRC operated in Boost mode.

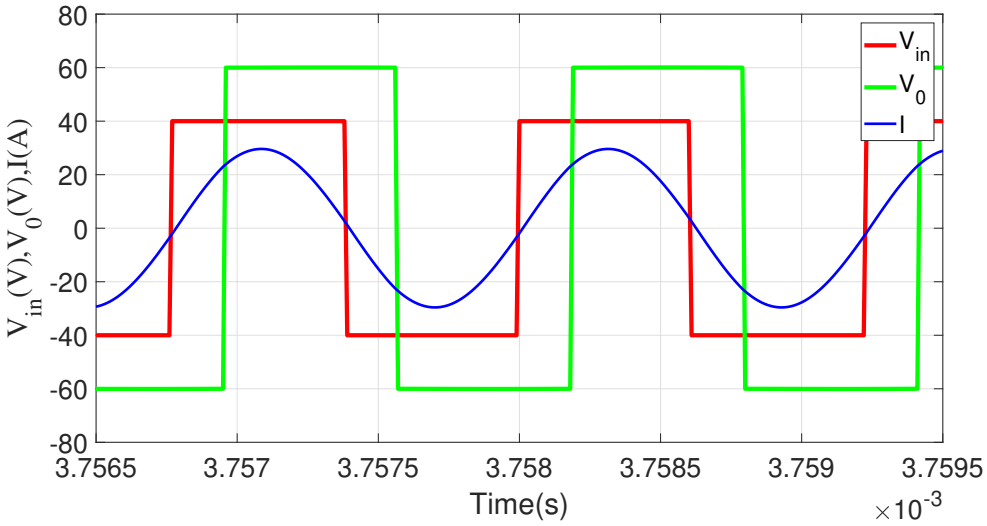


Figure 5.7: Voltages, Current at primary side of 1ϕ SRC *(Scale: Y-axis : 20 V/div, X-axis : 0.5μs/div)*

Here we see the ZVS condition being met, the input voltage is of two levels $\pm 40V$ and the output voltage is of two levels $\pm 60V$.

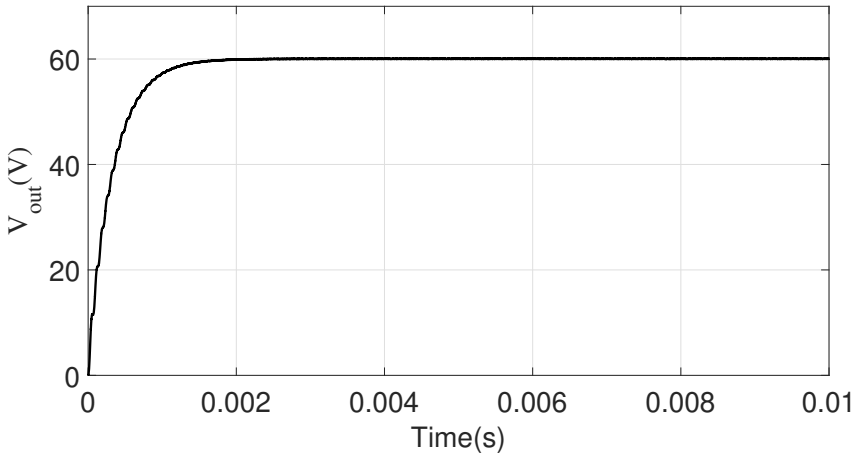


Figure 5.8: V_o *(Scale: Y-axis : 10 V/div, X-axis : 2ms/div)*

The output voltage waveform settles in $2\mu s$. Shown in the next page will be the voltage ripple of the output.

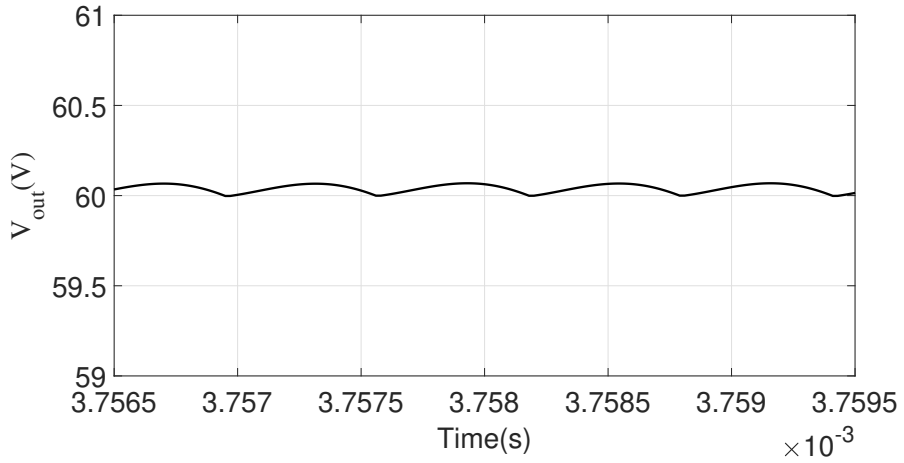


Figure 5.9: $V_{o_{magnified}}$ *.(Scale: Y-axis = 0.5 V/div, X-axis = 0.5μs/div)*

As earlier the output voltage ripple is of less than 20mV hence the converter output is within specifications and the ripple frequency is of $2f_s$.

5.4 Conclusion

In this chapter, a lucid discussion has been done on the 1ϕ SRC's operation as in Buck, Boost both in ideal as well as practical conditions. The effect of losses on the converter's gain has been discussed and the simulations have been done at 800kHz so that it can be used for later purposes when we actually build a GaNFET converter. Importance of ZVS has been clearly explained and conditions that need to be met for operating the converter with least switching losses has been derived.

Chapter 6

Single Phase DAB

6.1 Expression for the current I_p, I

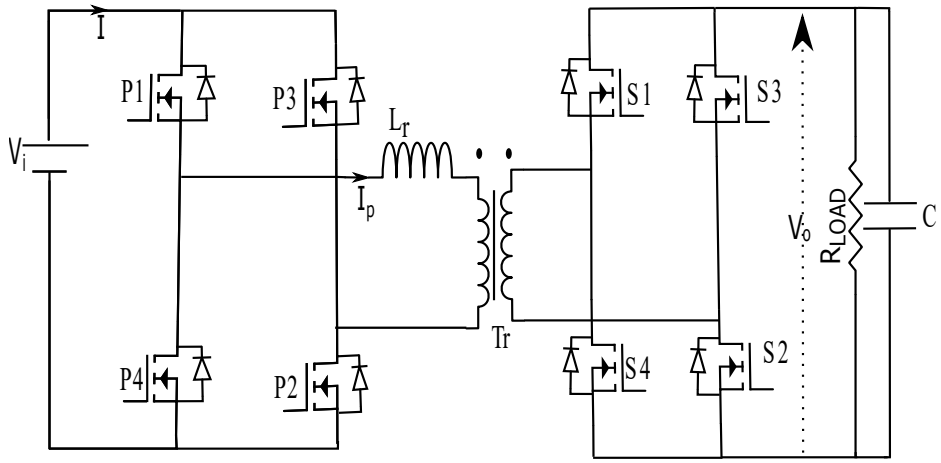


Figure 6.1: Schematic of a DAB

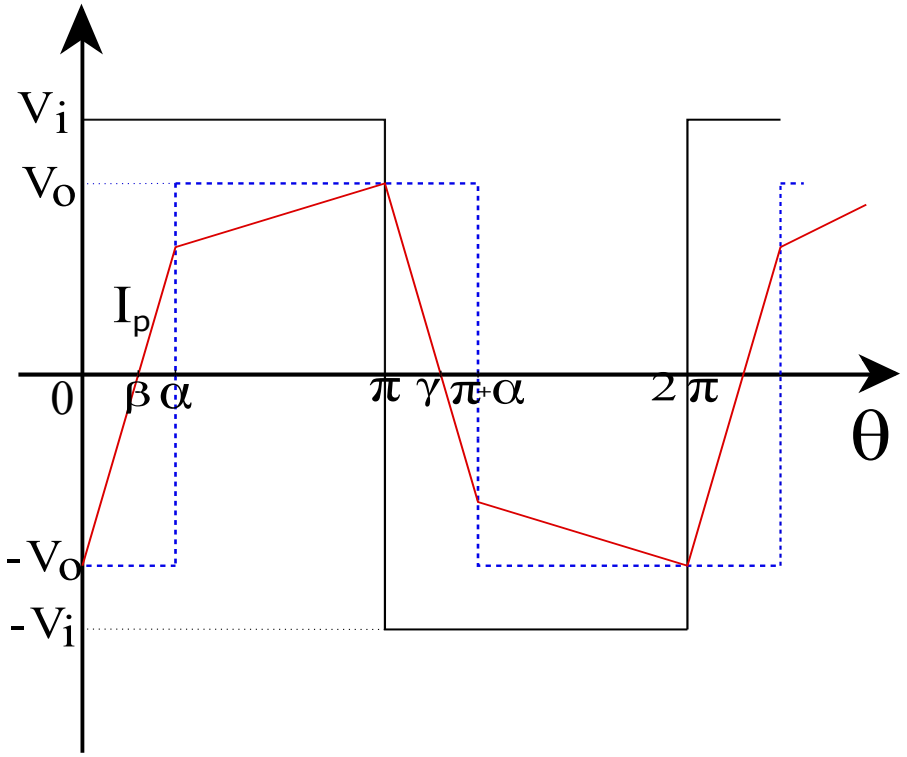


Figure 6.2: V_i, V_o & I_p waveforms in the above shown DAB

As illustrated in the above figure, the input bridge pole voltage is of two levels $\pm V_i$ and the output bridge pole voltage is of two levels $\pm V_o$. the output primary voltage waveform lags the primary pole voltage waveform by an angle α.

The assumptions taken here for easier calculations are :

- All the switches used here are considered to be ideal.
- The transformer used in the above shown schematic is 1:1 with infinte L_m, R_c and zero winding resistance.
- The output capacitor C and inductor L_r are ideal.

For the analysis of a Dual Active Bridge, it is very necessary to find the current flowing through the transformer windings. As shown in Fig.6.1, the current in the transformer primary is I_p since the transformer is 1:1 so $I_s = I_p$.
We know

$$V_L = L\frac{di}{dt}$$

As seen in Fig.6.1, V is the voltage appearing across the inductor i.e. the difference of the input side bridge voltage and the output side bridge voltage, since the turns ratio is 1:1. Here L is the summation of L_r and L_{lk}.
Let θ be a running variable where

$$\theta = \omega t$$

$$or \quad d\theta = \omega dt$$

The waveform of primary current as shown in Fig.6.2 can be divided into four time zones in a complete time period of 2π as (0 to α), (α to π), (π to $\pi + \alpha$) and ($\pi + \alpha$ to 2π).

For $0 < \theta < \alpha$

$$V_i + V_o = \omega L\frac{i(\theta) - i(0)}{\theta}$$

$$or \quad i(\theta) = i(0) + \frac{V_i + V_o}{\omega L}\theta \tag{6.1.1}$$

For $\alpha < \theta < \pi$

$$V_i - V_o = \omega L \frac{i(\theta) - i(\alpha)}{\theta - \alpha}$$
$$or \quad i(\theta) = i(\alpha) + \frac{V_i - V_o}{\omega L}(\theta - \alpha) \tag{6.1.2}$$

For $\pi < \theta < \pi + \alpha$

$$-V_i - V_o = \omega L \frac{i(\theta) - i(\pi)}{\theta - \pi}$$
$$or \quad i(\theta) = i(\pi) - \frac{V_i + V_o}{\omega L}(\theta - \pi) \tag{6.1.3}$$

For $\pi + \alpha < \theta < 2\pi$

$$-V_i + V_o = \omega L \frac{i(\theta) - i(\pi + \alpha)}{\theta - (\pi + \alpha)}$$
$$or \quad i(\theta) = i(\pi + \alpha) - \frac{V_i - V_o}{\omega L}(\theta - (\pi + \alpha)) \tag{6.1.4}$$

The boundary condition for the current is i(π)= -i(0), therefore from the eq.(6.1.2)

$$i(\pi) = i(\alpha) + \frac{V_i - V_o}{\omega L}(\pi - \alpha)$$

Substituting i(α) from eq.(6.1.1) we get;

$$i(\pi) = i(0) + \frac{V_i + V_o}{\omega L}\alpha + \frac{V_i - V_o}{\omega L}(\pi - \alpha)$$
$$or, -i(0) = i(0) + \frac{V_i + V_o}{\omega L}\alpha + \frac{V_i - V_o}{\omega L}(\pi - \alpha)$$
$$or, -2i(0) = \frac{V_i}{\omega L}\pi + \frac{V_o}{\omega L}(2\alpha - \pi)$$

$$or, i(0) = \frac{V_o}{\omega L}(\frac{\pi}{2} - \alpha) - \frac{V_i}{\omega L}\frac{\pi}{2} \tag{6.1.5}$$
$$or, i(\pi) = \frac{V_o}{\omega L}(\frac{\alpha - \pi}{2}) + \frac{V_i}{\omega L}\frac{\pi}{2} \tag{6.1.6}$$

Substituting value of i(0) from eq.(6.1.5) in eq.(6.1.1) we get

For $0 < \theta < \alpha$

$$i(\theta) = \frac{V_i}{\omega L}(\theta - \frac{\pi}{2}) + \frac{V_o}{\omega L}(\theta + \frac{\pi}{2} - \alpha) \tag{6.1.7}$$

Similarly finding i(α) by substituting $\theta = \alpha$ in the above equation we obtain;

$$i(\alpha) = \frac{V_i}{\omega L}(\alpha - \frac{\pi}{2}) + \frac{V_i}{\omega L}(\alpha - \frac{\pi}{2}) \tag{6.1.8}$$

Substituting i(α) from the above equation in eq.(6.1.2) we get

For $\alpha < \theta < \pi$

$$i(\theta) = \frac{V_i}{\omega L}(\theta - \frac{\pi}{2}) + \frac{V_o}{\omega L}(\frac{\pi}{2} - \theta + \alpha) \tag{6.1.9}$$

Similarly on substituting i(π) from eq.(6.1.6) in eq.(6.1.3) and eq.(6.1.4) we get;

For $\alpha < \theta < \pi + \alpha$

$$i(\theta) = \frac{V_i}{\omega L}(\frac{3\pi}{2} - \theta) + \frac{V_o}{\omega L}(\frac{\pi}{2} - \theta + \alpha) \tag{6.1.10}$$

For $\pi + \alpha < \theta < 2\pi$

$$i(\theta) = \frac{V_i}{\omega L}(\frac{3\pi}{2} - \theta) + \frac{V_o}{\omega L}(\theta - \alpha - \frac{3\pi}{2}) \tag{6.1.11}$$

Hence eqs. (6.1.7), (6.1.9), (6.1.10), and (6.1.11) govern the current waveform I_p. In the later sections, the above-obtained equations of the current shall be used to perform the Fourier Analysis.

Now we see the conduction states of various diodes and switches in the input side bridge, as per the Fig.6.2 when:

$0 < \theta < \beta$, V_i is +ve, I_p is -ve so body diodes of P1 and P2 conduct.

$\beta < \theta < \pi$, V_i is +ve, I_p is +ve so P1 and P2 conduct.

$\pi < \theta < \gamma$, V_i is -ve, I_p is +ve so body diodes of P3 and P4 conduct.

$\gamma < \theta < 2\pi$, V_i is -ve, I_p is -ve so P3 and P4 conduct.

The current I in the DC Bus V_i, is the summation of the currents flowing through P1 and P3. When the switch P3 or its diode conducts the direction of current flow is opposite to that of the actual convention as taken in I_p so from π to 2π we take negative I_p to find I. The waveform of I will be shown on the following page.

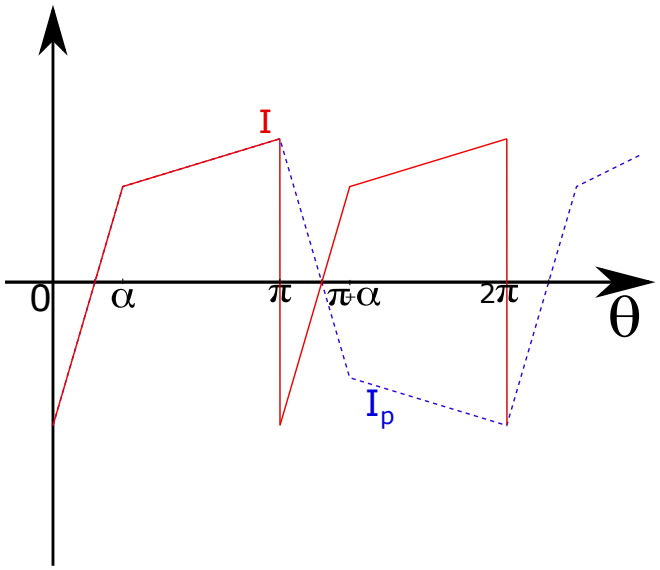


Figure 6.3: I, I_p waveforms in a DAB

As seen in the above figure the current waveform I is periodic with a period of π and has similar expression to that of I_p between 0 to π. Now we shall find the average of I so that later we can compute the DC Power.

$$I_{avg} = \frac{1}{\pi}\int_0^{\pi} I(\theta)d\theta$$

Substituting $I(\theta)$ from eq.(6.1.7) and eq.(6.1.9) we get:

$$= \frac{1}{\pi}\left\{\int_0^{\alpha}\left[\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\theta+\frac{\pi}{2}-\alpha)\right]d\theta+\int_{\alpha}^{\pi}\left[\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\frac{\pi}{2}-\theta+\alpha)\right]d\theta\right\}$$

$$= \frac{1}{\pi}\left\{\int_0^{\pi}\left[\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})\right]d\theta+\int_0^{\pi}\left[\frac{V_o}{\omega L}\frac{\pi}{2}\right]d\theta+\int_0^{\alpha}\left[\frac{V_o}{\omega L}(\theta-\alpha)\right]d\theta+\int_{\alpha}^{\pi}\left[\frac{V_o}{\omega L}(\alpha-\theta)\right]d\theta\right\}$$

$$= \frac{1}{\pi}\left\{\frac{V_i}{\omega L}\left(\frac{\theta^2}{2}-\frac{\pi\theta}{2}\right)\Big|_0^{\pi}+\frac{V_o}{\omega L}\frac{\pi\theta}{2}\Big|_0^{\pi}+\frac{V_o}{\omega L}\left(\frac{\theta^2}{2}-\alpha\theta\right)\Big|_0^{\alpha}+\frac{V_o}{\omega L}\left(\alpha\theta-\frac{\theta^2}{2}\right)\Big|_{\alpha}^{\pi}\right\}$$

$$= \frac{1}{\pi}\left[\frac{V_i}{\omega L}\left(\frac{\pi^2}{2}-\frac{\pi^2}{2}\right)+\frac{V_o}{\omega L}\left(\frac{\pi^2}{2}+\frac{\alpha^2}{2}-\alpha^2+\pi\alpha-\frac{\pi^2}{2}-\alpha^2+\frac{\alpha^2}{2}\right)\right.$$

$$= \frac{1}{\pi}\frac{V_o}{\omega L}\left[\pi\alpha-\alpha^2\right]$$

$$\boxed{I_{avg} = \frac{V_o}{\omega L}\alpha\left[1-\frac{\alpha}{\pi}\right]} \tag{6.1.12}$$

Now we shall compute the RMS of the Current waveform I_p. Since I_p has half-wave symmetry so RMS of I_p and I is the same.

$$I_{RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi} I^2(\theta)d\theta}$$

Substituting $I(\theta)$ from Equation (6.1.7) and (6.1.9)

$$= \left\{\frac{1}{\pi}\left[\int_0^{\alpha}\left(\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\theta+\frac{\pi}{2}-\alpha)\right)^2 d\theta \right.\right.$$
$$\left.\left. + \int_{\alpha}^{\pi}\left(\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\frac{\pi}{2}-\theta+\alpha)\right)^2 d\theta\right]\right\}^{\frac{1}{2}}$$

$$= \left\{\frac{1}{\pi}\left[\int_0^{\pi}\left(\frac{V_i^2}{\omega^2L^2}\left(\theta^2+\frac{\pi^2}{2^2}-\pi\theta\right)\right)d\theta \right.\right.$$
$$+\int_0^{\alpha}\left(\frac{V_o^2}{\omega^2L^2}\left(\theta^2+\frac{\pi^2}{2^2}+\alpha^2-2\alpha\theta+\pi\theta-\pi\alpha\right)\right)d\theta$$
$$+\int_{\alpha}^{\pi}\left(\frac{V_o^2}{\omega^2L^2}\left(\theta^2+\frac{\pi^2}{2^2}+\alpha^2-2\alpha\theta-\pi\theta+\pi\alpha\right)\right)d\theta$$
$$+\int_0^{\alpha}\left(\frac{2V_iV_o}{\omega L}\left(\theta^2-\alpha\theta+\frac{\alpha\pi}{2}-\frac{\pi^2}{2^2}\right)\right)d\theta$$
$$\left.\left.+\int_{\alpha}^{\pi}\left(\frac{2V_iV_o}{\omega L}\left(-\theta^2+\alpha\theta+\pi\theta-\frac{\alpha\pi}{2}-\frac{\pi^2}{2^2}\right)\right)d\theta\right]\right\}^{\frac{1}{2}}$$

$$= \left\{\frac{1}{\pi}\left[\frac{V_i^2}{\omega^2L^2}\left(\frac{\theta^3}{3}+\frac{\pi^2\theta}{4}-\frac{\pi\theta^2}{2}\right)\right|_0^{\pi}\right.$$
$$+\frac{V_o^2}{\omega^2L^2}\left(\left(\frac{\theta^3}{3}+\frac{\pi^2\theta}{4}+\alpha^2\theta-2\frac{\alpha\theta^2}{2}\right)\right|_0^{\pi}+\left(\pi\alpha\theta-\frac{\pi\theta^2}{2}\right)\Big|_{\alpha}^{\pi}-\left(\frac{\pi\theta^2}{2}-\pi\alpha\theta\right)\Big|_0^{\alpha}\Big)$$
$$\left.+\frac{2V_iV_o}{\omega L}\left(-\frac{\pi^2\theta}{4}\right|_0^{\pi}+\left(\frac{\theta^3}{3}-\frac{\alpha\theta^2}{2}+\frac{\alpha\pi\theta}{2}\right)\Big|_0^{\alpha}+\left(\frac{-\theta^3}{3}+\frac{\alpha\theta^2}{2}-\frac{\alpha\pi\theta}{2}+\frac{\pi\theta^2}{2}\right)\Big|_{\alpha}^{\pi}\right)\Big]\Big\}^{\frac{1}{2}}$$

On simplifying we get;

$$= \left\{\frac{1}{\pi}\left[\frac{V_i^2}{\omega^2L^2}\frac{\pi^3}{12}+\frac{V_o^2}{\omega^2L^2}\frac{\pi^3}{12}+\frac{2V_iV_o}{\omega^2L^2}\left(-\frac{\alpha^3}{3}+\frac{\pi\alpha^2}{2}-\frac{\pi^3}{12}\right)\right]\right\}^{\frac{1}{2}}$$

Let the gain be $\left(\frac{V_o}{V_i}=d\right)$

$$\boxed{I_{RMS} = \frac{V_i}{\omega L}\left\{\frac{1}{\pi}\left[\frac{\pi^3}{12}+d^2\frac{\pi^3}{12}+2d\left(-\frac{\alpha^3}{3}+\frac{\pi\alpha^2}{2}-\frac{\pi^3}{12}\right)\right]\right\}^{\frac{1}{2}}} \qquad (6.1.13)$$

6.2 Harmonic Analysis for the current I_p

As seen in Fig.6.3, current I_p exhibits a half wave symmetry which eases our calculations that is $I_p(\theta) = -I_p(\theta + \pi)$. As per Fourier Series

$$I_p(\theta) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(b_n \cos n\theta + a_n \sin n\theta)$$

where:-

$$a_0 = \frac{2}{\pi}\int_0^{\pi} I_p(\theta)d\theta$$

$$b_n = \frac{4}{2\pi}\int_0^{\pi} I_p(\theta)\cos n\theta d\theta$$

$$a_n = \frac{4}{2\pi}\int_0^{\pi} I_p(\theta)\sin n\theta d\theta$$

Due to half wave symmetry, the odd harmonics are only present in the waveform hence we calculate the Fourier coefficients a_o, a_n, b_n

$a_0 = 0$; since average of I_p is zero.

$$a_n = \frac{2}{\pi}\int_0^{\pi} I_p(\theta)\sin n\theta d\theta; \qquad \text{for n=odd}$$

Substituting I_p from equations (6.1.7) and (6.1.9) we get

$$a_n = \frac{4}{2\pi}\Bigg\{ \int_0^{\alpha}\left[\frac{V_i}{\omega L}(\theta - \frac{\pi}{2}) + \frac{V_o}{\omega L}(\theta + \frac{\pi}{2} - \alpha)\right]\sin n\theta d\theta$$

$$+ \int_{\alpha}^{\pi}\left[\frac{V_i}{\omega L}(\theta - \frac{\pi}{2}) + \frac{V_o}{\omega L}(\frac{\pi}{2} - \theta + \alpha)\right]\sin n\theta d\theta\Bigg\}$$

$$= \frac{4}{2\pi}\Bigg\{ \left[\frac{V_i}{\omega L}\int_0^{\pi}(\theta - \frac{\pi}{2})\sin n\theta d\theta\right] + \left[\frac{V_o}{\omega L}\int_0^{\alpha}(\theta + \frac{\pi}{2} - \alpha)\sin n\theta d\theta\right]$$

$$+ \left[\frac{V_o}{\omega L}\int_{\alpha}^{\pi}(\frac{\pi}{2} - \theta + \alpha)\sin n\theta d\theta\right]\Bigg\}$$

$$= \frac{4}{2\pi}\Bigg[\frac{V_i}{\omega L}\left(\frac{-\theta\cos n\theta}{n}\Bigg|_0^{\pi} + \int_0^{\pi}\frac{\cos n\theta}{n}d\theta + \frac{\pi\cos n\theta}{2n}\Bigg|_0^{\pi}\right)$$

$$+\frac{V_o}{\omega L}\left(\frac{-\theta\cos n\theta}{n}\Bigg|_0^{\alpha} + \int_0^{\alpha}\frac{\cos n\theta}{n}d\theta + \frac{\pi\cos n\theta}{2n}\Bigg|_{\pi}^{0}\right.$$

$$\left.-\frac{\theta\cos n\theta}{n}\Bigg|_{\alpha}^{\pi} + \int_{\pi}^{\alpha}\frac{\cos n\theta}{n}d\theta + \frac{\alpha\cos n\theta}{n}\Bigg|_0^{\alpha} - \frac{\alpha\cos n\theta}{n}\Bigg|_{\alpha}^{\pi}\right)\Bigg]$$

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(-\frac{\pi\cos n\pi}{n}+\frac{\pi}{2n}(\cos n\pi-1)\right)\right.$$
$$\left.+\frac{V_o}{\omega L}\left(\frac{\pi}{2n}(1-\cos n\pi)+\frac{2\sin n\alpha}{n^2}+\frac{\pi\cos n\pi}{n}-\frac{\alpha}{n}-\frac{\alpha\cos n\pi}{n}\right)\right] \tag{6.2.1}$$

When n is odd, $(\cos n\pi = -1)$ putting in eq.(6.2.1) we get;

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(\frac{\pi}{n}-\frac{\pi}{n}\right)+\frac{V_o}{\omega L}\left(\frac{\pi}{n}+\frac{2\sin n\alpha}{n^2}-\frac{\pi}{n}-\frac{\alpha}{n}+\frac{\alpha}{n}\right)\right]$$

$$\boldsymbol{a_n = \frac{4V_o}{\pi\omega L}\frac{\sin n\alpha}{n^2}} \tag{6.2.2}$$

Likewise, now we find the other Fourier series coefficient b_n

$$b_n = \frac{2}{\pi}\int_0^{\pi} I_p(\theta)\cos n\theta d\theta; \qquad \text{for n=odd}$$

Substituting I_p from eq.(6.1.7) and eq.(6.1.9) we get

$$b_n = \frac{4}{2\pi}\left\{\int_0^{\alpha}\left[\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\theta+\frac{\pi}{2}-\alpha)\right]\cos n\theta d\theta\right.$$
$$\left.+\int_{\alpha}^{\pi}\left[\frac{V_i}{\omega L}(\theta-\frac{\pi}{2})+\frac{V_o}{\omega L}(\frac{\pi}{2}-\theta+\alpha)\right]\cos n\theta d\theta\right\}$$

$$= \frac{4}{2\pi}\left\{\left[\frac{V_i}{\omega L}\int_0^{\pi}(\theta-\frac{\pi}{2})\cos n\theta d\theta\right]+\left[\frac{V_o}{\omega L}\int_0^{\alpha}(\theta+\frac{\pi}{2}-\alpha)\cos n\theta d\theta\right]\right.$$
$$\left.+\left[\frac{V_o}{\omega L}\int_{\alpha}^{\pi}(\frac{\pi}{2}-\theta+\alpha)\cos n\theta d\theta\right]\right\}$$

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(\frac{\theta\sin n\theta}{n}\Big|_0^{\pi}-\int_0^{\pi}\frac{\sin n\theta}{n}d\theta-\frac{\pi\sin n\theta}{2n}\Big|_0^{\pi}\right)\right.$$
$$+\frac{V_o}{\omega L}\left(\frac{\theta\sin n\theta}{n}\Big|_0^{\alpha}-\int_0^{\alpha}\frac{\sin n\theta}{n}d\theta+\frac{\pi\sin n\theta}{2n}\Big|_0^{\pi}\right.$$
$$\left.\left.-\frac{\theta\sin n\theta}{n}\Big|_{\alpha}^{\pi}+\int_{\alpha}^{\pi}\frac{\sin n\theta}{n}d\theta-\frac{\alpha\sin n\theta}{n}\Big|_0^{\alpha}+\frac{\alpha\sin n\theta}{n}\Big|_{\alpha}^{\pi}\right)\right]$$

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(\frac{\cos n\pi - 1}{n^2}\right) + \frac{V_o}{\omega L}\left(\frac{\alpha \sin n\alpha}{n} + \frac{\cos n\alpha - 1}{n^2} + \frac{\alpha \sin n\alpha}{n}\right.\right.$$

$$\left.\left. + \frac{\cos n\alpha - \cos n\pi}{n^2} - \frac{\alpha \sin n}{n} - \frac{\alpha \sin n}{n}\right)\right] \tag{6.2.3}$$

When n is odd, $(\cos n\pi = -1)$ putting in equation (6.2.3) we get;

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(\frac{-2}{n^2}\right) + \frac{V_o}{\omega L}\left(\cancel{\frac{\alpha \sin n\alpha}{n}} + \frac{\cos n\alpha}{n^2} - \cancel{\frac{1}{n^2}} + \cancel{\frac{\alpha \sin n\alpha}{n}}\right.\right.$$

$$\left.\left. + \frac{\cos n\alpha}{n^2} + \cancel{\frac{1}{n^2}} - \cancel{\frac{\alpha \sin n\alpha}{n}} - \cancel{\frac{\alpha \sin n\alpha}{n}}\right)\right]$$

$$= \frac{4}{2\pi}\left[\frac{V_i}{\omega L}\left(\frac{-2}{n^2}\right) + \frac{V_o}{\omega L}\left(\frac{2\cos n\alpha}{n^2}\right)\right]$$

$$\boldsymbol{b_n = \frac{4}{n^2 \pi \omega L}\left(V_o \cos n\alpha - V_i\right)} \tag{6.2.4}$$

Hence

$$\boxed{I_p(\theta) = \sum_{n=1,3,5\ldots}^{\infty}\left[\frac{4}{n^2\pi\omega L}\left(V_o \cos n\alpha - V_i\right)\right]\cos n\theta + \left[\frac{4V_o}{n^2\pi\omega L}\sin n\alpha\right]\sin n\theta} \tag{6.2.5}$$

The RMS of n^{th} harmonic of $I_p(\theta)$ is

$$I_{p_{RMSn}} = \sqrt{\left(\frac{4}{n^2\pi\omega L\sqrt{2}}\left(V_o \cos n\alpha - V_i\right)\right)^2 + \left(\frac{4V_o}{n^2\pi\omega L\sqrt{2}}\sin n\alpha\right)^2}$$

$$= \frac{4}{n^2\pi\omega L\sqrt{2}}\sqrt{\left(V_o \cos n\alpha - V_i\right)^2 + \sin^2 n\alpha}$$

$$= \frac{4}{n^2\pi\omega L\sqrt{2}}\sqrt{V_o^2 + V_i^2 - 2V_oV_i \cos n\alpha}$$

$\frac{V_o}{V_i} = d$

$$\boxed{I_{p_{RMSn}} = \frac{4V_i}{n^2\pi\omega L\sqrt{2}}\sqrt{d^2 + 1 - 2d\cos n\alpha}} \tag{6.2.6}$$

6.3 Essential Converter Parameters

6.3.1 Total Harmonic Distortion (THD)

$$THD = \sqrt{\left(\frac{I_{RMS}}{I_{p_{RMS1}}}\right)^2 - 1}$$

On substituting I_{RMS} from eq.(6.1.13) and $I_{p_{RMS1}}$ from eq.(6.2.6) we get;

$$THD = \sqrt{\left\{\frac{\frac{V_i}{\omega L}\left[\frac{1}{\pi}\left(\frac{\pi^3}{12} + \frac{d^2\pi^3}{12} + 2d\left(\frac{-pi^3}{12} - \frac{\alpha^3}{3} + \frac{pi\alpha^2}{2}\right)\right)\right]^{\frac{1}{2}}}{\frac{4V_i}{\pi\omega L\sqrt{2}}\left[d^2 + 1 - 2d\cos\alpha\right]^{\frac{1}{2}}}\right\}^2 - 1}$$

$$\boxed{THD = \sqrt{\frac{\pi}{8}\left[\frac{\frac{\pi^3}{12}(d-1)^2 - 2d\frac{\alpha^3}{3} + \pi\alpha^2 d}{d^2 + 1 - 2d\cos\alpha}\right] - 1}} \tag{6.3.1}$$

Shown below are the THDs for various voltage gain(d) and phase difference(α)

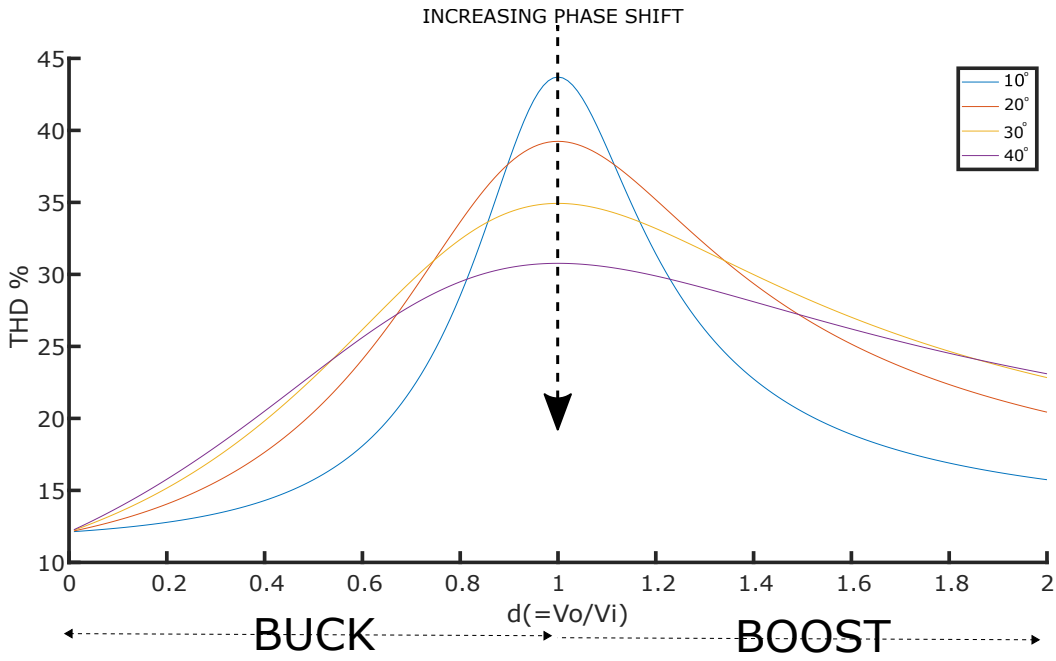


Figure 6.4: Variation of Total Harmonic Distortion vs Voltage Gain(d)

From the above curves, we can conclude that as d increases in the Buck region THD increases. Whereas when d is increased in the Boost Mode the THD decreases. If phase shift is increased the THD decreases.

6.3.2 Transformer Utilization Factor (TUF)

$$TUF = \frac{P_{DC}}{P_{AC}}$$
$$= \frac{V_i I_{avg}}{V_i I_{p_{RMSn}}}$$

Substituting I_{avg} and $I_{p_{RMSn}}$ from eq. (6.1.12) and eq.(6.2.6) we get;

$$= \frac{\frac{V_o}{\omega L}\alpha\left[1-\frac{\alpha}{\pi}\right]}{\frac{V_i}{\omega L}\left\{\frac{1}{\pi}\left[\frac{\pi^3}{12}+d^2\frac{\pi^3}{12}+2d\left(-\frac{\alpha^3}{3}+\frac{\pi\alpha^2}{2}-\frac{\pi^3}{12}\right)\right]\right\}^{\frac{1}{2}}}$$

$$\boxed{TUF = \frac{d\alpha\left[1-\frac{\alpha}{\pi}\right]}{\left\{\frac{1}{\pi}\left[\frac{\pi^3}{12}+d^2\frac{\pi^3}{12}+2d\left(-\frac{\alpha^3}{3}+\frac{\pi\alpha^2}{2}-\frac{\pi^3}{12}\right)\right]\right\}^{\frac{1}{2}}}} \tag{6.3.2}$$

Shown below are the TUFs for various voltage gain(d) and phase difference(α)

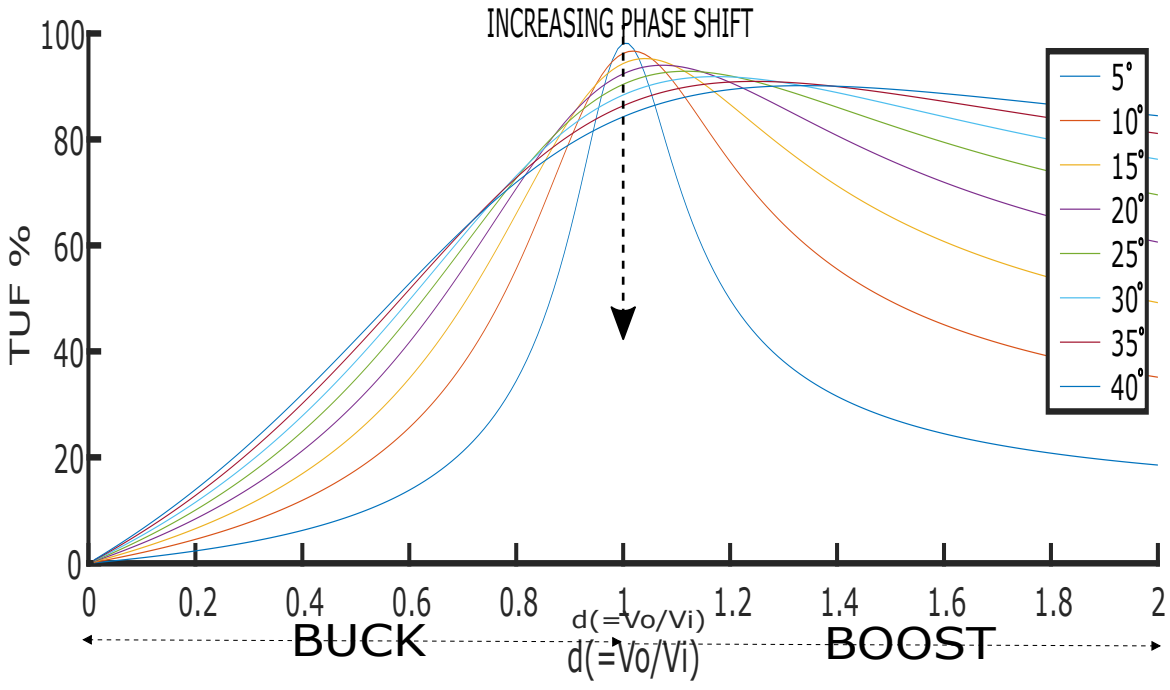


Figure 6.5: Variation of Transformer Utilization Factor vs Voltage Gain(d)

From the above curves, we infer that as d increases in the Buck region TUF increases. Whereas when d is increased in the Boost Mode the TUF decreases. If the phase shift is increased the TUF decreases. However when the phase shift is high i.e. ($\alpha > 40°$) for a given phase shift the TUF saturates in the Boost region.

6.3.3 Real Power (P)

The Real Power deliver by the input is equal to:-

$$P = V_i * I_{avg}$$

Substituting value of I_{avg} from eq.(6.1.12) we get;

$$P = V_i * \frac{V_o}{\omega L}\alpha\left[1 - \frac{\alpha}{\pi}\right];$$

$$or,\ \ P = \frac{V_i V_o}{\omega L}\alpha\left[1 - \frac{\alpha}{\pi}\right];$$

As defined earlier $d = \frac{V_o}{V_i}$

$$\boxed{P = \frac{dV_i^2}{\omega L}\alpha\left[1 - \frac{\alpha}{\pi}\right]} \tag{6.3.3}$$

6.3.4 Output Voltage (V_o)

The real power delivered by the input voltage source V_i is equal to the power delivered to the output resistance considering the system is ideal. Hence V_o is

$$\frac{V_o^2}{R} = P = \frac{V_o V_i}{\omega L}\alpha\left[1 - \frac{\alpha}{\pi}\right];$$

$$or,\quad \boxed{V_o = \frac{V_i R}{\omega L}\alpha\left[1 - \frac{\alpha}{\pi}\right]} \tag{6.3.4}$$

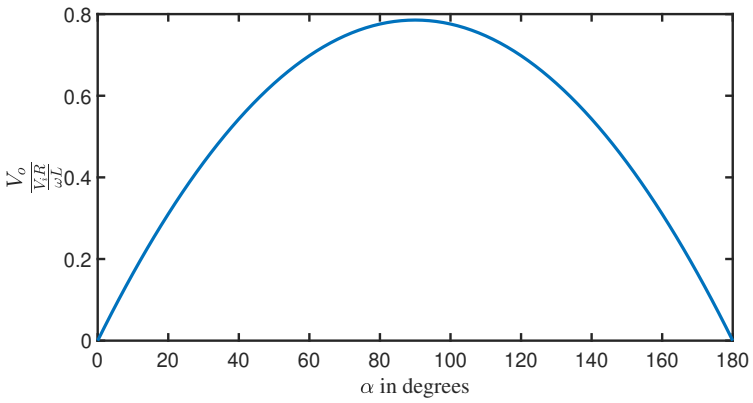


Figure 6.6: Variation of gain with α

The variation of V_o with α is shown in the below graph. As seen above the maximum gain is achieved at $\alpha = \frac{\pi}{2}$ and the maximum gain when $(R = \omega L)$ is $\frac{\pi}{4}$.

6.4 ZVS conditions for DAB

To find the zero crossing (β) in the Fig.6.2 is found by referring to eqn.(6.1.7) that is:

$$i(\theta) = \left[\frac{V_i}{\omega L}(\theta - \frac{\pi}{2}) + \frac{V_o}{\omega L}(\theta + \frac{\pi}{2} - \alpha)\right]\Bigg|_{\beta} = 0;$$

$$or, \qquad V_i(\frac{\pi}{2} - \beta) = V_o(\frac{\pi}{2} + \beta - \alpha);$$

$$or, \qquad V_i\frac{\pi}{2} + V_o(\alpha - \frac{\pi}{2}) = \beta(V_i + V_o);$$

$$or, \qquad \beta = \frac{V_i\frac{\pi}{2} + V_o(\alpha - \frac{\pi}{2})}{V_o + V_i} \tag{6.4.1}$$

For ZVS during turn On of both the bridges as discussed for 1ϕ SRC in the earlier chapter, $0 < \beta < \alpha$, therefore when $(\beta > 0)$;

$$or, \qquad V_i\frac{\pi}{2} + V_o(\alpha - \frac{\pi}{2}) > 0;$$

$$or, \qquad V_o(\alpha - \frac{\pi}{2}) > -V_i\frac{\pi}{2};$$

$$or, \boxed{\alpha > \frac{\pi}{2}(1 - \frac{V_i}{V_o})} \tag{6.4.2}$$

and when $(\beta < \alpha)$;

$$or, \qquad \frac{V_i\frac{\pi}{2} + V_o(\alpha - \frac{\pi}{2})}{V_i + V_o} < \alpha;$$

$$or, \qquad V_i\frac{\pi}{2} + V_o(\alpha - \frac{\pi}{2}) < \alpha(V_i + V_o);$$

$$or, \boxed{\alpha > \frac{\pi}{2}(1 - \frac{V_o}{V_i})} \tag{6.4.3}$$

Hence when the converter is operated in Buck Mode that is $V_o < V_i$, eq.(6.4.3) needs to be satisfied and when operated in Boost Mode that is $V_o > V_i$, eq.(6.4.2) needs to be satisfied.

For example when we want a converter in Buck operation for 1ϕ SRC, the condition for ZVS stands as eq.(5.8)

$$cos\delta < \frac{V_o}{V_i} => \delta < \cos^{-1}\frac{V_o}{V_i}$$

whereas for 1ϕ DAB the ZVS condition stands as

$$\alpha > \frac{\pi}{2}(1 - \frac{V_o}{V_i})$$

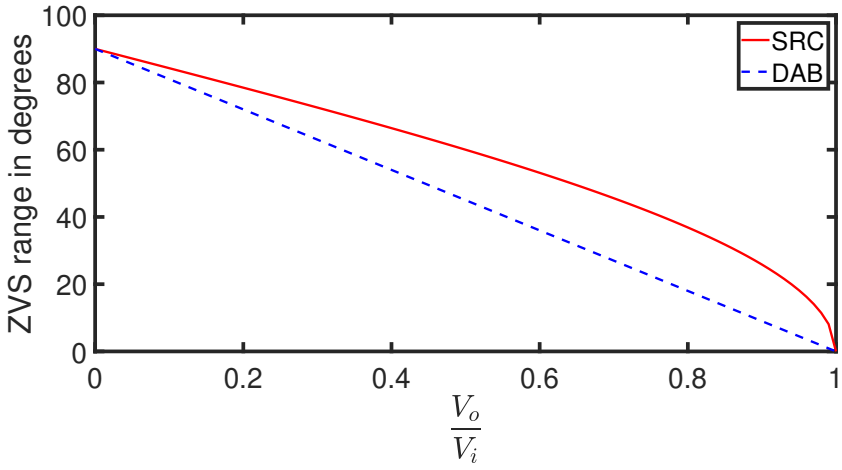


Figure 6.7: ZVS range for Buck Mode in SRC vs DAB

Now for Boost mode for 1ϕ SRC the condition for ZVS stands as eqn.(5.7)

$$cos\delta < \frac{V_i}{V_o} => \delta < \cos^{-1}\frac{V_i}{V_o}$$

whereas for 1ϕ DAB the ZVS condition stands as

$$\alpha > \frac{\pi}{2}(1 - \frac{V_i}{V_o})$$

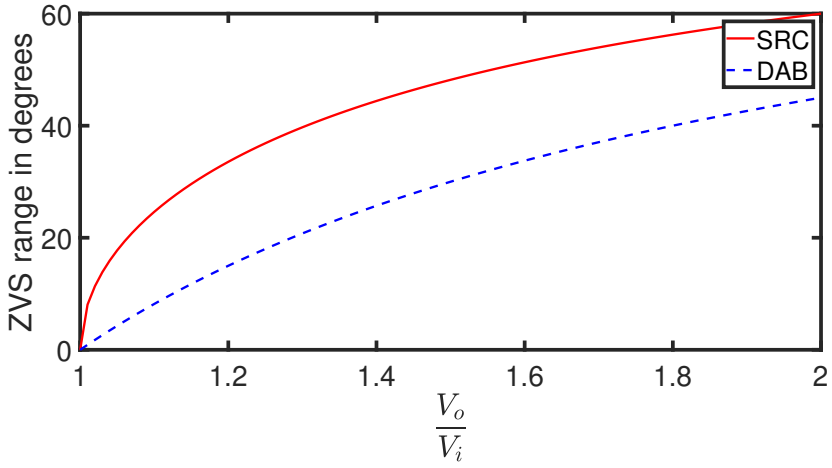


Figure 6.8: ZVS range for Boost Mode in SRC vs DAB

Hence from the above figures it is quite clear that for Boost as well as Buck mode, the DAB offers a better range for ZVS than compared to SRC. This is one of the many advantages offered by a DAB as compared to an SRC which shall be discussed later.

6.5 Simulation of 1ϕ DAB

Here the DAB is designed as $V_i = 60VDC$, $V_o = 28VDC$, $L = 10\mu H$, $L_{lk} = 0.01\mu H$, $L_m = 0.5mH$, $\alpha = 20°$, $R_{loss} = 0.1\Omega$, $R_{load} = 10\Omega$ and $f_s = 100kHz$.

Shown below are the waveforms showing the Input pole voltage, Output pole voltage and primary current of the transformer.

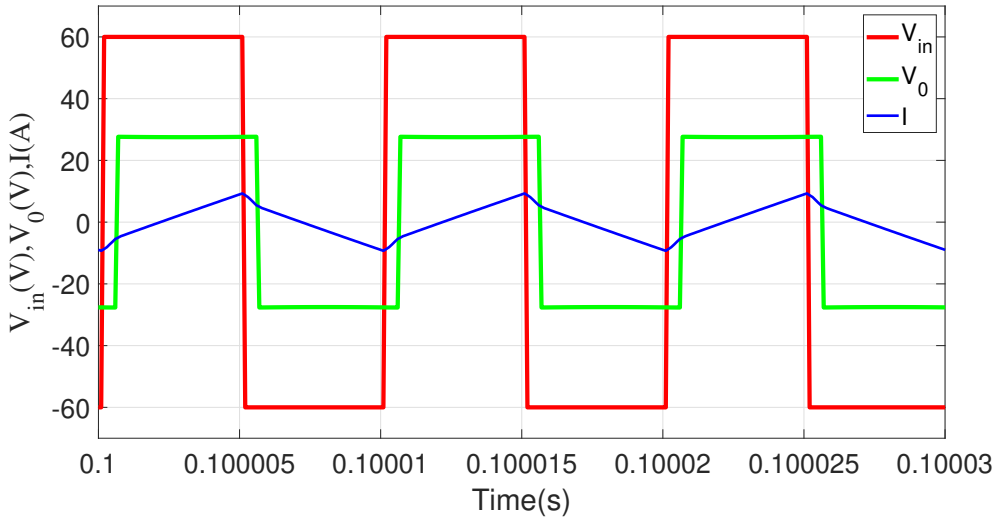


Figure 6.9: Voltages, Current at primary side of 1ϕ DAB *(Scale: Y-axis : 20V/div, X-axis : 5μs/div)*

Shown below are the FFT results of the current waveform, which shall be later compared with the derived results.

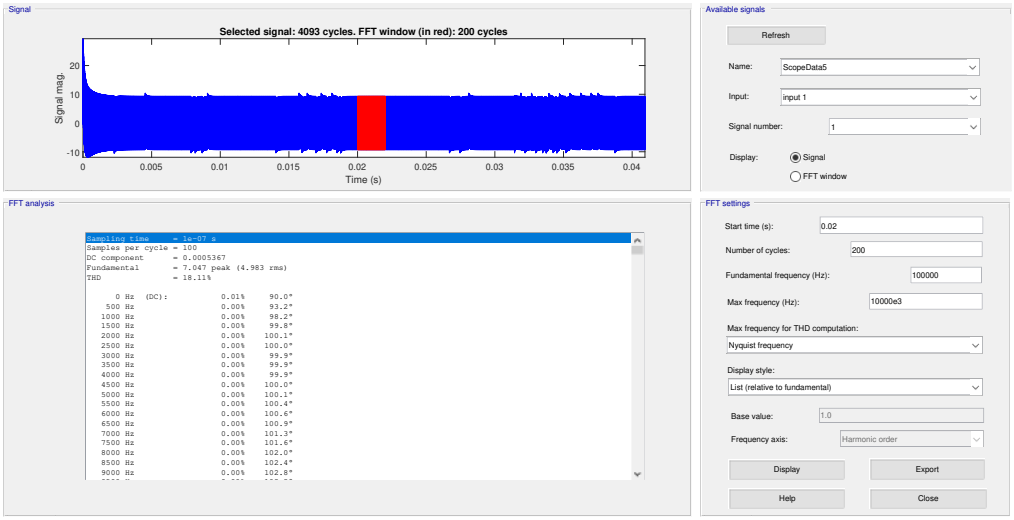


Figure 6.10: FFT analysis of the input side DC current

PARAMETERS	OBSERVED	CALCULATED
I_{rms}	4.991A	5.1008A
I_{1rms}	4.913A	5.0076A
THD	18.36%	19.38%
Gain	0.4683	0.4938

The difference between the observed and the calculated values is due to the reason that the analysis done is for ideal conditions, therefore the observed gain is less than the calculated gain. Due to the included resistance the observed current values are lesser than the calculated current values.

The reason for including series resistance in the converter is intentional, without the series resistances there is an offset in the primary current which results in unexpected output voltages and also results in saturation of the inductor.

6.6 Conclusion

In this chapter a detailed analysis of a 1ϕ DAB has been done, several essential converter parameters have been derived along with Fourier analysis of the current waveform, these derivations have been later verified using simulation results. Conditions for satisfying ZVS for both side bridges have been derived for the DAB and possible conclusions have been made stating the superiority of DAB over SRC. From the given Parameter vs gain/phase shift graphs, one can easily decide upon what should be the gain and the phase shift to maximize some parameter as per the individual's requirements.

Chapter 7

Hardware Organization

In the earlier chapters, the working of SRC and DAB has been clearly explained. So now we would like to develop a prototype of the GaN-based converter. The rating of this H-Bridge module will be 1kW for 50V,20A at the input side. As the rated voltage is 50V the device is selected with a safety factor of 2 on the voltage rating since the voltage waveform undergoes an overshoot if there is hard switching. The device selected is EPC2001C. It is an EGaN FET.

7.1 Device Characteristics

- Continuous $V_{DS} = 100V$
- $Continuous I_D = 36A@25°C$
- $V_{GS_{max}} = 6V \ \ \& \ \ V_{GS_{min}} = -4V$
- $R_{DS_{ON}} = 5.6m\Omega, R_{\theta JC} = 1°C/W$
- $C_{ISS} = 770pF, C_{RSS} = 10pF, C_{OSS} = 430pF$
- $Q_G = 7.5nC$
- Safe Operating Area

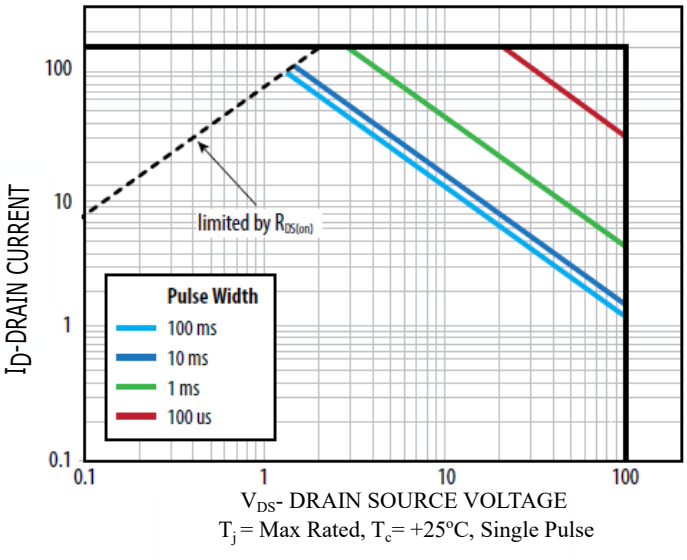


Figure 7.1: SOA

- Package : LGA(Land Grid Array)

  Such a package results in the least parasitic inductances consequently the least $L\frac{di}{dt}$. Here we can see the interleaved drain and source to minimize the leakage inductances. Since the traces are in μm so the current density would be very less to carry the rated current therefore there are 5 pads for drain and similarly 5 pads for source resulting in 5 parallel paths hence increasing the current carrying capability[11].

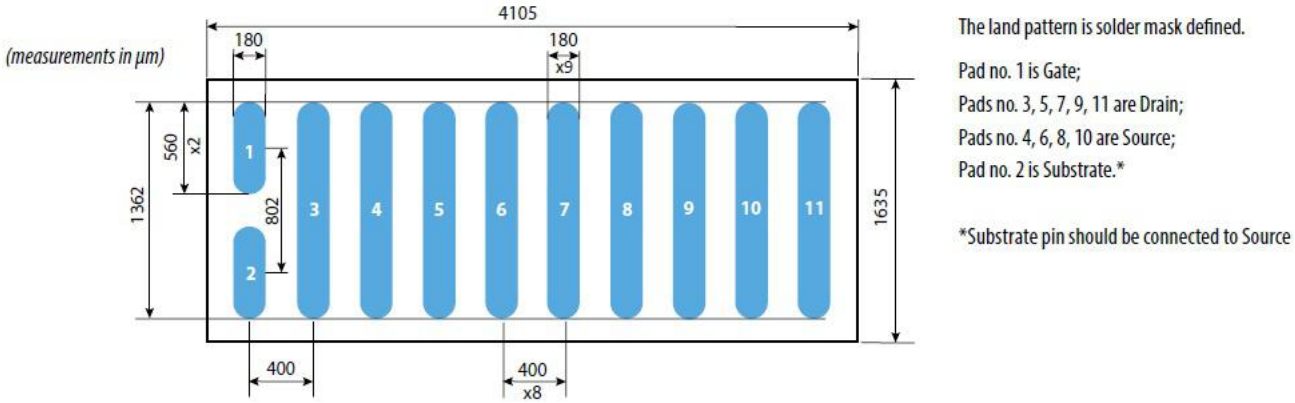


Figure 7.2: LGA Package

7.2 Lt-Spice Simulations

Presented below is a similar EPC2001 model simulated in LTspice to examine the turn On and turn Off at various conditions.

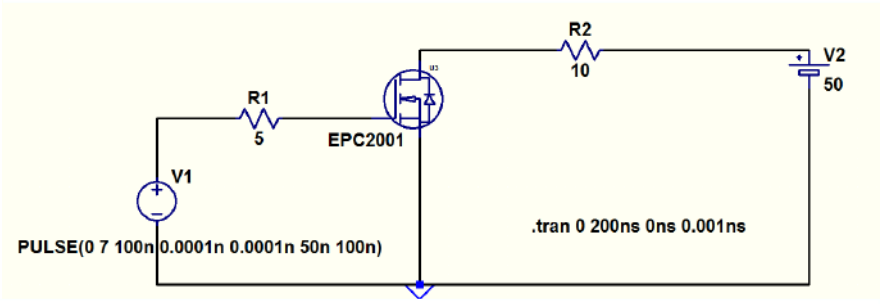


Figure 7.3: LTSpice model for Turn On/Off characteristics

7.2.1 Switching Dynamics with varying V_g

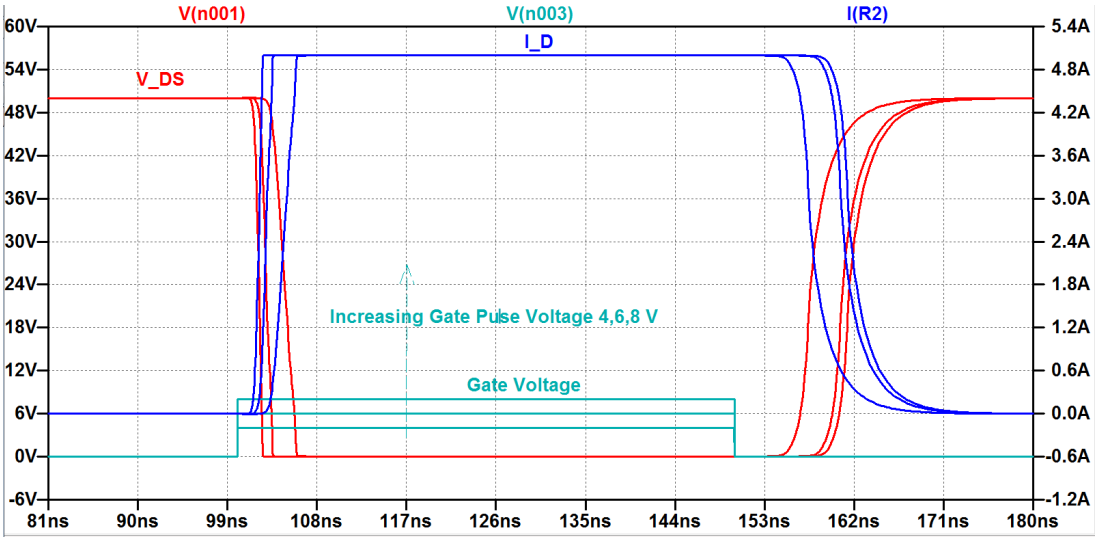


Figure 7.4: Turn On/Off with $V_g = 4, 6,$ and $8V$. *(Scale: Y-axis : 6 V,0.6 A/div, X-axis : 5μs/div)*

As seen in the preceding figure as the gate voltage is increased the turn On/Off is faster as more current is there to quickly charge the device capacitances.

7.2.2 Switching dynamics with varying R_g

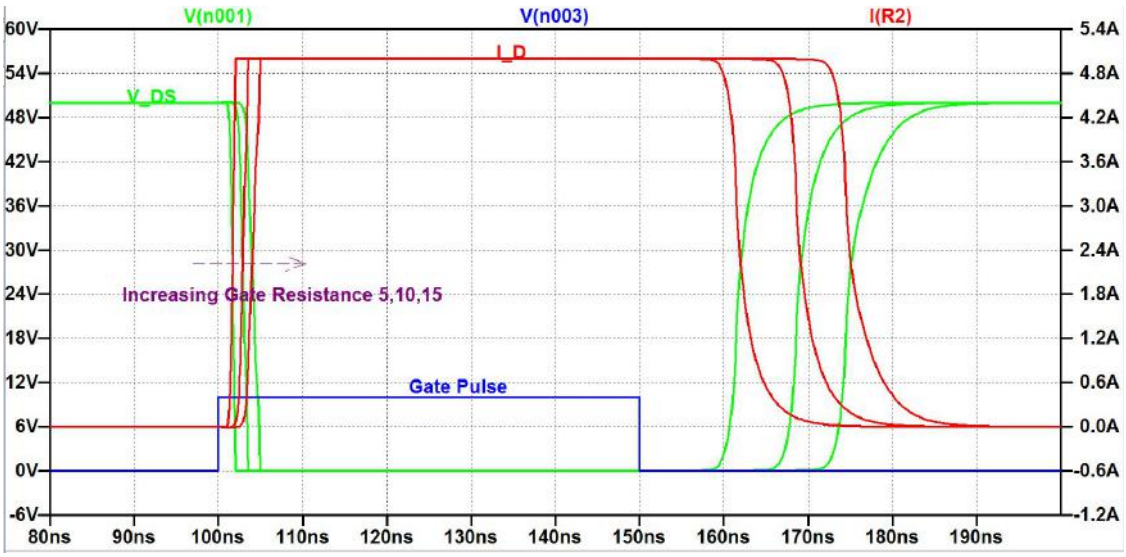


Figure 7.5: Turn On/Off with $R_g = 5, 10,$ and 15Ω *(Scale: Y-axis = 6V,0.6A/div, X-axis : 9ns/div)*

As gate resistance is increased the turn On/Off time increases additionally there is a reduction in the voltage overshoots.

7.2.3 Switching Characteristics with $R_g = 5\Omega$

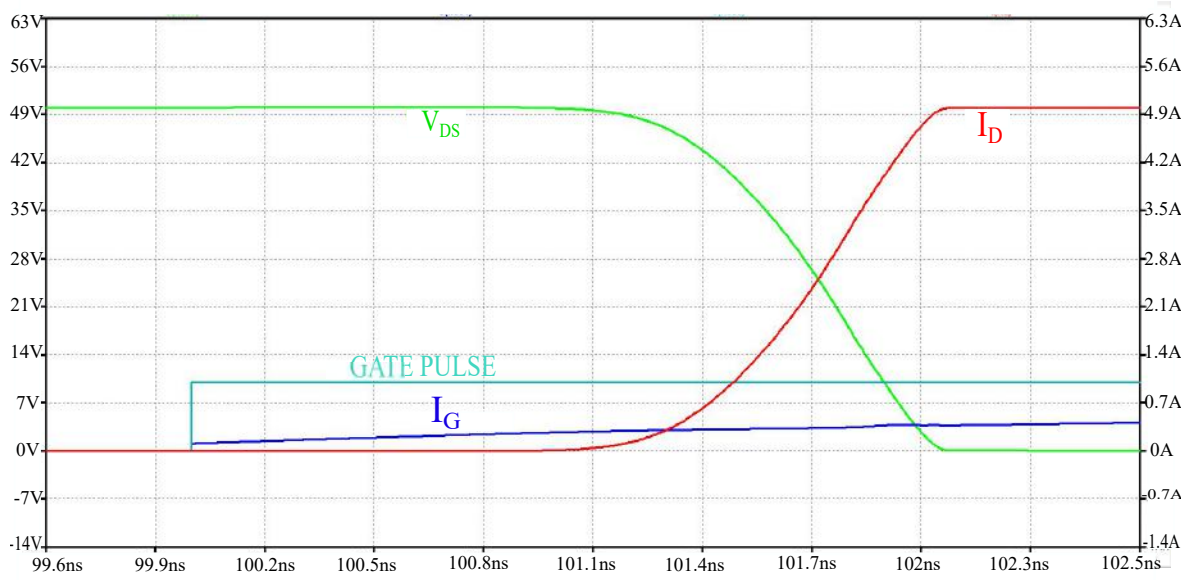


Figure 7.6: Turn On of EPC2001. *(Scale: Y-axis : 2V,0.6 A/div, X-axis : 0.3ns/div)*

Referring to the turn-On process of EPC2001C in the Fig.7.6

Delay Time = 0.91ns, throughout this time there is no change in device current it stays at zero but the V_{GS} keeps on increasing.

On time = (0.636ns+4.45ns), during this period the current rises exponentially in the device and the voltage across the device falls exponentially. During On time there are two waveforms of current rise. that is from (100.914ns to 101.55ns) and (101.55ns to 106ns). This is due to the charging of different capacitances of the GaNFET hence changing the time constant τ therefore the nature of the curve. Unlike a SiC-based FET where the rise of current and the fall of device voltage are distinct in the case of GaNFETs this distinction is difficult.

Hence, Total On Time = 6ns

On state voltage drop($V_{DS_{ON}}$)=27mV.

From the steady state of I_D we see the current rises upto 4.99A, hence the expected $R_{DS_{ON}}$ of the GaNFET can be calculated as $\left(\frac{50-0.027}{4.99} - 10\right) = 14.63m\Omega$. Therefore $R_{DS_{ON}} = 14.63m\Omega$

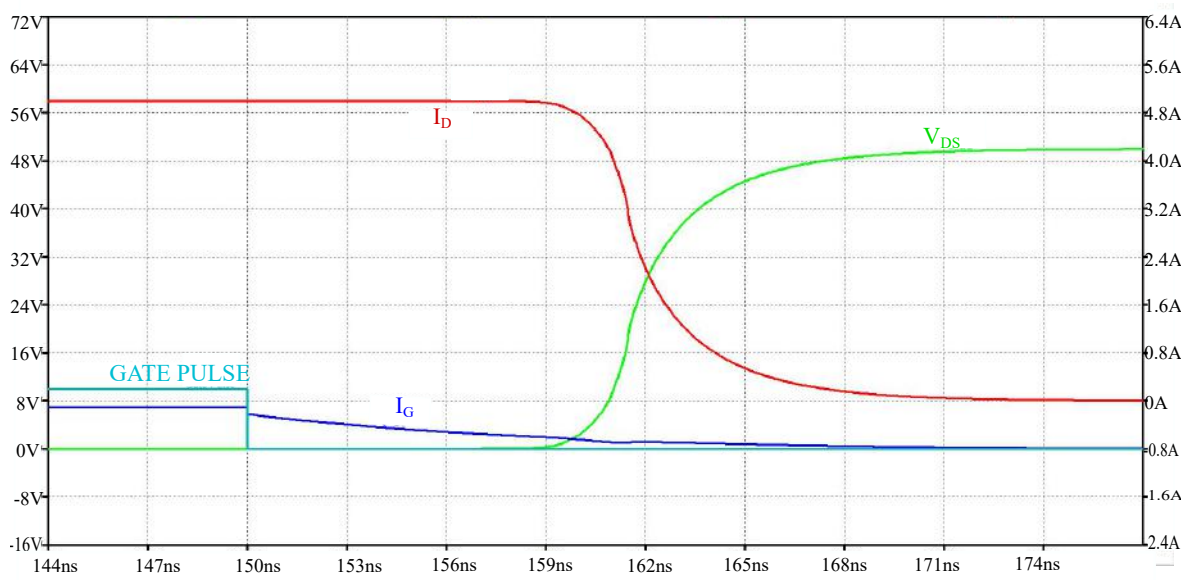


Figure 7.7: Turn Off of EPC2001. *(Scale: Y-axis : 8V,0.8 A/div, X-axis : 3ns/div)*

Likewise referring to the above figure for Turn Off process of EPC2001. Delay Time = 8.29ns, during this time there is no change in device current, current remains at 4.99A.

Off time = (3.918ns+12.792ns). The current falls exponentially in the device and the voltage across the device rises exponentially. During Off time there are two waveforms of current fall. From (158.29ns to 162.208ns) and (162.208ns to 175ns).This is due to the discharging of different capacitances of the GaNFET hence change the time constant τ consequently changing the nature of the curve.

Therefore, Total Off Time = 25ns,

Leakage Current=1.7 mA.

From the above results we infer that if we use $R_g = 5\Omega$, On time required is 6ns and the Off time required is 25ns. Hence a dead time in the earlier discussed H-bridge should be a minimum of 40ns between the complementary pulses to ensure the safety of the devices by preventing a shoot-through fault. So a gate driver should be such chosen that it has the facility of adjustable dead time.

7.3 Gate Driver

As per device recommendation the Gate Driver chosen is LMG1210, this is a

- Half Bridge Gate Driver
- Up to switching frequency of 50-MHz operation
- 10-ns typical propagation delay
- Two control input options
  - Single PWM input with adjustable dead time. In this mode one pulse generated is complement of the other.
  - Independent input mode. In this mode the two PWM's generated are independent of each other.
- 1.5-A peak source and 3-A peak sink currents
- Internal LDO for adaptability to voltage rails
- Internal Capacitive isolation
- Bootstrapping facility for the upper device
- High CMTI of 300-V/ns
- UVLO and over-temperature protection
- Low-inductance WQFN package
- Adjustable dead-time
- HO to LO capacitance less than 1 pF
- 3ns to 4ns high-side to low-side matching

7.3.1 Internal Circuitry of the Gate Driver

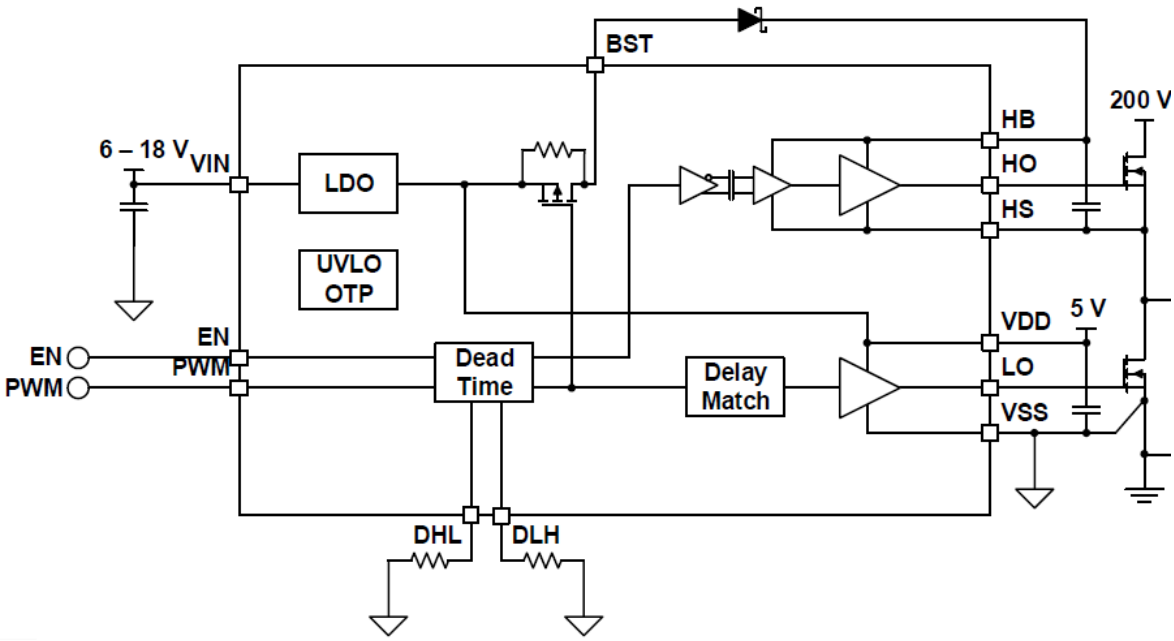


Figure 7.8: Circuit Diagram of LMG1210

7.3.2 Package of the Gate Driver

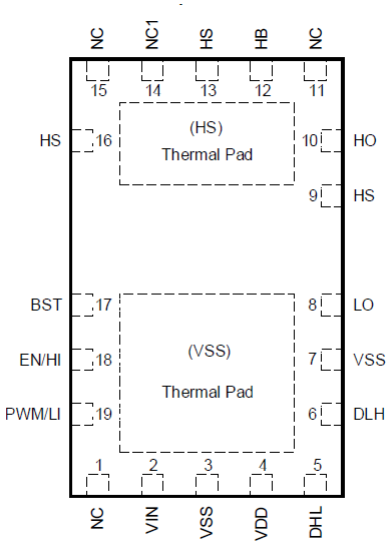


Figure 7.9: WQFN Package of LMG1210

7.4 Making of the 1ϕ Full Bridge PCB Layout

Following are some of the considerations for designing the PCB layout[11].

1. It is recommended to go for a minimum of 4layer PCB.
2. Since parasitics have a lot of impact in the performance of the GaN devices, so care must be taken to minimize these parasitics,
    - The gate driver is placed as close as possible to the eGaN FETs
    - The decoupling/filtering capacitors for the gate driver are placed as close as possible to the Gate Driver.
    - DC Bus needs to be sandwiched to reduce the leakage inductances.
3. To reduce the loop size and enhance magnetic self cancellation it is advisable to put traces onto the adjacent layers by the help of vias.

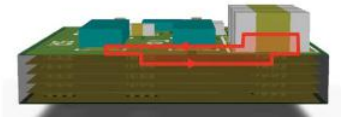


Figure 7.10: Reduced power loop in PCB

4. It is advisable to do an ENIG finish instead of the conventional HASL finish, as HASL finish results in bumpy solder pads which might result in shorting of the adjacent pads while the solder flux is put during reflow soldering, whereas ENIG finishing is a smooth bump-less finish that is suitable for fine pitch IC's.
5. It is recommended to use copper thickness of 1-2oz for all the layers.
6. Fiducials are important for component registration during the placement process of assembly.
7. Open silk-screen is recommended for proper rinsing during the reflow process of soldering for fine pitch IC's

7.5 1ϕ Full Bridge PCB

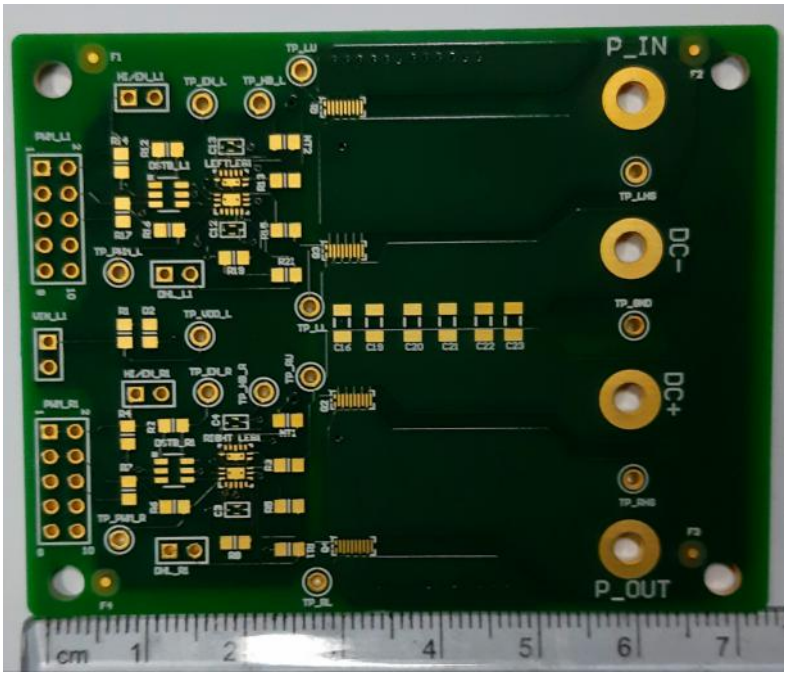


Figure 7.11: PCB top

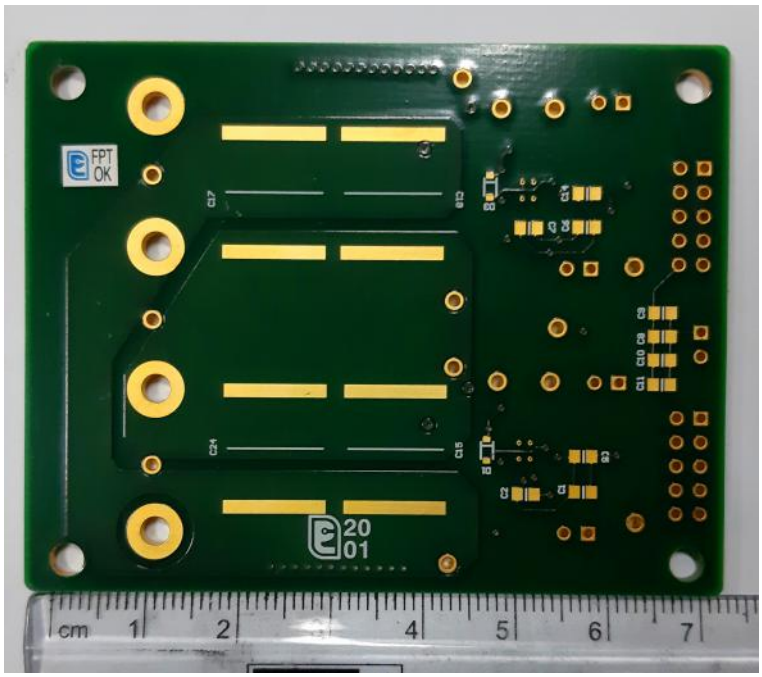


Figure 7.12: PCB bottom

Above shown are the top and the bottom view of the developed Single Phase Full Bridge prototype. Net board size is around $7cm \times 5cm$.

7.6 Conclusion

In this Chapter, a vivid discussion has been done on the hardware aspect of the 1ϕ Full-Bridge/H-Bridge prototype to be built using GaN devices. The used device has been first simulated in LTspice and its switching characteristics have been observed. The important properties of the chosen gate driver have been mentioned and finally, the development of the full-bridge PCB layout has been distinctly explained.

Chapter 8

Hardware Results

8.1 Inverter Mode with Inductive Load

A simple test to check the proper functioning of the developed board is operating the Full Bridge module as an inverter. Since we are going to switch at high f_s so arranging a load resistor for such high frequencies is difficult. So we perform the inverter test with an air-core inductor as the load. Shown below is the test setup:

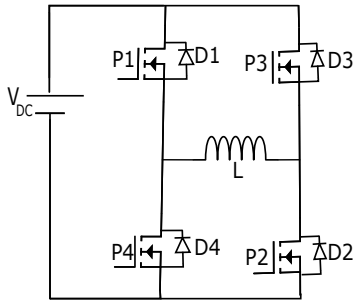


Figure 8.1: Inverter with Inductive Load

The inductor current waveform looks like:

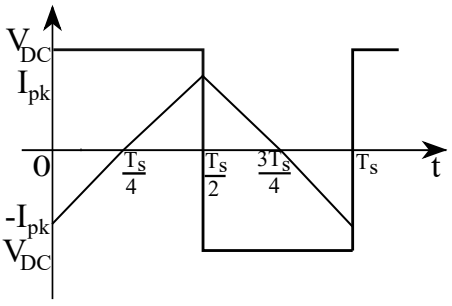


Figure 8.2: Pole Voltage, Current

From the above figure $V_{DC} = L\frac{di}{dt}$ where dt will be $\frac{T_s}{4}$. Hence, $I_{pk} = \frac{V_{DC}\frac{T_s}{4}}{L}$ and $I_{rms} = \frac{I_{pk}}{\sqrt{3}}$. Soon, this test shall be performed at various switching frequencies to ensure the proper functioning of the device and the developed PCB.

A dead time of 20ns is given between each complementary pair and R_g is chosen as 5Ω.

8.1.1 Test Results at 400kHz

Here $V_{DC} = 20V$, $L = 2.5\mu H$ therefore $I_{pk} = 5A$, $I_{rms} = 2.9A$

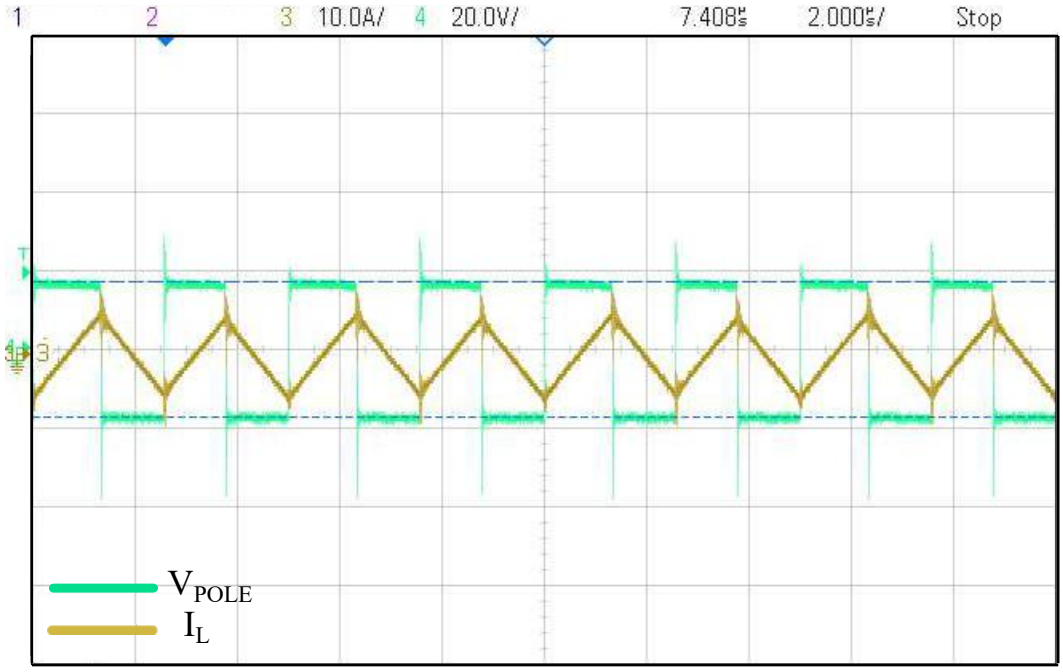


Figure 8.3: Pole Voltage, I_L *(Scale: Y-axis : 20V,10A/div, X-axis : 2µs/div)*

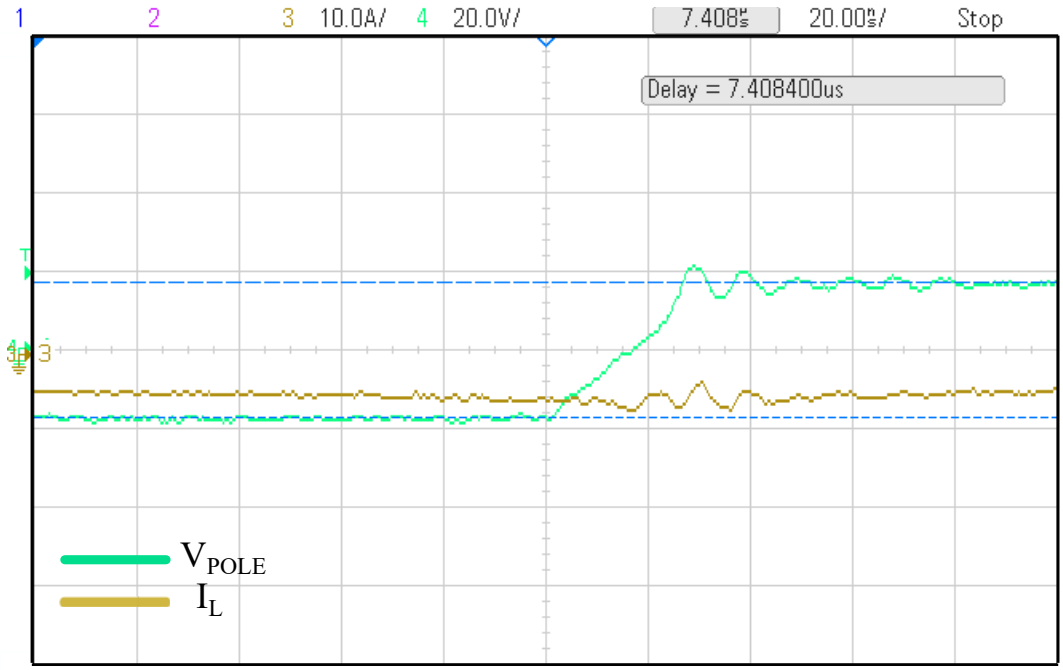


Figure 8.4: P2P4 Off *(Scale: Y-axis : 20 V,10A/div, X-axis : 20ns/div)*

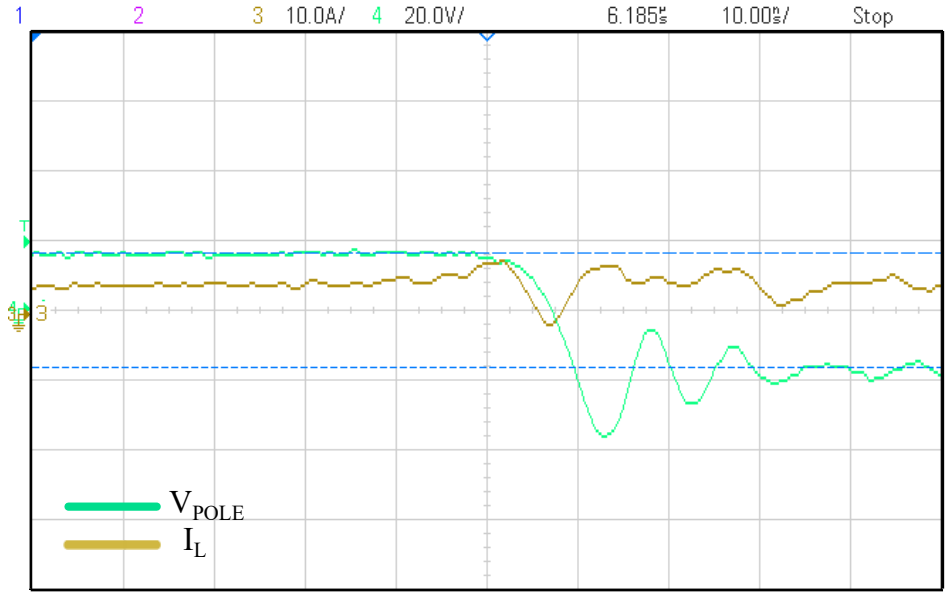


Figure 8.5: P1P2 Off. *(Scale: Y-axis : 20V,10A/div, X-axis : 10ns/div)*

In Fig.8.4, the overshoot during P3P4 turn Off and D1D2 turn On is around 5V. Whereas in Fig.8.5, we observe that the overshoot during P1P2 turn Off and D3D4 turn On is around 18V.

8.1.2 Test Results at 800kHz

Here $V_{DC} = 30V$, $L = 1.9\mu H$ therefore $I_{pk} = 5A$, $I_{rms} = 2.8A$

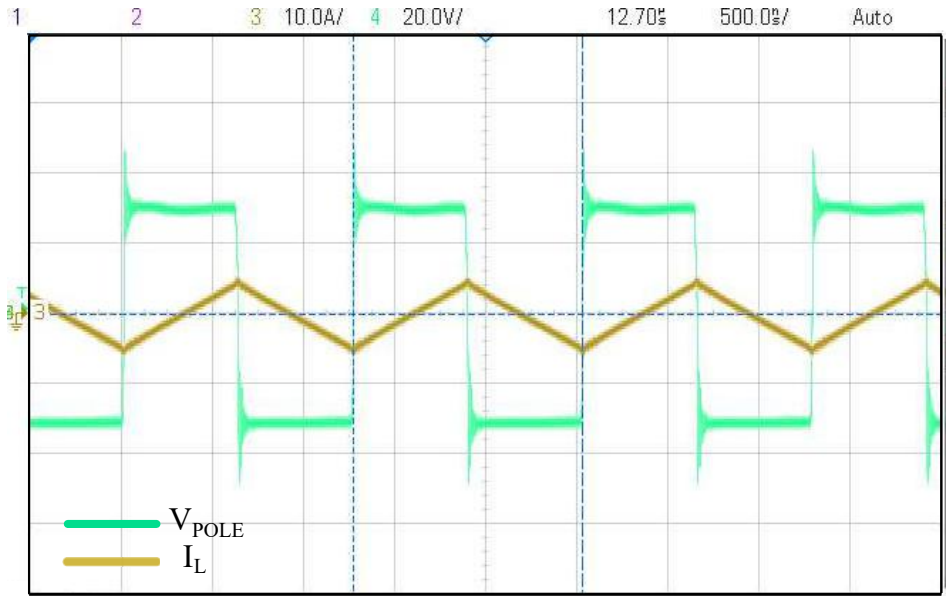


Figure 8.6: Pole Voltage, I_L *(Scale: Y-axis : 20V,10A/div, X-axis : 500ns/div)*

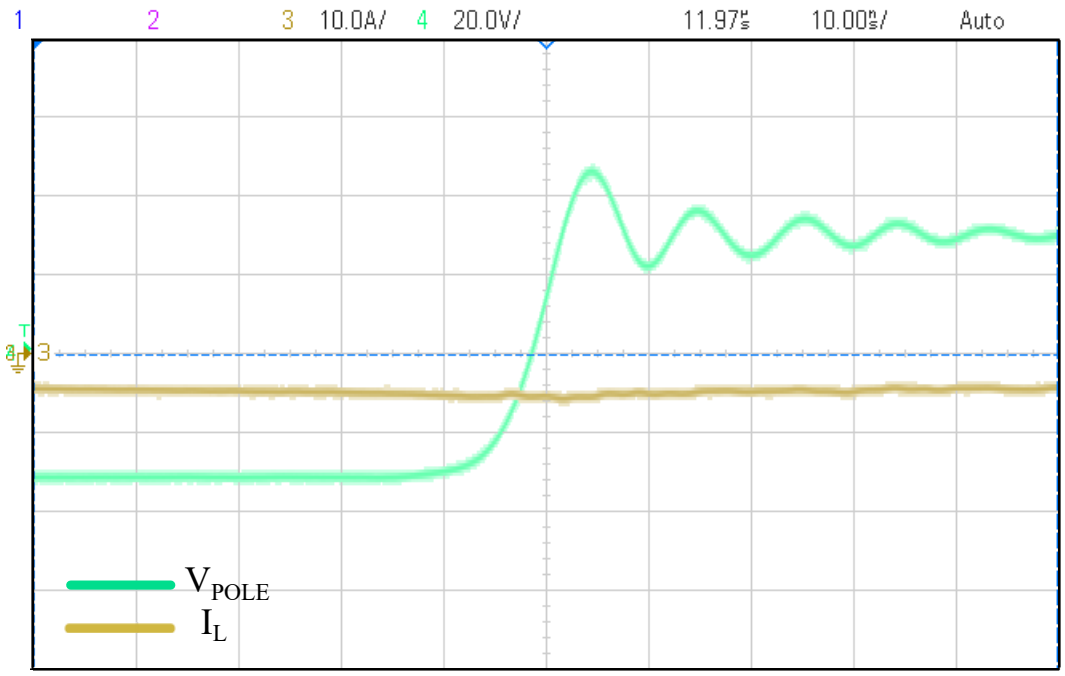


Figure 8.7: P3P4 Off *(Scale: Y-axis : 10V/div , X-axis : 20ns/div)*

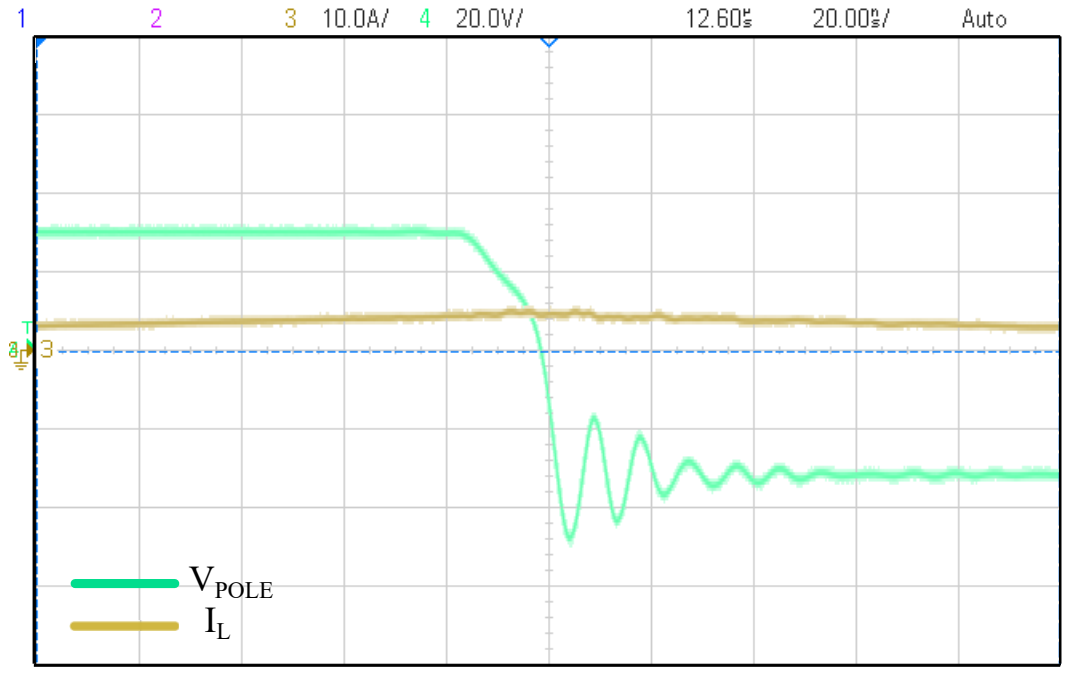


Figure 8.8: P1P2 Off. *(Scale: Y-axis : 20V,10A/div, X-axis : 20ns/div)*

In Fig.8.7, the overshoot during P3P4 turn Off and D1D2 turn On is around 18V. Whereas in Fig.8.8, we observe that the overshoot during P1P2 turn Off and D3D4 turn On is also around 18V.

8.1.3 Test Results at 1MHz

Here $V_{DC} = 28V$, $L = 1.9\mu H$ therefore $I_{pk} = 3.7A$, $I_{rms} = 2.2A$

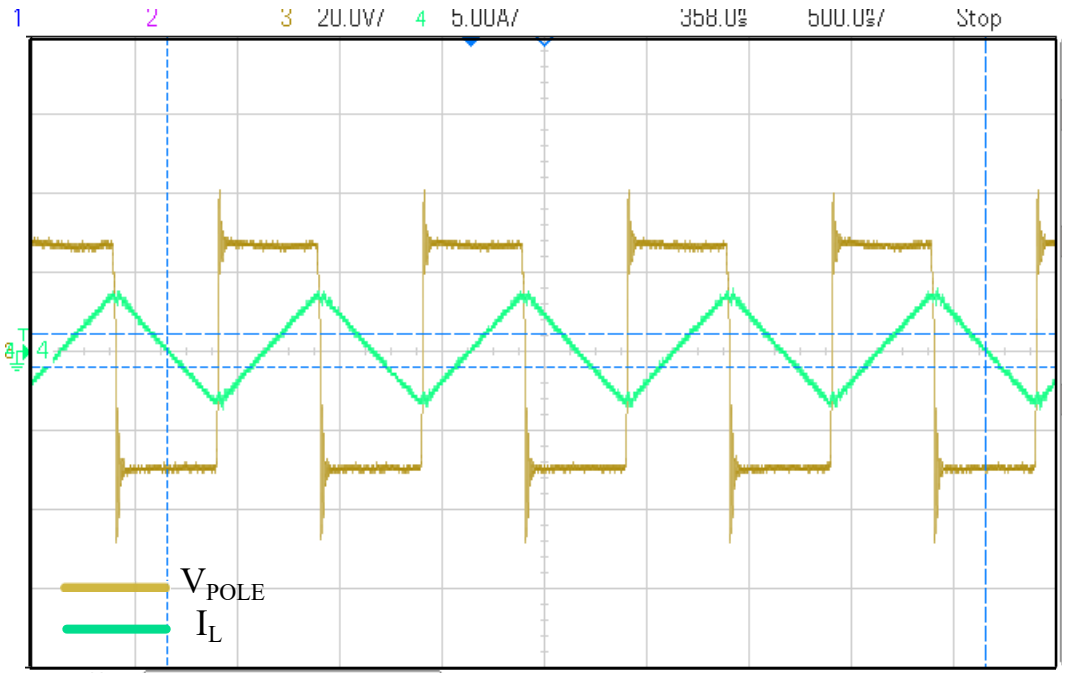


Figure 8.9: Pole Voltage,I_L *(Scale: Y-axis : 20V,5A/div, X-axis : 500ns/div)*

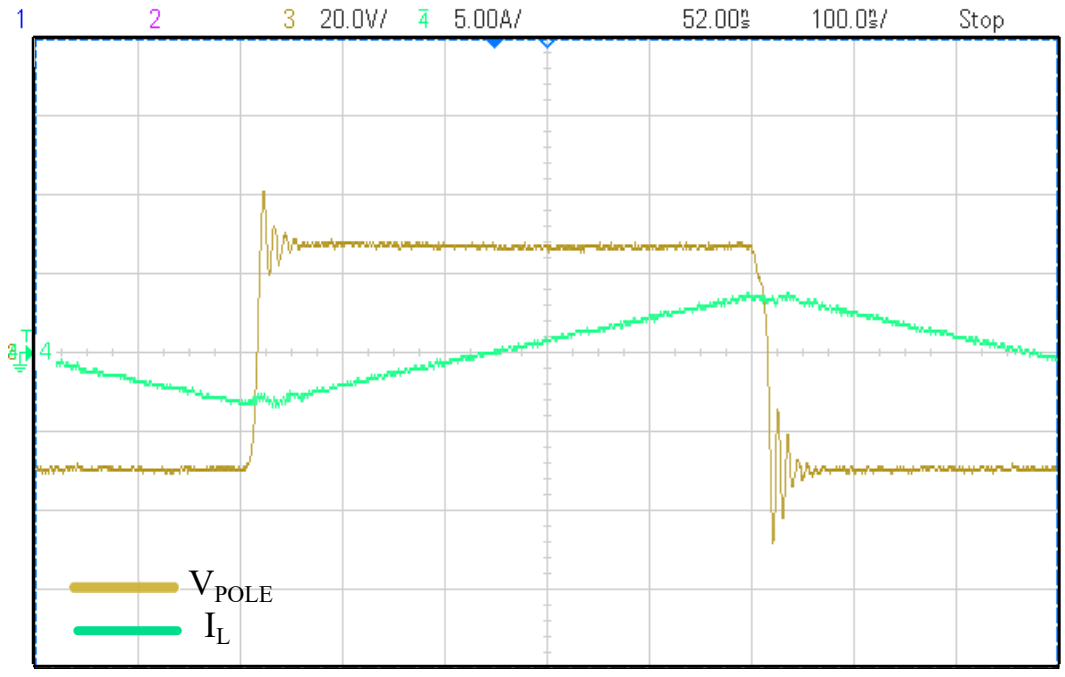


Figure 8.10: P3P4 off *(Scale: Y-axis : 10 V/div, X-axis : 20ns/div)*

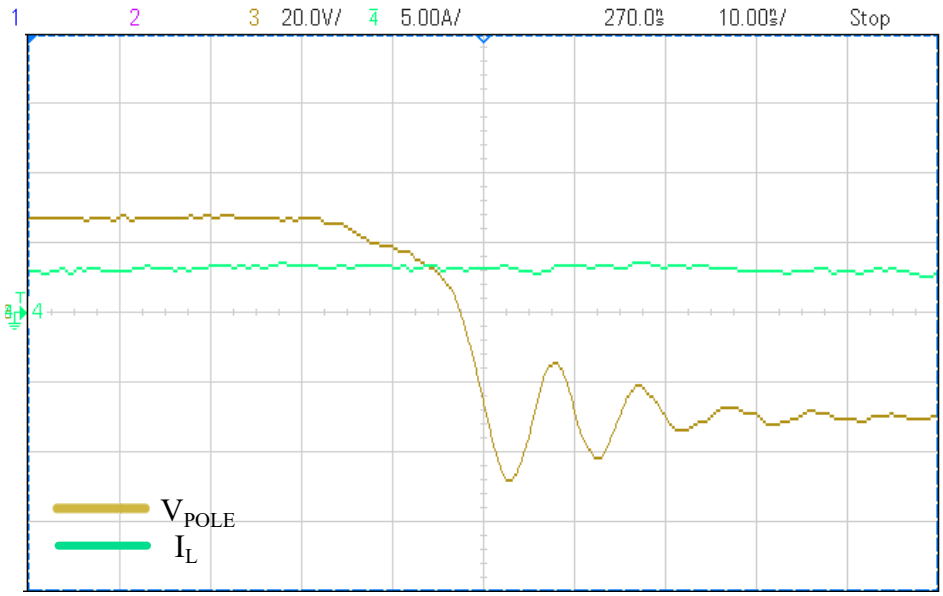


Figure 8.11: P1P2 Off. *(Scale: Y-axis : 10 V/div, X-axis : 20ns/div)*

In Fig.8.10, the overshoot during P3P4 turn Off and D1D2 turn On is around 12V. Whereas in Fig.8.11, we observe that the overshoot during P1P2 turn Off and D3D4 turn On is around 16V.

The overshoots observed are primarily due to the hard turn Off of the switches.

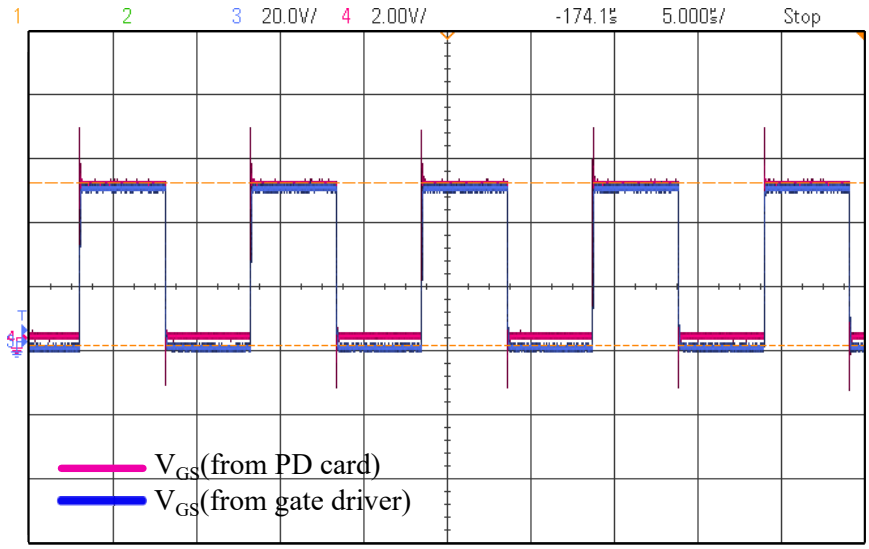


Figure 8.12: Gate Pulse(in blue) *(Scale: Y-axis : 2 V/div, X-axis : 5µs/div)*

Above shown is the gate pulse given to the bottom side GaNFET, here we observe overshoots in the V_{GS} which further deteriorates the voltage waveforms by injecting additional overshoots that has been discussed later.

Observed overshoots are not only due to the gate loop layout inductance but are also contributed by the overshoots in the gate pulses from the Protection and Delay(PD) card. In the earlier figure, it is observed that at no load the V_{GS}(in pink) has overshoots above 1.5V. Hence the proper functioning of the Control Card generating the PWM signals should be ensured without any overshoots. Dual Schmitt Trigger Buffer has been used in the gate driver section to arrest the overshoots. Proper choice of R and C is required in the PD card section to make the signals critically damped rather than under-damped to prevent such overshoots since $V_{GS_{max}}$ is limited to 6V. The threshold for the V_{GS} being 2.5V, one feasible option is to decrease the operating V_{GS} to 3.5V-4V to get a better buffer for V_{GS}.

Hence from the preceding inductive load tests, it is obvious that GaNFETs can function properly at 1MHz. So with a proper design that is by reducing the parasitic layout inductance, one can certainly bring down such overshoots. While performing the above tests the temperature of the GaNFETS too was monitored, it remained close to $40°C$ hence stating that the losses in the device are very less when the RMS current flowing in it is around 3A. So it can be inferred that for low power converters with RMS current within 5-6A there is no need of natural/forced cooling as the losses in the GaNFETs are too less hence making the device a perfect choice for developing a high power density converter. It is to be noted, when performing inverter mode with inductive load test as the switching frequency is increased the overshoots during hard turn off of the device keeps on increasing. This can be eliminated by designing the PCB with a lower layout inductance that shall be discussed later and also by using smaller packages of the elements used so as to reduce the parasitic inductances. As for now in the upcoming section, a better analysis shall be done on the switching performance of the GaNFET by performing DPT.

8.2 Double Pulse Test

The tests in the above section helped in examining the device performance during soft turn On and hard turn Off. To understand the switching dynamics at all the possible conditions like soft turn On/Off, hard turn On/Off at rated device currents, DPT is performed.

The DPT is performed on the Right Leg Lower Switch and the turn On and turn Off characteristics have been observed whereas the right side top switch has an inductor connected across it. When a pulse is given to the bottom switch the current starts to increase through the inductor and when the device is turned off, the current free-wheels through the top switch's body diode. In this test two pulses of varying width are given to the DUT so as to test the behaviour of device under various load currents.

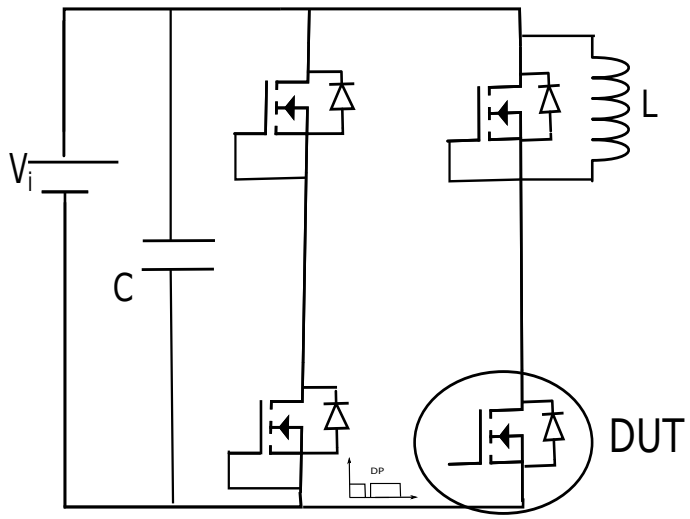


Figure 8.13: Double Pulse Test Setup, DP- Double Pulse for Q4-DUT

Here C represents the film capacitor present on the PCB and not the electrolytic capacitor present across the rectifier output since the pulses will be in the order of nano-seconds and hence the capacitors should be fast reacting so of a lower ESL hence the film capacitors. Other than the DUT all the other devices have been turned Off.

8.3 Double Pulse Test Results

8.3.1 Test at $R_g = 5\Omega$

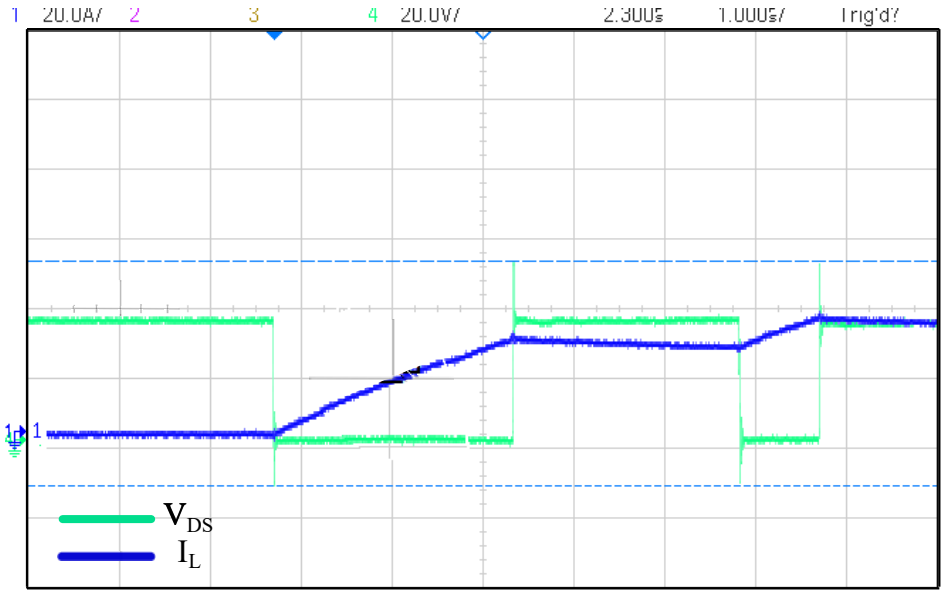


Figure 8.14: V_{DS}, I_L *(Scale: Y-axis : 20V,20A/div, X-axis : 1µs/div)*

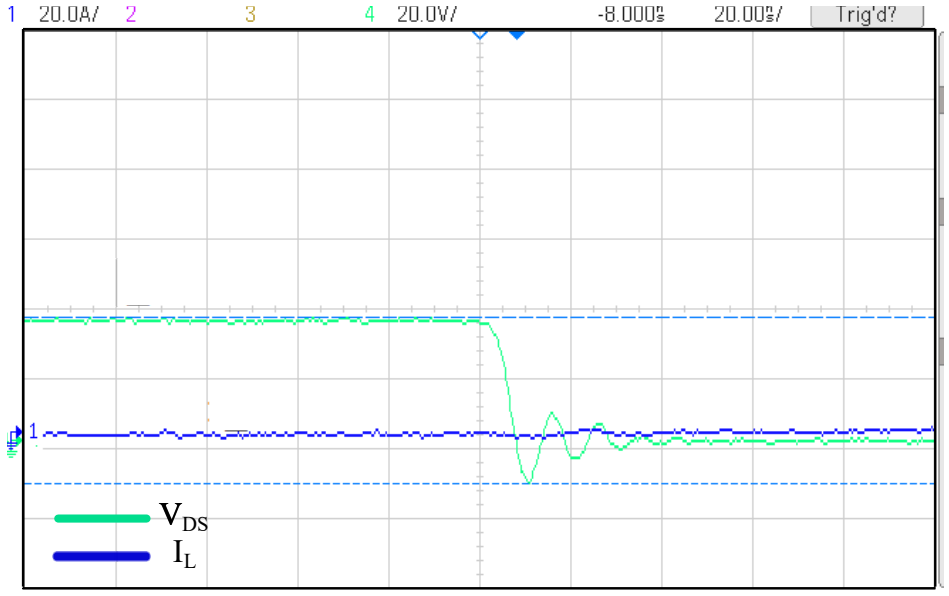


Figure 8.15: V_{DS}, I_L,first turn ON *(Scale: Y-axis : 20 V,20A/div, X-axis : 20ns/div)*

As observed in the preceding results we are plotting V_{DS} and the current through the inductor I_L. Since in the developed board there is no provision to measure the device current I_D and the gate-source measurement loop being quite large gives false V_{GS}. So we cannot exactly differentiate between the various stages while switching of the device but can approximately tell the On/Off time.

For the first turn On (Fig.8.15) it is a Zero Current switching. The On time can be approximated to be around *7.5ns*. The observed overshoot in the V_{DS} is of 12V.

During the period of the first pulse, the DUT is ON and the current builds up in the inductor as per the relation

$$V = L\frac{di}{dt}$$

Hence,

$$\int_0^I di = \int_0^{T_1} \frac{V}{L} dt$$

with the inductor of $3.12\mu H$, $V = V_i = 35V$ the duration of the first pulse(T_1) being $3.12\mu s$, the inductor current builds upto 28A in the first period.

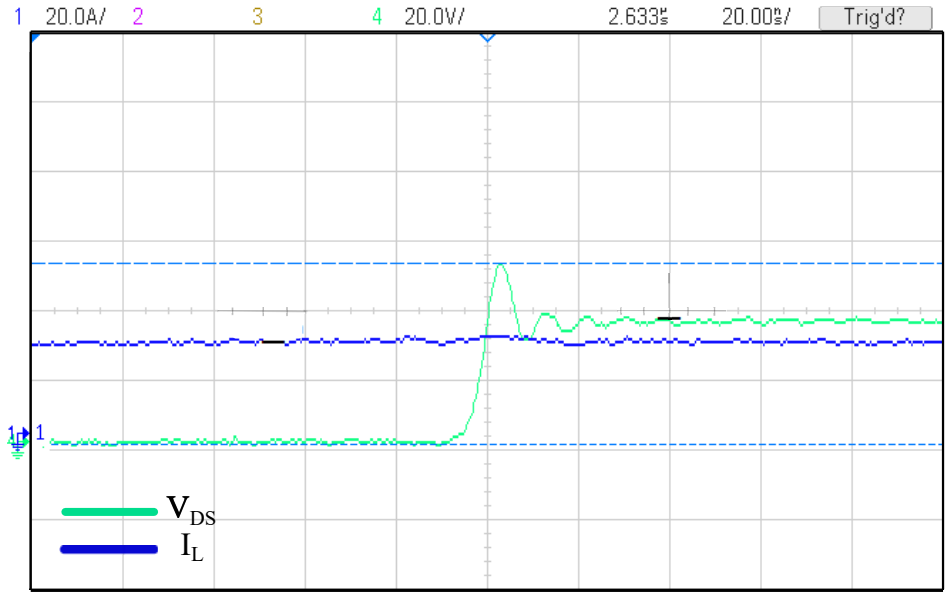


Figure 8.16: V_{DS}, I_L 28A hard turn Off *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

The above result is the first turn Off of the device and now it is a hard turn Off at at 28A and the observed overshoot in V_{DS} is around 17V which is greater than that of the Zero Current switching at the initial stage. The Off time can be approximated to be *10ns*.

In the forthcoming period (when the DUT is Off), ideally the current in the inductor, I_L should remain constant while it freewheels through the body diode of the above switch since the inductor is considered to be lossless. But in practice the inductor built is never lossless and the forward voltage drop of the body diode would decay the current I_L. Therefore, I_L decays to 25.6A from 28A.

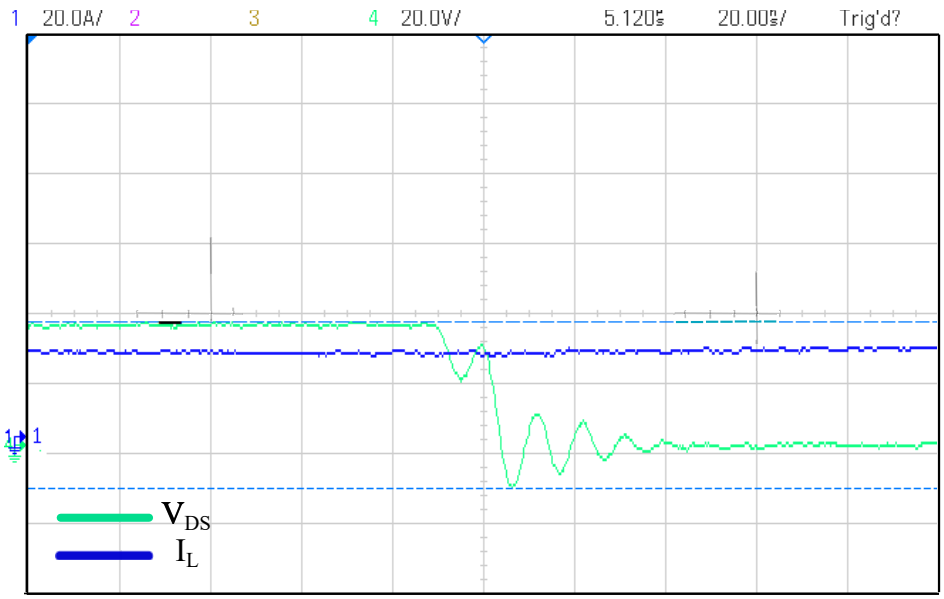


Figure 8.17: V_{DS}, I_L 26A hard turn On *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

At this time the DUT is again turned ON, but now it is a hard turn ON at 25.6A. During this period as earlier shown

$$V = L\frac{di}{dt}$$

hence

$$\int_{25.6}^{I} di = \int_{0}^{T_2} \frac{V}{L} dt$$

The width of the second On pulse T_2 being $1\mu s$ and L as earlier mentioned is $3.12\mu H$. I builds upto around 36A which is the rated continuous current carrying capability of the device. The turn On time of the device can be approximated to be about *12.5ns*. Hence it can be inferred that as the device current is increased the turn On time increased by 5ns whereas the voltage overshoot of 12V remains the same when the device was turned On with zero current in it.

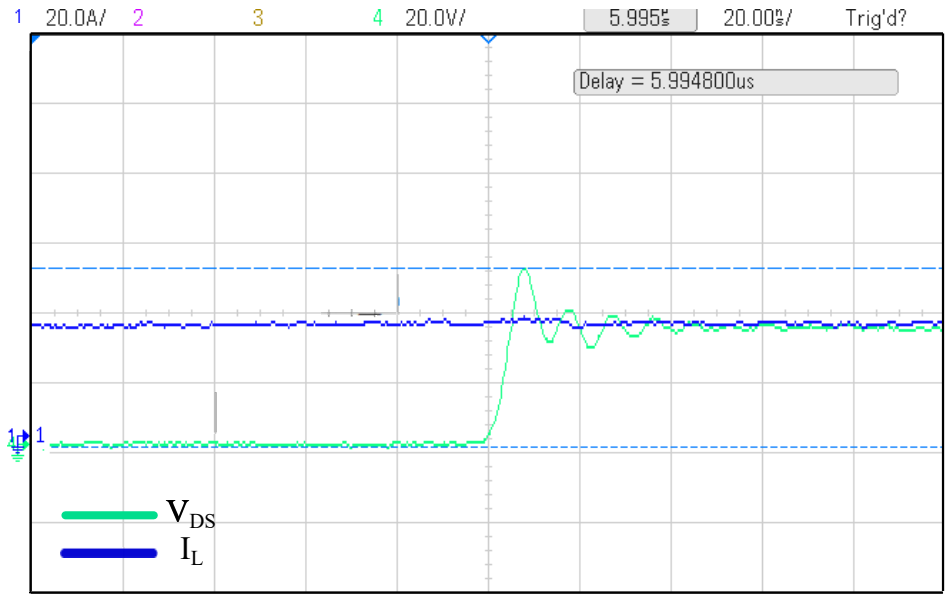


Figure 8.18: V_{DS}, I_L 34.4A hard turn OFF *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

Similarly when the device is turned Off at $I_L = 36.4A$ leading to a hard turn Off resulting in an overshoot of 16V and the time required to turn OFF can be approximated as *5ns*.

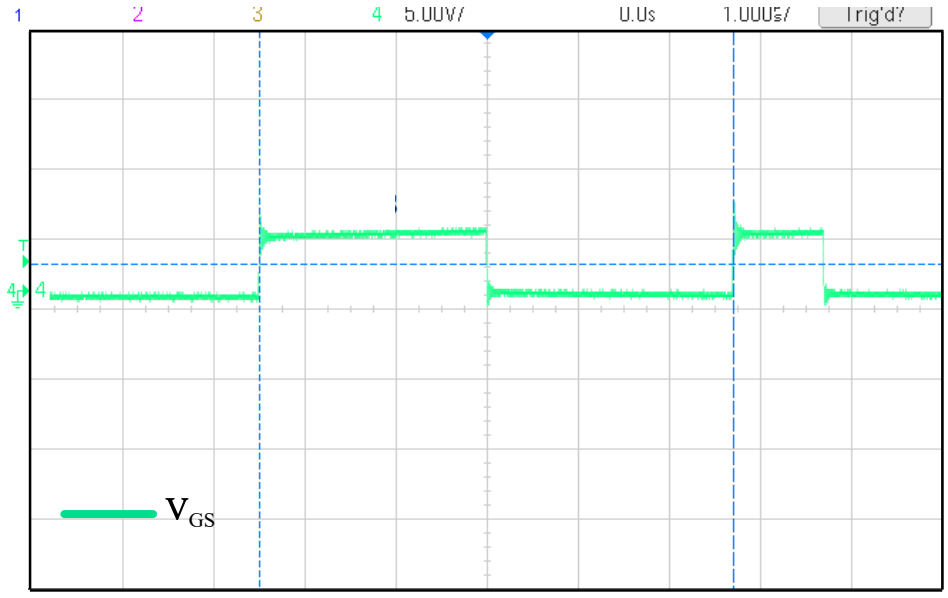


Figure 8.19: V_{GS} *(Scale: Y-axis : 5V/div, X-axis :* $1\mu s$*/div)*

Shown above is the gate to Source voltage of the DUT at no load current.

8.3.2 Test at $R_g = 3.3\Omega$

To understand the affect of reducing R_g, we shall be decreasing the R_g to 3.3Ω and performing the DPT.

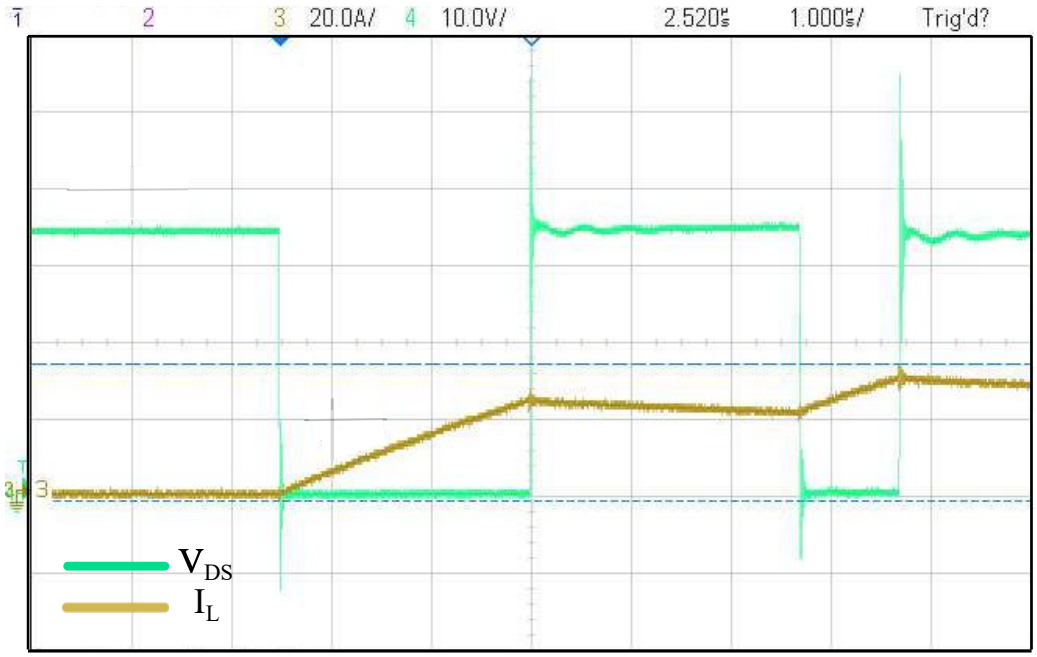


Figure 8.20: V_{DS}, I_L *(Scale: Y-axis : 10V,20A/div, X-axis : 1µs/div)*

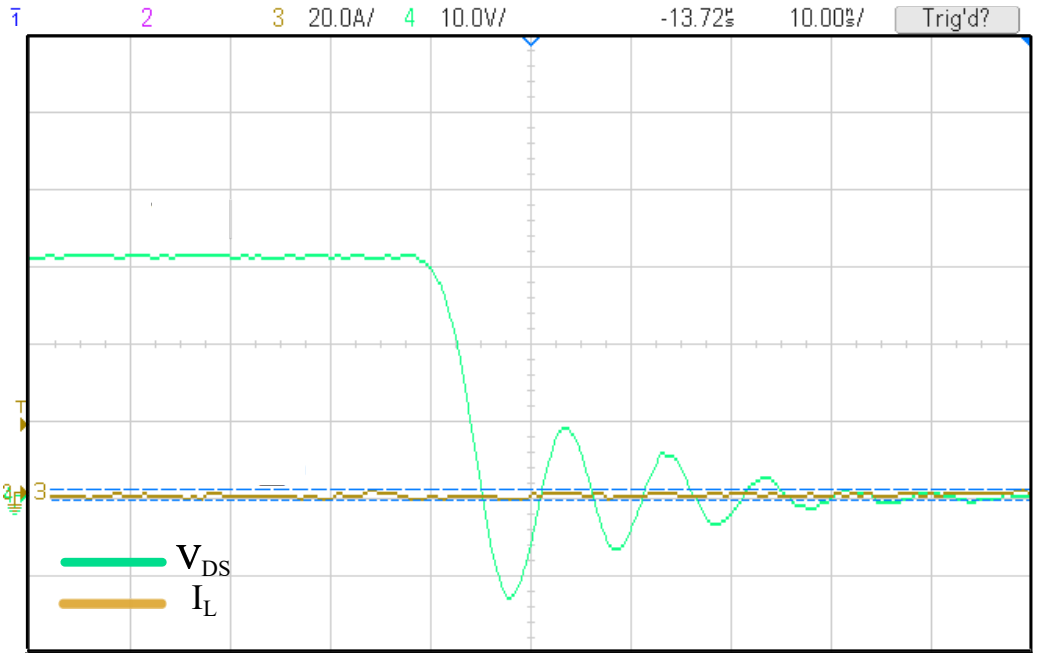


Figure 8.21: V_{DS}, I_L,first turn On *(Scale: Y-axis : 20V,20A/div, X-axis : 10ns/div)*

Here since the R_g is reduced, the overshoots in the device voltage shall increase, therefore now the DPT is performed at 32V DC instead of 35V as in earlier case.

As observed in Fig.8.21, for the first turn On it is a Zero Current switching and the On time can be approximated to be *5ns*. The observed overshoot in the V_{DS} is of 14V.

During the period of the first pulse (when the DUT is ON), the current builds up in the inductor as per the relation

$$V = L\frac{di}{dt}$$

Hence,

$$\int_0^I di = \int_0^{T_1} \frac{V}{L} dt$$

with the inductor of $3.12\mu H$, $V = V_i = 32V$ the duration of the first pulse(T_1) being $2.5\mu s$, the inductor current builds up to 24A in the first period.

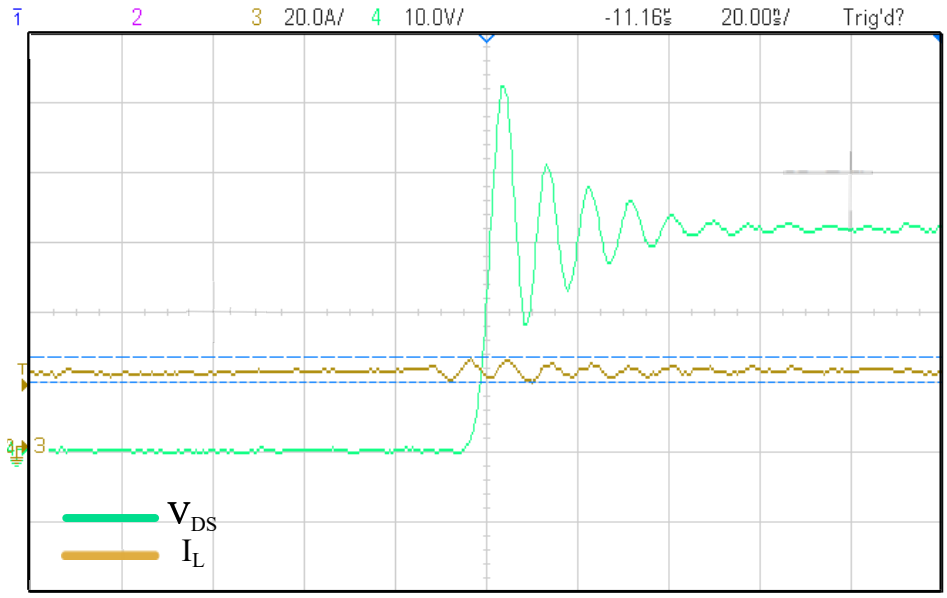


Figure 8.22: V_{DS}, I_L 24A hard turn Off *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

The observed turn Off time can be approximated to be *5ns* and the overshoot is of 17V at 24A hard turn Off with current ripple(pk-pk) of 7A. The time of crossing of I_L and V_{Ds} is the settling time of V_{DS} which is around 46ns.

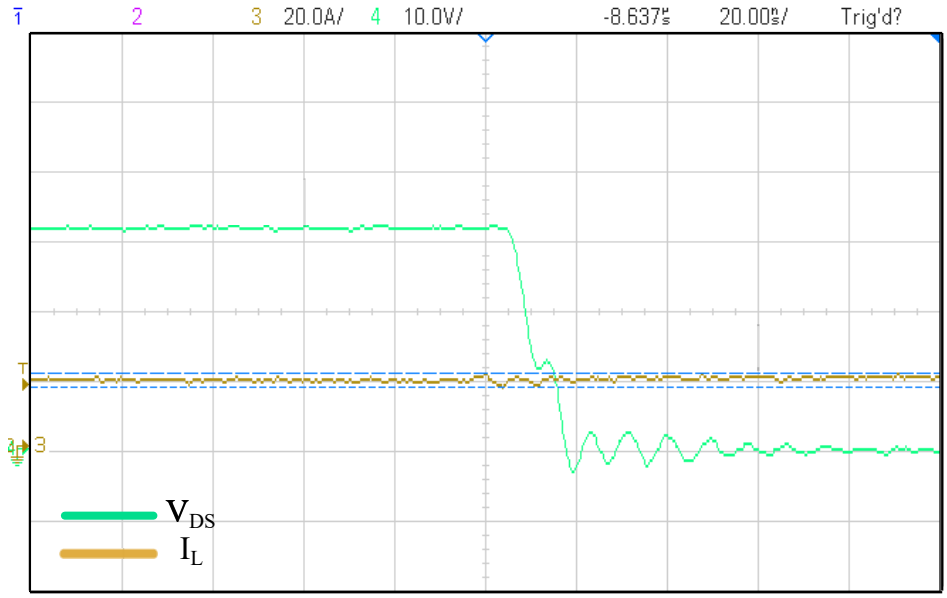


Figure 8.23: V_{DS}, I_L 22A hard turn On *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

From the above result, the observed turn On time can be approximated to be *12.5ns* and the overshoot is of 1.5V at 22A hard turn On.

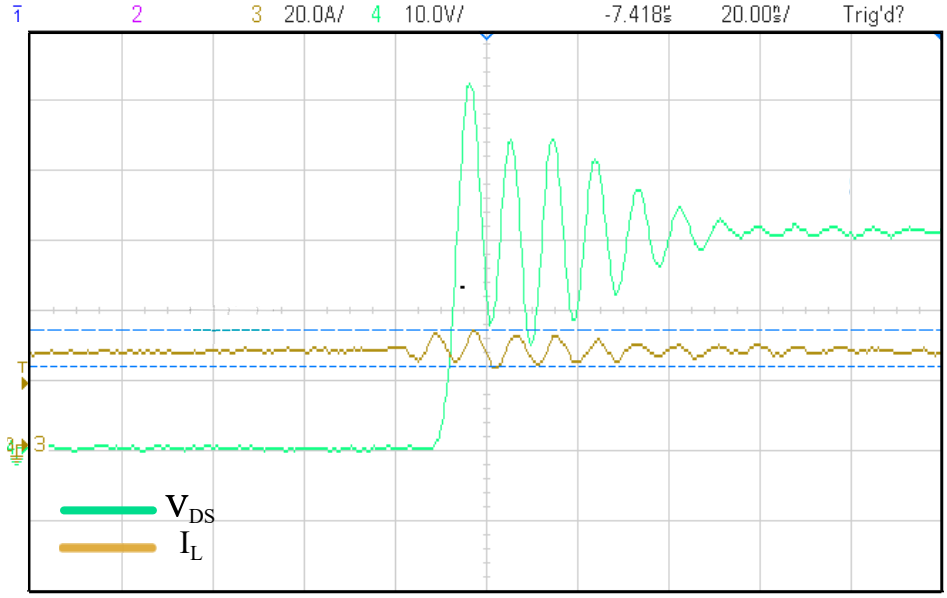


Figure 8.24: V_{DS}, I_L 36A hard turn Off *(Scale: Y-axis : 20V,20A/div, X-axis : 20ns/div)*

From the above result, the observed turn Off time can be approximated to be *2.5ns* and the overshoot is of 25V at 36A hard turn Off. The oscillations in V_{DS} and I_L are sustained for 55ns. Hence causing additional switching losses.

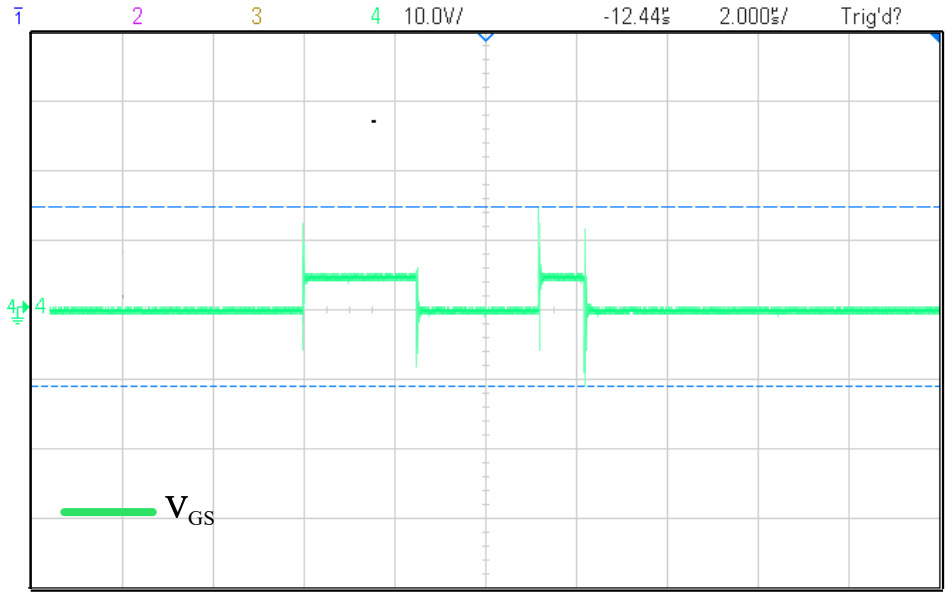


Figure 8.25: V_{GS} *(Scale: Y-axis : 10V/div, X-axis : 2µs/div)*

Above shown is Gate-Source voltage at 36A device current, overshoots of more than 5V can be seen.

8.3.3 Test at $R_g = 0\Omega$

Finally DPT has been done with gate resistance to be 0Ω. The inherent resistance of the gate is 0.2Ω and later all the results shall be compared. For this case $V_i = 30V$ and $L = 3.75\mu H$

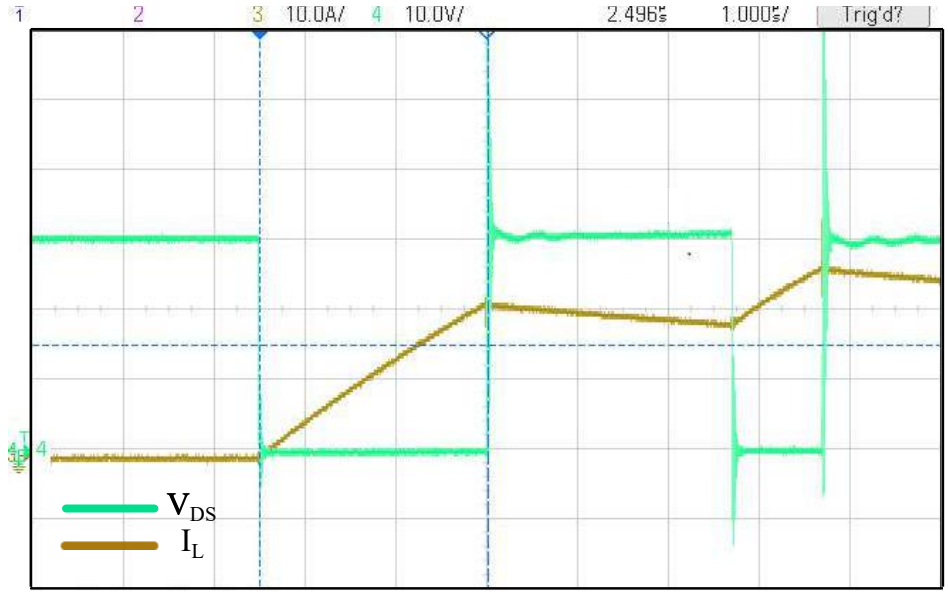


Figure 8.26: V_{DS}, I_L. *(Scale: Y-axis : 10V,20A/div, X-axis : 1µs/div)*

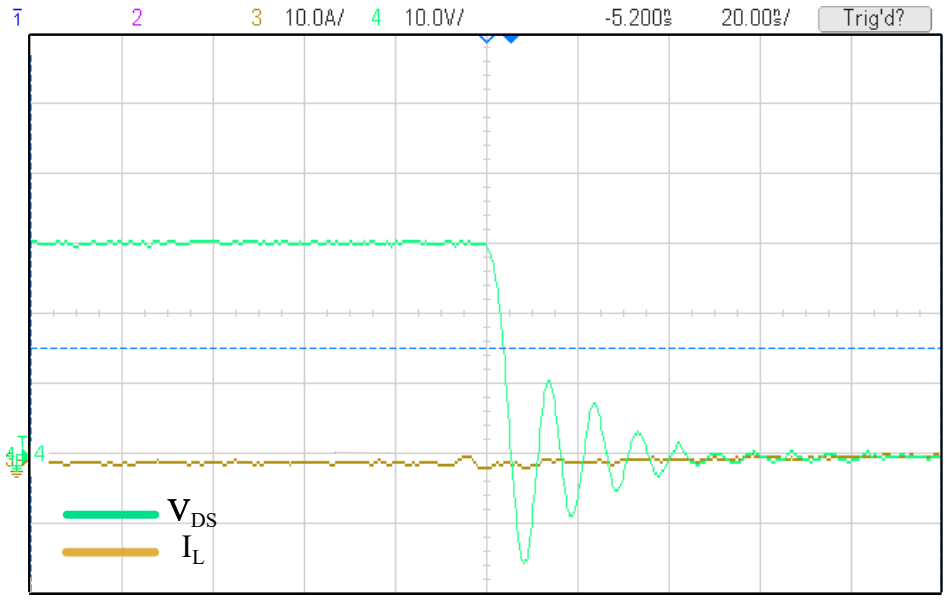


Figure 8.27: V_{DS}, I_L,first turn On at 0A *(Scale: Y-axis : 20V,20A/div, X-axis : 10ns/div)*

The turn On time is seen to be approximately *2.5ns* and the overshoot in V_{DS} is 16V.

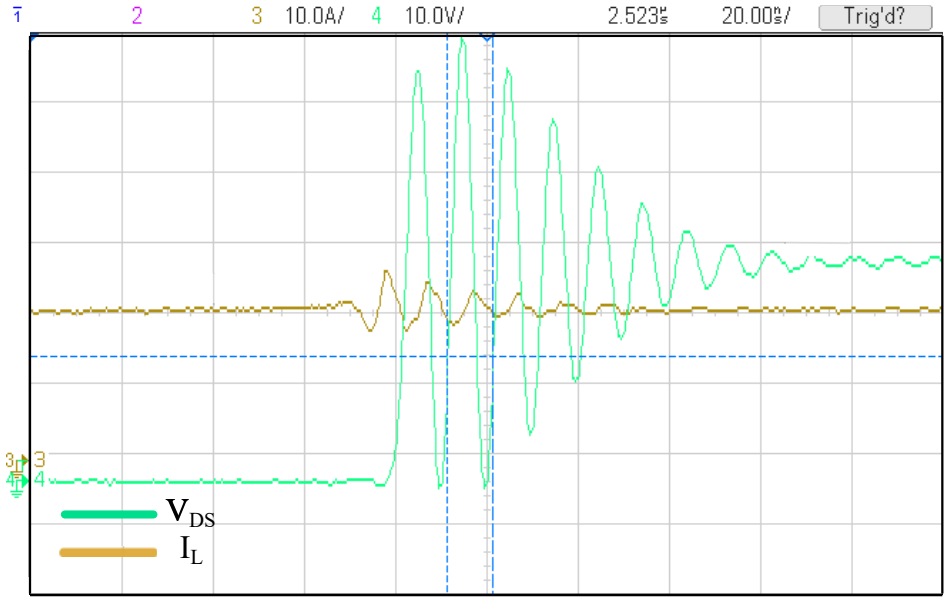


Figure 8.28: V_{DS}, I_L, first turn Off at 22A *(Scale: Y-axis : 10V,20A/div, X-axis : 20ns/div)*

The turn Off time observed is approximately to be *2.5ns*, an overshoot of 30V is seen and the oscillations are sustained for over 100ns. The crossing between V_{DS} and I_D for such long duration causes high switching losses.

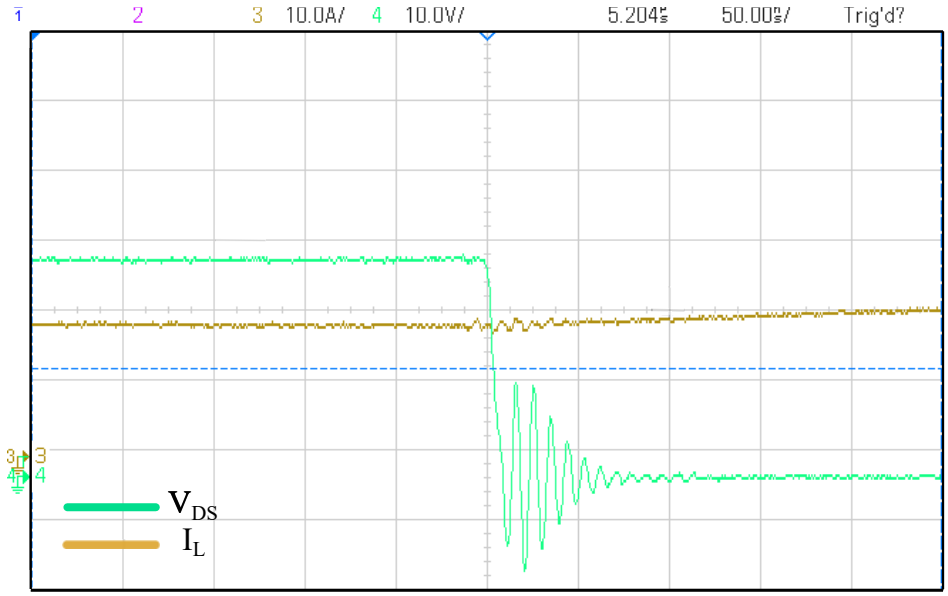


Figure 8.29: V_{DS}, I_L,second turn On at 18A *(Scale: Y-axis : 20V,20A/div, X-axis : 50ns/div)*

In the above figure, the turn On time observed is approximately to be *2.5ns*. The overshoot experienced in the switch is of 12V.

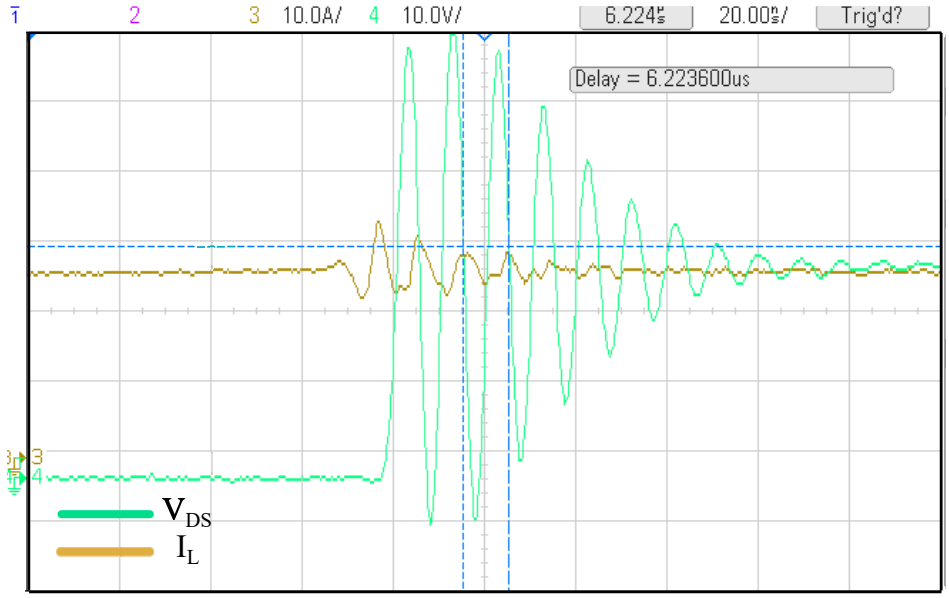


Figure 8.30: V_{DS}, I_L, second turn Off at 25A *(Scale: Y-axis : 10V,20A/div, X-axis : 20ns/div)*

The turn Off time observed is approximately *2.5ns*. An overshoot of 30V is seen while turning off. The crossing between V_{DS} and I_D is of 40ns.

Hence from the above results, we can certainly draw some obvious conclusions. Firstly, when the gate resistance is increased the respective turn On and turn Off time increase. Secondly, for any R_g the First turn On time is lesser than the second turn On time. Thirdly, the voltage overshoot during hard turn Off is always greater than the overshoot during turn ON, hence during turn Off there is a significant amount of loss that is greater than the switching loss during turn On. And Finally, when the $R_g = 0\Omega$ the turn On and turn Off time required is the same as 2.5ns. Therefore the switching dynamics cannot be reduced further.

Also seen in the above results is the V_{GS} of the device which shows huge overshoots above than the device's rating. For the given device one of the major limitation is the $V_{GS_{max}}$ that is 6V only(for EPC2001C) so only a safe margin of 1V is available with us to play around with. As per the device it is recommended to have a minimum gate resistance of 4.8Ω. The observed V_{GS} is not exactly that is appearing across the device, the high overshoots are observed due to the presence of inductance in the measurement path. Below shown is the measurement loop, the layout inductance present in the loop that results in wrong measurement of V_{GS}.

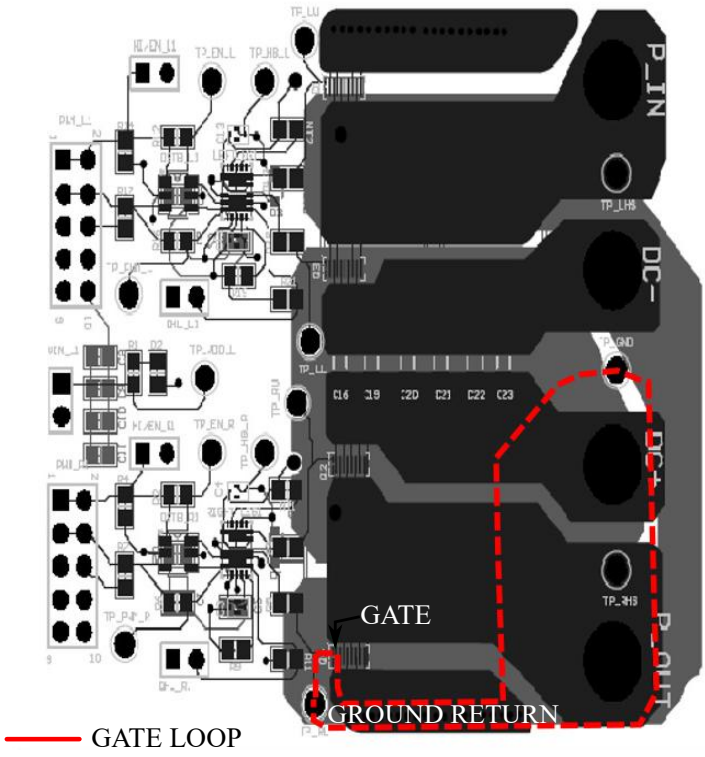


Figure 8.31: V_{GS} loop

The exact excursions in the gate source voltage for a particular gate resistance can be calculated by the expression.

$V_{GS_{peak}} = V_{DR}(1 + \exp^{\frac{-k\pi}{\sqrt{1-k}}})$ where $k = \frac{R_g}{2}\sqrt{\frac{L_{eq}}{C_{ISS}}}$. [31]

It is recommended to keep a test point as close to the gate return of the device as possible to see the actual gate source voltage. Therefore for safer operation of the device if we are operating around 500kHz keeping the gate resistance in $5 - 10\Omega$ is a safer option to minimize the overshoots. In Figure 8.15, the observed ringing frequency for the V_{DSON} for a bottom switch is around 100MHz i.e $f_n = 100MHz$ As we know the ringing frequency in power loop, $f_n = \frac{1}{2\pi\sqrt{L_{PL}C_{OSS}}}$ where L_{PL} is the inductance in the power loop. Hence calculated layout inductance in power loop is 4.5nH.

The calculated power loop inductance from the PCB is mainly the ESL of the film capacitors and the trace inductance, ESL which is around 10nH, 4 of such Film Capacitors are in parallel resulting in 2.5nH of ESL. Each device has trace inductance of around 0.314nH.

The difference between the observed and calculated power loop inductance is due to the fact that in calculation of the inductance we have considered the inductance of the planes as negligible and the resultant vias inductance will be very less because they have been paralleled. In the board designed it has very less common source inductance since the return to ground is by vias and a power plane resulting in very less parasitic inductance that can be considered negligible. The board parasitic capacitances that may come into action have also been ignored in the above calculations. In the above calculation no mutual effect has been considered that creeps from other the flux generated by the other copper planes.

Similarly in Figure 7.18, Observed ringing frequency for the V_{GS} for a bottom switch is around 100MHz i.e $f_n = 100MHz$. As we know the ringing frequency in gate loop, $f_n = \frac{1}{2\pi\sqrt{L_{GS}C_{ISS}}}$ where L_{GS} is the inductance in the gate loop. Hence observed layout inductance in gate loop is 4.38nH.

The calculated gate loop inductance is mainly decided as shown in Fig.8.31 by the trace running from gate driver output to the gate of the device the gate return is through a via. Therefore the calculated gate loop trace inductance is around 9nH by the microstrip inductance calculator.

$L_{ms} = 0.00508L(ln(\frac{2L}{W+H}) + 0.5 + 0.2235(\frac{W+H}{L}))\mu H$. [32]

The calculated via inductance is 0.9nH by the via inductance calculator
$L_{via} = 5.08h[ln(\frac{4h}{d}) + 1]nH$. [33]
Resulting in a total of 9.9nH. The huge difference between the calculated and observed inductance is mainly due to the flux cancellation generated by the beneath DC+ plane that results in a reduced value of inductance. Hence the value of the leakage inductance can be reduced considerably if we use components with smaller packages and use more stiching vias. Thus to get accurate results of the layout inductance during designing the board its better recommended to use some FEM software and avoid manual calculations.

8.4 Conclusion

Hence in this chapter, a lucid discussion has been made on the operation of the developed H-Bridge prototype working as an inverter with inductive load at 400kHz, 800kHz and 1MHz. Clearly the effect of increasing frequency is understood and the performance of the device at such high switching frequencies is remarkable which gives us the idea that these devices can be used at frequencies greater than 500kHz hence minimizing the converter size. DPT has been carried out on the DUT to study the dynamic switching characteristics of the GaNFETs and also estimate the value of layout inductances of the developed PCB which is remarkably very less around 2nH. The effect of reducing R_g on switching dynamics has been shown and hence a safer value of R_g has been derived that ensures the proper operation of the devices at high switching frequencies.

Chapter 9

Conclusions and Future work

9.1 Conclusions

In this thesis a detailed study of the GaN devices has been done which in today's market shall serve the best substitute for making high power density converters. Here a new topology that is 3ϕ multilevel SRC has been investigated and the it's evolution from standard 3ϕ converter has been explained. A proper analysis of the converter has been done and the importance of each component has been specifically mentioned. The simulations done in Chapter.4 clearly show the working of the 3ϕ Multilevel SRC, the effect of the non-idealities in the converter too has been explained with the help of Phasor Diagrams. Before moving onto the 3ϕ Multilevel topology the thesis takes a look on 1ϕ SRC nd the various conditions that need to be satisfied for ZVS during turn ON for input as well as output bridge have been derived and respective simulations have been done showing the working of the SRC in BOOST mode as well as BUCK, with as well as without non-idealities. In the next chapter a complete analysis has been done for ϕ DAB converter where various essential converter parameters have been derived and their variation with gain and the phase shift has been derived. Conditions that need to be satisfied for ZVS operation of the bridges have been derived and respective simulations have been done to support the derivations. In the next chapter of the thesis the development of the ϕ Full Bridge Module has been discussed, the used device has been simulated in LTSpice and the switching transitions have been observed. The various considerations that need to be taken while making of the layout too have been mentioned. Finally in the next chapter the above developed prototype has been tested as an inverter with inductive load at f_s upto 1MHz which clearly show the proper working at such high frequencies hence enabling us to make a more compact, high power density converter. DPT has been performed to study the switching dynamics of the used GaNFETs and analyze the layout inductance of the developed PCB, which can be later used to predict the overshoots across the device beforehand for a given design.

9.2 Scope of Future Work

The project mainly concentrates on the development of the 1ϕ SRC. The control of the above converter also itself is quite a challenge when it comes to control the converter at high frequencies, if the conventional average current mode control is done then measuring the current at frequencies of 1MHz is a challenge so some alternative control where equating power flows and hence controlling the output voltage by varying the f_s & δ is a good alternative. Control of 1ϕ SRC is already a field of extensive research but a simple control strategy would serve as a good topic to research on. Also the above designed PCB has already very less layout inductance but when working at high frequencies for compact high power density converters this small layout inductance can also be disastrous hence minimizing the inductance also serves as a good challenge and should be a good area to work on. At frequencies above 1MHz the EMI and EMC problems also creep into the system hence corrupting the gate signals, when the corruption of the gate signals is of considerable amount it might result in false turn ON/Off the devices hence malfunctioning of the converter. So ways to prevent the interference rather to minimize these is also a good scope to work on.

Similar to the design of the 1ϕ SRC, can be extended to build the proposed 3ϕ Multilevel SRC which can be actually used for automotive applications. In the three phase topology comparisons must be done between SRC and DAB for high switching frequencies and the advantage of one over the other must be clearly understood which shall make the converter with highest efficiency.

References

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