DESIGN OF CRYSTAL OSCILLATOR REFERENCES FOR FREQUENCY SYNTHESIZERS

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN OF CRYSTAL OSCILLATOR REFERENCES FOR FREQUENCY SYNTHESIZERS**, submitted by **Mahabaleshwar Bhat**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Crystal oscillators are used as reference clocks for generating higher frequency clocks due to their low output phase noise. In this project $20\,\mathrm{MHz}$ and $114\,\mathrm{MHz}$ crystal oscillators and a $990\,\mathrm{MHz}$ MEMS-resonator oscillator are designed in a 65nm process. All three oscillators have a worst-case Figure of Merit greater than $197\,\mathrm{dB}$. Digitally controlled capacitor banks were designed for tuning the oscillation frequency. The tuning range of the $20\,\mathrm{MHz}$, $114\,\mathrm{MHz}$, and $990\,\mathrm{MHz}$ oscillators are $9.6\,\mathrm{kHz}$, $7\,\mathrm{kHz}$, and $636\,\mathrm{kHz}$ respectively. The nominal power consumption of these oscillators are $118.5\,\mu\mathrm{W}$, $830.3\,\mu\mathrm{W}$, and $721.4\,\mu\mathrm{W}$ respectively. The area of the layouts of the $114\,\mathrm{MHz}$ and $990\,\mathrm{MHz}$ oscillators are 4.03 $\times 10^{-2}$ mm^2 and 6.192 $\times$ 10^{-3} mm^2 respectively.

Contents

List of Tables

List of Figures

ABBREVIATIONS

NMOS	Negative channel Metal Oxide Semiconductor
PMOS	Positive channel Metal Oxide Semiconductor
SS	Slow-Slow
FF	Fast-Fast
TT	Typical-Typical

Chapter 1

INTRODUCTION

The crystal oscillator, as the name suggests, uses a crystal for producing oscillations. For electrical oscillations, an LC tank circuit is necessary. The crystal is also modelled as an LC tank but with an inherent lossy component as shown in the Figure 1.1. R_m is the motional Resistance and represents the mechanical losses in the crystal. L_m is the motional Inductance and represents the movement of the crystal mass. C_m is the motional Capacitance which represents the charge gained during the vibrations. C_o represents the electrodes of the crystal plus the stray capacitance from the holder.

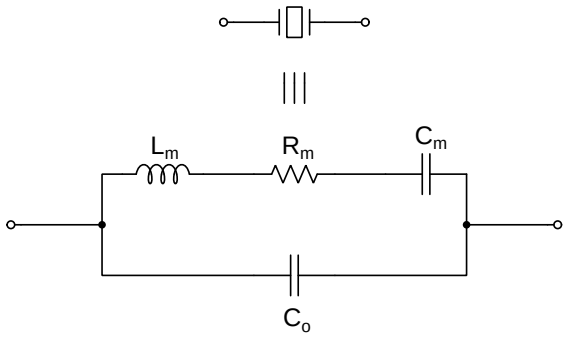


Figure 1.1: Equivalent model of a crystal.

The motional Resistance R_m will not allow the crystal to have sustained oscillations. So we need an active circuitry which will provide the necessary "negative" resistance to cancel out R_m. The magnitude of the real part of the impedance Z_a as shown in Figure 1.2, should be greater than or equal to R_m to start and have sustained oscillations.

Figure 1.3 shows a three-point oscillator [1], [2]. If we consider Z_1, Z_2 and Z_3 to be pure capacitance impedances, then the real part of the negative impedance Z_c is given by,

$$Re(Z_c) = \frac{-g_m C_1 C_2}{(g_m C_3)^2 + \omega^2 (C_1 C_2 + C_2 C_3 + C_1 C_3)^2}$$

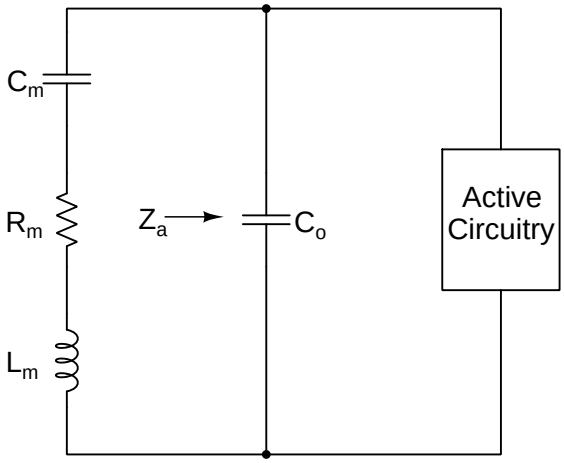


Figure 1.2: Impedance Z_a.

From the equation, we can see that the real part of the impedance Z_c i.e. R_N, does not monotonically increase with g_m. It increases and reaches a maximum at a particular value of g_m and then starts decreasing. For the oscillator to function properly, we need to make sure that the R_N is more than the motional resistance at all process and temperature corners.

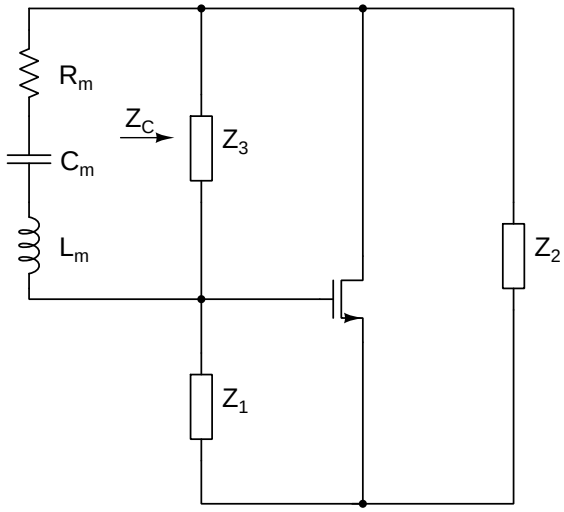


Figure 1.3: General form of three-point oscillator.

In this project, the topology used for the design of crystal oscillator is as shown in the Figure 1.4. It is called as Pierce oscillator, named after its inventor George W. Pierce. The expression for its frequency of oscillation is [4],

$$f_p = \frac{1}{2\pi\sqrt{L_m}}\sqrt{\frac{1}{C_m} + \frac{1}{(C_o + C_L)}}$$

where $C_L = C_1 \parallel C_2$

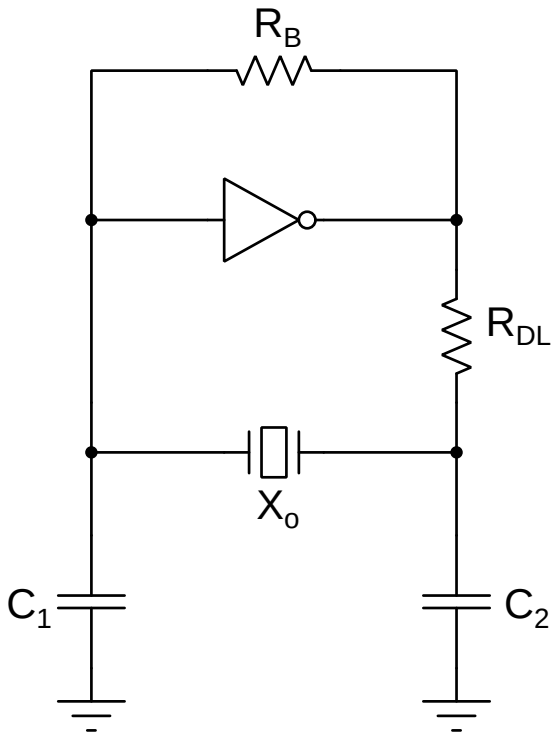


Figure 1.4: Pierce oscillator.

For the Pierce oscillator, the expression for negative resistance including the feedback resistor R_B and the R_{ds} of the amplifier is given by,

$$R_N = \frac{R_B(1+g_m R_{ds})^2 + \omega^2 R_B R_{ds}(-g_m R_B R_{ds} C_1 C_2 + R_{ds}(C_1+C_2)^2 + R_B C_1^2)}{(1+g_m R_{ds} - \omega^2 R_B R_{ds}(C_1C_2+C_2C_3+C_1C_3))^2 + (\omega R_{ds}(C_1+C_2) + \omega R_B(C_1+C_3(1+g_m R_{ds})))^2}$$

The values of R_m, L_m, C_m, C_o are the characteristics of the crystal and are obtained from the datasheet. The load capacitance C_L will also be specified for obtaining a particular frequency of oscillation.

Chapter 2

CRYSTAL OSCILLATORS

2.1 General topology

The general schematic of the designed Pierce oscillators is shown in Figure 2.1. The core consists of a self-biased inverter which acts as the active component to provide the required negative resistance. The cap bank acts as the load capacitor which can be varied to tune the frequency of oscillation. The resistor R_{DL} is used to limit the current through the crystal. The sine wave is taken out through a buffer at t1. This is because the waveform at t1 has lesser noise and distortion as compared to t2. The buffer is used to convert the sine wave to a square wave which can be used as a reference clock source. The Oscillator is designed in the TSMC 65GP process with a supply voltage of $1\,\mathrm{V}$.

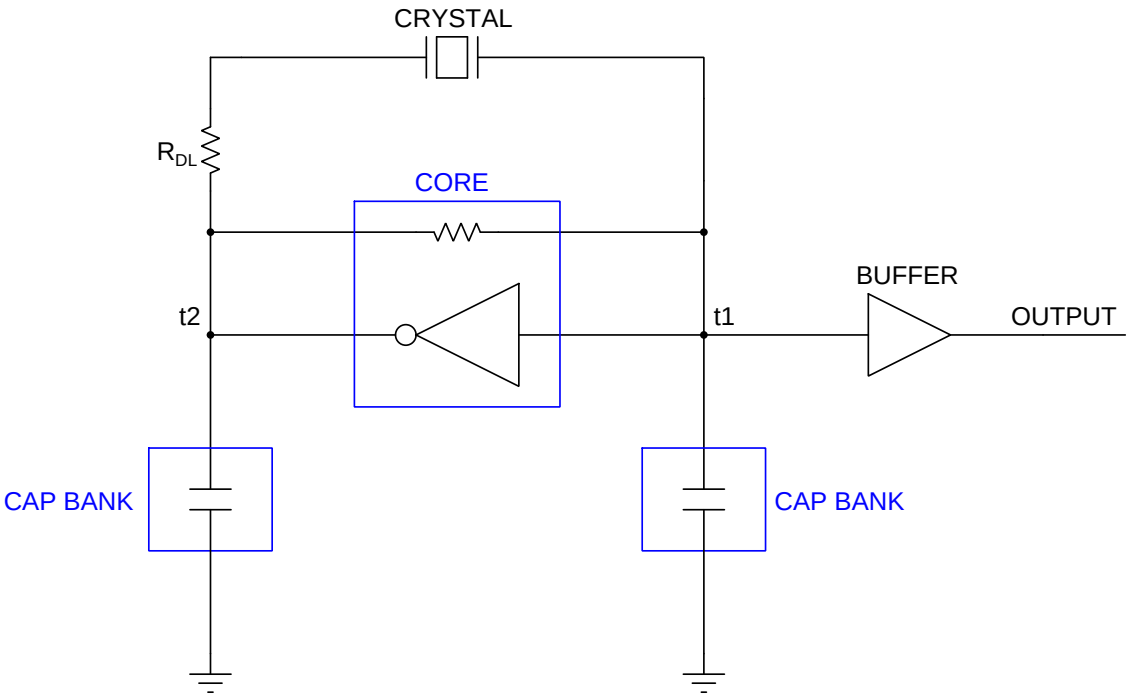


Figure 2.1: General schematic of Pierce oscillator.

2.2 20 MHz Oscillator

The crystal used for the 20 MHz oscillator was ECX-2236 (ECS Inc. International) [6] which has a motional resistance of 34 Ω. The shunt capacitance C_o is 2 pF and the prescribed load capacitance C_L is 8 pF for the frequency of 19.2 MHz. The drive level, that is, the maximum power allowed to be dissipated through the crystal is 100 µW.

The 20 MHz crystal oscillator uses the same topology as shown in Figure 2.1. As seen in Chapter 1 the expression for negative resistance is

$$R_N = \frac{R_B(1+g_m R_{ds})^2+\omega^2 R_B R_{ds}(-g_m R_B R_{ds} C_1 C_2 + R_{ds}(C_1+C_2)^2 + R_B C_1^2)}{(1+g_m R_{ds}-\omega^2 R_B R_{ds}(C_1C_2+C_2C_3+C_1C_3))^2+(\omega R_{ds}(C_1+C_2)+\omega R_B(C_1+C_3(1+g_m R_{ds})))^2}$$

Here, the values of the variables are taken as R_B = 40 kΩ, R_{ds} = 2 kΩ and C_3 = 2 pF. The plot of R_N versus g_m is shown in Figure 2.2 for load capacitance values of 4 pF, 8 pF, and 13 pF.

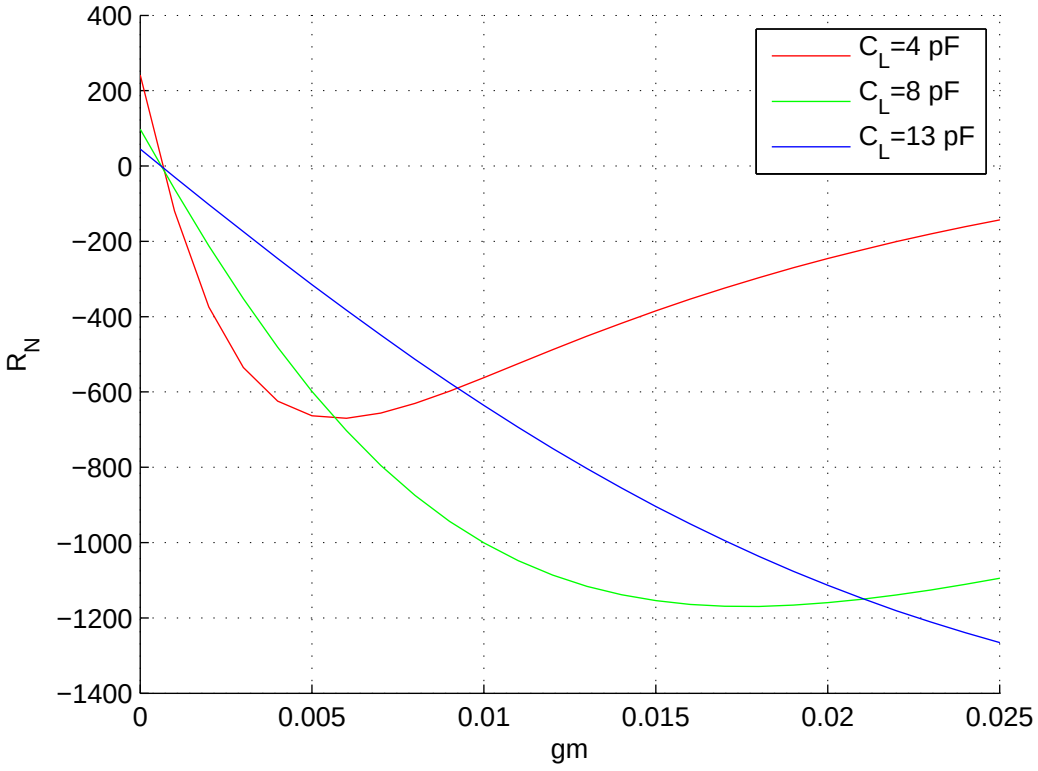


Figure 2.2: R_N versus g_m plot.

2.2.1 Oscillator core

From the plot, we can see that the g_m that we need varies with the load capacitance. It will also vary with process and temperature corners. So the oscillator core is designed to be programmable to obtain various values of g_m. Figure 2.3 shows the schematic of the core. It has self-biased inverters which act as the active component providing the required negative resistance to have sustained oscillations. The PMOS and the NMOS transistors in the four branches are of the same size. Each transistor has a g_m of approximately $1\,\mathrm{mS}$ at TT $27\,^{\circ}\mathrm{C}$. The control bits CTL0,1,2,3 are used to switch on and off the four branches. The aim is to have sustained oscillations by getting the required value of g_m with low power consumption.

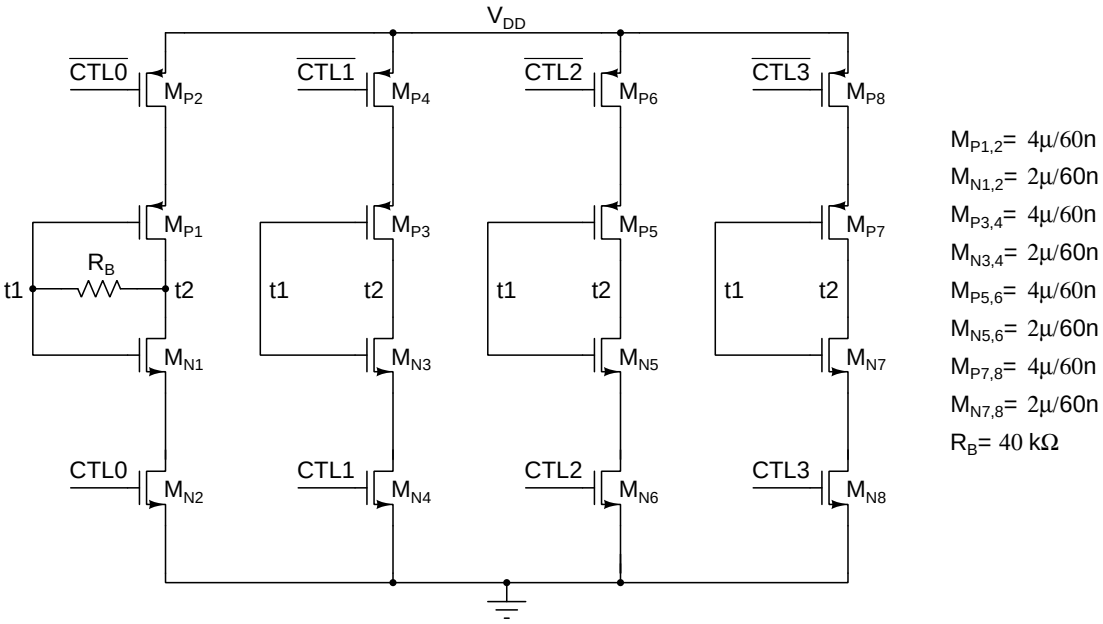


Figure 2.3: Schematic of Oscillator core.

2.2.2 Capacitor bank

The block diagram of the capacitor bank is shown in Figure 2.4. It has 128 instances of the main cap bank unit and 7 instances of sub cap bank unit. The sub cap bank unit is for getting a higher frequency resolution. The value of the sub cap unit capacitance is chosen such that the frequency tuning stays almost linear and there exists a continuity during tuning. So, C_{sub} = $C_{main}/(N+1)$ where N is the number of sub cap units used. Here N=7 and C_{main} = $150\,\mathrm{fF}$. Therefore, C_{sub} = $18.75\,\mathrm{fF}$.

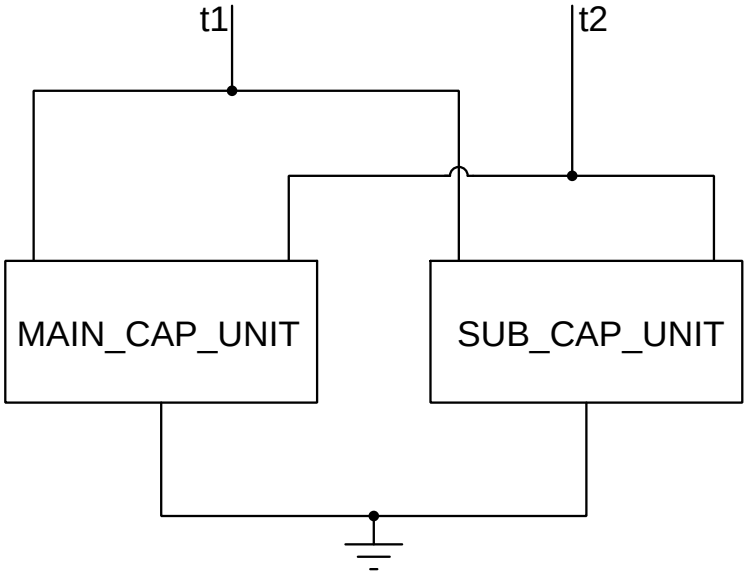


Figure 2.4: Capacitor bank block diagram.

Figure 2.5 shows the schematic of the main cap bank unit. The differential capacitance provided by the unit is $150\,\mathrm{fF}$ at TT $27\,^{\circ}\mathrm{C}$. S is the control signal used to switch the main cap bank unit on and off. M_{N1} and M_{N2} connect the capacitors to ground when S=1. M_{P1} and M_{P2} are used to prevent the NMOSes from getting switched ON when S=0. The transistors are sized such that the quality factor is high in the ON state and the OFF capacitance is low. The worst-case quality factor is 268 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $19\,\mathrm{fF}$ (FF $80\,^{\circ}\mathrm{C}$).

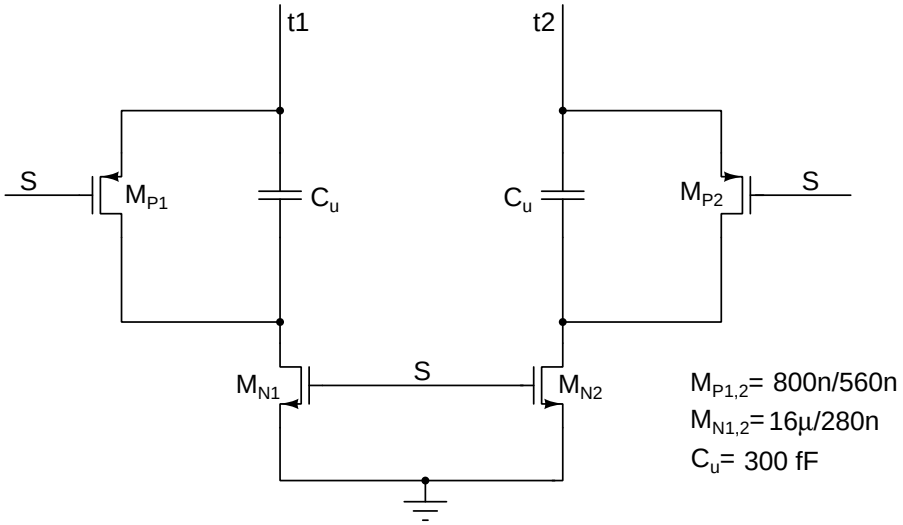


Figure 2.5: Main cap unit.

Figure 2.6 shows the schematic of the sub cap bank unit. The capacitance provided by the unit is 18.75 fF. The worst-case quality factor is 102 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $1.45\,\mathrm{fF}$ (FF $80\,^{\circ}\mathrm{C}$).

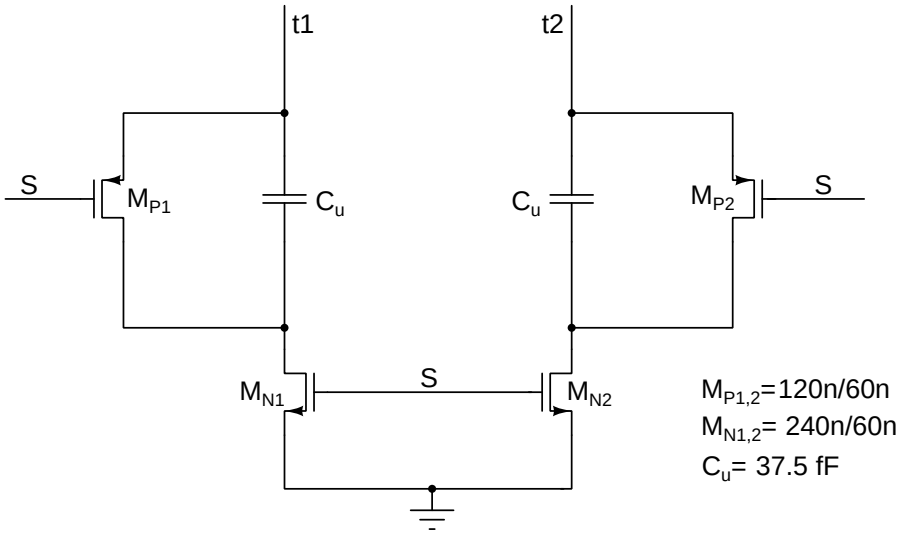


Figure 2.6: Sub cap unit.

2.2.3 Voltage buffer

Figure 2.7 shows the schematic of the voltage buffer. The capacitor C_C is used as the decoupling capacitor. The resistor R_B is used for self-biasing. The transistors are sized such that they provide enough gain and their thermal noise contribution is minimum.

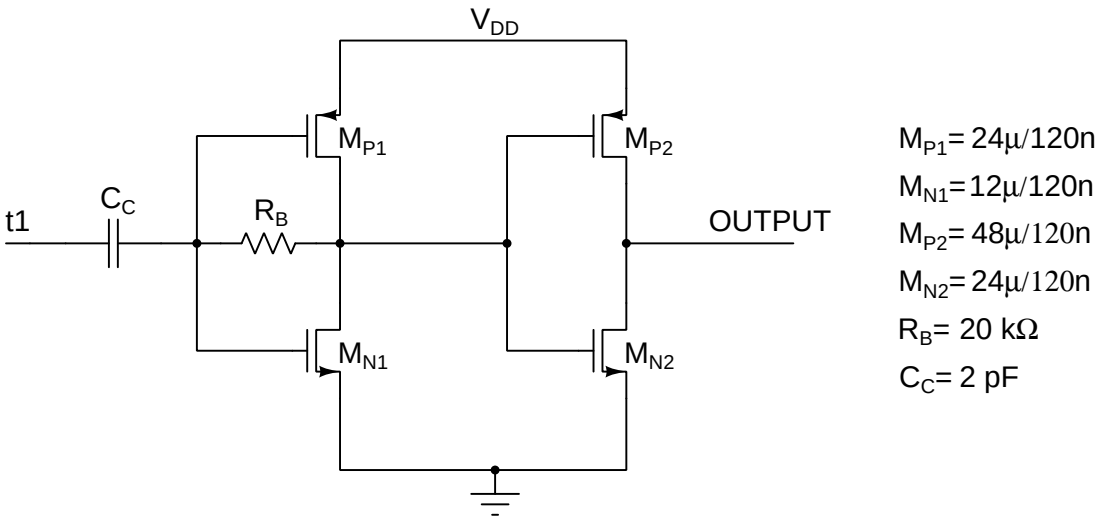


Figure 2.7: Schematic of the voltage buffer.

2.2.4 Simulation results

The simulations were done for load capacitances of $4\,\mathrm{pF}$, $8\,\mathrm{pF}$, and $13\,\mathrm{pF}$. The simulations were done across SS, SF, TT, FS, and FF process corners for $0\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ temperatures. To get the necessary negative resistance across all the corners, the g_m

had to be varied. This was done by switching on and off the inverter branches of the core, thereby obtaining the required g_m with reasonable power consumption. The drive limiting resistor R_{DL} used here was $500\,\Omega$. The simulations were done using hb and hbnoise(sampled jitter) analysis. The results tables consist of the power consumed by the core, the power dissipated in the crystal, the phase noise at the output of the buffer, taken at offset frequencies of $1\,\mathrm{kHz}$, $10\,\mathrm{kHz}$, and $100\,\mathrm{kHz}$, the peak to peak amplitude of oscillation at t1, and the oscillation frequency.

The Figure of Merit (FoM) of an oscillator is given by the expression [3],

$$FoM = |phasenoise(dBc/Hz)| + 20\log_{10}\left(\frac{f_0}{\Delta f}\right) - 10\log_{10}\left(Power(mW)\right)$$

where f_0 is the frequency of oscillation and Δf is the offset frequency at which the phase noise is measured. Tables 2.1, 2.2 and 2.3 show the results for $4\,\mathrm{pF}$, $8\,\mathrm{pF}$, and $13\,\mathrm{pF}$ respectively. The worst and the best cases of each parameter are indicated by red and blue colors respectively.

Table 2.1: Results for load capacitance = $4\,\mathrm{pF}$.

Corner	**Temperature** (°C)	**Total Power** (μW)	**Drive Level** (μW)	**Phase noise**			**Amplitude at T1** (V_{pk-pk})	**Oscillation Frequency** (MHz)
				@1kHz (dBc/Hz)	**@10kHz** (dBc/Hz)	**@100kHz** (dBc/Hz)		
SS	0	**42.6**	**10.67**	**-130.7**	**-150.2**	-151.2	788.9m	19.2166
	80	48.2	10.55	-130.5	-149.3	-150.4	780.1m	19.2165
FF	0	110.5	6.911	**-118.3**	-143.9	-148.2	688.4m	19.2203
	80	**133**	**6.453**	-118.7	**-142.5**	**-146.7**	**663m**	19.2202
TT	0	60.06	9.705	-123.7	-148.7	-151.2	**797.4m**	19.2181
	27	63.24	9.612	-124	-148.6	-151	791.6m	19.2181
	80	69.44	9.389	-124.1	-148	-150.3	768.6m	19.2181
FS	0	58.52	9.41	-124.4	-148.9	-151.1	787.4m	19.2181
	80	67.63	9.077	-124.7	-147.8	-150	768.4m	19.2181
SF	0	60.99	9.596	-123.7	-148.8	**-151.3**	790.7m	19.2181
	80	68.59	9.137	-124	-147.6	-149.9	766.9m	19.2180

Table 2.2: Results for load capacitance = 8 pF.

Corner	Temperature °C)	Total Power (μW)	Drive Level (μW)	Phase noise @1kHz (dBc/Hz)	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Amplitude at T1 (V_{pk-pk})	Oscillation Frequency (MHz)
SS	0	**74.6**	**22.66**	**-137.5**	**-150.4**	-151.2	768.9m	19.2117
	80	87.71	21.83	-137	-149.3	-150	752m	19.2117
FF	0	217.9	14.68	-127.2	-146.3	-148.9	730.5m	19.2147
	80	**271.1**	**12.94**	**-126.9**	**-143.9**	**-147.1**	683.2m	19.2147
TT	0	110.5	20.67	-131.6	-150.2	**-151.4**	803m	19.2130
	27	118.5	20.2	-131.7	-149.8	-151	792.7m	19.2130
	80	134.8	19.1	-131.9	-148.9	-150.2	768.6m	19.2130
FS	0	102.4	21.42	-132.2	-150.2	-151.3	**819.1m**	19.2129
	80	123	20.39	-132.2	-148.7	-149.9	796.1m	19.2130
SF	0	119.6	18.01	-131.1	-149.7	-151	747.5m	19.2129
	80	144.2	14.91	-131.2	-147.7	-149.2	**676.7m**	19.2129

Table 2.3: Results for load capacitance = 13 pF.

Corner	Temperature °C	Total Power (μW)	Drive Level (μW)	Phase noise @1kHz (dBc/Hz)	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Amplitude at T1 (V_{pk-pk})	Oscillation Frequency (MHz)
SS	0	**111.3**	34.12	**-143.1**	-148.4	-149.1	**538.6m**	19.2077
	80	135.9	35.55	-142.1	-147.6	-148.3	549.7m	19.2077
FF	0	321.1	40.08	-136.2	-146.6	-148.8	**740.4m**	19.2095
	80	**396.4**	35.62	**-134.5**	**-144.3**	**-147.3**	697.5m	19.2095
TT	0	170.6	45.04	-140	**-149.5**	**-150.5**	694.9m	19.2084
	27	183.1	44.18	-140	-149.1	-150.1	688m	19.2085
	80	209.2	41.83	-139.5	-148	-149.2	669m	19.2085
FS	0	162.3	**45.44**	-140.3	-149.4	-150.4	698.4m	19.2084
	80	196.6	43.61	-139.8	-148	-149.2	683.7m	19.2085
SF	0	177.2	39.43	-139.1	-148.9	-150	649.2m	19.2084
	80	215.1	**32.31**	-137.9	-146.8	-148.1	586.7m	19.2085

We can see that the tuning range of the oscillator is 9.6 kHz at TT(27 °C) when load capacitance is varied from 4 pF to 13 pF. The FoM at TT(27 °C) with a load of 8 pF is 206 dB. The worst-case FoM is 197 dB at FF(80 °C) with 13 pF load.

Figures 2.8 and 2.9 show waveform at t1 and the phase noise plot from PSS simulation for SS(0 °C), TT(27 °C) and FF(80 °C) corners respectively with the load of 13 pF.

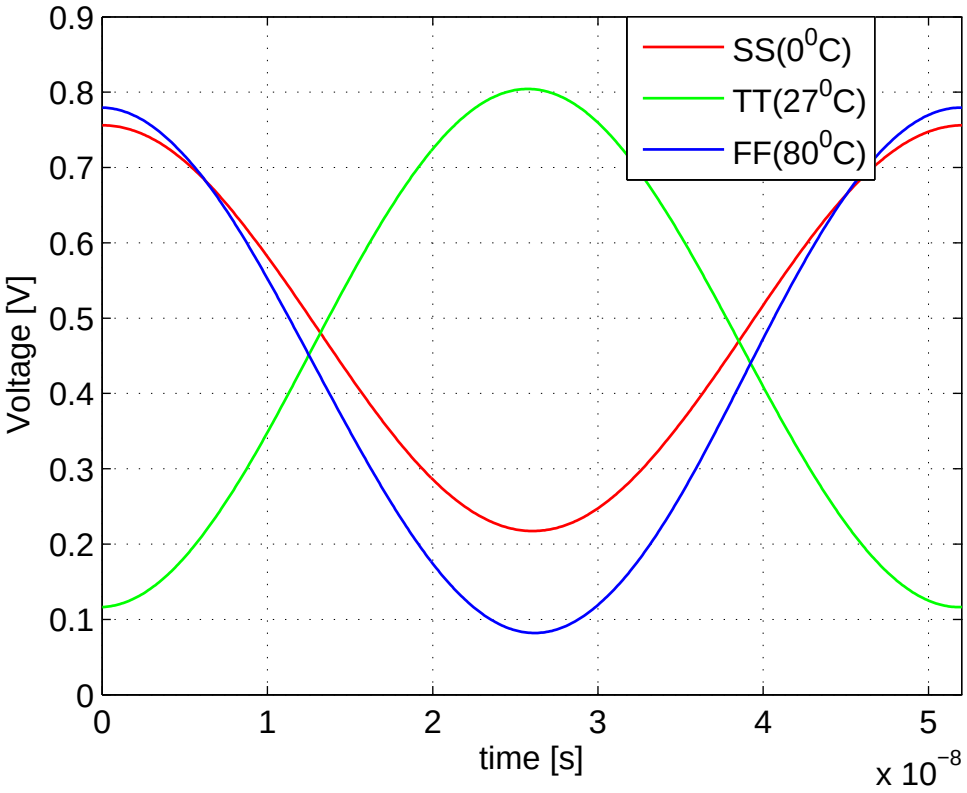


Figure 2.8: Oscillation waveform at t1.

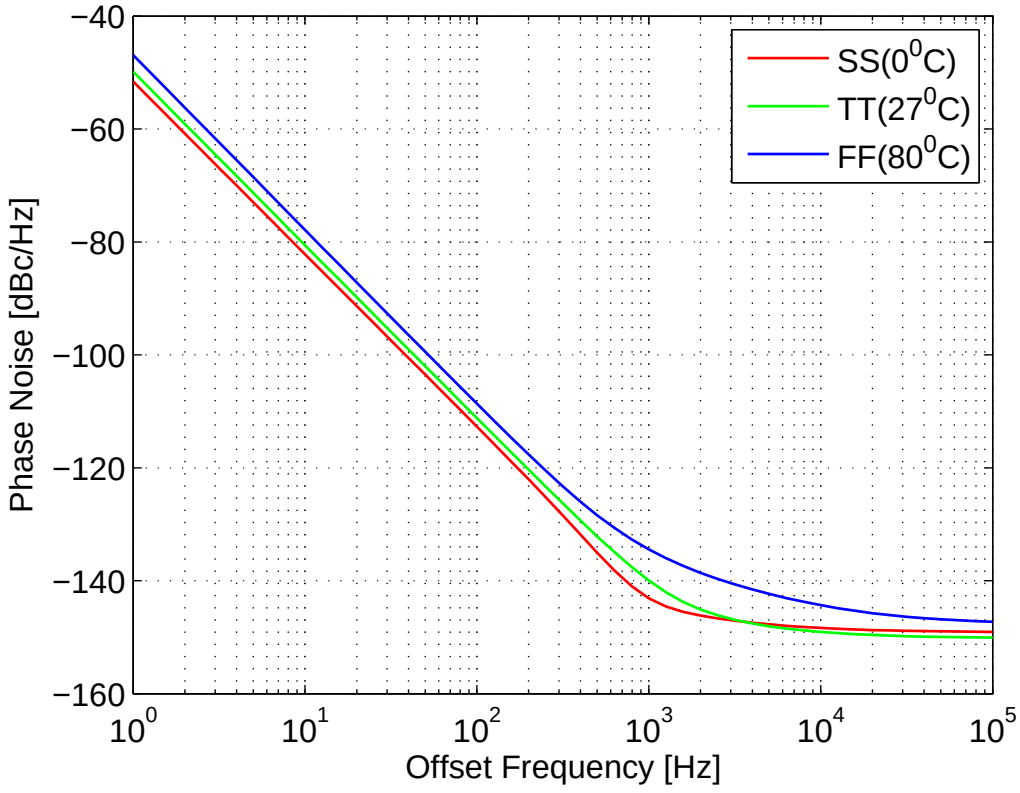


Figure 2.9: Phase noise at the output of the buffer.

2.3 114 MHz Oscillator

The crystal used for the $114\,\mathrm{MHz}$ oscillator was CS-023E (Connor-Winfield Corp.) [7] which has a motional resistance of $39\,\Omega$. The shunt capacitance C_o is $2.5\,\mathrm{pF}$ and the prescribed load capacitance C_L is $18\,\mathrm{pF}$ for the frequency of $114.285\,\mathrm{MHz}$. The drive level, that is, the maximum power allowed to be dissipated through the crystal is $200\,\mathrm{uW}$.

The power dissipated in the crystal can be determined by the expression

$$P(\omega) = \frac{V_P^2 R_m}{2\left(R_m^2 + \left(\omega L_m - \frac{1}{\omega C_{Lm}}\right)^2\right)}$$

where V_P is the voltage across the crystal, R_m, L_m are motional resistance and inductance as discussed in Chapter 1. C_{Lm} is the effective capacitance given by

$$C_{Lm} = \frac{C_m(C_o + C_L)}{C_m + C_o + C_L}$$

C_m is the motional capacitance, C_o is the shunt capacitance and C_L is the load capacitance.

For a V_P of $1\,\mathrm{V}$ and a C_L of $18\,\mathrm{pF}$, the dissipated power turns out to be $3.16\,\mathrm{mW}$ which is much higher than the drive level limit. Hence a lower value of load capacitance was used in the oscillator.

The $114\,\mathrm{MHz}$ crystal oscillator uses the same topology as shown in Figure 2.1. The capacitor bank and gm are modified suitably. As seen in Chapter 1 the expression for negative resistance is

$$R_N = \frac{R_B(1+g_m R_{ds})^2 + \omega^2 R_B R_{ds}(-g_m R_B R_{ds} C_1 C_2 + R_{ds}(C_1+C_2)^2 + R_B C_1^2)}{(1+g_m R_{ds} - \omega^2 R_B R_{ds}(C_1C_2+C_2C_3+C_1C_3))^2 + (\omega R_{ds}(C_1+C_2) + \omega R_B(C_1+C_3(1+g_m R_{ds})))^2}$$

Here, the values of the variables are taken as R_B = $50\,\mathrm{k\Omega}$, R_{ds} = $1\,\mathrm{k\Omega}$ and C_3 = $2.5\,\mathrm{pF}$. The plot of R_N versus g_m is shown in Figure 2.10 for load capacitance values of $2\,\mathrm{pF}$, $3.3\,\mathrm{pF}$, and $4.3\,\mathrm{pF}$.

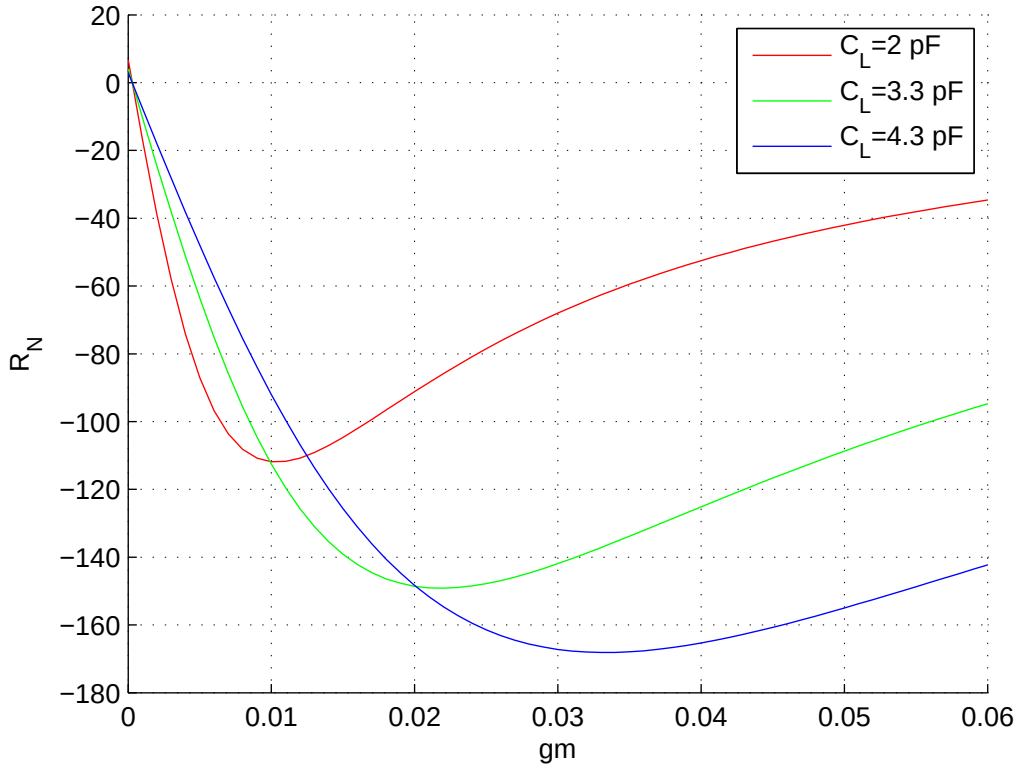


Figure 2.10: R_N versus g_m plot.

2.3.1 Oscillator core

From the plot, we can see that the g_m that we need varies with the load capacitance. It will also vary with process and temperature corners. So the oscillator core is designed to be programmable to obtain various values of g_m. Figure 2.11 shows the schematic of the core. It has self-biased inverters which act as the active component providing the required negative resistance to have sustained oscillations. The sizes of the PMOS and the NMOS transistors are as shown. The first inverter branch of the core has a g_m of approximately $3.16\,\mathrm{mS}$ TT $27\,^{\circ}\mathrm{C}$. The second branch has twice the size of the first branch and hence twice the g_m, i.e. $6.32\,\mathrm{mS}$. The third and the fourth branches have four times the size of the first branch and hence a g_m of $12.65\,\mathrm{mS}$. The control bits CTL0,1,2,3 are used to switch on and off the four branches. The aim is to have sustained oscillations by getting the required value of g_m with low power consumption.

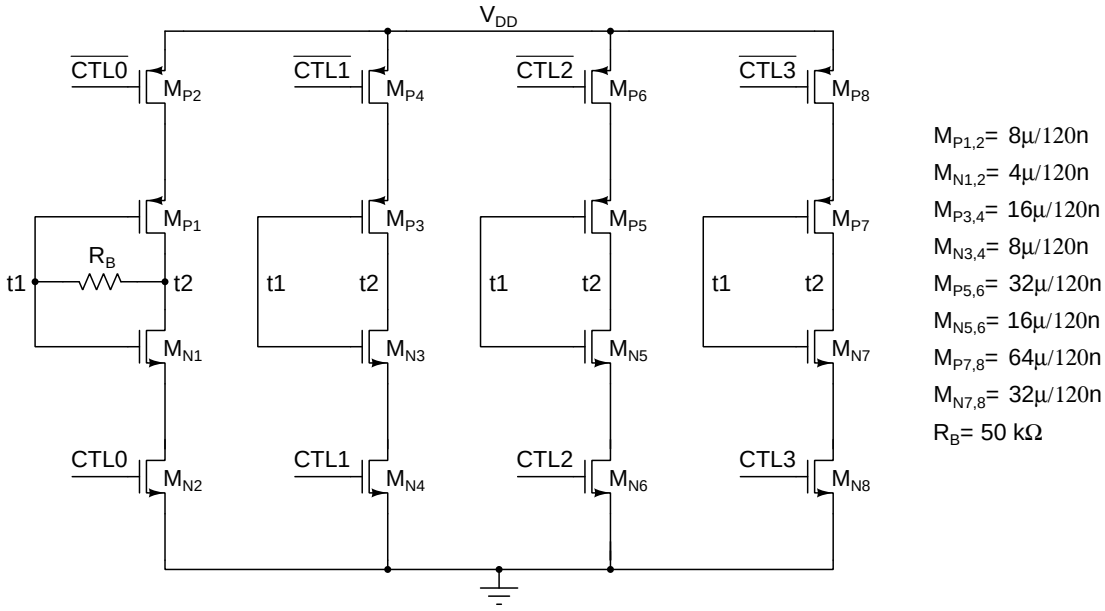


Figure 2.11: Schematic of Oscillator core.

2.3.2 Capacitor bank

The block diagram of the capacitor bank is shown in Figure 2.12. It has 40 instances of the main cap bank unit and 7 instances of sub cap bank unit. The sub cap bank unit is for getting a higher frequency resolution. The value of the sub cap unit capacitance is chosen such that the frequency tuning stays almost linear and there exists a continuity during tuning. So, C_{sub} = $C_{main}/(N+1)$ where N is the number of sub cap units used. Here N=7 and C_{main} = 150 fF. Therefore, C_{sub} = 18.75 fF.

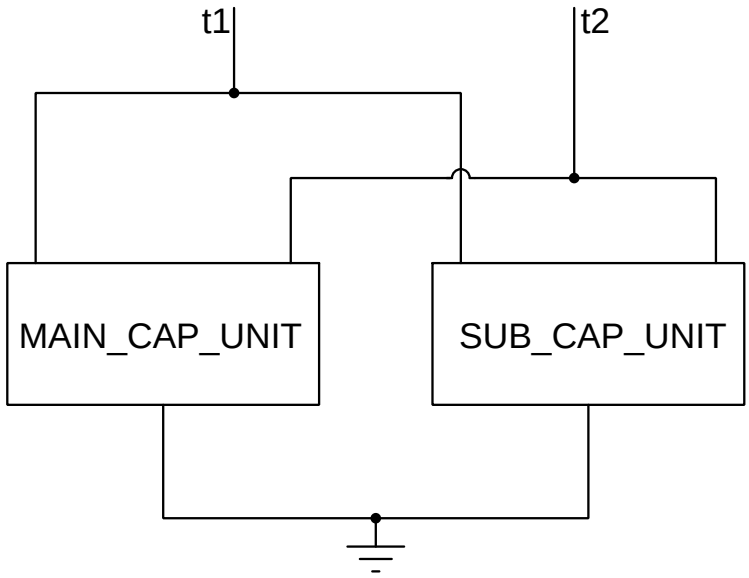


Figure 2.12: Capacitor bank block diagram.

Figure 2.13 shows the schematic of the main cap bank unit. The differential capac-

itance provided by the unit is $150\,\mathrm{fF}$ at TT $27\,^{\circ}\mathrm{C}$. S is the control signal used to switch the main cap bank unit on and off. M_{N1} and M_{N2} connect the capacitors to ground when S=1. M_{P1} and M_{P2} are used to prevent the NMOSes from getting switched ON when S=0. The transistors are sized such that the quality factor is high in the ON state and the OFF capacitance is low. The worst-case quality factor is 45 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $16\,\mathrm{fF}$ (FF $80\,^{\circ}\mathrm{C}$).

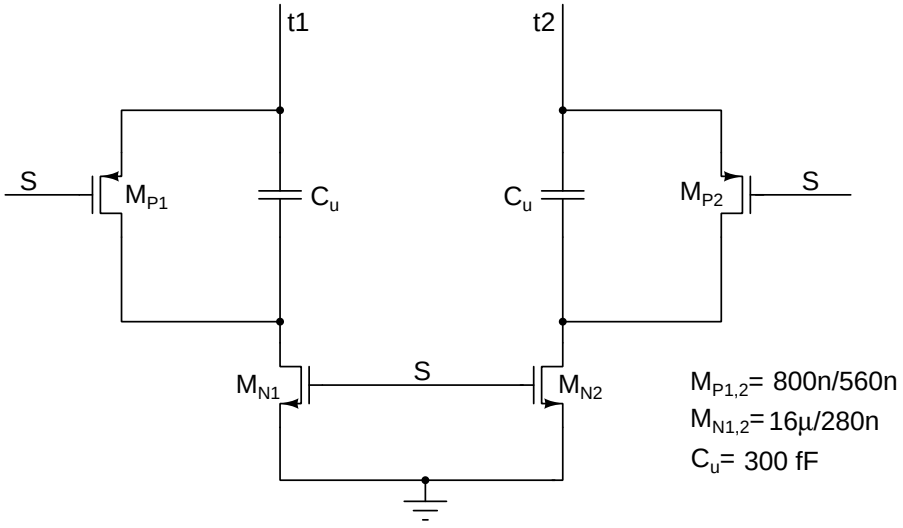


Figure 2.13: Main cap unit.

Figure 2.14 shows the schematic of the sub cap bank unit. The capacitance provided by the unit is $18.75\,\mathrm{fF}$. The worst-case quality factor is 17.26 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $1.36\,\mathrm{fF}$ (SS $80\,^{\circ}\mathrm{C}$).

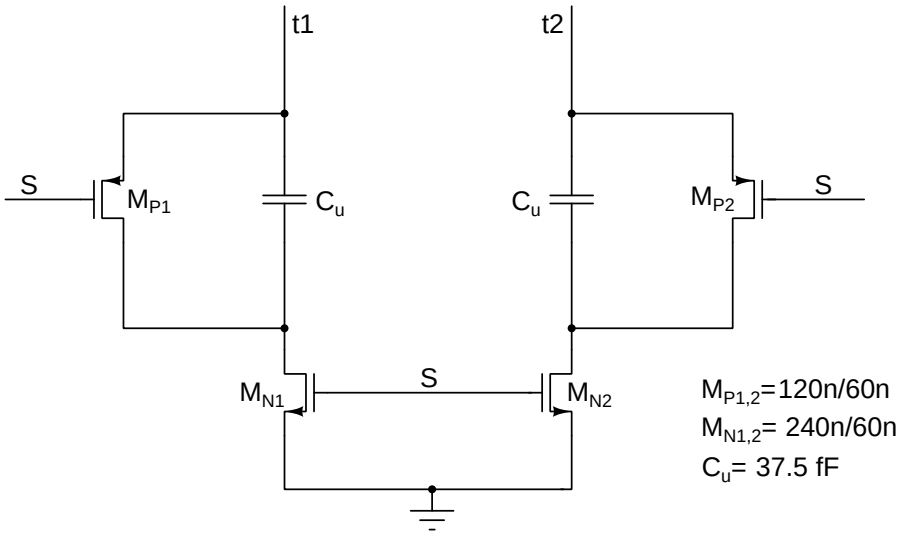


Figure 2.14: Sub cap unit.

2.3.3 Voltage buffer

Figure 2.15 shows the schematic of the voltage buffer. The capacitor C_C is used as the decoupling capacitor. The resistor R_B is used for self-biasing. The transistors are sized such that they provide enough gain and their thermal noise contribution is minimum.

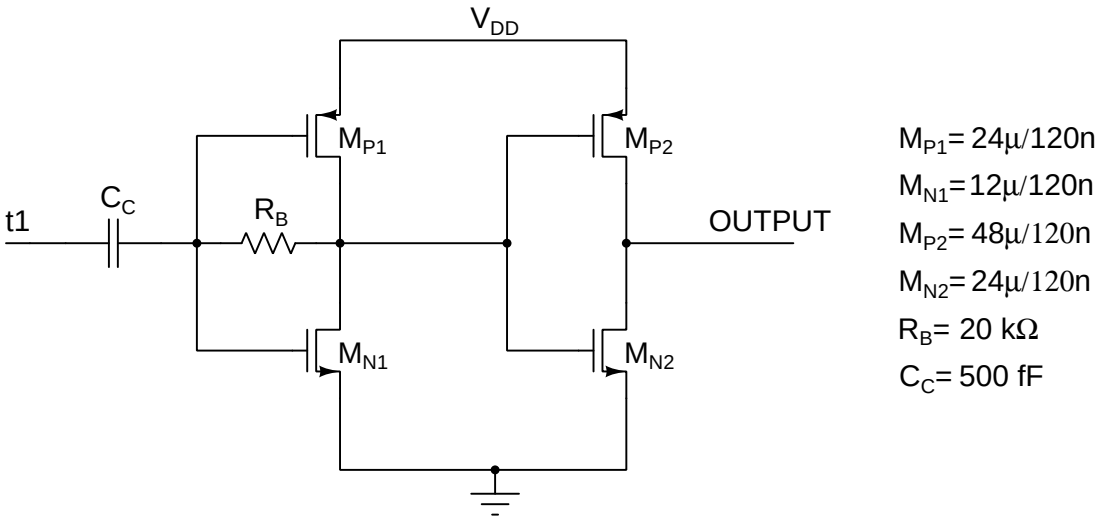


Figure 2.15: Schematic of the voltage buffer.

2.3.4 Layout

The layout of the 114 MHz oscillator is shown in Figure 2.16. Each of the blocks of the Pierce oscillator is highlighted.

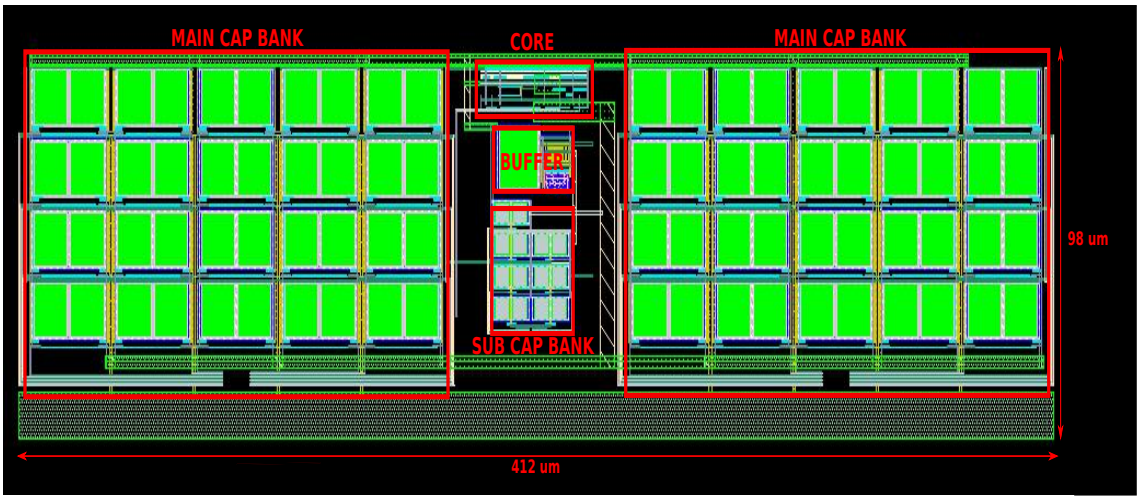


Figure 2.16: Layout of 114 MHz oscillator.

2.3.5 Simulation results

The simulations were done for load capacitances of $2\,\mathrm{pF}$, $3.3\,\mathrm{pF}$, and $4.3\,\mathrm{pF}$. The simulations were done across SS, SF, TT, FS, and FF process corners for $0\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ temperatures. The drive limiting resistor R_{DL} used here was $100\,\Omega$. The simulations were done using hb and hbnoise(sampled jitter) analysis.

Tables 2.4, 2.5 and 2.6 show the results for $2\,\mathrm{pF}$, $3.3\,\mathrm{pF}$, and $4.3\,\mathrm{pF}$ respectively. The worst and the best cases of each parameter are indicated by red and blue colors respectively.

Table 2.4: Results for load capacitance = $2\,\mathrm{pF}$

Corner	**Temperature** ($^{\circ}\mathrm{C}$)	**Core Power** (μW)	**Drive Level** (μW)	**Phase noise**			**Amplitude at T1** (V_{pk-pk})	**Oscillation Frequency** (MHz)
				@1kHz (dBc/Hz)	**@10kHz** (dBc/Hz)	**@100kHz** (dBc/Hz)		
SS	0	**405.3**	**106.2**	-123.7	-143.7	-149.1	**530.8m**	114.316
	80	505.5	97.84	**-124.1**	-143.9	-148.3	500.9m	114.317
FF	0	537.7	72.26	-119.3	-143.6	-148.4	424.6m	114.321
	80	711.5	**63.22**	-120.0	**-142.9**	**-147**	**396.1m**	114.321
TT	0	608.1	65.97	**-119**	-143.7	-149.2	496.2m	114.319
	27	493.9	89.22	-121.5	-144	-149	482.6m	114.319
	80	587.0	83.70	-121.9	-143.7	-148.2	463.9m	114.319
FS	0	547.7	83.95	-120.9	-143.9	-149.1	448.1m	114.319
	80	761.7	76.56	-121.9	-144.3	-148.3	420.2m	114.319
SF	0	563.9	84.86	-121.2	**-144.4**	**-149.6**	447.2m	114.319
	80	**786.3**	75.73	-122.2	-144.2	-148.4	415.3m	114.319

Table 2.5: Results for load capacitance = 3.3 pF

Corner	Temperature (°C)	Core Power (μW)	Drive Level (μW)	Phase noise @1kHz (dBc/Hz)	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Amplitude at T1 (V_{pk-pk})	Oscillation Frequency (MHz)
SS	0	615.9	**141.9**	-127.6	-143.8	-148.8	**511.4m**	114.313
	80	809.2	131.1	**-128.3**	-144.1	-148.2	485.5m	114.313
FF	0	**566.9**	112.6	**-123.0**	-144.5	-149.2	509.1m	114.316
	80	708.2	**100.5**	-123.4	**-143.8**	**-147.8**	479.4m	114.316
TT	0	743.8	125.1	-125.6	-144.4	-149.3	490.1m	114.315
	27	830.3	121.5	-126.0	-144.4	-149.0	480.7m	114.315
	80	**1022**	114.3	-126.4	-144.3	-148.3	463.4m	114.315
FS	0	734.5	124.2	-125.5	-144.5	-149.3	489.6m	114.315
	80	1006	114.9	-126.4	-144.6	-148.6	465.8m	114.315
SF	0	755.0	124.8	-125.8	**-144.8**	**-149.7**	488.5m	114.315
	80	1004	113.3	-126.6	-144.6	-148.6	**460.5m**	114.315

Table 2.6: Results for load capacitance = 4.3 pF

Corner	Temperature (°C)	Core Power (μW)	Drive Level (μW)	Phase noise @1kHz (dBc/Hz)	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Amplitude at T1 (V_{pk-pk})	Oscillation Frequency (MHz)
SS	0	**674.5**	**160.0**	-129.3	**-143.4**	-148.3	474.2m	114.310
	80	862.1	148.4	**-130.1**	-143.6	**-147.6**	**453.1m**	114.310
FF	0	785.4	144.8	**-125.5**	-144.7	-149.1	**507.5m**	114.313
	80	**998**	**130.6**	-125.9	-143.9	-147.8	480.3m	114.314
TT	0	732.1	157.7	-128.1	-144.5	-149.2	500.8m	114.312
	27	796.3	153.5	-128.3	-144.3	-148.8	492.7m	114.312
	80	938.5	144.1	-128.5	-144.0	-148.1	475.7m	114.312
FS	0	723.4	156.3	-128.1	-144.6	-149.3	499.3m	114.312
	80	926.5	144.4	-128.6	-144.4	-148.4	476.9m	114.312
SF	0	740.8	157.5	-128.4	**-144.8**	**-149.6**	499.7m	114.312
	80	951.6	143.0	-128.7	-144.4	-148.5	473.3m	114.312

We can see that the tuning range of the oscillator is 7 kHz at TT(27 °C) when load capacitance is varied from 2 pF to 4.3 pF. The FoM at TT(27 °C) with a load of 3.3 pF is 211 dB. The worst-case FoM is 208.9 dB at FF(80 °C) with 13 pF load.

Figures 2.17 and 2.18 show waveform at t1 and the phase noise plot from PSS simulation for SS(0 °C), TT(27 °C) and FF(80 °C) corners respectively with the load of 3.3 pF.

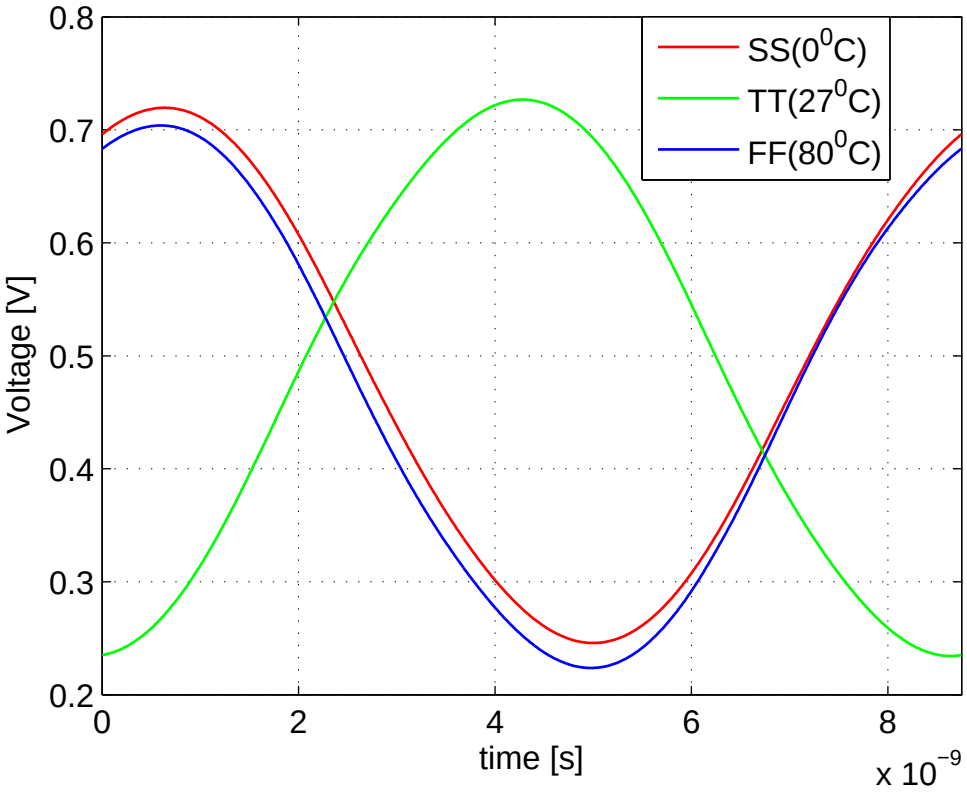


Figure 2.17: Oscillation waveform at t1.

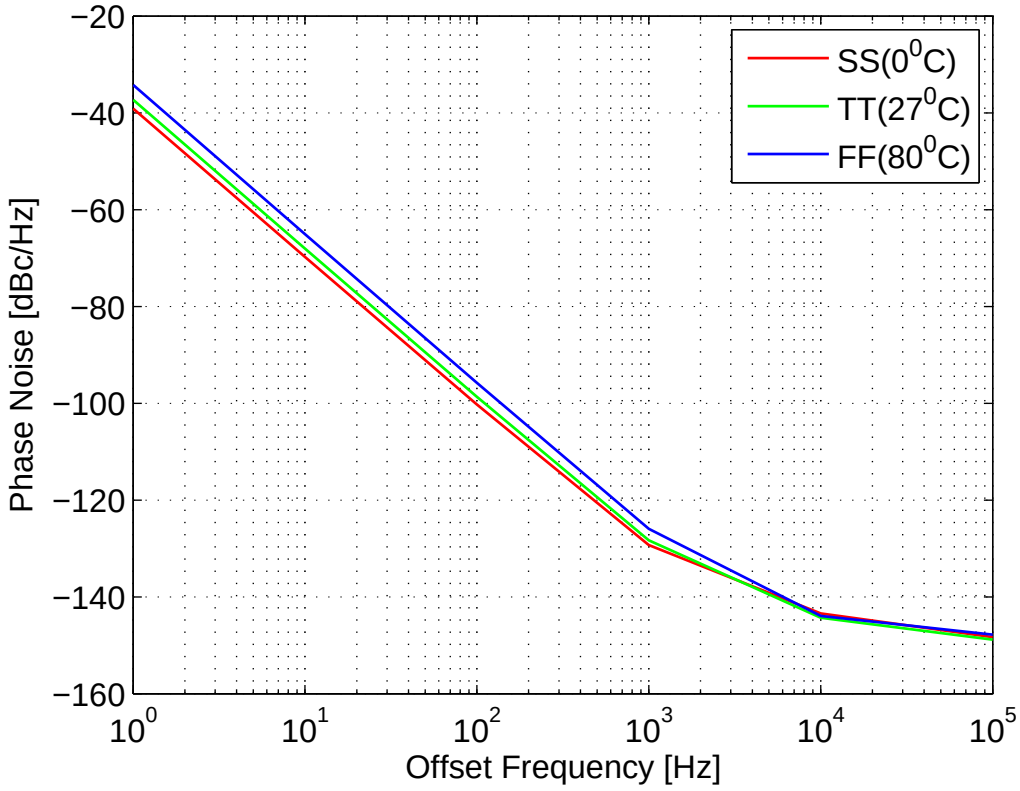
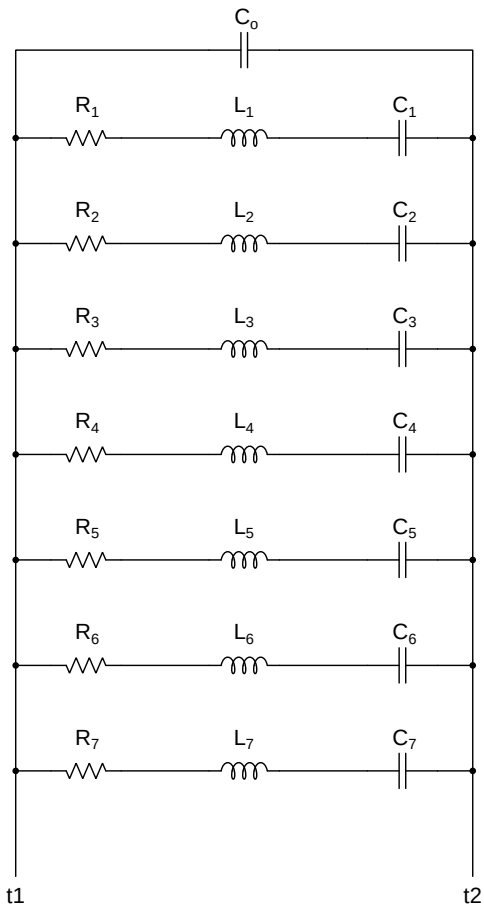


Figure 2.18: Phase noise at the output of the buffer.

2.4 MEMS resonator oscillator

The resonator used here is a MEMS piezoelectric resonator using a process similar to that described in [8]. Its model is shown in Figure 2.19. It is a multi mode resonator which can have multiple frequencies of oscillation. The dominant mode is the first branch which oscillates at a frequency of $991\,\mathrm{MHz}$. The motional resistance of the dominant mode as seen from the figure is $84.37\,\Omega$. The shunt capacitor C_o is $10\,\mathrm{fF}$.



R_1 = 84.3741 Ω L_1 = 51.1529 mH C_1 = 506.07 aF

R_2 = 604.693 Ω L_2 = 301.91 mH C_2 = 80.3301 aF

R_3 = 1.9216 kΩ L_3 = 1.13792 mH C_3 = 20.8479 aF

R_4 = 2.1751 kΩ L_4 = 1.03294 mH C_4 = 25.2544 aF

R_5 = 2.9199 kΩ L_5 = 1.01854 mH C_5 = 25.2161 aF

R_6 = 3.1661 kΩ L_6 = 790.384 µH C_6 = 29.9810 aF

R_7 = 11.734 kΩ L_7 = 3.03652 mH C_7 = 7.9482 aF

C_o = 10 fF

Figure 2.19: Model of the MEMS Resonator.

As seen in Chapter 1 the expression for negative resistance is

$$R_N = \frac{R_B(1+g_m R_{ds})^2+\omega^2 R_B R_{ds}(-g_m R_B R_{ds} C_1 C_2 + R_{ds}(C_1+C_2)^2 + R_B C_1^2)}{(1+g_m R_{ds}-\omega^2 R_B R_{ds}(C_1C_2+C_2C_3+C_1C_3))^2+(\omega R_{ds}(C_1+C_2)+\omega R_B(C_1+C_3(1+g_m R_{ds})))^2}$$

As we can see, R_N inversely depends on the square of frequency. Since the frequency of oscillation is high, getting the required negative resistance needs a very high g_m. If we increase the size of the inverters for getting a higher g_m, R_{ds} will decrease thereby decreasing the negative resistance. But with lower load capacitance, the required nega-

tive can be obtained with reasonable value of g_m.

Here, the values of the variables are taken as R_B = 50 kΩ, R_{ds} = 500 Ω and C_3 = 10 fF. The plot of R_N versus g_m is shown in Figure 2.20 for load capacitance values of 50 fF, 225 fF, and 400 fF.

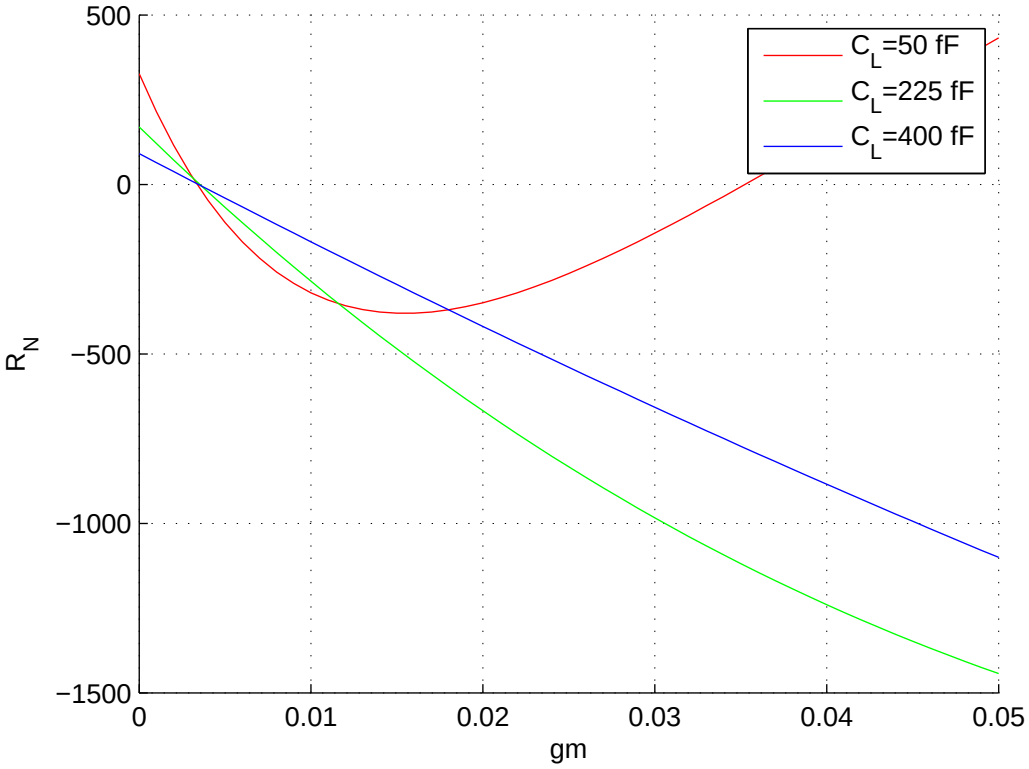


Figure 2.20: R_N versus g_m plot.

2.4.1 Oscillator core

From the plot, we can see that the g_m that we need varies with the load capacitance. It will also vary with process and temperature corners. So the oscillator core is designed to be programmable to obtain various values of g_m. Figure 2.21 shows the schematic of the core. It has self-biased inverters which act as the active component providing the required negative resistance to have sustained oscillations. The sizes of the PMOS and the NMOS transistors are as shown. The first inverter branch of the core has a g_m of approximately 2.7 mS TT 27 °C. The second branch has twice the size of the first branch and hence twice the g_m, i.e. 5.5 mS. The third and the fourth branches have four times the size of the first branch and hence a g_m of 11 mS. The control bits CTL0,1,2,3 are used to switch on and off the four branches. The aim is to have sustained oscillations

by getting the required value of g_m with low power consumption.

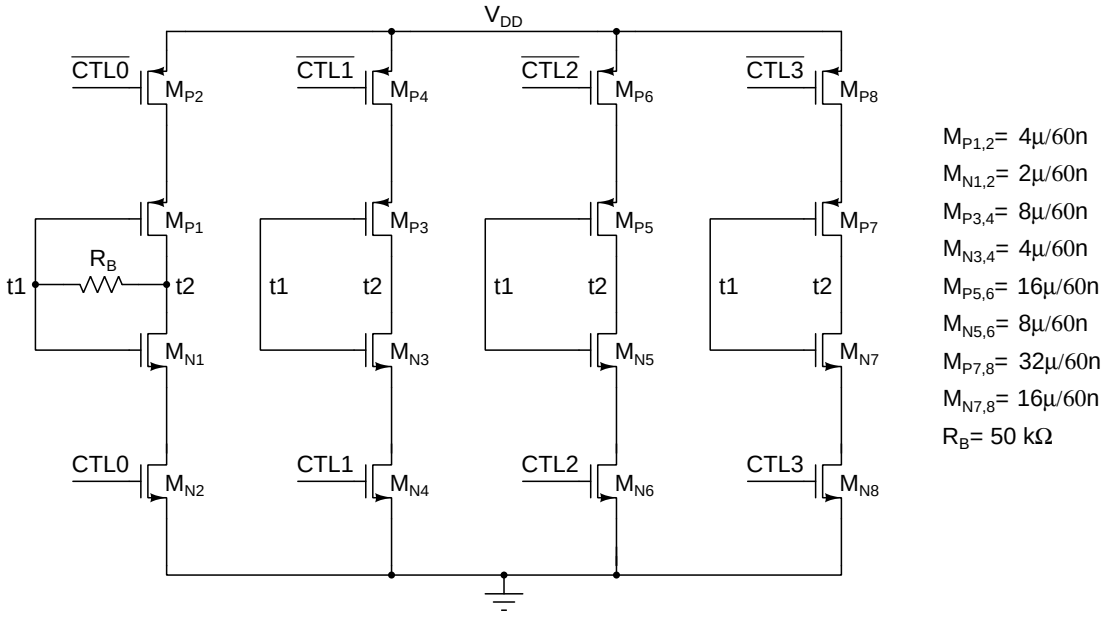


Figure 2.21: Schematic of Oscillator core.

2.4.2 Capacitor bank

The block diagram of the capacitor bank is shown in Figure 2.22. It has 10 instances of the main cap bank unit and 3 instances of sub cap bank unit. The sub cap bank unit is for getting a higher frequency resolution. The value of the sub cap unit capacitance is chosen such that the frequency tuning stays almost linear and there exists a continuity during tuning. So, C_{sub} = $C_{main}/(N+1)$ where N is the number of sub cap units used. Here N=3 and C_{main} = 50 fF. Therefore, C_{sub} = 12.5 fF.

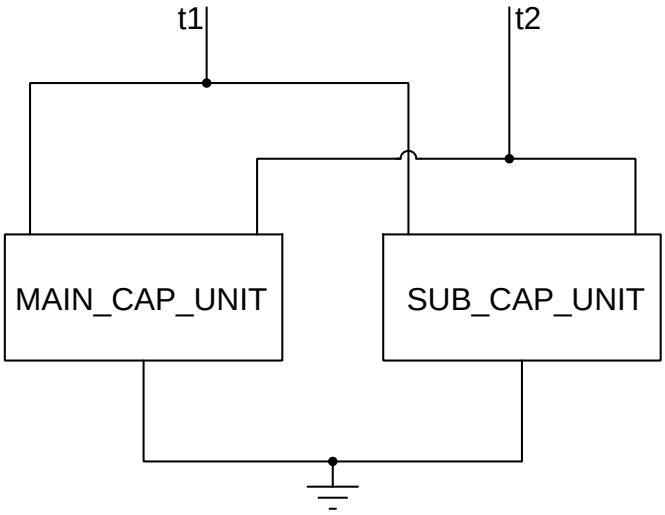


Figure 2.22: Capacitor bank block diagram.

Figure 2.23 shows the schematic of the main cap bank unit. The differential capacitance provided by the unit is $50\,\mathrm{fF}$ at TT $27\,^{\circ}\mathrm{C}$. S is the control signal used to switch the main cap bank unit on and off. M_{N1} and M_{N2} connect the capacitors to ground when S=1. M_{P1} and M_{P2} are used to prevent the NMOSes from getting switched ON when S=0.The transistors are sized such that the quality factor is high in the ON state and the OFF capacitance is low. The worst-case quality factor is 15.84 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $10\,\mathrm{fF}$ (FF $80\,^{\circ}\mathrm{C}$).

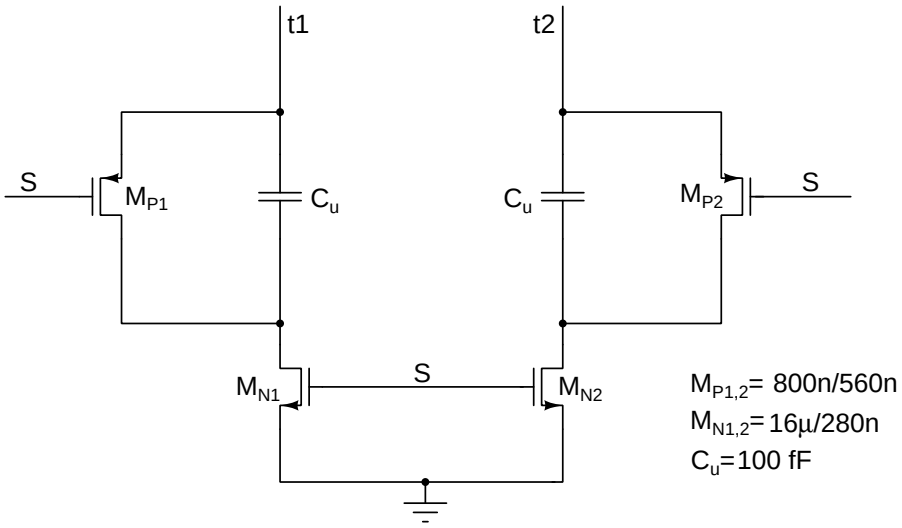


Figure 2.23: Main cap unit.

Figure 2.24 shows the schematic of the sub cap bank unit. The capacitance provided by the unit is $12.5\,\mathrm{fF}$. The worst-case quality factor is 3.27 (SS $80\,^{\circ}\mathrm{C}$) and the OFF capacitance is $1.02\,\mathrm{fF}$ (SS $80\,^{\circ}\mathrm{C}$).

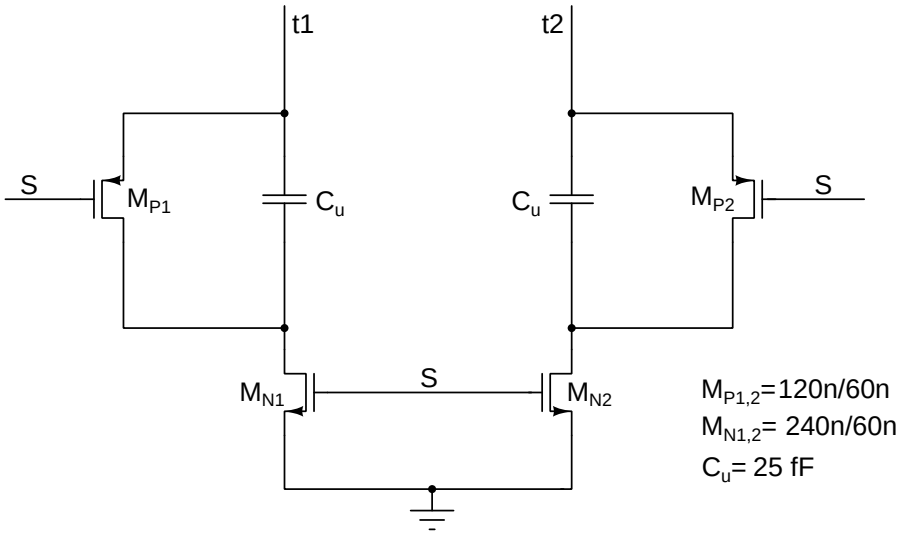


Figure 2.24: Sub cap unit.

2.4.3 Voltage buffer

Figure 2.25 shows the schematic of the voltage buffer. The capacitor C_C is used as the decoupling capacitor. The resistor R_B is used for self-biasing. The transistors are sized such that they provide enough gain and their thermal noise contribution is minimum.

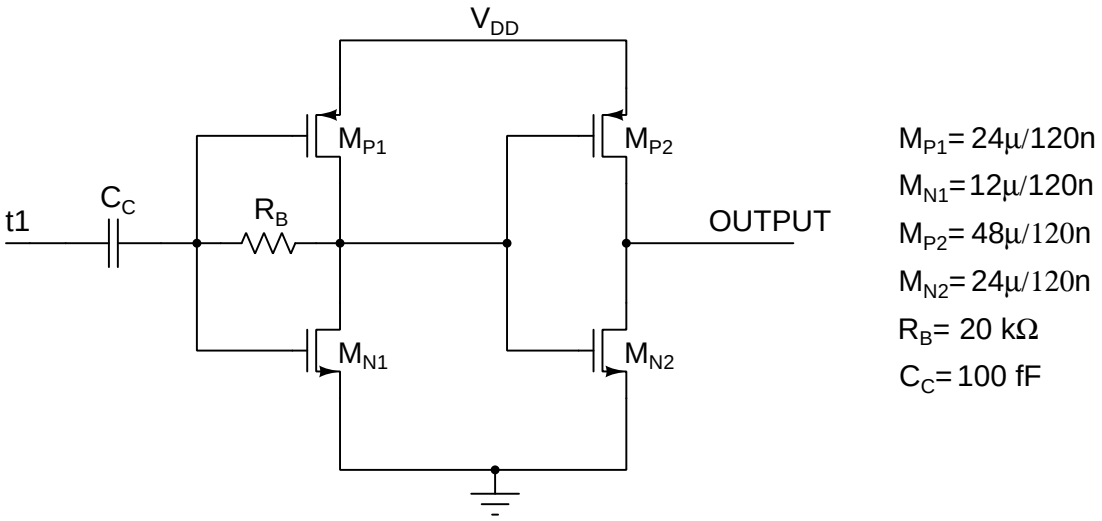


Figure 2.25: Schematic of the voltage buffer.

2.4.4 Layout

The layout of the MEMS resonator oscillator is shown in Figure 2.26. Each of the blocks of the Pierce oscillator is highlighted.

The MEMS resonator has a layout with pads arranged in GSGSG configuration(G-ground, S-signal). So the oscillator will be interfaced with the resonator as shown in Figure 2.27. So a pad frame was designed to facilitate the interface. The pad frame along with the resonator layout in shown in Figure 2.28. The centre to centre spacing between the pads of the resonator is $150\,\mu\mathrm{m}$ and the distance between the pads is $50\,\mu\mathrm{m}$.

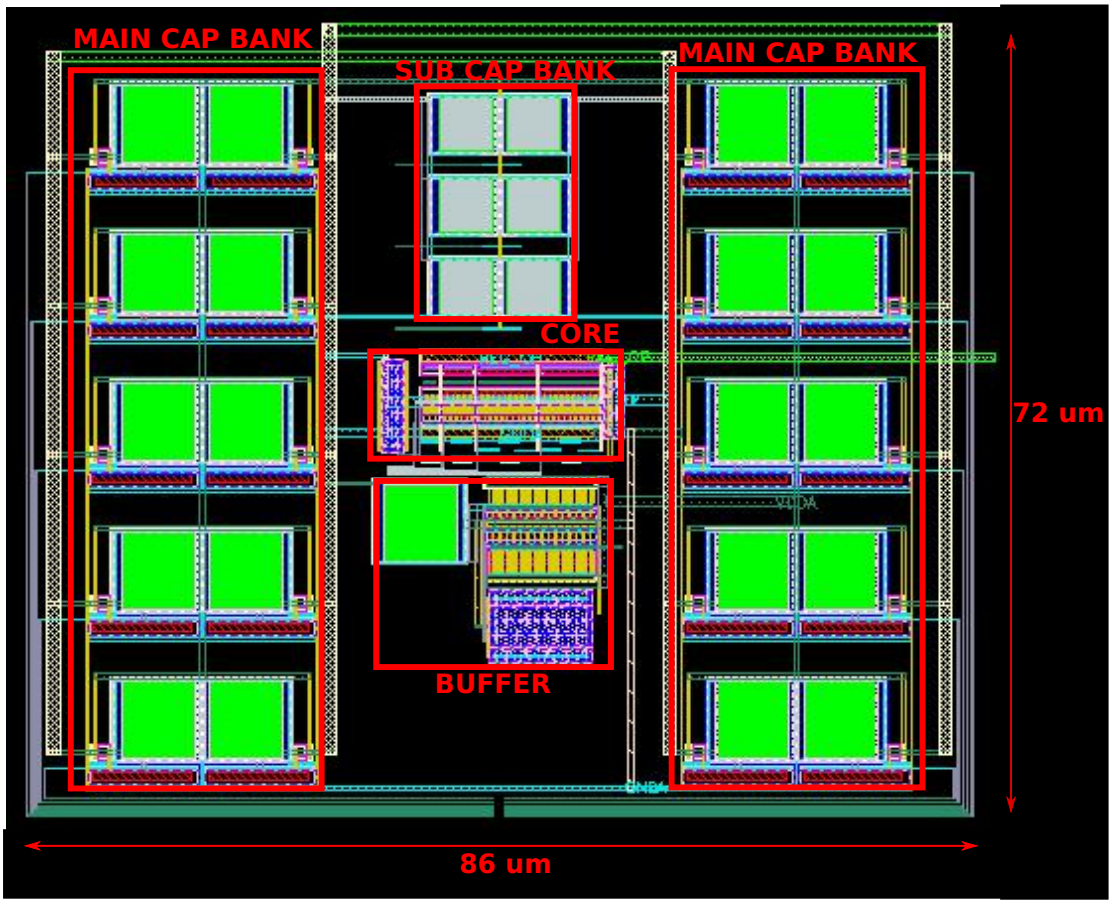


Figure 2.26: Layout of MEMS resonator oscillator.

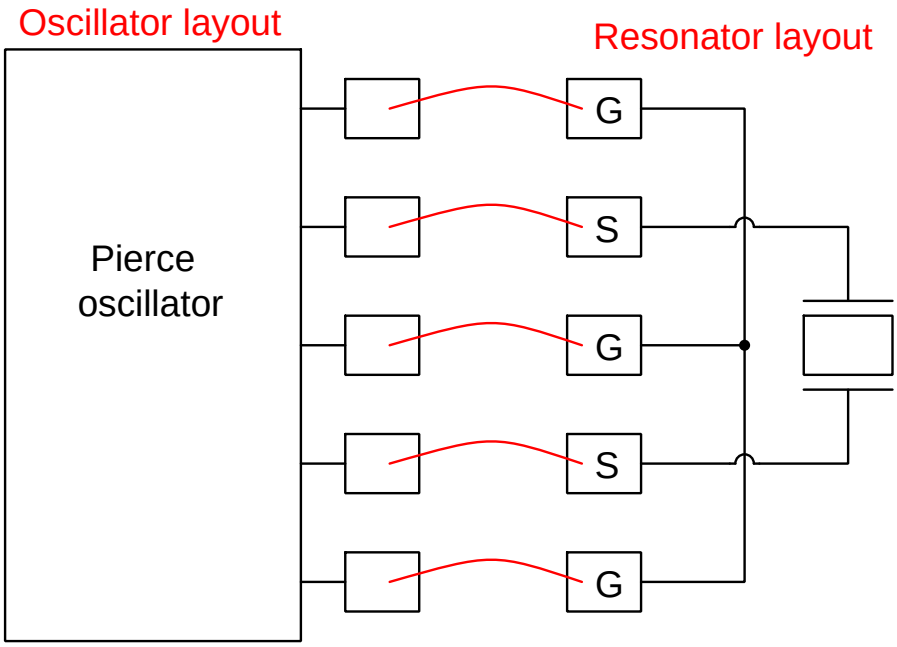


Figure 2.27: GSGSG configuration.

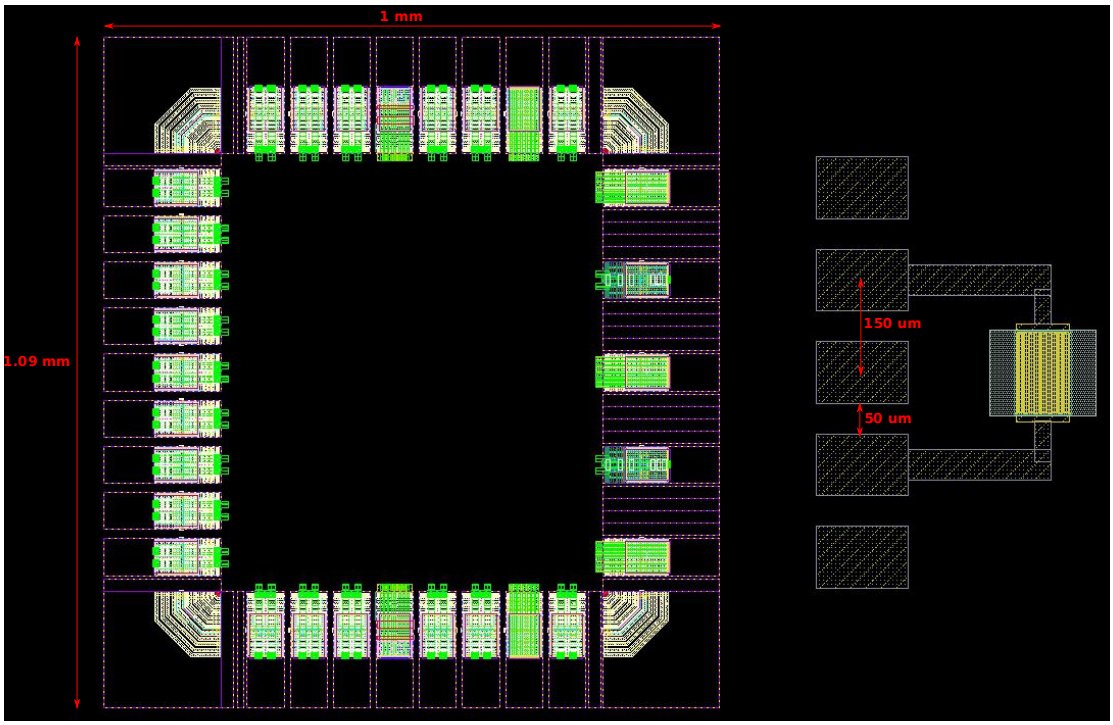


Figure 2.28: Resonator layout along with the pad frame.

2.4.5 Simulation results

The simulations were done for load capacitances of $50\,\text{fF}$, and $400\,\text{fF}$. The simulations were done across SS, SF, TT, FS, and FF process corners for $0\,^{\circ}\text{C}$ and $80\,^{\circ}\text{C}$ temperatures. The drive limiting resistor R_{DL} used here was $100\,\Omega$. The simulations were done using hb and hbnoise(sampled jitter) analysis.

Tables 2.7 and 2.8 show the results for $50\,\text{fF}$ and $400\,\text{fF}$ respectively. The worst and the best cases of each parameter are indicated by red and blue colors respectively.

Table 2.7: Results for C_L = 50 fF

Corner	**Temperature** °C)	**Core Power** (μW)	**Drive Level** (μW)	**Phase noise**			**Amplitude at T1** (V_{pk-pk})	**Oscillation Frequency** (MHz)
				@10kHz (dBc/Hz)	**@100kHz** (dBc/Hz)	**@1MHz** (dBc/Hz)		
SS	0	176	**45.97**	-111.8	-139.4	-149.4	**657.9m**	990.418
	80	217.3	44.63	**-112**	**-139.4**	**-148.7**	633.2m	990.408
FF	0	268.4	32.96	**-108.3**	**-137**	**-150.5**	571.7m	990.533
	80	**329.4**	**30.32**	-109	-137.2	-149.2	**542.1m**	990.503
TT	0	174.9	40.4	-110.6	-138.7	-150.2	631.7m	990.430
	27	186.9	39.82	-110.8	-138.8	-149.9	622.9m	990.423
	80	212.2	38.33	-111.1	-138.8	-149.2	604.6m	990.408
FS	0	**172.2**	38.85	-110.6	-138.7	-150.1	629.1m	990.449
	80	208.5	37.51	-111	-138.7	-149.2	607m	990.426
SF	0	177.6	41.15	-110.5	-138.6	-150	628.6m	990.412
	80	216.5	38.57	-111.1	-138.8	-149	598.8m	990.391

Table 2.8: Results for C_L = 400 fF

Corner	Temperature °C	Core Power (μW)	Drive Level (μW)	Phase noise @10kHz (dBc/Hz)	Phase noise @100kHz (dBc/Hz)	Phase noise @1MHz (dBc/Hz)	Amplitude at T1 (V_{pk-pk})	Oscillation Frequency (MHz)
SS	0	**541.7**	**120.5**	-120.7	**-143.2**	-148.2	459.4m	989.705
	80	700.5	108.2	**-121.5**	-143.6	**-147.4**	**433.4m**	989.719
FF	0	733.6	96.48	**-118**	**-144.4**	**-150.1**	**508.6m**	989.863
	80	**901.7**	**79.29**	-118.3	-143.7	-148.5	460.1m	989.863
TT	0	657.9	117.9	-119.5	-144.3	-149.4	501.8m	989.784
	27	721.4	112.8	-119.8	-144.3	-149	489.9m	989.787
	80	852.8	101.6	-120.2	-144.1	-148.3	464m	989.791
FS	0	647.2	116.6	-119.5	-144.2	-149.4	500.1m	989.784
	80	836.6	101.3	-120.2	-144.1	-148.3	464.6m	989.792
SF	0	669.3	116.4	-119.4	-144.1	-149.2	497.5m	989.784
	80	871.1	99.2	-120.2	-143.9	-148	457.7m	989.791

We can see that the tuning range of the oscillator is 636 kHz at TT(27 °C) when the load capacitance is varied 50 fF to 400 fF. The FoM of at TT(27 °C) with a load of 400 fF is 210.3 dB. The worst-case FoM is 208.8 dB at FF(80 °C) with a load of 400 fF.

Figures 2.29 and 2.30 show waveform at t1 and the phase noise plot from PSS simulation for SS(0 °C), TT(27 °C) and FF(80 °C) corners respectively with the load of 400 fF.

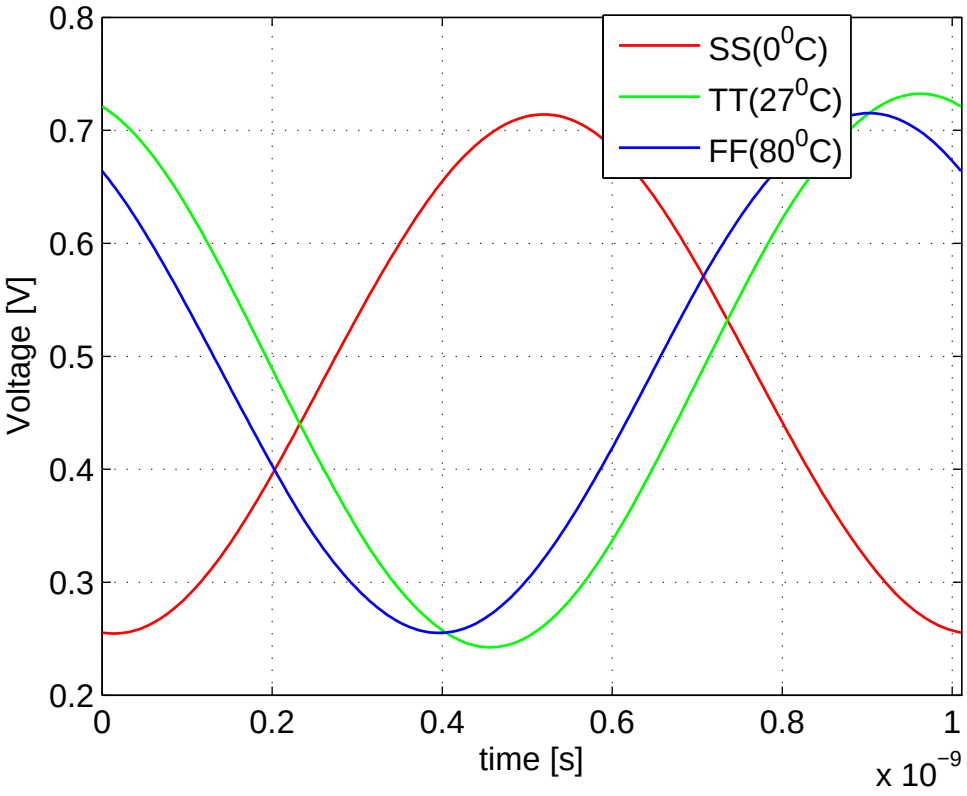


Figure 2.29: Oscillation waveform at t1.

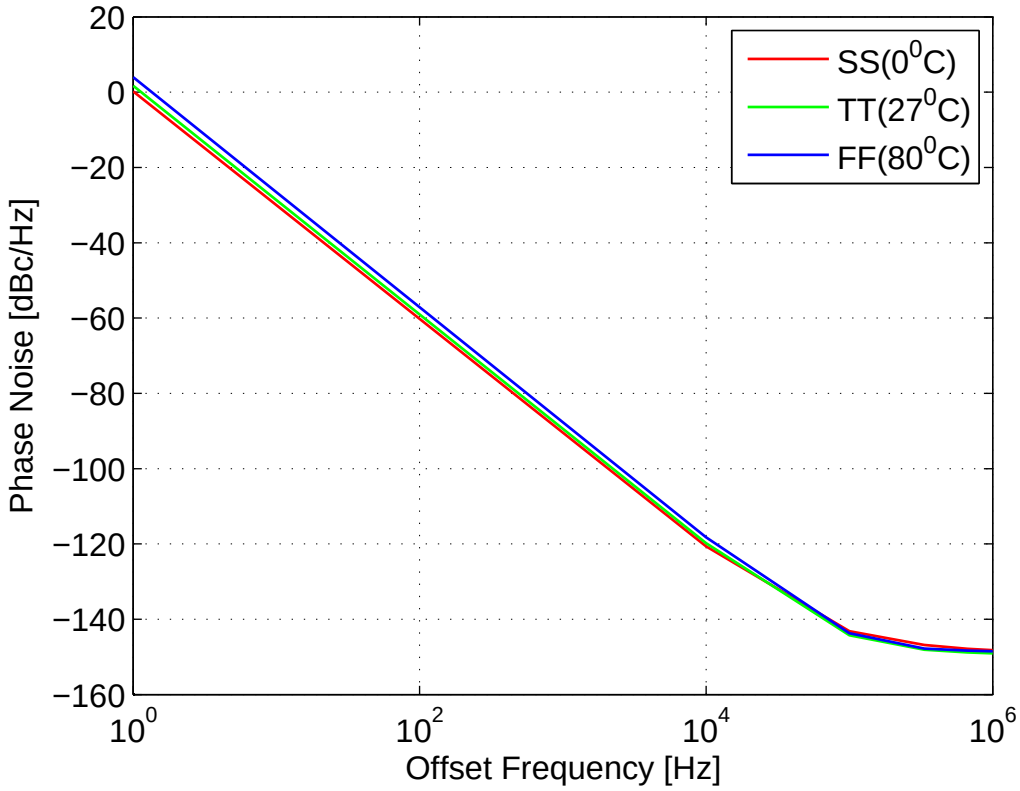


Figure 2.30: Phase noise at the output of the buffer.

Chapter 3

CONCLUSION

Two crystal oscillators of $20\,\mathrm{MHz}$ and $114\,\mathrm{MHz}$, and a MEMS resonator oscillator of $990\,\mathrm{MHz}$ were designed in TSMC 65GP process. The $20\,\mathrm{MHz}$ oscillator simulations were run using the design netlist. Layouts of the $114\,\mathrm{MHz}$ and $990\,\mathrm{MHz}$ oscillators were made and their RC extracted netlists were used for simulations. The nominal simulated results of the oscillators are as shown in Table 3.1. These oscillators can be conveniently used as low phase noise references for frequency synthesizers.

Table 3.1: Nominal simulated specifications.

Parameters	**20 MHz**	**114 MHz**	**990 MHz**
Resonator type	Crystal model [6]	Crystal model [7]	MEMS resonator [8]
Supply voltage	$1\,\mathrm{V}$	$1\,\mathrm{V}$	$1\,\mathrm{V}$
Oscillation Frequency	19.2130 MHz	114.315 MHz	989.787 MHz
Power consumption	$118.5\,\mu\mathrm{W}$	$830.3\,\mu\mathrm{W}$	$721.4\,\mu\mathrm{W}$
Output phase noise	$-151\,\mathrm{dBc/Hz}$ @$100\,\mathrm{kHz}$	$-149\,\mathrm{dBc/Hz}$ @$100\,\mathrm{kHz}$	$-149\,\mathrm{dBc/Hz}$ @$1\,\mathrm{MHz}$
Drive level	$20.2\,\mu\mathrm{W}$	$121.5\,\mu\mathrm{W}$	$112.8\,\mu\mathrm{W}$
Amplitude of Oscillation	$792.7\,\mathrm{mV}$	$480.7\,\mathrm{mV}$	$489.9\,\mathrm{mV}$
Area	NA	4.03 $\times 10^{-2}$ mm^2	6.192 $\times$ 10^{-3} mm^2

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