IIT Madras 5G TestBed

Testing of Transmitter Chain, Data Recorder and Accessing of PS RAM

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ABSTRACT

The report explains three tasks/projects related to on and off chip memory utilization in Xilinx FPGA device. In the first task, a hardware debugging approach for testing 5G transmitter chain is discussed in which IPs that are malfunctioning has to be identified. The approach proposed was to divide the chain into two, test the target part, if not faulty divide the chain into new parts with additional IP in the target part and repeat. The hardware implementation results are discussed and the limitation of such approach is presented.

In the second task, a debugging approach is discussed for hardware systems for which the data generated on hardware needs to be analyzed. If the data needed to capture is larger, xilinx debugging IPs like ILA and system ILA cant be used. So, a design to capture data from a target IP in PL and then storing it in the DDR SDRAM is proposed. This RAM exists off the chip. DMA is made use of in the design for the movement of data. The design was developed and then implemented in hardware and the results are presented.

In the third task, the design to store the critical data generated in the PL into the PS DDR and to retrieve the same data back into PL when needed, is discussed. Also the performance of zynq Ultrascale+ was done to assess the throughput possible. For the purpose of this design, two custom IPs were developed. One to source and the other to sink the data in the PL. This design also makes use of DMA for the movement of data. The design was implemented in the hardware successfully and its results are presented.

*Only title page and abstract have been uploaded to maintain confidentiality of information related to 5G testbed. Full report have been submitted to Project guide.