Design of a 5 GHz VCO and PLL for Clocking a Delta-Sigma ADC

A Project Report

submitted by

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in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JULY 2020

THESIS CERTIFICATE

This is to certify that the thesis titled **Design of a 5 GHz VCO and PLL for Clocking a Delta-Sigma ADC**, submitted by **KRISHN KUMAR**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 1st August 2020

ACKNOWLEDGEMENTS

Foremost, I would like to express my sincere gratitude to my mentor Dr. Nagendra Krishnapura for his excellent guidance and continuous support throughout my project, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of my project and writing of this thesis. Despite his hectic schedule he was always approachable and took his time to discuss the problems and give advice and suggestions. Weekly meetings with him were the best and kept me motivated for my work. I would like to appreciate him for his teaching style. It is so wonderful that one will get motivated to work under him. It is an immense pleasure for me to work under his mentorship. I would like to appreciate him for being so gentle with every student of him. I could not imagine having a better mentor than him for my project.

I would like to express my sincere gratitude to Aditya Narayanan for his continuous support during the course of the project. Despite the busy schedule of his Ph.D. work, he has always helped me and cleared my doubts. He helped me to enhance my knowledge about RF circuits and cadence tools. Without his help, I would not have finished my work on time. I would like to thank Rohit Goel for his support in the layout. I would like to thank Ashwin, Chithra, Naveen, Aswani, Ashish for their supports. I would also like to thank my friend Jose Sebastian and Mahabaleshwar Bhat for their time to time discussions with me to clear the concepts.

Finally, I am extremely grateful to my parents for their love, prayers, caring and sacrifices for educating and preparing me for my future. Without their support, I would not have reached here.

ABSTRACT

KEYWORDS: VCO; LDO; Divider; PFD; Charge Pump; PLL.

This project involves the design of a clock generator for a delta-sigma ADC with an output frequency of $2.55\,\mathrm{GHz}$ to $2.65\,\mathrm{GHz}$. A PLL with double the required frequency is used and the output is divided by 2 to generate the output clock. The phase noise specification is -111 dBc/Hz at $2\,\mathrm{MHz}$ offset. The architecture used is CMOS voltage biased VCO. A 3-Bit programmable tail resistor bank is used to control the current variation in the VCO core across corners. A 4-bit programmable capacitor bank is used to achieve the required tuning range across all corners and temperature. The VCO is powered by a $1\,\mathrm{V}$ low noise LDO.

The VCO is used in a phase-locked loop with a divider, PFD, charge pump and a loop filter to generate a fixed frequency of $5.144\,\mathrm{GHz}$ (which will become $2.57\,\mathrm{GHz}$ after division by 2) to drive a High speed $2.57\,\mathrm{GHz}$ ADC. The divider is using a cascade of 5 TSPC Latches arranged in a chain fashion. The PFD is a three-state Phase frequency detector circuit that resets its states when both the outputs become high. The Loop filter is a 2nd order type-I LPF.

The PLL reference frequency is $114.314\,\mathrm{MHz}$. It consumes $3\,\mathrm{mW}$ of power in TT $27\,^{\circ}\mathrm{C}$ and achieves the phase noise of $-117.8\,\mathrm{dBc/Hz}$ at $2\,\mathrm{MHz}$ offset. The design has been done in the TSMC $65\,\mathrm{nm}$ GP process and it occupies an area of $0.2\,\mathrm{mm}^2$.

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ABBREVIATIONS

IITM	Indian Institute of Technology, Madras
VCO	Voltage Controlled Oscillator
PLL	Phase-Locked Loop
PFD	Phase Frequency Detector
PN	Phase noise
Q	Quality-Factor
BW	Bandwidth
PSRR	Power Supply Rejection Ratio

CHAPTER 1

INTRODUCTION

1.1 Motivation

The clock is one of the important requirements for the operation of digital or semi-digital circuits. These clocks are generated by oscillators and require a PLL circuit to have a stable frequency. In this work We have studied different architectures of VCO; then, a VCO of frequency range $5.1\,\mathrm{GHz}$ to $5.3\,\mathrm{GHz}$ and an Integer-N PLL are designed in the TSMC $65\,\mathrm{nm}$ GP process.

1.2 Performance parameters of oscillators

Frequency Range: An RF oscillator must be designed such that its frequency can be varied (tuned) across a certain range.
Output Voltage Swing: They must produce sufficiently large output swings to ensure nearly complete switching of the transistors in the subsequent stages.
Drive Capability: Oscillators may need to drive a large load capacitance offered from the subsequent stages.
Phase noise: The spectrum of an oscillator in practice deviates from an impulse and is broadened by the noise of its constituent devices which is termed as "phase noise".
Supply Sensitivity: The frequency of an oscillator may vary with the supply voltage, an undesirable effect because it translates supply noise to frequency (and phase) noise.

1.3 Basic principles of oscillators

An oscillator is a system that produces periodic output with a self-sustaining mechanism. It allows its noise to grow and eventually becomes a periodic signal. Usually, for higher frequencies, we prefer LC oscillators. The reason is it has a lower phase noise.

However, there is one disadvantage that the inductor consumes a large area on the chip. For a circuit to have self-sustained oscillation it must satisfy the Barkhausen's criterion. According to this criterion to have self-sustained oscillation at a frequency ω_1, the loop gain must be unity with a phase of 360 at ω_1.

Let's analyze the following circuit:

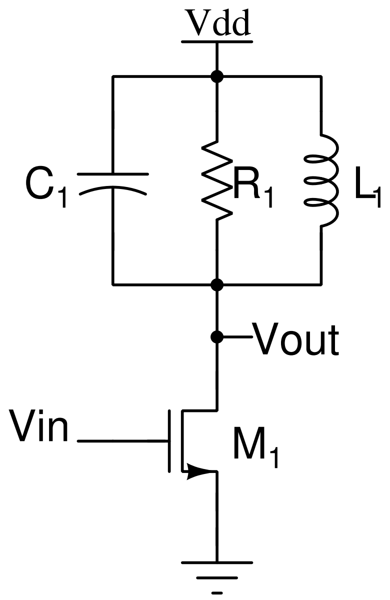


Figure 1.1: Single-stage tuned amplifier.

At low frequency, inductor L_1 will dominate. So,

$$\frac{V_{out}}{V_{in}} = -G_m L_1 s$$

At this frequency, the gain is very small with a phase of $-90°$.

At resonance, R1 will dominate. So,

$$\frac{V_{out}}{V_{in}} = -G_m R_1$$

At this frequency, the gain is larger than 1 with a phase of $-180°$.

At higher frequency, the capacitor will dominate. So,

$$\frac{V_{out}}{V_{in}} = -G_m/sC_1$$

Here again, the gain becomes very small with a phase of +90°.

But we need a phase of $360°$ at resonance. We can achieve this by adding an extra stage shown below:

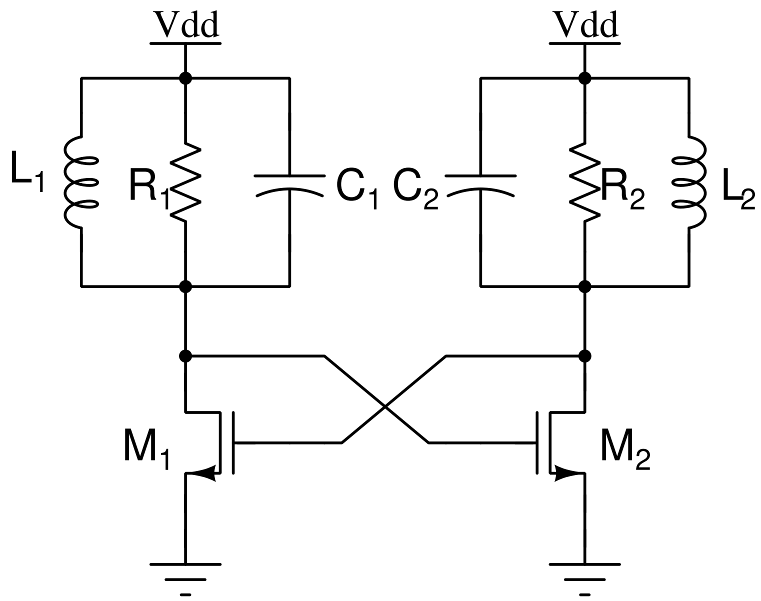


Figure 1.2: Cascade of two tuned amplifiers.

Here at resonance, we will get a loop gain of $(G_m R_1)^2$ and phase of $360°$. The circuit will oscillate if $(G_m R_1)^2 \geq 1$ i.e loop gain ≥ 1.

1.4 Phase noise of VCO

Ideally, an oscillator output must be a perfectly periodic sinusoidal signal in the form of $x(t) = A\cos(\omega_c t)$ with zero crossings at exact integer multiples of $2\pi/\omega_c$. However, in reality, the noise of the oscillator randomly changes the zero crossing instants of $x(t)$. This random variations can be modeled as a random phase shift in the $x(t)$ and given by $x(t) = A\cos(\omega_c t + \phi_n(t))$ where $\phi_n(t)$ is called as phase noise. If we consider $\phi_n(t) \ll 1$ then the above equation can be simplified as $x(t) \approx A\cos\omega_c t - 2A\phi_n(t)\sin\omega_c t$. So, the spectrum of $\phi_n(t)$ is translated to ω_c.

The Leeson's formula for phase noise is given by [3]

$$L(\triangle\omega) \propto \frac{1}{A^2}\frac{kT}{C}\frac{\omega_o}{Q}\frac{1}{\triangle\omega^2} \tag{1.1}$$

Where,

$L(\triangle\omega)$: Phase noise at an offset frequency of $\triangle\omega$.

A: Amplitude of oscillation.

Q: Quality factor.

ω_o: Frequency of oscillation.

C: Equivalent capacitance of tank.

k: Boltzmann's constant.

T: Temperature in kelvin.

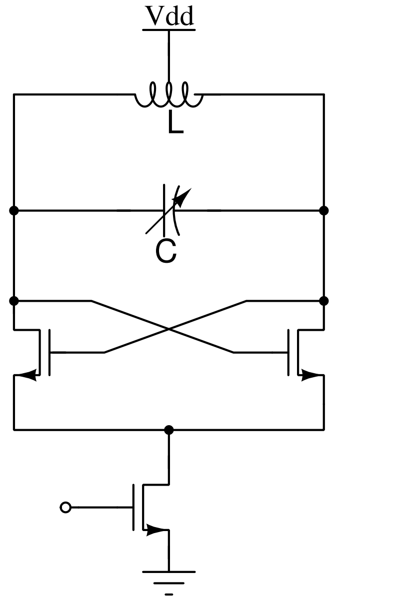
Here we can see that the phase noise $L(\triangle\omega)$ is inversely proportional to quality factor(Q) and A^2. So, we can reduce the phase noise by increasing Q and A. But the quality factor is limited by the inductor's quality factor which is fixed for a tank. Hence, to reduce the phase noise more power needed to be burnt.

CHAPTER 2

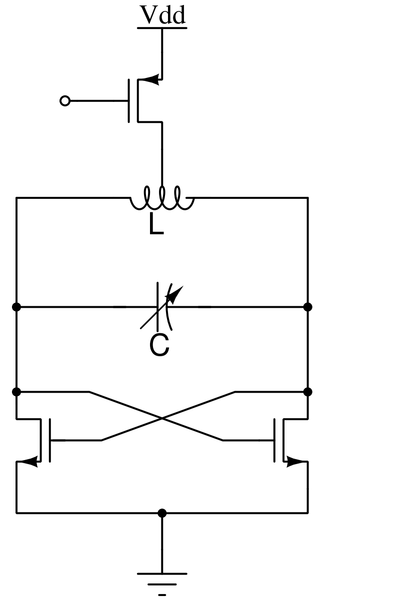
VCO ARCHITECTURE AND DESIGN

2.1 VCO architecture

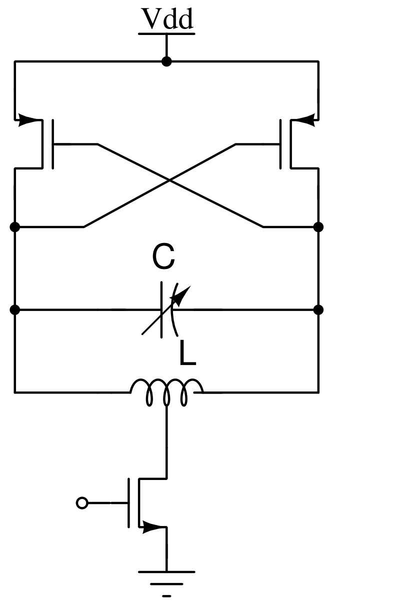
From Leeson's formula, we can see that there is a direct trade-off between phase noise and power consumption of the VCO. For a given process quality factor will be fixed, So, we can reduce the phase noise by increasing the amplitude of oscillator output i.e. burning more power. But simultaneously we also need to keep in mind that we require a VCO which achieves a good phase noise with as minimum power consumption as possible. There are several architectures proposed in the literature. Some of them include current biased VCOs and voltage biased VCOs with NMOS (or PMOS) cross-coupled pair. In current biased VCOs, there will be either a PMOS current source at the top or an NMOS current source at the bottom. This current source contributes a considerable amount of phase noise to the VCO. So, if that noise is a concern then we go for voltage biased VCOs. However, NMOS (or PMOS) only configuration doesn't have the best output swing. We can improve the output swing by using a CMOS cross-coupled architecture. It reuses the current, hence provides double the amplitude of that of an NMOS or PMOS only VCO. In voltage biased VCO current changes across corners. Hence to maintain a required current across corners this topology comes with a programmable tail resistor.



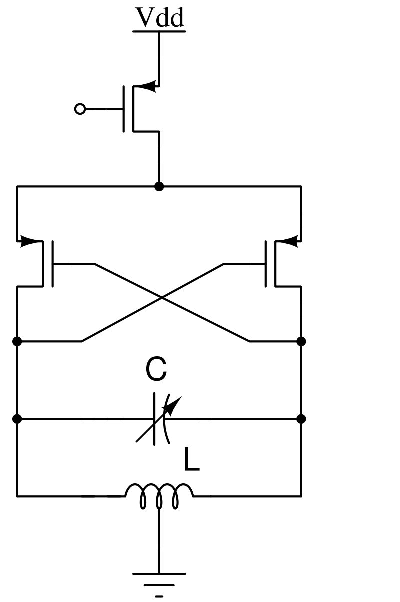
(a) NMOS cross-coupled with NMOS current source.



(b) NMOS cross-coupled with PMOS current source.



(c) PMOS cross-coupled with NMOS current source.



(d) PMOS cross-coupled with PMOS current source.

Figure 2.1: Different current biased VCO architectures.

2.2 Voltage Biased VCO

This architecture consists of a CMOS cross-coupled pair along with a programmable 3-bit tail resistor bank. It is powered by a 1V low noise on-chip LDO because the supply rails are noisy and degrade the phase noise of the VCO. The LDO converts 1.2V to 1V with low noise and high PSRR.

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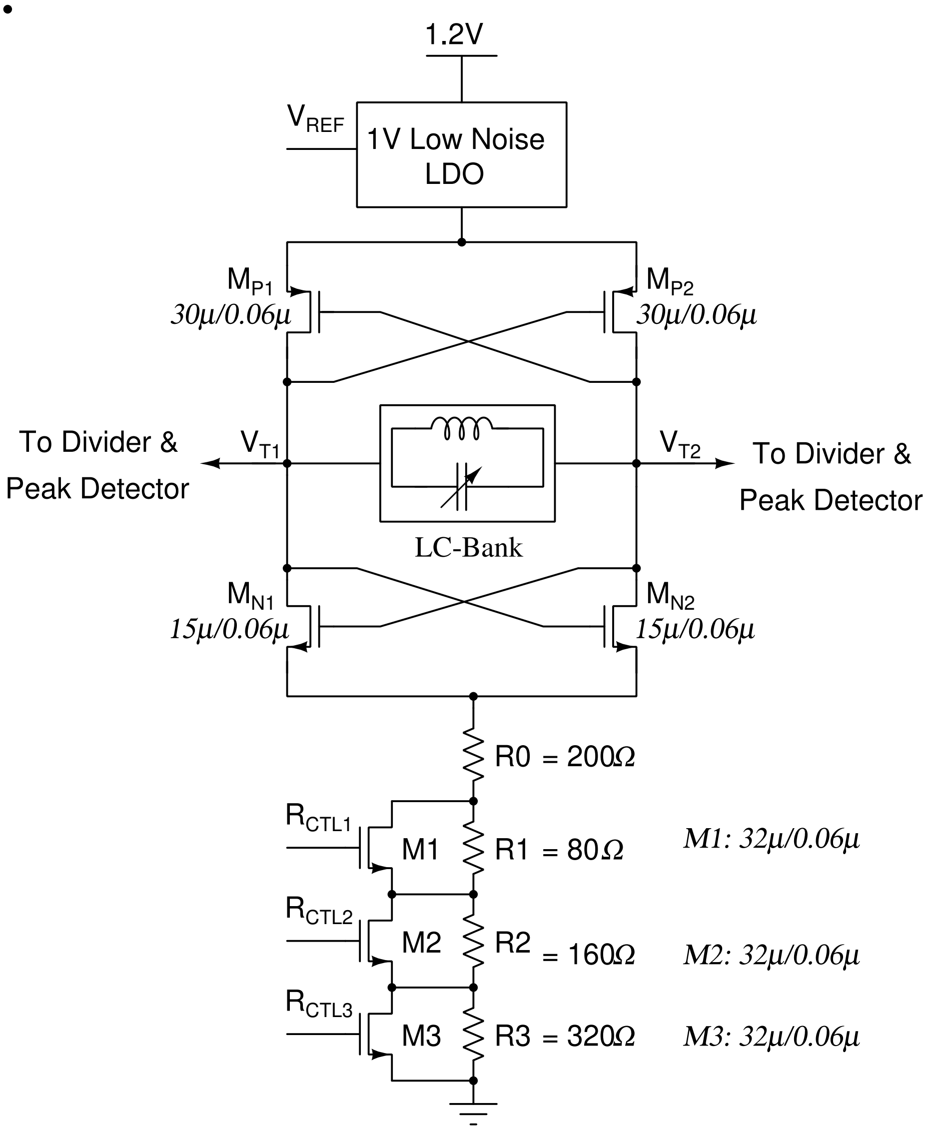


Figure 2.2: Voltage biased VCO.

2.3 VCO Design

2.3.1 Choice of Inductor

From Leeson's formula, we can see that to achieve a good phase noise with minimum power consumption we need to increase the quality factor of the tank as much as possible. The total quality factor of the tank is dominated by the inductor because capacitors generally have a much larger quality factor. So, we try to maximize the quality factor of the inductor. Here we have used an inductor with 3 turns and spacing of $4\,\mu\text{m}$ between the turns.

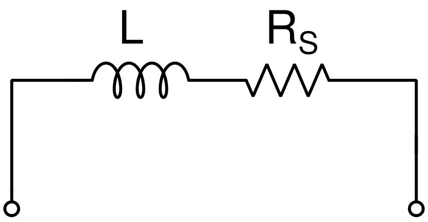


Figure 2.3: Lossy inductor with series loss resistance.

R_s is the series loss resistance of the inductor. If Q_L is the quality factor of inductor then R_s can be written as

$$R_S = \frac{\omega_0 L}{Q_L} \tag{2.1}$$

The parallel loss resistance of inductor can be written as

$$R_P = \omega_0 L Q_L \tag{2.2}$$

A higher value of the inductor will lead to higher R_P. Which will eventually increase the output swing. Thus we will require lesser power to achieve the same phase noise specification. A Large inductor consumes more space on the chip. If we use a large inductor then we will need to use a smaller capacitor. The use of a smaller capacitor might create a problem when parasitics will start to dominate. So, for our case, we chose the value of inductance is $1.77\,\text{nH}$ with a quality factor of 21.4 at a frequency of $5\,\text{GHz}$.

2.3.2 Capacitor bank

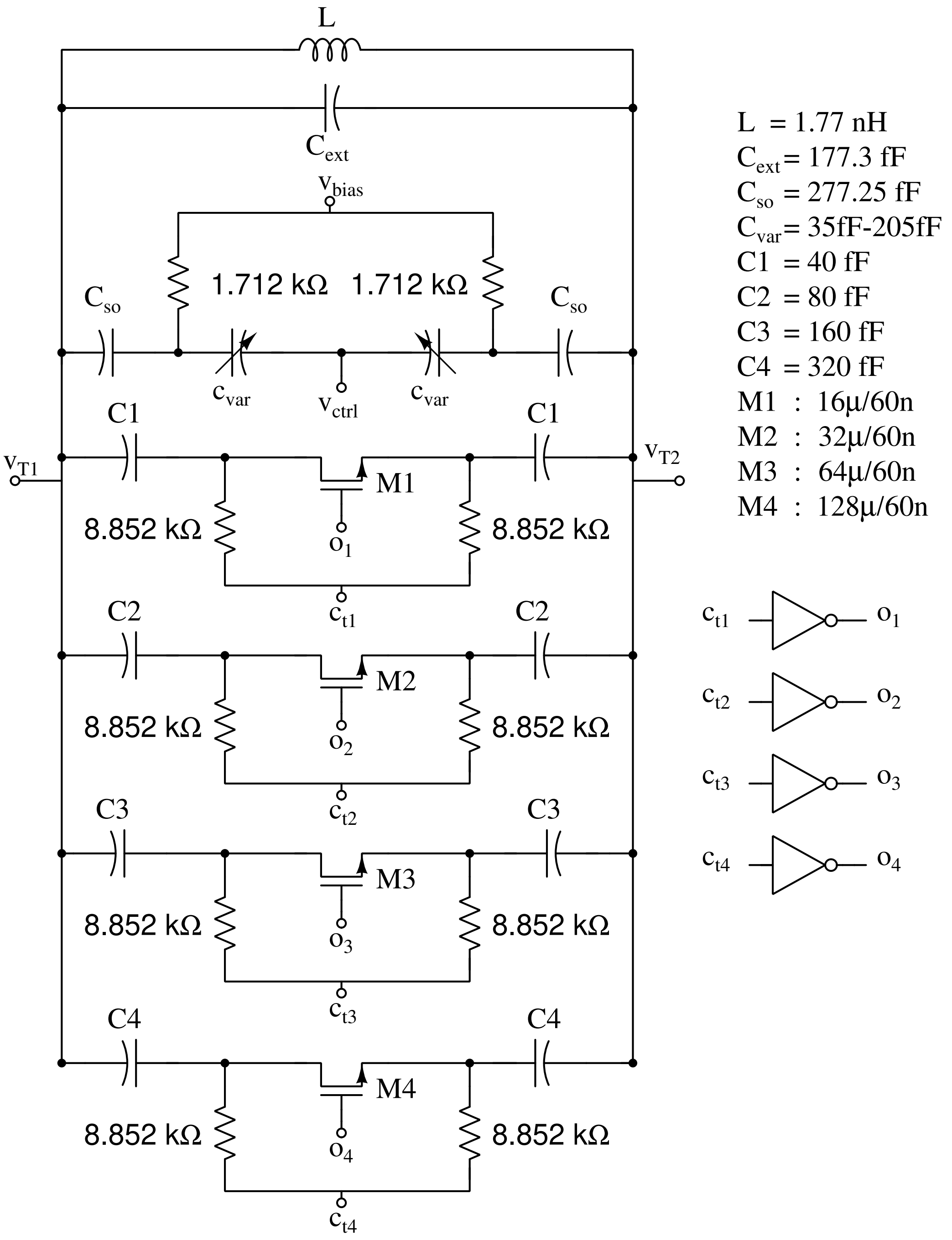


Figure 2.4: Capacitor bank.

The capacitor bank consists of a varactor and 4-bit programmable capacitor bank. Programming is achieved with the help of MOS switches. A fixed capacitor C_{ext} of value $177\,\mathrm{fF}$ is also used which determines the frequency of VCO when the capacitor bank is off. MOS switches should be sized higher so that it offers least on-resistance and thus better quality factor of the bank.

Because the quality factor of the capacitor is given by

$$Q_C = \frac{1}{\omega_0 RC} \tag{2.3}$$

Where R is the series resistance of the capacitor.

But large MOS also have more parasitics(C_{gd} and C_{gs}), which may lead to AM to PM conversion and thus phase noise degradation. We chose the sizes so that MOS parasitics are 10 times smaller than the single side capacitor of a branch in the off state. The capacitor Bank is used for tuning the VCO. Varactor is used for fine-tuning and a 4-bit programmable capacitor is used for coarse tuning such that the required frequency band should be covered in all corners.

The quality factor of the tank is given by

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{2.4}$$

Where Q_L and Q_C are quality factors of the inductor and capacitor bank respectively.

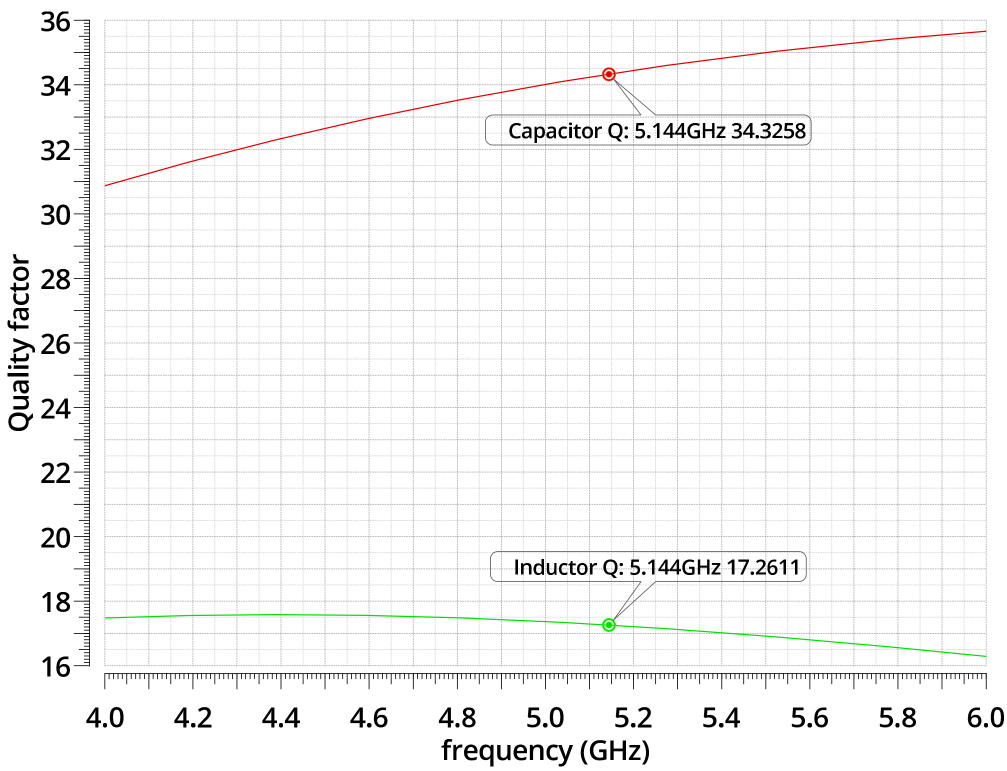


Figure 2.5: Q-factor plot of inductor and capacitor bank.

Quality factors are calculated using the SP analysis. Z-parameter is measured. Then Quality factor will be the ratio of the imaginary part to the real part of the Z_{11}. The worst-case Q_C and Q_L are found to be 34.2 and 17.3 respectively at $5.15\,\mathrm{GHz}$ in SS corner $80\,°\mathrm{C}$. So, the worst case Q_{tank} will be 11.5.

2.3.3 Negative Resistance

All inductors and capacitors are lossy and come with a resistive part also called loss resistance. This loss resistance is responsible for the oscillation to die out after some time. We need to cancel out this loss to have a sustained oscillation. A negative resistance circuit is used to do this. In our case, we are using a CMOS cross-coupled pair. The negative resistance R_N must be lesser than the loss resistance R_P of the tank so that equivalent resistance is still negative. In our case tank parallel resistance is R_P = $1.193\,\mathrm{k\Omega}$.
Negative resistance is given by

$$R_N = \frac{2}{g_{mn} + g_{mp}} \tag{2.5}$$

Where g_{mp} = $2.328\,\mathrm{mS}$ and g_{mn} = $2.613\,\mathrm{mS}$ measured in SS corner where the current will be minimum. Therefore R_N = $404\,\Omega$. This cancels the tank loss by a sufficient margin.

2.3.4 Tail Resistance

Due to the absence of a bias current source in voltage bias VCO, the current will vary across corners and temperature. To maintain the defined current across corner we use a 3-bit programmable tail resistor bank. It consists of a fixed resistance R_0 = $200\,\Omega$ and three programmable resistors R_1 = $80\,\Omega$, R_2 = $160\,\Omega$ and R_3 = $320\,\Omega$.

2.4 Peak detector circuit

2.4.1 Need for peak detection

The current in the VCO core varies across the corners and so does the output swing. We will detect the differential output swing using a peak detector and when the detected peak is greater than 1V, we will fix that current by programming the resistor bank. Therefore, we can save power by limiting the swing to near about 1V.

2.4.2 Design of peak detector

VCO differential output is applied through coupling capacitors to the input of a differential NMOS pair. NMOS pair is biased at V_{Drive} = $470\,\mathrm{mV}$. This bias voltage may change across corners if generated using a simple voltage divider. Therefore we use a replica bias scheme, which uses a large gain OPAMP in a negative feedback loop to fix the bias voltages independent of corner variation. When VCO output is applied to NMOS pair, NMOS current changes, and therefore to adjust the current change tail node voltage across NMOS M_1 and M_2 also change until the current in NMOS pair becomes equal to the current in tail transistors M_1 and M_2. The average increase in tail node voltage is half times the single-ended peak voltage of VCO output. This voltage is applied to a comparator to generate the logic level.

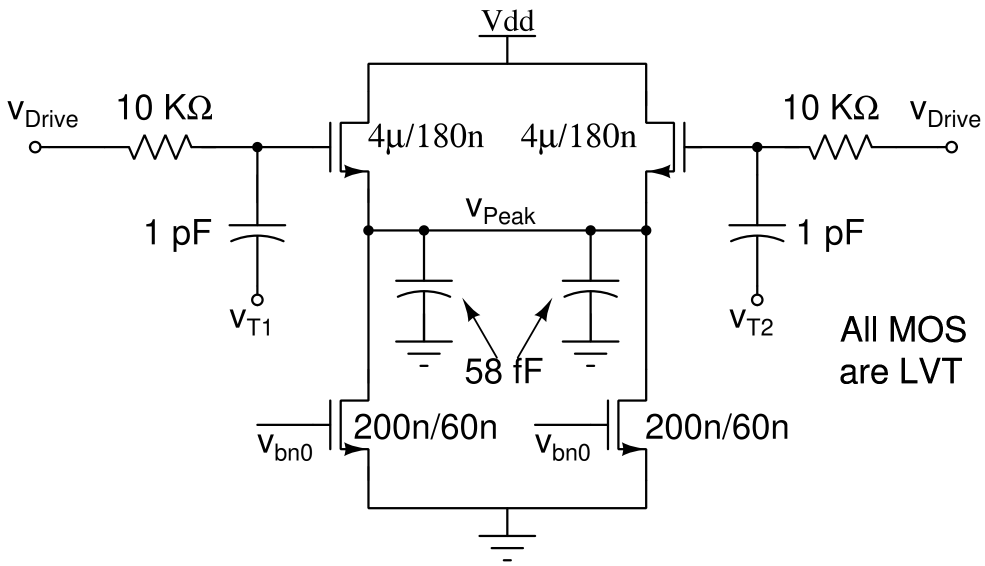


Figure 2.6: Peak detector circuit.

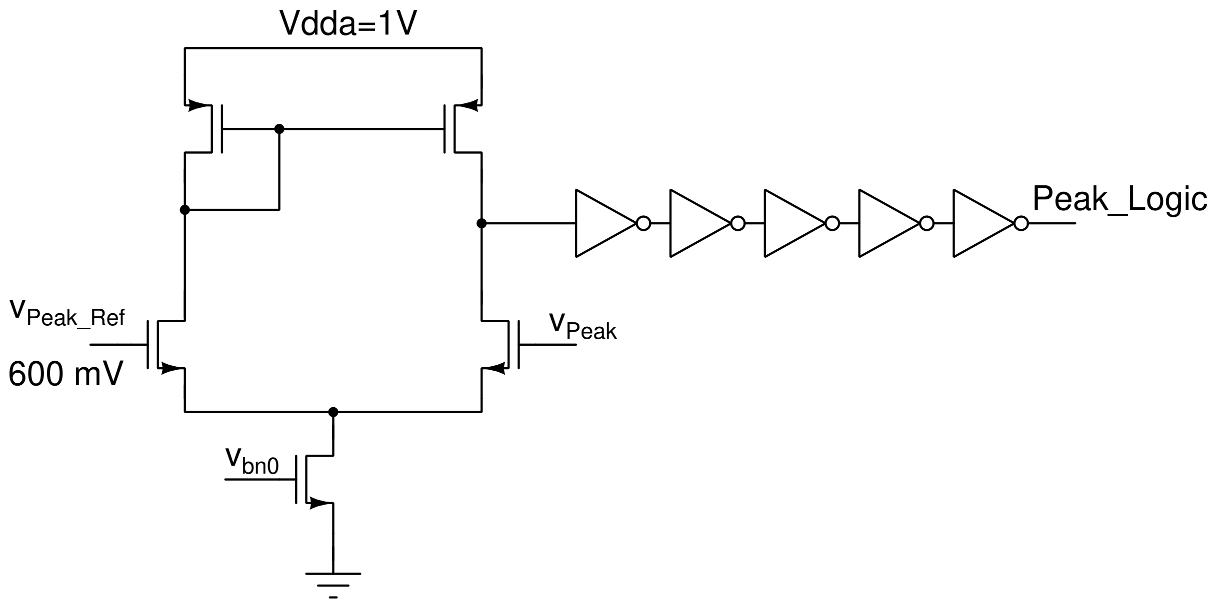


Figure 2.7: Peak detector Logic.

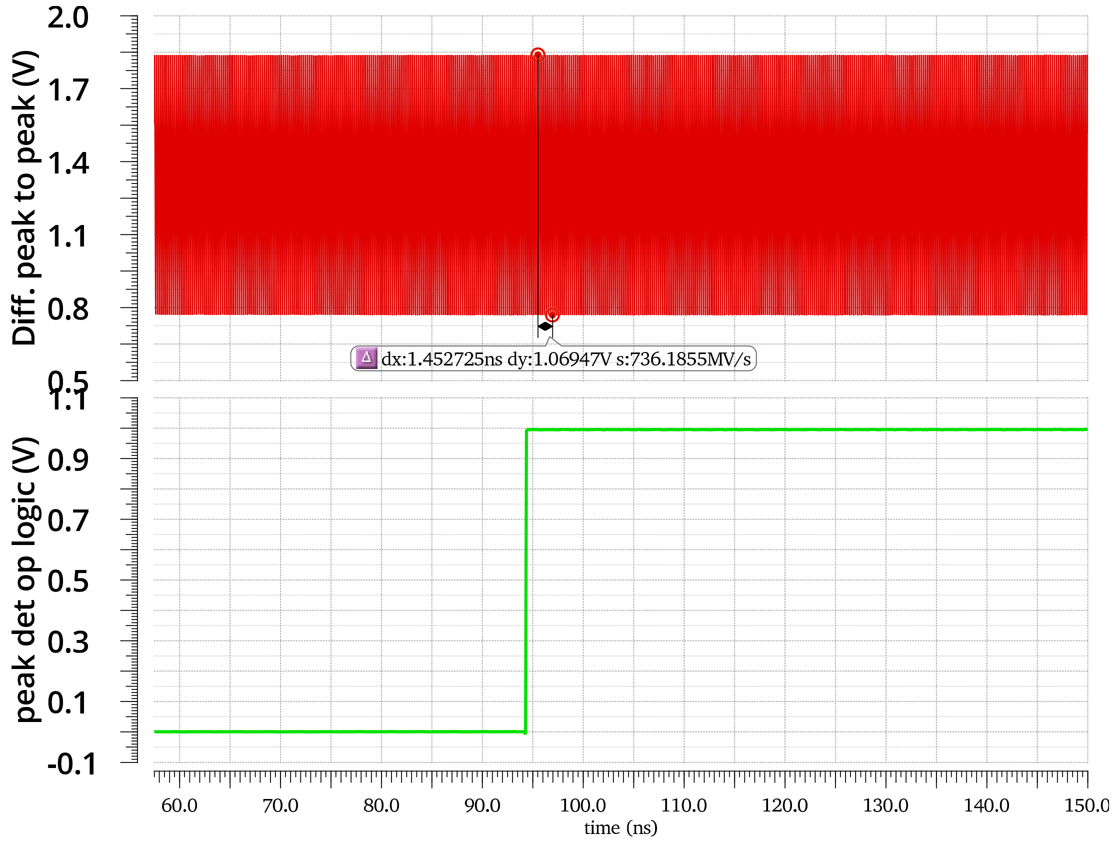


Figure 2.8: Peak detector logical output for 1 V peak to peak.

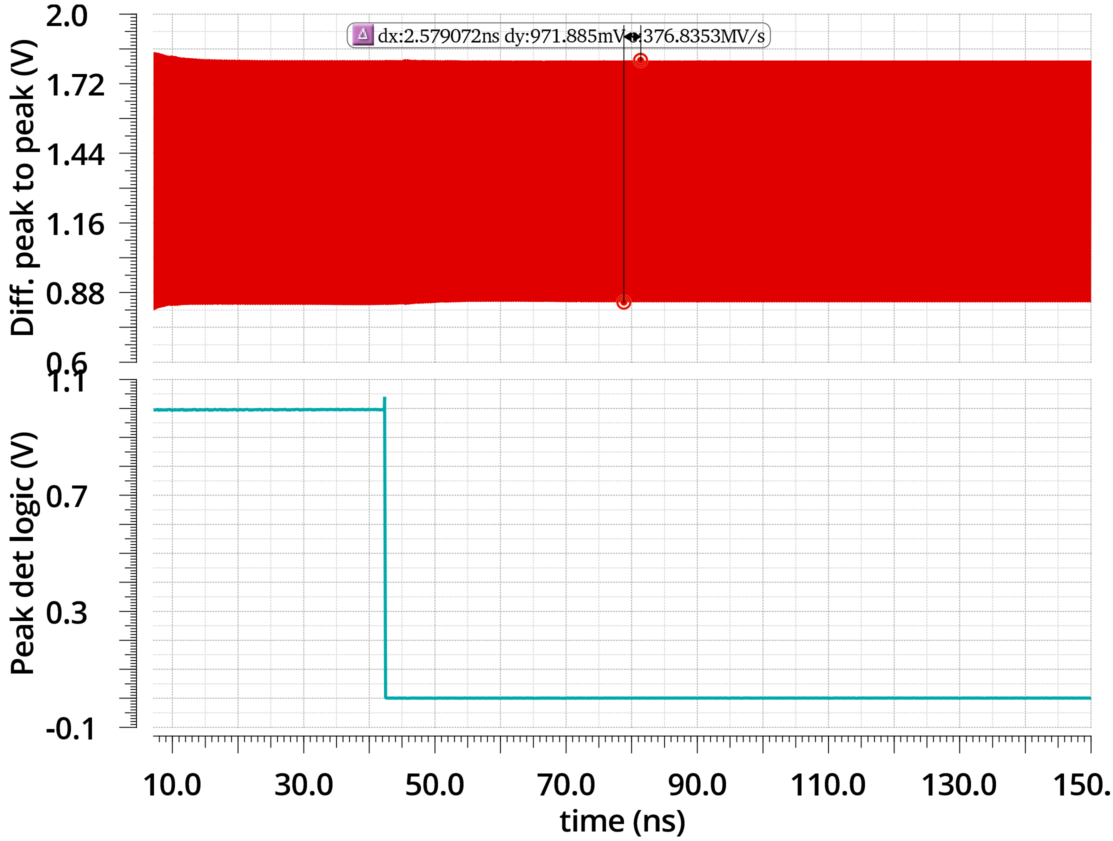


Figure 2.9: Peak detector logical output for $0.97\,\mathrm{V}$ peak to peak.

Figure 2.8 and 2.9 shows the transient simulation results of the VCO. We have set the peak detector threshold such that the logical output of the peak detector should be Vdd when differential peak to peak output of VCO is greater than $1\,\mathrm{V}$ else it should be zero. The green curve is the peak detector logical output which is logical 1 when differential peak to peak of the VCO is $1\,\mathrm{V}$ (fig 2.8) and logical zero when differential peak to peak is $0.97\,\mathrm{V}$ (fig 2.9).

CHAPTER 3

Low dropout regulator

3.1 Design of the low dropout regulator

The power supply rails are noisy and can not be used to power the VCO. Therefore we need a regulator circuit. Low dropout regulator(LDO) converts 1.2V to 1V regulated output with a good PSRR and very less phase noise contribution. LDO output is used to power up the VCO.

LDO consists of a two-stage opamp used in negative unity feedback configuration (Fig 3.1) driving a PMOS whose output is the supply node for VCO. The reference input V_{REF} to the LDO is a $0.7\,\mathrm{V}$ supply generated using a fractional bandgap circuit.

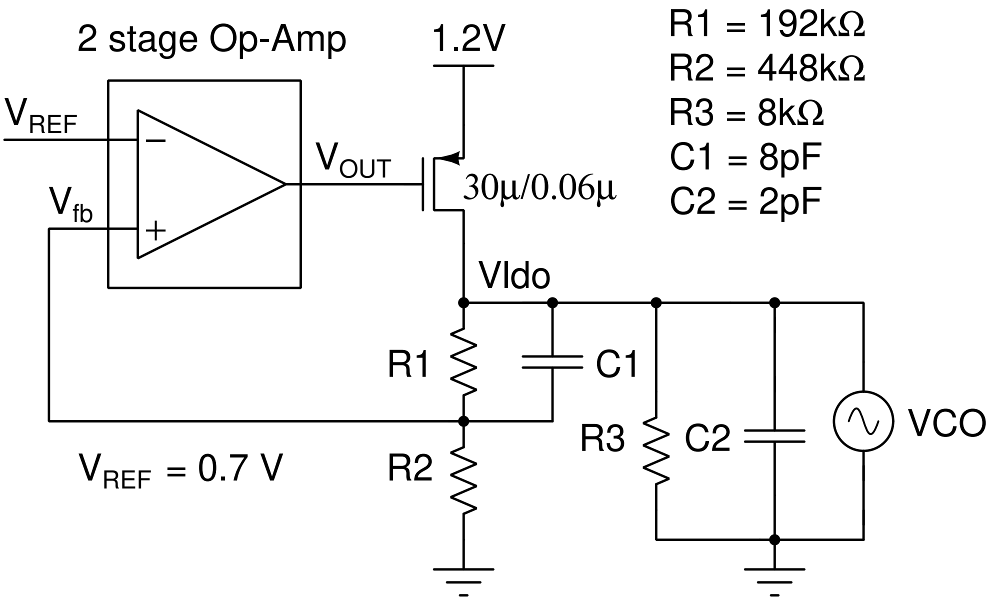


Figure 3.1: Schematic of the LDO.

The opamp used is a dominant pole compensated two-stage opamp (fig 3.2). The inverting input V_{REF} is connected to a bandgap output of $0.7\,\mathrm{V}$ and non-inverting input V_{fb} is connected to a resistor divider. Due to the high gain of opamp the non-inverting input will also settle to $0.7\,\mathrm{V}$ which will eventually make the node voltage of $Vldo$ settle at $1\,\mathrm{V}$.

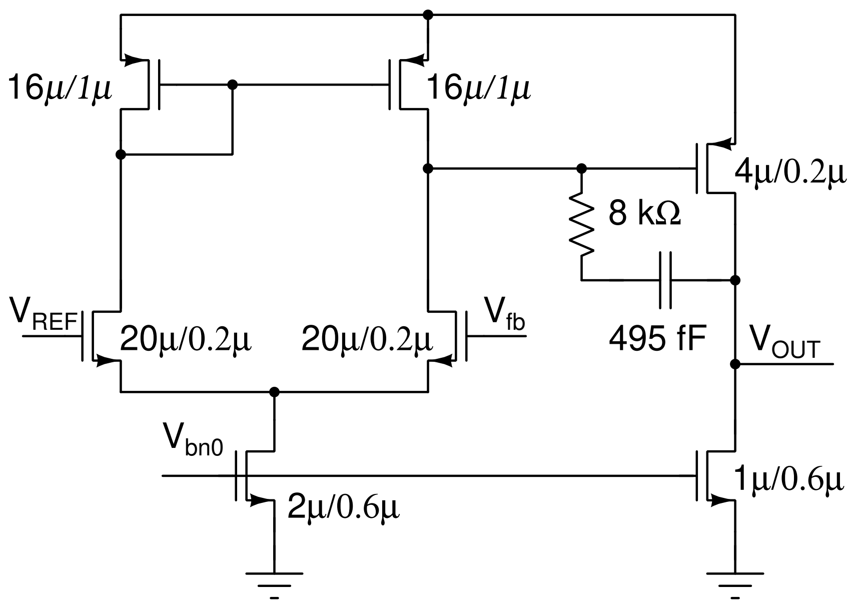


Figure 3.2: Schematic of LDO opamp.

To reduce the phase noise contribution by LDO we have used a high value of $R1$ (and therefore high $R2$) in parallel with an $8\,\text{pF}$ capacitor $C1$ (fig 3.1). $R3$ and $C2$ are used to improve the PSRR at high frequency.

Stb analysis is done to plot loop gain and phase.

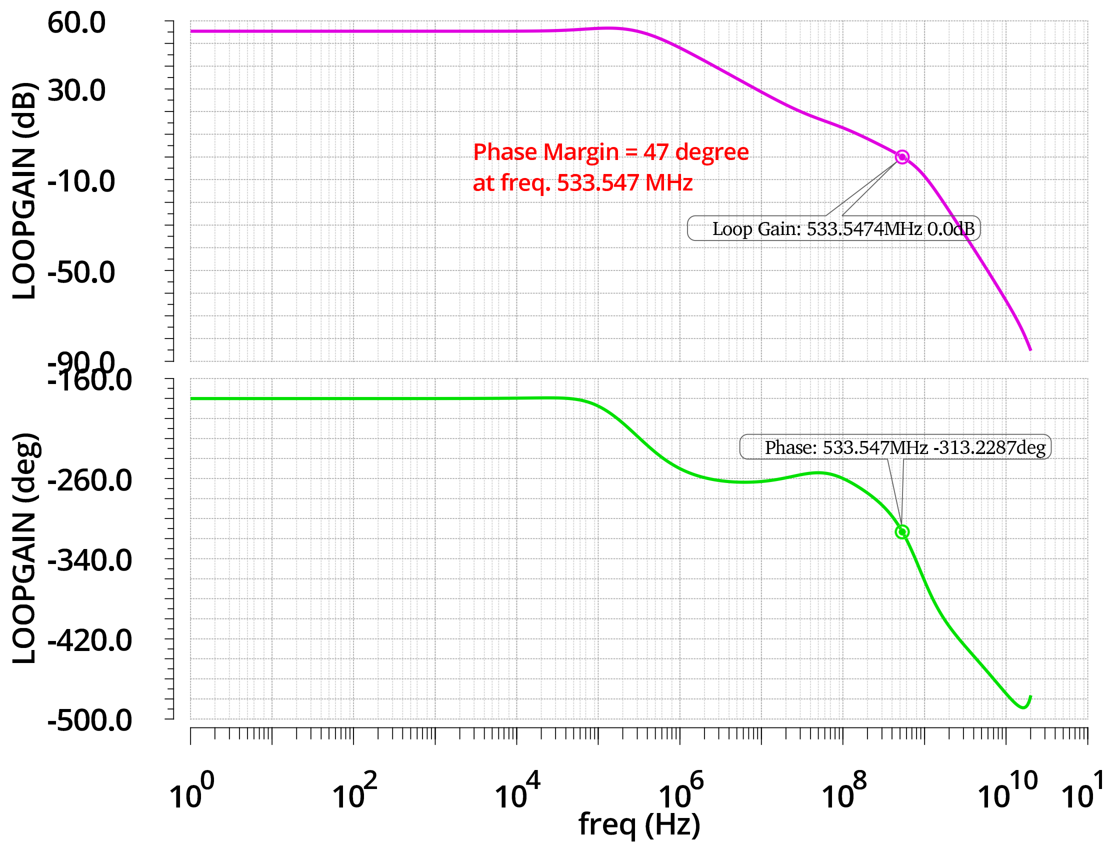


Figure 3.3: Loop gain plot of LDO with the load.

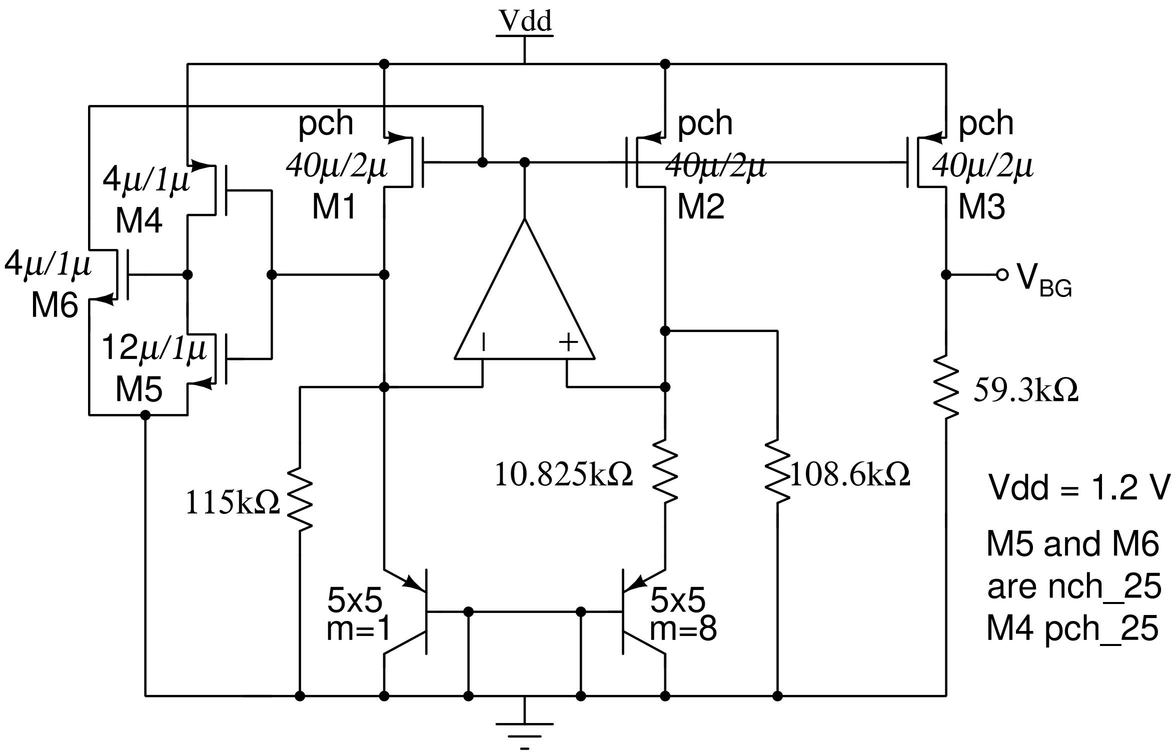


Figure 3.4: A 0.7 V band-gap reference circuit.

A low pass filter is used at the output of bandgap to reduce the phase noise contribution by the band-gap circuit. It uses an NMOS connected in series with a capacitor of value $16\,\mathrm{pF}$ (fig 3.3).

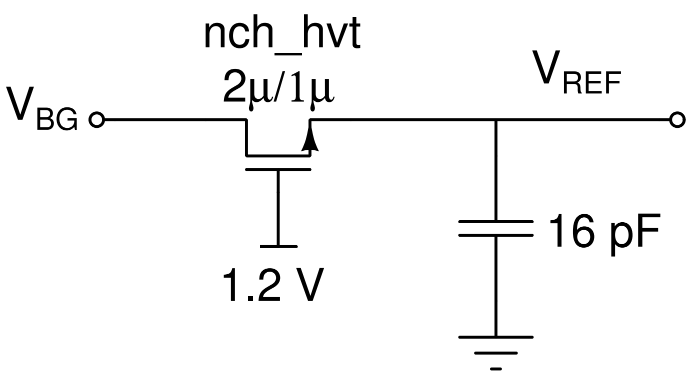


Figure 3.5: Low pass filter for bandgap.

3.2 Noise simulation of LDO

AC analysis has been done for PSRR measurement and noise analysis has been done for output noise measurement.

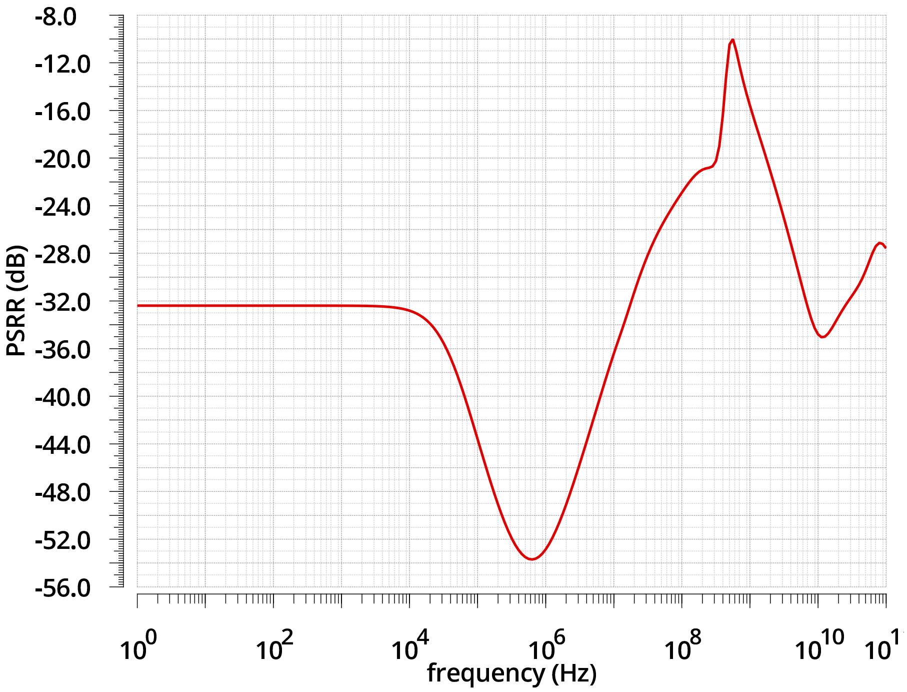


Figure 3.6: PSRR of LDO.

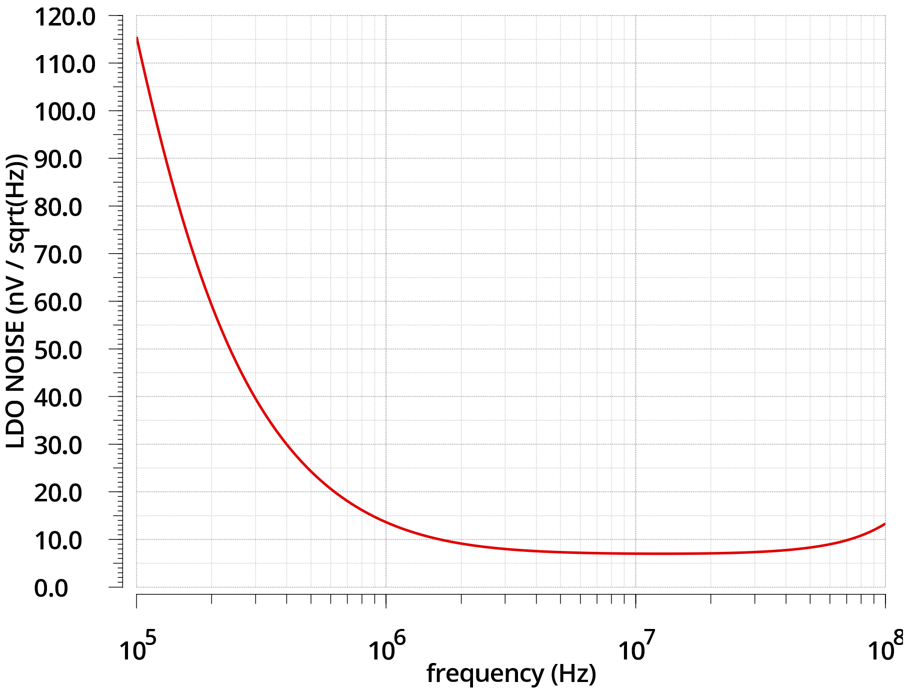


Figure 3.7: Noise at the output of LDO.

CHAPTER 4

Phase locked loop

4.1 Divider

4.1.1 Design of the divider

In a PLL, the feedback divider is designed to provide the required divide ratio. TSPC latch is used as divider because of their low power consumption as compared to other configurations. Two TSPC latch are cascaded to make a 2or3 divider. TSPC Latch is a dynamic circuit. Its states are defined as voltage stored at node parasitics which may leak if left floating for a long duration. Therefore, It has a low-frequency limitation and can not be used at a frequency below $500\,\mathrm{MHz}$.

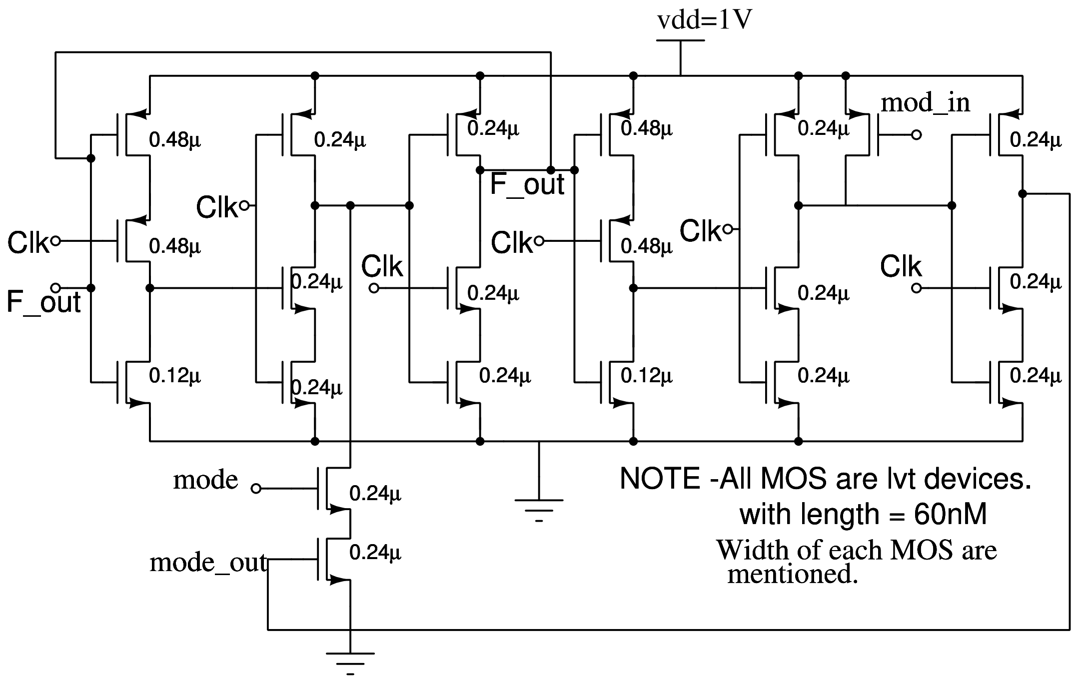


Figure 4.1: Schematic of 2or3 divider.

Five MOD-2or3 dividers are cascaded in a chain to form a programmable MOD-32or63 divider. We are using here MOD-45 divider for our PLL. Choose the combination P1 P2 P3 P4 P5 = 0 1 1 0 1 for division ratio of 45.

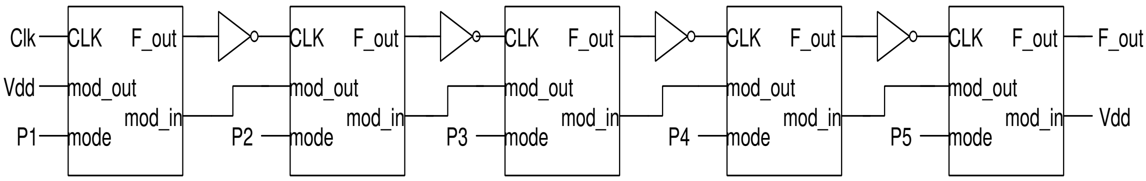


Figure 4.2: Schematic of Mod-45 divider

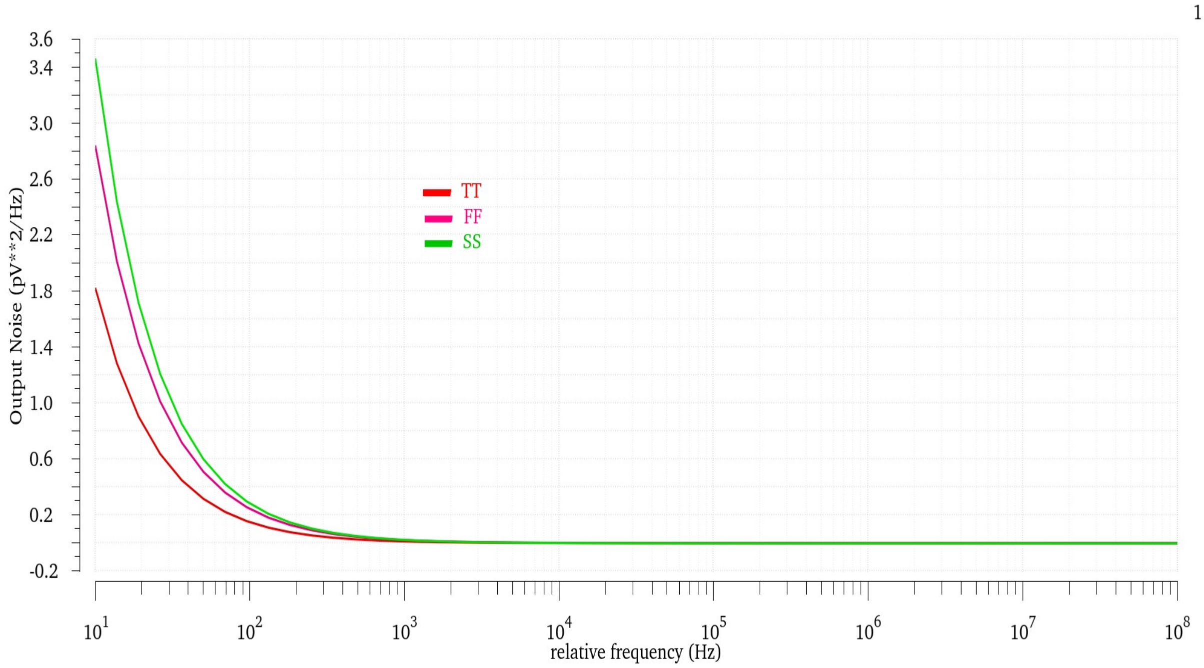


Figure 4.3: Noise at the output of divider.

4.2 Phase detector

4.2.1 Design of phase detector

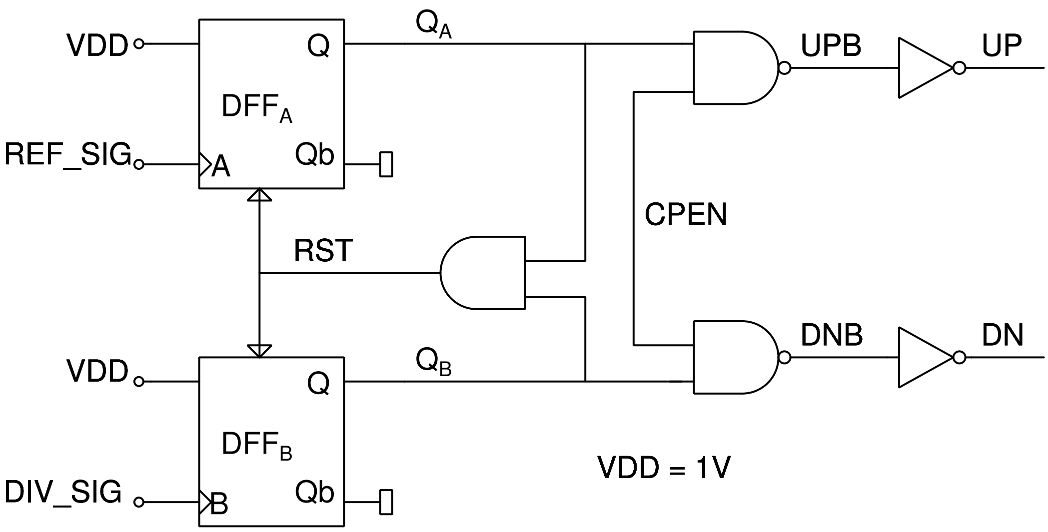


Figure 4.4: Phase frequency detector.

The circuit consists of two edge triggered D flip flops DFF_A and DFF_B. The D input of both FFs are connected to logic '1' and The clock input of DFF_A and DFF_B are connected to REF_{SIG} and DIV_{SIG} respectively. A positive edge on A will set Q_A to D_A (D_A = D_B = 1) and similarly, a positive edge on B sets Q_B high. When Q_A = Q_B = 1, AND gate will reset both the FFs. Q_A and Q_B both will be high for the duration of AND gate delay plus FF reset delay. We have used AND gate of $200\,\mathrm{p\,sec}$ delay.

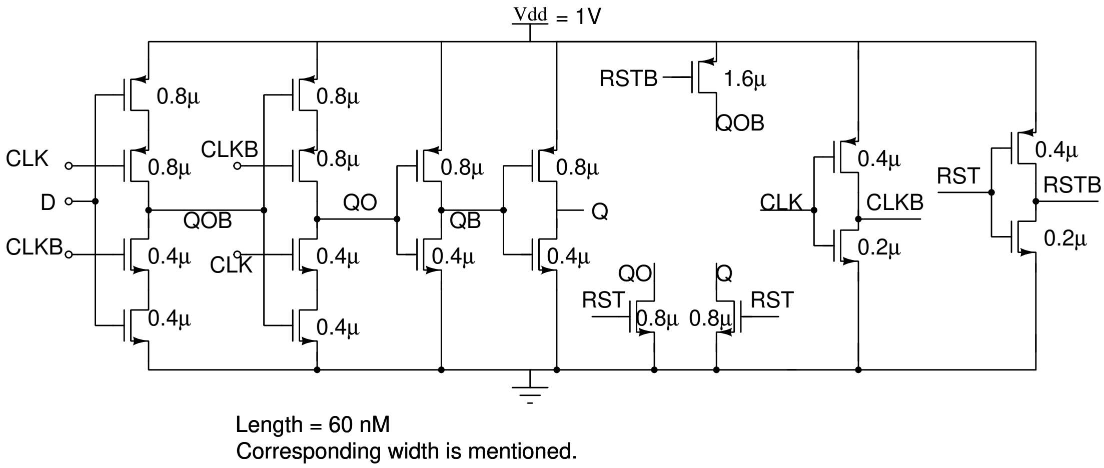


Figure 4.5: DFF schematic.

The operation of the PFD is shown below

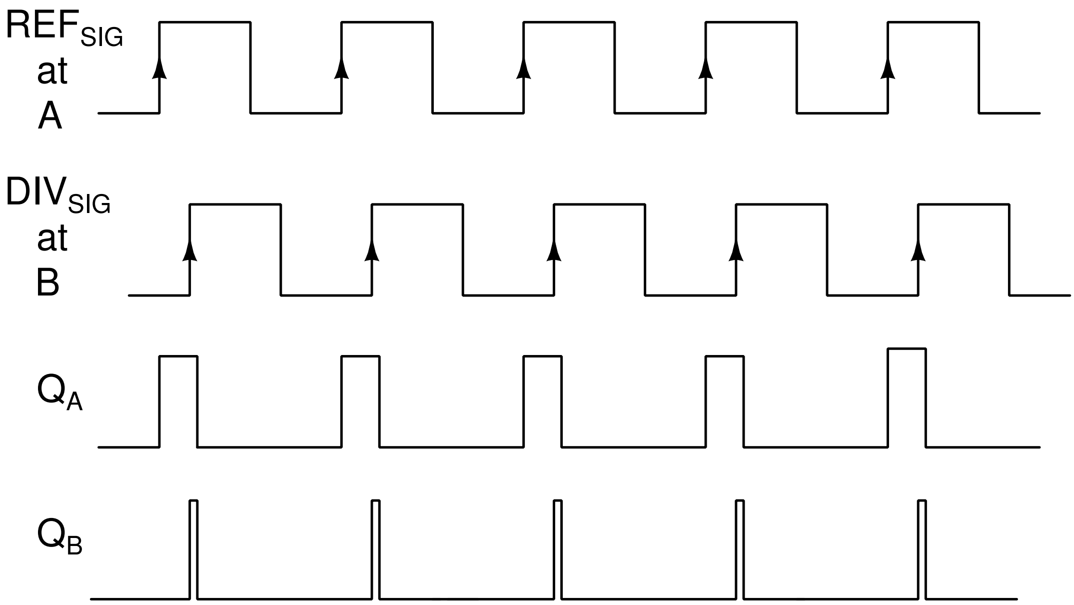
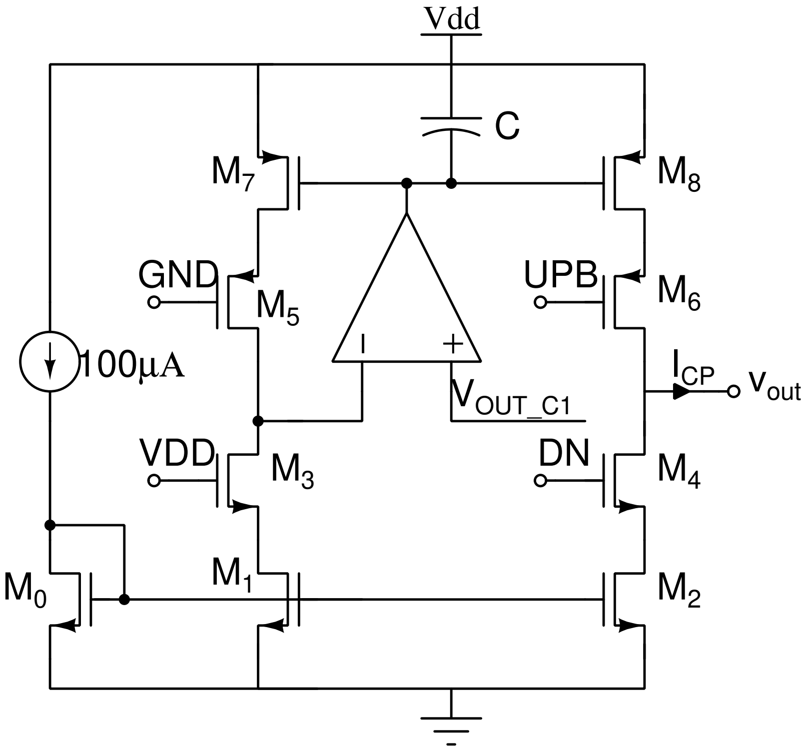


Figure 4.6: PFD output waveforms.

4.3 Charge pump and loop filter

4.3.1 Design of charge pump



M_0	1.1µ*21/1µ	
M_1	1.1µ/1µ	
M_2	1.1µ*8/1µ	
M_3	200n/60n	LVT
M_4	200n*8/60n	LVT
M_5	200n/60n	LVT
M_6	200n*8/60n	LVT
M_7	1.58u/1µ	
M_8	1.57µ*8/1µ	
C	2 pF	

Figure 4.7: Charge pump schematic.

A charge pump sinks or sources current for a fixed period. The charge pump is driven by the outputs of PFD. Here two current sources PMOS M_8 and NMOS M_2 correspond to the source and sink respectively. M_6 and M_4 are two switches that turn ON with UP and DN signal from PFD. MOS M_1 and M_7 are biasing transistors. The charge pump current I_{CP} is chosen to be $32\,\mu$A. The charge pump current will depend on the node voltage of V_{out}. We have chosen V_{out} to be $0.5\,$V to have approximately equal current of $32\,\mu$A for both NMOS and PMOS (due to the same V_{ds}) such that in phase-locked condition average current should be zero.

Consider a capacitor is connected to the V_{out} terminal. Now, during UP is high (or UPB Low) the capacitor will charge linearly and during DN it will discharge. The capacitor will hold the value when both UP and DN signals are low. The output waveforms are shown below

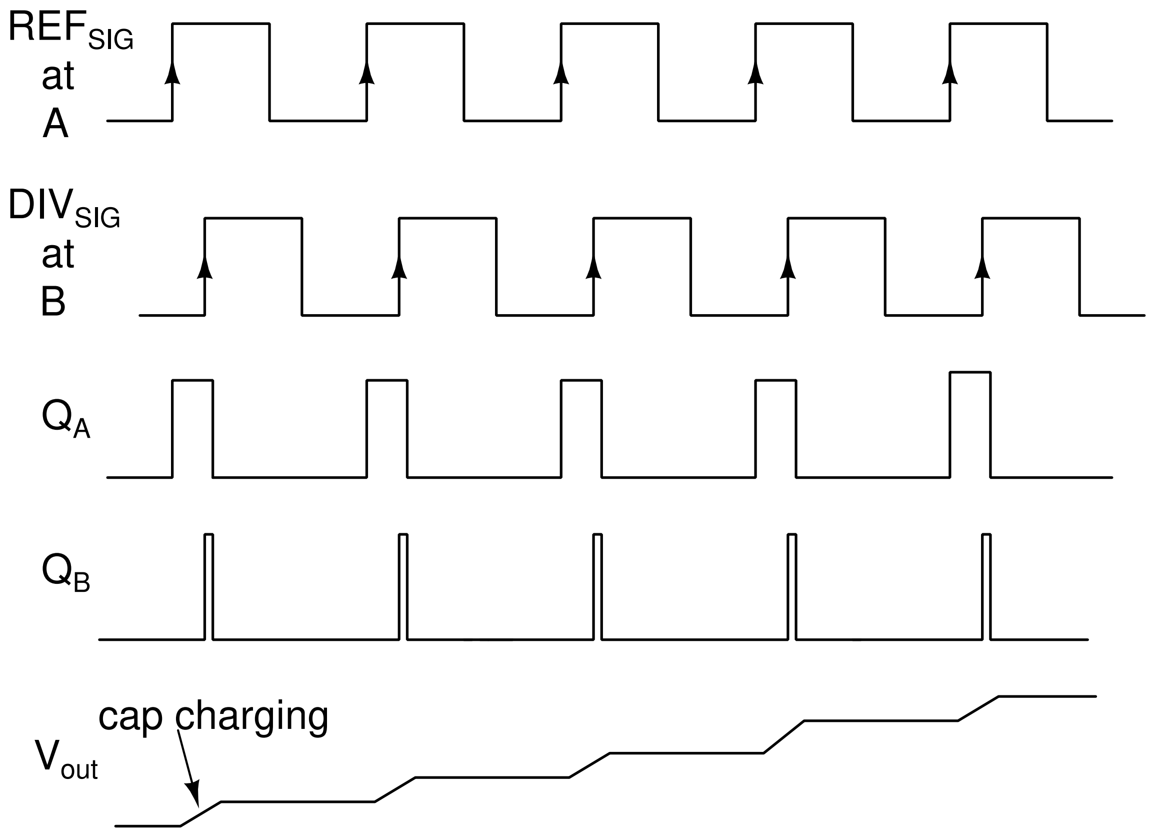


Figure 4.8: Charge pump output waveform.

4.3.2 Design of Loop Filter

Loop filter converts charge pump current to control voltage required for VCO. It uses a series combination of resistor R and a capacitor C_1. Whenever there is a phase difference at the PFD inputs, the average of "UP-DN" will be non-zero and thus some non-zero average current will flow through loop filter and generate the voltage V_{ctrl}. If there is a mismatch in the charge pump current sources then there will always be a small average current which will cause a small ripple in charge pump voltage V_{ctrl}. The extra capacitor C_2 is added to reduce this ripple.

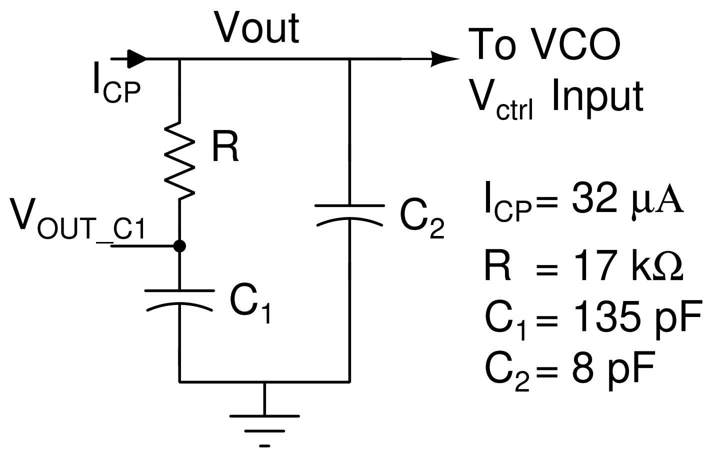


Figure 4.9: Loop filter schematic.

4.4 Design and implementation of PLL

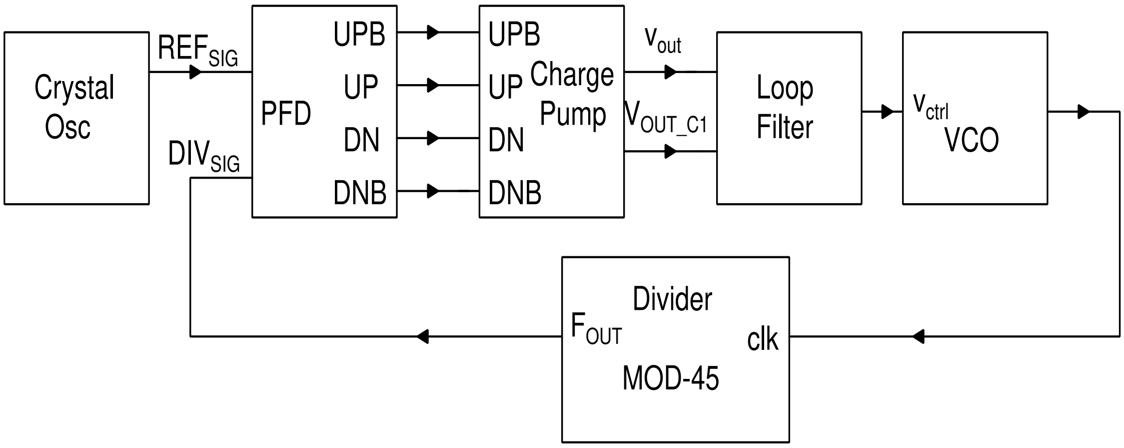


Figure 4.10: Block diagram of PLL.

The block-level implementation of PLL is shown in Fig 8.1. It consists of a crystal oscillator operating at $114.314\,\mathrm{MHz}$, a divider to obtain the frequency same as reference frequency $114.314\,\mathrm{MHz}$, a PFD block to detect the phase difference, a charge pump, and loop filter to generate the control voltage corresponding to phase difference detected by PFD and a VCO to generate the frequency corresponding to the V_{ctrl} generated by loop filter to reduce the phase difference at PFD input.

A type-II and 3rd order PLL is designed with the phase noise specification shown in table 8.1. The loop bandwidth is chosen to be $500\,\mathrm{kHz}$. The nominal phase margin is $60°$ at a unity gain frequency of $457\,\mathrm{kHz}$.

Table 4.1: Phase noise at PLL output.

Phase noise at output of PLL ‖ R=$17\,\mathrm{k\Omega}$ C1= $135\,\mathrm{pF}$ C2 = $8\,\mathrm{pF}$		
Ref frequency	Required phase noise in dBC/Hz	Simulated phase noise in dBC/Hz
$1\,\mathrm{MHz}$	-81	-107.9
$2\,\mathrm{MHz}$	-111	-117.8
$3\,\mathrm{MHz}$	-121	-123.6

CHAPTER 5

LAYOUT AND POST LAYOUT SIMULATION RESULTS

5.1 Layout of PLL

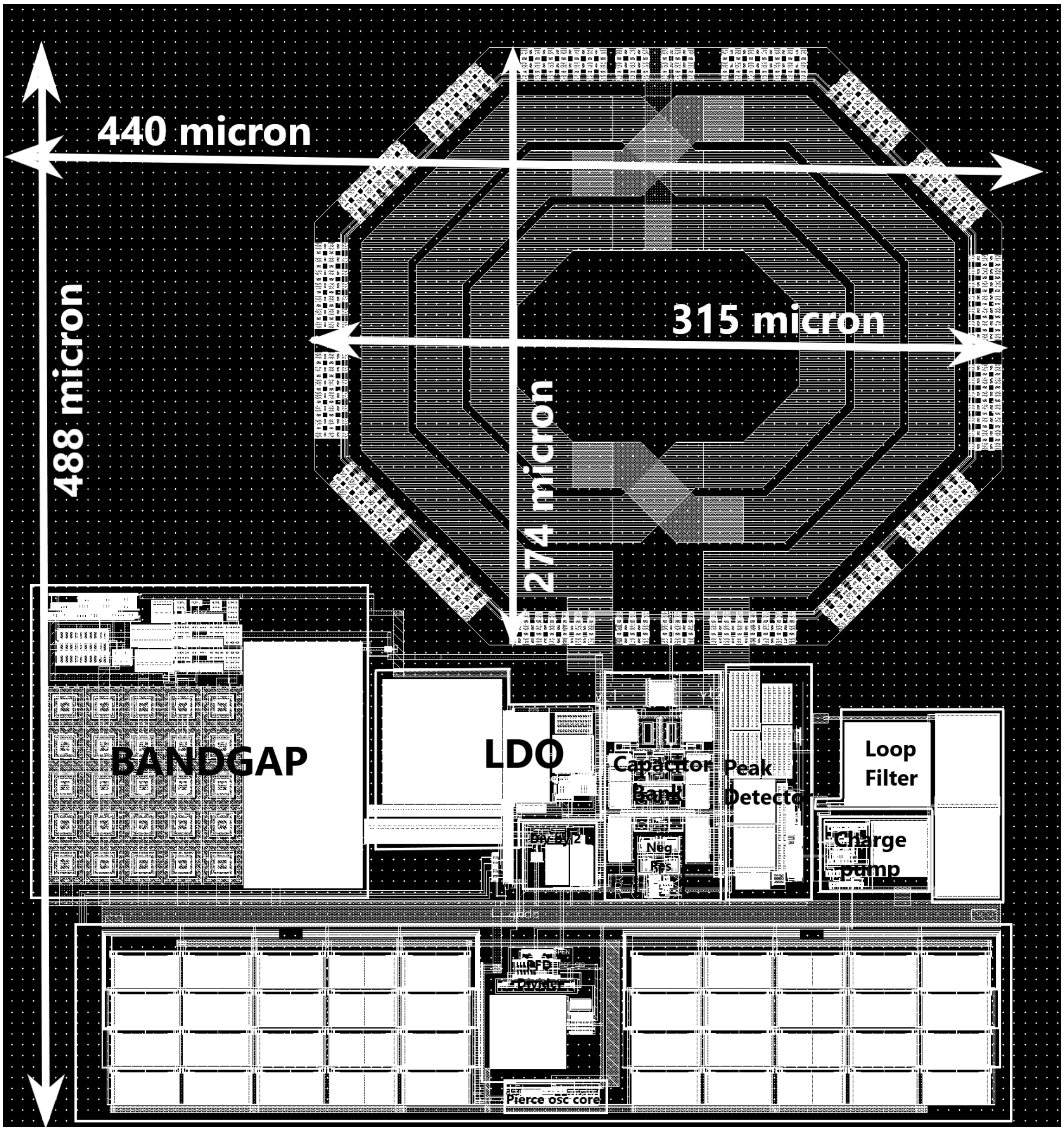


Figure 5.1: Layout of PLL.

5.2 VCO Simulation Results

Here only those results are shown which satisfy the following conditions:

1) Phase noise (PN) at $2\,\text{MHz} \leq -115\,\text{dBc/Hz}$.

2) $5.1\,\text{GHz} \leq$ $output\ frequency$ $\leq 5.3\,\text{GHz}$.

3) $220\,\text{MHz} \leq \text{K}_{VCO}$ $\leq 290\,\text{MHz}$.

Table 5.1: TT 0 °C Results with LDO.

TT Corners Results @ 0 °C for R3 R2 R1 = 1 0 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
0 1 1 1	0	5.029	-120.900	1.212	634.600
0 1 1 1	0.5	5.087	-120.200	1.204	636.600
0 1 1 1	1	5.180	**-120.000**	**1.169**	**642.600**
1 0 0 0	0	5.078	**-121.900**	**1.415**	**619.600**
1 0 0 0	0.5	5.137	-121.200	1.412	621.800
1 0 0 0	1	5.232	-121.100	1.384	629.100
1 0 0 1	0	5.139	-121.700	1.409	624.100
1 0 0 1	0.5	5.201	-120.900	1.407	626.100
1 0 0 1	1	5.299	-120.800	1.378	633.100

Table 5.2: TT 0 °C results without LDO.

TT Corners Results @ 0 °C without LDO		
C4 C3 C2 C1	vctrl (V)	Phase noise at 2 MHz
1 0 0 0	0	-122.800 dBc/Hz
1 0 0 0	0.5	-121.900 dBc/Hz
1 0 0 0	1	-122.000 dBc/Hz

Table 5.3: TT 80 °C Results with LDO.

TT Corners Results @ 80 °C for R3 R2 R1 = 1 0 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
0 1 1 1	0	5.015	-118.300	1.083	634.600
0 1 1 1	0.5	5.074	-117.800	1.077	636.600
0 1 1 1	1	5.160	**-117.400**	**1.049**	**642.600**
1 0 0 0	0	5.064	**-119.500**	**1.277**	**619.600**
1 0 0 0	0.5	5.125	-118.900	1.276	621.800
1 0 0 0	1	5.212	-118.700	1.253	629.100
1 0 0 1	0	5.123	-119.200	1.273	624.100
1 0 0 1	0.5	5.187	-118.700	1.272	626.100
1 0 0 1	1	5.277	-118.500	1.249	633.100

Table 5.4: SS 0 °C Results with LDO.

SS Corners Results @ 0 °C for R3 R2 R1 = 1 1 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
1 1 0 0	0	5.057	**-122.400**	1.497	634.600
1 1 0 0	0.5	5.123	-121.400	1.500	636.600
1 1 0 0	1	5.222	-121.500	**1.484**	**642.600**
1 1 0 1	0	5.130	-122.200	1.500	**619.600**
1 1 0 1	0.5	5.199	-121.100	1.504	621.800
1 1 0 1	1	5.302	-121.200	1.488	629.100
1 1 1 0	0	5.208	-122.000	1.527	624.100
1 1 1 0	0.5	5.280	**-120.900**	**1.532**	626.100
1 1 1 0	1	5.388	-121.000	1.518	633.100

Table 5.5: SS 80 °C Results with LDO.

SS Corners Results @ 80 °C for R3 R2 R1 = 1 1 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
1 1 0 0	0	5.035	-120.400	1.409	634.600
1 1 0 0	0.5	5.102	-119.600	1.414	636.600
1 1 0 0	1	5.192	-119.600	**1.402**	**642.600**
1 1 0 1	0	5.106	-120.200	1.414	619.600
1 1 0 1	0.5	5.177	-119.400	1.421	**621.800**
1 1 0 1	1	5.270	-119.400	1.409	629.100
1 1 1 0	0	5.182	-120.000	1.443	624.100
1 1 1 0	0.5	5.255	**-119.200**	**1.450**	626.100
1 1 1 0	1	5.353	**-119.200**	1.439	633.100

Table 5.6: FF 0 °C Results with LDO.

FF Corners Results @ 0 °C for R3 R2 R1 = 0 0 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
0 0 0 0	0	5.051	**-120.300**	**1.231**	**633.700**
0 0 0 0	0.5	5.101	-120.000	1.218	636.600
0 0 0 0	1	5.189	-119.500	1.171	643.900
0 0 0 1	0	5.099	-120.100	1.215	636.600
0 0 0 1	0.5	5.151	-119.700	1.202	639.400
0 0 0 1	1	5.241	-119.300	**1.155**	**646.000**
0 0 1 0	0	5.149	-120.000	1.223	635.300
0 0 1 0	0.5	5.203	-119.600	1.210	638.100
0 0 1 0	1	5.296	**-119.100**	1.163	645.000

Table 5.7: FF 80 °C Results with LDO.

FF Corners Results @ 80 °C for R3 R2 R1 = 0 1 1					
C4 C3 C2 C1	vctrl (V)	Output freq.(GHz)	Phase noise at 2 MHz (dBc/Hz)	Differential peak to peak output (V)	Average VCO current (μA)
0 0 0 0	0	5.037	**-117.800**	**1.202**	**752.400**
0 0 0 0	0.5	5.090	-117.500	1.191	755.200
0 0 0 0	1	5.169	-117.000	1.153	762.900
0 0 0 1	0	5.084	-117.500	1.189	755.400
0 0 0 1	0.5	5.138	-117.200	1.178	758.000
0 0 0 1	1	5.220	-116.700	**1.141**	**765.300**
0 0 1 0	0	5.133	-117.400	1.197	753.700
0 0 1 0	0.5	5.189	-117.100	1.186	756.300
0 0 1 0	1	5.273	**-116.600**	1.148	763.900

PSS and pnoise analysis are done to plot the below results. Frequency and K_{VCO} has been plotted for 16 capacitor bank combinations.

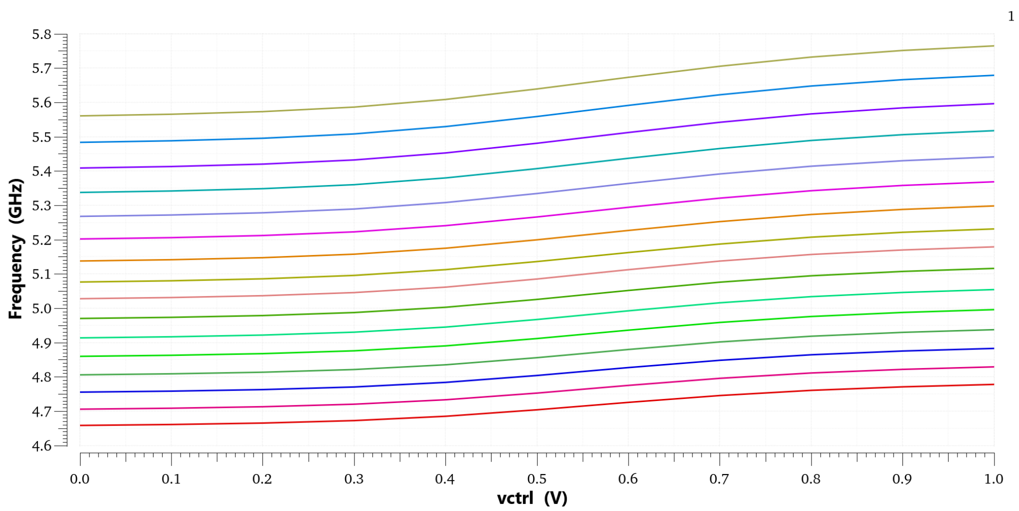


Figure 5.2: Tuning range TT 0 °C.

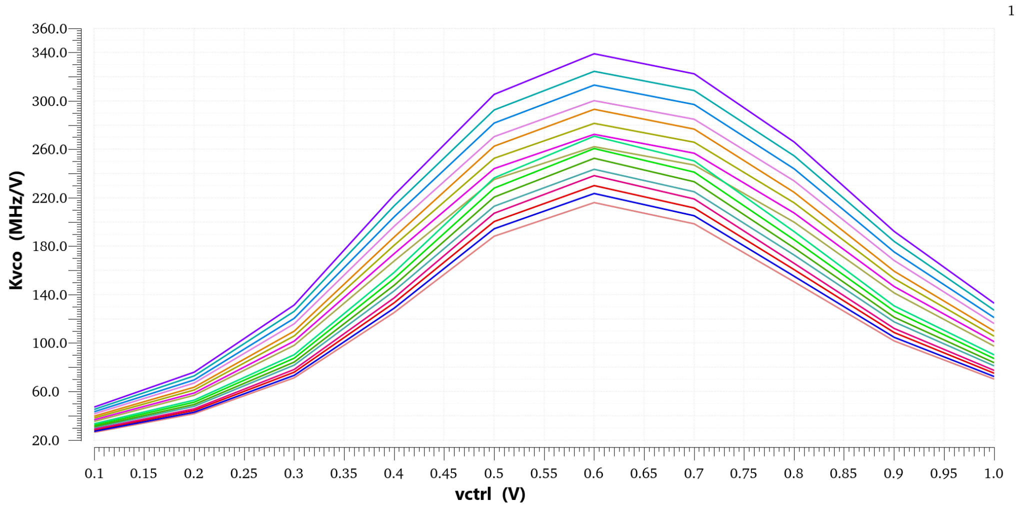


Figure 5.3: Kvco vs control voltage TT 0 °C.

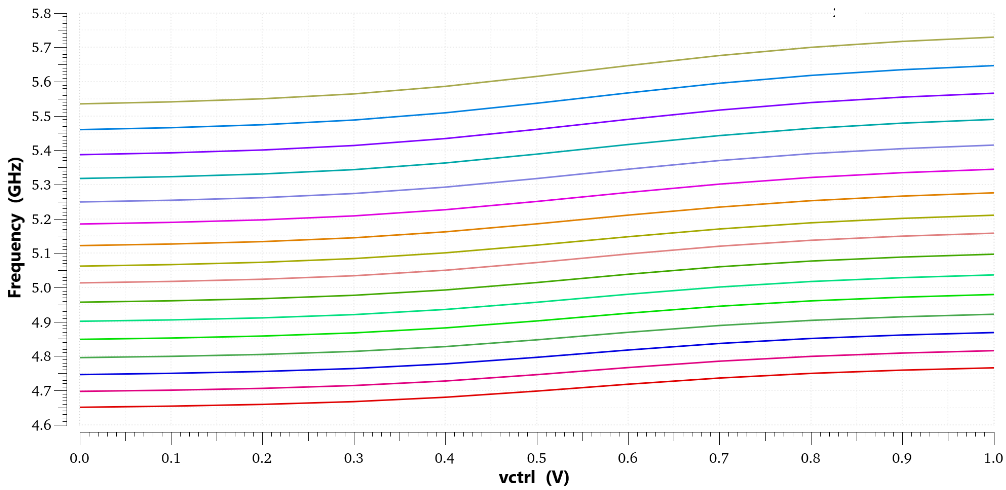


Figure 5.4: Tuning range TT 80 °C.

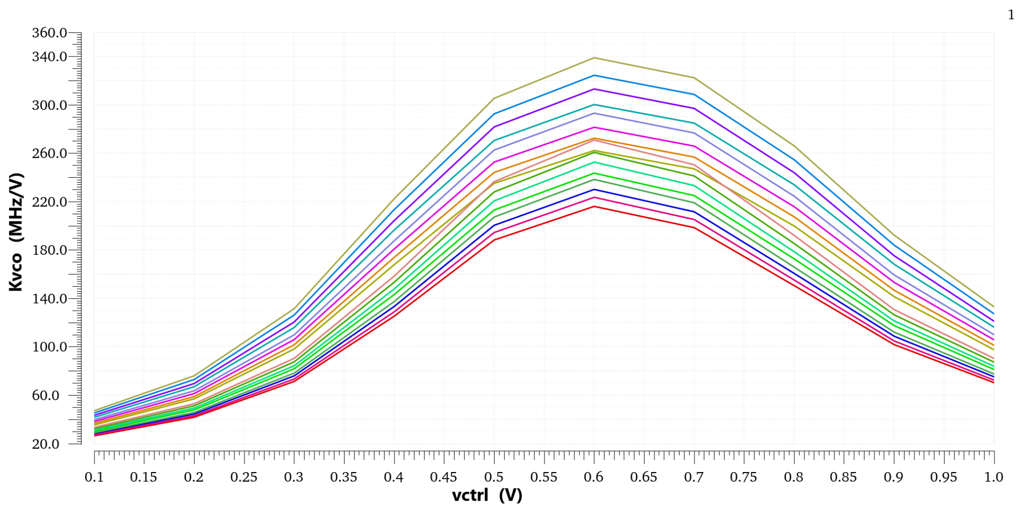


Figure 5.5: Kvco vs control voltage TT 80 °C.

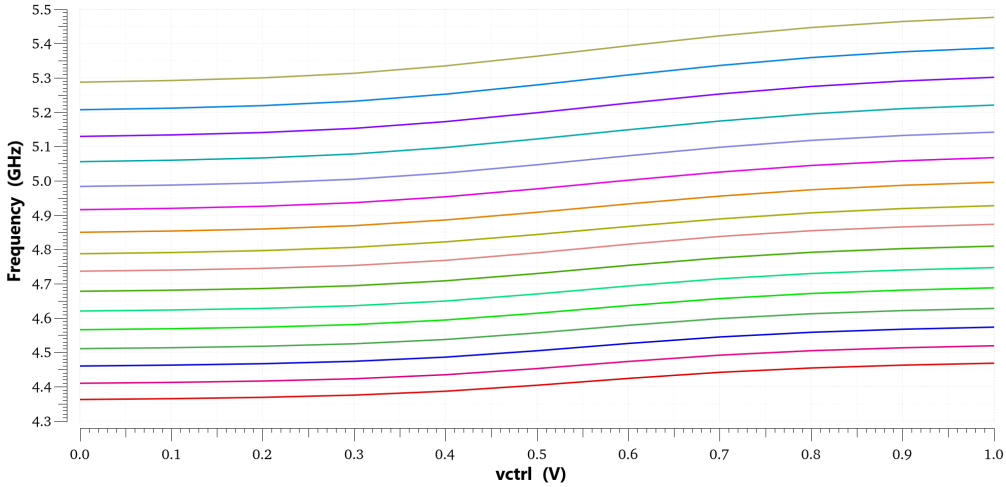


Figure 5.6: Tuning range SS 0 °C.

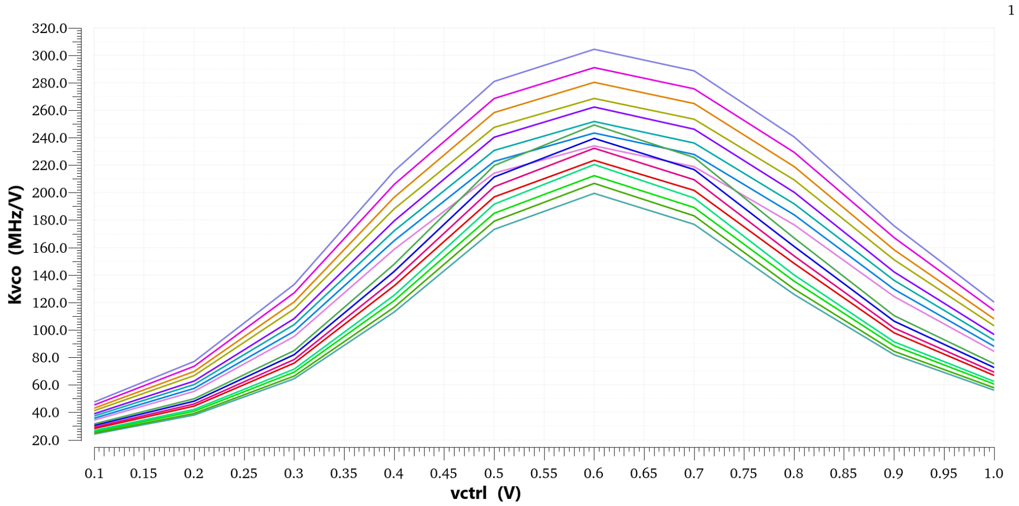


Figure 5.7: Kvco vs control voltage SS 0 °C.

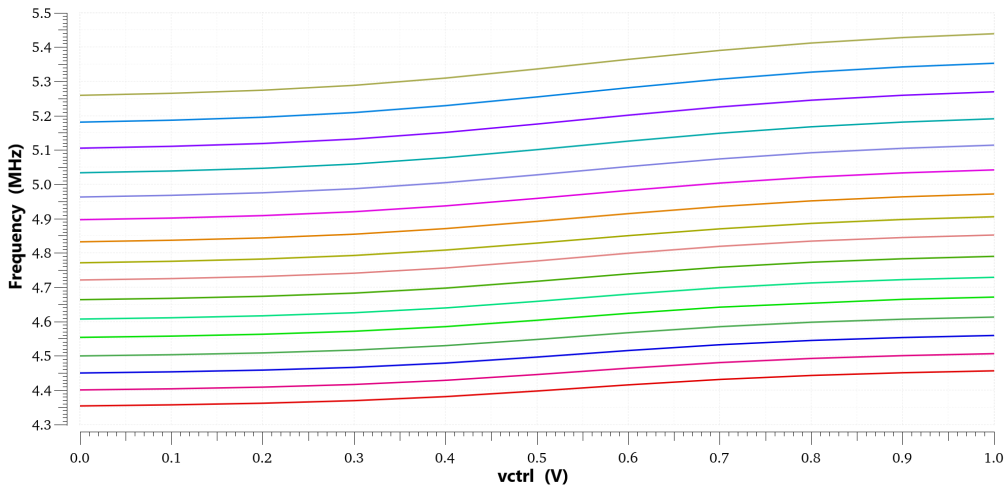


Figure 5.8: Tuning range SS 80 °C.

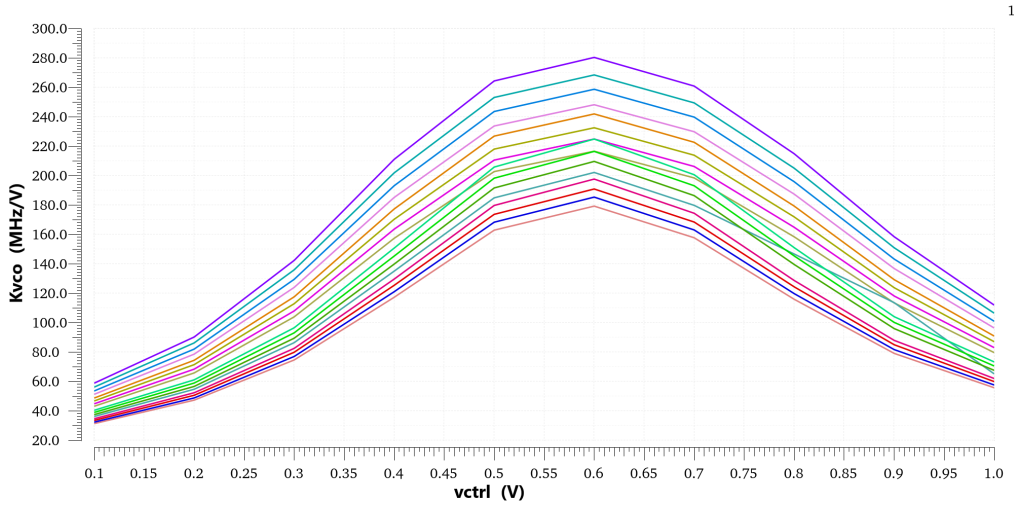


Figure 5.9: Kvco vs control voltage SS 80 °C.

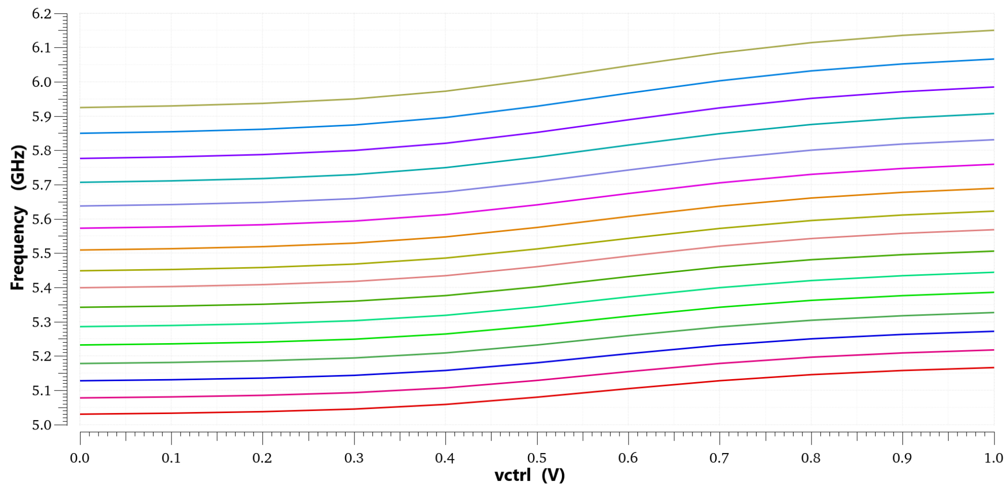


Figure 5.10: Tuning range FF 0 °C.

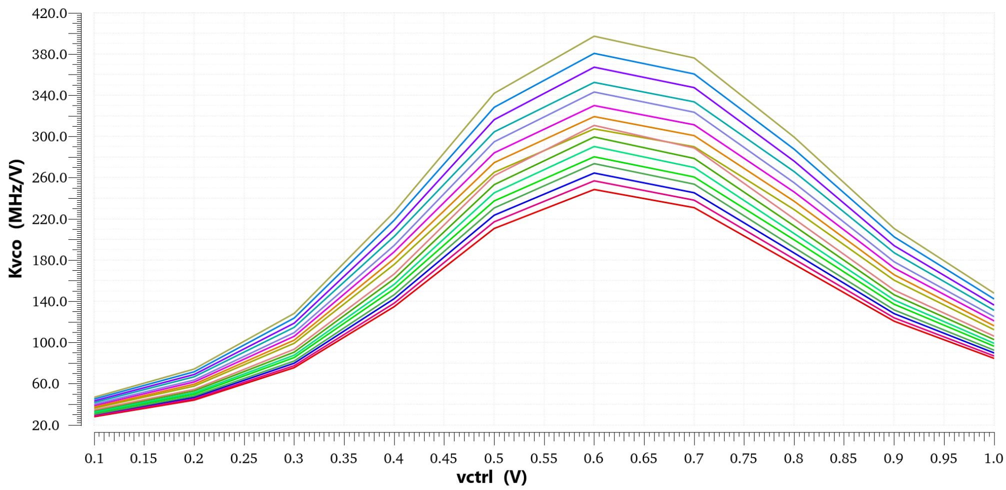


Figure 5.11: Kvco vs control voltage FF 0 °C.

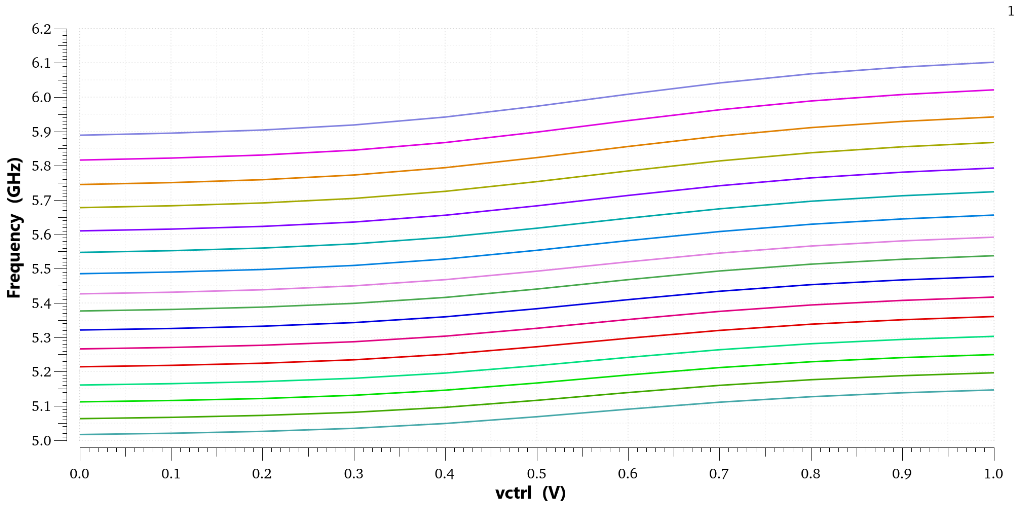


Figure 5.12: Tuning range FF 80 °C.

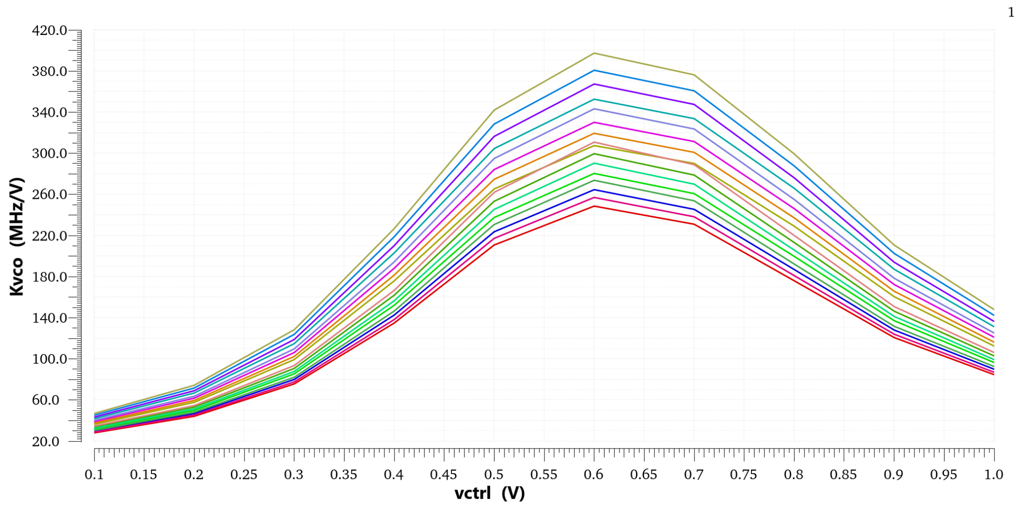


Figure 5.13: Kvco vs control voltage FF 80 °C.

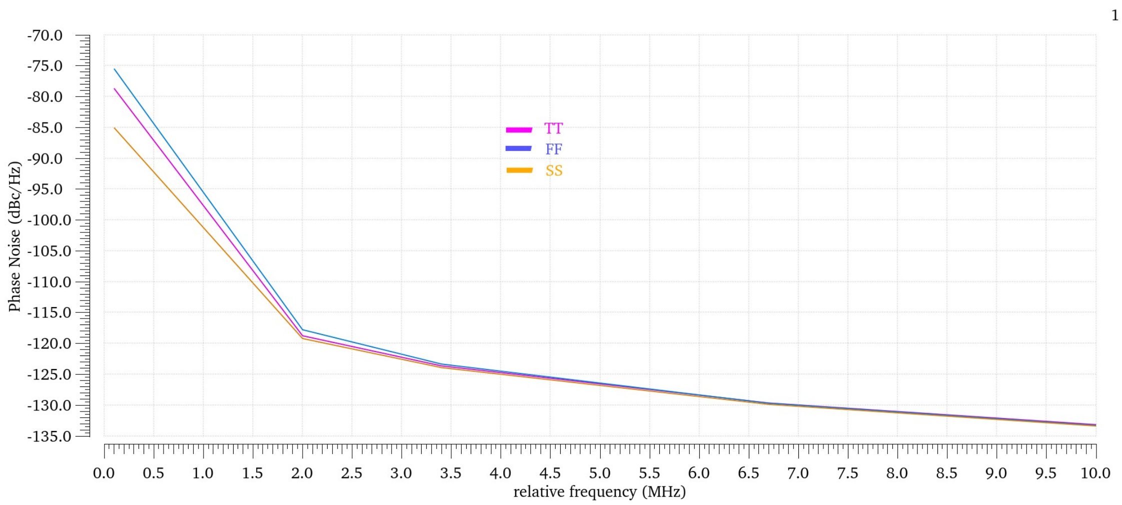


Figure 5.14: Phase noise of VCO across TT, SS, and FF.

5.2.1 FOM of VCO

FOM of VCO can be given by the formula [1]

$$FOM_{VCO} = -10\log\left(L_{VCO}(\triangle\omega)\frac{P}{1\,\mathrm{mW}}\left(\frac{\triangle\omega}{\omega_o}\right)^2\right). \tag{5.1}$$

From the above simulation results, we see that worst-case phase noise and power consumption is coming in the FF corner. So, our worst-case FOM will be FoM_{VCO} = $-186.6\,\mathrm{dBc/Hz}$ and the FoM_{VCO} in TT corner is $-191.46\,\mathrm{dBc/Hz}$.

5.3 PLL Simulation Results

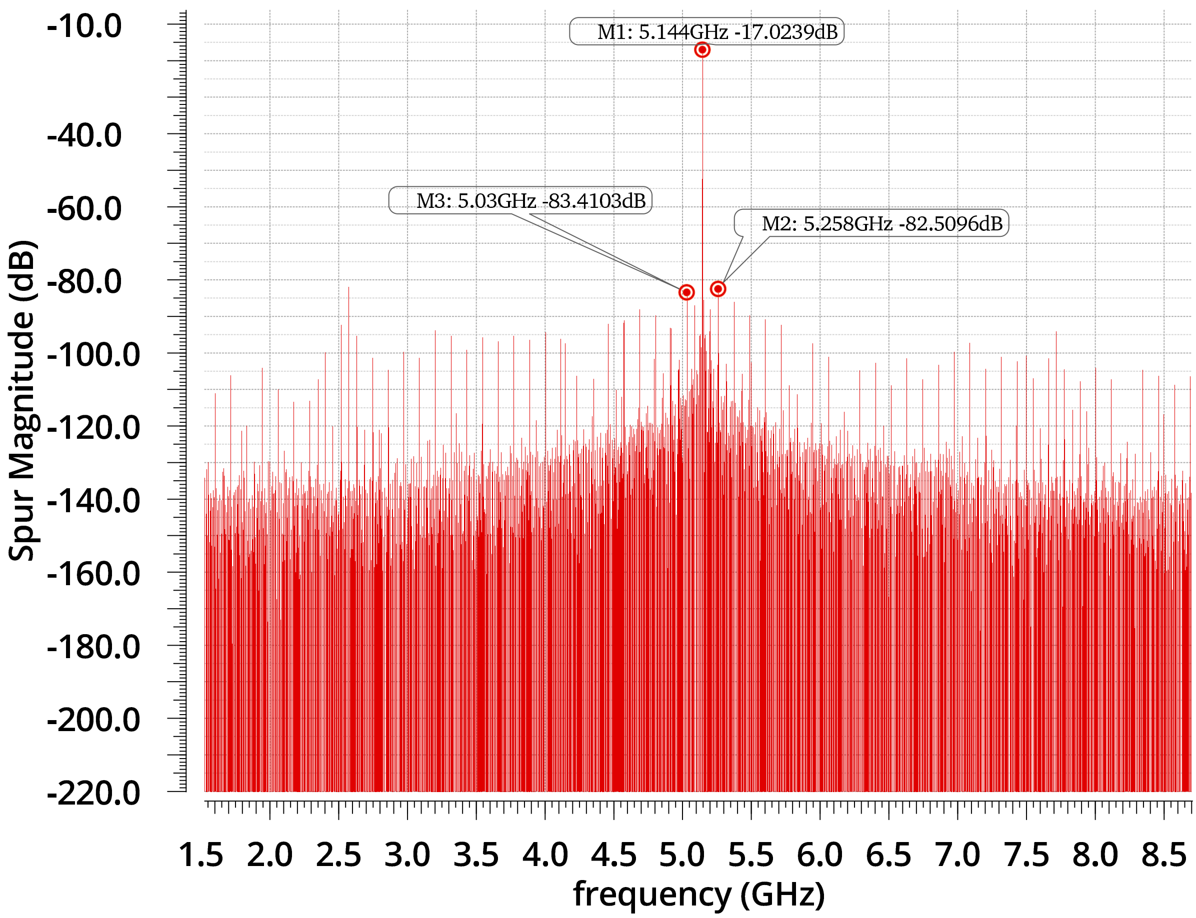


Figure 5.15: PLL output Spectrum in FF 0 °C.

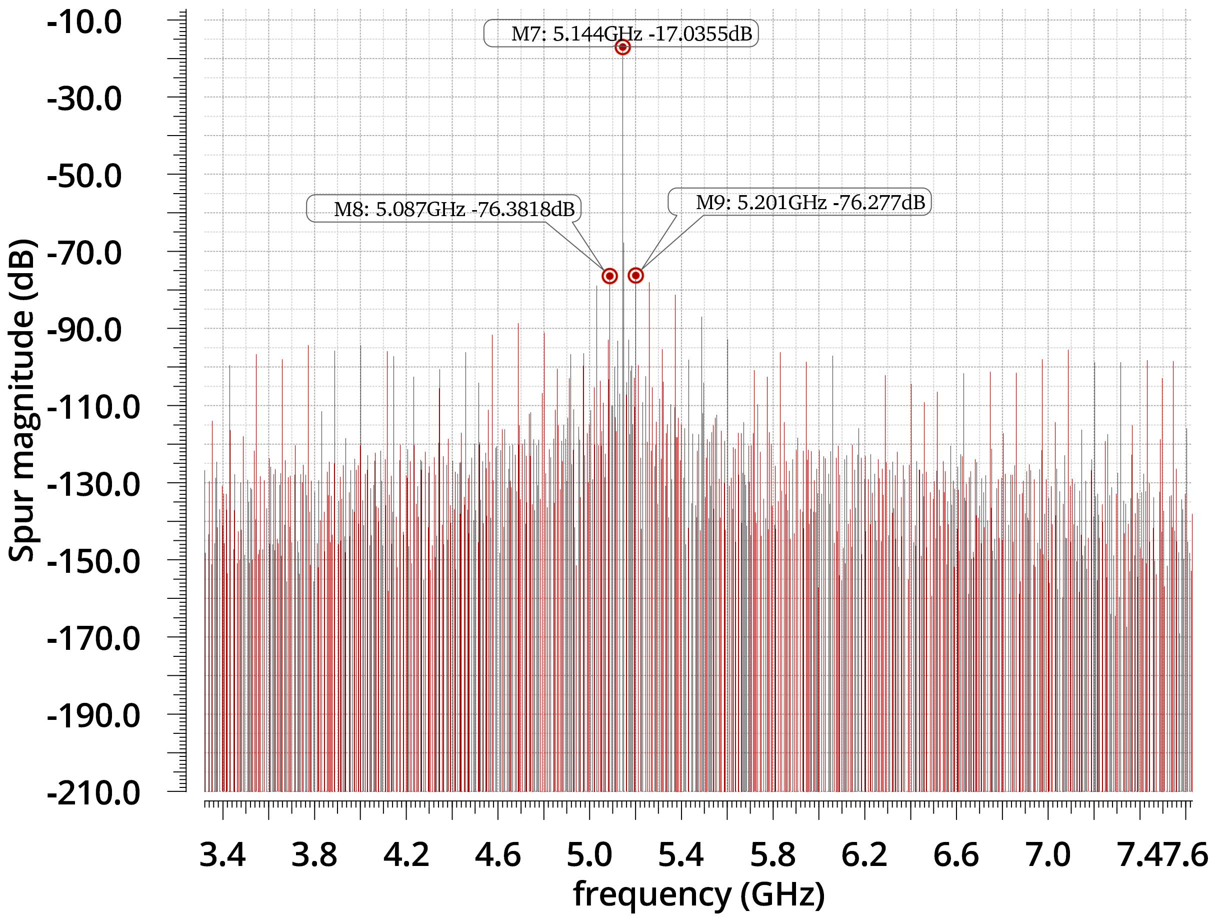


Figure 5.16: PLL output Spectrum in FF 80 °C.

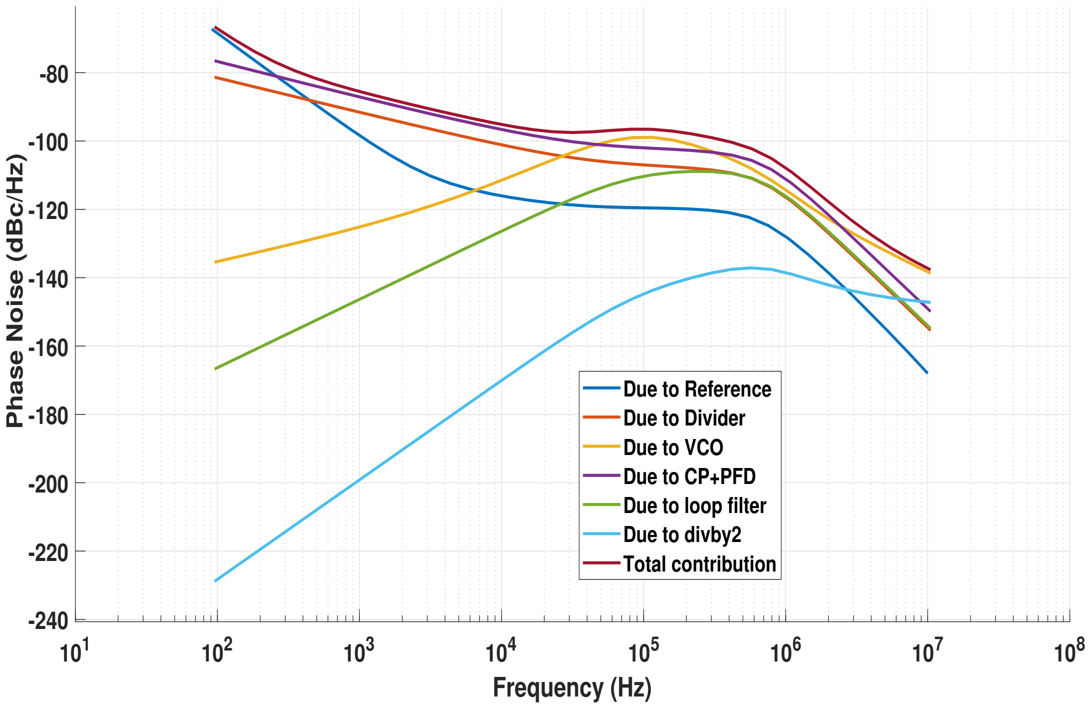


Figure 5.17: Phase noise plot at PLL output.

5.4 Designed specification

Table 5.8: Specification summary.

Designed specifications of PLL in TT 27 °C	
Specifications	Simulated value
Output frequency	2.57 GHz
Phase noise at 3 MHz	−123.6 dBc/Hz
Spur at 114.3 MHz	−54.4 dBc
Settling time	10 µs
Jitter in 1.286 GHz BW	1.098 ps
Power	3 mW

5.5 Power consumption

Table 5.9: Power consumption summary.

Power consumption	
Design block	Power(µW)
VCO core	579
Peak detector	145
Bandgap and LDO	213
Buffer and divide by 2	944
PFD	115
Charge pump	56
Divider	166
Reference	830
Total	3048

CHAPTER 6

CONCLUSION

A $5.144\,\mathrm{GHz}$ VCO and PLL for clocking a delta-sigma ADC was presented in this thesis. The 4-bit capacitor bank ensures the VCO output frequency to fall within the required range and the peak detector allows us to control VCO current to reduce wastage of power. The opamp reduces the mismatch in charge pump current and therefore reduces the spur levels at the output of PLL. The spur level is now $-54.4\,\mathrm{dBc}$. The nominal power consumed by the PLL is $3\,\mathrm{mW}$.

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