Electothermal simulation for SOI MOSFET based circuits

A thesis submitted in partial fulfillment of the requirements for the award of the degree of

MASTER OF TECHNOLOGY

in

ELECTRICAL ENGINEERING

by

K Sashidhar
(EE18M035)

Under the guidance of
Prof. Dr. Janakiraman Viraraghavan

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY MADRAS

CHENNAI-600036

MAY 2020

THESIS CERTIFICATE

This is to certify that the thesis entitled "**Electrothermal simulation for SOI MOSFET based circuits**" submitted by **K SASHIDHAR** to the Department of Electrical Engineering, Indian Institute of Technology Madras for the award of the degree of **Master of Technology**, is a bonafide record of the research work carried by him under my supervision. The research work was carried out at the Indian Institute of Technology, Madras.

The content of this thesis, in full or in parts, have not been submitted to any other institute or university for the award of any other degree or diploma.

Dr. Janakiraman Viraraghavan
Professor, Project Guide
Dept. of Electrical Engineering
IIT Madras, 600036

Place: Chennai
Date: 15/06/2020

ACKNOWLEDGEMENTS

I sincerely express my profound gratitude to my project guide, Prof. Janakiraman Viraraghavan, for his esteemed guidance and encouragement throughout the course of this project work. I am thankful to him for his most valuable guidance and his suggestions had been the source of inspiration for me during the conduct of this project and keep me on the right track which contributed immensely to the completion of this project.

I would like to thank the Department of Electrical Engineering, Indian Institute of Technology Madras, to who gave me an opportunity to undergo project work in their esteemed institution.

Finally, most importantly, I wish to express my heartfelt thanks to my family and friends, for being my source of energy.

K Sashidhar

ABSTRACT

In SOI MOSFET the self-heating effect increases as the technology scales down, due to which the electrothermal simulation is necessary to obtain the correct electrical characteristics and thermal profile of the circuits. However, for very large circuits the electrothermal simulation has a time constraint. In this paper, a quick method to generate the thermal network is proposed along with which the electrical network can be simulated at the SPICE level.

TABLE OF CONTENTS

ACKNOWLEDGEMENT.....iii

ABSTRACT.....iv

LIST OF TABLES.....vi

LIST OF FIGURES.....vii

CHAPTER

1. INTRODUCTION.....8
2. THERMAL MODELING.....11
3. INTERCONNECT MODELING.....13
4. RESULTS.....18
5. CONCLUSION.....20

REFERENCES.....21

APPENDIX24

LIST OF TABLES

Table 4.1 Device Temperature.....19

LIST OF FIGURES

Fig 1.1 Bulk and SOI devices.....8
Fig 2.1 Equivalent circuit for self-heating simulation.....12
Fig 3.1 Temperature profiles of two device circuit in GENIUS.....15
Fig 3.2 Two device circuit.....15
Fig 3.3 Interconnect Model.....16
Fig 3.4 Flowchart.....17
Fig 4.1 Id vs Vds.....18
Fig 4.2 Id vs Vgs.....18

CHAPTER-1

INTRODUCTION

1.1 SOI Devices:

Silicon is the most widely used semiconductor material. It is available abundantly and it is easier than other materials to convert into a pure single crystal. When heated to high temperature, silicon is stable unlike other semiconductor materials and an insulating and passivated material, silicon dioxide, can readily be grown on it. The excellent electrical and chemical properties of Si02 are the most important factor which made silicon such a successful semiconductor material.

Metal-Oxide-Semiconductor (MOS) devices are made at the surface of silicon wafers that are 700-800 um thick, but occupy around just 1 micrometer at the surface of the wafer. The remainder of the wafer serves as mechanical support for the devices and sometimes gives rise to unwanted parasitic interactions with the devices. In a silicon-on-insulator (SOl) wafer the devices are fabricated in a thin silicon layer. This silicon layer is single-crystalline and sits on an insulating material. Silicon thickness ranges from 10 nm to several micrometers, as required in the application, and the silicon dioxide layer thickness ranges between 50 nm and 1um. The whole structure rests on a mechanical substrate, which is usually made of silicon. The oxide layer between the active top silicon layer and the mechanical silicon substrate is called the buried oxide (BOX).

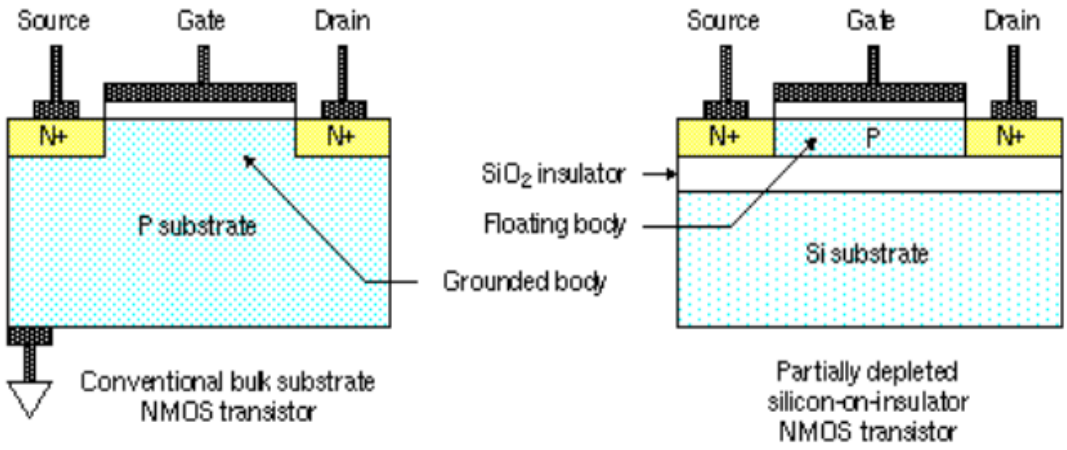


Fig 1.1. Bulk and SOI devices

Silicon-on-insulator(SOI) devices became quite successful in the past few decades and they are still being used in mainstream chip-making techniques. The advantages of using SOI devices as compared to bulk substrate devices are

I. Since the device is isolated from the bulk by buried oxide it provides lower parasitic capacitance and hence we get a power advantage of around 3 times when compared to devices that have been fabricated using bulk CMOS process.

II. It improves performance of the device by 25-30 percent as there is resistance to latch-up due to complete isolation of n- and p-well structures.[24]

III. The leakage currents are lower due to the isolation of device from substrate.

IV. Antenna issues are reduced.

V. We get better yield because of high density and hence wafer is utilized better.

VI. Short channel effects are subdued due to isolation of device from substrate.

Due to complete isolation of device from substrate by the buried oxide in SOI devices, floating body is created. Due to impact ionization holes are created and a positive charge is built up in the silicon body of the transistor. This charge can’t be removed rapidly enough as there is no contact with the body available. When the drain voltage is high enough, the channel electrons get sufficient energy in the high electric field near the drain and generate electron hole pairs through impact ionization. The generated electrons rapidly flow into the drain, and the holes migrate toward the lowest potential region, i.e., the p-type floating body. The source/body diode is created and is in forward bias and hence the holes which are at the lowest potential region will now be swept into the source. This causes floating body effect. This creates unwanted issues if not accounted for.

As we know the mobility of the charge carriers in the channel depends on the temperature of the device and hence the channel current is a function of the temperature of the device. We use BSIMSOI model for modelling of SOI device in SPICE , which will be discussed later in detail. In this model we have an option to consider the temperature effect on the device current calculation. There is a parameter called *shmod* created in model file which tells the simulator whether to consider temperature effect or not.

1.2 Self heating in SOI:

Due to the relatively poor thermal conductivity of the buried oxide layer (BOX) a significant amount of heat is generated even at low power densities. Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect within the device is less efficient than in bulk. Hence self- heating effect arises, which results in the rise of the average device temperature[3][5]. The device heats up to 50ºC to 150ºC. The rise in device temperature results in a substantial reduction of mobility, current drive and carrier saturation velocity and leads to degradation of device over a period of time. Hence, self-heating is a serious problem in SOI devices

As heat is being trapped within the device, it eventually flows through the interconnect metals[5]. It further leads to electro migration, higher power consumption, increased delay time, joule heating etc[3]. Hence electrothermal simulation is needed to obtain the correct behavior of the circuit. To get a realistic temperature profile as well as electrical characteristics of the circuit apart from the device level model, the interconnect coupling between the devices and other heat losses must be taken into account which depends on the designed layout. Given that we have the parasitic extracted netlist from the layout of any circuit and device level thermal model(like BSIMSOI), we propose a quick method to obtain the realistic temperature profile of the given circuit based on electrothermal simulation by capturing the heat flow between devices via interconnect. The results are verified in the device simulator(2-D GENIUS tool)[23].

Chapter 2 mainly covers the existing thermal modeling of SOI devices using BSIMSOI model. In Chapter 3 the interconnect heat flow model is proposed which can be used both in isothermal and non-isothermal models. Here BSIMSOI model along with the proposed interconnect model are used which can be easily implemented in SPICE related tools. In Chapter 4 the results obtained through Genius device simulator are discussed and Chapter 5 concludes the electro thermal modeling of SOI devices.

CHAPTER-2

THERMAL MODELING

2.1 Electro-thermal simulation:

The electro-thermal simulation is categorized into two fundamental methods. In first method the simulator solves the heat conduction problem numerically using techniques such as finite difference method[10][8] and finite element method [11][12].The major advantages are higher accuracy and ability to handle different heat sources as well as boundary conditions[14]. But the shortcoming is large simulation time to perform electrothermal simulation for very large circuits. The second method is fundamentally based on modeling heat equation into electrical circuits. Here, fundamental idea is that heat flow and electrical current flow are dual in nature. The heat flow is modeled as the electrical current passing through the thermal resistance, the temperature difference corresponds to voltage drop and heat absorption is modeled as a thermal capacitance. The second method is recommended for electrothermal simulation due to its timing advantage. In this, the single-node thermal circuit model (isothermal model) BSIMSOI [22] is used which assumes constant SOI device temperature. [4] The isothermal model has its own advantage and disadvantages over non-isothermal model. The electrothermal simulation is necessary because the current in the device and device temperature are interdependent on each other and the device temperature further depends on the feedback from the thermal network due to heat losses through interconnect and oxides.

2.2 Modeling of temperature in BSIMSOI model:

Self-heating in SOI devices is more significant than in bulk devices as the thermal conductivity of silicon dioxide, which is used as BOX in SOI devices is about two orders of magnitude lower than that of silicon, which is used as substrate in bulk devcies. It may increase the junction leakage, degrade the carrier mobility, enhance the impact ionization rate, and therefore affect the output characteristics of floating-body SOI devices.

BSIMSOI models the self-heating by using an auxiliary $R_{th}C_{th}$ circuit as shown in fig 2.1. When the self-heating selector *shmod* is ON and the thermal resistance is non-zero, the external temperature node (T node) will be created in SPICE simulation to facilitate the

simulation of thermal coupling among neighboring devices. The T node will be created as a voltage node and it is connected to ground via a thermal resistance R_{th} and a thermal capacitance C_{th}

$$R_{th}=\frac{R_{th0}}{W_{eff}+W_{th0}}, C_{th}=C_{th0}\cdot\left(W_{eff}+W_{th0}\right) \quad (1)$$

Here, R_{th0} is normalized thermal resistance and C_{th0} is normalized thermal capacitance. W_{th0} Is the minimum width for thermal resistance calculation. The current source driving the circuit has magniude equal to the power dissipated in the device.

$$P=\left|I_{ds}\,x\,V_{ds}\right| \quad (2)$$

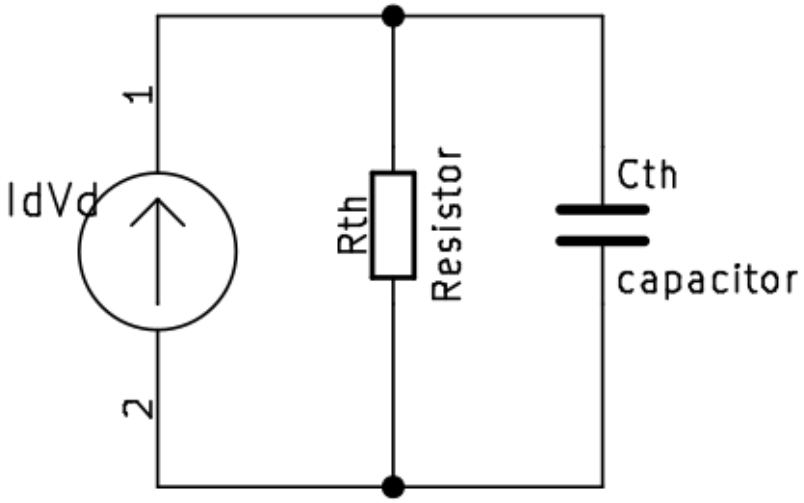


Fig 2.1. Equivalent circuit for self-heating simulation

CHAPTER-3

INTERCONNECT MODELING

3.1 Interconnect modeling:

The interconnect modeling mainly consists of metal interconnect and oxide below metal(FOX). The heat dissipation in any MOSFET(BSIMSOI) depends on the product of drain current(I_d) and applied voltage(V_{dd}), which decides the average channel temperature. The temperature, current, and power depend on each other. The temperature node at the device level is provided by the BSIMSOI model in the SPICE simulation. As mentioned in Chapter 2, to find R_{th0} normalized thermal resistance in BSIMSOI model, the temperature characteristics of the single SOI device are plotted in device simulator GENIUS . In the SPICE model *shmod* is kept ON and an arbitrary non zero value is given to R_{th0} so that T node is created. Thermal resistance equivalent to the electrical resistance of the BOX which is lying below the channel, is connected to the T node of the MOSFET and ground. Now that self-heating is on in SPICE model, we need to match its temperature characteristics with the temperature characteristics of Genius model by calibrating R_{th0} value. R_{th0} value is taken when both the temperature characteristics are matched exactly.

Simulation of two device circuit is done in a device simulator to verify if the above mentioned thermal modeling is sufficient or not. If the above model is sufficient then there has to be no heat flow from one device to the other.

3.2 Construction of device circuit in GENIUS:

The code is written to build the required device and give the required connections to the terminals. The code follows specific order of commands through which the device is built.

I. Global parameters such as Temperature, width etc are defined using command *GLOBAL*.

II. Mesh is generated as simulations are performed in a discrete mesh. Predefined mesh data structures(*Type=S_TRI3*) (triangular mesh) can be used to generate mesh using command *MESH*.

III. Various regions (such as drain, source, drain1 etc) are labeled with Cartesian co-ordinate system and material used in each region is specified using command *REGION*.

IV. Doping profile is defined, with Cartesian co-ordinate system using command *PROFILE*.

V. External sources used in the circuit are defined and each source is provided with id (name) using command *vsource*.

VI. Boundary conditions are specified, i.e., the type of boundary at the intersection of two different regions is specified (such as Insulator Interface, Ohmic contact, Gate contact etc) using the commands *boundary* and *contact*.

VII. The physical model of each material is loaded to the simulation system using *PMI* command.

VIII. Numerical solutions are obtained using different types of solvers after attaching external sources to the respective electrodes using *ATTACH*. *DDML2* method is used to select the level-two drift-diffusion equation solver, which includes the lattice temperature variation in device.

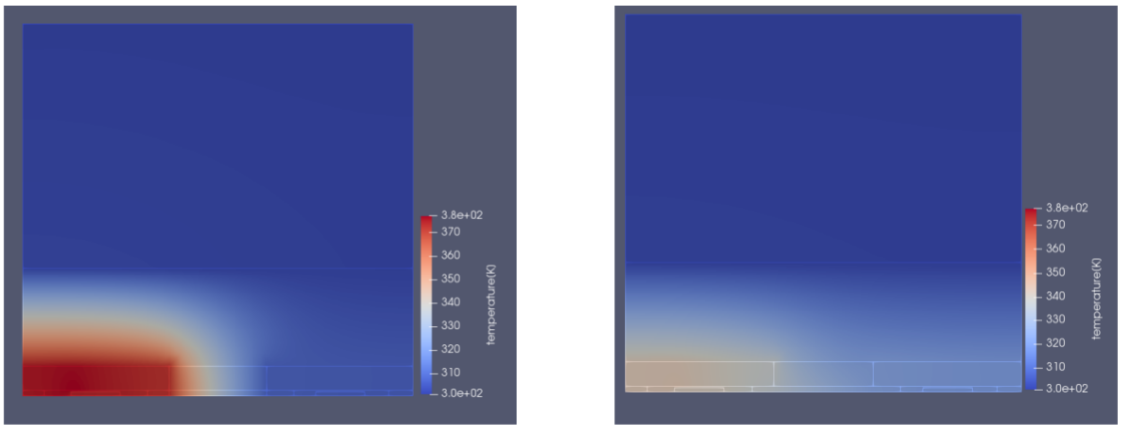
IX. The *SOLVE* command instructs Genius to solve the semiconductor device equations.

X. Using *EXPORT* command the obtained results can be exported into a file for further analysis.

The code used for construction of two device model in GENIUS is given in APPENDIX section.

In order to study the effect of interconnect and characterize the temperature of devices in a circuit, the two device circuit is implemented in GENIUS as shown in Fig 3.2. Fig 3.1a and Fig 3.1b show two SOI MOSFET built using 2-D GENIUS device tool where in Fig 3.1a the two SOI MOSFET are separated by silicon dioxide, while in Fig 3.1b it is

connected by metal interconnect. In both the cases only one device is ON while other one is OFF, drain voltage=1.5V, gate voltage=1.5V, width=200nm, channel length=180nm.



(a) Without metal interconnect (b) With metal interconnect

Fig 3.1. Temperature profiles of two device circuit in GENIUS

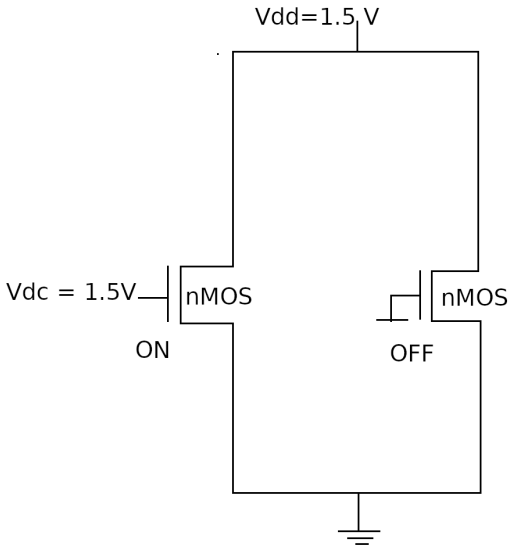


Fig 3.2. Two device circuit

Fig 3.1a shows two SOI MOSFETs which are adjacent to each other and are separated only by silicon dioxide, while in Fig 3.1b there is metal interconnect in between, along with the silicon dioxide layer and are under identical biased condition. It is clearly observed that the majority of trapped heat flows through the interconnect metal to the neighboring device in Fig 3.1b, hence decreasing the effective channel temperature as opposed to Fig 3.1a, where the heat is being trapped in the channel resulting in high device temperature. To obtain realistic electrical characteristics and thermal profile of the given circuit in SPICE,

the thermal network needs to be developed which provides the feedback to the electrical network. So, the heat flow through the interconnect metal to the neighboring device needs to be modeled in the thermal network.

The heat flow in interconnect lines is modeled by T-network as shown in Fig 3.3.

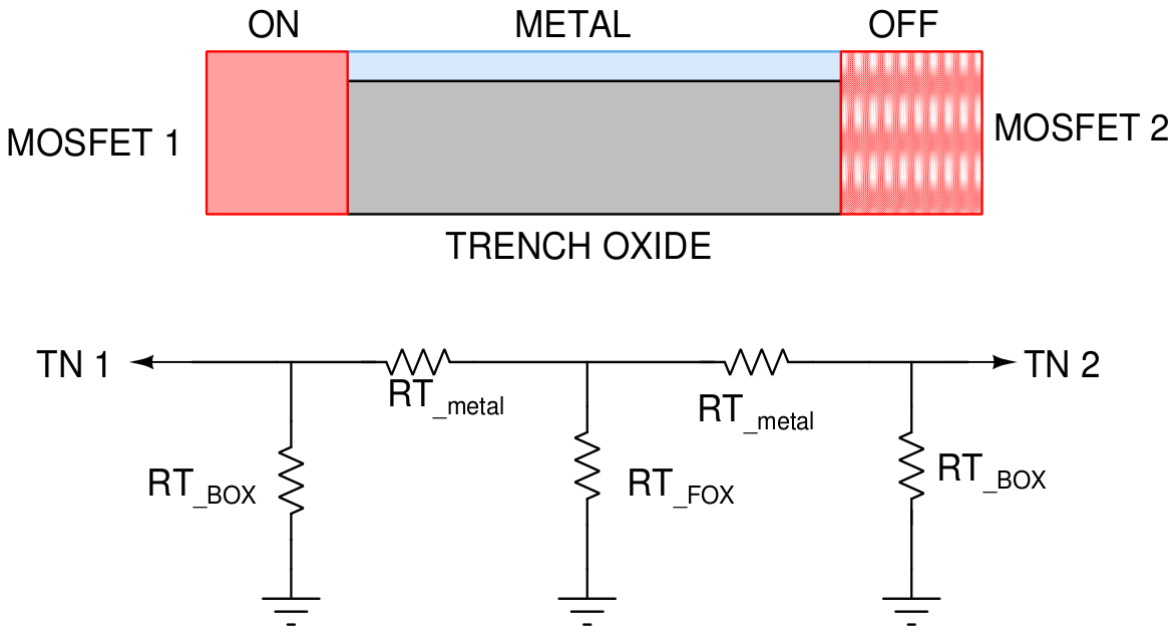


Fig 3.3. Interconnect Model

The interconnect can further be divided into k-regions i.e., k number of T network. (For simplicity we assumed k=1). One of the major problems with the BSIMSOI model is having a single temperature node [3] [2], which ignores the large temperature gradient in the silicon film, hence the interconnect lines cannot be modeled accurately. This problem can be solved by introducing an RT_{BOX} resistance in the thermal model.

Fig 3.3 shows the overall model, which consists of the T network that models the interconnect heat flow through metal, FOX and RT_{BOX} is introduced to overcome the limitation of single temperature node in BSIMSOI model.

Fig 3.4 shows the proposed algorithm for the electrothermal circuit simulation to obtain accurate electrical and thermal characteristics. Given that we have the layout of the circuit, the electrical parasitic netlist can be extracted and with the help of parasitic netlist, we can generate the thermal netlist. Together with electrical and thermal netlist now the other operations can be performed like DC analysis, AC analysis, temperature analysis etc.

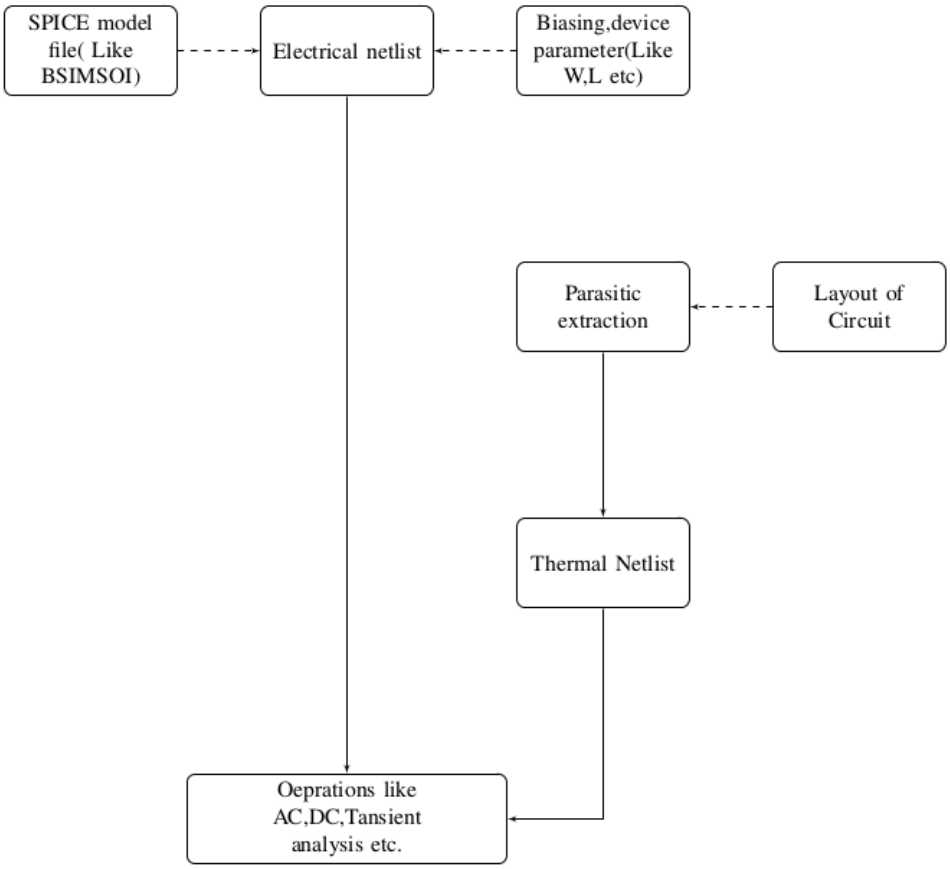


Fig 3.4. Flowchart

CHAPTER-4

RESULTS

4.1 Single device :

In order to study the characteristics of SOI MOSFET, an SOI nMOSFET is implemented in GENIUS with W = 0.4um and L = 0.2 um.

The output characteristics I_d vs V_{ds} are plotted after fixing V_{gs} = 1.5V and varying V_{ds} from 0 to 1.8 V with self heating effect on and off. The results plot is shown in Fig 4.1.

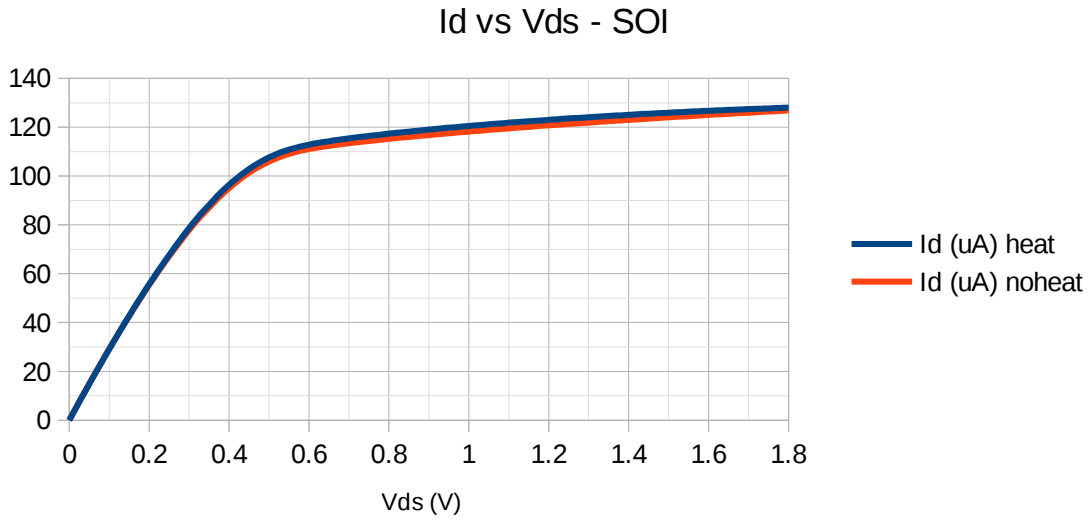


Fig. 4.1. Id vs Vds

The transfer characteristics I_d vs V_{gs} are plotted after fixing V_{ds} = 1.5V and varying V_{gs} from 0 to 1.8 V with self heating effect on and off. The results plot is shown in Fig 4.2.

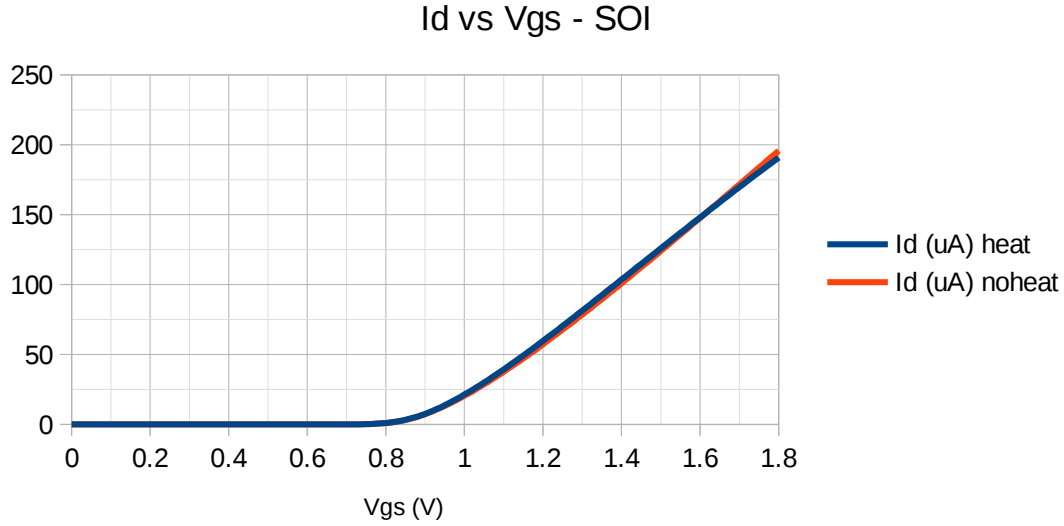


Fig. 4.2. Id vs Vgs

The current transfer characteristics plotted in device simulator GENIUS are plotted with self-heating kept on (using DDML2 solver). To match the performance of device in both device simulator and SPICE simulator, this current transfer characteristics are first matched to that in SPICE simulator by varying various parameters in BSIMSOI model file. To match the temperature characteristics R_{th0} normalized thermal resistance is calibrated such that temperature characteristics of the device are matched both in Device simulator and SPICE simulator, as discussed in Chapter 3. R_{th0} value obtained is **0.18797**.

After fixing the R_{th0} value, the single device characteristics (both current and temperature) of SPICE simulator match to that in device simulator GENIUS.

4.2 Two device:

Two device circuit is constructed as shown in the Fig 3.2 where one device is ON and the other is OFF.

The structure is built in GENIUS code, as explained in Chapter 3 and the sample code is added in APPENDIX. The idea here is to study the heat flow through the interconnect that connects ON device and OFF device and how the heat flow varies as the distance between the two devices is changed. Channel length of both devices is L = 0.2 µm and width W = 0.2 µm.

Hence, the interconnect length between the ON device and OFF device is varied and temperatures of ON device and OFF device obtained are tabulated below.

Interconnect Length (in µm)	ON device Temperature (in °C)	OFF device Temperature (°C)
0.2	86.7	44.5
0.4	97.7	34.3
0.6	104.6	28.4
0.8	109.4	24.4
1	112.9	21.6

Table 4.1. Device Temperature

It is observed that as the distance between ON device and OFF device increases, the heat flow from ON device to OFF device decreases.

CHAPTER-5

CONCLUSION

Self-heating in SOI devices is a concern and it needs to be modeled perfectly to study the performance of the devices. The modeling of the T node holds good for single device circuit only. In the circuits with multiple devices heat generated in one device can flow through the interconnect metal and the oxide below to the neighboring device. To get a realistic temperature profile as well as electrical characteristics of the circuit apart from the device level model, the interconnect coupling between the devices and other heat losses must be taken into account in SPICE model.

In an attempt to perform Electothermal simulation for SOI MOSFET based circuits and obtain accurate electrical and thermal characteristics, it is found that the heat modeling which uses BSIMSOI model holds good only for single device because in multiple device circuits heat flow is observed from ON device to OFF device through the interconnect and the oxide below and hence the equivalent thermal resistance of the interconnect and the oxide needs to be incorporated in the circuit by forming the T-network in order to obtain accurate Thermal and Electrical characteristics.

REFERENCES

[1] H. Kopka and P. W. Daly, *"A Guide to L A TEX"*, 3rd ed. Harlow, England:Addison-Wesley, 1999

[2] Yu, F., Cheng, M. -. (2007). *"Electrothermal simulation of SOI CMOS analog integrated circuits."* Solid-State Electronics, 51(5), 691-702. doi:10.1016/j.sse.2007.02.029

[3] Yu, F., Cheng, M. -., Habitz, P., Ahmadi, G. (2004). *"Modeling of thermal behavior in SOI structures. IEEE Transactions on Electron Devices,"* 51(1), 83-91. doi:10.1109/TED.2003.820939

[4] "BSIM model UC Berkley". *Device.eecs.berkley.edu,2020,* https://www-device.eecs.berkely.edu/ bsimsoi

[5] Yu, F., Cheng, M. -. (2004). *"Application of heat flow models to SOI current mirrors."* Solid-State Electronics, 48(10-11 SPEC. ISS.), 1733-1739. doi:10.1016/j.sse.2004.05.007

[6] Teng, C. -., Cheng, Y. -., Rosenbaum, E., Kang, S. -. (1997). *"ITEM:A temperature-dependent electromigration reliability diagnosis tool"* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 16(8), 882-893.doi:10.1109/43.644613

[7] Bilotti, A. A. (1974). *"Static temperature distribution in IC chips with isothermal heat sources."* IEEE Transactions on Electron Devices, 21(3), 217-226. doi:10.1109/T-ED.1974.17899 Schafft, H. A. (1987)

[8] hen, D., Li, E., Rosenbaum, E., Kang, S. -. (2000). *"Interconnect thermal modeling for accurate simulation of circuit timing and reliability."* IEEE Transactions on Computer-Aided Desgn Integr. Circuits systems,vol.19,np.2,pp.197-205,Feb. 2000

[9] Banerjee, K., Mehrotra, A., Sangiovanni-Vincentelli, A., Hu, C.(1999). *"On thermal effects in deep sub-micron VLSI interconnects."* Proceedings - Design Automation Conference, , 885-891

[10] Cheng, Y. -., Raha, P., Teng, C. -., Rosenbaum, E., Kang, S. -.(1998). *"ILLIADS-T: An electrothermal timing simulator for temperature-sensitive reliability diagnosis of CMOS VLSI chips."* IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 17(8),668-681. doi:10.1109/43.712099

[11] Sabry, M. -., Bontemps, A., Aubert, V., Vahrmann, R. (1997). *"Realistic and efficient simulation of electro-thermal effects in VLSI circuits."* IEEE Transactions on very Large Scale Integration (VLSI) Systems, 5(3), 283-289. doi:10.1109/92.609871

[12] Wünsche, S., Clauß, C., Schwarz, P., Winkler, F. (1997). *"Electro-thermal circuit simulation using simulator coupling."* IEEE Transactions on very Large Scale Integration (VLSI) Systems, 5(3), 277-282.doi:10.1109/92.609870

[13] Leung, K. N., Mok, P. K. T. (2003). *"A CMOS voltage reference based on weighted VGS for CMOS low-dropout linear regulators."* IEEE Journal of Solid-State Circuits, 38(1), 146-150. doi:10.1109/JSSC.2002.806265

[14] Pedram, M., Nazarian, S. (2006). *"Thermal modeling, analysis, and management in VLSI circuits: Principles and methods."* Proceedings of the IEEE, 94(8), 1487-1501. doi:10.1109/JPROC.2006.879797

[15] Ko, P., Huang, J., Liu, Z., Hu, C. (1993). *"BSIM3 for analog and digital circuit simulation."* IEEE Symp.on VLSI Technology CAD, 400-429

[16] Zhang, K., Cheng, M. -. (2010). *"Thermal circuit for SOI MOSFET structure accounting for nonisothermal effects."* IEEE Transactions on Electron Devices, 57(11), 2838-2847. doi:10.1109/TED.2010.2068391

[17] P. Su, S. K. H. Fung, S. Tang, F. Assaderaghi and C. Hu, *"BSIMPD: A Partial-Depletion SOI MOSFET Model for Deep-Submicron CMOS Designs"* , Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, pp.197-200

[18] Chester, G. V., Thellung, A. (1961). *"The law of wiedemann and franz"*. Proceedings of the Physical Society, 77(5), 1005-1013. doi:10.1088/0370-1328/77/5/309

[19] Burzo, M. G., Komarov, P. L., Raad, P. E. (2003). *"Thermal transport properties of gold-covered thin-film silicon dioxide."* IEEE Transactions on Components and Packaging Technologies,26(1), 80-88.doi:10.1109/TCAPT.2003.811467

[20] Wang, T. -., Chen, C. C. -. (2004). *"SPICE-compatible thermal simulation with lumped circuit modeling for thermal reliability analysis based on modeling order reduction."* Paper presented at the Proceedings - 5th International Symposium on Quality Electronic Design, ISQUED 2004,357-362.

[21] Jeon, J., Jhon, H. -., Kang, M. (2018). *"Circuit modeling of the electro-thermal behavior of nanoscale bulk-FinFETs."* Journal of Computational Electronics, 17(1), 146-152. doi:10.1007/s10825-017-1058-8

[22] *"BSIMSOI3.2 Users' Manual"*, UC Berkeley, Department of EECS.

[23] *"Genius Semiconductor Device Simulator"*. *Cogenda.Com*, 2020, https://www.cogenda.com/article/Genius.

[24] *"Wiedemann–Franz Law." Wikipedia*, Wikimedia Foundation, 7 June 2020, en.wikipedia.org/wiki/Wiedemann–Franz_law.

APPENDIX

Sample 2 device code:

```
#============================================================
=========

# Genius example: SOI heat effect simulation

# We simulate drain-source current of SOI transistor

# with DDML1 and lattice temperature corrected DDML2 solver.

#============================================================
==========

GLOBAL  T=300 Z.width=0.4

MESH   Type=S_TRI3  Triangle="pzA"

X.MESH WIDTH=0.2 H1=0.050 H2=0.010

X.MESH WIDTH=0.2 H1=0.010 H2=0.010

X.MESH WIDTH=0.2 H1=0.010 H2=0.050

X.MESH WIDTH=0.2 H1=0.050 H2=0.010

X.MESH WIDTH=0.2 H1=0.010 H2=0.010

X.MESH WIDTH=0.2 H1=0.010 H2=0.050

X.MESH WIDTH=0.2 H1=0.050 H2=0.010

X.MESH WIDTH=0.2 H1=0.010 H2=0.010


Y.MESH N.SPACES=10 Y.TOP=-0.03 Y.BOTTOM=0

Y.MESH DEPTH=0.1 H1=0.010 H2=0.010

Y.MESH DEPTH=0.4 H1=0.05

Y.MESH DEPTH=1.0 H1=0.05 H1=0.1


REGION Label=Gate_Ox   Y.TOP=-0.02 Y.BOTTOM=0.0     Material=SiO2

REGION Label=Device    Y.TOP=0.0   Y.BOTTOM=0.1 X.MIN=0.0 X.MAX=1.6 Material=Si

REGION Label=Device1    Y.TOP=0.0   Y.BOTTOM=0.1 X.MIN=1 X.MAX=1.6 Material=Si

REGION Label=Buried_Ox Y.TOP=0.1   Y.BOTTOM=0.5     Material=SiO2
```

REGION Label=Buried_Ox1 Y.TOP=0.0 Y.BOTTOM=0.1 X.MIN=0.6 X.MAX=1 Material=SiO2

REGION Label=Bulk Y.TOP=0.5 Y.BOTTOM=1.5 Material=Si

REGION Label=Source X.MIN=0.0 X.MAX=0.1 Y.BOTTOM=0.0 Y.TOP=-0.02 Material=Elec

REGION Label=Gate X.MIN=0.2 X.MAX=0.4 Y.BOTTOM=-0.002 Y.TOP=-0.02 Material=Elec

REGION Label=Drain X.MIN=0.5 X.MAX=1.1 Y.BOTTOM=0.0 Y.TOP=-0.02 Material=Al

REGION Label=Source1 X.MIN=1.5 X.MAX=1.6 Y.BOTTOM=0.0 Y.TOP=-0.02 Material=Elec

REGION Label=Gate1 X.MIN=1.2 X.MAX=1.4 Y.BOTTOM=-0.002 Y.TOP=-0.02 Material=Elec

#REGION Label=Drain1 X.MIN=1 X.MAX=1.1 Y.BOTTOM=0.0 Y.TOP=-0.02 Material=Elec

FACE Label=Substrate Location=BOTTOM

#---

doping profile

DOPING Type=analytic

#substrate

PROFILE Ion=Acceptor N.PEAK=1.7E17 Type=Uniform X.MIN=0.0 X.MAX=1.6 Y.TOP=0.0 Y.BOTTOM=0.1

PROFILE Ion=Acceptor N.PEAK=6E16 Type=Uniform X.MIN=0.0 X.MAX=1.6 Y.TOP=0.5 Y.BOTTOM=1.5

#Uniform doping for source

PROFILE Ion=Donor Type=Uniform N.PEAK=2E18 X.MIN=0.0 X.MAX=0.2 Y.TOP=0.0 Y.BOTTOM=0.1

#Uniform doping for drain

PROFILE Ion=Donor Type=Uniform N.PEAK=2E18 X.MIN=0.4 X.MAX=0.6 Y.TOP=0.0 Y.BOTTOM=0.1

#Uniform doping for source1

PROFILE Ion=Donor Type=Uniform N.PEAK=2E18 X.MIN=1.5 X.MAX=1.6 Y.TOP=0.0 Y.BOTTOM=0.1

#Uniform doping for drain1

PROFILE Ion=Donor Type=Uniform N.PEAK=2E18 X.MIN=1 X.MAX=1.1 Y.TOP=0.0 Y.BOTTOM=0.1

#--

vsource Type = VDC ID = GND Tdelay=0 Vconst=0

vsource Type = VDC ID = VCC Tdelay=0 Vconst=1.5

vsource Type = VDC ID = VGATE Tdelay=0 Vconst=1.5

vsource Type = VDC ID = VGATE1 Tdelay=0 Vconst=0

#--

specify boundary condition.

boundary Type = InsulatorInterface ID=Device_to_Gate_Ox QF=0

boundary Type = InsulatorInterface ID=Buried_Ox_to_Device QF=0

boundary Type = InsulatorInterface ID=Bulk_to_Buried_Ox QF=0

boundary Type = InsulatorInterface ID=Buried_Ox1_to_Device QF=0

boundary Type = InsulatorInterface ID=Buried_Ox1_to_Device1 QF=0

boundary Type = InsulatorInterface ID=Device1_to_Gate_Ox QF=0

contact Type = GateContact ID=Gate WorkFunction=5 Heat.Transfer=0

contact Type = OhmicContact ID=Source Heat.Transfer=1e4

contact Type = OhmicContact ID=Drain Heat.Transfer=1e4

contact Type = GateContact ID=Gate1 WorkFunction=5 Heat.Transfer=0

contact Type = OhmicContact ID=Source1 Heat.Transfer=1e4

#contact Type = OhmicContact ID=Drain1 Heat.Transfer=1e4

boundary Type = OhmicContact ID=Substrate Heat.Transfer=1e4 Ext.Temp=300

PMI Region=Device Type=Mobility Model=Lucent

PMI Region=Bulk Type=Mobility Model=Constant

#--

```
# compute a initial distrubution of p and n

#REFINE.C  Region=Device Variable=Doping Measure=SignedLog cell.fraction=0.2

METHOD   Type = Poisson     NS=Basic  LS=GMRES

SOLVE    Type = EQUILIBRIUM

EXPORT   CGNSFile=soi_init_new.cgns  VTKFile=soi_init_new.vtu

#set gate bias by dcsweep method
#=============================================================
=========

METHOD   Type = DDML1   NS=Basic  LS=LU

SOLVE    Type=DCSWEEP VScan=Gate VStart=0.0 VStep=0.01 VStop=0.1

EXPORT   CGNSFile=gate_new.cgns

IMPORT   CGNSFile=gate_new.cgns

ATTACH   Electrode=Gate Vapp=VGATE

ATTACH   Electrode=Gate1 Vapp=VGATE1

ATTACH   Electrode=Source Vapp=GND

ATTACH   Electrode=Source1 Vapp=GND

ATTACH   Electrode=Drain Vapp=VCC

#ATTACH   Electrode=Drain1 Vapp=GND

# we use ddm solver with lattice heating here.

METHOD   Type = DDML2    NS=Basic  LS=LU Toler.relax=1e5 Maxit=150

SOLVE    Type=DCSWEEP VScan=Gate VStart=0 VStep=0.01 VStop=1.8 out.prefix=drain_ht

#SOLVE Type=Transient TStart=0 TStep=1e-12 TStepMax=1e-6 TStop=100e-6
out.prefix=drain_ht1

EXPORT   VTKFile=soi_heat_new.vtu

END

#=============================================================
=========
```