Impact of Material Parameters on the Performance and Scaling of $Ge_2Sb_2Te_5$ Phase Change Memory Devices

A PROJECT REPORT

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CERTIFICATE

This is to certify that the project titled "**Impact of Material Parameters on the Performance and Scaling of $Ge_2Sb_2Te_5$ Phase Change Memory Devices**" being submitted to the Indian Institute of Technology Madras by **Bhanwar Lal Rawal (EE18M020)**, in partial fulfilment of the requirements for the award of the degree of **Master of Technology** in **Microelectronics and Photonics** in **Electrical Engineering** is a bonafide record of work carried out by him/her under my supervision. The contents of this project report, in full or in parts, have not been submitted to any other institute or university for the award of any degree or diploma.

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ABSTRACT

Phase Change Memory is a memory that is working on the principle of switching mechanism between crystalline and amorphous states of the material. During the fabrication of the device, composition of the phase change material alloy (GST) can fluctuate from its nominal value when there is a fluctuation in any of the process parameters using physical vapour deposition technique (e.g. deposition temperature, chamber pressure/process vacuum, Argon flow rate, sputtering rate). The resultant change in the material composition directly affects the material parameters such as lattice heat capacity, thermal conductivity, electrical resistivity, melting temperature, glass transition temperature etc. These material parameter affect the resistance of crystalline and amorphous state (R_{SET}, R_{RESET}) during programming, power consume by the material to switch between the states, radius of amorphous dome (U_a).

In the project, most and least significant input material parameter are measured on basis of their sensitivity to affect the output programming parameters of the material (R_{RESET}, R_{SET}, P_{RESET}, U_a) and rank them on basis of their sensitivity to affect the programming of the device.

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3.2 The overall ranking of the input variables between 50 nm and 10 nm HR devices by considering all the output factors simultaneously. The overall ranking is based on the average of the absolute value of the coefficients associated with the individual input parameter obtained from all the output factors.

Chapter 1

INTRODUCTION

1.1 Requirements of Emerging Non-Volatile Memory Technology

In fastest growing digital world, everything is happening fast. In this digital world, rate of data generation is increasing day by day. Since more and more data is generating everyday, our requirement of data storage capacity is increasing with fast speed. In this situation everyone wants computer, mobiles and any other electronic gadgets with fast speed and large data storage capacity. In this situation we need a new memory technology with higher data storage capacity, fast read-write speed, high endurance and high data retention capacity with low power consumption. There are several types of emerging memory technology like Phase Change Memory (PCM), Magnetoresistive Random Access Memory (MRAM), Ferroelectric Random Access Memory (FeRAM), Resistive Random Access Memory (RRAM), 3D-Crosspoint Memory (3D-XPoint).

Phase change memory is one of the promising candidate for storage class technology to replace the conventional memory technology because PCM have a multi bit data storage capacity with fast switching speed.

1.2 Phase Change Memory

Phase change memory is a high speed, non-volatile memory with high endurance and high data retention capacity with low power consumption. As it is very clear with the name phase change that there should be changes between the different phases of the material (crystalline and amorphous) by applying voltage/current pulse. Crystalline state (low resistance state) of the material is called as SET state as well as amorphous state (higher resistance state) of the material is called as RESET state. Initially phase change material Ge2Sb2Te5 is found to be in crystalline state. It will switch from crystalline state to amorphous by applying large amplitude voltage pulse with short period of time. Similarly to switch from amorphous state to crystalline state we need to apply short amplitude voltage pulse with large time period. Here low resistance crystalline state is considered as to store binary logic-1 in it as well as high resistance amorphous state is considered as to store binary logic-0 in it[1].

1.2.1 Working Principle

Initially material is found to be in crystalline state. It is low resistance state because all atoms are arranged in a particular order so it is also called as ordered state. Since all atoms are arranged in a regular sequence, there is no any (ideally) disordered atom available in between the crystal structure so there is no any (ideally) trap state found in the crystal state. Since there is no any trap state available, conductivity of the material is high and resistivity is low. In amorphous state, all atoms are disordered so there are large number of trap states are available. Because of trap states, electrons will face

multiple capture and release by trap states so this is cause of reduce in conductivity and increase in resistivity. In the crystalline state resistivity is of the order of KΩ as well as in the amorphous state resistivity is of the order of MΩ.

Initially apply RESET voltage pulse with high amplitude and short time period on the crystalline state so GST material will heat up above melting temperature by joule's heating through heater. This leads GST material to get melted. In this state all atoms gets disordered, at this time drastically cool down the material so it will switch to amorphous state by melt-quench process. Here resistance of the material is high compared to crystalline state because of disordered atoms. Similarly to switch from amorphous state to crystalline state, apply SET voltage pulse having small amplitude for large time period so material will heat up above crystalline temperature so all atoms will try to become ordered and material will comes to its initial crystalline state where resistance of material is low. Crystalline temperature is always less then melting temperature.

The programming pulse parameters for the RESET and SET operation for 50 nm HR device are 1.5 mA, 1 ns/20 ns/1 ns and 800 μA, 10 ns/100 ns/10 ns (I, tr/tw/tf) and for 10 nm HR device, RESET and SET pulse parameters are 220 μA, 1 ns/20 ns/1 ns and 120 μA, 10 ns/100 ns/10 ns (I, tr/tw/tf) respectively. 1 nA, 500 ns (I, t) is used for read pulse follow for each programming pulse[14].

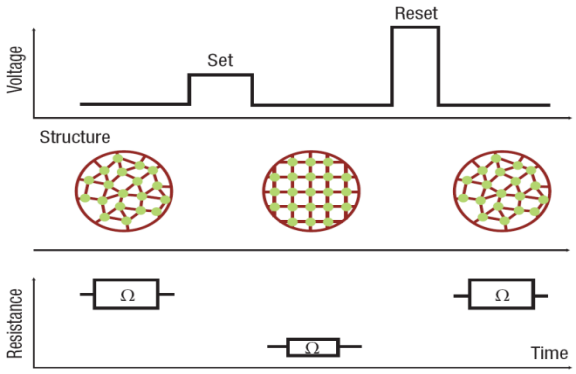

Figure 1.1: Switching mechanism of PCM from amorphous to crystalline by applying SET pulse (short amplitude pulse) and from crystalline to amorphous by applying RESET pulse (large amplitude pulse)[1].

1.2.2 Structure

There are various kind of structure of phase change memory cell but in the project I use mushroom type structure. In the structure, phase change material is active material alloy Ge2Sb2Te5, top and bottom electrode are of tungsten (W), heater is of material TiN and SiO2 is used as insulator. The active phase change material is in contact with TiN from top and bottom side but bottom side TiN is used as heater because its resistivity is high because area is low as its small radius. Heater is always covered with insulator so no heat will losses outside the device and maximum fraction of the active phase change material will change their phase. Another side of heater is connected with tungsten (W) known as bottom electrode similarly top electrode is also formed on the top of TiN. Here heater radius HR is always smaller than radius of active phase change material in appropriate ratio. In the structure top and bottom electrode provides electrical contact to the device.

Initially material is in crystalline state so whenever current pulse passes through the device, heater will heat up above melting temperature so active phase change material connected with heater will heat up and get melted then converted to amorphous state. Since heat flow in the active material is equal in all direction so it will melted equally and will convert to amorphous state equally in all direction. This amorphous state gets a structure like hemisphere on the heater so this structure is looks like mushroom. This is the reason to called this structure as mushroom type structure.

In the figure 1.2a showing 3-D structure of PCM device cell in cylindrical coordinates (r, ɵ and z). Figure 1.2b is half device structure in 2-D cylindrical coordinates (r and z).

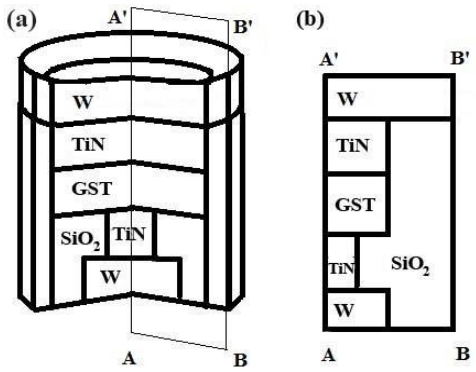

Figure 1.2: 3-D schematic of a mushroom-type PCM device. (a) The cylindrical device structure exhibits rotational symmetry (left). (b) The half device structure is simulated using cylindrical coordinates (right)[14].

1.3 Challenges of Phase Change Memory

There are various challenges in the phase change memory. Here focusing on one of the key challenge of phase change memory e.g. resistance drift effect. In the amorphous state of the GST material resistance increases over time, this phenomenon is known as resistance drift.

Characterization of resistance drift in amorphous chalcogenide materials GST is done by various experiments and found that the characterization methods are mostly based on an empirical model, in which the resistance of amorphous chalcogenide follows a power-law increase over time.

$$R(t) = R(t_0)(t/t_0)^{\wedge}v$$

Where: R(t) = Resistance after time t.

R(t0) = Initial resistance at time t=0.

v = Drift Coefficient

Here drift coefficient v is a main factor that affect the programming of the cell. Drift coefficient for programmed cell lies between the range of 0.03 -0.11[8], depending on the material and device type etc. Drift coefficient v also varies with other factors, such as temperature, readout current, mechanical stresses and the size of amorphous fraction within the cell[8][6].

Effect of drift coefficient and time on resistance is shown in figure 1.3. Here it showing that resistance of each level is increasing as drift coefficient is increase. Resistance is also increasing with time for large drift coefficient but for small drift coefficient it almost constant over time.

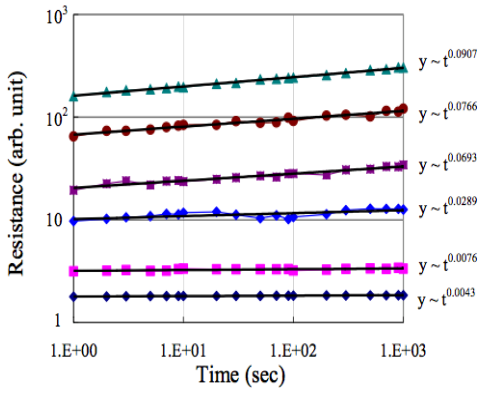

Figure 1.3: Drift coefficient (i.e., exponential term of t) varies with different resistance levels at room temperature right after programming[8].

As it is very clear with figure 1.3 that drift coefficient increases for different resistance level increase but in figure 1.4 showing that drift coefficient is reducing with

increase in readout current. For small readout current 10nA, ν is increase over temperature but for 100nA readout current, ν is almost constant but by further increase in readout current 1uA, drift coefficient (ν) is decreasing over temperature.

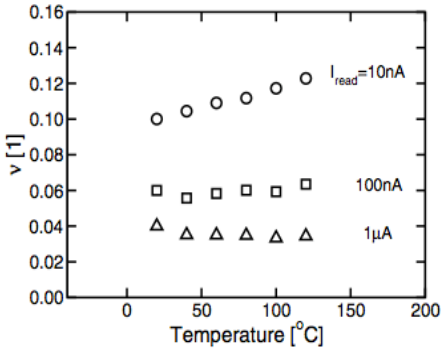

Figure 1.4: Measured drift coefficient ν varies with temperature and readout current[8].

This effect is hamper for multi bit storage because there are some intermediate resistance states are available so when resistance is increase with time there will be shifting in the resistance of intermediate states. Due to shifting, overlapping of the intermediate state resistance will be there, this cause of information loss. But for single bit storage, this effect is not hampering because there is only two states so no shifting of resistance will be there.

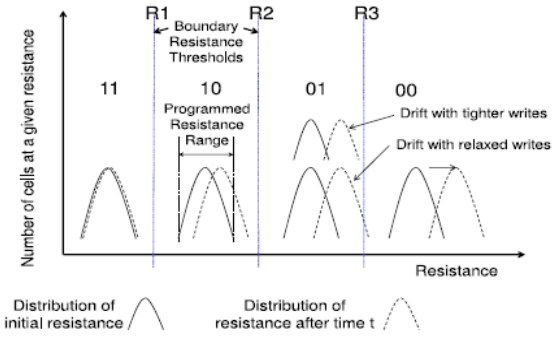

Figure 1.5: Distribution of Initial Programmed Resistance and Resistance after Drift (For 2-bit programming)[18]

1.4 Motivation

Phase change material is ternary alloy so the composition of the alloy phase change material (GST) can fluctuate from its nominal value when there is a fluctuation in any of the process parameters using physical vapour deposition technique (e.g. deposition temperature, chamber pressure/process vacuum, Argon flow rate, sputtering rate). The resultant change in the material composition directly affects the material parameters such as lattice heat capacity, thermal conductivity, electrical resistivity, melting temperature, glass transition temperature (parameters are not exhaustive).

For phase change material GST, it is very difficult to achieve the desired composition ($Ge_2Sb_2Te_5$) with the fluctuating process parameters, and hence, the change in material parameters is unavoidable. The aforementioned reasons are also applicable to metallic nitride alloys (Ti_xN_{1-x}), which is used as a heater material in PCM devices and there could be a deviation in these alloys.

Since the material parameter are disturbed, these disturbed material parameters can affect the performance of the phase change memory devices by affecting the different performance parameters including RESET resistance (R_{RESET}), SET resistance (R_{SET}), RESET power (P_{RESET}) and amorphous dome thickness (U_a).

It is very challenging to probe the most significant material parameters that can affect the programming of PCM devices thorough experimental investigation. However, TCAD simulations are highly helpful and robust to provide insights into the programming characteristics of PCM devices by intentionally changing the material parameters to a certain percentage, ± 5% (assuming there is a composition variation).

By exploiting Plackett-Burman design of experiment method, the linear regression (first order equation) is formed between input and output variables. The weights of the coefficient from the equation decide whether the input material parameter is least sensitive or most sensitive to the corresponding output performance parameter.

1.5 Objectives

The goal of the project is to measure the effect of various material parameters such as lattice heat capacity, thermal conductivity, electrical resistivity, melting temperature, glass transition temperature on the programming parameter R_{RESET}, R_{SET}, P_{RESET} and U_a and rank them on basis of their sensitivity to affect the programming parameters for actual device (HR=50nm) and scaled down device (HR=10nm).

During the switching process, resistance of both states gets affected by material parameters. Since power is proportional to resistance so due to variation in resistance, power consumption is also affected. So in this project I have to measure that which material parameter is more affecting the resistance and power of the material in both crystalline and amorphous states.

Chapter 2

SIMULATION APPROACH AND DEVICE CALIBRATION

2.1 Simulation Methodology

In this section, simulation process is explained step by step. These steps involved in forming the linear relation between input and output variables of the device with varying material parameters. These are discussed as following:

Step 1: Initially design the PCM device structure with appropriate structure parameter like heater radius (HR), heater height, GST radius, GST thickness etc. Now apply RESET and SET pulse with nominal pulse parameters so device will start working. In this stage material parameters have its nominal value. These material parameters are known as input parameters.

Step 2: Now introduce small variation (± 5%) in input parameters, where +5% is showing increase in nominal value of parameter by 5% and -5% is showing decrease in nominal value of parameter by 5%.

Step 3: Since there are many possible combinations (2^7 combinations) for 7 input parameters. PB-DoE is employed, which gives 12 most appropriate combinations for 7 input parameters.

Step 4: Use 12 input combinations for device simulation to extract all output parameters for 12 different input combinations by TCAD Sentaurus.

Step 5: Now use all 12 input-output combinations to calculate the coefficients corresponds to each input parameters for each output parameter by using linear regression technique. Use a statistical tool (IBM-SPSS Statistics 20) to perform a linear regression technique to obtain the first-order equation in the following form:

$$y = A.x_1 + B.x_2 + C.x_3 + \ldots\ldots + constant \quad (1)$$

Where y is the output variable, x_1, x_2, x_3 are the input variables and A, B, C are the coefficients of the corresponding input parameter.

The impact of the variations on each of the output parameters, R_{RESET}, R_{SET}, P_{RESET} and U_a is observed using linear regression. Assuming, there are k input variables and m output responses, then y_j can be given by,

$$y_j = \beta_{j\_0} + \beta_{j\_x1}.x_1 + \beta_{j\_x2}.x_2 + \ldots. + \beta_{j\_xk}.x_k \quad (2)$$

Where j takes value from 1 to m, all the β's are corresponding coefficients.

In this case, there are 7 input variables x, and 4 response parameters y. The input and response parameters are given as,

$$x = \{T_m, T_g, C_{v\_GST}, k_{\_GST}, C_{v\_TiN}, \rho_{\_TiN}, k_{\_TiN}\}$$

$$y = \{R_{RESET}, R_{SET}, P_{RESET}, U_a\}$$

For example, R_{SET} written in terms of equation (2) can be modeled as,

$$R_{SET} = \beta_{R\_SET\_0} + \beta_{R\_SET\_Tm}.T_m + \beta_{R\_SET\_Tg}.T_g + \beta_{R\_SET\_Cv\_GST}.\ C_{v\_GST} + \beta_{R\_SET\_k\_GST}.$$

$$k_{\_GST} + \beta_{R\_SET\_Cv\_TiN}.\ C_{v\_TiN} + \beta_{R\_SET\_k\_TiN}.\ k_{\_TiN} + \beta_{R\_SET\_\rho\_TiN}.\ \rho_{\_TiN} \quad (3)$$

The other responses, R_{RESET}, P_{RESET} and U_a can be modeled in a similar way[14][17].

Based on the value of coefficients, the input parameters can be ranked for each response as rank 1 for most significantly affecting the particular response, and the last rank considered as the least significant affecting parameter.

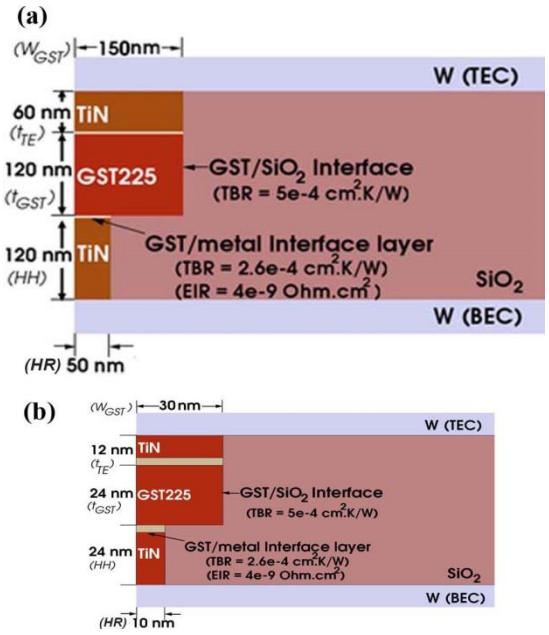

Figure 2.1: Device structures of the mushroom-type PCM device used to study the impact of process-induced variability. (a) 50 nm heater radius (HR) device. (b) An isotropically scaled-down device of a 10 nm HR device[14].

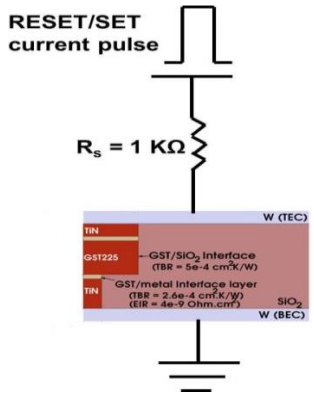

Figure 2.2: The circuit setup used for the transient simulation of the PCM device. The setup consists of a PCM cell (50 nm/10 nm heater radius device) connected to an external resistor of 1KΩ, where the RESET/SET current pulse is applied.[14]

2.2 Material Parameters for PCM Device Simulation

Materials	Thermal conductivity (W/K.cm)	Lattice heat capacity ($J/K.cm^3$)
amorphous GST	0.002	1.25
crystalline GST	0.005	1.25
TiN (heater)	0.12	0.3235
TiN (top electrode)	0.13	3.235
W	1.75	2.58
SiO_2	0.014	3.1

Table 2.1: Thermal parameters used for the PCM simulation of Mushroom-type Phase change memory devices[14]

2.3 PB-DoE Pattern for 7-Input Variables

For 7-input parameters, 128 combinations are possible. Out of these combinations PB-DoE generate 12 most appropriate combinations.

Input variables / Runs	C_{v_GST} (J/Kcm^3)	k_{GST} (W/K.cm)	T_m (K)	T_g (K)	k_{heater} (W/K.cm)	C_{v_heater} (J/Kcm^3)	ρ_{heater} (Ω.cm)
1	+	+	-	+	+	+	-
2	+	+	-	-	-	+	-
3	+	+	+	-	-	-	+
4	+	-	+	+	-	+	+
5	+	-	+	+	+	-	-
6	+	-	-	-	+	-	+
7	-	+	+	-	+	+	+
8	-	+	+	+	-	-	-
9	-	+	-	+	+	-	+
10	-	-	+	-	+	+	-
11	-	-	-	+	-	+	+
12	-	-	-	-	-	-	-

Table 2.2: 12 runs PB-DoE pattern for 7 input variables. The 12 different input combinations are used to test the device capability for the RESET and SET programming by using the pulse parameters of the nominal device (+ represents +5% increase in nominal value; - represents -5% decrease in nominal value).

2.4 Variation in Nominal Value of Material Parameters

Material Parameters	original device/scaled-down device	
	Nominal value	Range (± 5 %)
GST melting Temperature (T_m)	880 K	836 to 924 K
GST glass transition Temperature (T_g)	550 K	522.5 to 577.5 K
GST lattice heat capacity (C_{v_GST})	1.25 J/K.cm^3	1.1875 to 1.3125 J/K.cm^3
GST thermal conductivity ($k_{\_GST}$)	5e-3 W/K.cm	4.75e-3 to 5.25e-3 W/K.cm
TiN lattice heat capacity (C_{v_TiN})	0.3235 J/K.cm^3	0.307325 to 0.339675 J/K.cm^3
TiN thermal conductivity ($k_{\_TiN}$)	0.12 W/K.cm	0.114 to 0.126 W/K.cm
TiN electrical resistivity ($\rho_{\_TiN}$)	2.5e-3 Ω.cm	2.375e-3 to 2.625e-3 Ω.cm

Table 2.3: Ge2Sb2Te5 and TiN heater material parameters of the original device (50 nm heater radius) and scaled-down device (10 nm heater radius) showing their respective nominal values and their variation in the range of ± 5%. The material parameters are assumed to be same for both the devices.

2.5 Performance Metrics for 12-Input Combinations

2.5.1 For 50 nm HR Device:

Table represents the output parameters extracted for the 12 different input combinations for the 50 nm HR device.

Runs	C_{v_GST} (J/Kcm3)	$k_{\_GST}$ (W/K.cm)	T_m (K)	T_g (K)	$k_{\_heater}$ (W/K.cm)	C_{v_heater} (J/Kcm^3)	$\rho_{\_heater}$ (Ω.cm)	R_{RESET} (MΩ)	R_{SET} (KΩ)	P_{RESET} (mW)	U_a (nm)
1	1.3125	0.00525	836	577.5	0.126	0.339675	0.002375	0.979	6.3	3.675	66.5
2	1.3125	0.00525	836	522.5	0.114	0.339675	0.002375	0.928	5.99	3.66	66.7
3	1.3125	0.00525	924	522.5	0.114	0.307325	0.002625	0.062	4.19	3.69	47.3
4	1.3125	0.00475	924	577.5	0.114	0.339675	0.002625	0.0635	4.53	3.69	47.3
5	1.3125	0.00475	924	577.5	0.126	0.307325	0.002375	0.0589	4.27	3.66	46.9
6	1.3125	0.00475	836	522.5	0.126	0.307325	0.002625	0.926	6.02	3.72	66.4
7	1.1875	0.00525	924	522.5	0.126	0.339675	0.002625	0.0633	4.04	3.705	46.9
8	1.1875	0.00525	924	577.5	0.114	0.307325	0.002375	0.0659	4.35	3.63	47
9	1.1875	0.00525	836	577.5	0.126	0.307325	0.002625	1	6.33	3.72	67.9
10	1.1875	0.00475	924	522.5	0.126	0.339675	0.002375	0.06083	3.92	3.645	46.5
11	1.1875	0.00475	836	577.5	0.114	0.339675	0.002625	1	6.32	3.705	67.2
12	1.1875	0.00475	836	522.5	0.114	0.307325	0.002375	0.939	6	3.66	67.5

Table 2.4: Extraction of the output parameters for the 12 different input combinations for the 50 nm HR device. The corresponding output parameters are R_{RESET}, R_{SET}, P_{RESET} and U_a.

2.5.2 For 10 nm HR Device:

Table represents the output parameters extracted for the 12 different input combinations for the 10 nm HR device.

Runs	C_{v_GST} (J/Kcm3)	$k_{\_GST}$ (W/K.cm)	T_m (K)	T_g (K)	$k_{\_heater}$ (W/K.cm)	C_{v_heater} (J/Kcm^3)	$\rho_{\_heater}$ (Ω.cm)	R_{RESET} (MΩ)	R_{SET} (KΩ)	P_{RESET} (μW)	U_a (nm)
1	1.3125	0.00525	836	577.5	0.126	0.339675	0.002375	33.5	164	227.92	16.5
2	1.3125	0.00525	836	522.5	0.114	0.339675	0.002375	33.4	150	227.04	16.5
3	1.3125	0.00525	924	522.5	0.114	0.307325	0.002625	0.863	74	226.38	10.1
4	1.3125	0.00475	924	577.5	0.114	0.339675	0.002625	0.864	77.8	226.38	10.1
5	1.3125	0.00475	924	577.5	0.126	0.307325	0.002375	0.53	65.3	221.76	10
6	1.3125	0.00475	836	522.5	0.126	0.307325	0.002625	33.4	150	233.86	16.5
7	1.1875	0.00525	924	522.5	0.126	0.339675	0.002625	0.72	68.1	227.7	10.1
8	1.1875	0.00525	924	577.5	0.114	0.307325	0.002375	0.782	74.1	220.66	10.1
9	1.1875	0.00525	836	577.5	0.126	0.307325	0.002625	33.7	165	233.86	16.6
10	1.1875	0.00475	924	522.5	0.126	0.339675	0.002375	0.537	63	221.76	10.1
11	1.1875	0.00475	836	577.5	0.114	0.339675	0.002625	33.8	165	232.98	16.6
12	1.1875	0.00475	836	522.5	0.114	0.307325	0.002375	33.5	150	227.04	16.7

Table 2.5: Extraction of the output parameters for the 12 different input combinations for the 10 nm HR device.

Chapter 3

RESULTS AND CONCLUSION

3.1 Results

The ranking provides useful information for tuning the particular input material parameters for the corresponding output parameter. For example, to achieve low power RESET, one should concentrate to reduce the P_{RESET} metric. Table 3.1 showing individual ranking of input parameter for each output parameter.

The present study reveals that resistivity of the heater ($\rho_{\_TiN}$) is the most sensitive parameter for a bigger device (50 nm heater radius), whereas melting temperature (T_m) is the most sensitive parameter for a smaller device (10 nm heater radius) for the P_{RESET}. Similarly, T_m is most sensitive for all other parameters $R_{RESET,}$ R_{SET}, and U_a for actual device (50 nm heater radius) as well as for scale down device (10 nm heater radius). (Refer Table 3.1).

Moreover, Table 3.2 lists the overall ranking of the input parameters in order to compare the performance of 50 nm and 10 nm heater radius devices. The overall ranking is based on the average of the absolute value of the coefficients associated with the individual input parameter obtained from all the output factors. The overall ranking suggests that GST melting temperature (T_m) and heater electrical resistivity ($\rho_{\_TiN}$) play a major role on the performance of 50 nm and 10 nm HR devices.

Also, the present study gives the guidelines for designing the new material with respect to the performance at the device level.

Input factors	Rank (original device – 50 nm HR)				Rank (scaled-down device – 10 nm HR)			
	R_{RESET}	R_{SET}	P_{RESET}	U_a	R_{RESET}	R_{SET}	P_{RESET}	U_a
C_{v_GST}	3 *(0.014)*	7 *(0.010)*	4 *(0.089)*	3 *(0.019)*	4 *(0.002)*	6 *(0.020)*	*6 (0.001)*	3 *(0.004)*
$k_{\_GST}$	4 *(0.009)*	6 *(0.012)*	5 *(0.044)*	6 *(0.003)*	5 *(0.001)*	3 *(0.039)*	4 *(0.005)*	4 *(0.003)*
T_m	1 *(0.999)*	1 *(0.981)*	2 *(0.354)*	1 *(0.999)*	1 *(1.000)*	1 *(0.990)*	1 *(0.729)*	1 *(1.000)*
T_g	2 *(0.036)*	2 *(0.177)*	6 *(0.022)*	5 *(0.007)*	2 *(0.004)*	2 *(0.116)*	4 *(0.005)*	5 *(0.001)*
$\rho_{\_TiN}$	7 *(0.001)*	3 *(0.047)*	1 *(0.886)*	2 *(0.220)*	3 *(0.003)*	4 *(0.036)*	2 *(0.674)*	2 *(0.006)*
$k_{\_TiN}$	5 *(0.007)*	4 *(0.030)*	3 *(0.244)*	7 *(0.002)*	2 *(0.004)*	5 *(0.024)*	3 *(0.121)*	2 *(0.006)*
C_{v_TiN}	6 *(0.002)*	5 *(0.014)*	6 *(0.022)*	4 *(0.010)*	5 *(0.001)*	6 *(0.020)*	5 *(0.003)*	5 *(0.001)*

Table 3.1: The individual ranking of the input variables for the corresponding output factors is shown for the original device (50 nm HR) and the scaled-down device (10 nm HR). The individual ranking is based on the absolute value of the coefficients associated with each input parameter for the corresponding output factors. The coefficient values (italicized and given in braces) are shown next to the rank.

Overall Ranking	Input Factors	
	Original device (50 nm HR)	Scaled-down device (10 nm HR)
1	T_m*(0.833)*	T_m*(0.929)*
2	$\rho_{\_TiN}$(0.288)	$\rho_{\_TiN}$(0.180)
3	$k_{\_TiN}$(0.071)	$k_{\_TiN}$(0.039)
4	T_g*(0.060)*	T_g*(0.032)*
5	C_{v_GST} (0.033)	$k_{\_GST}$ (0.012)
6	$k_{\_GST}$(0.017)	C_{v_GST}(0.007)
7	C_{v_TiN}(0.012)	C_{v_TiN}(0.006)

Table 3.2: The overall ranking of the input variables between 50 nm and 10 nm HR devices by considering all the output factors simultaneously. The overall ranking is based on the average of the absolute value of the coefficients associated with the individual input parameter obtained from all the output factors. The coefficient values (italicized and given in braces) are shown next to the input parameter symbol. The ranking suggests that GST melting temperature and heater electrical resistivity play a major role on the performance of 50 nm and 10 nm HR devices.

3.2 Conclusion

The impact of material parameters on mushroom-type PCM device is investigated and the critical input parameters are identified for the important performance metrics. The result shows that the different material parameters have different sensitivity for the programming of the device. The study reveal that only two material parameters, melting temperature of the GST (T_m) and resistivity of heater material TiN ($\rho_{\_TiN}$) are most sensitive parameter so they will play a dominant role in the programming of 50 nm and 10 nm HR devices. All other parameters are least sensitive so they will play least significant role in the programming of both 50nm and 10nm HR devices. Further, the thermal conductivity of GST ($k_{\_GST}$) is playing a least significant role in both device but it ranked as 6th position in 50 nm HR device, whereas it is ranked as 5th position in 10 nm HR device. Therefore, we can conclude that thermal conductivity of GST ($k_{\_GST}$) is some more sensitive in the scaled-down device as compared to actual 50 nm HR device. The result suggest that the most and least sensitive input parameters can be effectively used for the better optimization of SET/RESET pulse parameters to achieve a reliable programming for the future technology.

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