Analysis, Design and Control of Fourth Order DC-DC Boost Converter

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Analysis, Design and Control of Fourth Order DC-DC Boost Converter**, submitted by **Rohan V Madnani**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Place: Chennai
Date:

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Rohan V Madnani

To my Gurudeva - Sri Sri Paramahansa Yogananda

Abstract

This report discusses the analysis, design and control of Boost Converter with Output CL Filter (BCOCLF). The converter is a fourth order system containing two inductors and two capacitors. The following are its main attributes.

- The well known conventional boost converter have the problem of discontinuous output current, which can be undesirable in many applications.
- The proposed design of the fourth order boost converter solves this problem with the use of output CL filter.
- Although there are other fourth order boost converters which solve the aforementioned problem, this converter is unique in the aspect that it keeps the converter DC gain same as that of the conventional boost converter.

Keywords: *Boost Converter, DC-DC converter, fourth order boost converter, BCOCLF, no ripple output current*

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

It is well known that transformers are used to step-up or step-down ac voltages keeping the power unchanged. They are easy to implement, rugged and highly efficient electrical devices. But unfortunately, they cannot be used for DC systems as the transformer would saturate for a DC current would produce a constant flux in its core. Hence there was a need for the development of devices that could step-up or step-down DC voltages, much similar to the way transformers do so. With the advent of Power Electronics in the early 1950s, this became possible. The following are the three basic power electronic DC-DC converters and their function(s) [1, 2].

- Buck converter: step-down DC voltage
- Boost converter: step-up DC voltage
- Buck-Boost converter: step-down or step-up DC voltage

The three are called basic converters, because all other DC-DC converters have been derived from these three topologies [2]. Apart from these, many more DC-

DC converters namely the Ck, Sepic, Zeta and Flyback converter have been reported in literature [3, 4].

The basic converter topologies have one inductor and one capacitor in their circuitry. Thus because of these two storage elements, they form a second order system. Because of switching, currents on either the input side, or the output side or both (in case of buck-boost converters) are discontinuous. This discontinuity in current is undesirable. This is because since the average current demanded by the load is constant, it is met by peaky currents owing to the discontinuity. As per literature, this kind of peaky currents are harmful to DC voltage source, most likely to be a battery [5 - 11]. Hence higher order DC-DC converters are designed to counter this problem.

1.2 Objectives and Contributions

DC-DC converters with CL filters are reported in literature [12 - 15]. CL filters either on the output side, or input side or both, help to reduce switching frequency ripple and lower the EMI [16]. Further there is a reduction in ripple current (on the side wherever the filter is placed) as reported in [13]. Various fourth order converter topologies have been reported in the literature. Some fourth order buck converter topologies are namely - FOBUC, BCIF and BCICLF [13]; while for boost converter, they are - HGFBC and FODBC [17]. Due to the presence of these filter components, the DC gain of these fourth order converters tend to change from that of their corresponding conventional second order topology. However, a fourth order buck converter namely BCICLF was proposed in [13] which retained the converter gain as equal to the gain of conventional buck converter, and also solved the aforementioned problem of ripple current on the input side. Taking inspiration from this, a fourth order boost converter is proposed in this report

such that the ripple on the output side is brought down as compared to second order boost converter, and also the converter gain is retained same as that of the conventional boost converter. The said converter along with its controller is designed and simulated in MATLAB Simulink and performance results are obtained.

1.3 Overview of the Report

In chapter 1, an introduction to the basic idea of the project work is given describing the motivation that had driven it and the objectives it has met. In chapter 2, a review of basic three DC-DC converter topologies is carried out, their steady state analysis and design of their parameters are attended in detail. In chapter 3, an overview of design and control of conventional boost converter is given describing in detail its challenges and shortcomings - the major one being the discontinuous output current of boost converter and its detrimental effects on converter's life. To encounter this, the need for fourth order DC-DC converters is discussed through an example of a fourth order buck converter topology that retains DC gain of conventional buck converter and has no right half plane zeros. Inspired from this, a new fourth order boost converter topology retaining gain as that of conventional boost converter is then proposed; such that the output current becomes continuous and converter life is enhanced. Its detailed steady state analysis and design parameters are given. The derivation of the proposed converter's transfer function and design of its controller are also discussed here. Finally, the simulation results in the form of wave-forms and tabulated data are given. Derived conclusions from this study and future scope of development are presented in chapter 4.

Chapter 2

Review of basic DC-DC Converter Topologies

Introduction

This chapter deals with the steady state analysis and design of inductance and capacitance for the three basic DC-DC converters namely the Buck, Boost and the Buck-Boost converter. These three converters are the basic building blocks for all other DC-DC converters, hence it is important to understand their operation, steady state analysis and design [2].

Also, it is important to note that all analysis in this report is done considering that the power remains same on both sides of the converter, i.e. ideal operation (no losses in the converter) and also only for continuous current mode (CCM) of operation.

2.1 Basic Concepts for Steady State Analysis

To analyze the steady state functioning and design of basic DC-DC converter topologies, two fundamental theories are vitally instrumental.

- Inductor volt-second balance
- Capacitor charge balance

2.1.1 Inductor Volt-Second Balance

The steady state operation of DC-DC converters have two modes of operation:

- T_{on} - indicating time during which the semiconductor switch is conducting.
- T_{off} - indicating time during which the semiconductor switch is not conducting.

Depending on the circuit topology, the inductor charges or discharges in either of the time intervals. The total time T_s which denotes the switching time period of one cycle, is the sum of the times T_{on} and T_{off}.

Now in steady state, since the average inductor current has to remain same over one cycle, the net $\left\langle \frac{di_L(t)}{dt} \right\rangle = 0$. Also we know that $v_L(t) = L\frac{di_L(t)}{dt}$, therefore the following can be written [1]:

$$\frac{1}{T_s}\int_0^{T_s} v_L(t)dt = \langle v_L \rangle = 0 \tag{2.1}$$

2.1.2 Capacitor Charge Balance

Capacitors in the converters have a constant average voltage in steady state operation, although there is charging and discharging of capacitors taking place during T_{on} and T_{off} time intervals. Thus the net $\left\langle \frac{dv_C(t)}{dt} \right\rangle = 0$ as averaged over

one cycle. Now since current through capacitor is given as $i_C(t) = C\frac{dv_C(t)}{dt}$, the following equation can be written [1]:

$$\frac{1}{T_s}\int_0^{T_s} i_C(t)dt = \langle i_C \rangle = 0 \tag{2.2}$$

2.2 Buck Converter

Buck converters are used for stepping down DC voltages. The fundamental circuit diagram of buck converter is as given in Figure 2.1 [2].

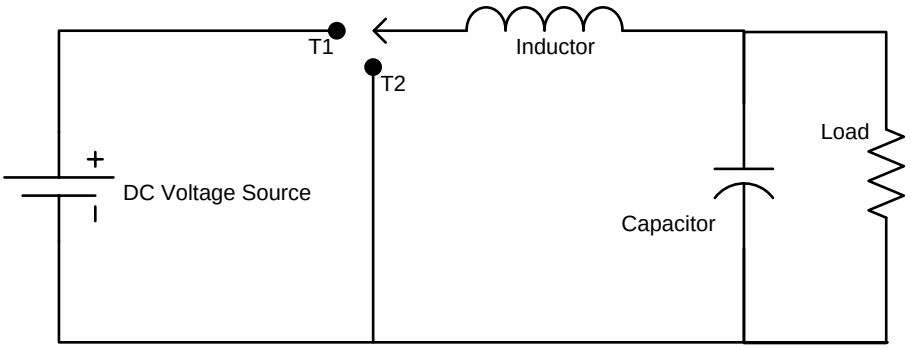

Figure 2.1: Fundamental circuit diagram of buck converter

During T_{ON} terminal T1 is connected to the inductor, while during T_{OFF} terminal T2 is connected to inductor. Thus the inductor charges during T_{ON} and discharges during T_{OFF}. In actual circuit, this SPDT switch is implemented by the use of a controlled switch (in this case MOSFET) and an uncontrolled switch (in this case diode) as shown in Figure 2.2.

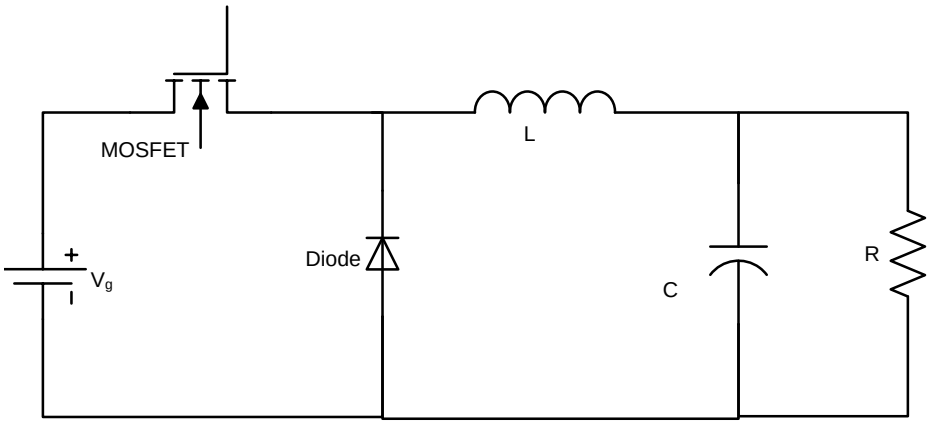

Figure 2.2: Circuit diagram of buck converter

The steady state analysis of buck converter goes as follows [1, 2]:

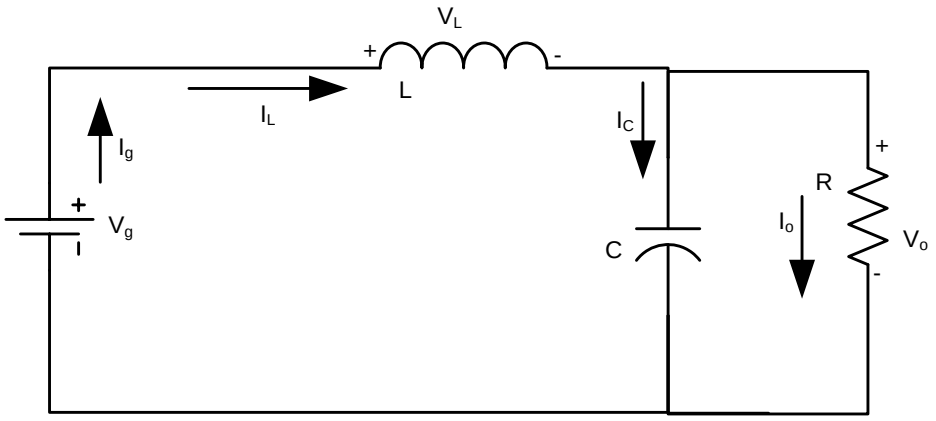

Figure 2.3: Buck converter equivalent circuit during T_{ON} mode of operation

Equations during T_{ON} mode:

$$\begin{aligned} v_L &= V_g - V_o \\ \implies \frac{di_L(t)}{dt} &= \frac{V_g - V_o}{L} \end{aligned} \tag{2.3}$$

$$i_C = i_L - \frac{V_o}{R} \tag{2.4}$$

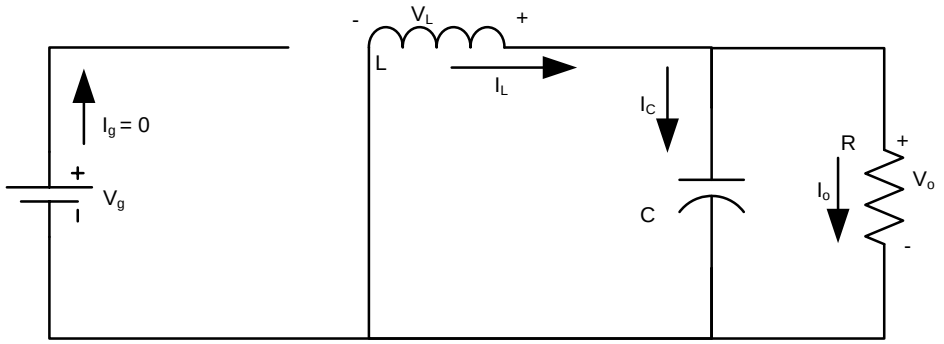

Figure 2.4: Buck converter equivalent circuit during T_{OFF} mode of operation

Equations during T_{OFF} mode:

$$\begin{aligned} v_L &= -V_o \\ \implies \frac{di_L(t)}{dt} &= \frac{-V_o}{L} \end{aligned} \tag{2.5}$$

$$i_C = i_L - \frac{V_o}{R} \tag{2.6}$$

also, $\langle i_L \rangle = \frac{V_o}{R}$ averaged over one switching cycle.

Converter Gain:

Now applying inductor volt-second balance using (2.3) and (2.5), we get,

$$\begin{aligned} (V_g - V_o)(DT_s) + (-V_o)(1-D)T_s &= 0 \\ \implies V_o &= DV_g \end{aligned} \tag{2.7}$$

where D is called the duty cycle of the switch and is defined as,

$$D = \frac{T_{ON}}{T_s}$$

Considering ideal operation, input power is equal to output power, $P_{in} = P_{out}$. Therefore, $I_g = DI_o$.

Capacitor Design:

Using (2.3) and (2.5) and the average value of inductor current, its waveform is constructed as shown in Figure 2.5. From (2.4) and (2.6), and Figure 2.5, capacitor current waveform is constructed as shown in Figure 2.6. Assuming that all the ripple current flows through the capacitor, the required capacitor value can be calculated as,

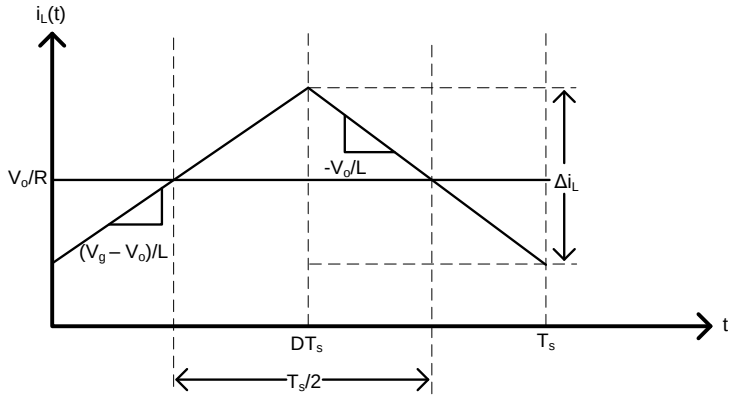

Figure 2.5: Inductor current for buck converter

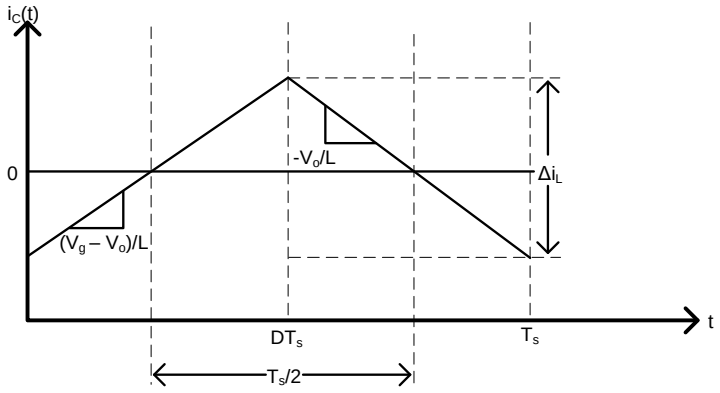

Figure 2.6: Capacitor current for buck converter

$$\begin{aligned} \Delta Q &= \frac{\Delta I_L T_s}{8} \\ \implies C\Delta V_o &= \frac{\Delta I_L T_s}{8} \\ \implies C &= \frac{\Delta i_L}{8 f \Delta V_o} \end{aligned} \tag{2.8}$$

where ΔQ is the change in charge of the capacitor and f is switching frequency given by $f = \frac{1}{T_s}$.

Inductor Design:

Referring to Figure 2.5, we can write the following:

$$\begin{aligned} \Delta I_L &= \frac{(V_g - V_o)(DT_s)}{L} \\ \implies L &= \frac{(V_o)(1-D)}{\Delta I_L f} \end{aligned} \tag{2.9}$$

2.3 Boost Converter

Boost converter steps-up DC voltages. Hence fundamentally it has the reverse circuit of buck converter as shown in Figure 2.7 [2].

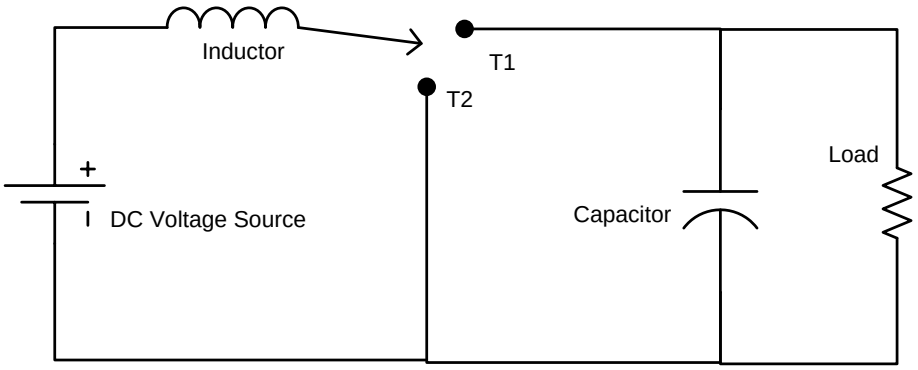

Figure 2.7: Fundamental circuit diagram of boost converter

During T_{ON}, the inductor pole is connected to T2 and the source charges the inductor. Later during T_{OFF}, the indcutor is discharged to the load by being connected to T1.

Thus the actual circuit diagram for implementing this is given as in Figure 2.8.

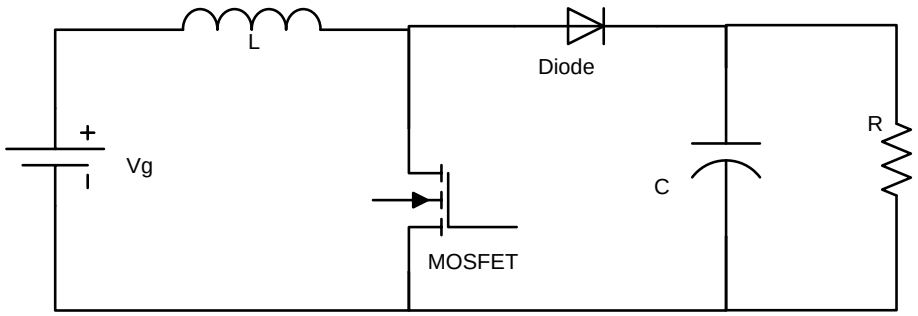

Figure 2.8: Circuit diagram of boost converter

Converter steady state analysis is as follows [1, 2]:

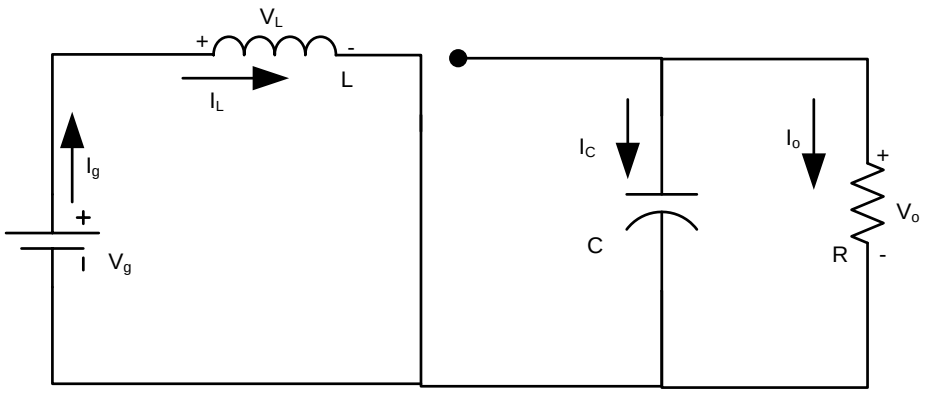

Figure 2.9: Boost converter equivalent circuit during T_{ON} mode of operation

Equations during T_{ON} mode:

$$\begin{aligned} v_L &= V_g \\ \implies \frac{di_L(t)}{dt} &= \frac{V_g}{L} \end{aligned} \tag{2.10}$$

$$i_C = \frac{-V_o}{R} \tag{2.11}$$

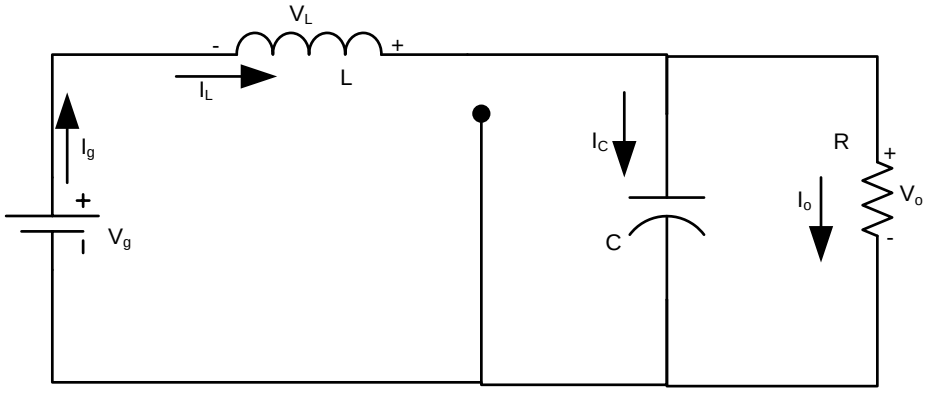

Figure 2.10: Boost converter equivalent circuit during T_{OFF} mode of operation

Equations during T_{ON} mode:

$$\begin{aligned} v_L &= V_g - V_o \\ \implies \frac{di_L(t)}{dt} &= \frac{V_g - V_o}{L} \end{aligned} \tag{2.12}$$

$$i_C = \frac{I_g - V_o}{R} \tag{2.13}$$

Converter Gain:

Applying inductor volt-second balance to (2.10) and (2.12).

$$\begin{aligned} \frac{V_g D T_s}{L} + \frac{(V_g - Vo)(1-D)T_s}{L} &= 0 \\ \implies \frac{V_o}{V_g} &= \frac{1}{1-D} \end{aligned} \tag{2.14}$$

Applying capacitor charge balance to (2.11) and (2.13).

$$\begin{aligned} \frac{-V_o D}{R} + \frac{(I_g - V_o)(1-D)}{R} &= 0 \\ \implies I_g &= \frac{V_o}{R(1-D)} \\ \implies \frac{I_g}{I_o} &= \frac{1}{1-D} \end{aligned} \tag{2.15}$$

Capacitor Design:

Using current equations of the capacitor; $i_C(t) = C\frac{dv_C(t)}{dt}$ and $\langle v_C(t) \rangle = V_o$ averaged over one cycle, we get the following waveform of the capacitor voltage $v_C(t)$ (Figure 2.11).

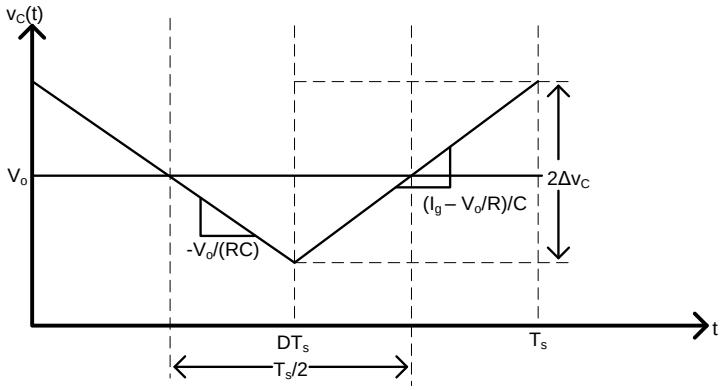

Figure 2.11: Capacitor voltage for boost converter

$$\begin{aligned} 2\Delta V_C &= \frac{V_o D T_s}{RC} \\ \implies C &= \frac{V_o D}{2Rf\Delta V_C} \end{aligned} \tag{2.16}$$

Inductor Design:

Similarly using inductor voltage (2.10) and (2.12), Figure 2.12 is obtained.

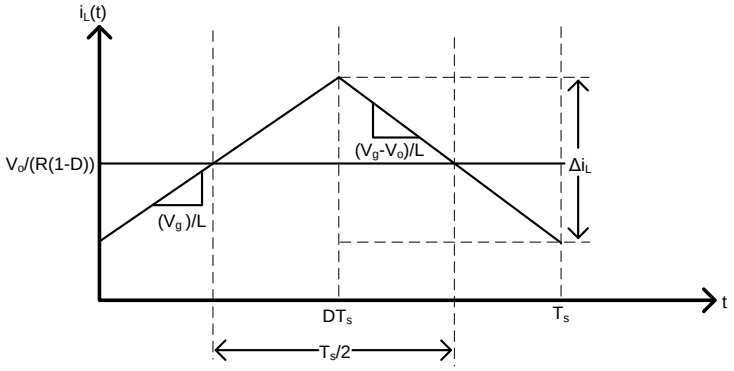

Figure 2.12: Inductor current for boost converter

$$\Delta I_L = \frac{V_g D T_s}{L}$$
$$\implies L = \frac{V_o D(1-D)}{f \Delta I_L} \tag{2.17}$$

2.4 Buck-Boost Converter

The buck-boost type of converter can be used for stepping up as well as stepping down of the DC voltages. This is achieved by varying the duty ratio D.
Fundamental circuit diagram of buck-boost converter is given in Figure 2.13 [2].

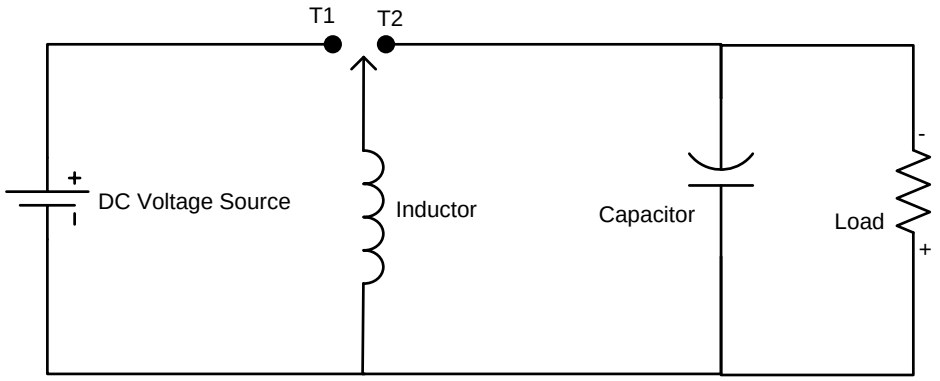

Figure 2.13: Fundamental circuit diagram of buck-boost converter

When inductor pole is connected to T1 during T_{ON}, the inductor gets charged through the source, whereas during T_{OFF} it is connected to T2 and discharges to the load.
It is important to note that here the discharges from the lower side and hence a reverse polarity is obtained at the output as shown in the figure.
In practice, the SPDT is realised using MOSFET and a diode (Figure 2.14).

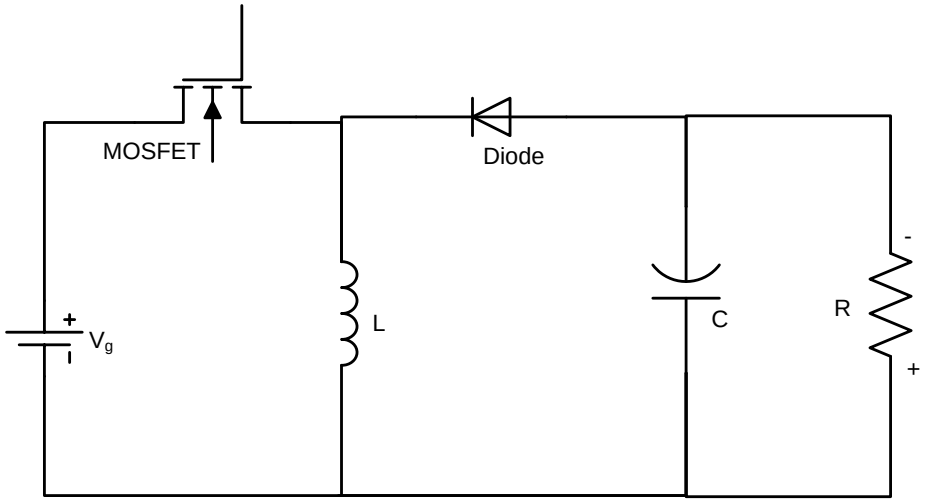

Figure 2.14: Circuit diagram of buck-boost converter

The converter steady state analysis is as follows [1, 2]:

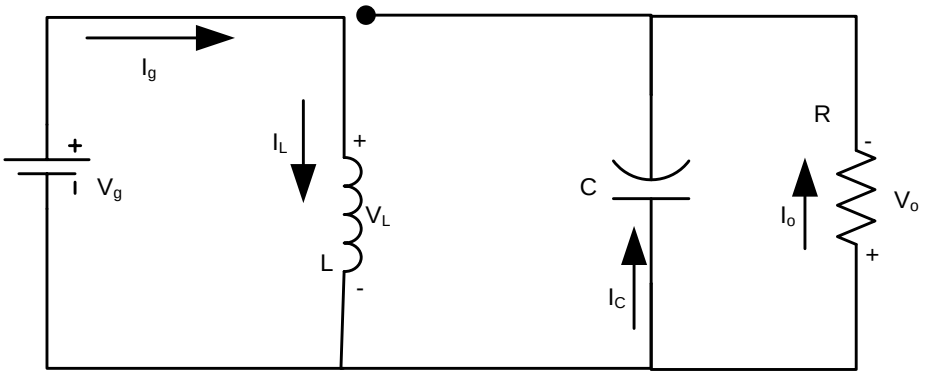

Figure 2.15: Buck-boost converter equivalent circuit diagram during T_{ON} mode of operation

Equations during T_{ON} mode:

$$\begin{aligned} v_L &= V_g \\ \implies \frac{di_L(t)}{dt} &= \frac{V_g}{L} \end{aligned} \tag{2.18}$$

$$i_C = \frac{-V_o}{R} \tag{2.19}$$

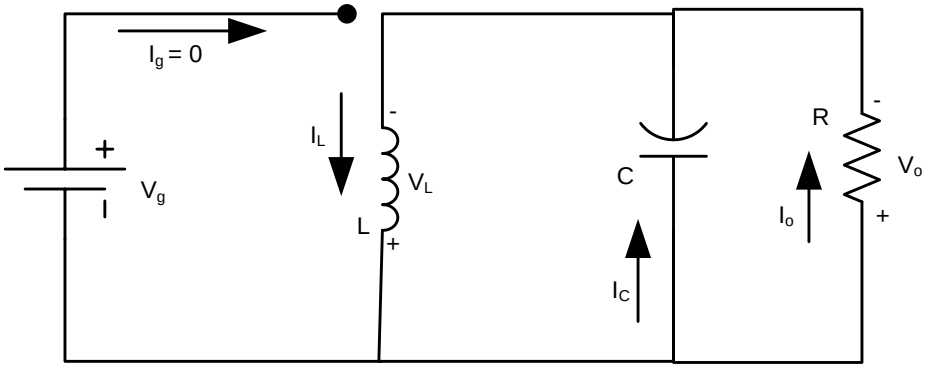

Figure 2.16: Buck-boost converter equivalent circuit diagram during T_{OFF} mode of operation

Equations during T_{OFF} mode:

$$\begin{aligned} v_L &= V_o \\ \implies \frac{di_L(t)}{dt} &= \frac{V_o}{L} \end{aligned} \tag{2.20}$$

$$i_C = I_L - \frac{-V_o}{R} \tag{2.21}$$

Converter Gain:

Applying inductor volt-second balance to (2.18) and (2.20).

$$\begin{aligned} V_g D + V_o(1-D) &= 0 \\ \implies \frac{V_o}{V_g} &= \frac{-D}{(1-D)} \end{aligned} \tag{2.22}$$

Therefore, we see that the output voltage has opposite polarity as compared to the input voltage.

By capacitor charge balance applied to (2.19) and (2.21), we have

$$I_L = \frac{V_o}{R(1-D)}$$

and by power balance, we know that

$$\frac{I_g}{I_o} = \frac{D}{1-D}$$

Hence we can write $I_g = DI_L$

Capacitor Design:

Using current equations of the capacitor; $i_C(t) = C\frac{dv_C(t)}{dt}$ and $\langle v_C(t)\rangle = V_o$ averaged over one cycle, we get the following waveform of the capacitor voltage $v_C(t)$ (Figure 2.17).

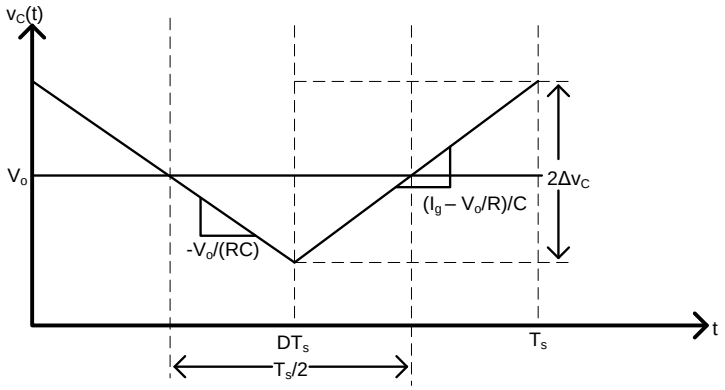

Figure 2.17: Capacitor voltage for buck-boost converter

$$\begin{aligned} 2\Delta V_C &= \frac{V_o D T_s}{RC} \\ \implies C &= \frac{V_o D}{2Rf\Delta V_C} \end{aligned} \tag{2.23}$$

Inductor Design:

Using inductor voltage (2.18) and (2.20), the inductor current waveform as shown in Figure 2.18 is obtained.

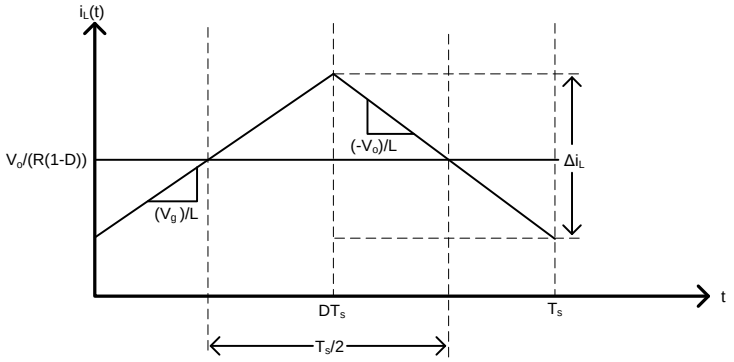

Figure 2.18: Inductor current for buck-boost converter

$$\begin{aligned} \Delta I_L &= \frac{V_g D T_s}{L} \\ \implies L &= \frac{V_o(1-D)}{f \Delta I_L} \end{aligned} \tag{2.24}$$

Chapter 3

Boost Converter with Output CL Filter

Introduction

In this chapter, we shall discuss about the design and simulation of a DC-DC boost converter for given voltage transformation ratio, power rating and switching frequency. We shall then see the shortcomings in its performance, by simulating it in MATLAB Simulink. To overcome those shortcomings, we shall propose a new topology for boost converter, having four storage elements - two inductors and two capacitors. We shall then design this new converter for the same specifications as the previous one and compare the performances of the two converters.

3.1 Design and Steady State Performance of DC-DC Boost Converter

In this section, 12/48 V voltage ratio, 100 W power rating, 100 KHz switching frequency boost converter shall be designed along with its controller, and shall be

simulated in MATLAB Simulink, chiefly to analyze its steady state performance.

3.1.1 Converter Design

Power rating $P = 100\,\mathrm{W}$

Input voltage $V_g = 12\,\mathrm{V}$

Output voltage $V_o = 48\,\mathrm{V}$

Therefore, D = 0.75

Switching frequency $f = 100\,\mathrm{KHz}$

Rated load $R = \frac{48^2}{100} = 23.04\,\Omega$

Rated output current $I_o = \frac{48}{23.04} = 2.0834\,\mathrm{A}$

Using (2.15), rated input current $I_g = 8.3334\,\mathrm{A}$

According to [18], the current ripple can be between 20% to 40% of the rated value. Considering close to ideal operation, we choose $\Delta I_L = (10\%)I_g = 0.8334\,\mathrm{A}$

From (2.16) and (2.17), we get $C = 8.138\,\mu\mathrm{C}$ and $L = 108\,\mu\mathrm{H}$.

3.1.2 Converter transfer function and controller tuning

Since we want to control the output voltage of the boost converter by varying the duty ratio D, we use the 'Gvd(s)' transfer function of boost converter as given in [1].

$$G_{vd}(s) = G_{d0}\frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{3.1}$$

where, $G_{d0} = \frac{V_o}{1-D}$, $\omega_0 = \frac{1-D}{\sqrt{LC}}$, $Q = (1-D)R\sqrt{\frac{C}{L}}$ and $\omega_z = \frac{(1-D)^2R}{L}$.

Substituting values in (3.1), converter transfer function and its bode plot are obtained as shown in Figure 3.1.

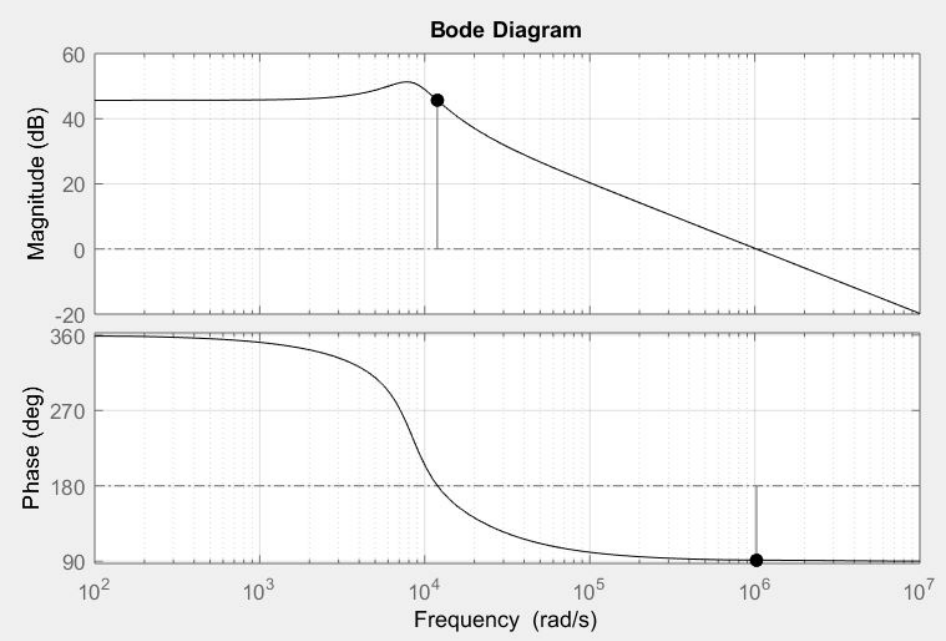

Figure 3.1: Bode plot of $G_{vd}(s)$ transfer function

Clearly, the system is unstable with a phase margin of $-269°$ and gain margin -45.7dB. Hence a controller is must for its stable operation and for good steady state performance.

Along with the controller with transfer function G_c, the overall block diagram of the system looks like what is shown in Figure 3.2.

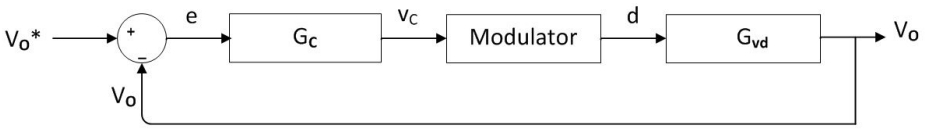

Figure 3.2: Control block diagram for voltage control of boost converter

We shall tune a PI controller for the given transfer function, such that the new gain crossover frequency (ω_{gc}) is obtained around 7000 rad/s with a phase margin of around $90°$ and a positive gain margin.

General transfer function for PI controller is given as.

$$G_c = \frac{k_p(sT+1)}{sT}$$

Therefore, using open loop transfer function of the system, and applying the following conditions,

$$|G_c G_{vd}|_{7000\,\mathrm{rad/s}} = 1$$

and

$$\frac{1}{T} = \frac{\omega_{gc}}{10}$$

we get k_p as 2.8184×10^{-3} and T as $\frac{1}{700}$. These values were substituted and bode plot was found to be stable. Due to resonance around $\omega = 7000\,\mathrm{rad/s}$, and the resulting curvature in the magnitude plot, the new bode is found to intersect the $0\,\mathrm{dB}$ line at a a lesser than expected value. Hence ω_{gc} is obtained at $452\,\mathrm{rad/s}$ and gain margin is $4.75\,\mathrm{dB}$. The resulting Bode plot is shown in 3.3

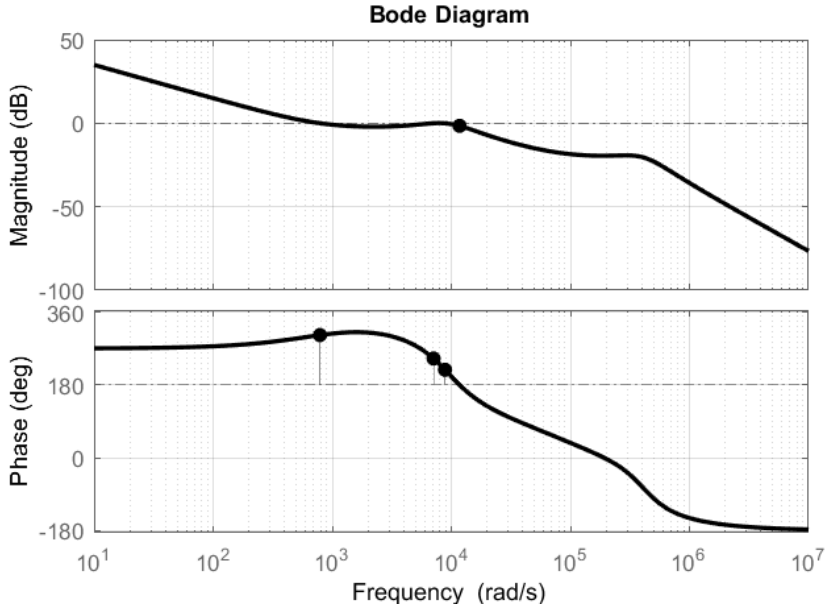

Figure 3.3: Bode plot of $G_{vd}(s) * G_c(s)$ transfer function

It can be seen that two gain cross-over frequencies are obtained.

3.1.3 Results

The designed values of inductor, capacitor at rated load and given switching frequency along with the controller are now simulated in MATLAB Simulink and results are observed for output voltage, converter output current and load current as are showed in Figures 3.5 - 3.7 respectively. For reference, these quantities are marked in Figure 3.4.

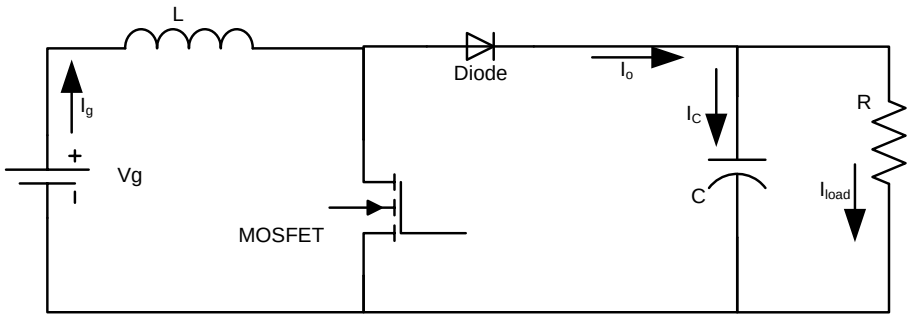

Figure 3.4: Boost converter circuit with marked currents and voltages to be studied

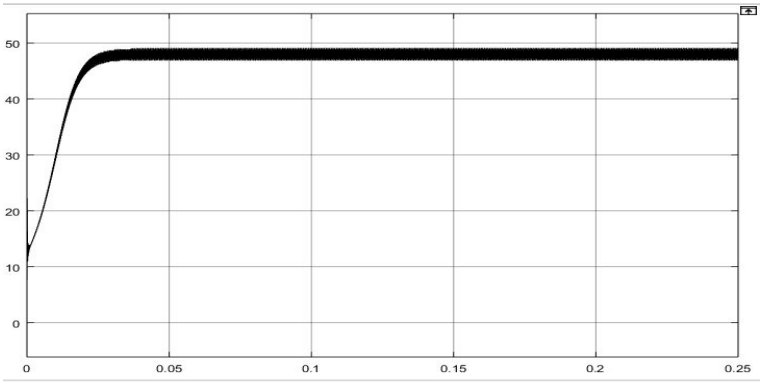

Figure 3.5: V_o (V) v/s time (s)

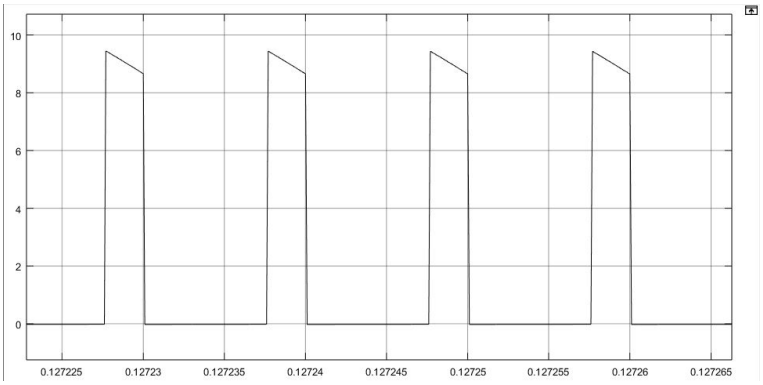

Figure 3.6: I_o (A) v/s time (s)

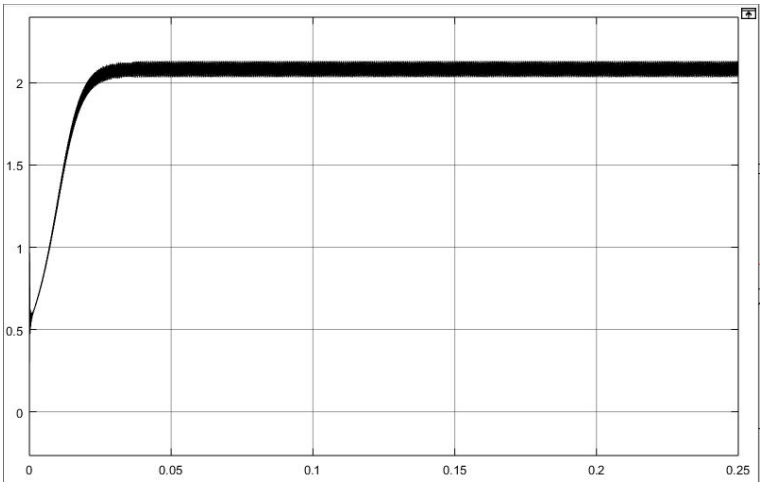

Figure 3.7: I_{load} (A) v/s time (s)

3.1.4 Shortcomings in Steady State Performance

From simulation results, it is evident that I_o is peaky in nature. This is because during T_{ON} mode of operation, no current flows from the input to the output of boost converter, and the average value of current demanded by the load needs to be met anyways. I_{load} on the other hand is having comparatively less ripple, because most of it has been absorbed by the output capacitor, but it is still close to 5% of the demanded average value. Because of high current ripple in I_o,

capacitor voltage v_C ripple is also found to be about 5% of the average output voltage.

It is reported in [19] that high ripple in capacitor current causes internal heating owing to ESR and hence degradation of capacitor life. This in turn affects the life of the converter as a whole. Hence it comes important to address this problem of high ripple in output current. For the same, we shall propose a new topology of fourth order boost converter in section 3.3.

3.2 Introduction to Fourth Order DC-DC Converters

The problem of discontinuous output current is not unique to boost converter. A similar problem of discontinuous input current exists for buck converters also. To encounter this problem, many fourth order DC-DC converter topologies are proposed in literature. One of them is Buck Converter with Input CL Filter (BCICLF) as reported in [13]. The circuit diagram for BCICLF is given in Figure 3.8.

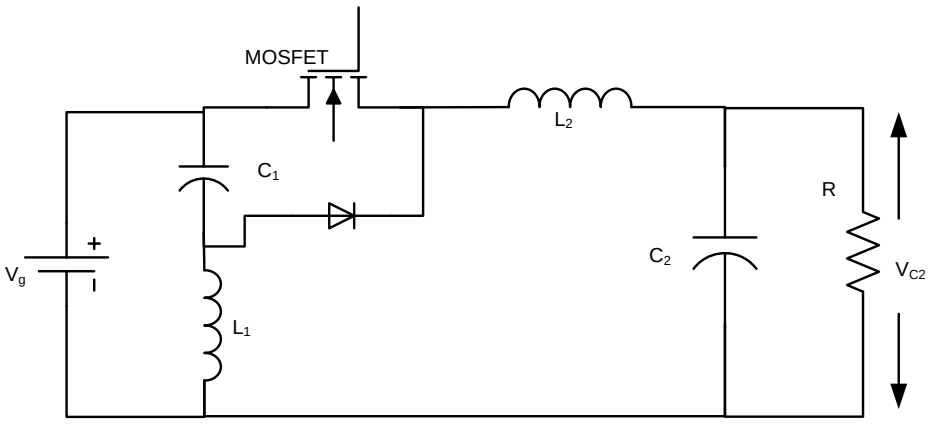

Figure 3.8: Circuit diagram for BCICLF

Although other topologies of fourth order buck converters also solve the problem of discontinuous input current, but the presence of CL filters also tend to modify the converter gain as compared to their conventional counterparts. This topology is unique in this aspect that its converter gain is same as that of the conventional buck converter. That is, the converter gain of BCICLF is given as,

$$V_o = DV_g$$

If this converter is utilized for interfacing a voltage source such as a battery, with a DC system, then the input current ripple is reported to have reduced to such an extent that battery life has enhanced and EMI has reduced. Although other fourth order buck converters have too been successful in achieving these feats, but unlike them, BCICLF it does not have any non-minimum phase zeros in the output voltage to duty ratio transfer function. As a result, BCICLF has a superior dynamic performance and its control is much simpler as compared to other fourth order buck converters.

3.3 BCOCLF - Design and Performance

Thinking on the same lines for boost converter output current ripple problem, we shall now propose a new topology to address it. The converter is called Boost Converter with Output CL Filter (BCOCLF). Circuit diagram for BCOCLF is given in Figure 3.9.

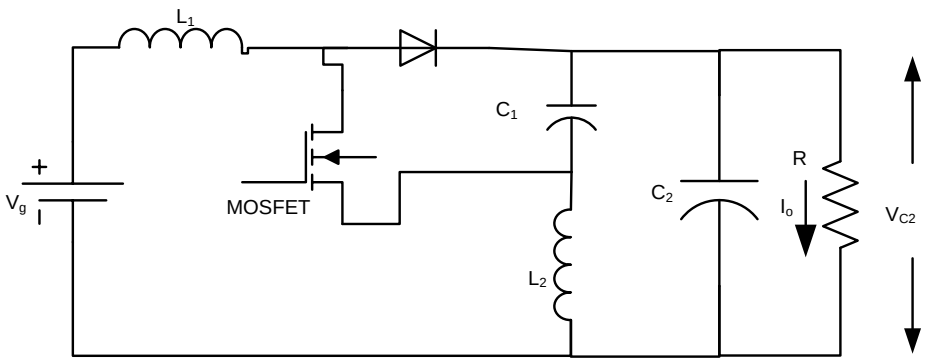

Figure 3.9: Circuit diagram of BCOCLF

As shown in the figure, the CL filter is added on the output side. In steady state, the output voltage is greater than the input voltage. When the MOSFET is conducting, the voltage at the n terminal of the diode is V_o and that on its p terminal is V_g, hence the diode is reverse biased and does not conduct. During this on time, the inductors L_1 and L_2 are charging and as soon as the MOSFET goes off, the polarity of inductor voltages get reversed as explained by Lenz's law, and hence the diode is forward biased by the voltage source and inductor L_1. Thus the output voltage is now enhanced. Also, during T_{OFF} time period, the capacitor C_1 gets charged as shall be discussed, and during T_{ON} it discharges to the load. Hence, essentially, there is always a load current flowing from the converter, and this is the reason how output current ripple is reduced. Interestingly, upon doing the circuit analysis, capacitor C_1 voltage averaged over one cycle, comes out to be equal to source voltage. Hence during T_{ON} mode, the output voltage is approximately zero, and during T_{OFF} mode, it is the enhanced value. This is pretty much the case in conventional boost converter also. Therefore, the converter gain is same as that of conventional boost converter.

3.3.1 Steady State Analysis and Design

For steady state analysis of the converter, we shall consider the converter equivalent circuit during T_{ON} and T_{OFF} separately.

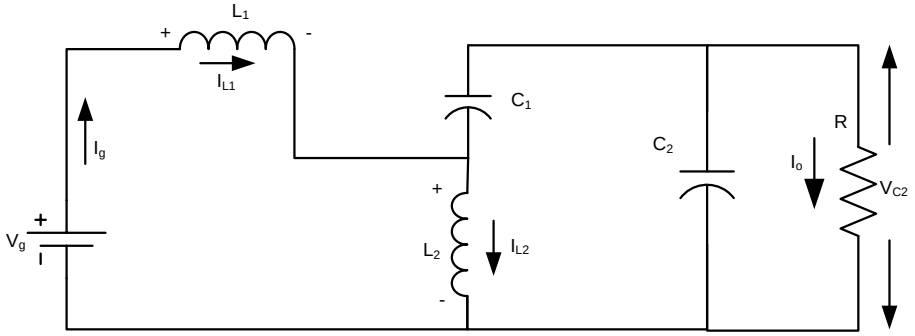

Figure 3.10: Equivalent circuit of BCOCLF during T_{ON} mode of operation

Equations during T_{ON} mode:

$$V_g - v_{L1} - v_{L2} = 0 \tag{3.2}$$

$$\begin{aligned} v_{L1} &= V_g + V_{C1} - V_{C2} \\ \implies \frac{di_{L1}(t)}{dt} &= \frac{V_g + V_{C1} - V_{C2}}{L_2} \end{aligned} \tag{3.3}$$

$$v_{L2} = V_{C2} - V_{C1} \tag{3.4}$$

$$\begin{aligned} i_{C1} &= -I_o \\ \implies \frac{dv_{C1}}{dt} &= \frac{-I_o}{C_1} \end{aligned} \tag{3.5}$$

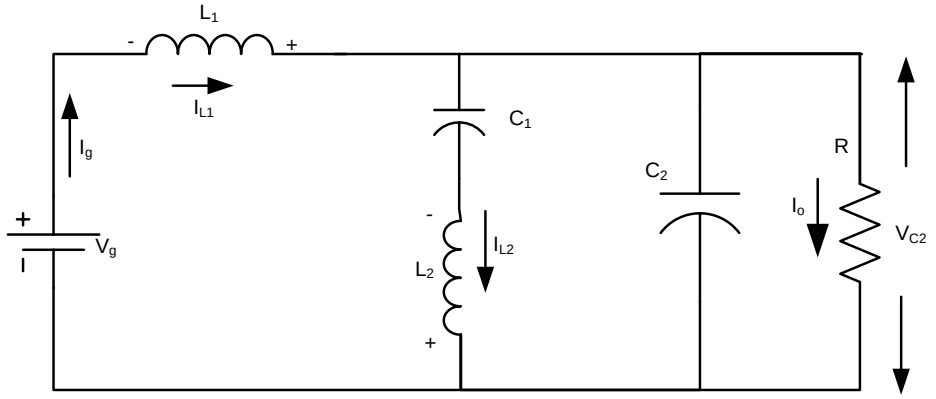

Figure 3.11: Equivalent circuit of BCOCLF during T_{OFF} mode of operation

Equations during T_{OFF} mode:

$$V_g - v_{L1} - v_{L2} - V_{C1} = 0 \tag{3.6}$$

$$\begin{aligned} v_{L1} &= V_g - V_{C2} \\ \implies \frac{di_{L1}(t)}{dt} &= \frac{V_g - V_{C2}}{L_2} \end{aligned} \tag{3.7}$$

$$v_{L2} = V_{C2} - V_{C1} \tag{3.8}$$

$$\begin{aligned} i_{C1} &= I_g - I_o \\ \implies \frac{dv_{C1}}{dt} &= \frac{I_g - I_o}{C_1} \end{aligned} \tag{3.9}$$

3.3.1.1 Converter Gain

Applying inductor volt-second balance for L_1 using (3.3) and (3.7).

$$\begin{aligned}(V_g + V_{C1} - V_{C2})D + (V_g - V_{C2})(1-D) = 0 \\ \implies V_{C1} = \frac{V_{C2} - V_g}{D}\end{aligned} \tag{3.10}$$

Applying inductor volt-second balance for L_2 using (3.4) and (3.8).

$$\begin{aligned}(V_{C2} - V_{C1})D + (V_{C2} - V_{C1})(1-D) = 0 \\ \implies V_{C1} = V_{C2} = V_o\end{aligned} \tag{3.11}$$

(3.10) and (3.11) imply

$$\frac{V_o}{V_g} = \frac{1}{1-D} \tag{3.12}$$

Applying capacitor charge balance for capacitor C_1 using (3.5) and (3.9).

$$\begin{aligned}(-I_o)D + (I_g - I_o)(1-D) = 0 \\ \implies \frac{I_g}{I_o} = \frac{1}{1-D}\end{aligned} \tag{3.13}$$

3.3.1.2 Inductor L_1 Design

Using (3.3) and (3.7), inductor current waveform is drawn as shown in Figure 3.12

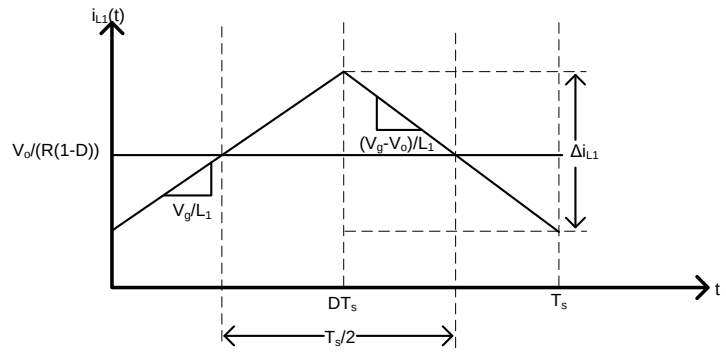

Figure 3.12: Inductor L_1 current waveform for BCOCLF

$$\begin{aligned} \Delta I_{L1} &= \frac{V_g D T_s}{L1} \\ \implies L_1 &= \frac{V_o D(1-D)}{\Delta I_{L1} f} \end{aligned} \tag{3.14}$$

3.3.1.3 Capacitor C_2 Design

Knowing $\langle v_{L2} \rangle = 0$ averaged over one cycle, we can fairly assume that all the ripple current Δi_{L1} is flowing through capacitor C_2. Therefore,

$$\begin{aligned} \Delta Q_2 &= \frac{\Delta I_{L1} T_s}{8} \\ \implies C_2 &= \frac{V_o D(1-D)}{8 f^2 L_1 \Delta V_o} \end{aligned} \tag{3.15}$$

3.3.1.4 Capacitor C_1 Design

Using (3.5) and (3.9), capacitor voltage waveform is obtained as shown in Figure 3.13.

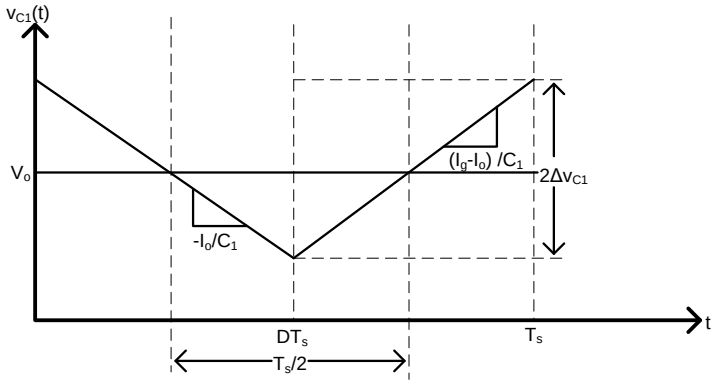

Figure 3.13: Capacitor C_1 voltage waveform for BCOCLF

$$\begin{aligned} 2\Delta V_{C1} &= \frac{I_o D T_s}{C_1} \\ \implies C_1 &= \frac{I_o D}{2 f \Delta V_{C1}} \end{aligned} \tag{3.16}$$

3.3.2 Converter Transfer Function

State space method is used to find out the converter transfer function. Converter T_{ON} and T_{OFF} mode equations are used to obtain small signal model of the converter. Since the converter has four storage elements, four state variables - inductor currents of L_1 and L_2 and capacitor voltages of C_1 and C_2 are studied. For small signal analysis, all voltages, currents and the duty ratio are written as a combination of their averaged DC value and small signal time varying quantity

[1].

$$\begin{aligned}
\langle v_g(t)\rangle_{T_S} &= V_g + \hat{v_g}(t) \\
d(t) &= D + \hat{d}(t) \\
\langle v_{C1}(t)\rangle_{T_S} &= V_{C1} + \hat{v_{C1}}(t) \\
\langle v_{C2}(t)\rangle_{T_S} &= V_{C2} + \hat{v_{C2}}(t) \\
\langle i_{L1}(t)\rangle_{T_S} &= I_{L1} + \hat{i_{L1}}(t) \\
\langle i_{L2}(t)\rangle_{T_S} &= I_{L2} + \hat{i_{L2}}(t)
\end{aligned} \tag{3.17}$$

Taking T_{ON} and T_{OFF} mode equations and averaging them over one cycle we get,

$$L_1\frac{d\langle i_{L1}(t)\rangle_{T_s}}{dt} = \langle v_g(t)\rangle_{T_s} - \langle v_{C2}(t)\rangle_{T_s} + \langle v_{C1}(t)\rangle_{T_s}d(t) \tag{3.18}$$

$$L_2\frac{d\langle i_{L2}(t)\rangle_{T_s}}{dt} = \langle v_{C2}(t)\rangle_{T_s} - \langle v_{C1}(t)\rangle_{T_s} \tag{3.19}$$

$$C_1\frac{d\langle v_{C1}(t)\rangle_{T_s}}{dt} = \langle i_{L2}(t)\rangle_{T_s} - \langle i_{L1}(t)\rangle_{T_s}d(t) \tag{3.20}$$

$$C_2\frac{d\langle v_{C2}(t)\rangle_{T_s}}{dt} = \langle i_{L1}(t)\rangle_{T_s} - \langle i_{L2}(t)\rangle_{T_s} - \frac{\langle v_{C2}(t)\rangle_{T_s}}{R} \tag{3.21}$$

Values from (3.17) are substituted and the state space matrix is formed as given in (3.22).

$$\begin{pmatrix} \hat{i_{L1}}(t) \\ \hat{i_{L2}}(t) \\ \hat{v_{C1}}(t) \\ \hat{v_{C2}}(t) \end{pmatrix} = \begin{pmatrix} 0 & 0 & \frac{D}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} & \frac{1}{L_2} \\ \frac{-D}{C_1} & \frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & \frac{-1}{C_2} & 0 & \frac{-1}{RC_2} \end{pmatrix} \begin{pmatrix} \hat{i_{L1}}(t) \\ \hat{i_{L2}}(t) \\ \hat{v_{C1}}(t) \\ \hat{v_{C2}}(t) \end{pmatrix} + \begin{pmatrix} \frac{1}{L_1} & \frac{V_{C1}}{L_1} \\ 0 & 0 \\ 0 & \frac{-I_{L1}}{C_1} \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \hat{v_g}(t) \\ \hat{d}(t) \end{pmatrix} \tag{3.22}$$

For controlling the output voltage by varying the duty cycle, transfer function of output voltage to duty ratio (G_{vd}) is required. Hence the output equation is given as,

$$\hat{v_{C2}}(t) = \begin{pmatrix} 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} \hat{i_{L1}}(t) \\ \hat{i_{L2}}(t) \\ \hat{v_{C1}}(t) \\ \hat{v_{C2}}(t) \end{pmatrix} \tag{3.23}$$

Using (3.22) and (3.23) and taking their Laplace transforms, the following transfer function is obtained.

$$G_{vd}(s) = \frac{\begin{array}{r} V_{C1}RC_1L_2s^2 - I_1(L_1R + DL_2R)s \\ +V_{C1}R(1-D) \end{array}}{\begin{array}{r} RL_1L_2C_1C_2s^4 + L_1L_2C_1s^3 \\ +(RL_1C_1 + RL_2C_1 + RL_1C_2 + RL_2C_2D^2)s^2 \\ +(L_2D^2 + L_1)s + (D^2 - 2D + 1)R \end{array}} \tag{3.24}$$

For study, a 12/48 V, 100 W, 100 KHz switching frequency BCOCLF along with its controller is designed. 12 V input voltage is chosen because most batteries are 12 V sources, and 48 V is chosen because it is the optimum LVDC microgrid distribution voltage [20].

$V_g = 12\,\mathrm{V}$

$V_o = 48\,\mathrm{V}$

$P = 100\,\mathrm{W}$

$I_grated = 8.3334\,\mathrm{A}$

$I_orated = 2.083\,34\,\mathrm{A}$

$R_rated = 23.04\,\mathrm{A}$

$D = 0.75$

$f = 100\,\text{KHz}$

Substituting in (3.14), (3.15) and (3.16) we get,

$L_1 = 108\,\mu\text{H}$

$L_2 \approx L_1 = 108\,\mu\text{H}$

$C_1 = 3.225\,\mu\text{C}$

$C_2 = 1.085\,\mu\text{C}$

Substituting these values back in (3.24), and obtaining the G_{vd} bode plot as shown in Figure 3.14

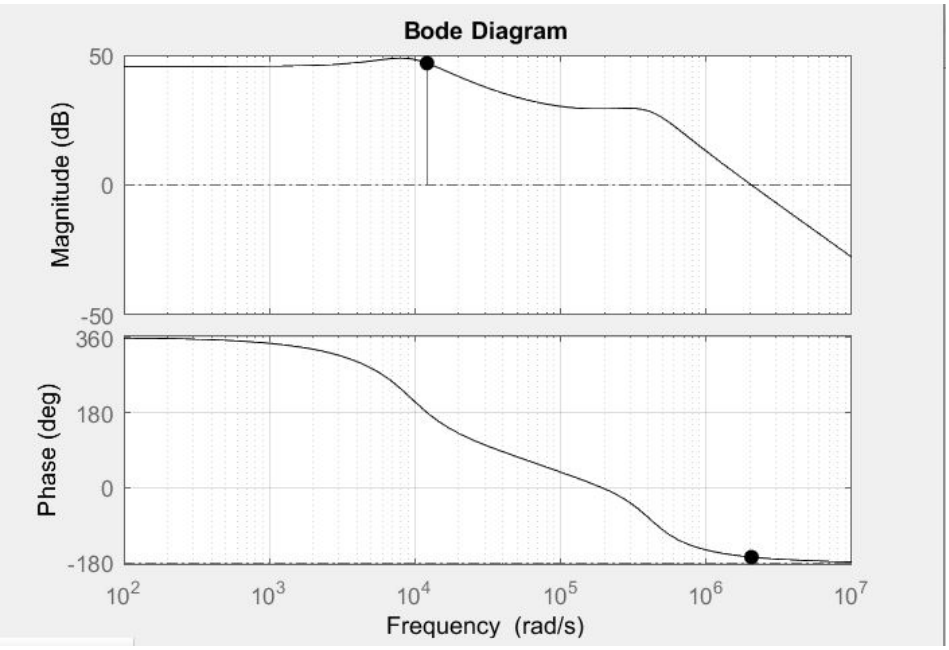

Figure 3.14: Bode plot of G_{vd} for designed BCOCLF

Clearly, the system is unstable with a phase margin of -526°at gain crossover frequency $\omega_{gc} = 2.05 \times 10^6$ rad/s and gain margin of $-46.9\,\text{dB}$ at phase crossover frequency $\omega_{pc} = 1.21 \times 10^4$ rad/s and hence a controller is required for its stable dynamic and steady state performance.

3.3.3 Controller Design

The general block diagram for control scheme of the mentioned converter is the same as we used for boost converter and is shown in Figure 3.2.

The converter output volatge is compared with reference value and error signal is generated. This error is fed to the controller having a gain G_c which generated a control voltage v_c. In the modulator block, this control voltage was compared with a sawtooth wave of peak magnitude V_m and frequency equal to the switching frequency of the converter as shown in Figure 3.15

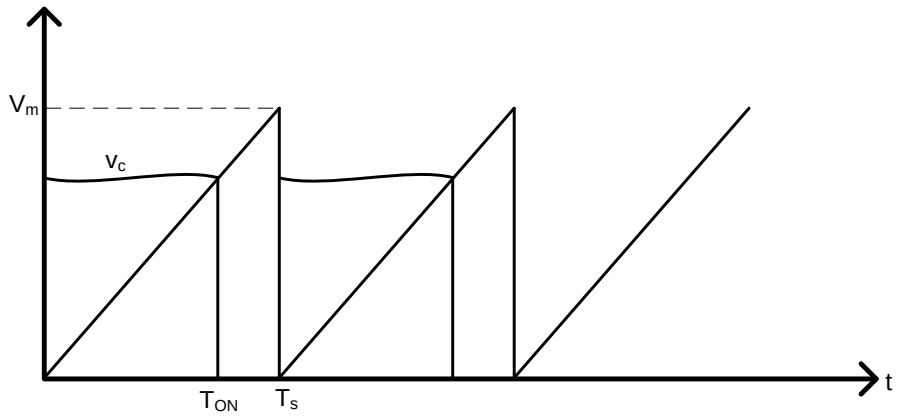

Figure 3.15: Gate pulse generation by modulator

In our case $V_m = 1V$ and $T_s = 10^{-5}s$.
A PI controller was used with transfer function

$$G_c = k_p + \frac{k_p}{sT}$$

Referring to the bode plot in Figure 3.14, the k_p and T values are set such that system is stabilized and steady state error is reduced. The controller was designed such that gain crossover frequency is obtained at 8000 rad/s, with a phase margin

of about 90°. Using the conditions

$$|G_c G_{vd}|_{8000\,\mathrm{rad/s}} = 1$$

and,

$$\frac{1}{T} = \frac{\omega_{gc}}{10}$$

the values are found to be $k_p = 3.6308 \times 10^{-3}$ and $T = \frac{1}{800}$. The overall system's bode plot was obtained as shown in Figure 3.16.

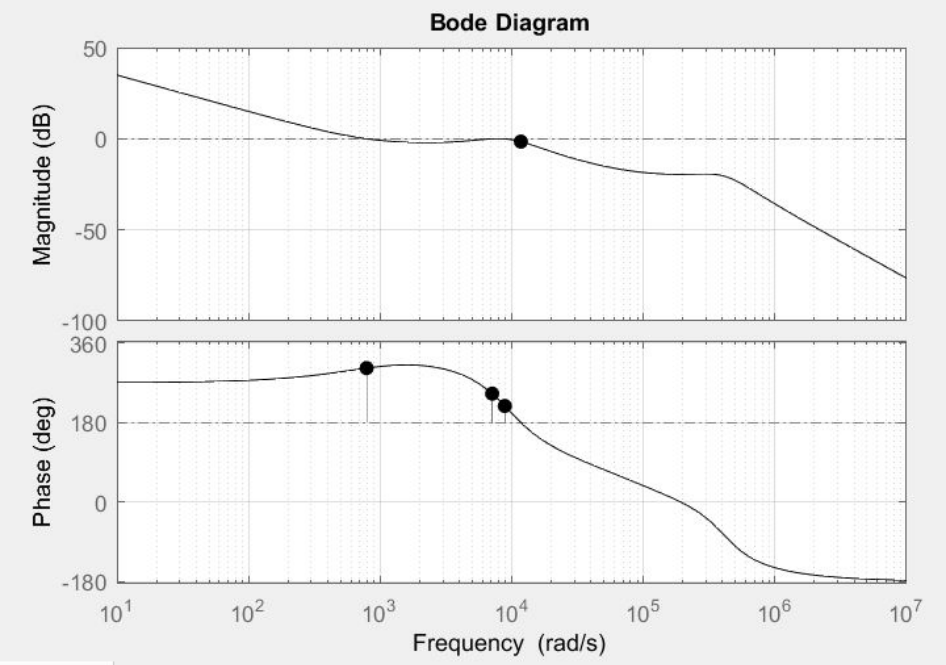

Figure 3.16: Bode plot of plant with controller

Owing to the curvature in the magnitude plot, due to resonance around 8000 rad/s, it is seen that the system is stable with a phase margin of 123°at gain crossover frequency $\omega_{gc} = 789\,\mathrm{rad/s}$ and gain margin of 1.57 dB at phase crossover frequency $\omega_{pc} = 11\,700\,\mathrm{rad/s}$. The steady state error is reduced to zero because of the pole at origin.

3.3.4 Results

The BCOCLF with calculated values of inductors, capacitors and controller parameters are simulated in MATLAB Simulink. The simulation was carried out of 500 ms and load was changed as,

0 ms - 125 ms: 100% of rated load, $R = 23.04\,\Omega$

125 ms - 250 ms: 75% of rated load, $R = 30.72\,\Omega$

250 ms - 375 ms: 50% of rated load, $R = 46.08\,\Omega$

375 ms - 500 ms: 25% of rated load, $R = 92.16\,\Omega$ Output voltage, output current, all other state variables and output power were observed for their mean value, peak to peak ripple percentage, settling time (t_s) and overshoot/peak to peak spike during a transient.

Consider Figure 3.17 showing BCOCLF and the quantities that are measured.

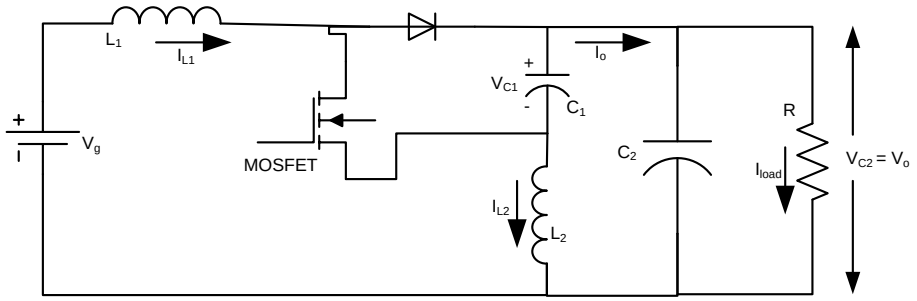

Figure 3.17: BCOCLF circuit diagram with to be measured quantities marked

The observations are shown in Figures 3.18 - 3.23.

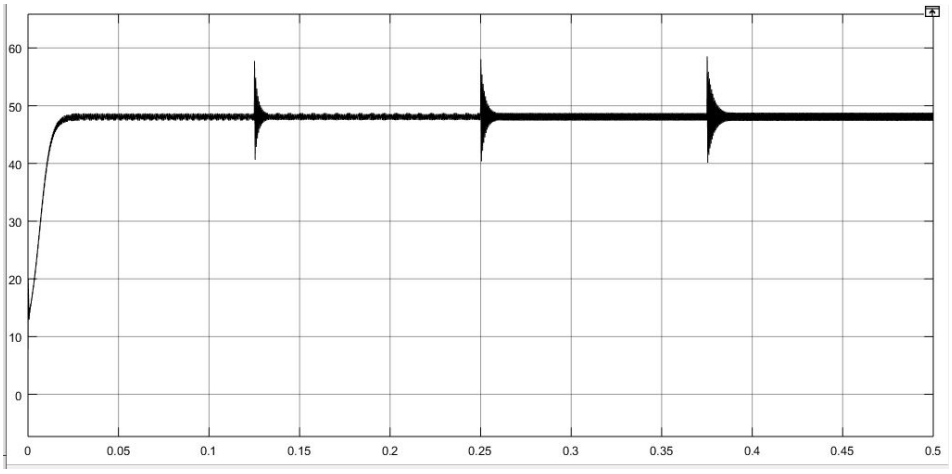

Figure 3.18: Output voltage $V_o(V)$ v/s Time(s)

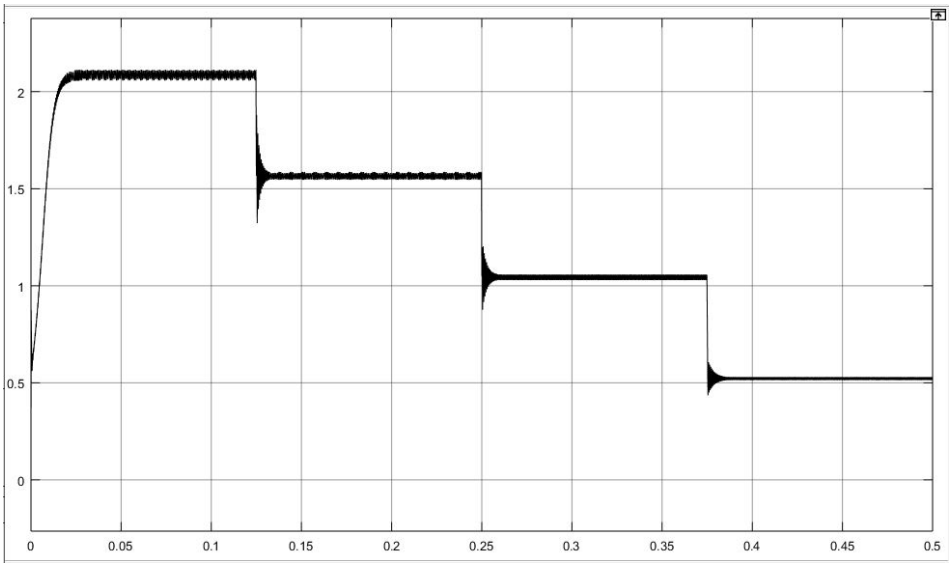

Figure 3.19: Load current $I_{load}(A)$ v/s Time(s)

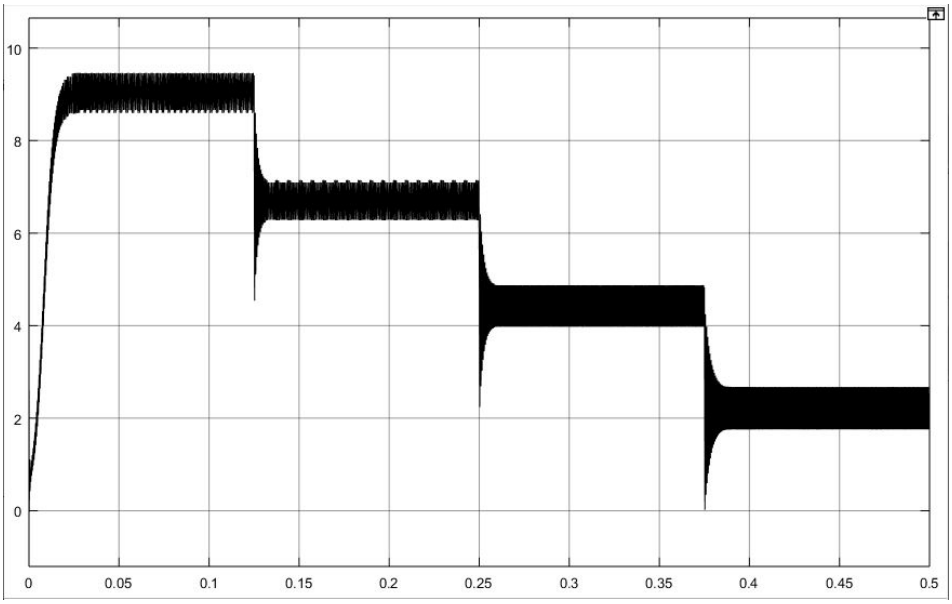

Figure 3.20: Inductor L_1 current $I_{L1}(A)$ v/s Time(s)

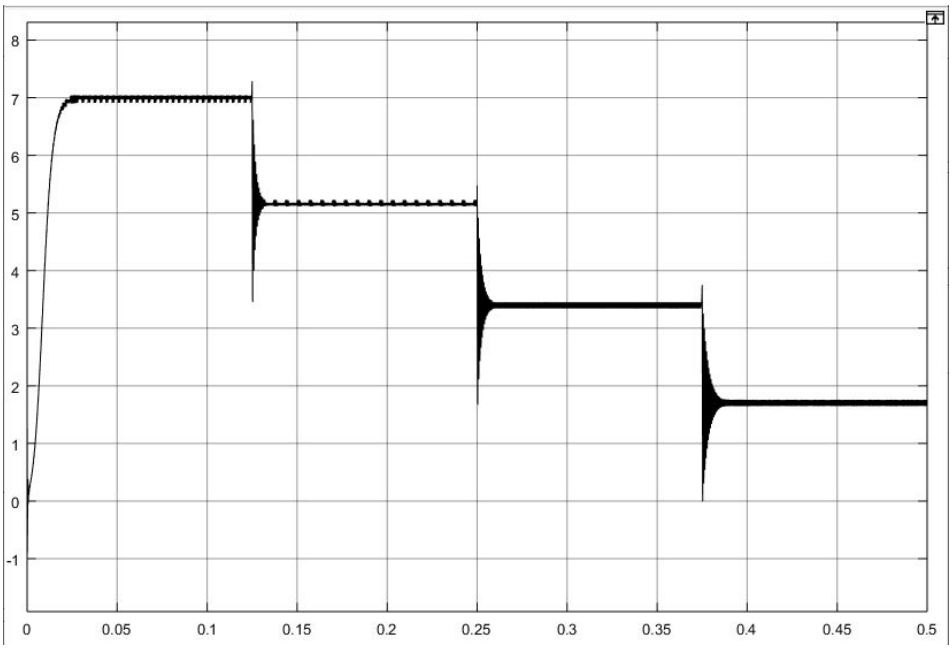

Figure 3.21: Inductor L_2 current $I_{L2}(A)$ v/s Time(s)

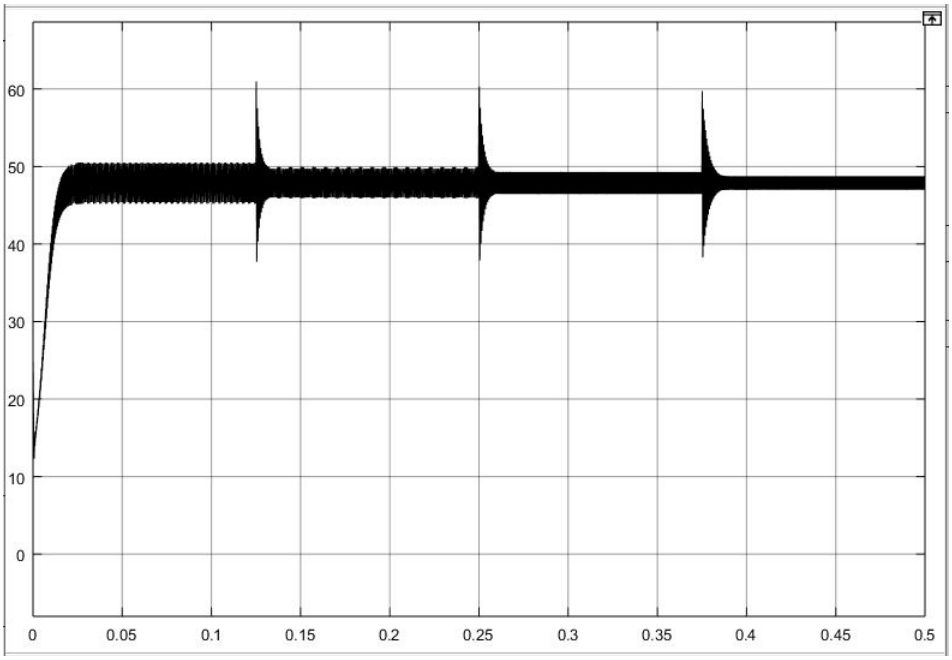

Figure 3.22: Capacitor C_1 voltage $V_{C1}(V)$ v/s Time(s)

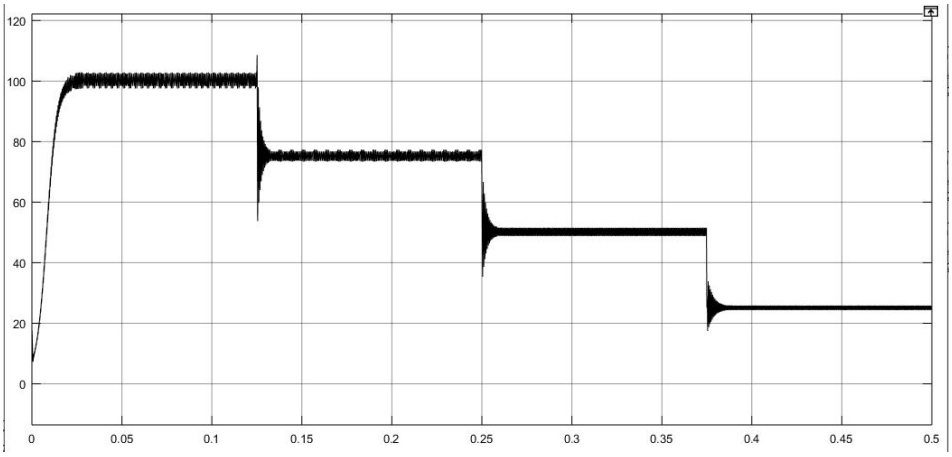

Figure 3.23: Output Power $P_o(W)$ of BCOCLF v/s Time(s)

The results are tabulated in Tables 3.1 to 3.4.

Note: All percentages are taken w.r.t. the mean value.

Quantity	Mean Value	t_s (ms)	Overshoot	p-p ripple (in %)
$V_o(V)$	48.00V	22	0	2.65
$I_{load}(A)$	2.08A	22	0	2.64
$P_o(W)$	99.99W	25	0	5.30
$I_{L1}(A)$	9.07A	21	0	9.55
$I_{L2}(A)$	6.99A	24	0	1.91
$V_{C1}(V)$	48.00V	20	0	11.08

Table 3.1: Results for 0-125 milliseconds, 100% load

Quantity	Mean Value	t_s (ms)	Spike	p-p ripple (in %)
$V_o(V)$	48.00V	7.90	17.12V	2.62
$I_{load}(A)$	1.56A	8.06	0.79A	2.62
$P_o(W)$	74.96W	7.67	54.85W	4.01
$I_{L1}(A)$	6.71A	7.29	4.22A	12.98
$I_{L2}(A)$	5.15A	7.78	3.83A	2.17
$V_{C1}(V)$	48.00V	7.42	23.28V	8.41

Table 3.2: Results for 125-250 milliseconds, 75% load

Quantity	Mean Value	t_s (ms)	Spike	p-p ripple (in %)
$V_o(V)$	48.00V	8.67	17.71V	2.72
$I_{load}(A)$	1.04A	8.34	0.71A	2.73
$P_o(W)$	50.00W	9.17	37.31W	5.47
$I_{L1}(A)$	4.44A	8.28	4.18A	20.26
$I_{L2}(A)$	3.39A	8.84	3.80A	3.211
$V_{C1}(V)$	48.00V	9.70	22.44V	5.96

Table 3.3: Results for 250-375 milliseconds, 50% load

Quantity	Mean Value	t_s (ms)	Spike	p-p ripple (in %)
$V_o(V)$	48.00V	11.34	18.42V	2.98
$I_{load}(A)$	0.52A	9.58	0.62A	3
$P_o(W)$	25.00W	9.64	19.56W	5.95
$I_{L1}(A)$	2.23A	11.05	4.29A	41.34
$I_{L2}(A)$	1.70A	11.29	3.76A	6.46
$V_{C1}(V)$	48.00V	11.95	21.47V	3.69

Table 3.4: Results for 375-500 milliseconds, 25% load

Now let us compare the converter output currents for boost converter and BCOCLF for same operating conditions. The boost converter output current, and BCOCLF's output current are shown in Figures 3.24 and 3.25.

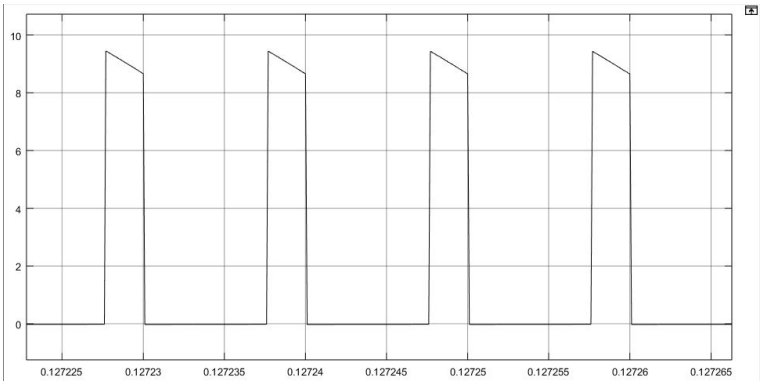

Figure 3.24: I_o (A) v/s time (s)

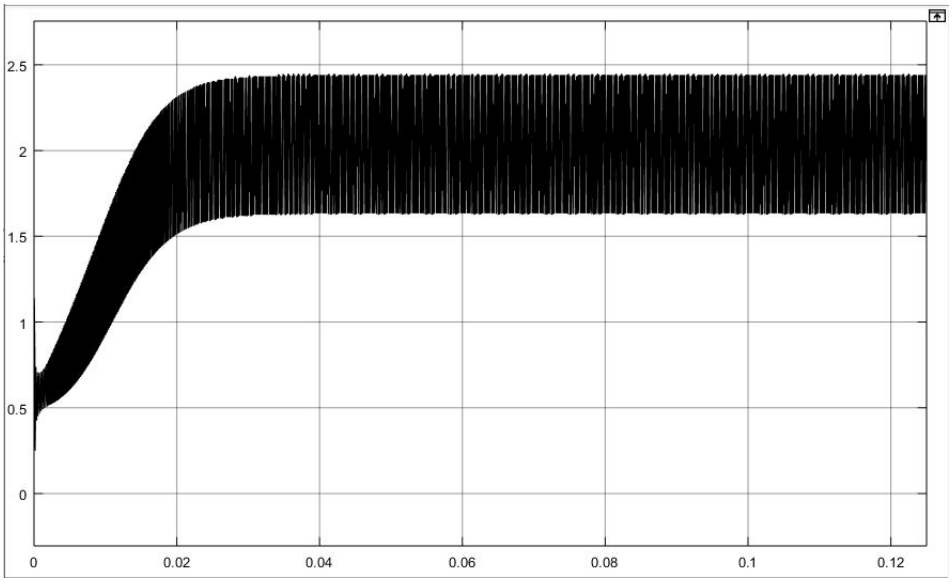

Figure 3.25: Output current $I_o(A)$ vs Time(s) for BCOCLF

From observing the output currents for the two converters, it is evident that the peak-peak variation for output current in boost converter is 9.41A which is reduced to 0.823A in BCOCLF; which means a nearly eleven times reduction!

This can mean an enhanced life of the output capacitor, as the internal heating of capacitors owing to ESR is greatly dependent on the current ripple magnitude [19]. Thus converter life shall be increased.

Summary

Firstly in this chapter, in section 3.1 the design of boost converter for 12/48 V, 100 W and 100 KHz switching frequency operation was discussed. We saw its resultant output voltage, output current and load current. It was observed that the converter's output current was discontinuous and hence peaky in nature, in order to meet the average load current demanded. This was found to be detrimental to output capacitor's life as it would cause much internal heating in it. Moreover, a peaky output current meant more ripple in the load current thus being harmful for sensitive loads as well. Thus we felt the need for fourth order converters. In section 3.2, a fourth order buck converter topology and its key features were discussed. Working on the same lines for boost converter, a fourth order boost converter topology - BCOCLF was introduces in section 3.3. For control of the converter, its output voltage to duty ratio transfer function was derived using small signal modelling and state space averaging methods. By simulating this converter and its controller for the same operating conditions as boost converter, the output voltage, output current, load current and all state variables were observed and results were tabulated. Finally it was seen how BCOCLF's output current was continuous owing to the converter's topology. Hence BCOCLF was found to have an upper edge on conventional boost converter in terms of steady state performance and converter life.

Chapter 4

Conclusions and Scope for Future Work

In this chapter, we shall make conclusions based on whatever is learned from simulating conventional boost converter and BCOCLF under given operating conditions. Further the scope of future development of this converter shall be discussed.

4.1 Conclusions

Observing the analysis and performance of conventional boost converter and BCOCLF, we conclude the following points:

- **Converter gain:** The converter gain for BCOCLF is same as that of the conventional boost converter, despite of the output CL filter.
- **Load current ripple reduction:** The conventional boost converter of same power rating, voltage transformation ratio and switching frequency operating for full load had a load current ripple of around 5%. BCOCLF

on the other hand, has 2.65% of load current ripple, which is nearly half of the conventional value.

- **Output current ripple:** Due to the presence of CL filter, output current of BCOCLF is not discontinuous as it is the case with conventional boost converter. As a result, for the same load, the output current need not be peaky unlike the conventional boost converter. The peak-peak variation for output current in boost converter was reduced by 11 times in BCOCLF. This could mean enhanced life of the output capacitor, as the internal heating of capacitors owing to ESR is greatly dependent on the current ripple magnitude [19]. Thus converter life shall be increased.

- **Complexity:** As the number of storage elements increases, complexity of the system increases. Analysis and controller design becomes cumbersome. Moreover, transient analysis becomes intricate.

- **Reliability:** BCOCLF uses four storage elements and one switching device while boost converter uses two storage elements and one switching device. Failure of any of these components will lead to malfunctioning of the converter. Therefore, BCOCLF is less reliable as compared to boost converter.

- **Cost:** All performance advantages of BCOCLF come at the cost of an additional inductor-capacitor pair. Comparing values of capacitance- the required value for boost converter is about $8\,\mu$C and the total required value for BCOCLF is about $3\,\mu\text{C} + 1\,\mu\text{C} = 4\,\mu\text{C}$ which is still lesser than that for the boost converter. Moreover, since BCOCLF requires two capacitors, manufacturing multiple BCOCLFs would require capacitors to be purchased in bulk. Both these factors - decreased capacitance value requirement and purchasing capacitors in bulk shall bring down the cost of manufacturing of BCOCLF. But on the other hand, there is also an extra inductance required

and the total inductance requirement value for BCOCLF exceeds that of boost converter. Hence, on an overall basis, BCOCLF would be a costlier device.

4.2 Scope of Future Development

Although BCOCLF seems to work properly under given operating conditions, its study is not yet complete. There are certain areas which can be worked upon in future to enable BCOCLF a cost effective, and a robust device thereby making it a usable product in power systems industry. They are listed as follows:

- **Inductor L_2 design:** The current through inductor L_2 was found to be a non-linear function of time, and hence designing precise value of L_2 was found cumbersome. Hence for the sake of simplicity, its value was approximated to that of inductor L_1. Further studies can be carried to find precise value of L_2.

- **Analysis with losses:** All the analysis done in this report was for loss-less, ideal operation of the converter. Further studies can be done considering resistive inductors and capacitors with ESR, along with diode voltage drop and switching losses.

- **DCM operation:** In the report, the DC-DC converter BCOCLF was analyzed for only continuous current mode (CCM) operation. Studies can be extended to DCM operation as well.

- **Application to microgrids:** Converter studies for its application to microgrids for interfacing batteries, solar panels etc. can be carried out, making use of its technical advantages for a superior service in power systems.

References

[1] R.W. Erickson and D. Maksimović (2000). *Fundamentals of Power Electronics, Second Edition.* New York: Springer.

[2] L. Umanand (2013). *Switched Mode Power Conversion (Video).* IISc Bangalore: NPTEL.

[3] S. Dahale, A. Das, N. M. Pindoriya and S. Rajendran, "An overview of DC-DC converter topologies and controls in DC microgrid," *2017 7th International Conference on Power Systems (ICPS)*, Pune, 2017, pp. 410-415.

[4] M. A. Chewale, R. A.Wanjari, V. B.Savakhande and P. R.Sonawane, "A Review on Isolated and Non-isolated DC-DC Converter for PV Application," *2018 International Conference on Control, Power, Communication and Computing Technologies (ICCPCCT)*, Kannur, 2018, pp. 399-404.

[5] N. Omar, J. Van Mierlo, B. Verbrugge, and P. Van den Bossche, Power and life enhancement of battery-electrical double layer capacitor for hybrid electric and charge-depleting plug-in vehicle applications, *Electrochimica Acta*, vol. 55, no. 25, pp. 75247531, Oct. 2010.

[6] E. Schaltz, A. Khaligh, and P.O. Rasmussen, Influence of battery/ultracapacitor energy-storage sizing on battery lifetime in a fuel cell hybrid electric vehicle, *IEEE Trans. Veh. Technol.*, vol. 58, no. 8, pp. 38823891, Oct. 2009.

[7] R. Carter, A. Cruden, and P. J. Hall, Optimizing for efficiency or battery life in a battery/supercapacitor electric vehicle, *IEEE Trans. Veh. Technol.*, vol. 61,

no. 4, pp. 15261533, May 2012.

[8] J. Cao and A. Emadi, A new battery/ultracapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehicles, *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 122132, Jan. 2012.

[9] L. Ni, D. J. Patterson, and J. L. Hudgins, High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application, *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 11411151, Mar. 2012.

[10] M. Camara, B. Dakyo, and H. Gualous, Polynomial control method of DC/DC converters for DC-Bus voltage and currents management battery and supercapacitors, *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 14551467, Mar. 2012.

[11] J. J. Awerbuch and C. R. Sullivan, Control of ultracapacitor-battery hybrid power source for vehicular applications, *in Proc. IEEE Energy 2030 Conf.*, Nov. 2008, pp. 17.

[12] V. Grigore and J. Kyyra, "A step-down converter with low ripple input current for power factor correction," *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, New Orleans, LA, USA, 2000, pp. 188-194 vol.1.

[13] M. Veerachary, "Analysis of Minimum-Phase Fourth-Order Buck DCDC Converter," *in IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 144-154, Jan. 2016.

[14] M. Veerachary and A. S. Choudhary, "Design and analysis of 4th-order buck DC-DC converter," *2014 9th International Conference on Industrial and Information Systems (ICIIS)*, Gwalior, 2014, pp. 1-6.

[15] M. Veerachary, "High gain fourth-order boost converter for DC-grid applications," *2016 IEEE 7th Power India International Conference (PIICON)*, Bikaner, 2016, pp. 1-6.

[16] Z. Qiu, H. Lu, Y. Cui, and Y. Mei, Design of a new type of the damped filter for system stability of DCDC converter, *in Proc. IEEE ISAPE*, 2012, pp. 10821085.

[17] M. Veerachary, "Analysis of fourth-order double boost converter," *2014 6th IEEE Power India International Conference (PIICON)*, Delhi, 2014, pp. 1-6.

[18] http://www.ti.com/lit/an/slva372c/slva372c.pdf

[19] N. Khera, S. A. Khan, T. Islam and A. K. Agarwala, "Low cost online method for condition monitoring of aluminum electrolytic capacitors," *2014 International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, 2014, pp. 771-774.

[20] M. Alam, K. Kumar, J. Srivastava and V. Dutta, "A Study on DC Microgrids Voltages based on Photovoltaic and Fuel Cell Power Generators," *2018 7th International Conference on Renewable Energy Research and Applications (ICRERA)*, Paris, 2018, pp. 643-648.