Design of a 4-bit flash ADC in a TSMC180nm process

A Thesis

Submitted by

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THESIS CERTIFICATE

This is to certify that the thesis entitled **"Design of a 4-bit flash ADC in a TSMC180nm process"** submitted by **YARRAMNENI GEETHA PRASUNA**, to the Indian Institute of Technology, Madras for the award of the degree of **BACHELOR OF TECHNOLOGY** is a bonafide record of research work carried out by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT:

Low resolution flash ADCs are used as part of quantizers in delta-sigma ADCs. In this work, a 4-bit flash ADC is designed for use in a delta-sigma ADC. It is designed in the TSMC 180nm process based on a similar design in the UMC 180nm process.

CHAPTER 1

INTRODUCTION

Flash ADCs are made by cascading high-speed comparators. Fig. 1.1 shows as N-bit flash ADC. The circuit uses 2^N-1 comparators for an N-bit converter. The reference voltage is provided by a resistive divider with 2^N resistors. Each comparator's reference voltage is one least significant bit (LSB) higher than the reference voltage of the comparator below it. When the analog input voltage V_i of a comparator exceeds the reference voltage applied to it, the comparator outputs a 1, otherwise, the output is 0. Comparators X_1 through X_4 produce 1's and the remaining comparators produce 0's if the analog input is between V_{X4} and V_{X5}. The input signal becomes smaller than the respective comparator reference-voltage levels at the point where the code changes from ones to zeros.

The output of the comparator array is in the form of *thermometer code*. The name comes from the fact that the design is similar to that of a mercury thermometer, in which the mercury column always rises to the proper temperature and no mercury is present above it.

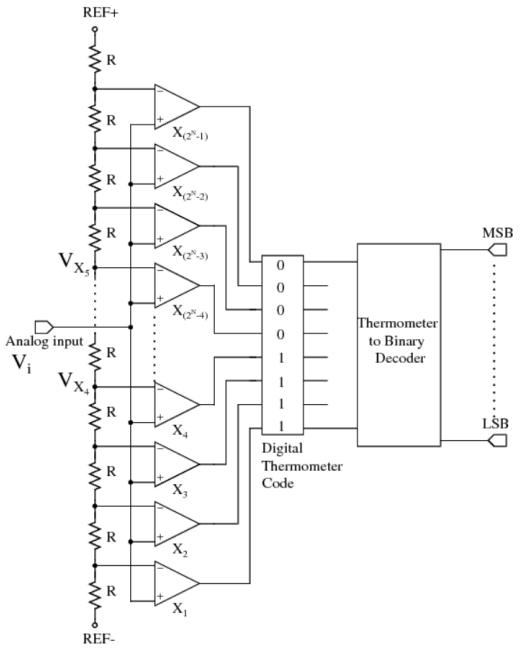

Fig. 1.1 Sample block diagram of N-bit flash ADC.

CHAPTER 2

FLASH ADC DESIGN IN UMC180:

A 16-level mid-rise flash ADC is designed in UMC180. This will require the use of fifteen comparators. Each of the comparators has a strong-arm latch which reduces the number of clock phases required by the ADC.

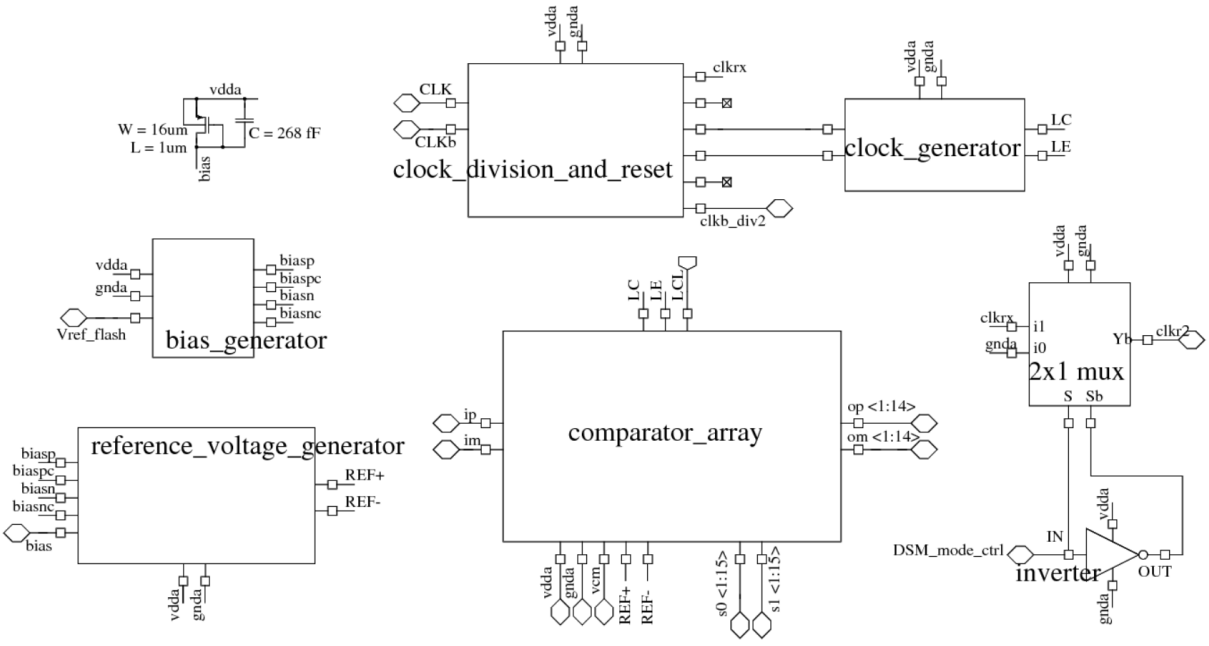

Fig. 2.1 Flash ADC schematic in UMC180

List of blocks in Flash ADC:

- bias_generator
- reference_voltage_generator
- comparator_array
- clock_division_and_reset
- clock_generator
- 2x1_mux
- inverter

2.1 Creating test bench for flash ADC in UMC180:

The output of the flash ADC in Fig. 2.1 is a 15-bit thermometer code. Thermometer code is converted into binary code using the thermometer to binary code block (Therm_to_Bin). Thereafter, there's an ideal DAC block (ideal_DAC) that outputs 16 levels (output node named as dsmout) taking binary code as input. SNR is calculated from dsmout. Clocks and currents will be generated by the remaining blocks in the test bench shown below.

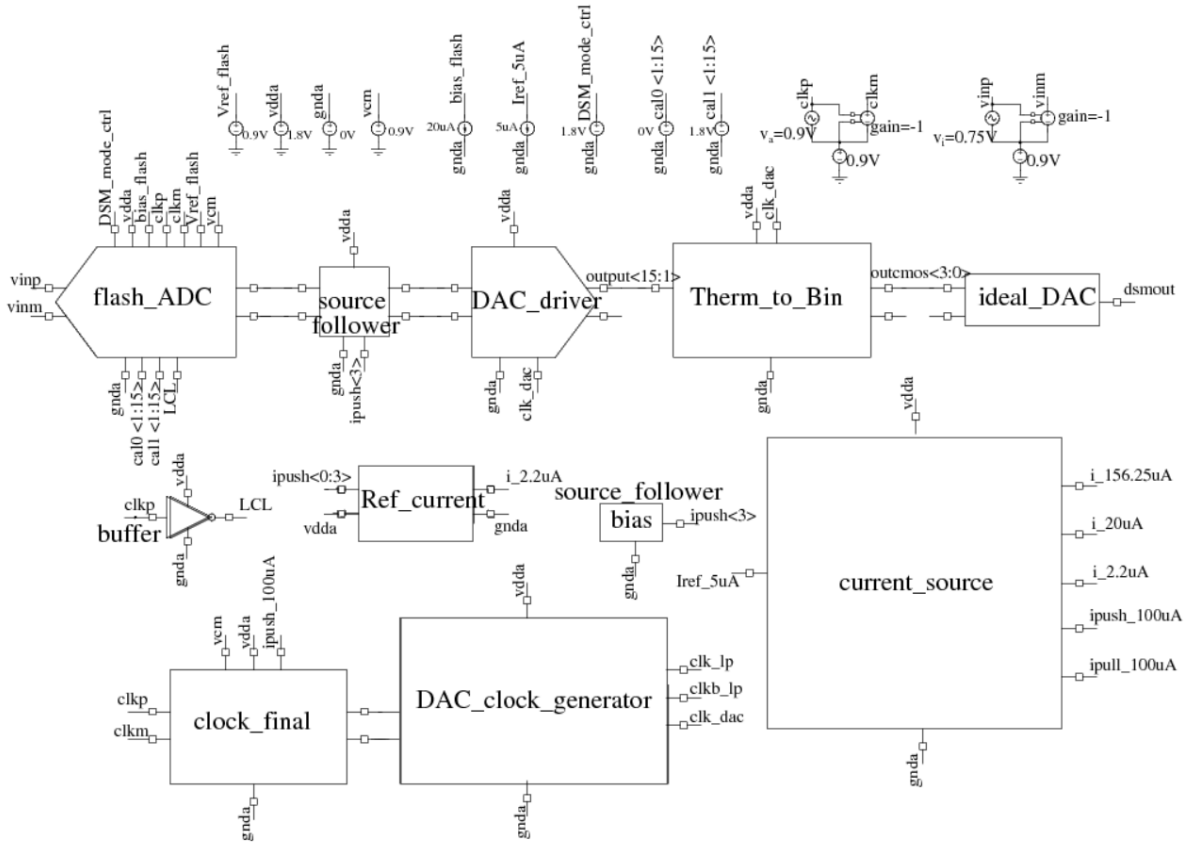

Fig. 2.2 Flash ADC Test Bench schematic in UMC180

2.2 Flash ADC schematic simulation in UMC180:

A differential sine wave with an amplitude of 0.75 V (V_i) and a DC voltage of 0.9 V is fed into the flash ADC with an input frequency of 800 * (5/512) which is 7.81 MHz and a sampling frequency of 800 MHz with a supply voltage of 1.8 V. The duration of the transient simulation for an N point FFT, should be greater than N/800 MHz, so running a transient simulation

for 0.86 us and using 512-point FFT with hanning window and 3 signal bins included, yields an SNR of 25.84 dB, which is identical to the ideal SNR for a 4-bit flash ADC, 25.84 dB.

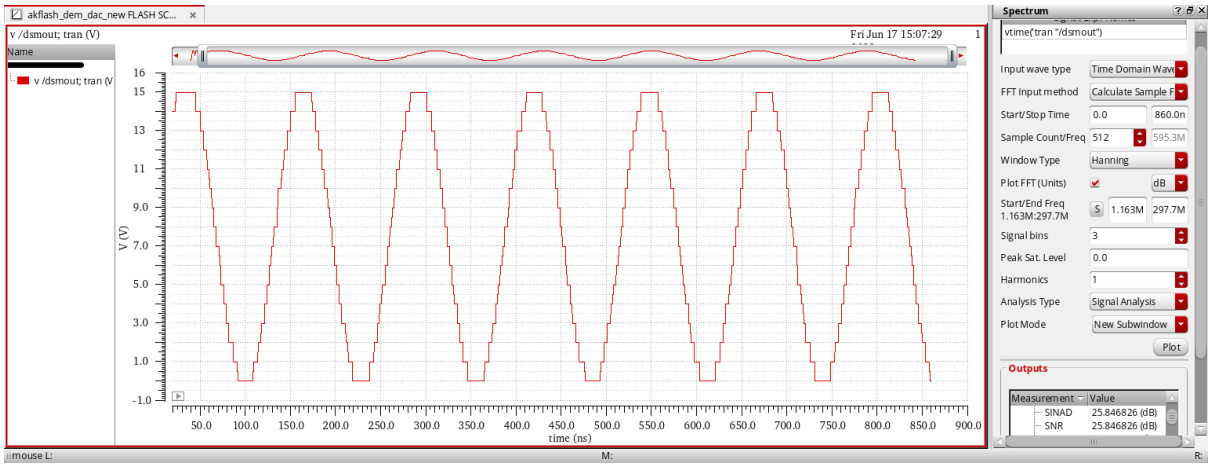

Fig. 2.3 Output of ideal_DAC and SNR simulation from the same.

CHAPTER 3

FLASH ADC SCHEMATIC IN TSMC180:

3.1 Porting schematic from UMC180 to TSMC180:

The schematic in TSMC180 is obtained by hierarchically copying the entire schematic of the flash ADC, including its test bench, from UMC180 to TSMC180 and then running the script 'Remasterinstances_v7.il' for updating the devices (NMOS, PMOS, resistor, and capacitor) in each of the blocks. Following are the device names in UMC180 and their equivalent devices in TSMC180.

Table 3.1 UMC180 devices and their equivalent devices in TSMC180

UMC180		TSMC180	
Library	Device Name	Library	Device Name
UMC180	N_18_MM	tsmc18	nmos2v_mac
UMC180	P_18_MM	tsmc18	pmos2v_mac
UMC180	MIMCAPS_MM	tsmc18	mimcap_2p0_sin
UMC180	RNHR1000_MM	tsmc18	rphripoly

3.2 Flaws in the script and modifications to the TSMC180 schematic:

- A few transistor widths were changed from 240 nm in UMC180 to 2 um in TSMC180 by the script. So, they were manually changed back to 240 um.
- The script did not update the multiplicity of the MOSFETs, so all MOSFETs were assigned a default multiplicity of 1. They were given their original multiplicity manually on a case-by-case basis.
- In TSMC180, NCAP_MM and PCAP_MM from UMC180 must be replaced with NMOS and PMOS capacitors, respectively. The series resistance of

a MOS capacitor is proportional to its length. To reduce the delay, the length is reduced from 4 um to 0.5 um while the number of fingers is increased proportionately to keep the area the same.

3.3 Flash ADC schematic simulation in TSMC180:

With all the input conditions (supply voltage, input amplitude, and sampling frequency) being the same as UMC180 for TSMC180, the SNR value obtained was 24.25 dB.

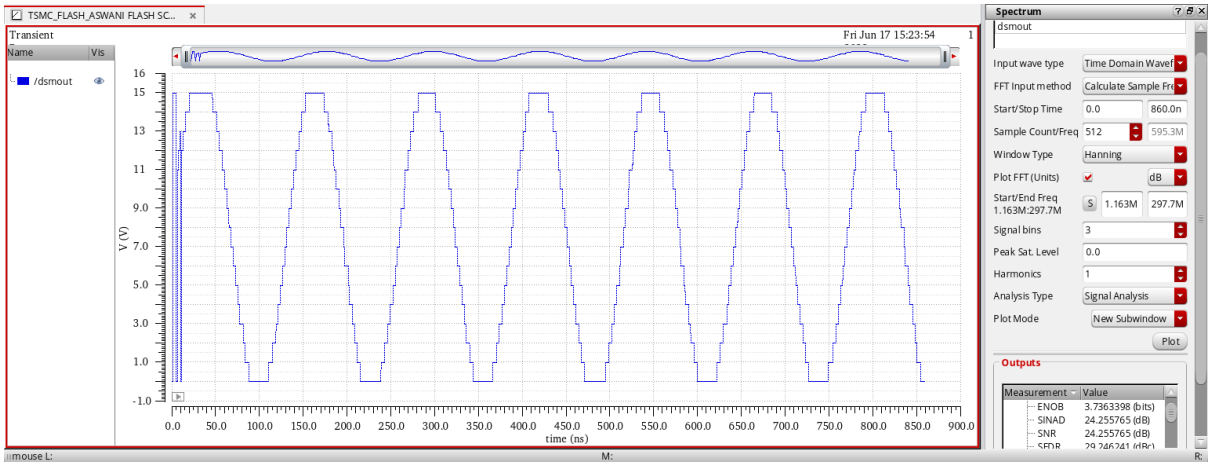

Fig. 3.1 Output of ideal_DAC and SNR simulation from the same.

In order to improve SNR, the input differential amplitude was slightly tweaked around 0.75 V, to observe its effect on the SNR and at 0.7025 V, the SNR reached a maximum of 25.55 dB.

Table 3.2 SNR variation with Input Amplitude

Percentage change in input voltage peak	0%	4.50%	5%	5.60%	6.30%	7%	7.50%	10%
vip maximum (in V)	1.65	1.616	1.612	1.607	1.602	1.597	1.593	1.575
vip minimum (in V)	0.15	0.183	0.187	0.192	0.197	0.202	0.206	0.225
amplitude of differential input (in V)	0.75	0.716	0.712	0.7075	0.7025	0.6975	0.6935	0.675
SNR in dB	**24.25**	25.438	25.45	25.555	**25.556**	25.25	25.375	25

For further improvement, comparing node voltages, the problem is found to be in common mode reference voltages (vcmref+ and vcmref-) generated by the reference_voltage_generator block which go to the comparators as Vrefa<1:15> after being generated by resistor chain between vcmref+ and vcmref-. The common-mode reference voltages are listed below. From table 3.3 the deviation in reference voltages is less for voltages around 0.9 V (green highlighted entries). The full-scale is off, which could be due to a problem with currents and/or resistor values in the reference_voltage_generator block.

Table 3.3 Comparison of common mode reference voltages

	UMC180 testbench	**TSMC180 test bench**
vcmref+ (in V)	1.639	1.615
vcmref- (in V)	0.1442	0.171
vrefa<1> (in V)	1.542	1.521
vrefa<2> (in V)	1.446	1.429
vrefa<3> (in V)	1.352	1.338
vrefa<4> (in V)	1.259	1.248
vrefa<5> (in V)	1.166	1.16
vrefa<6> (in V)	1.075	1.07
vrefa<7> (in V)	0.983	0.982
vrefa<8> (in V)	0.893	0.894
vrefa<9> (in V)	0.802	0.805
vrefa<10> (in V)	0.71	0.717
vrefa<11> (in V)	0.619	0.628
vrefa<12> (in V)	0.526	0.539
vrefa<13> (in V)	0.433	0.449
vrefa<14> (in V)	0.34	0.358
vrefa<15> (in V)	0.245	0.267

CHAPTER 4

FLASH ADC LAYOUT IN TSMC180:

4.1 Streaming layout from UMC180 to TSMC180:

The flash ADC layout was exported from UMC180 to TSMC180 block by block using the layer map, which was created by mapping layers of UMC180 to TSMC180.

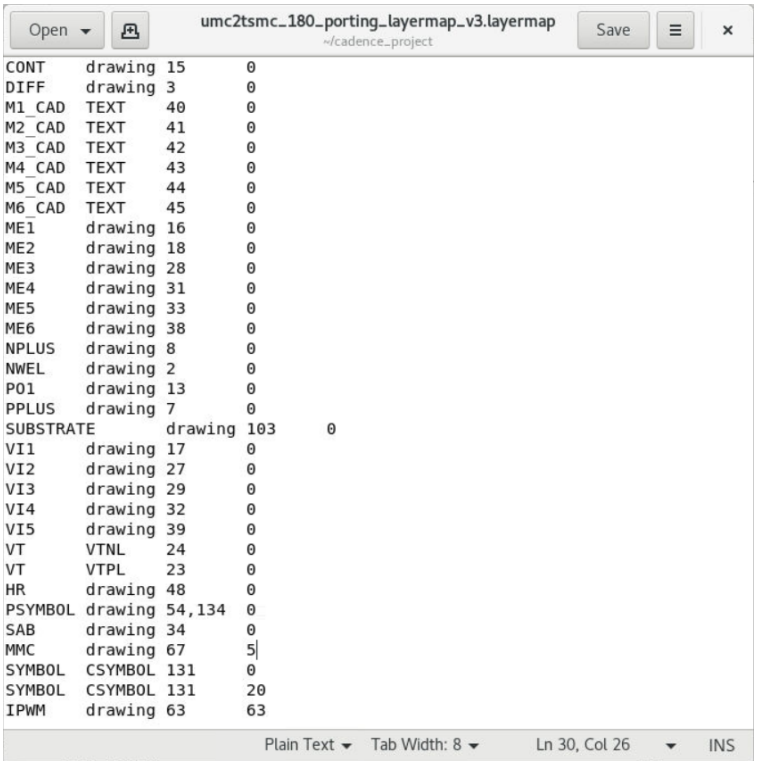

Fig. 4.1 Layer map from UMC180 to TSMC180.

4.2 Replacing resistors and capacitors manually:

UMC180 layers are substituted with corresponding TSMC180 layers in the preceding step, but the build of resistors and capacitors in TSMC180 differs from UMC180, so these must be manually instantiated in the layout.

In a subsequent trial to reduce the area by searching for a denser resistor, rphripoly is discovered to have the highest density (1.08 kohm/um at minimum width of 1 um). Furthermore, the width and length of resistors and capacitors differ in TSMC180 and UMC180, owing to the large minimum width and minimum length in TSMC180. The values are listed below.

Table 4.1 Minimum width and length of resistor and capacitor

UMC180	Minimum width	Minimum length
Resistor (RNHR1000_MM)	180 nm	1 um
Capacitor (MIMCAPS_MM)	1.28 um	1.28 um
TSMC180	Minimum width	Minimum length
Resistor (rphripoly)	1 um	2 um
Capacitor (mimcap_2p0_sin_2t)	4 um	4 um

The layout must be changed significantly to fit these large resistors and capacitors of the same value as UMC180 in TSMC180, as shown below.

Table 4.2 Comparison of widths and lengths for same resistance and capacitance values

	UMC 180	Available space after exporting layers to TSMC180	TSMC 180
Typical Resistance value:	14.98 kohm	14.98 kohm	14.98 kohm
Width	0.2 um	0.2 um	1 um
Length	3 um	4.5 um	13.4 um
Typical Capacitance value:	35.6 fF	35.6 fF	35.6 fF
Width	3.1 um	4.1 um	4 um
Length	7.6 um	11.2 um	4 um

To save space, common-mode feedback resistors of 40 kohms are replaced with 20 kohms in the reference_voltage_generator block in TSMC180. Transient simulations were re-run with 20 kohm resistors in the schematic to ensure that no effect on SNR was observed.

4.3 Measures taken during modification the Layout:

- All of the metals were drawn with a width that was neither too small nor too large.
- No metal lines are run over capacitors to reduce parasitics.
- Metal lines that contact the resistor's end are designed to add very little resistance in comparison to the resistor itself.
- Symmetry of the layout is not compromised at any point.

4.4 LVS issues:

- Missing Bulk connections:

  Bulk connections to every MOSFET are made using a multipart path.

- Missing labels/ports/instances:

  Provide pins to metal lines according to the schematic; in a few cases, labels were streamed as text in the layout, resulting in a missing label error. These errors are solved by renaming text as metal pins.

- MOSFETs length mismatch:

  MOS capacitors are manually replaced in the layout because the instances in the TSMC180 schematic are shorter and have more fingers than those in the UMC180 schematic. These MOSFETs bulk connections have also been properly made.

- Resistance mismatch:

  When a particular resistor is made to fit in a particular space by making it into a few segments in series, resistance mismatch can occur. Slightly tweaking the length of the resistor in the schematic such that it is made to be a multiple of segment length in layout solves the issue.

4.5 DRC issues:

- Vias width and spacing:

  Vias 1 to 4 must be 0.26 um x 0.26 um wide, while Via 5 must be 0.36 um x 0.36 um wide. In the TSMC180 layout, all the vias are selected at once to make their dimensions equal to the above values. Vias 1 to 4 must have a minimum spacing of 0.26 um which has been met easily but Via 5 must be spaced at a minimum of 0.35 um.

- Contact width and spacing:

  All contacts are selected to make their width 0.22 um x 0.22 um and are spaced at a minimum of 0.25 um.

- Metal width, spacing, area:

  Metal 6 must have a minimum width of 2.6 um and a minimum spacing of 2.5 um. These are significantly larger than UMC180 (1.2 um as minimum width and 1um as minimum spacing) and must be changed in the TSMC180 layout. Metal area errors require a minimum of 0.202 um2 of the metal area on the via. As a result, the enclosures of these metals must all be changed to 0.095 um on all the sides (left, right, top, bottom).

- Nwell spacing:

  The spacing between nwells of the same potential must be at least 0.6um. To solve this error, extra nwells are drawn in between the gaps to make all the nwells touch.

- PIMP and NIMP spacing and minimum width:

  PIMPs / NIMPs must have a minimum width of 0.44 um and minimum spacing of 0.44 um. To solve this, PIMP / NIMP are drawn respectively in such a way that they just touch.

4.6 DRC Antenna issues:

- Long metal lines on the layout serve as antennas when connected to the MOSFETs gate on one end. To solve this, the metal line is snipped closer to the gate, carried to one of the top metals, and then returned to the original metal.

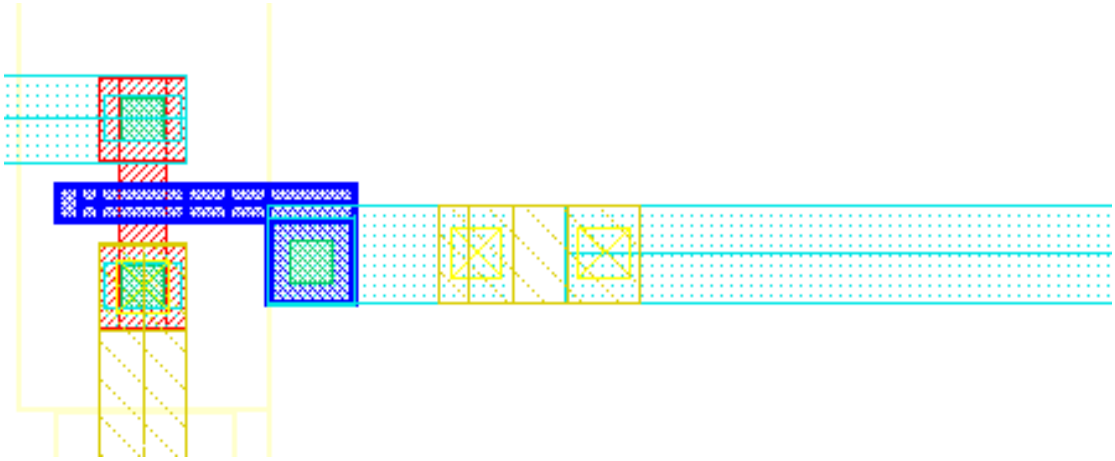

Fig. 4.2 Example connection to avoid Metal 1 acting as antenna.

- When the connections to mimcap_sin_2t are made directly using metal 5 for one terminal and metal 6 for the other, the antenna error occurs. Taking the terminal with the metal 5 connection to metal 6 first and then back to any desired metal for connection solves the antenna error.

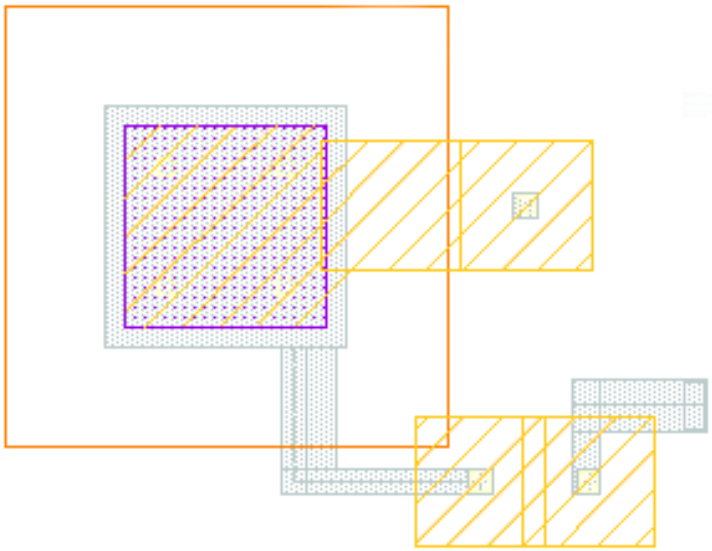

Fig. 4.3 Example showing Metal 5 carried to Metal 6 and brought back to Metal 5.

CHAPTER 5

MOS CAPACITOR SIMULATIONS:

5.1 Modeling MOS capacitor with ideal components:

To model a MOS capacitor with an ideal resistor in series with the capacitor, use portz in cadence to find Z parameters, where real (Zin) is series resistance and imaginary (Zin) is 1/(jwC), where C is capacitance. The modeled MOS capacitor with varying numbers of fingers is shown below.

Table 5.1 series resistance (R_series) and gds for MOSFETSs in UMC180 and TSMC180

TSMC180	Bias voltage = 0.9 V				
Pmos2v_mac	area= W* L * Fin = 64 um^2				
Width	Length	Fingers	R_series: real (Zin) constant across frequency from 10 kHz to 10 MHz	Capacitance	gds
4 um	4 um	4	12 ohms	550 fF	130.9 uS
4 um	2 um	8	6 ohms	553 fF	508.74 uS
4 um	1 um	16	3 ohms	559 fF	1.97 mS
4 um	0.5 um	32	1.5 ohms	571 fF	8.43 mS
Nmos2v_mac	area= W* L * Fin = 64 um^2				
Width	Length	Fingers	R_series (in ohm)	Capacitance	gds
2 um	4 um	8	2.99 ohms	561 fF	537 uS
2 um	2 um	16	1.49 ohms	563 fF	2.11 mS
2 um	1 um	32	0.744 ohms	569 fF	8.32 mS
2 um	0.5 um	64	0.37 ohms	580 fF	33.4 mS

UMC180	Bias voltage = 0.9 V				
P18_MM	area= W* L * Fin = 64 um^2				
Width	Length	Fingers	R_series (ohms)	Capacitance	gds
4 um	4 um	4	in order of nano	525 fF	98 uS
4 um	2 um	8	in order of nano	523 fF	381 uS
4 um	1 um	16	in order of nano	522 fF	1.46 mS
4 um	0.5 um	32	in order of nano	531 fF	5.74 mS
N18_MM	area= W* L * Fin = 64 um^2				
Width	Length	Fingers	R_series (ohms)	Capacitance	gds
2 um	4 um	8	in order of nano	532 fF	632 uS
2 um	2 um	16	in order of nano	536 fF	2.45 mS
2 um	1 um	32	in order of nano	544 fF	9.28 mS
2 um	0.5 um	64	in order of nano	565 fF	33.7 mS

It can be seen that, as the number of fingers increases with total length remaining constant, series resistance decreases proportionally. In addition, series resistance is significantly larger in TSMC180 than in UMC180. This is suspected to be due to modelling error in UMC180.

5.2 Modeling the distributed channel resistor of the MOS capacitor:

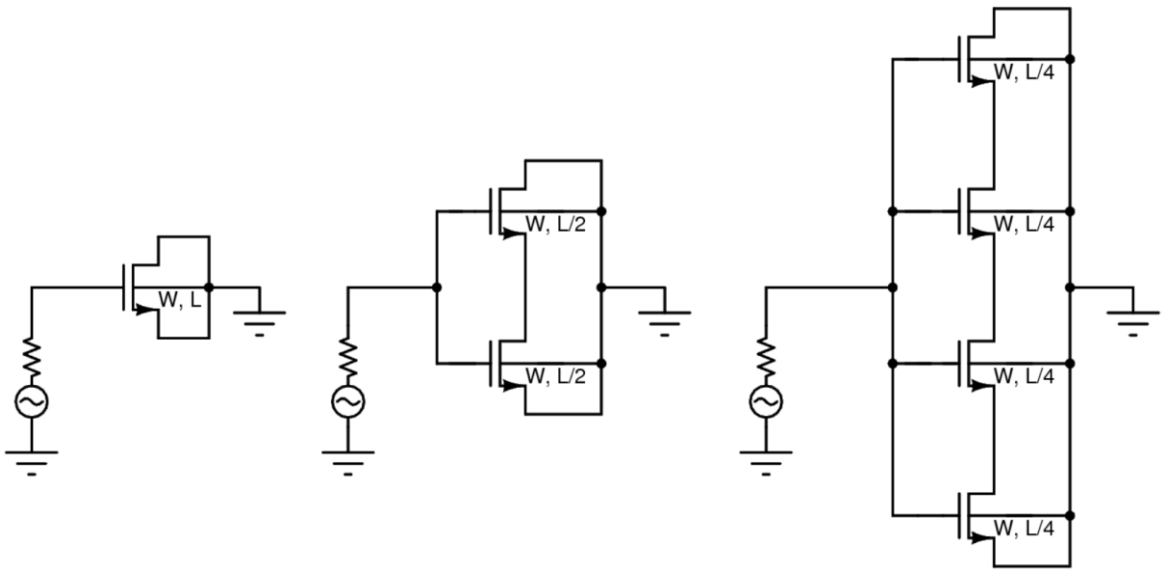

Fig. 5.1 MOS capacitor with varying number of transistor fingers in series.

Table 5.2 Series resistance and gds for transistor fingers in series

TSMC180	Bias voltage = 0.9 V					
Device name	Length (um)	Width (um)	number of devices in series	R_series : Re (Zin) in ohms	gds (in uS)	1/gds (in kohm)
nmos2v_mac	2	2	1	24	128	7.81
nmos2v_mac	1	2	2	541	248	4.03
nmos2v_mac	0.5	2	4	686	492	2.03

UMC180	Bias voltage = 0.9 V					
Device name	Length (um)	Width (um)	number of devices in series	R_series : Re (Zin) in ohms	gds (in uS)	1/gds (in kohm)
N18_MM	2	2	1	0.5	154	6.49
N18_MM	1	2	2	419	290	3.45
N18_MM	0.5	2	4	573	527	1.89

TSMC180	Bias voltage = 1.8 V					
Device name	Length (um)	Width (um)	number of devices in series	R_series : Re (Zin) in ohms	gds (in uS)	1/gds (in kohm)
nmos2v_mac	2	2	1	24	329	3.04
nmos2v_mac	1	2	2	223	657	1.52
nmos2v_mac	0.5	2	4	274	1373	0.73

UMC180	Bias voltage = 1.8 V					
Device name	Length (um)	Width (um)	number of devices in series	R_series : Re (Zin) in ohms	gds (in uS)	1/gds (in kohms)
N18_MM	2	2	1	0.5	361	2.77
N18_MM	1	2	2	173	709	1.41
N18_MM	0.5	2	4	221	1379	0.72

At low frequencies, the looking in resistance and capacitance of a distributed RC line contacted at both ends will converge to R/12 and C, respectively as N increases.

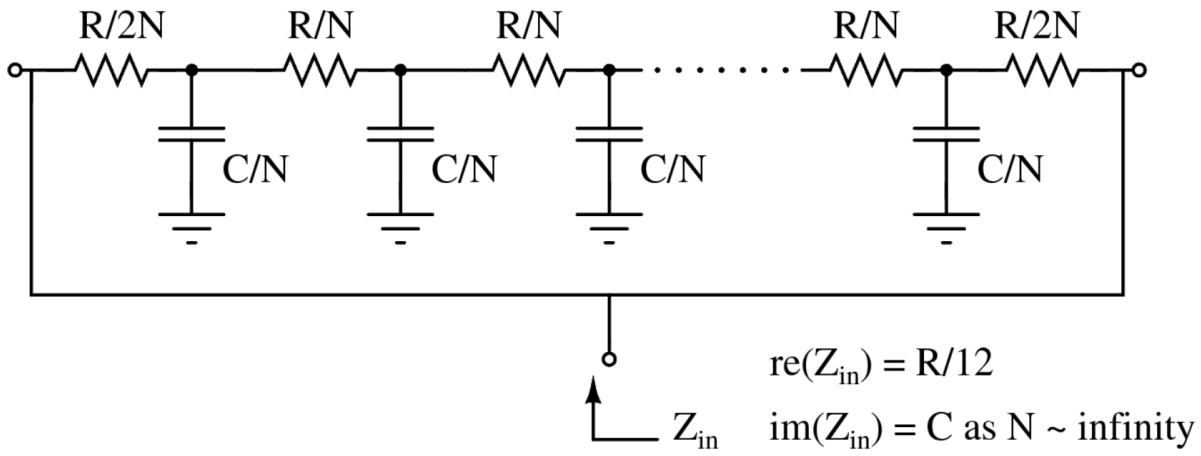

Fig. 5.2 Distributed RC line contacted on both ends.

From table 5.2 the single device has gds = 128 uS, the looking in resistance should be 1/(12*gds) = 651 ohms, which is close to the series resistance value of 0.5 um length fingers. The bottom line is that the series resistance is much larger when distributed nature is accounted for. This can make bypass capacitors ineffective.

Running a schematic transient simulation with bypass capacitor's transistor fingers in series showed no effect on performance. SNR remained at 25.55 dB. In addition, when an ideal resistance of 500 ohms is put in series with bypass capacitors with fingers in parallel, also had no effect on SNR.

CHAPTER 6

RC EXTRACTION:

In TSMC180, RCCC extraction was performed on the DRC and LVS clean layout of the flash ADC. The SNR dropped from 25 dB to 18.6 dB after a transient simulation on the RCCC extracted schematic. Upon further analysis, individually extracting parasitics block by block reference_voltage_generator block alone degraded SNR by ~4 dB.

Table 6.1 SNR with RC extracted blocks

RCCC extraction block:	SNR at 0.675V input amplitude
None	25 dB
Total flash ADC	18.6 dB
Comparator_array block alone	25.18 dB
Reference_voltage_generator alone	19.82 dB
Clock_generator block alone	25.04 dB
Clock_division_and_reset block alone	24.99 dB
Bias_generator block alone	24.46 dB
All blocks except the reference_voltage_generator block	24.01 dB

Various ways of debugging the reference_voltage_generator block:

6.1 Comparison with RCCC extracted layout values in UMC180:

Table 6.2 SNR of RCCC extracted schematic in UMC180

RCCC extraction:	SNR at 0.675V input amplitude
None	24.29 dB
Total flash ADC	24.81 dB
reference_voltage_generator block alone	24.27 dB

The schematic value is matching with RCCC extracted in UMC180. Hence, the degradation could have occurred as a result of changes made to the TSMC180 layout after streaming.

6.2 Tweaking frequency to observe its effect on performance:

Table 6.3 SNR variation with input frequency

Change in input frequency in TSMC180 at 0.675 V input amplitude and fs= 800 MHz		
fin in MHz	SNR Of schematic alone	After RCCC extraction
4.6875	24 dB	18.4 dB
7.8125	25 dB	18.6 dB
10.9375	24 dB	18.8 dB
14.0625	23 dB	19 dB

From Table 6.3, when frequency is tweaked around 7.8125 MHz, there is not much effect on the performance of flash ADC.

6.3 Dummy devices and bulk voltages:

The layout's dummy devices are checked for any violations, but none are discovered. PMOS devices have Vgs >= 0 V with bulk voltage 1.8 V (supply voltage) and similarly, NMOS devices have Vgs <=0 V with bulk voltage 0 V (ground).

6.4 No parasitic, parasitic Resistance alone, and parasitic capacitance alone extraction results:

Table 6.4 Comparison of No parasitic and parasitic extractions

Extraction of reference_voltage_generator block alone	SNR at 0.675 V input amplitude
No RC	19.8 dB
R extraction	19.8 dB
C+CC extraction	19.9 dB
RCCC extraction	19.8 dB

It's worth noting that the results with no parasitics are also poor. Hence, the parasitics are not to blame for the degradation.

6.5 Nwell proximity issue:

When Nwell drawings are close together in a layout, they have the ability to alter the MOSFET's threshold voltage, causing the device to deviate from its original purpose. This is due to the fact that the nwells are not perfectly cuboid but instead curve at corners within the substrate. So nearby Nwell's in the reference_voltage_generator block's layout are surrounded by larger nwells with just enough dimension to solve this problem.

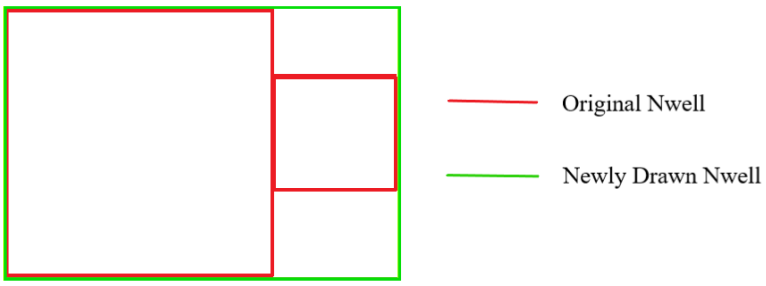

Fig. 6.1 Sample diagram depicting Nwell Drawings.

The results improved significantly as a result of this change, and the RCCC extracted results match the schematic. Final schematic and layout are present in the library ygpflash_adc.

Table 6.5 Comparison of SNR for schematic and RCCC extracted schematic

Flash ADC simulation	SNR at 0.675 V input amplitude	SNR at 0.7025 V input amplitude
Schematic alone	25 dB	25.55 dB
Total RCCC extraction	24.88 dB	24.99 dB

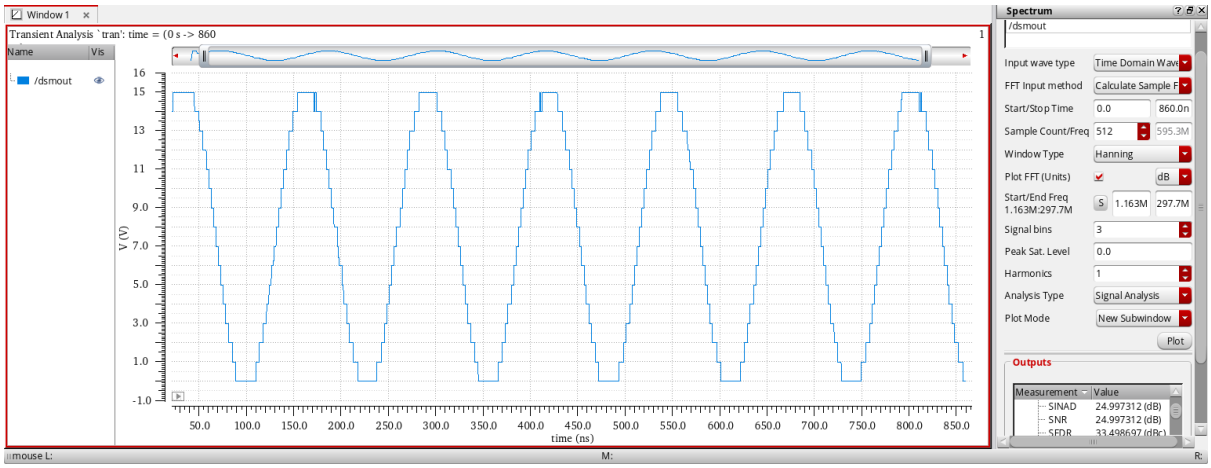

Fig. 6.2 SNR from the simulation of RCCC extracted TSMC180 schematic at 0.7025V input amplitude.

CONCLUSION:

A 4-bit flash ADC has been designed in TSMC180nm process from a similar existing design in UMC180nm. It is achieved by porting between the PDKs, using the two scripts 'Remaster_Instances_v7.il' which updates the devices in schematic and 'LayerUpdateDevices_v4.il' which updates the layers in the layout. Then modifications were made to the schematic and layout as discussed above to meet the performance specifications.

There are a few things which can be improved in this design:

- From table 3.3, there is slight deviation in common mode reference voltages between UMC180 and TSMC180. Node voltages of the reference_voltage_generator block can be compared between the 2 PDKs to check as to why this is happening.
- From Fig. 6.2, there are few glitches in the dsmout plot on the 14^{th} level.

REFERENCES:

1) G. Satyanarayana, 'Remasterinstances_v7.il' to update devices and 'LayerUpdateDevices_v4.il' to update layers from UMC180 to TSMC180.

THE END