# Auto-Reconfigurable Low Drop-Out Regulator Supporting Zero to Infinite Output Capacitance

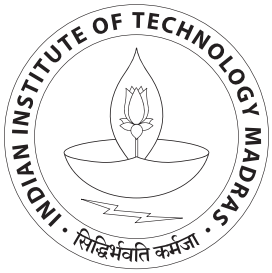
*A Project Report*

*submitted by*

**K J R K VARA PRASAD**

*in partial fulfilment of the requirements*
*for the award of the degree of*

**BACHELOR OF TECHNOLOGY**




**DEPARTMENT OF ELECTRICAL ENGINEERING**
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# THESIS CERTIFICATE

This is to certify that the thesis entitled **Auto-Reconfigurable Low Drop-Out Regulator Supporting Zero to Infinite Output Capacitance**, submitted by **K J R K Vara Prasad** (**EE18B055**), to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelors of Technology** and **Master of Technology**, is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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# ABSTRACT

**KEYWORDS**: Low Drop Out regulator, Phase margin, Gate pole, Output pole, Miller compensation, Feed forward compensation

This project implements an Auto-Reconfigurable Low Drop-Out Regulator Supporting Zero to Infinite Output Capacitance, with a maximum load up to 10 mA. The output capacitance range is determined by injecting a constant DC current into the output node and measuring the time for the voltage to rise upto a fixed $\Delta V$ using a D flip flop based counter. Depending upon the output capacitance range, the LDO is stabilized using miller compensation or feed forward compensation or neither. The LDO implemented in this project regulates an input voltage of 1.8V to output voltage of 1.5V with a maximum load current of 10mA.

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# ABBREVIATIONS

| | |
|---|---|
| **LDO** | Low Drop out regulator |
| **PMIC** | Power Management Integrated Circuits |
| **PSRR** | Power Supply Rejection Ratio |
| **UGB** | Unity Gain Bandwidth |
| **PM** | Phase margin |
| **LHP** | Left half plane |
| **RHP** | Right half plane |

# NOTATION

| | |
|---|---|
| $V_{ref}$ | Reference voltage for error correction |
| $g_m$ | Transconductance of error amplifier |
| $g_{m_p}$ | Small signal transconductance of PMOS |
| $R_{ds}$ | Small signal drain to source resistance of PMOS |
| $V_{out}$ | Output Voltage of the LDO |
| $V_{in}$ | Input Voltage of the LDO |
| $\beta$ | Feedback factor |

# CHAPTER 1

# INTRODUCTION

The number of ICs on a single circuit board is continuously expanding due to advancements in the semiconductor industry, and all of these ICs require a steady and regulated DC according to their stated voltage and power. This creates room for a lot of DC – DC voltage regulators on the chip. These voltage regulators keep the voltages from a power supply within a range that is compatible with the other electrical components so that their performance is not disturbed.

There are two types of voltage regulators namely Switching regulators and Linear regulators. Today's portable and handheld gadgets are powered by a Power Management IC (PMIC) which contains multiple switching and linear regulators on a single chip. Switching regulators are efficient at a larger voltage drop and are expensive and noisy. Linear regulators are efficient at a low voltage drop and these are cheaper with small size and lesser noise compared to switching regulators.

This report starts with the basic introduction to Low drop out(LDO) regulators. Pushing to general types of LDOs, their applications and control techniques. Then goes to discusses about the stability of LDO and types of compensation and the Limitations with supporting wide range of output capacitance. Then it goes to discuss about the new proposed Auto Reconfigurable LDO , how it works and supports any output capacitance. This is followed by the advantages of this new architecture and then simulation results.

# CHAPTER 2

# BACKGROUND

## 2.1 Introduction to Low Drop out regulators

A low-dropout regulator (LDO regulator) is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage. Since LDOs are step-down converters, the output voltage is always less than the input voltage. However, these regulators offer a few advantages: they are often easy to design, dependable, and cost-effective, with low noise and very low output voltage ripple. LDOs provide a relatively clean output compared to switching regulator, having better line and load transients.

### Applications of LDO:

**1. Regular power supply:**

LDOs are efficient at low voltage drops. These can be used as a regular power supply for higher loads when the voltage drop is low and for lighter loads when the voltage drop is high.

**2. Sub regulators:**

Due to the low noise and less output ripple, LDOs are connected in series with a switching regulator in order to suppress the ripple. The LDO will filter the ripple and provide a cleaner output.

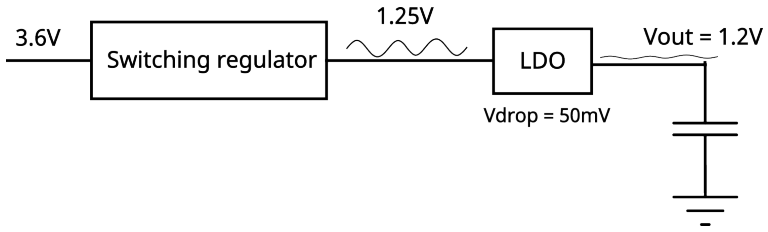



Figure 2.1: LDO used as sub regulator in series with switching regulator

**3. Parallel or auxiliary current source**

LDO is often connected in parallel with the switching regulator in order to achieve faster transient response. During the transient, all the fast current requirement will be met by the LDO because of its high bandwidth, hence acting like an auxiliary current source, and when output is met, all the load current will be supplied by switching regulator.

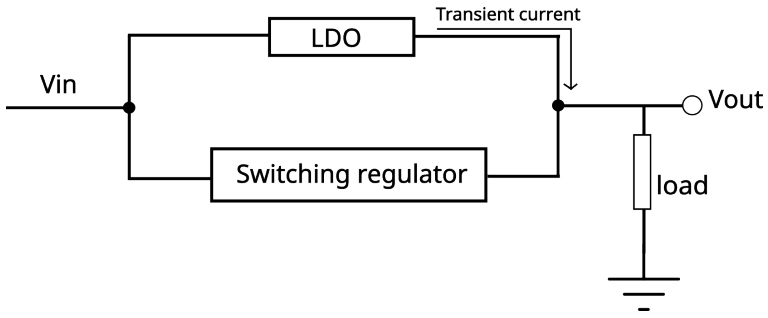



Figure 2.2: LDO used as an auxiliary current source

## 2.2 Types of LDO

LDOs are classified into Analog LDO and Digital LDO based on their control feedback. In Analog LDOs, the current through the pass element is controlled by varying the gate voltage of the pass transistor with an error amplifier. While the digital counterpart is controlled by quantizing the current by the number of pass transistors which act as switches turning ON and OFF, the number of pass

transistors ON at a particular instant decides the amount of current that passes through the pass element. This is achieved with a digital controller and a switch array.

Digital LDOs are smaller in area compared to Analog LDOs and they also have a relatively low quiescent current. Digital LDOs are much better when it comes to process scalability and have relatively less stability issues. But they have poor PSRR as their pass transistors operate in deep triode region.The Digital LDO also has a slow transient response. It slowly controls the output voltage (Vout) with a coarse digital voltage step. In contrast, the analog LDO quickly controls Vout with a fine analog voltage control and also has a good PSRR. Hence the Analog LDO is preferred when the circuits designed are to be precise and very sensitive. We'll be focusing on Analog LDOs in this report.

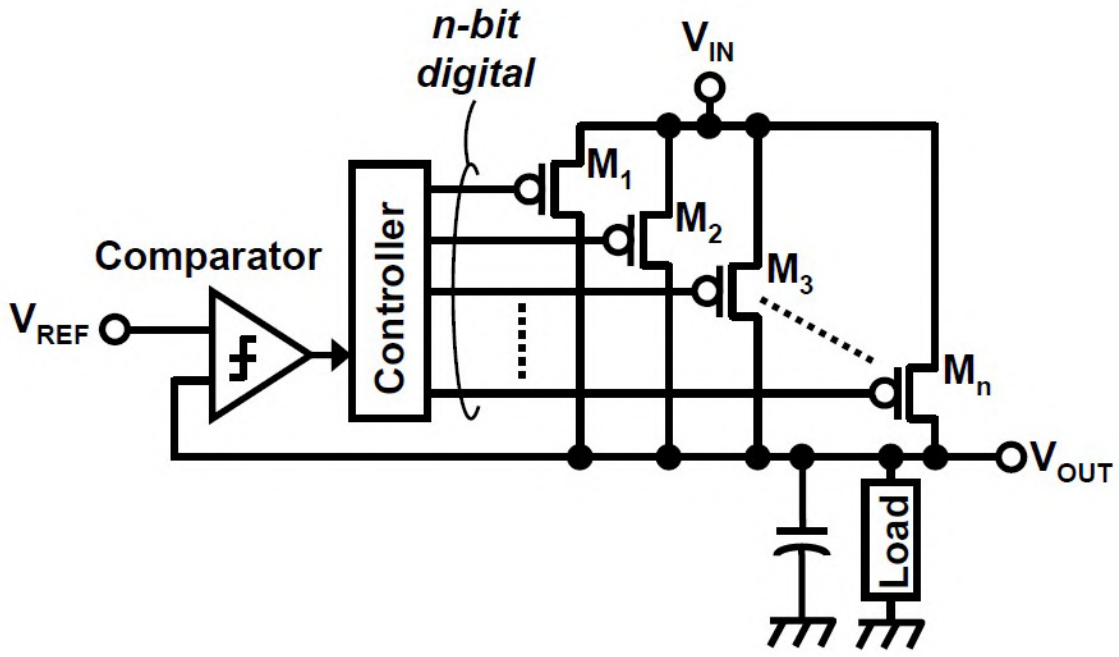



Figure 2.3: Digital LDO

## 2.3 Structure of Analog LDO

The design of an analog LDO consists of a voltage reference, an error amplifier, a pass element and a feedback voltage divider. The pass element can be either a bipolar transistor or a MOSFET. The general difference between these is how the pass element is driven. A bipolar pass element is a current-driven device, whereas the MOSFET is a voltage driven device. In modern days, MOSFETs are generally used as pass elements in an LDO.

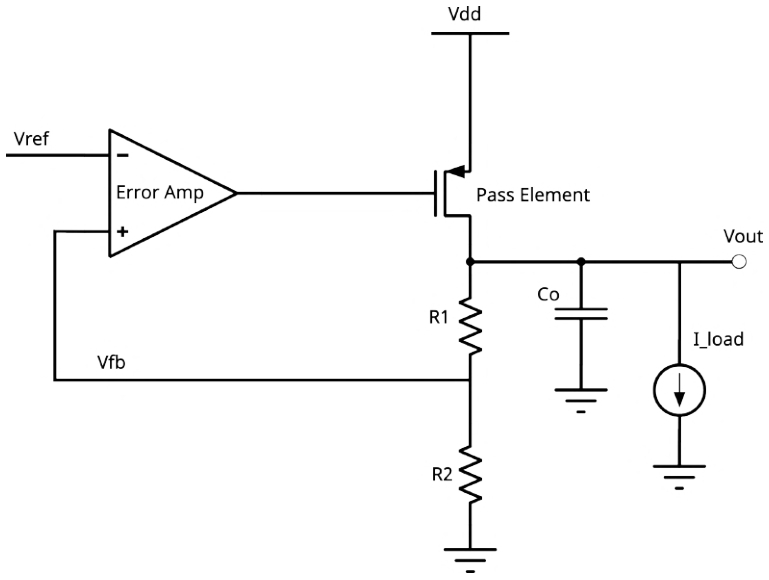



Figure 2.4: PMOS LDO

Consider the above figure 2.4.The error amplifier controls the gate voltage of the PMOS transistor, that is used as the pass element. This in turn controls the current flowing through the PMOS transistor. The amplifier compares the scaled output voltage(feedback) and its voltage reference to control the gate voltage of the pass element. If the feedback is higher than the voltage reference, the amplifier increases the gate voltage of the pass element, making the $V_{gs}$ of PMOS smaller. This reduces the current through PMOS, and helps in bringing the output voltage down. Similarly, if the feedback is lower than the voltage reference, it increases

the $V_{gs}$ in turn increases the current through the PMOS. This makes the output voltage, Vout, to lower down to the desired value, given by the equation 2.1

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref} \tag{2.1}$$

### 2.3.1 Pass Element

The pass element can either be a PMOS or an NMOS transistor. Both have their own advantages and disadvantages. The PMOS pass transistors can degrade the Power Supply Rejection Ratio (PSRR) of the LDO at higher frequencies[1]. An NMOS transistor can also be used as a pass transistor with its drain as the power supply and output at its source as shown in the fig 2.5

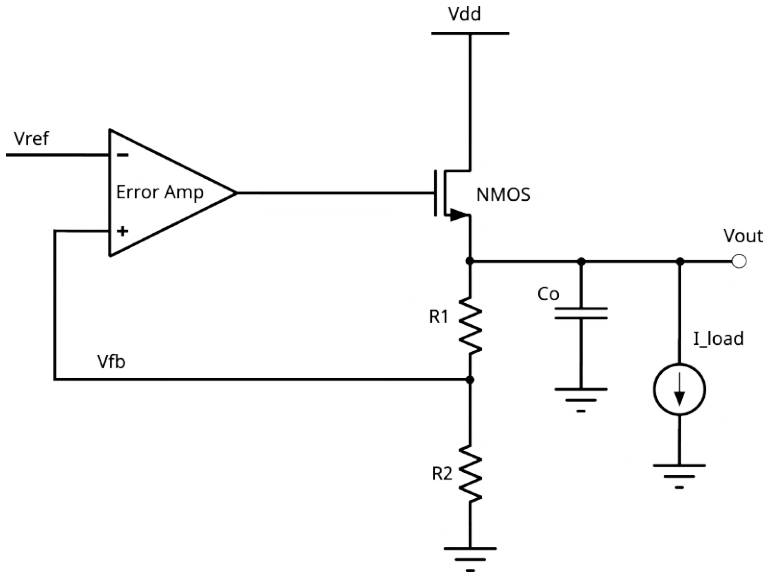



Figure 2.5: NMOS LDO

NMOS LDO has an intrinsic local feedback as its source is connected to output. This would have an improved load regulation and also a better power supply rejection (PSRR). The compensation complexity required for an NMOS pass element is relatively less. Also for the same load current and dropout voltage spec,

PMOS LDO will be relatively larger than an NMOS LDO due to lower mobility of holes ($\mu_n \simeq 2 * \mu_p$). But the downside to using an NMOS pass element is that the maximum output voltage that it can support is limited to $V_{DD} - V_{TH}$. The voltage dropout can be very small when a PMOS pass element is used. In this project, we used PMOS LDO because the voltage dropout is very low and no charge pump is used to maintain the large voltage headroom.

## 2.4 Small signal Analysis

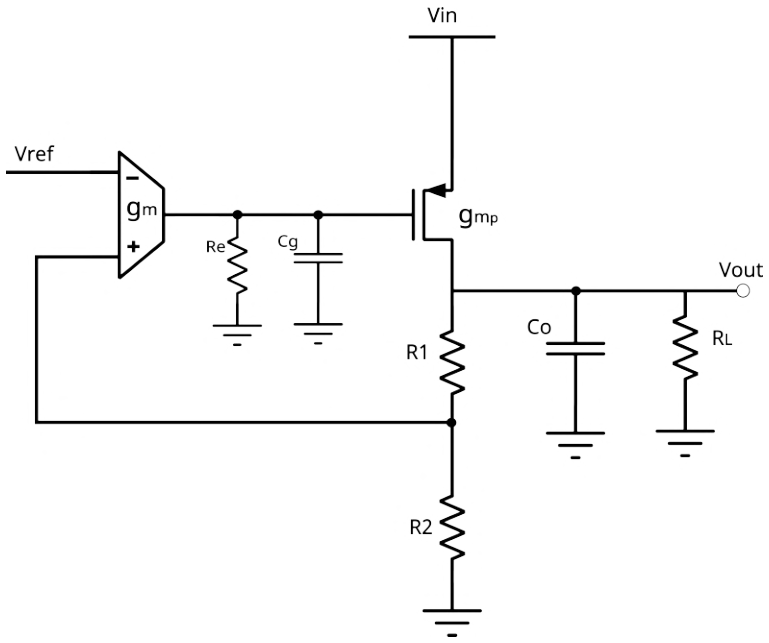



Figure 2.6: small signal PMOS LDO

The above is the small signal equivalent circuit of the PMOS LDO The frequency response of the above LDO is given by:

$$LG(s) = \frac{\beta A_1 A_2}{(1 + sR_e C_g)(1 + sR_o C_o)} \tag{2.2}$$

Where,

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$A_1 = g_m R_e$$

$$A_2 = g_{m_p} R_o$$

$$R_o = \frac{R_L((R_1 + R_2)||R_{ds})}{R_L + (R_1 + R_2)||R_{ds})}$$

The poles of this frequency response are

$W_{pgate} = \frac{1}{R_e C_g}$ – Gate pole or Error Amplifier pole

$W_{pout} = \frac{1}{R_o C_o}$ – Output pole.

## 2.5 Stability of LDO and need of compensation

LDO is a closed loop system. The phase margin of the open loop frequency response defines the stability of the LDO. It is given by the equation:

$$\text{PhaseMargin} = 180° - \tan^{-1}\left(\frac{W_{ugb}}{W_{pgate}}\right) - \tan^{-1}\left(\frac{W_{ugb}}{W_{pout}}\right)$$

Where, $W_{ugb}$ is the unity gain frequency of the system. For a better stability in the closed loop, the phase margin of the loop is preferred to be more than 60 degrees. The LDO in this project is designed for $V_{in}$ = 1.8$V$ and $V_{out}$ = 1.5V with load current $I_L$ varying from 0 to 10mA. The CMOS technology used is TSMC 180 nm. Below are the other parameters of the LDO:

$V_{ref}$ = 0.6 $V$ $\implies$ $\beta = \frac{V_{out}}{V_{ref}} = \frac{1.5}{0.6} = 2.5$

$R_2$ = 100 K $\implies$ $R1$ = 150 K ($\because \beta = 2.5$)

$g_m = 4.59\ \mu A/V,\ Re \simeq 25.5\ M\Omega, C_g \simeq 1.23\ pF$

for PMOS - $L$ = 180nm, $W = 565\ \mu m$

The width of the PMOS is chosen in a way such that it stays in saturation region for the entire load range of 0 to 10mA. The $R_L$ varies from 150 Ω to ∞ and $C_o$ varies from 0 to ∞. Below is the table showing the phase margin for various values of $C_o$ and $I_L$:

Table 2.1: Phase Margin of LDO for various $C_o$ and $I_L$

| $C_o$ | $I_L$ | DC gain | Gate pole | Out pole | Phase margin |
|---|---|---|---|---|---|
| 10 pF | 0 mA | 66 dB | 1.36 K | 1.032 M | 14.8° |
| 10 pF | 1 mA | 63.5 dB | 1.61K | 103 M | 60.8° |
| 10 pF | 10 mA | 56 dB | 2.8 K | 462 M | 68.7° |
| 100 pF | 0 mA | 66 dB | 1.26K | 118K | 5.64° |
| 100 pF | 1 mA | 63.5 dB | 1.61K | 11.1 M | 50.73° |
| 100 pF | 10 mA | 56 dB | 2.8K | 49 M | 66.9° |
| 1nF | 0 mA | 66 dB | 712 | 21K | 4.93° |
| 1nF | 1 mA | 63.5 dB | 1.6K | 1.1 M | 19.5° |
| 1nF | 10 mA | 56 dB | 2.8 K | 4.95 M | 51.9° |

From 2.1, For various ranges of output capacitance and load, the Phase margin of the system goes below 60° i.e., the system is unstable, . Having the second pole of the system inside the unity gain bandwidth (Unity gain bandwidth) results in poor phase margin. This highlights the need of a proper compensation technique to improve the phase margin and stabilize the LDO. The next chapter discusses about various compensation techniques which can improve the stability of the system.

# CHAPTER 3

# Compensation Techniques of LDO and Challenges

## 3.1 Dominant pole compensation

Dominant pole compensation is one of the simplest compensation techniques, which can be implemented by making the dominant pole more dominant by increasing the capacitance at that node. This lowers the dominant pole which in turn reduces the UGB of the system there by effectively pushing out the non dominant pole out of UGB and increasing the phase margin.

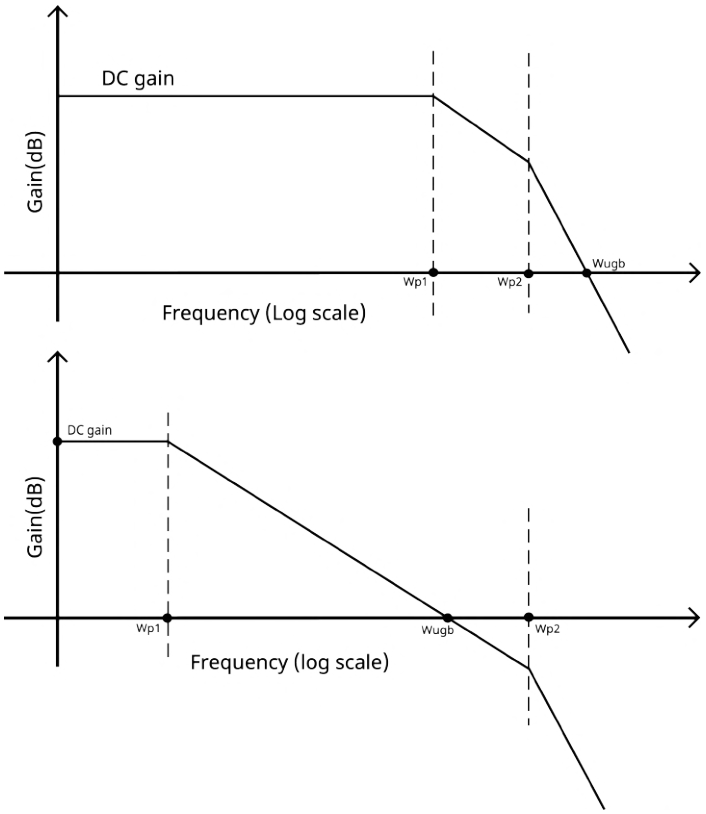



Figure 3.1: Before and after dominant pole compensation

## 3.2 Stability with error amp vs output pole dominant

For the LDO we designed, the capacitance can be inserted either at the gate of the PMOS or at the output of the LDO depending on which pole is dominant.

### Case 1 : Error Amplifier pole is dominant

In this case, to further improve the phase margin, we need to insert the capacitance Cc at the input of the PMOS gate (error amplifier output). The new poles will be :

$$W_{p1_{new}} = \frac{1}{R_e(C_g + C_c)}$$

$$W_{p2} = \frac{1}{R_o C_o}$$

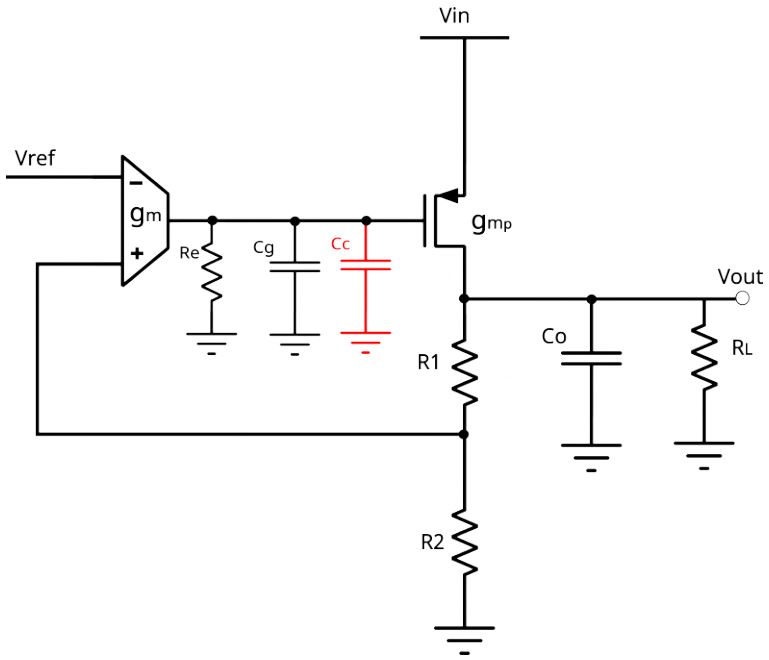



Figure 3.2: Gate pole Dominant PMOS LDO

Clearly, this won't support upto infinite capacitance as $C_o$ goes from 0 to $\infty$, $W_{p2}$ can go as low as 0 and there will be a region where it can come inside $W_{ugb}$ which makes the system unstable. Let's consider a maximum output capacitance of 1nF for our LDO. The phase margin will be worst when the output load is infinity and out put capacitance is maximum. The $R_o$ then will be $(R_1 + R_2||R_{ds})$. For phase margin greater than 60°:

$$\begin{aligned} W_{p2} &\geq \sqrt{3} W_{ugb} \\ \frac{1}{R_o C_o} &\geq \sqrt{3} A_1 A_2 \cdot \frac{1}{R_e (C_c + C_g)} \\ C_c + C_g &\geq \frac{\sqrt{3} A_1 A_2 \cdot R_o C_o}{R_e} \end{aligned}$$

The approximate minimum capacitance value we get by substituting our LDO parameters is $C_c \simeq 15.27$ nF. Below is the table after dominant pole compensation.

Table 3.1: PM of LDO for various $C_o$ and $I_L$ after dominant pole compensation

| $C_o$ | $I_L$ | DC gain | Gate pole | Out pole | Phase margin |
|---|---|---|---|---|---|
| 10 pF | 0 mA | 66 dB | 0.42 | 128 K | 89.58° |
| 10 pF | 1 mA | 63.5 dB | 0.41 | 19.4 M | 90° |
| 10 pF | 10 mA | 56 dB | 0.41 | 190 M | 90° |
| 100 pF | 0 mA | 66 dB | 0.43 | 13.6 K | 86.16° |
| 100 pF | 1 mA | 63.5 dB | 0.41 | 2 M | 90° |
| 100 pF | 10 mA | 56 dB | 0.41 | 20 M | 90° |
| 1nF | 0 mA | 66 dB | 0.45 | 1.37 K | 60.02° |
| 1nF | 1 mA | 63.5 dB | 0.42 | 209 K | 89.8° |
| 1nF | 10 mA | 56 dB | 0.41 | 2 M | 90° |

If 15.27 nF capacitance is used for the dominant pole compensation, then the system is stable for an output capacitance of 1 nF . Having a 15nF capacitor ON CHIP is very difficult because it'd occupy a huge area. Besides this type of com-

pensation supports only till 1nF. Let's look into the case where output pole is dominant.

## Case 2 : Output pole is dominant

In this case, to further improve the phase margin, we need to insert the capacitance Cc at the output of the LDO. The new poles will be :

$$W_{p1} = \frac{1}{R_e C_g}$$

$$W_{p2_{new}} = \frac{1}{R_o(C_o + C_c)}$$

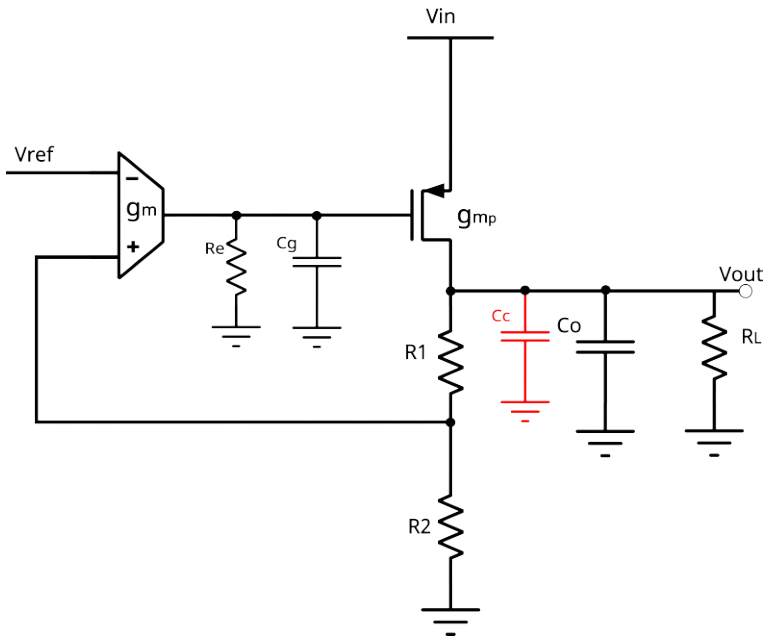



Figure 3.3: Output pole Dominant PMOS LDO

$C_g$ and $R_e$ of an LDO are dependent on the gate capacitance of the PMOS and output resistance of the error amplifier. Hence they are fixed for a particular LDO design. The phase margin will be worst when the output load is minimum . The

$R_o$ then will be $\simeq R_L$. For phase margin greater than 60°:

$$\begin{aligned} W_{p2} &\geq \sqrt{3} W_{ugb} \\ \frac{1}{R_e C_g} &\geq \sqrt{3} A_1 A_2 \cdot \frac{1}{R_o (C_c + C_o)} \\ C_c + C_o &\geq \frac{\sqrt{3} A_1 A_2 \cdot R_e C_g}{R_o} \end{aligned}$$

The approximate minimum capacitance value we get by substituting our LDO parameters is $C_c \simeq 273.38 \mu F$. This capacitance can be OFF chip also, but having such big capacitance just to stabilize the LDO is the downside of this type of compensation, Otherwise this LDO is stable for all ranges of capacitance and load unless there is a change in gate cap and error amplifier resistance due to process variations. But using dominant pole compensation will lower the UGB of the system.

## 3.3 Miller compensation

Miller compensation is a technique for stabilizing op-amps by means of a capacitance connected in negative-feedback across the second stage. Miller compensation exploits the Miller effect to simulate a large capacitance using a physically small capacitor Cc that can easily be fabricated on chip without wasting precious area. Due to miller effect, pole splitting happens and this lowers the gate pole and pushes out the output pole farther. This also introduces a right half plane zero to the frequency response (which needs to be taken care properly). Equation 3.1 is the frequency response after inserting a miller capacitance [2]:

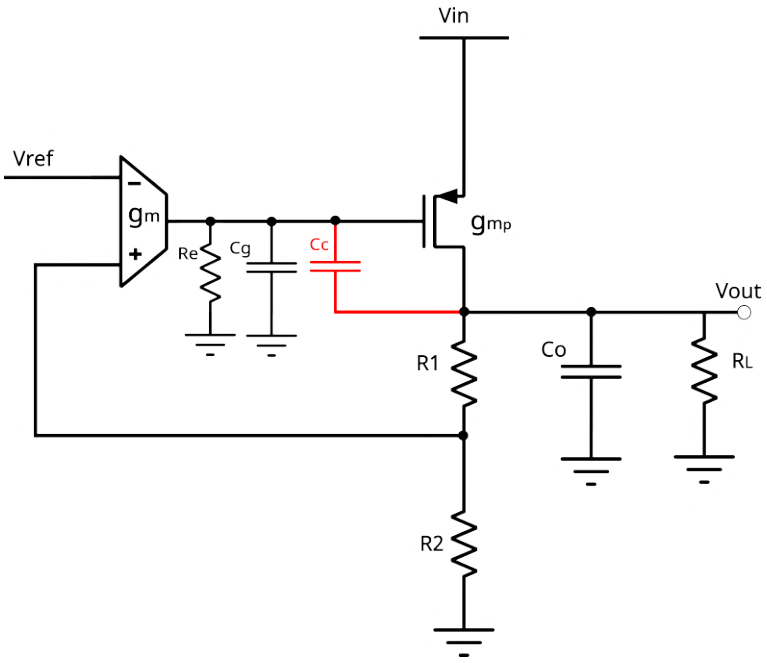



Figure 3.4: Miller compensation of PMOS LDO

$$LG(s) = \frac{\beta A_1 A_2 (1 - \frac{s}{W_z})}{(1 + \frac{s}{W_{pgate_m}})(1 + \frac{s}{W_{pout_m}})} \tag{3.1}$$

Where, ($\beta A_1, A_2$ are same as before )

$$z = \frac{g_{m_p}}{C_c}$$

$$W_{pgate_m} \simeq \frac{1}{R_o g_{m_p} R_e Cc} = \frac{W_{pgate}}{R_o g_{m_p}} \qquad < \left(W_{pgate}\right)$$

$$W_{pout_m} = \frac{g_{m_p}}{C_o + \frac{C_g C_c}{C_g + C_c}} \simeq \frac{g_{m_p}}{C_o + C_g} \qquad > \left(W_{pout}\right)$$

$W_{pgate_m}$ and $W_{pout_m}$ are the new poles after miller compensation where $W_{pgate}$ and $W_{pout}$ are poles without miller compensation. From the above equations, one can say that the new poles after miller compensation are now far apart compared to previous one (3.5). Similar to dominant pole compensation, the UGB of the system reduces when miller compensation is implemented.

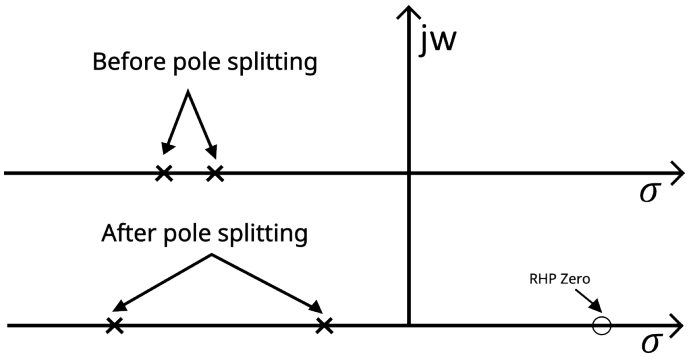



Figure 3.5: location of poles and zeros before and after miller compensation

Assuming $W_{pgate_m} << W_{pout_m}$, $W_{ugb} = \frac{g_m}{C_c}$. The new phase margin is given as below:

$$\text{PhaseMargin} = 180^\circ - \tan^{-1}\left(\frac{W_{ugb}}{W_{pgate_m}}\right) - \tan^{-1}\left(\frac{W_{ugb}}{W_{pout_m}}\right) - \tan^{-1}\left(\frac{W_{ugb}}{W_z}\right)$$

As we can see, the RHP zero has negative effect on the phase margin. However, If we choose $gm_p >> gm$, then the phase lag contributed by the RHP zero i.e., $\tan^{-1}\left(\frac{W_{ugb}}{W_z}\right)$ will have minimal effect on the overall phase margin. Neglecting the effect of zero, For phase margin to be greater than 60°:

$$\begin{aligned} W_{p2} &\geq \sqrt{3} W_{ugb} \\ \frac{g_{m_p}}{C_o + C_g} &\geq \sqrt{3} A_1 A_2 \cdot \frac{1}{g_{m_p} R_o R_e C_c} \\ C_c &\geq \frac{\sqrt{3} A_1 A_2 \cdot (C_o + C_g)}{g_{m_p}^2 R_o R_e} \end{aligned}$$

Miller compensation tries to make gate pole more dominant and push the output pole farther. This improves the phase margin in case where gate pole is dominant without compensation. If output pole is dominant, using miller compensation may further reduce the phase margin. Hence miller compensation won't work till infinite output capacitance for a limited $C_c$. Let's implement miller

compensation for 2.1 taking maximum output cap of 1nF. The phase margin will be worst when the output load is infinity and out put capacitance is maximum. The $R_o$ then will be $(R_1 + R_2||R_{ds})$. Calculating the values from above equation, $C_c \geq (41.03)$ pF .

Table 3.2: PM of LDO for various $C_o$ and $I_L$ after miller compensation

| $C_o$ | $I_L$ | DC gain | Gate pole | Out pole | Phase margin |
|---|---|---|---|---|---|
| 10 pF | 0 mA | 66 dB | 9.2 | 2.39 M | 87.73° |
| 10 pF | 1 mA | 63.5 dB | 11.1 | 253 M | 89.8° |
| 10 pF | 10 mA | 56 dB | 24.6 | 1.14 G | 89.9° |
| 100 pF | 0 mA | 66 dB | 9.2 | 245 K | 84.30° |
| 100 pF | 1 mA | 63.5 dB | 11.1 | 27.5 M | 89.76° |
| 100 pF | 10 mA | 56 dB | 24.6 | 119 M | 89.88° |
| 1nF | 0 mA | 66 dB | 9.17 | 26.3 K | 58.55° |
| 1nF | 1 mA | 63.5 dB | 11.1 | 2.79M | 89.45° |
| 1nF | 10 mA | 56 dB | 24.6 | 12 M | 89.81° |

By adding a small capacitance, we are achieving a good stability improvement. This is a good replacement for dominant pole compensation where we require very high on chip capacitance ($\simeq$ 15nF) to make the gate pole dominant. From the table, For 0 mA load and 1nF, We can see that there is a slight deviation from what we calculated. This is because of the negative effect of the RHP zero on the phase margin. Since $gm_p$ decreases with decrease in load current, we can't completely ignore the effect of RHP zero.

## 3.4 RHP plane zero and Series Resistance

The Right half plane zero adds phase lag to the system while increasing the loop gain. This will reduce the phase margin. We should negate the effect of RHP

zero inorder to achieve better phase margin. There are many ways to do it, one such method is adding a series resistance ($R_z$) to the miller capacitance.

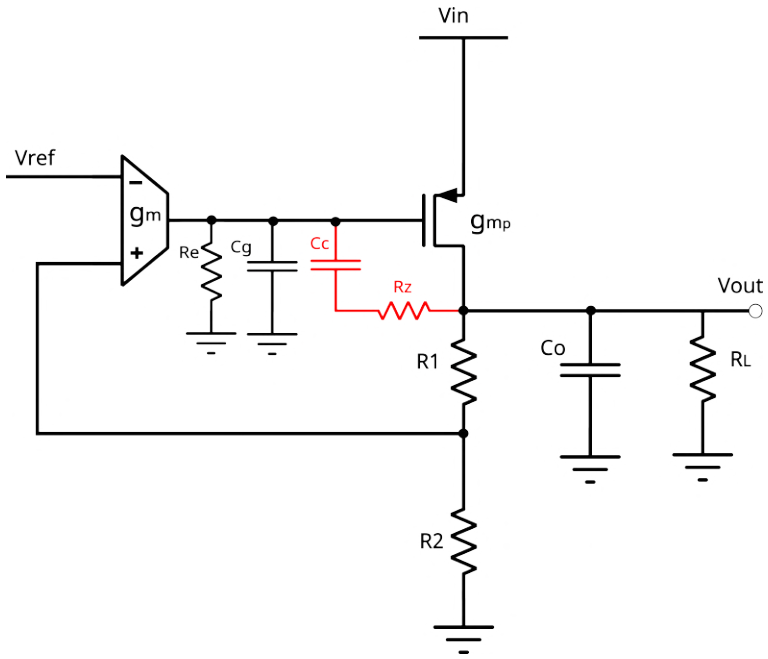



Figure 3.6: Resistance in series with miller cap to negate RHP zero

Adding series resistance to the feedback miller path will increase the impedance of the path there by weakening the effect of forward feedback from error amplifier to output. By adding a series resistance, the poles will be split and the new gate pole and output pole will be almost same as that of without a series resistance. But there will be a change in the RHP zero and also a new third pole will be added to the frequency response which will be far outside UGB. The new zero will be:

$$z_{new} = \frac{1}{\left(R_z - \frac{1}{g_{m_p}}\right)C_c}$$

The series resistance is chosen such that $R_z \simeq \frac{1}{g_{m_p}}$, so the RHP zero can now be pushed to $\infty$ making its effect minimal. If we choose $R_z > \frac{1}{g_{m_p}}$, the zero now becomes a left half plane zero which helps in improving the phase margin. In our

LDO design, choosing a series resistance of 8.26K Ω will cancel out the effect of RHP zero. Any series resistance above it will only help in improving the phase margin further, but we should be cautious of the new third pole that is introduced due to the series resistance which might come in to UGB if we increase $R_z$. The new LHP zero can also be used to cancel out the non dominant pole, but since we have a wide range of load current and capacitance, it might not be much useful in our design.

We can also reduce the miller capacitance if we use a series resistance. The phase lead by LHP zero will improve the phase margin of the system due to which we can relax the miller capacitance value. Below is the comparison of phase margin of the LDO for [PM1] ($C_c$ = 41.03pF , $R_z$ = 8.26K) and [PM2] ($C_c$ = 20pF , $R_z$ = 100K):

Table 3.3: PM of LDO after RHP zero compensation

| $C_o$ | $I_L$ | DC gain | PM (41pF, 8.3K) | PM2 (20pF,100K) |
|---|---|---|---|---|
| 10 pF | 0 mA | 66 dB | 90.30° | 107.65° |
| 10 pF | 1 mA | 63.5 dB | 92.14° | 113.15° |
| 10 pF | 10 mA | 56 dB | 92.32° | 113.19° |
| 100 pF | 0 mA | 66 dB | 86.87° | 105.05° |
| 100 pF | 1 mA | 63.5 dB | 92.13° | 108.25° |
| 100 pF | 10 mA | 56 dB | 92.29° | 111.05° |
| 1nF | 0 mA | 66 dB | 60.73° | 61.42° |
| 1nF | 1 mA | 63.5 dB | 92.07° | 107.37° |
| 1nF | 10 mA | 56 dB | 92.19° | 109.47° |

## 3.5 Feed forward compensation

Both dominant pole compensation and miller compensation techniques lower the gate pole and there by pushing the non dominant pole outside UGB which also results in lowering of UGB. The feed-forward compensation technique uses a transconductance block connected across the second stage as shown in the 3.7. This adds a new LHP zero and an LHP pole to the existing transfer function and feed forward compensation won't reduce the UGB of the system[3].

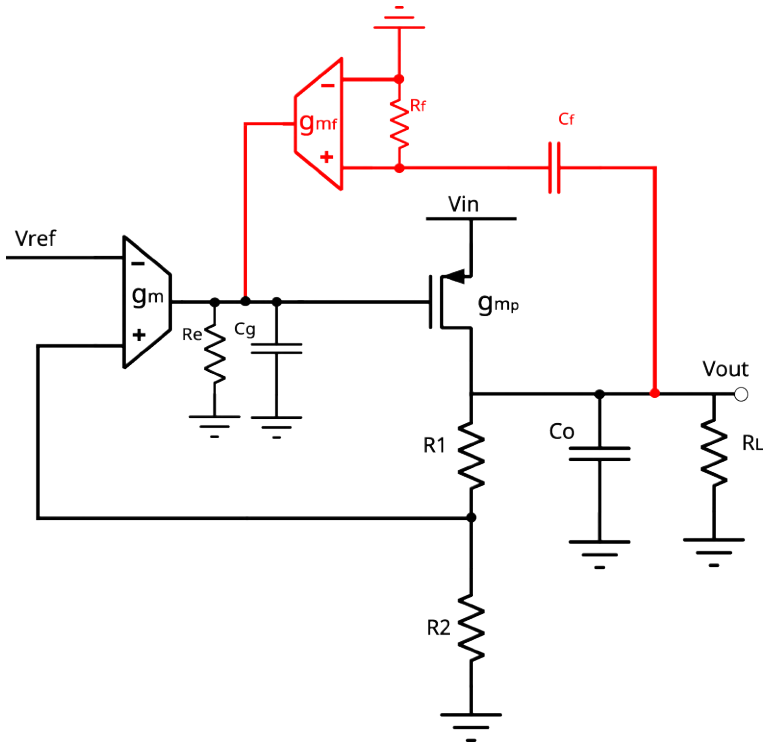



Figure 3.7: Feed forward compensated PMOS LDO

Below is the transfer function of the feed forward compensated LDO:

$$LG(s) = \frac{\beta g_m g_{m_p} R_e R_o \left(1 + \left(1 + \frac{g_{m_f}}{\beta g_m}\right) sC_f R_f\right)}{\left(1 + sC_g R_e\right)\left[\left(1 + sR_o C_o\right)\left(1 + sR_f C_f\right) + sC_f R_o\right]} \tag{3.2}$$

After approximations, below are the locations of poles and zero:

$$W_{pgate} = \frac{1}{R_e C_g}$$
$$W_{pout} = \frac{1}{R_o C_o}$$
$$W_{pff} = \frac{1}{R_f C_f}$$
$$W_Z = \frac{1}{\left(1 + \frac{g_{m_f}}{\beta g_m}\right) C_f R_f}$$

The newly formed LHP zero can be used to improve the phase margin. We can use this LHP pole to cancel any existing pole. In our LDO, We are going to fix the zero of this system such that it cancels out the gate pole (which doesn't change with load). Choose $R_f$, $C_f$ and $g_{m_f}$ of the feed forward block such that

$$R_e C_g \simeq \left(1 + \frac{g_{m_f}}{\beta g_m}\right) C_f R_f$$

The values of $R_f$, $C_f$ must be chosen in a way such that the non dominant pole won't come inside UGB of the frequency response. Typically it should be $R_f C_f >> R_o C_o$. Feed forward compensation is a very good technique to improve the phase margin of the system and it works for a very wide range of load capacitance and load currents, but it requires an additional transconductance block which in general has $g_{m_f} >> g_m$. This requires a lot of power and using feed forward compensation is a power inefficient method.

## 3.6 Limitations with supporting wide range of output capacitance

Let's look at the phase margin of the circuit for two extreme cases of load without any compensation for a wide range of capacitance :

**Case 1: Zero load current** $I_L \simeq 0 \implies R_L = \infty$

| Output Capacitance | Pole 1 | Pole 2 | Phase margin | Dominant pole |
|---|---|---|---|---|
| 10pF | 1.36 K | 1.032 M | 14.78° | Gate pole |
| 50pF | 1.31 K | 225 K | 6.56° | Gate pole |
| 100pF | 1.26 K | 118 K | 5.64° | Gate pole |
| 200pF | 1.16 K | 64K | 4.46° | Gate pole |
| 500pF | 943 K | 31K | 4.37° | Gate pole |
| 1nF | 712 | 21K | 4.93° | Output pole |
| 2nF | 510 | 15K | 6.01° | Output pole |
| 5nF | 230 | 12K | 8.59° | Output pole |
| 10nF | 123 | 11.9 K | 11.75° | Output pole |
| 20nF | 62 | 11.4 K | 16.41° | Output pole |
| 50nF | 18.2 | 11.2 K | 24.85° | Output pole |
| 100nF | 10.5 | 11 K | 34.92° | Output pole |
| 500nF | 3.5 | 10.9 K | 65.31° | Output pole |
| 1uF | 1.9 | 10.9K | 76.24° | Output pole |
| 2uF | 0.92 | 10.9K | 82.89° | Output pole |
| 5uF | 0.41 | 10.9K | 87.13° | Output pole |

Table 3.4: Phase margin of the LDO design for Zero load current

From tables 3.4 and 3.5, We observe that at very low output capacitance, the gate pole is dominant. As we keep on increasing the output capacitance, both poles will come closer and gradually the output pole will become dominant.

**Case 2: 10 mA load current** $R_L = 150\Omega$

| Output capacitance | Pole 1 | Pole 2 | Phase margin | Dominant pole |
|---|---|---|---|---|
| 10pF | 2.8 K | 462 M | 68.63° | Gate pole |
| 50pF | 2.8 K | 97 M | 67.85° | Gate pole |
| 100pF | 2.8 K | 49 M | 66.87° | Gate pole |
| 200pF | 2.8 K | 24.7 M | 64.95° | Gate pole |
| 500pF | 2.8 K | 9.8 M | 59.47° | Gate pole |
| 1nF | 2.8 K | 4.95 M | 51.60° | Gate pole |
| 2nF | 2.8 K | 2.47 M | 40.97° | Gate pole |
| 5nF | 2.8 K | 994K | 26.87° | Gate pole |
| 10nF | 2.8 K | 499 K | 19.07° | Gate pole |
| 20nF | 2.77 K | 251 K | 13.31° | Gate pole |
| 50nF | 2.71 K | 103 K | 9.08° | Gate pole |
| 100nF | 2.59 K | 54 K | 7.28° | Gate pole |
| 200nF | 2.39 K | 29 K | 5.95° | Gate pole |
| 500nF | 1.87 K | 15 K | 5.43° | Output pole |
| 1uF | 1.32 K | 10.6 K | 6.03° | Output pole |
| 2uF | 814 | 8.6 K | 7.21° | Output pole |
| 5uF | 370 | 7.55 K | 10.49° | Output pole |
| 10uF | 193 | 7.23K | 13.66° | Output pole |
| 50uF | 40 | 6.99K | 29.26° | Output pole |
| 100uF | 20 | 6.96K | 40.34° | Output pole |
| 200uF | 10 | 6.94 K | 53.82° | Output pole |
| 300uF | 6.72 | 6.94 K | 61.98° | Output pole |
| 500uF | 4 | 6.94K | 70.99° | Output pole |

Table 3.5: Phase margin of the LDO design for 10 mA load current

Based on the location of poles, we've classified them into four categories :

Cyan – Gate pole is strongly dominant, so no need of any compensation

Yellow – Gate pole > output pole. So, miller compensation is good enough

Red – Output pole > Gate pole. So needs a very good compensation

Green – No compensation because output pole dominant (strictly no miller).

The red and yellow regions are where we need to compensate our LDO. Below is the comparison of all compensation techniques we have discussed in this report:

| **Compensation** | **Advantages** | **Disadvantages** |
|---|---|---|
| Dominant pole Compensation (gate pole) | • Easy to implement<br>• Improves phase margin<br>• Works well within a given maximum output capacitance range | • Need large ON Chip capacitor<br>• Can't support up to infinite output capacitance<br>• Lowers the UGB |
| Dominant pole Compensation (Output pole) | • Easy to implement<br>• Improves phase margin<br>• Works well within a given maximum output capacitance range | • Need a very very large off chip capacitor<br>• Lowers the UGB |
| Miller compensation | • Easy to implement<br>• Improves phase margin<br>• Works well within a given maximum output capacitance range | • Can't support till infinite output capacitance<br>• Lowers the UGB<br>• Degrades phase margin when output pole is dominant |
| Feed forward compensation | • Works for a very wide range of capacitance and load currents.<br>• Improves phase margin.<br>• Doesn't lower the UGB. | • Requires an additional transconductance block.<br>• Power inefficient. |

Table 3.6: A comparison of existing compensation techniques

In the yellow region, the gate pole is greater than output pole but it is not dominant enough. Hence using miller compensation with a series resistance will be best solution for this. The red region is where we need to look into the most. In this region, the output pole is greater than gate pole. But it is not dominant enough to have a good phase margin. Using miller compensation or dominant pole compensation in this region might degrade the phase margin further unless a large miller capacitance or shunt capacitance is used. Feed forward compensation can be used in this case but it comes at the cost of extra power consumption.

The limitations of supporting wide capacitance range is that, simple techniques such as dominant pole compensation or miller compensation doesn't work perfect for all ranges. Enabling feed forward compensation for all ranges of capacitance is not a very good idea enabling it not when needed will decrease the efficiency of the LDO. After some capacitance $C_o > C_{max}$, the system becomes output pole dominant and phase margin will be greater than 60°.

# CHAPTER 4

# Proposed Auto Reconfigurable LDO

## 4.1 Working Principle

The basic idea of this proposed Auto Reconfigurable LDO is to use either miller compensation or feed forward compensation or neither based on the output capacitance. Let $C_{min}$ be the output capacitance below which the LDO is stable for all ranges of load current if a miller compensation is used. Let $C_{max}$ be the output capacitance after which the LDO is stable for all ranges of load current without any compensation. Below table summarizes the compensation techniques that are going to be used based on the output capacitance:

| **Case** | **Range of $C_o$** | **Dominant pole** | **Compensation technique** |
|---|---|---|---|
| 1 | $C_o < C_{min}$ | Gate pole | Miller compensation |
| 2 | $C_{min} \leq C_o \leq C_{max}$ | Output pole | Feed Forward Compensation |
| 3 | $C_o > C_{max}$ | Output pole | No compensation |

Table 4.1: Compensation technique based on output capacitance

It is fine to enable feed forward compensation even when $C_o > C_{max}$, but miller compensation should be strictly off in this region because pole splitting will bring the gate pole and output pole together which reduces the phase margin.

## 4.2 Technique for measuring the output capacitance

We don't need to precisely measure the output capacitance; instead, we need to determine the range in which the output capacitance resides in order to decide which compensation technique should be implemented. These are the steps involved in measuring the $C_o$

- Turn off all the sources in the LDO and inject a constant DC current in to the output node.
- Measure the output voltage. The output voltage is of the form :

$$V_{out} = R_o I_{dc} \left(1 - e^{\frac{-t}{R_o C_o}}\right)$$

- Let the time required for $V_{out}$ to reach $\Delta$v is $t_0$, where $\Delta$v is a fixed voltage value.
- Use a comparator to measure $t_0$ as pulse. The negative terminal is connected to output of LDO and positive terminal is connected to a voltage $\Delta$v.
- For small value of $\Delta$v, $t_0$ will be small. Then the above $V_{out}$ equation can be approximated as :

$$\Delta \text{v} \simeq I_{dc} R_o \left(1 - (1 + \frac{-t_0}{R_o C_o}\right)$$
$$\Delta \text{v} = \frac{I_{dc} \cdot t_0}{C_o}$$
$$C_o = \frac{I_{dc} \cdot t_0}{\Delta \text{v}}$$

- Let $C_{min}$ be the lower range of $C_o$ below which the gate pole is dominant always with PM > 60° and $C_{max}$ be the upper range of $C_o$ above which the output pole is always dominant with PM > 60°
- Use two counters with clock periods $T_{min}$ and $T_{max}$ respectively and clock gated with $t_0$ and $\overline{Q}$ [4] . The output of the counter will be 1 if $t_0$ > T/2 . Otherwise, the output is 0.
- $T_{min}$ and $T_{max}$ corresponds to the time taken by capacitors to get charged to $\Delta$v when a current $I_{dc}$ is injected into the capacitors $C_{min}$ and $C_{max}$ respectively.

$$C_{min} = \frac{I_{dc} \cdot T_{min}}{2\Delta \text{v}}$$
$$C_{max} = \frac{I_{dc} \cdot T_{max}}{2\Delta \text{v}}$$

The clocks $T_{min}$ and $T_{max}$ can be generated using two oscillators. Or else we can also use a single oscillator to generate $T_{min}$ and then scale it down to $T_{max}$ as well. The range of output capacitance can be calculated based on outputs of the two counters $Q_0$ and $Q_1$. Below is how the table looks like :

| **Case** | **Counter 1 ($Q_0$ for $C_{min}$)** | **Counter 2 ($Q_1$ for $C_{max}$)** | **Range of $C_o$** | **Compensation** |
|---|---|---|---|---|
| 1 | 0 | 0 | $C_o < C_{min}$ | Miller |
| 2 | 0 | 1 | doesn't exist | NA |
| 3 | 1 | 0 | $C_{min} \leq C_o \leq C_{max}$ | Feed Forward |
| 4 | 1 | 1 | $C_o > C_{max}$ | Not required |

Table 4.2: Output of counters vs Range of output capacitance

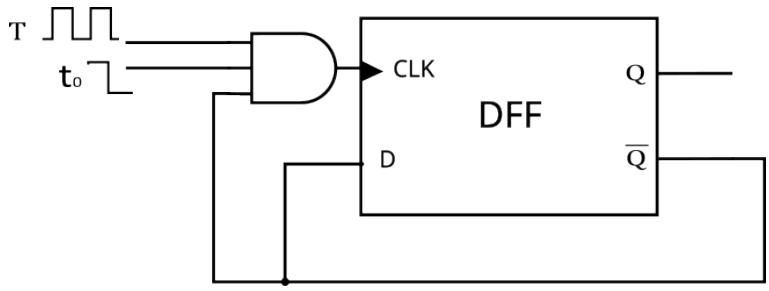
Based on the outputs of counter, a decoder logic can be used as control input to enable the compensation techniques. The logic is

Miller_enable = $Q_0$ (**NOR**) $Q_1$

Feed forward enable = $Q_0$ (**XOR**) $Q_1$

## Clock Gated Counter

Figure 4.1: Counter to compare $t_0$ with T




This is designed using a positive edge D flip flop. The output Q of D flip flop is initially set to 0 using the reset pin. The clock period is T and $t_0$ is the output pulse of comparator. This is a one bit counter with the clock input being **AND**

gated with $t_0$ and $\overline{Q}$ of the DFF. Hence the counter can only counts from $0 \rightarrow 1$. If $t_0 > T/2$, then the gate will not pass the positive edge of the clock so the output of the DFF remains at 0. If $t_0 > T/2$, then the positive clock edge passes the gate at T/2 which triggers the DFF and it's output becomes 1. It won't become 0 again unless reset due to the clock gated with $\overline{Q}$ (technically it stops counting). By Mapping $T_{min}$ and $T_{max}$ with $C_{min}$ and $C_{max}$, we can find the range of output capacitance.

## 4.3 Implementing the proposed LDO Circuit

### 4.3.1 Miller Compensation path:

We have planned to implement Miller compensation when the gate pole is dominant but output pole is inside UGB. The miller feedback consists of a miller capacitance $C_c$, a switch and a RHP nulling resistor $R_z$ connected in series. This feedback path is connected across the second stage of the LDO i.e., output of error amplifier and the Output voltage node. The switch is designed using a CMOS and is controlled by $V_{miller}$ which lets us enable or disable miller compensation[5].

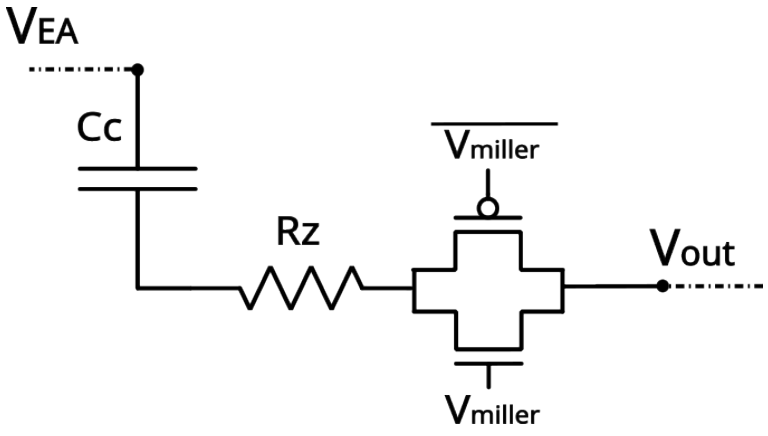



Figure 4.2: Miller Feedback path

### 4.3.2 Feed forward path

We have planned to implement Feed Forward compensation when the output pole is dominant but the gate pole is inside UGB. The feed forward path consists of a capacitance $C_f$, a resistance $R_f$ and a transconductance block $G_{m_f}$. The $C_f$ is connected between $V_{out}$ and positive terminal of the $G_{m_f}$. The $R_f$ is connected between positive terminal of the $G_{m_f}$ and ground. The negative terminal of $G_{m_f}$ is grounded and the output is connected to the gate of PMOS powerFET. The transconductance block is enabled or disabled using $V_{ff}$.

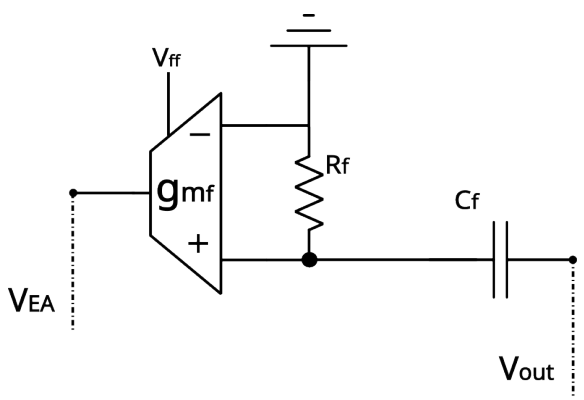



Figure 4.3: Feed forward compensation path

### 4.3.3 Circuit to measure output capacitance

A current $I_{dc}$ should be injected into node at least till $T_{max}/2$ seconds to get the range of output capacitance. The $I_{dc}$ can be realised using a current mirror circuit which is turned ON or turned OFF using EN_MEAS control. While injecting current, the PMOS LDO should be OFF so that it doesn't interfere with $V_{out}$. After t = $T_{max}/2$ , the current can be $I_{dc}$ should be turned OFF and the LDO can be turned ON . After t = $T_{max}/2$ , the output of counters $Q_0$ and $Q_1$ will be settled and circuit will be now operate with the necessary compensation enabled.

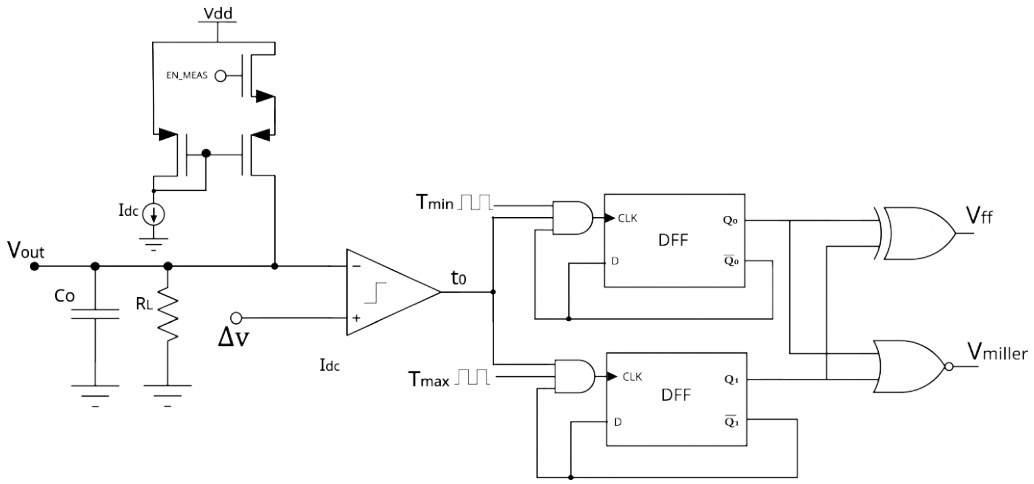



Figure 4.4: Circuit to measure output Capacitance

### 4.3.4 Final Circuit schematic

The below figure 4.5 is the complete architecture of the proposed auto reconfigurable LDO which supports zero to infinite capacitance with a maximum load of 10mA.

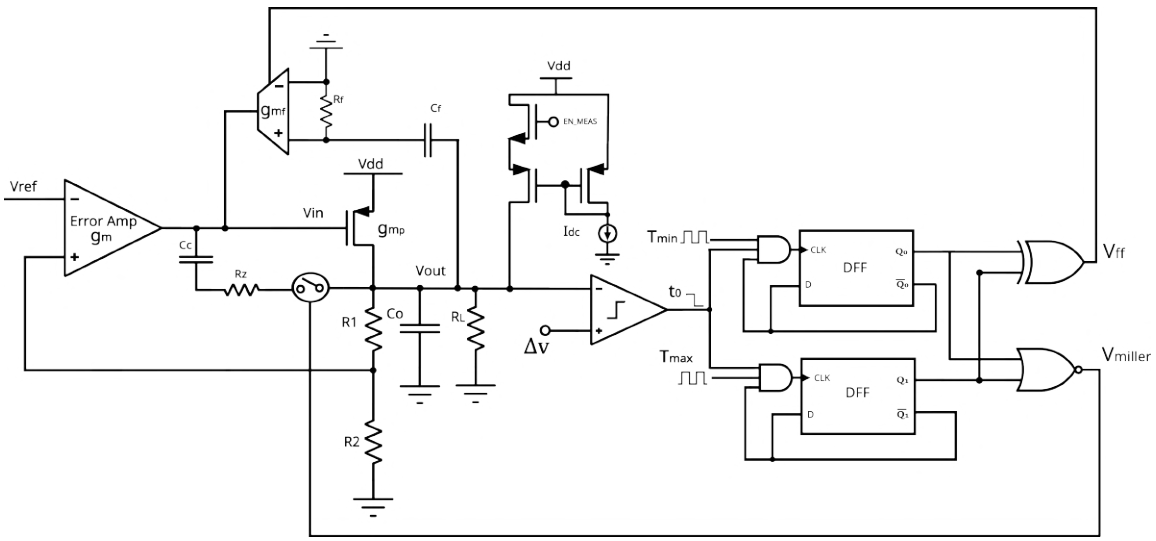



Figure 4.5: Final LDO circuit

## 4.4 Mapping the measured values with compensation

Now with the architecture being completed, we need to fix the parameters involved in the design of the circuit. The technology being used is tsmc 180nm. Table 4.3 shows the values of parameters of the circuit that we have previously used. The remaining parameters are $C_c$, $R_z$, $C_f$, $R_f$, $G_{m_f}$, $T_{min}$, $T_{max}$ where as $R_L$ and $C_o$ are variable loads (externally connected).

| Parameter | Value |
|---|---|
| $Vin$ | 1.8 V |
| $Vout$ | 1.5 V |
| Max Load | 10 mA |
| $Vref$ | 0.6 V |
| $R_1$ | 150 K Ω |
| $R_2$ | 100 K Ω |
| W | 565 $\mu$m |
| L | 0.18 $\mu$m |
| $g_m$ (err amp) | 5$\mu$ A |
| $R_e$ | 10 M Ω |
| $C_g$ | 1.28 pF |
| $I_{dc}$ | 1 mA |
| $\Delta$v | 50mV |

Table 4.3: Design parameters of the proposed LDO

### Miller compensation parameters

From table 3.2, for 1nF output capacitance, using a miller capacitance of 41pF gave stable results. We are limiting the capacitance to 20pF since it is ON chip, and connecting a series resistance of 10K to nullify the zero effect. This new miller capacitance will now give stable result for all loads till a maximum capacitance of 500pF. Hence $C_c$ = 20pF and $R_z$ = 10K Ω.

## Feed Forward block parameters

The Feed forward block is used to cancel the gate pole. From tables 3.4 and 3.5, the gate pole is located at around 80 KHz. The new zero introduced due to this compensation is $\frac{1}{\left(1+\frac{g_{m_f}}{\beta g_m}\right) C_f R_f}$ and new pole is $\frac{1}{R_f C_f}$. The new pole should be greater than output pole for all ranges of $C_o$ and $R_L$ in which this compensation is enabled. Fix $C_f$ = 10pF and $R_f$ = 100K which satisfies this condition. For the zero to cancel pole:

$$R_e C_g \simeq \left(1 + \frac{g_{m_f}}{\beta g_m}\right) C_f R_f$$
$$g_{m_f} \simeq \frac{\beta R_e C_g g_m}{C_f R_f}$$

On substituting the values, We get $g_{m_f} \simeq 20\mu A/V$.

## Time periods $T_{min}$ and $T_{max}$

Let $C_{min}$ be the lower range of $C_o$ below which the gate pole is dominant always with PM > 60° and $C_{max}$ be the upper range of $C_o$ above which the output pole is always dominant with PM > 60°. We have $C_{min}$ = 500 pF and $C_{max}$ = 272.3 $\mu F$ from previous equations. The time period of clocks for counters $Q_0$ and $Q_1$ are

$$T_{min} = \frac{2\Delta \mathrm{v} \cdot C_{min}}{I_{dc}}$$
$$T_{max} = \frac{2\Delta \mathrm{v} \cdot C_{max}}{I_{dc}}$$

On substituting the values, we get $T_{min}$ = 50ns and $T_{max}$ = 27.3ms

# CHAPTER 5

# Simulation results

## 5.1 DC Load Regulation

The Load resistance $R_L$ is varied and the settling output voltage $V_{out}$ is plotted. It changes by 3.7 mV across loads.

$V_{out}$ = 1.5008803V at $R_L = 150\Omega$

$V_{out}$ = 1.5045836V at $R_L = \infty$

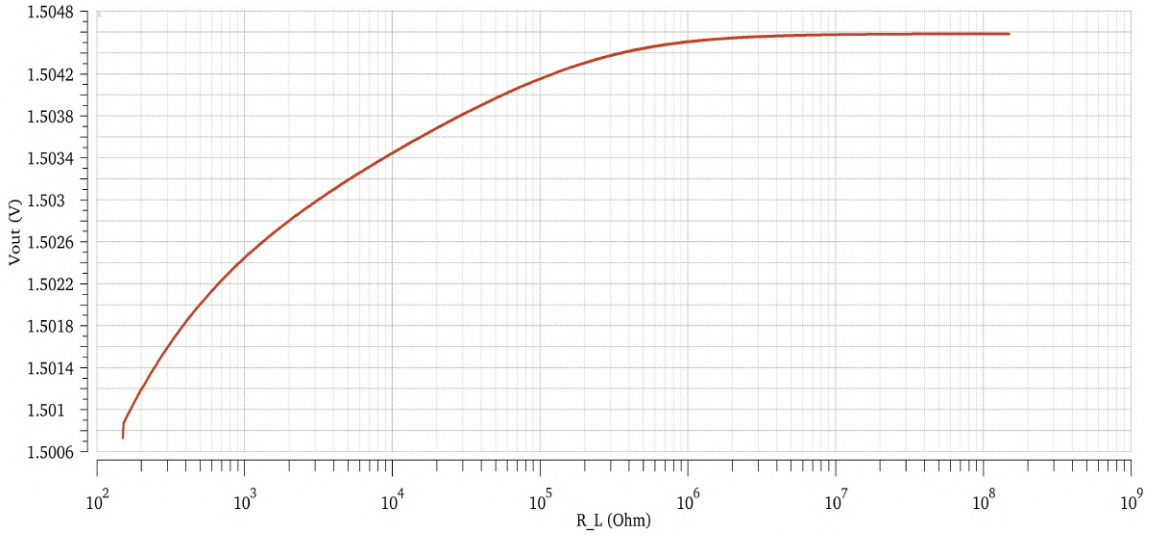



Figure 5.1: Output Voltage $V_{out}$ vs Load Resistance (log scale)

$$\text{Load regulation} = \frac{V_{\text{no load}} - V_{\text{max load}}}{V_{\text{no load}}} \times 100\%$$
$$= \frac{3.7\ mV}{1.5\ V} \times 100\%$$
$$\simeq 0.25\%$$

## 5.2 Line regulation

The Input voltage $V_{in}$ is swept from 1.8V to 2V and the output voltage $V_{out}$ is plotted. It changes by 55.71 $\mu$V across the range.

$V_{out}$ = 1.5045836V at $V_{in}$ = 1.8 $V$

$V_{out}$ = 1.50463931 at $V_{in}$ = 2 $V$

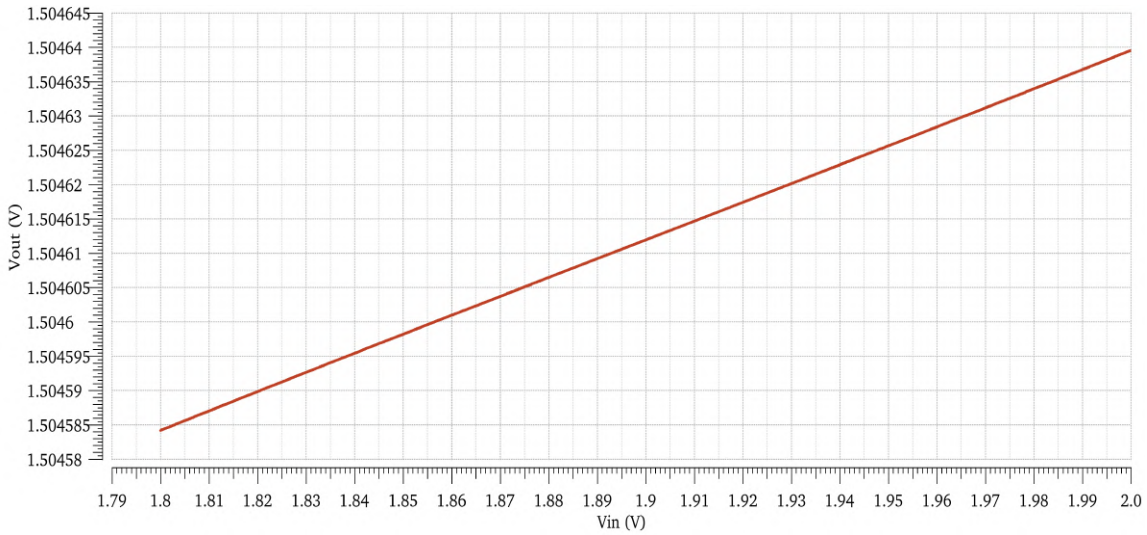



Figure 5.2: Output Voltage $V_{out}$ vs Input Voltage $V_{in}$

$$\begin{aligned}\text{Line regulation} &= \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \times 100\% \\ &= \frac{55.7\ \mu V}{0.2\ V} \times 100\% \\ &\simeq 0.02785\%\end{aligned}$$

## 5.3 Stability of LDO for extreme cases

This table contains the new phase margin of the LDO upon the previous LDO phase margin for various loads and capacitance (taken from 3.4 and 3.5 )

| Rload | Cout | Phase margin | Dominant pole | C_miller | Comp type | R_z | New PM |
|---|---|---|---|---|---|---|---|
| Infinite | 10pF | 14.78 | Gate | 20p | Miller only | 10K | 89.56 |
| Infinite | 50pF | 6.56 | Gate | 20p | Miller only | 10K | 86.46 |
| Infinite | 100pF | 5.64 | Gate | 20p | Miller only | 10K | 82.64 |
| Infinite | 200pF | 4.46 | Gate | 20p | Miller only | 10K | 75.55 |
| Infinite | 300pF | 4.46 | Gate | 20p | Miller only | 10K | 75.55 |
| Infinite | 500pF | 4.37 | Gate | 20p | Miller only | 10K | 61.95 |
| Infinite | 1nF | 4.93 | Output pole | – | Feed forw | – | 107.81 |
| Infinite | 3nF | 6.01 | Output pole | – | Feed forw | – | 102.83 |
| Infinite | 5nF | 8.59 | Output pole | – | Feed forw | – | 96.09 |
| Infinite | 10nF | 11.75 | Output pole | – | Feed forw | – | 85.70 |
| Infinite | 20nF | 16.41 | Output pole | – | Feed forw | – | 78.53 |
| Infinite | 50nF | 24.85 | Output pole | – | Feed forw | – | 77.44 |
| Infinite | 75nF | 30.38 | Output pole | – | Feed forw | – | 78.96 |
| Infinite | 100nF | 34.92 | Output pole | – | Feed forw | – | 80.31 |
| Infinite | 200nF | 47.69 | Output pole | – | Feed forw | – | 83.89 |
| 150 | 500nF | 5.43 | Output pole | – | Feed forw | – | 115.71 |
| 150 | 1uF | 6.03 | Output pole | – | Feed forw | – | 100.67 |
| 150 | 2uF | 7.21 | Output pole | – | Feed forw | – | 89.39 |
| 150 | 5uF | 10.49 | Output pole | – | Feed forw | – | 74.71 |
| 150 | 10uF | 13.66 | Output pole | – | Feed forw | – | 69.55 |
| 150 | 20uF | 18.89 | Output pole | – | Feed forw | – | 69.98 |
| 150 | 50uF | 29.26 | Output pole | – | Feed forw | – | 75.92 |
| 150 | 100uF | 40.34 | Output pole | – | Feed forw | – | 81.22 |
| 150 | 200uF | 53.82 | Output pole | – | Feed forw | – | 85.22 |
| 150 | 300uF | 61.98 | Output pole | – | – | – | 61.98 |
| 150 | 500uF | 70.99 | Output pole | – | – | – | 70.99 |

Table 5.1: New Phase margin for various loads and capacitance

## 5.4 Output of counter for various values of Co

The circuit used for measuring output capacitance of LDO has two counters Q0 and Q1 which are provided with clocks of time period $T_{min}$ and $T_{max}$ respectively. Figure 5.3 and 5.4 are the outputs of counters Q0 and Q1 respectively for various output capacitance. Q0 and Q1 are used to determine the compensation technique needed to be enabled. Figures 5.5 and 5.6 are the outputs of decoder logic for Feed forward enable and Miller enable respectively.

**Counter 1 - Q0**

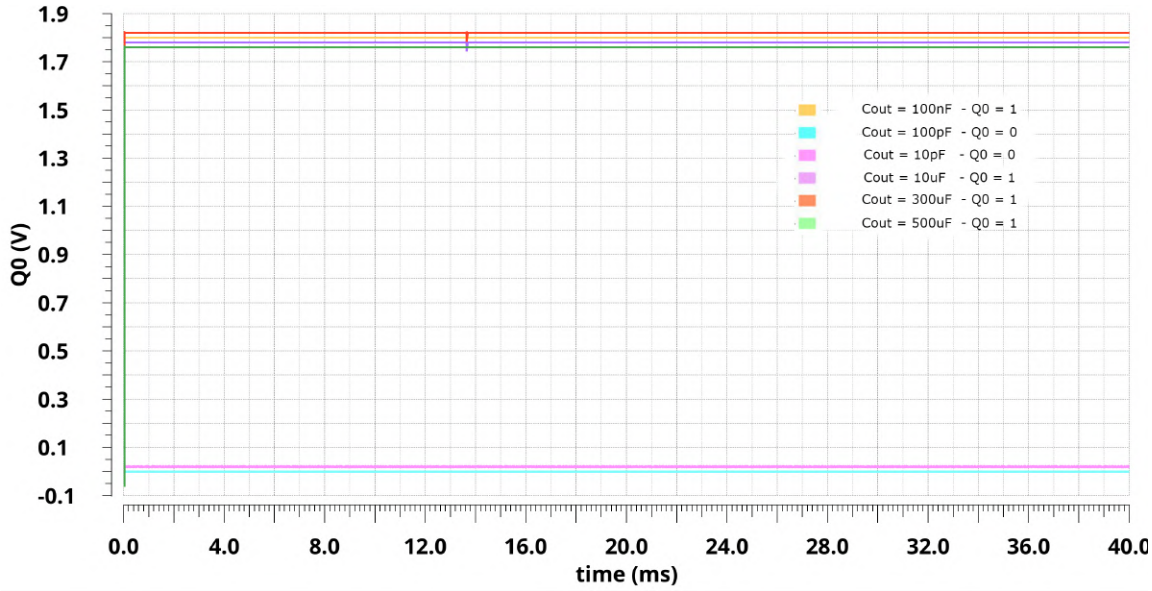



Figure 5.3: Q0 values for various output capacitance

### Counter 2 - Q1

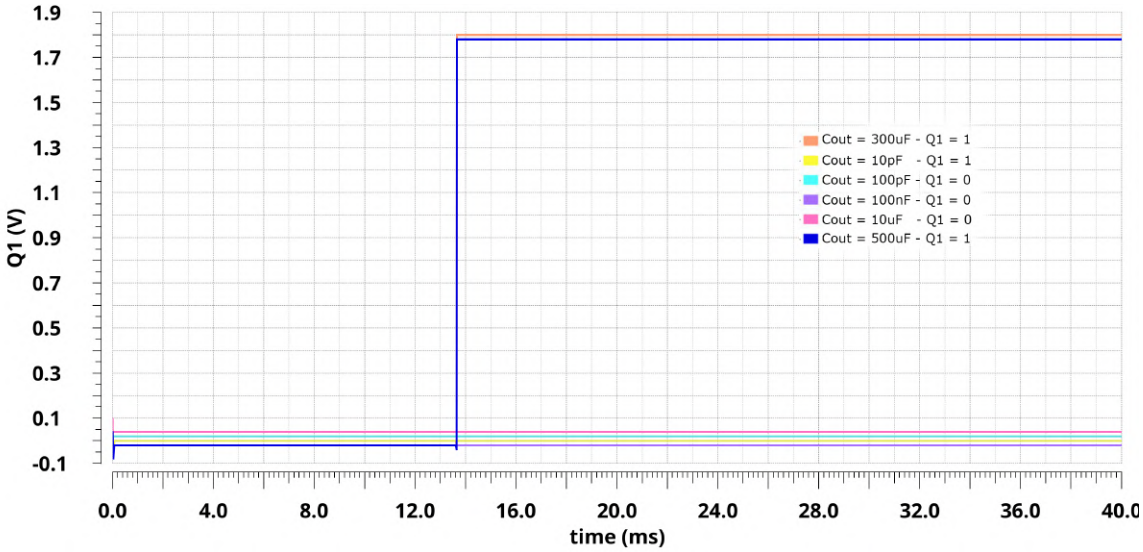



Figure 5.4: Q1 values for various output capacitance

### Feed forward Enable

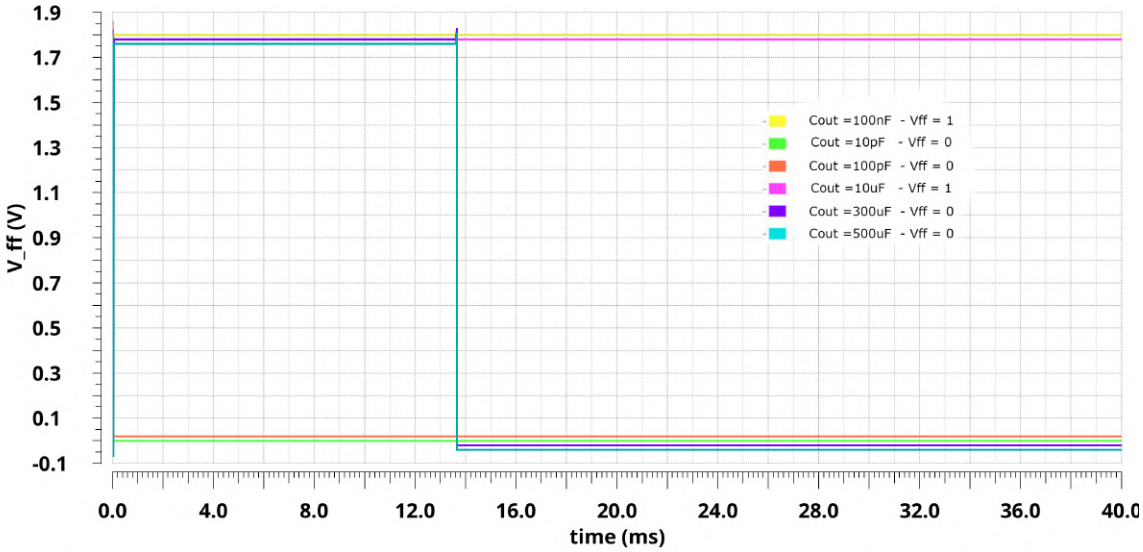



Figure 5.5: Vff values for various output capacitance

**Miller enable**

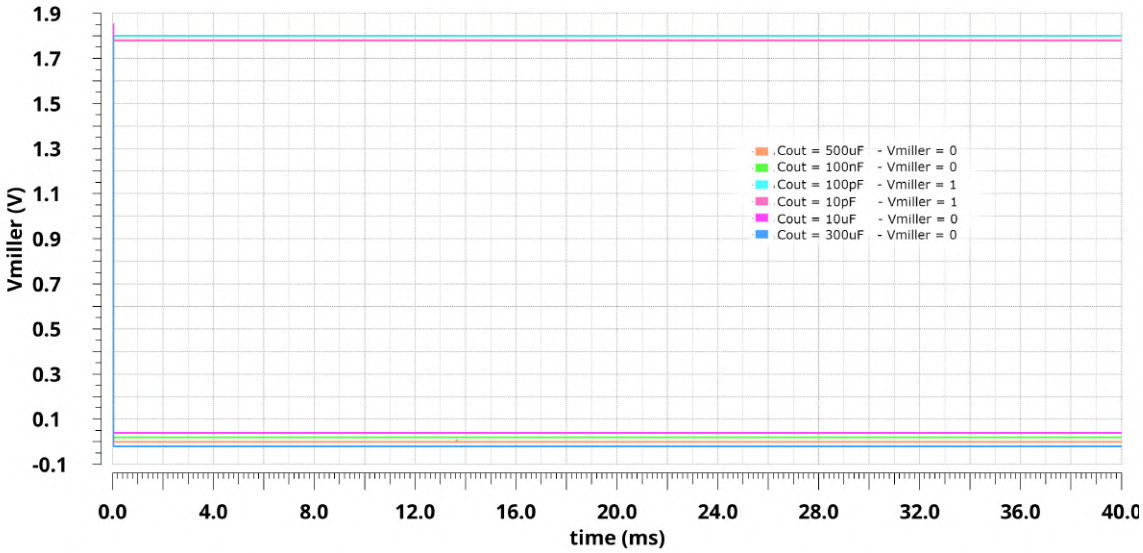



Figure 5.6: Vmiller values for various output capacitance

| $C_o$ | **Counter 1 ($Q_0$)** | **Counter 2 ($Q_1$)** | **Vmiller** | **V_ff** |
|---|---|---|---|---|
| 10pF | 0 | 0 | 1 | 0 |
| 100pF | 0 | 0 | 1 | 0 |
| 10nF | 1 | 0 | 0 | 1 |
| 10 uF | 1 | 0 | 0 | 1 |
| 300 uF | 1 | 1 | 0 | 0 |
| 500 uF | 1 | 1 | 0 | 0 |

Table 5.2: Counter outputs for various Co

## 5.5 Loop Gain Magnitude

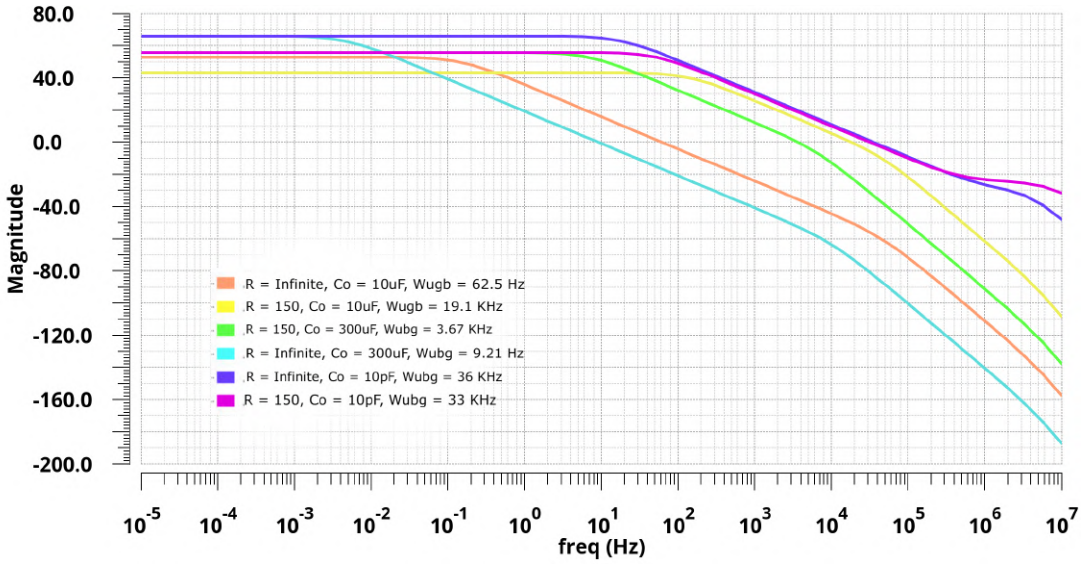



Figure 5.7: Loop Gain for various capacitance at R = ∞ and R = 150Ω

## 5.6 Phase response

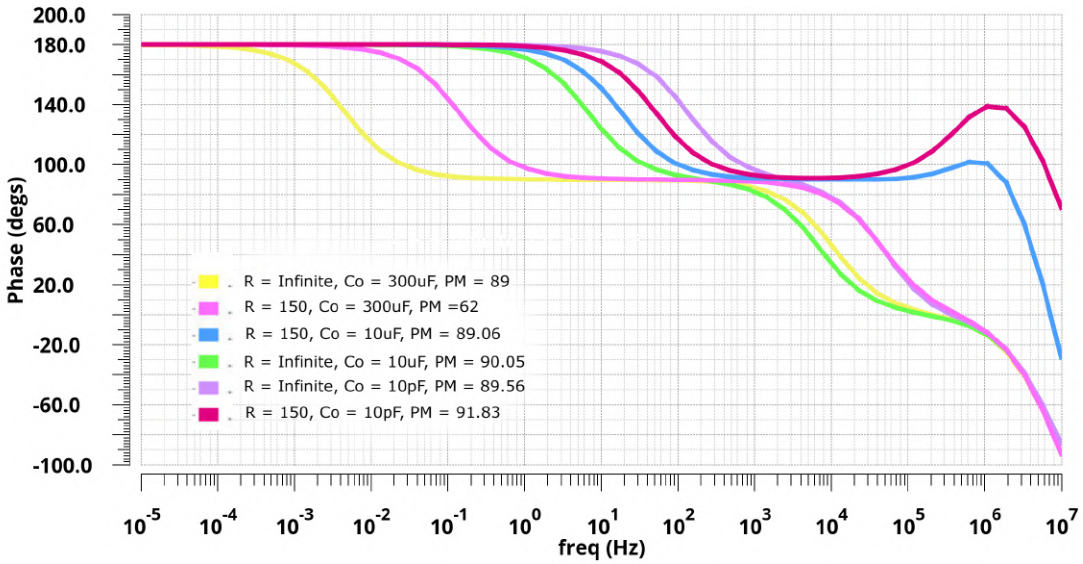



Figure 5.8: Phase response for various capacitance at R = ∞ and R = 150Ω

## 5.7 Vout vs Vref

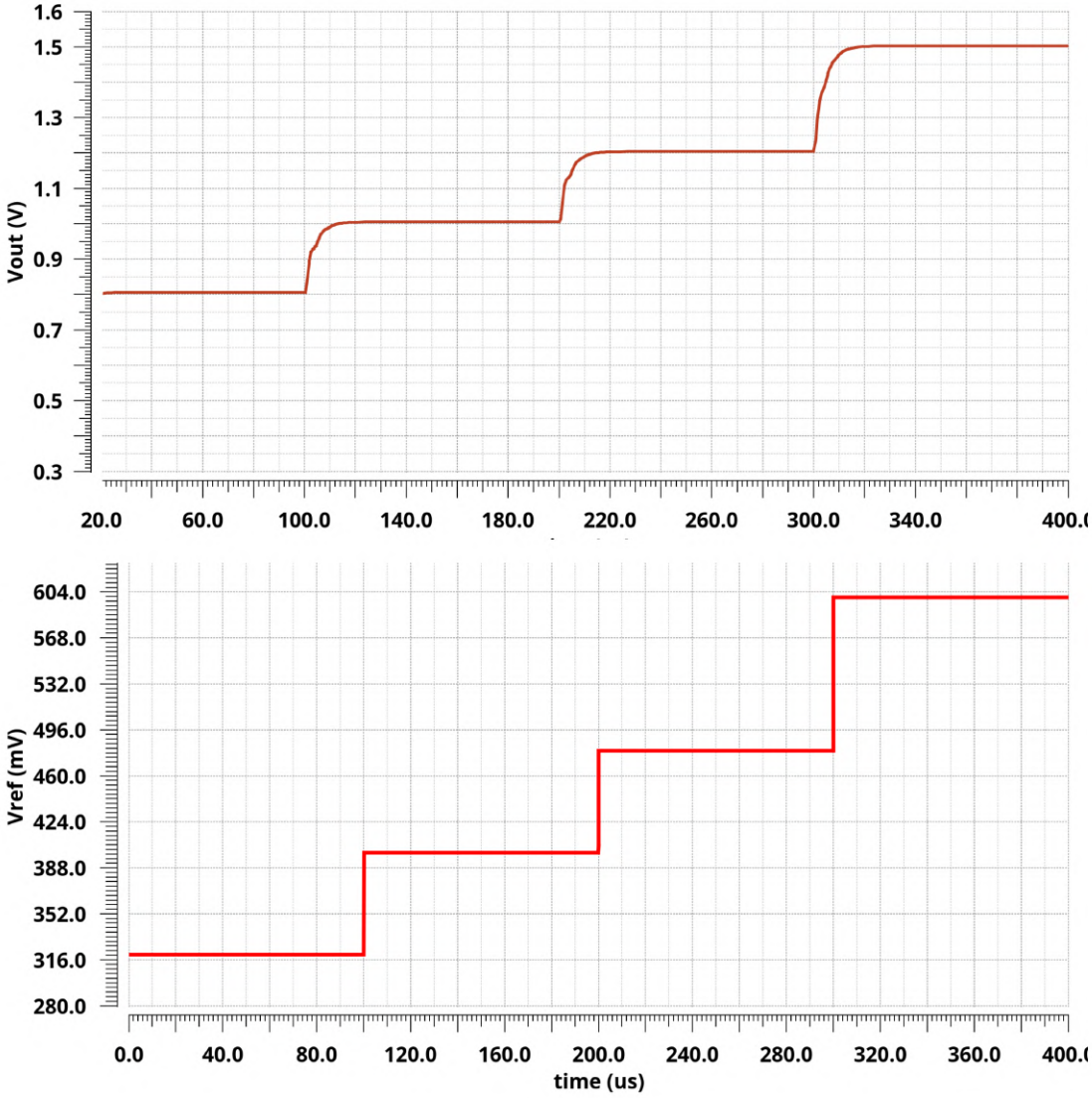



Figure 5.9: Output Voltage vs Reference Voltage transient

## 5.8 Load Transient

The output transient voltage is measured by changing the load from 0mA to 10mA over a rise time of 100ns. Below is the load transient for Co = 10pF, Co = 10uF, Co = 300uF.

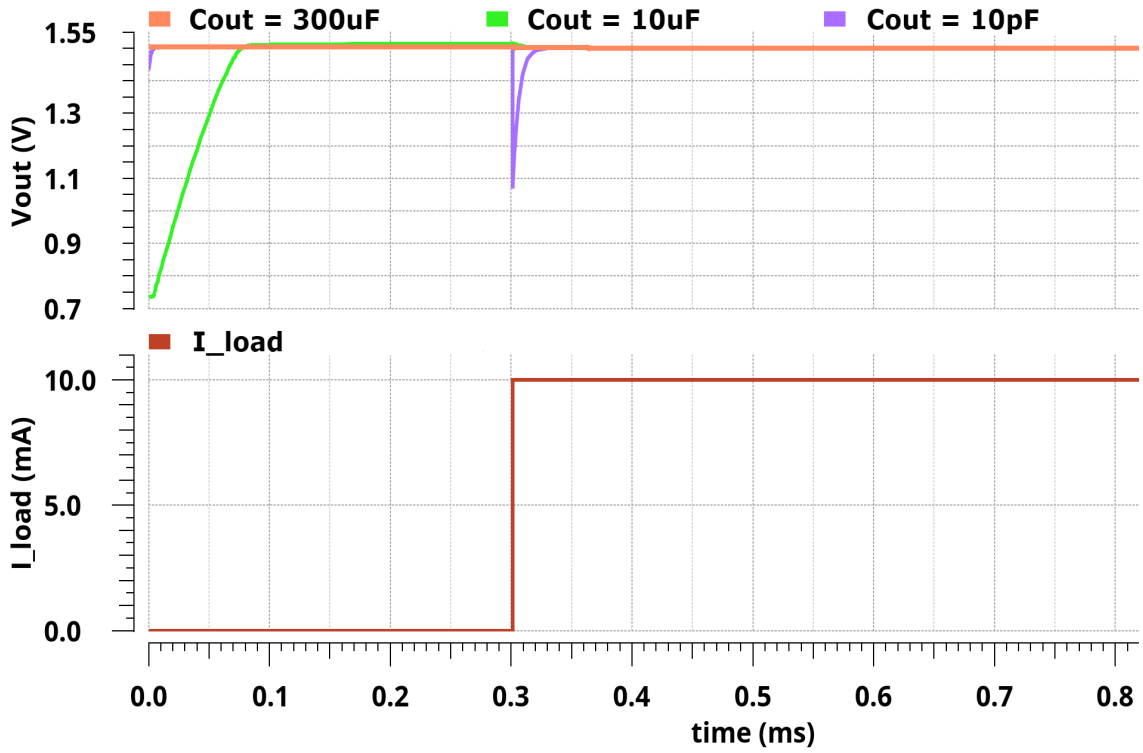



Figure 5.10: Load transient for 10pF ,10uF and 300uF output capacitance

# CHAPTER 6

# Conclusion and Future work

The proposed architecture chooses the compensation required by measuring the output capacitance of the LDO by injecting a constant current for a duration of $T_{max}$ seconds. This LDO is very stable for a wide range of capacitance and current loads. The main focus on this project has been on stability. Now this has been resolved, the other features such as PSRR, load and line transients of this circuit can be improved in the future work. The output resistance of the feed forward transconductance block can be improved so that it won't affect the impedance at the output node of the error amplifier. The undershoots and overshoots during transients need to be improved in the future work.

# REFERENCES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