POLAR POWER AMPLIFIER DESIGN

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **POLAR POWER AMPLIFIER DESIGN**, submitted by **NITHIN BABU**, to the Indian Institute of Technology Madras, for the award of the degree of **BACHELOR OF TECHNOLOGY**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

The goal of this project is to design an RF Power Amplifier (PA) with Polar Modulation, using *Cadence Virtuoso*. Usually the baseband information in a communication channel is broken down into the I-component (In-phase) and the Q-component (Quadrature). In the case of Polar Modulation, it is broken down into Amplitude Modulation (AM) and Phase Modulation (PM). Hence, we will have to design a PA to work in the 3.5GHz frequency range, and modulate the signal as polar modulation.

The PM component comes from the module present before the PA, and it will go through the PA, appearing at the output. The AM component will come through the supply node of the PA, and will be combined with the PM component at the output of the PA. To facilitate the integration of the AM component into the PA, we design a Low Dropout Regulation (LDO), and connect its output to the supply node of the PA.

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CHAPTER 1

POWER AMPLIFIER DESIGN PROCEDURE

For the entire design procedure, we use **TSMC 65GP** Technology to design the circuits. The Power Amplifiers (PAs) use ***nch*** model for the NMOS and ***pch*** for the PMOS, whereas the Low Dropout Regulators (LDOs) use ***nch_18*** model for the NMOS and ***pch_18*** model for the PMOS.

1.1 Designing a Common-Source Power Amplifier

We start with the design of an ideal common-source power amplifier (PA) by plotting various parameters of the NMOS. We plot the transit frequency (Ft) vs δ (where δ = 2*Id/gm), Ft*gm/Id vs δ, and gm*Ro vs δ for multiple values of L of the NMOS from 60nm to 200nm. We also plot gm(ac) vs δ by varying Vgs of the NMOS, to find the value of delta at which gm(ac) is maximized . This will help us figure out the characteristics of this particular NMOS, and will also help us to pin point the required operating points for our circuit.

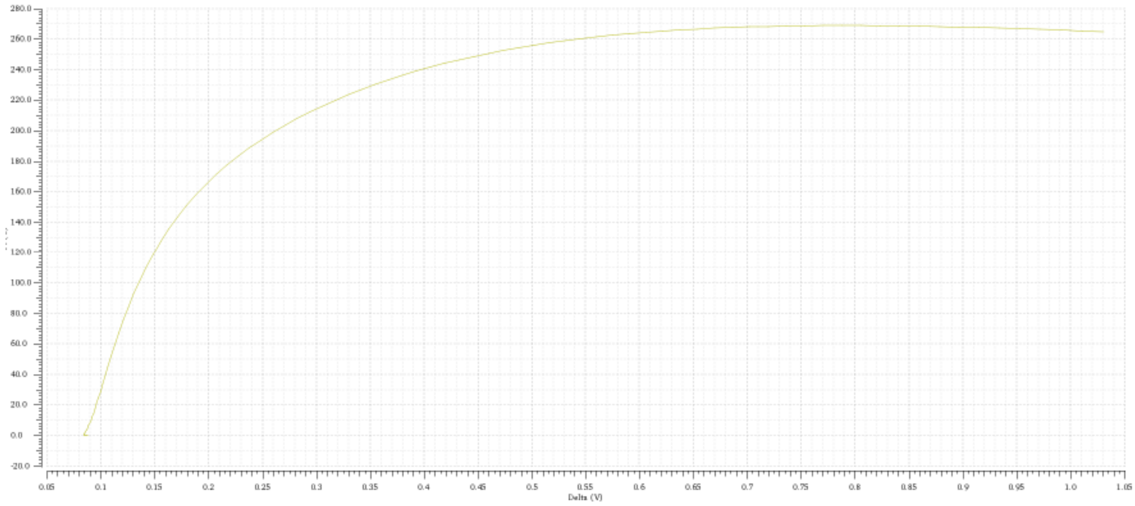


Figure 1.1: Ft vs δ

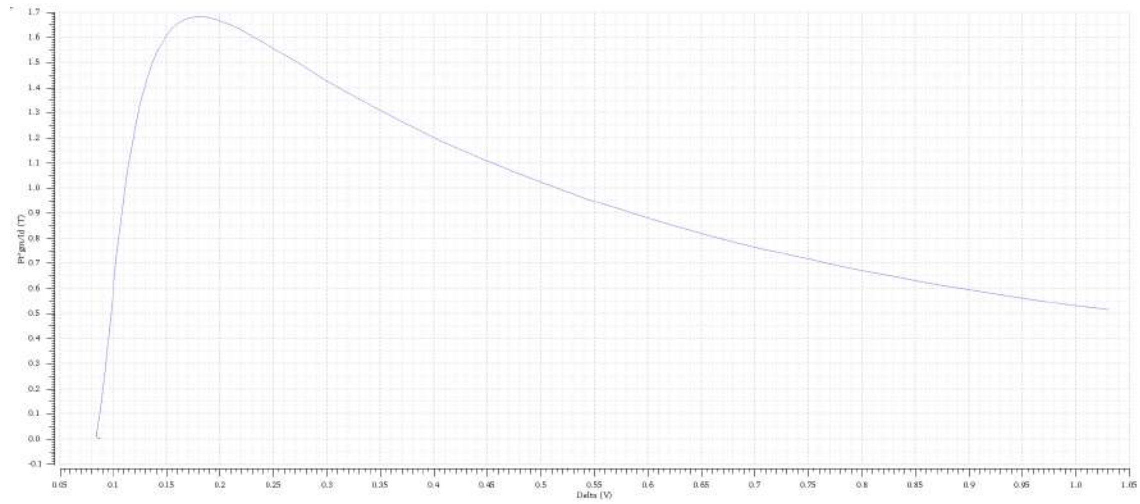


Figure 1.2: Ft*gm/Id vs δ

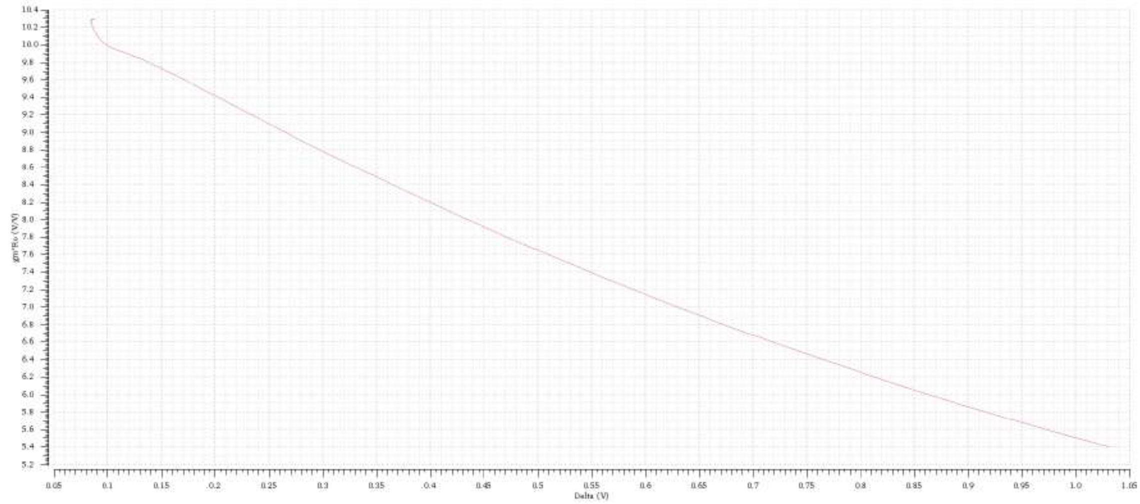


Figure 1.3: gm*Ro vs δ

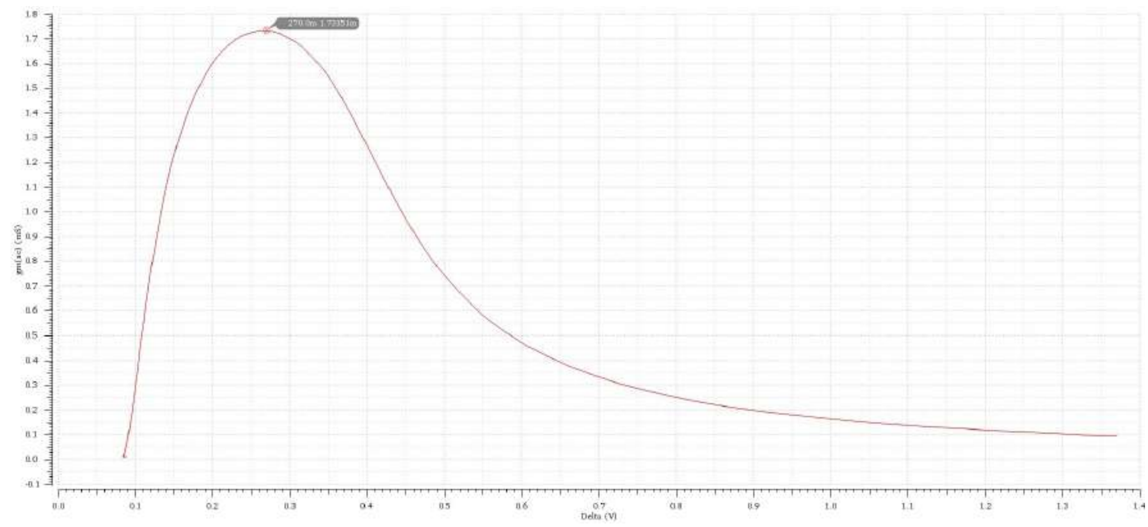


Figure 1.4: gm(ac) vs δ

The Length of the NMOS is chosen as 60nm (minium length), and the width is 2.5µm. From the above plot, we can say that maximum **gm(ac)** is **1.73mS** at δ **= 270mV**. At δ = 270mV, **gm(DC) = 2.72mV** and **Id = 367µA.**

Once the operating points of the NMOS have been decided, we start with the actual design of the PA. We started with a simple differential 2 transistor NMOS with an inductor-resistor(50 Ω) load on either drains of the MOSFETs.

1.1.1 Basic Power Amplifer Design

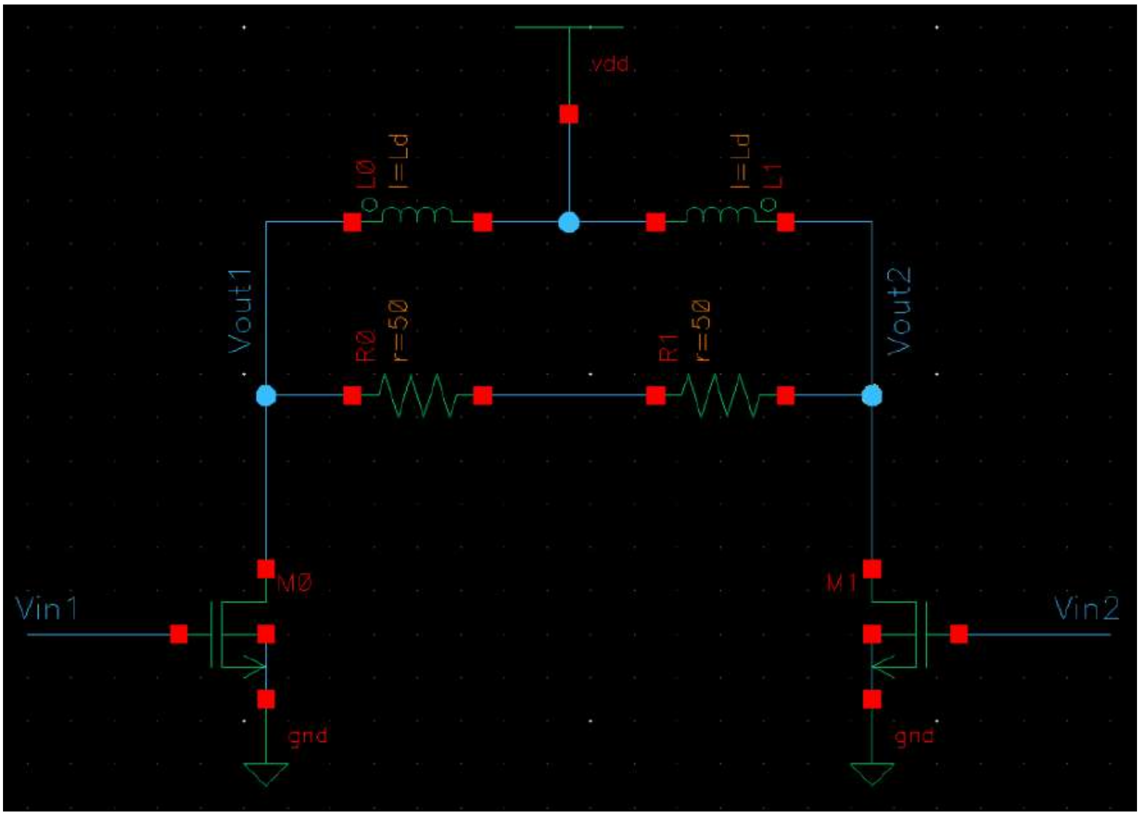


Figure 1.5: Basic PA Schematic

For TSMC65GP *nch* MOSFETs, the supply voltage, VDD = 1V.

Hence, $Vout1_{DC}$ = $Vout2_{DC}$ = 1V.

Considering the breakdown characteristics of the NMOS, $Vout1_{max}$ = $Vout2_{max}$ = 1.7V.

Vd_{sat} = 0.2V, hence, to stay in saturation region, $Vout1_{min}$ = $Vout2_{min}$ = 0.3V (a bit higher than saturation).

$$\Rightarrow 0.3V \leq Vout1, Vout2 \leq 1.7V$$

For the NMOS M0:

$$Pout_{max1} = P1 = \frac{(Vout1_{swing,max})^2}{2(50)} = \frac{(Vout1_{max} - Vout1_DC)^2}{100} = \frac{(0.7)^2}{100} = 4.9mW$$

Similarly, for the NMOS M1: $Pout_{max2} = P2 = 4.9mW$

Hence, $P_{total} = P1 + P2 = 9.8mW$

Let M0, M1 have W = 2.5µm, and L = 60 nm, with f fingers each. For Best cut-off condition: $I_{bias} = \frac{Vout_{amp,max}}{50} = \frac{0.7}{50} = 14mA$

For the NMOS M0 and M1: gm(ac) = 1.73mS at δ = 270mV, gm(DC) = 2.72mS, and Id = 367µA.

Since, we need $\text{I}_{bias} = 14mA \Rightarrow f = \frac{14mA}{367uA} = 38$

Hence, for the NMOS M0 and M1: number of fingers, f = 38

From the above detailed calculations, we can say that, for both NMOS M0 and M1, with W = 2.5µm, L = 60nm, number of fingers = 38, and Ibias = 14mA, we will be able to get a total differential power output, **$\mathbf{P}_{out}$ = 9.8mW.**

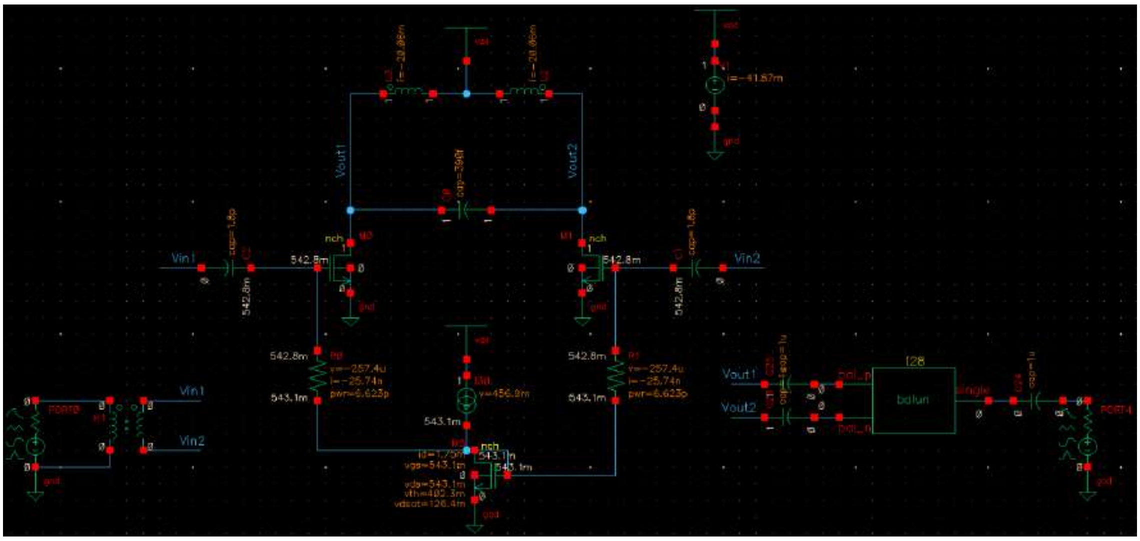


Figure 1.6: Basic PA Schematic with Current Mirror

The above schematic shows the PA along with a current mirror, which has a base current of **1.75mA** that is scaled up to the required current at the PA NMOS, M0 and M1, and AC blocking capacitors at the required positions. The differential ends of the PA are also attached with Baluns (or transformers) to create a single ended inputs and outputs (for simulation purposes). At the drains of the NMOS, we have added two inductors of **2.4nH** inductance, which is equivalent to a centre-tap inductance of **4.8nH**.

There is also a capacitance across the differential outputs of capacitance **390fF**. This LC tank setup will ensure the resonance to occur at **3.5GHz** as required.

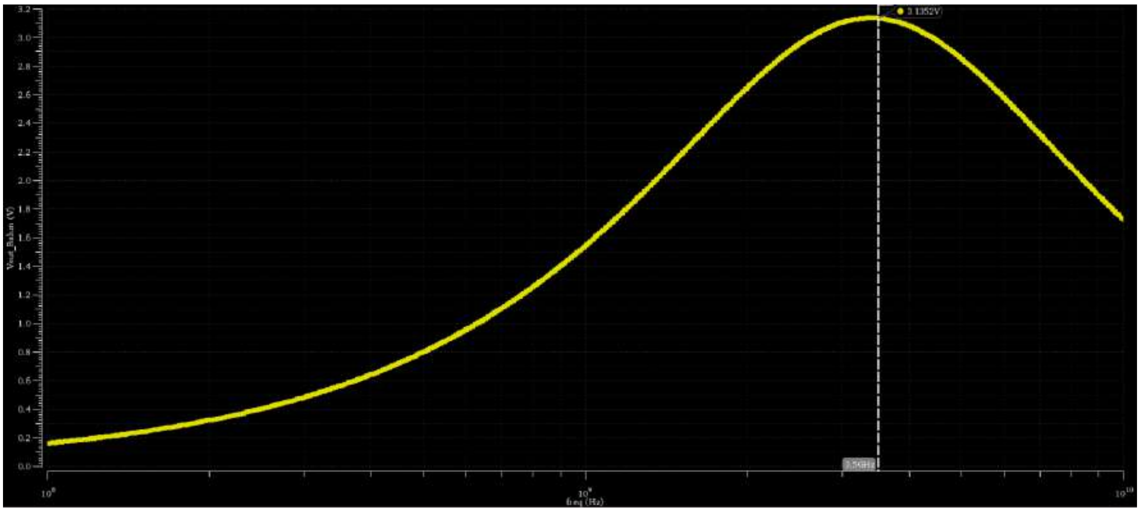


Figure 1.7: AC Gain at the output of the PA (Vout_balun)

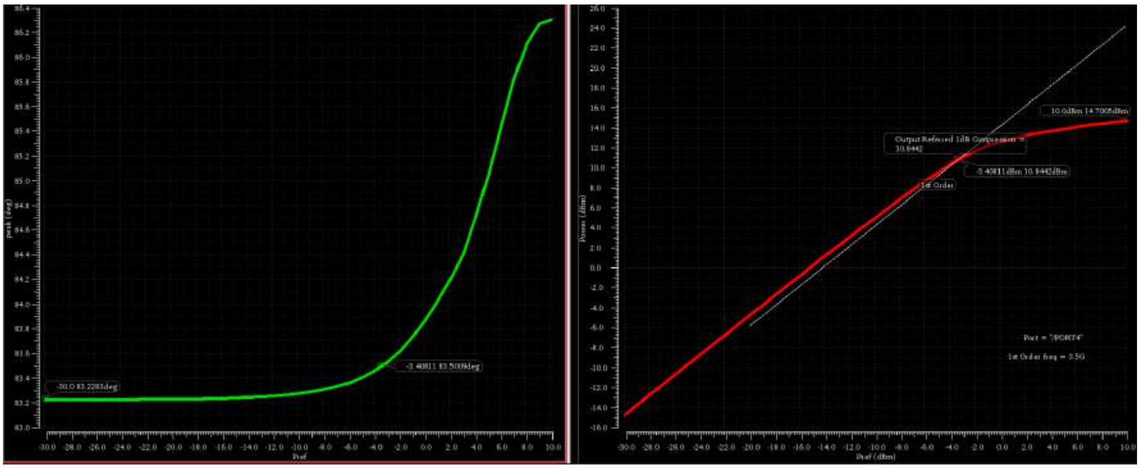


Figure 1.8: Phase Variations at differential output; P1dB Compression Plot

The AC analysis peaked at 3.5GHz with a gain of **3.1352 V/V**. The P1dB compression point was **10.8442 dBm**, saturated output power at **14.7 dBm**, with an output phase difference of **0.2723**°.

1.1.2 Capacitive Neutralization for the PA

In the PA NMOS M0 and M1, there is capacitance present between the gates and drains (Cgd). Hence, at higher frequencies these capacitances provide a path for current to flow, thereby causing an effect of instability in the power amplifier design.

To measure instability in a circuit in Cadence, we can run Hb + Hbsp simulation and obtain the Kf (Stability factor) plot for a particular circuit. If Kf > 1 for the entire range of frequencies, then the circuit is assumed to be stable. But if Kf < 1 at any point, then the circuit is considered to not be in a stable state.

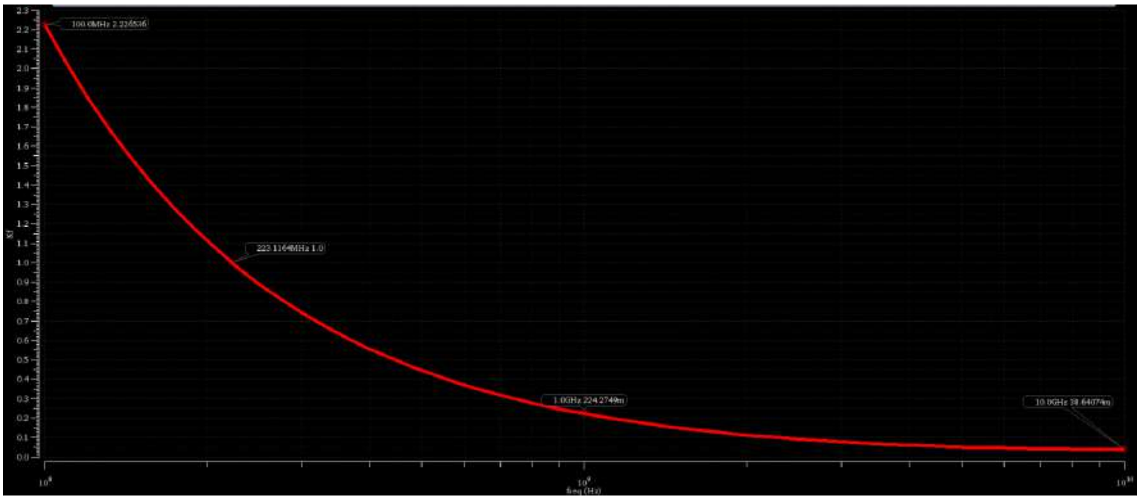


Figure 1.9: Kf Plot before Capacitive Neutralization

One way to eliminate this instability is through capacitive neutralization. What this means is that, we add a capacitance of nearly same value as the Cgd, but connect it across the exact opposite voltage. So for example, in our PA case, across M0, we connect the capacitor from gate of M0 to Vout2 (Drain of M1). And across M1, we connect it from gate of M1 to Vout1 (Drain of M0). This basically nullifies the current flow across the drain-gate path, thus improving the stability of the circuit.

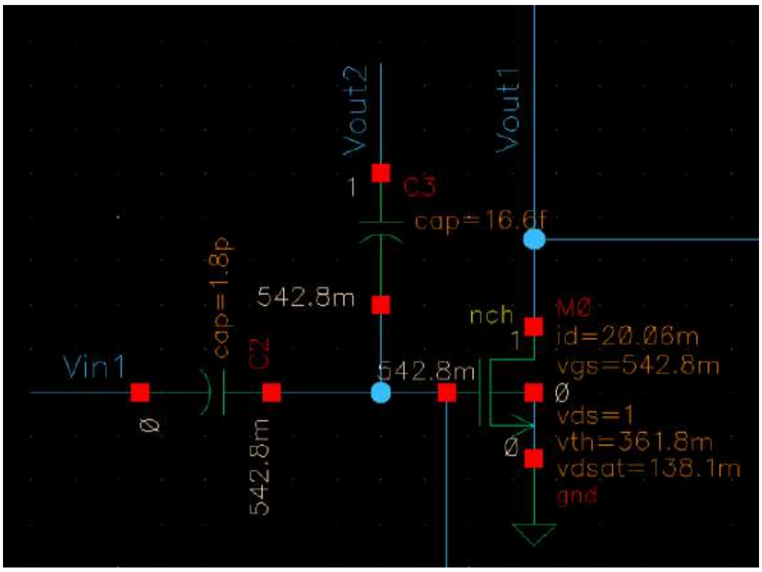


Figure 1.10: NMOS with Capacitive Neutralization

The above schematic shows the addition of capacitive neutralization capacitors. In our case, a capacitance of 16.6fF was used to get the best Kf plot. We will replace the ideal capacitor with an NMOS (with shorted drain and source) whose capacitance (across gate and drain) will mimic the same functioning of capacitive neutralization. These types of capacitors are also known as MOSFET capacitors, or moscaps in short. We are using moscaps here because they can track Cgd of NMOS M0 and M1 across process variations, and change the capacitance accordingly.

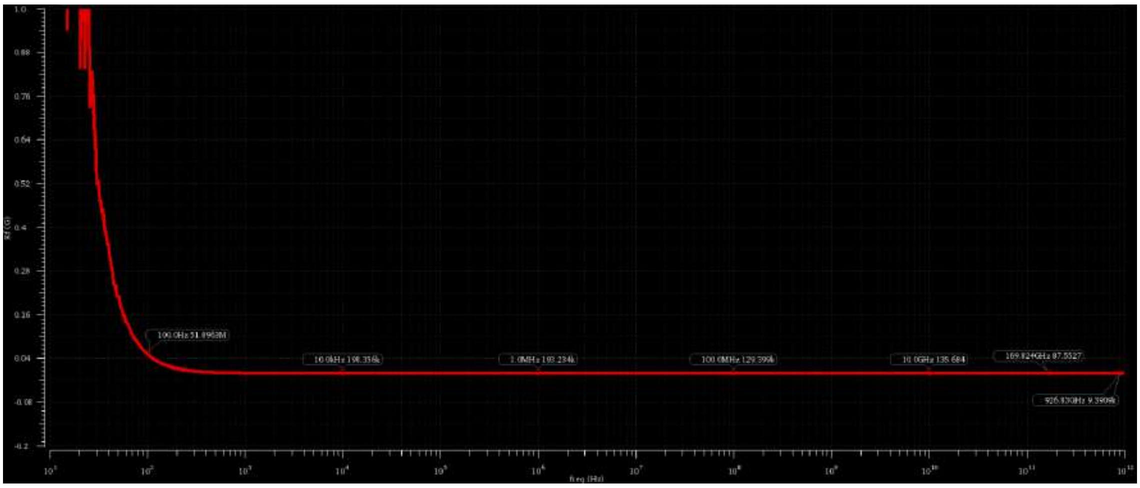


Figure 1.11: Kf Plot after Capacitive Neutralization

As can be seen from the above Kf plot, after capacitive neutralization, Kf value is definitely greater than 1 throughout the frequency range.

1.1.3 Final Design of the Power Amplifier

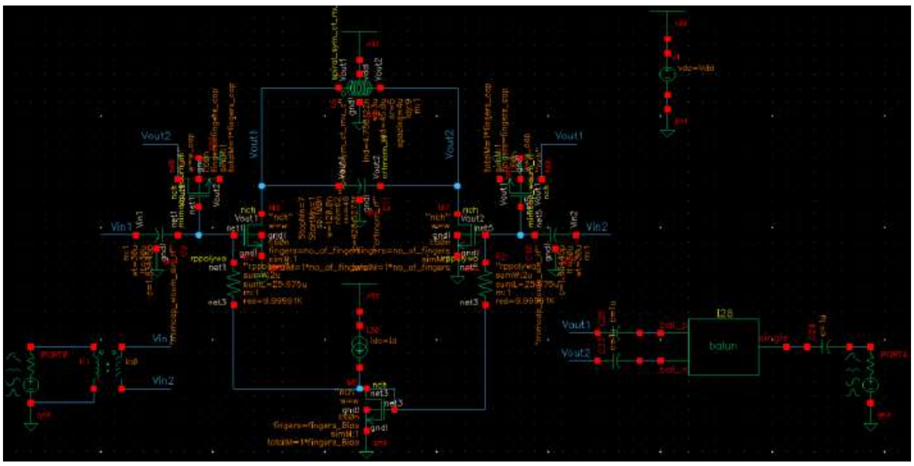


Figure 1.12: Final Schematic Design of the Power Amplifier

For our previously designed PA, we would need to make a few more changes. After replacing the ideal capacitors for capacitive neutralization with moscaps, we should also replace any ideal components with TSMC components. For example, the ideal inductors are to be replaced with TSMC *spiral centre-tap* inductors, the capacitors are replaced with TSMC *crtmom_rf* capacitors, and the bias resistors are replaced with TSMC *rppolywo* resistors.

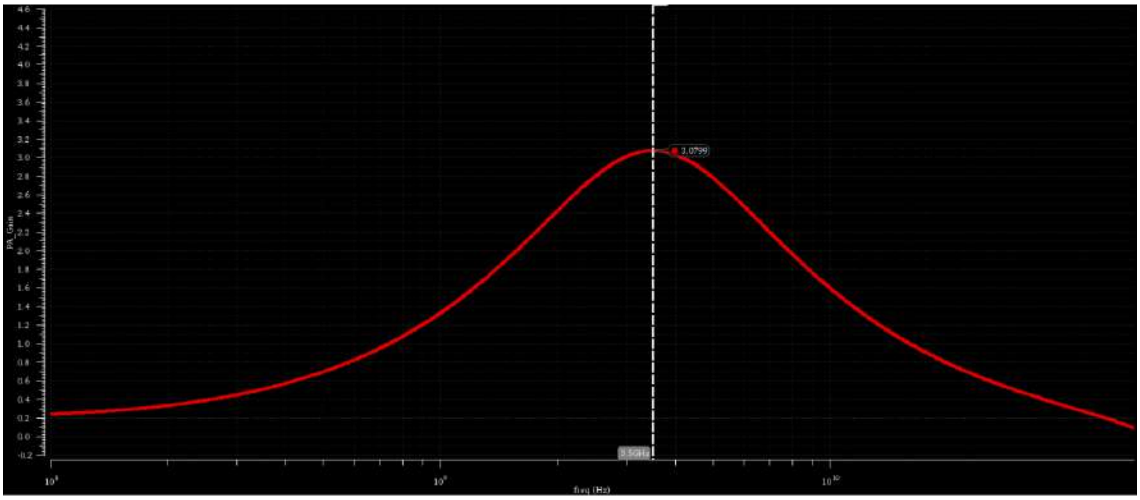


Figure 1.13: AC Gain for updated PA design

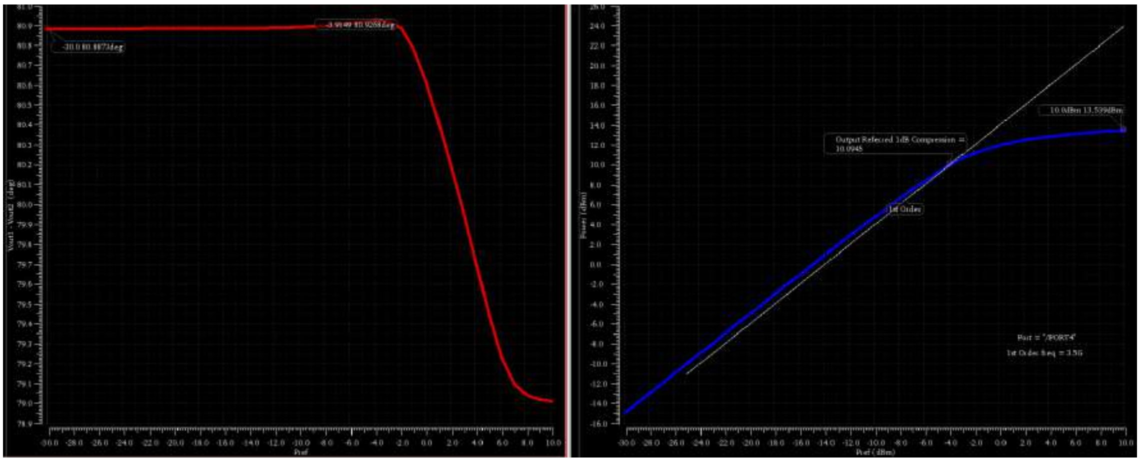


Figure 1.14: Phase Variations at differential output; P1dB Compression Plot

From the above plots, we can see that, for the updated design of the Power Amplifier, AC gain peaks at 3.5GHz with a gain of **3.0799 V/V**, a P1db compression point is at **10.0945 dBm** with saturated output power of **13.539 dBm**, and output phase difference of **0.0395°.**

1.1.4 Design of Pre-Power Amplifier (Inverter)

The higher width of the PA implies that the capacitance at their gates (Cgg) will be significantly higher (around 120fF). This means that RF modules prior to the PA will face a high capacitive load, thus, increasing the difficulty to generate full-swing signals. To avoid this, we use a driver (buffer stage) to drive the PA. This buffer stage is known as a pre-power amplifer (PPA), and in our case, will be a simple inverter.

We want to design an inverter with appropriate sizing such that, when the input is given a pulse with rise and fall times of 20ps, the rise and fall times at the output of the inverter is less than 20ps.

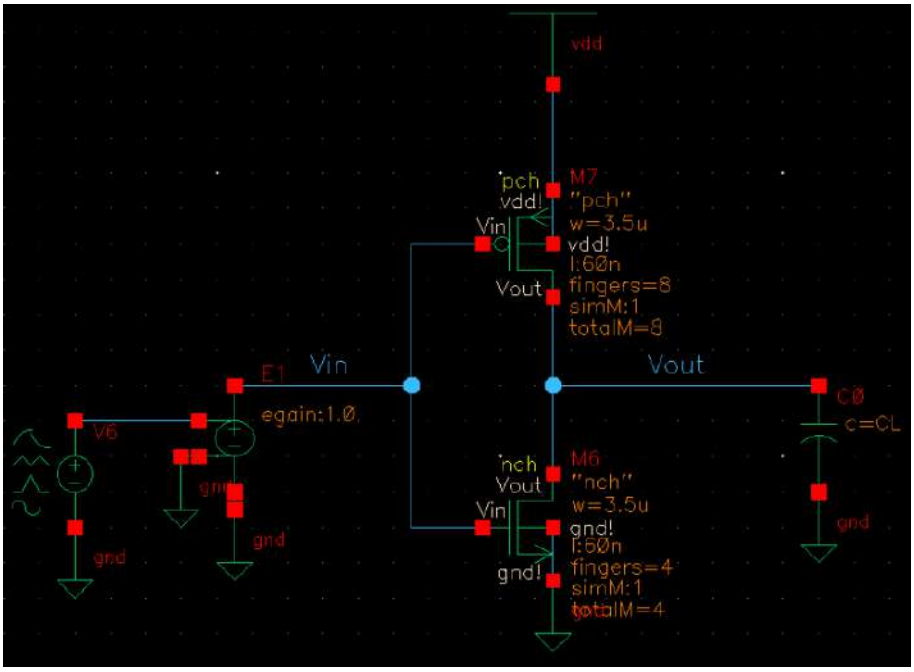


Figure 1.15: Schematic of Inverter (PPA)

The above is the schematic design for the inverter (PPA) with the following sizing:

- NMOS: W = 3.5µm, L = 60nm, fingers = 4
- PMOS: W = 3.5µm. L = 60nm, fingers = 8
- CL = 120 fF

The above design of the inverter had an output rise time and a fall time of **19.29ps**, for a pulse input with 10MHz frequency and a rise and fall time of **20ps**.

The output impedance for the above circuit was determined using PSS + PAC analysis. First, we remove CL and add a voltage source (with AC and PAC magnitude = 1) at the output of the inverter. After performing PSS + PAC, we plot the current through the voltage source vs frequency. From the current and voltage value (at 3.5GHz), we can find out the output impedance of the inverter. The output impedance of the inverter is **42.78** Ω **- j0.94** Ω. This impedance should be given at the input port of the PA.

1.1.5 Integration of PA and PPA

Since our PA and PPA have been designed, we can start by integrating both of them to form the PA + PPA circuit. We would ideally start by providing a sinusoidal signal at the input of the PPA and observe the output of the PA. This would let us know the working of the entire PA + PPA setup, and correct for possible errors, if any.

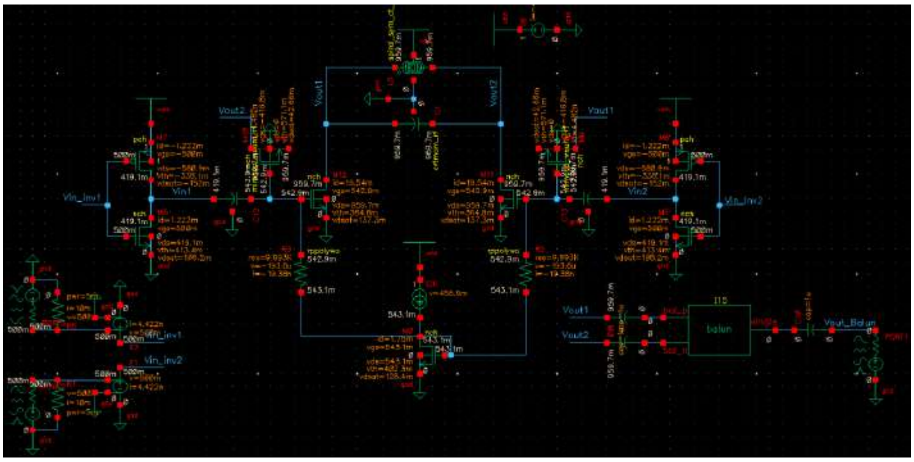


Figure 1.16: Basic Schematic Design of PA + PPA

As seen in the above schematic diagram, a differential input (sinusoidal) is given at the input, and the output (Vout1 - Vout2) is observed. We perform both *transient* analysis as well as *Hb* analysis to get the transient and spectral plots respectively.

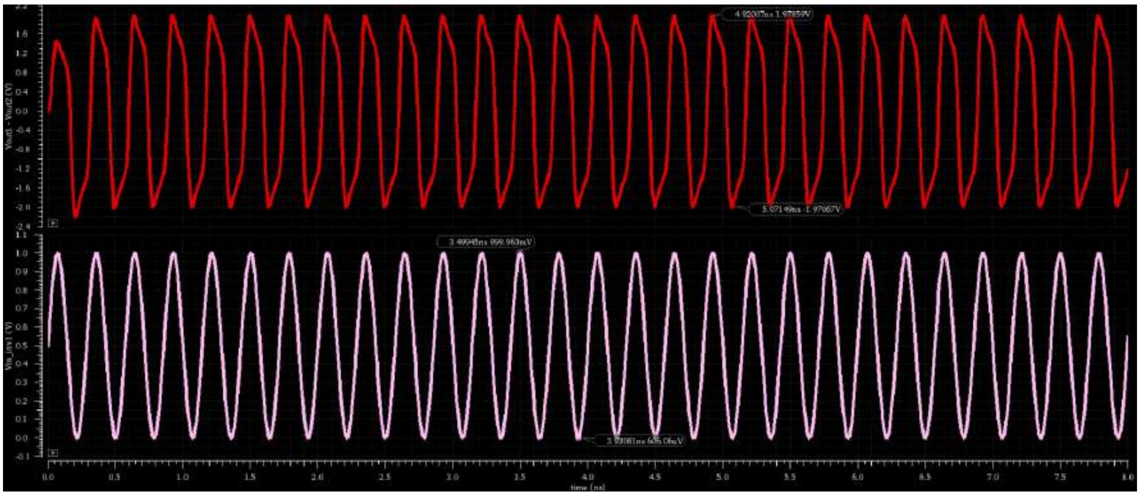


Figure 1.17: Differential Output of PA + PPA for a differential sinusoidal input

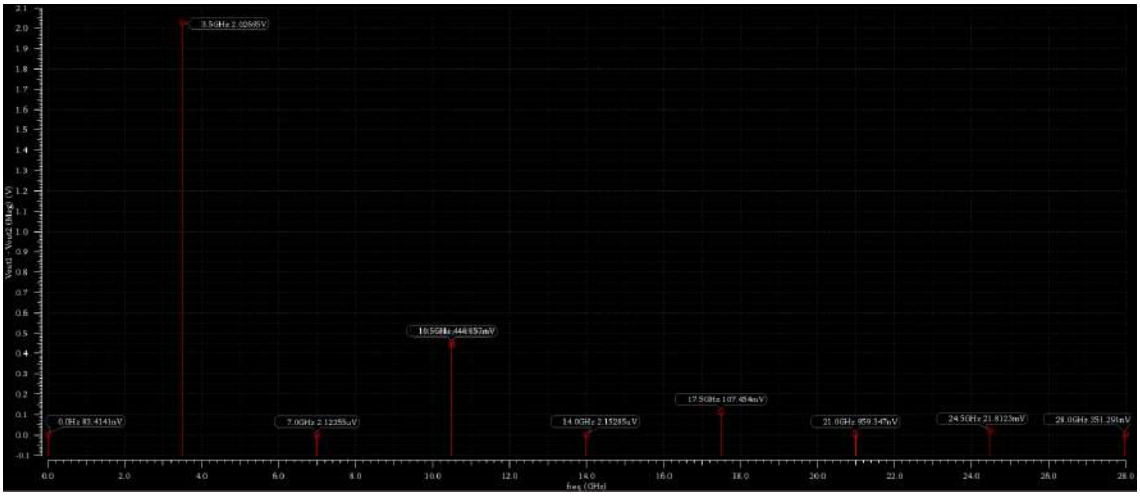


Figure 1.18: Differential Output Spectrum of PA + PPA

The above plots represent the transient and spectral plots of the differential output (Vout1 - Vout2) along with their peaks, for various frequencies.

1.1.6 PA + PPA as a Switching Power Amplifier

The above PA + PPA design is also considered to be a case of switching power amplifier. What this means is that, the input to the PA (Vin1, Vin2) have an almost square wave type signal, because of the inverter before it. The inverter pulls the output to either Vdd (1V in this case) or to ground depending upon the input to the inverter. This means that, the input to the PA oscillates between Vdd (1V) and gnd (0V), thus driving the PA to produce maximum possible power (Saturated Power).

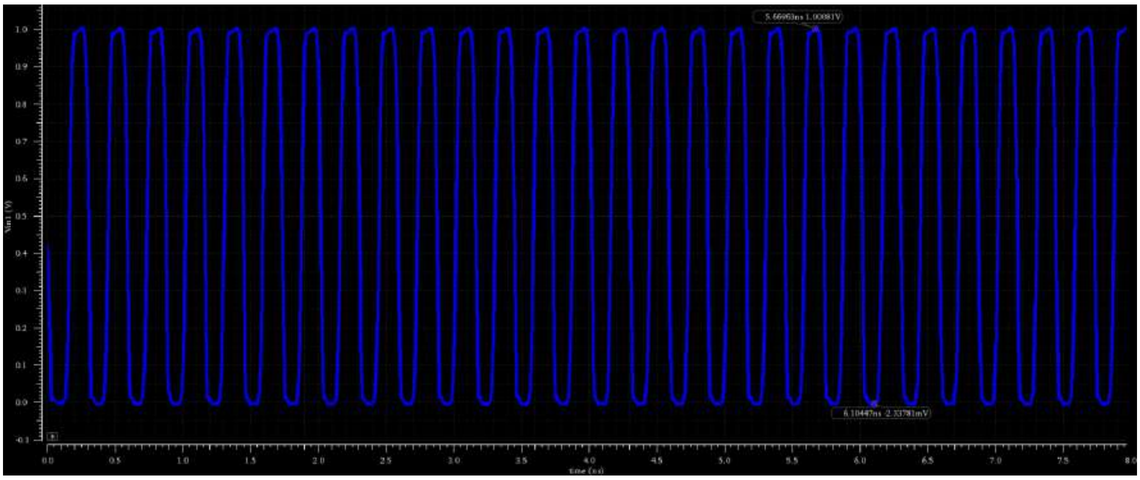


Figure 1.19: Vin1 (input to the PA) of PA + PPA

An important implication of having switching PAs, since their inputs oscillate between Vdd and gnd, we can say:

$$Pout_{max} = \frac{2(Vout1_{max})^2}{2*50} \approx \frac{2(Vdd)^2}{2*50} \Rightarrow Pout_{max} \propto (Vdd)^2$$

Hence, in this case, it can be said: $Vout1 - Vout2 \propto Vdd$

This implies that, when operated at saturation power, the output amplitude of the PA is proportional to the Vdd supply voltage. This paves the way for us to integrate **Amplitude Modulation** into our circuit. Any AM variation can be reflected as a variation of Vdd voltage, and this in turn will be seen as a variation in the amplitude of the output of the PA.

To test this proportionality, we need to slowly vary Vdd for the PA + PPA circuit (from 800mV to 1.2V), and see a linear variation in the output voltage of the PA (Vout1 - Vout2). If the plot is linear, then it provides a confirmation for us to integrate Amplitude Modulation into the Vdd supply node of the PA.

To perform this test, we do a PSS simulation with beat frequency as 3.5GHz, while sweeping the Vdd from 800mV to 1.2mV with a step of 20mV. We then plot the output voltage (Vout1 - Vout2) against Vdd and observe the plot.

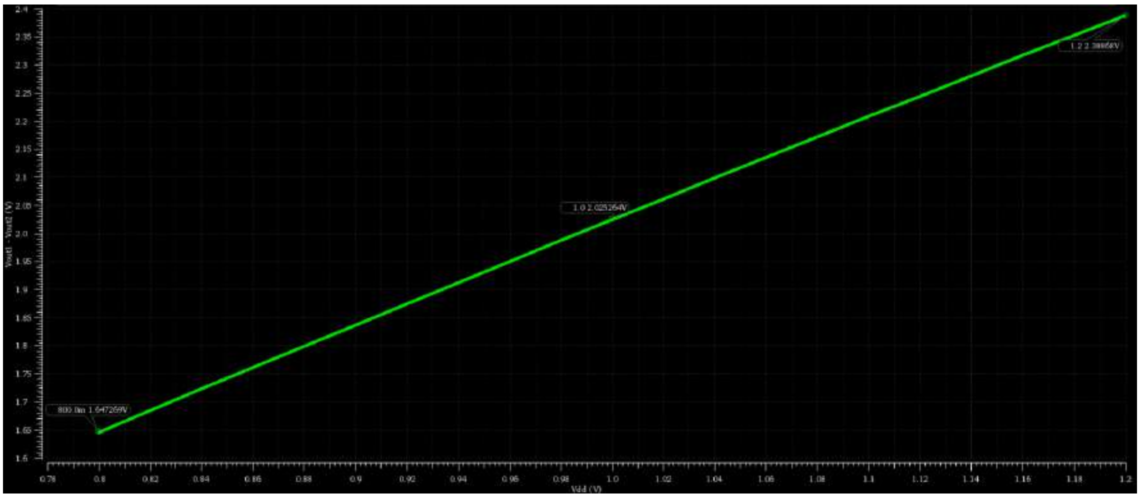


Figure 1.20: Vout vs Vdd for PA + PPA circuit

As observed from the plot, it is a linear curve. Hence, the output of the PA is linearly proportional to the Vdd supply voltage. This means that Amplitude Modulation can be implemented at the Vdd supply of the PA.

1.1.7 Addition of Parasitic Inductances and Capacitances

We will be using QFN packaging to fabricate the chip for our design. Hence, we also need to take into account the effect of the parasitic inductances and capacitances that these fabrication processes might add to the overall design. These consists of **Bond wire** inductances, **Bond pad**, and **PCB pad** capacitances.

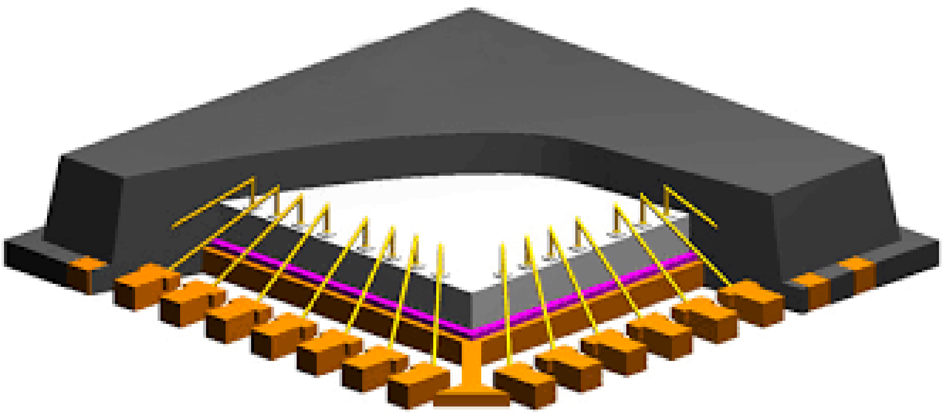


Figure 1.21: QFN Packaging of an IC

The above diagram shows the interior of a QFN packaged IC. The bondwire inductance here is due to the wire (often gold) connecting the IC port to the external port. The Bond pad capacitance occurs the internal IC port, and the PCB pad capacitance occurs at the external port.

Hence, to simulate the effect of these parasitics in Cadence, we need to add these components in the order as shown below, at the input, output, supply and the ground nodes of our circuit. The values of the parasitics used are as follows:
L_bondwire = 2.5nH (with Quality Factor = 30), C_bondpad = 60fF, C_pcbpad = 100fF.

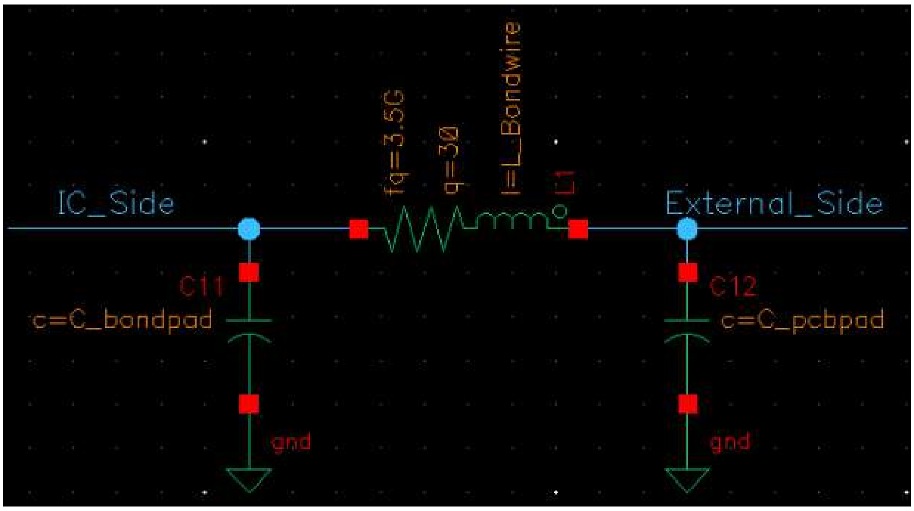


Figure 1.22: Equivalent Circuit to Emulate the Parasitics Function

1.1.8 Integrating Parasitics into PA + PPA Design

The below schematic shows the integration of parasitics into PA + PPA circuit. We haven't integrated the parasitics into the input side of PA + PPA, as there will be another module present that is connected directly to the input of the PA. Hence, we have added parasitics at the output and bias nodes, Vdd supply node, and the ground node. Another point to note, the values of the bond wire inductance at the output node, and for the ground node have been changed as follows:

L_bondwire_output = 1.5nH, L_bondwire_gnd = 800pH, and all other bond wire inductance = 2.5nH.

The reason for this change is that, since the ground node will be the base of the IC, its bond wire inductance will be lower. And for the output case, we deliberately change it to 1.5nH (This can be done by strategically placing the IC in a certain location inside the package) to match the specifications that we require.

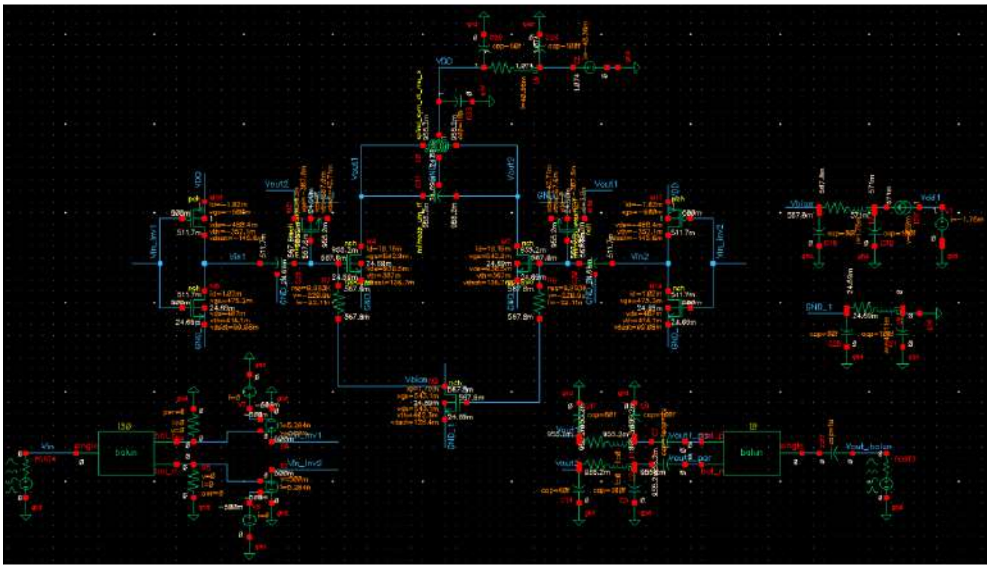


Figure 1.23: PA + PPA schematic with integrated parasitics

The additional parasitic inductors and capacitors create certain changes to our circuit. Firstly, It changes the effective LC tank inductance and capacitance seen at the drains of the NMOS of the PA. Hence, the values for the actual inductor and capacitor present in the LC tank was tweaked a bit, to match the required values. Also, since the output parasitic setup acts like an up-match π network, it increases the differential 100 ohm resistance seen at the output. This also changes the S22 value observed, which also needs to be corrected by tweaking the LC tank inductance and capacitance values. The current LC tank inductance, **Ld = 5.68nH**; LC tank capacitance, **Cd = 403fF**.

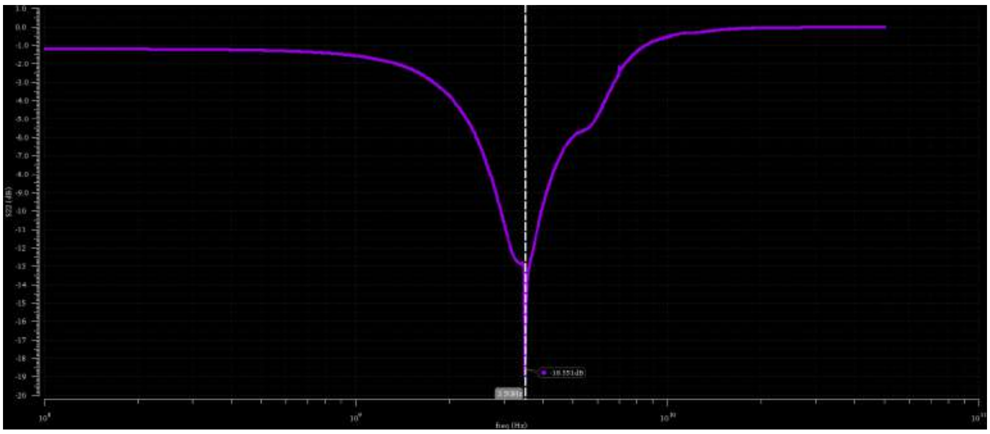


Figure 1.24: S22 Plot of PA + PPA

The above plot shows the S22 of the PA + PPA design after accounting for the changes caused by the bond wire parasitics. For a good design, S22 should lie between -15dB to -20 dB. Our design has an S22 of **-18.551dB** at 3.5GHz.

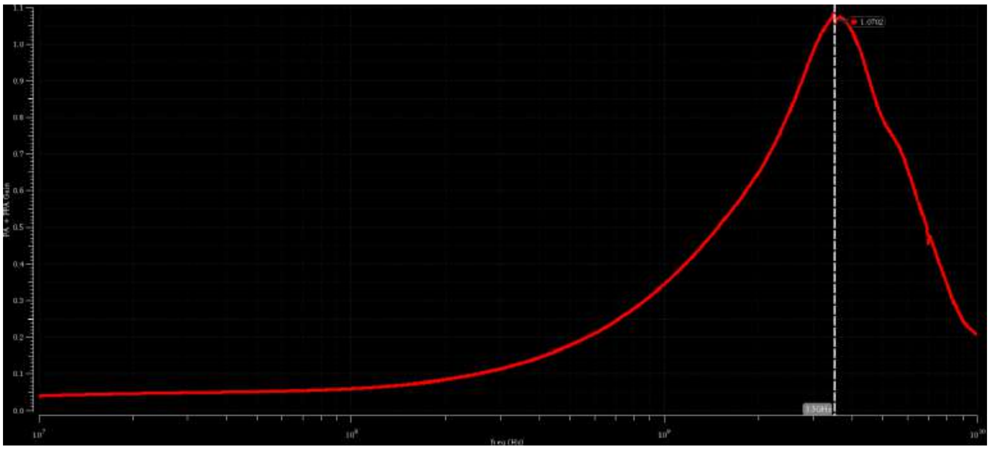


Figure 1.25: Gain Plot of PA + PPA

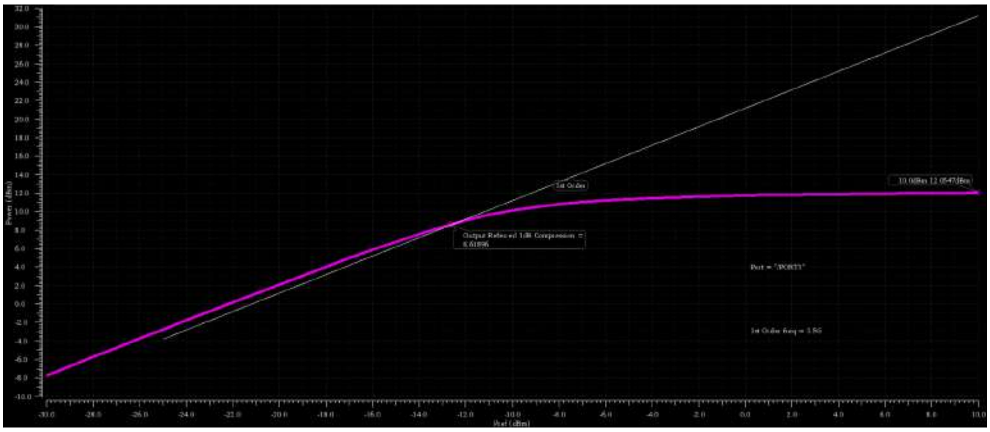


Figure 1.26: Compression Plot of PA + PPA

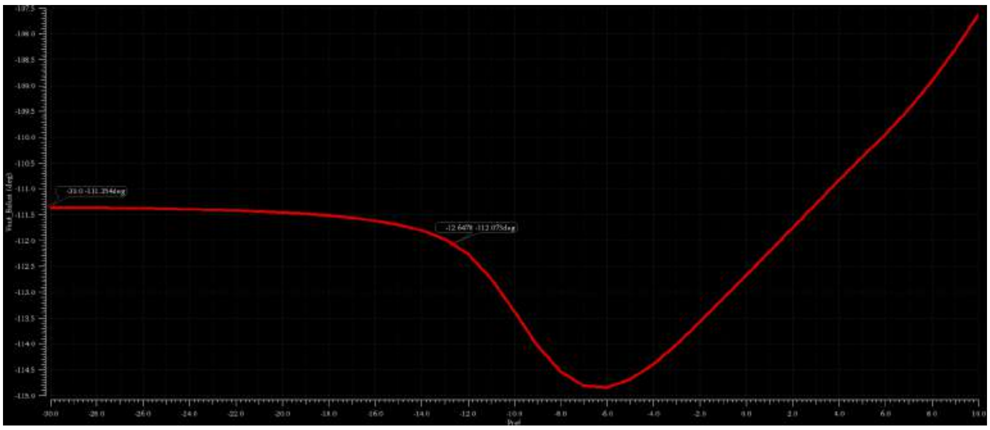


Figure 1.27: Phase Variation Plot of PA + PPA

The above two plots shows the gain, P1dB and phase variation for the PA + PPA design with bond wire parasitics. The gain peaks at 3.5GHz with a gain of **1.07 V/V**. The compression plot has a P1dB of **8.62 dBm**, saturation power of **12.055 dBm**, and phase variation of **0.719**°.

1.1.9 Layout Design for PA + PPA Circuit

Before designing the layout for the PA + PPA circuit, we need to create a schematic and symbol consisting of only the components required for the PA + PPA and create a symbol for that. We also need to make sure all the components are not ideal ones and belong to the TSMC65GP library. The below schematics shows the schematic and symbol for our PA + PPA circuit.

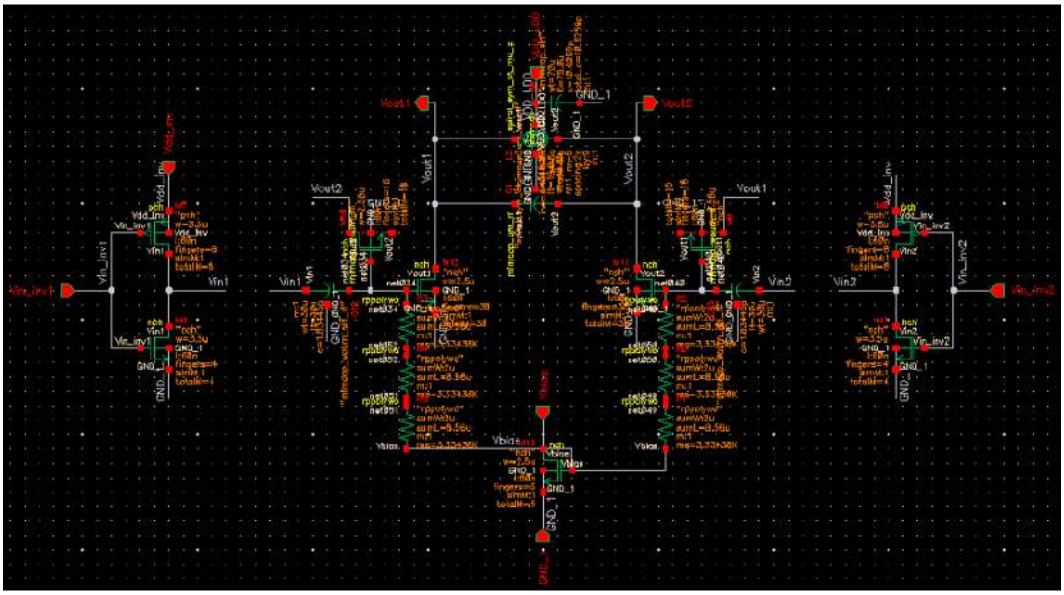


Figure 1.28: Schematic for PA + PPA

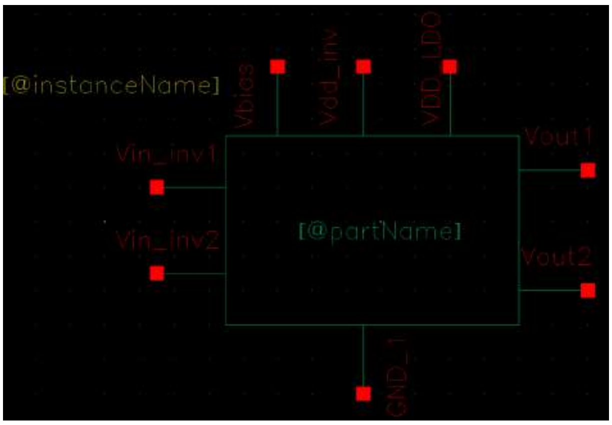


Figure 1.29: Symbol for PA + PPA

In the above schematic, the bias resistor (initially 10KΩ) has been divided into 3 equal resistors (3.33KΩ) in series. This is for optimizing the spacial orientation of the bias resistor during the layout design.

Things to keep in mind while designing the layout for the PA + PPA:

- Higher metal layers have lesser resistance. Hence, for metal layers that carry higher current, wider metal layers need to be used.
- Wider metal layers have lesser resistance and higher capacitance, and vice-versa. This will come in handy when any part of the circuit is resistance/ capacitance dependent.
- For RF Modules, when the frequency is higher, there shouldn't be any sharp 90°turns, rather it should be 45°turn.
- Since, our circuit is differential, we need to make sure our PA + PPA layout needs to be as symmetric as possible.
- All similar MOSFETs should be as close to as possible, so that process variations affect all of them in the same way.

Keeping all the above points in mind, the layout designed for PA + PPA circuit is as shown below.

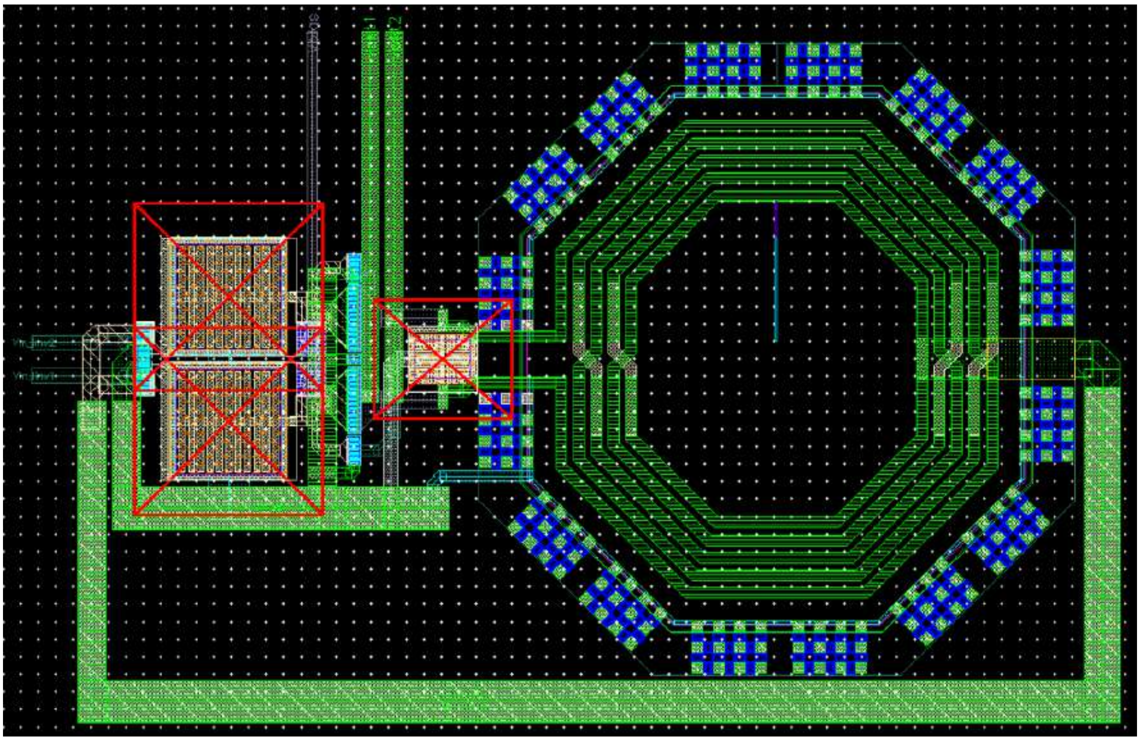


Figure 1.30: Layout Design for PA + PPA Circuit

The input, output, bias and supply nodes of the circuit is as follows:

- **Vin_inv1, Vin_inv2** : Left side of the layout (Inputs).
- **Vbias** : Top side of the layout (Bias node).
- **Vout1, Vout2**: Top side of the layout (Output).
- **GND_1**: Thick rail below bias capacitors (Ground node).
- **VDD**: Thickest Rail at the bottom of the layout (Supply node).

The DRC and LVS success results are as shown below:

Figure 1.31: DRC of Layout Design for PA + PPA Circuit

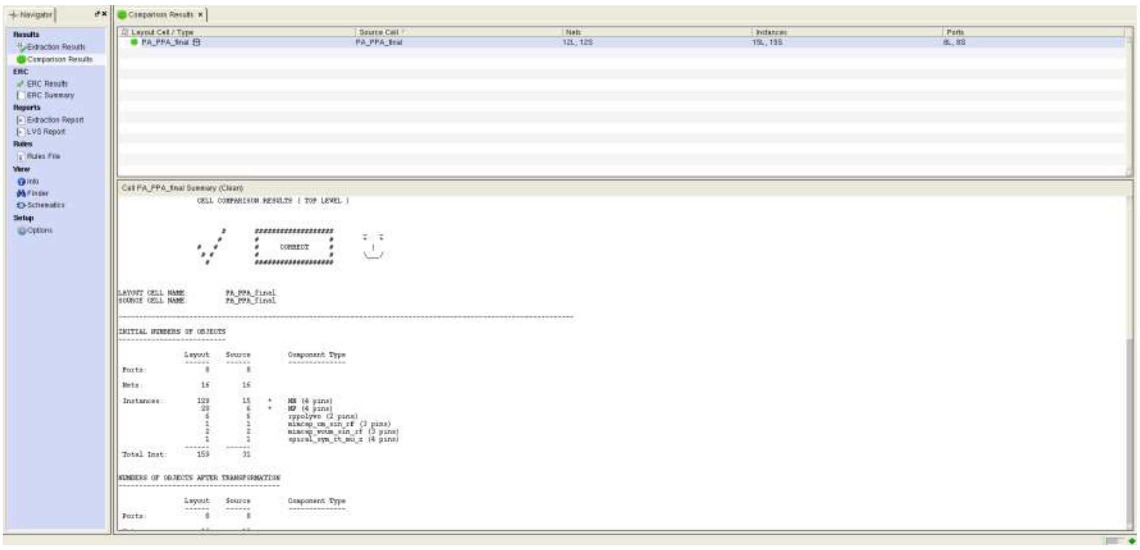


Figure 1.32: LVS of Layout Design for PA + PPA Circuit

A few key features about the above layout design:

- Guard rings have been used for MOSFETs to isolate them from external signals.
- Dummy MOSFETS have been attached at the end of each multi-fingered MOSFETs. This helps in reducing variations among the many fingers of the MOSFETs.
- The differential output rails, as well as VDD and GND_1 rails have multiple metal layers and multiple vias in parallel. This is to reduce the resistance across this lines, as they carry a significantly higher amount of current.

The PEX Success simulation of the above layout design is as shown below.

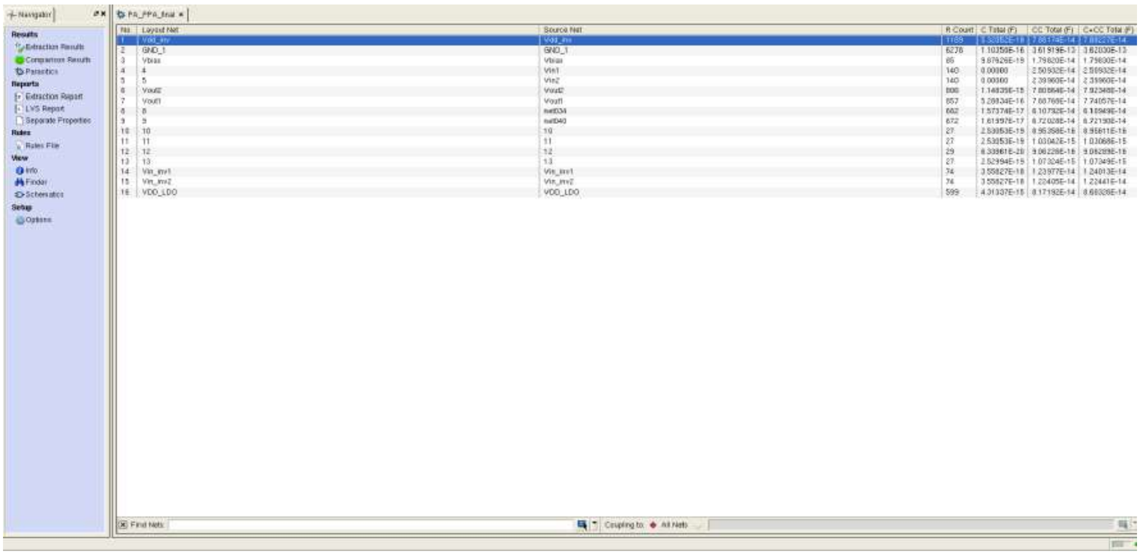


Figure 1.33: PEX of Layout Design for PA + PPA Circuit

A few things to keep in mind while performing PEX simulations:

- We need to enable TICER reduction, and keep it below 10GHz.
- PEX simulation must be performed for both CC extraction, followed by RCC extraction. We first use the CC extract netlist of the PA + PPA and make tweaks to the circuit with respect to that. Once changes have been made, we use the RCC extracted netlist of the PA + PPA, and analyse the circuit, to make sure it meets our required specifications.

After performing simulations with CC extracted netlist, the resonance peak has been shifted a bit, because of the newly added capacitance due to the CC extraction. This can be removed by tweaking the inductances and capacitance at the LC tank of the PA to recover the resonance back at 3.5GHz. Hence, the new value of the LC tank inductance is **4.19nH**, and the LC tank capacitance is **348.1fF**.

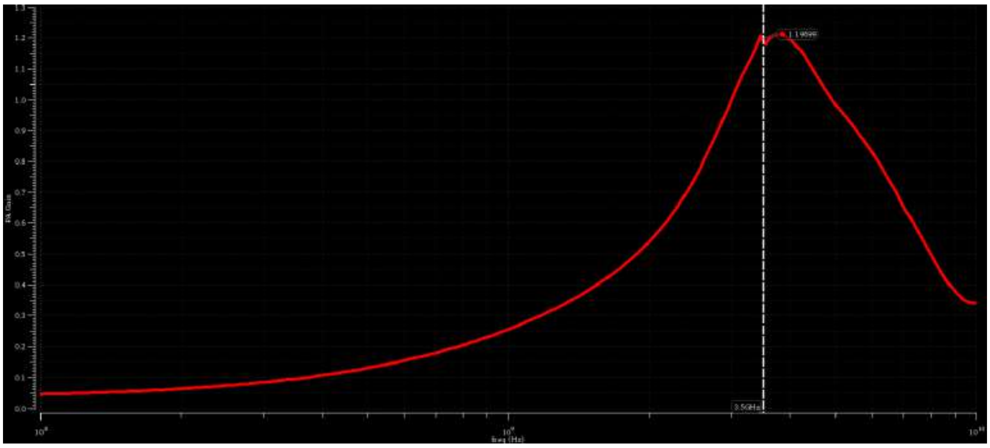


Figure 1.34: Gain Plot of CC extracted netlist for PA + PPA

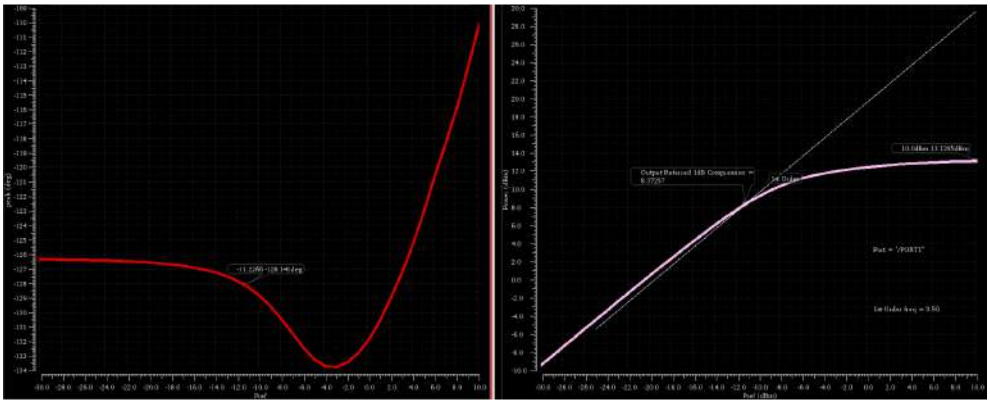


Figure 1.35: Compression and Phase Variation Plot of CC extracted netlist for PA + PPA

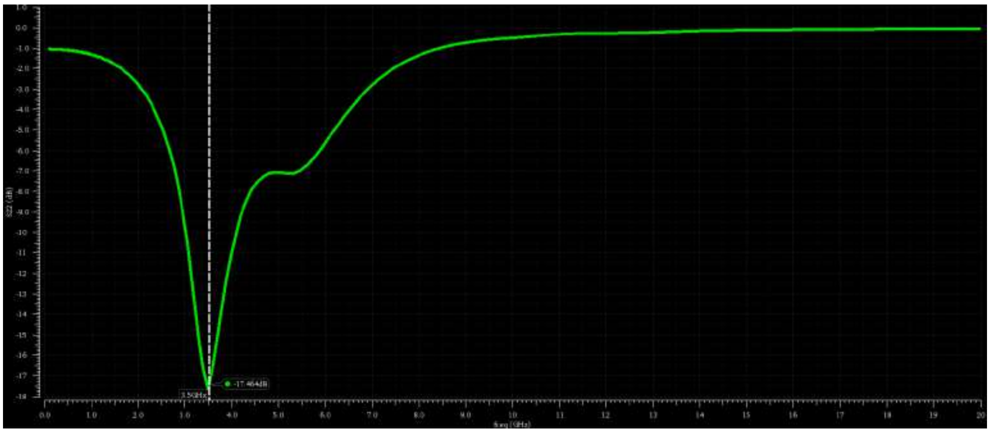


Figure 1.36: S22 Plot of CC extracted netlist for PA + PPA

The above are the plots showing the specifications of the **CC extraced netlist** for the PA + PPA. It has a PA gain of **1.197 V/V**, and S22 of **-17.46 dB** at 3.5GHz, P1db of **8.37 dBm**, with saturation power of **13.1285 dBm**, and phase variation of **1.68**°.

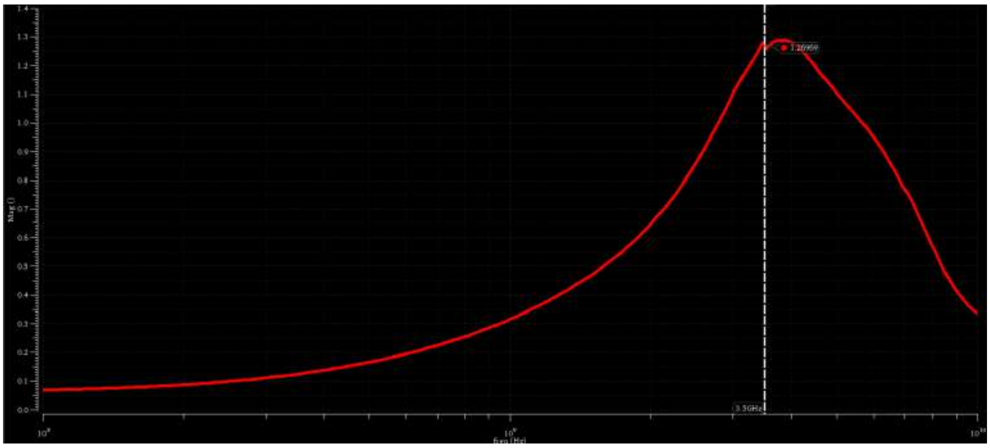


Figure 1.37: Gain Plot of CC extracted netlist for PA + PPA

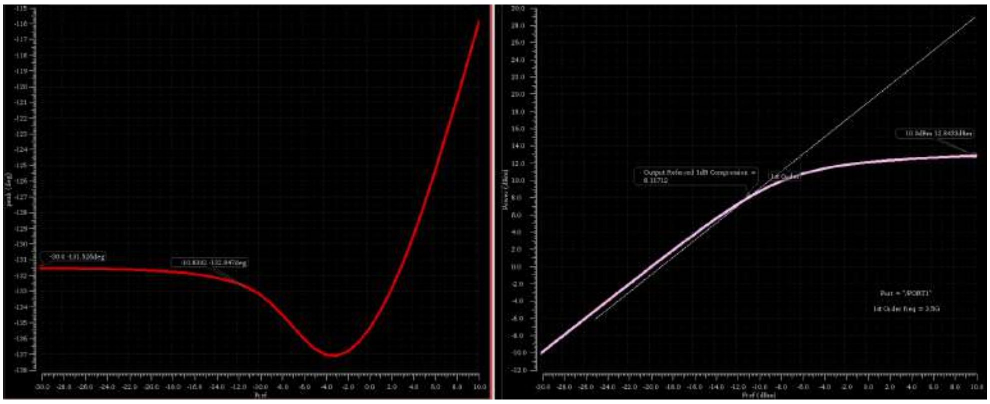


Figure 1.38: Compression and Phase Variation Plot of CC extracted netlist for PA + PPA

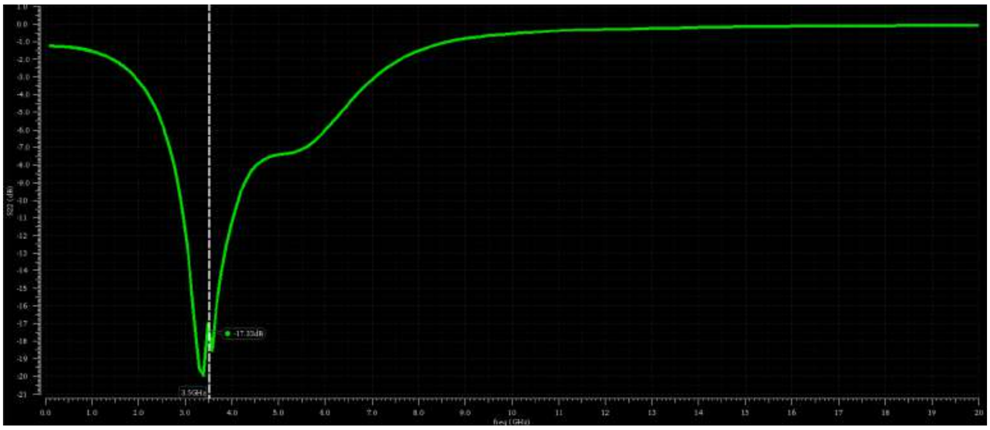


Figure 1.39: S22 Plot of CC extracted netlist for PA + PPA

The above are the plots showing the specifications of the **RCC extraced netlist** for the PA + PPA. It has a PA gain of **1.27 V/V**, and S22 of **-17.33 dB** at 3.5GHz, P1db of **8.117 dBm**, with saturation power of **12.843 dBm**, and phase variation of **1.32**°.

1.2 Design of LDO for Amplitude Modulation

The Low Dropout Regulator (LDO) is used to implement Amplitude Modulation (AM) for the PA + PPA setup. LDOs are generally used to regulate votlages at a specific value, so its devoid of any external influence. The PA + PPA input will contain Phase Modulated (PM) signals, whereas the AM signals will come from the input of the LDO, and this will be supplied to the supply node (VDD) of the PA. In our since, because of the switching nature of the PA, the differential output of the PA is directly proportional to the supply voltage signal, and hence, AM can be implemented into the PA by this method.

1.2.1 Design of a Basic LDO Circuit

Let us start with a basic design of the LDO. The diagram below shows the basic schematic for the LDO. Here, the AM signal input is at Vref, which is a sinusoidal signal at 100MHz, with V_{dc} = 1V, and amplitude = 200mV (Oscillates between 0.8V and 1.2V), and Vout will be connected to the supply node (VDD) of the PA.

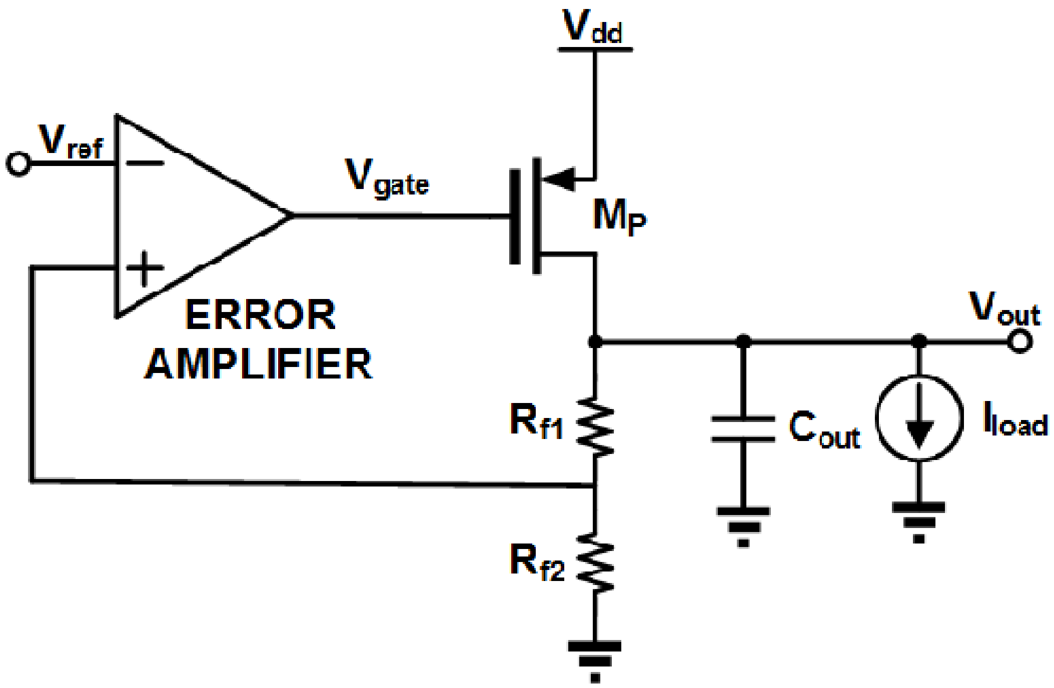


Figure 1.40: Basic Circuit Diagram of LDO

To find out the load at the output of the LDO, we need to find the Zout of the PA.

We can do this by attaching a Vdc = 1V (AC magnitude = 1V) at the supply node of the PA, performing Hb + Hbac analysis and finding out the current at this node. From here

$$Zout = \frac{1V}{I_{real} + jI_{imaginary}}$$

We can find the Rout and Cout at the frequency of 3.5GHz, and that would be out load for the LDO. By performing the above simulations, we got Rout as **16.86**Ω and Cout as **5.35pF**.

We start the design of the above basic LDO circuit in Cadence, to test the functionality of the LDO. We can use a VCCS to mimic the functionality of the opamp in the above case.

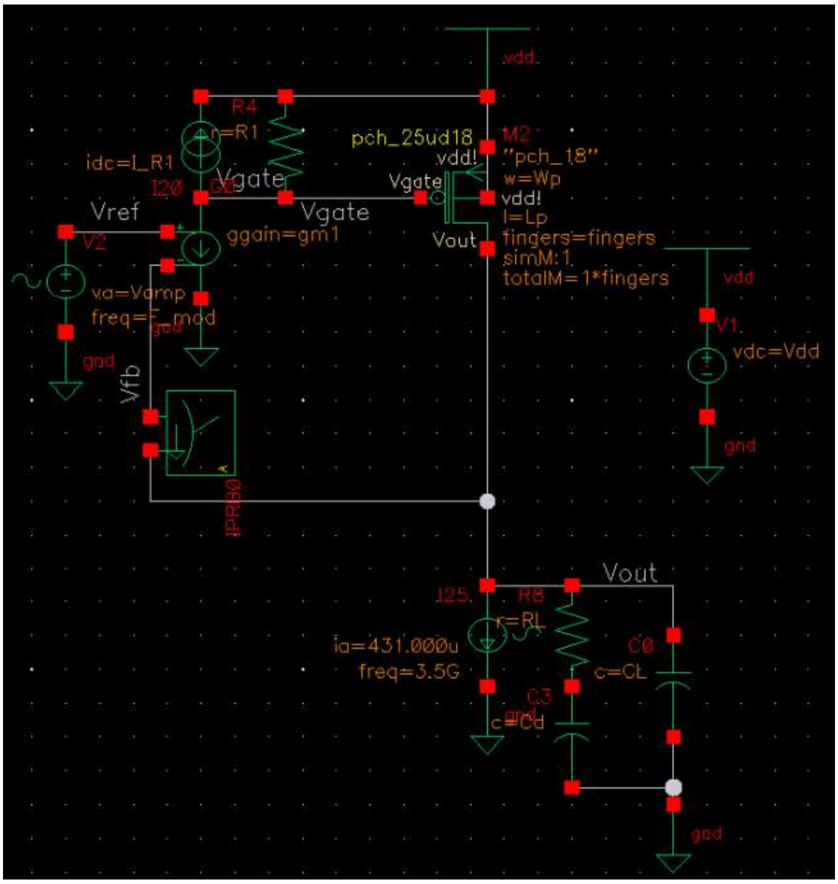
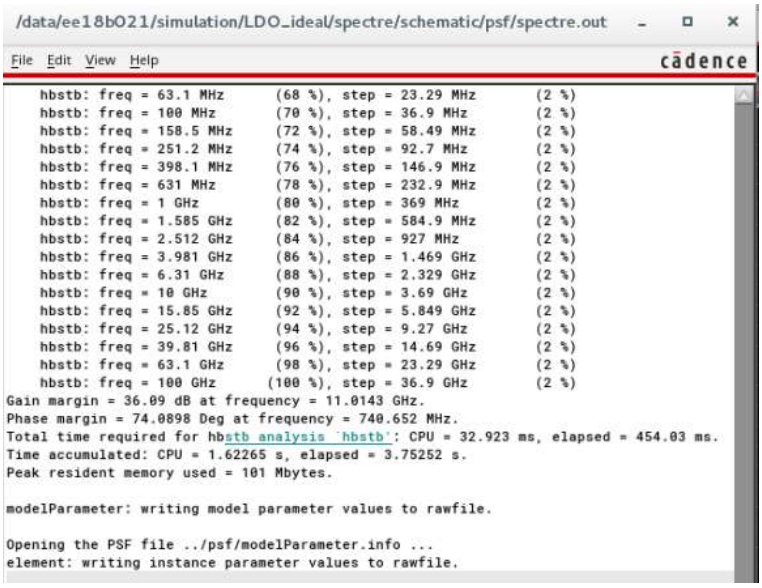


Figure 1.41: Basic Schematic of LDO

The VCCS + resistor (R1) + DC current source mimics the functioning of the opamp in the above case. The load resistance, load capacitance and total current through the LC tank of the PA are all connected at the output of the LDO. We are using **nch_25ud18** and **pch_25ud18** for the design of the LDO, as they can withstand the higher **VDD of 1.8V**. For this circuit, we would like to have a gain of atleast **25 V/V** with a Phase Margin (PM) of atleast **60°**.

Figure 1.42: Transient Plot for LDO



/data/ee18b021/simulation/LDO_ideal/spectre/schematic/psf/spectre.out

File Edit View Help cādence

```
    hbstb: freq = 63.1 MHz       (68 %), step = 23.29 MHz       (2 %)
    hbstb: freq = 100 MHz        (70 %), step = 36.9 MHz        (2 %)
    hbstb: freq = 158.5 MHz      (72 %), step = 58.49 MHz       (2 %)
    hbstb: freq = 251.2 MHz      (74 %), step = 92.7 MHz        (2 %)
    hbstb: freq = 398.1 MHz      (76 %), step = 146.9 MHz       (2 %)
    hbstb: freq = 631 MHz        (78 %), step = 232.9 MHz       (2 %)
    hbstb: freq = 1 GHz          (80 %), step = 369 MHz         (2 %)
    hbstb: freq = 1.585 GHz      (82 %), step = 584.9 MHz       (2 %)
    hbstb: freq = 2.512 GHz      (84 %), step = 927 MHz         (2 %)
    hbstb: freq = 3.981 GHz      (86 %), step = 1.469 GHz       (2 %)
    hbstb: freq = 6.31 GHz       (88 %), step = 2.329 GHz       (2 %)
    hbstb: freq = 10 GHz         (90 %), step = 3.69 GHz        (2 %)
    hbstb: freq = 15.85 GHz      (92 %), step = 5.849 GHz       (2 %)
    hbstb: freq = 25.12 GHz      (94 %), step = 9.27 GHz        (2 %)
    hbstb: freq = 39.81 GHz      (96 %), step = 14.69 GHz       (2 %)
    hbstb: freq = 63.1 GHz       (98 %), step = 23.29 GHz       (2 %)
    hbstb: freq = 100 GHz       (100 %), step = 36.9 GHz        (2 %)
Gain margin = 36.09 dB at frequency = 11.0143 GHz.
Phase margin = 74.0898 Deg at frequency = 740.652 MHz.
Total time required for hbstb analysis `hbstb': CPU = 32.923 ms, elapsed = 454.03 ms.
Time accumulated: CPU = 1.62265 s, elapsed = 3.75252 s.
Peak resident memory used = 101 Mbytes.

modelParameter: writing model parameter values to rawfile.

Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.
```

Figure 1.43: Phase Margin for LDO

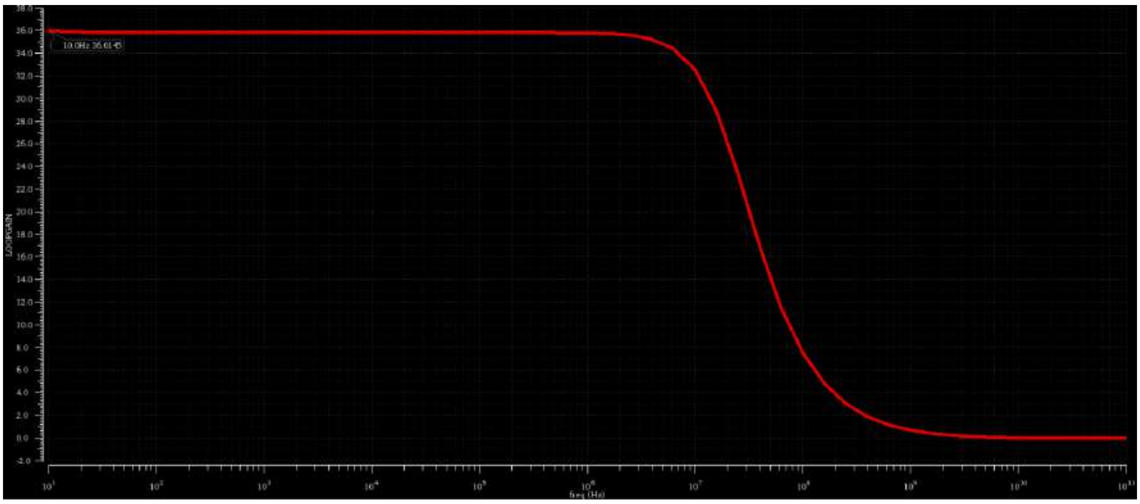


Figure 1.44: Loop Gain Magnitude Plot for LDO

The above plot shows the transient analysis plot, the Phase Margin, as well as the Loop Gain plots for the basic LDO design. As we can see, the loop has a gain magnitude of **36.0145 V/V**, with a PM of **74.09**° at a unity gain frequency **740.652MHz**.

1.2.2 Design of LDO with 1-stage Opamp

We can move ahead with the design, by replacing the ideal opamp, with a custom 1-stage opamp, using TSMC65GP MOSFETs. We want an overall gain of atleast **20 V/V** for the Opamp, with an output resistance of atleast **4K**Ω. The schematic for the LDO circuit with 1-stage opamp is as shown below.

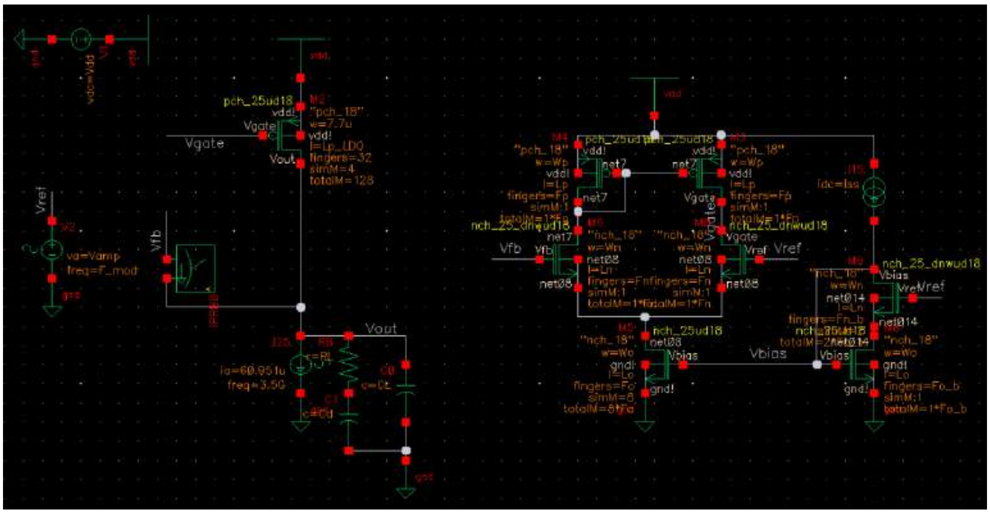


Figure 1.45: Schematic of LDO with Opamp

The opamp differential NMOS and the current mirror NMOS is made using TSMC **nch_25_dnwud18**. These are deep nwell NMOS. These are necessary here, as these specific NMOS have a non-ground bulk connection, hence, needs a separate substrate connection. The deep nwell will facilitate such a connection. This opamp has a gm of **7.34mS**, Rout of **2.95K**Ω, and a total gain of **21.9 V/V**.

The Below plots shows the transient plots of Vref and Vout, the Phase Margin, and the loop gain of the LDO. The loop gain magnitude is **30.197 V/V** or **29.6 dB**, with a PM of **65.783**° at a unity gain frequency of **624.91MHz**.

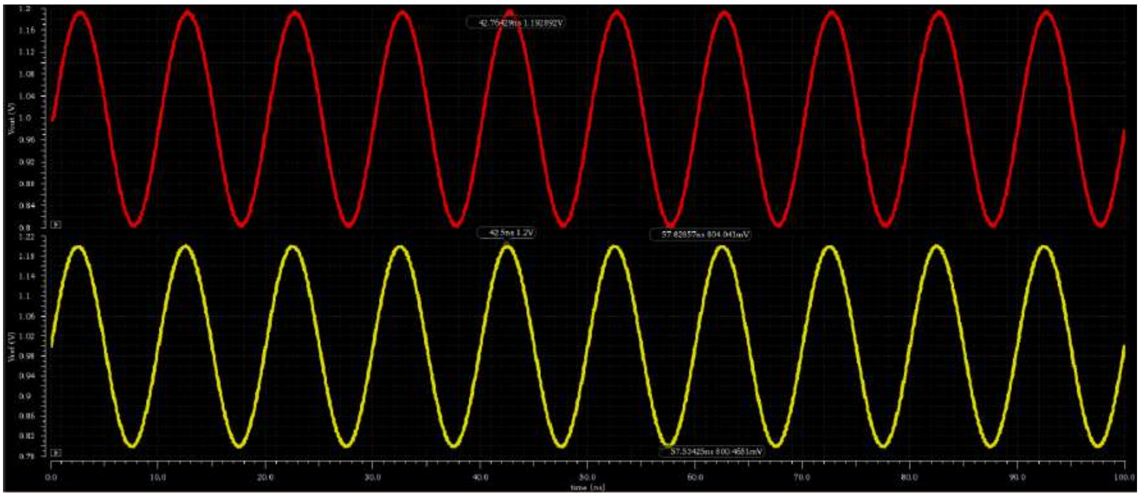


Figure 1.46: Transient Plot for LDO with Opamp

```
    hbstb: freq = 666.8 GHz   (98.4 %), step = 16.68 GHz    (100 m%)
    hbstb: freq = 683.9 GHz   (98.5 %), step = 17.1 GHz     (100 m%)
    hbstb: freq = 701.5 GHz   (98.6 %), step = 17.54 GHz    (100 m%)
    hbstb: freq = 719.4 GHz   (98.7 %), step = 17.99 GHz    (100 m%)
    hbstb: freq = 737.9 GHz   (98.8 %), step = 18.46 GHz    (100 m%)
    hbstb: freq = 756.8 GHz   (98.9 %), step = 18.93 GHz    (100 m%)
    hbstb: freq = 776.2 GHz     (99 %), step = 19.41 GHz    (100 m%)
    hbstb: freq = 796.2 GHz   (99.1 %), step = 19.91 GHz    (100 m%)
    hbstb: freq = 816.6 GHz   (99.2 %), step = 20.42 GHz    (100 m%)
    hbstb: freq = 837.5 GHz   (99.3 %), step = 20.95 GHz    (100 m%)
    hbstb: freq = 859 GHz     (99.4 %), step = 21.48 GHz    (100 m%)
    hbstb: freq = 881 GHz     (99.5 %), step = 22.04 GHz    (100 m%)
    hbstb: freq = 903.6 GHz   (99.6 %), step = 22.6 GHz     (100 m%)
    hbstb: freq = 926.8 GHz   (99.7 %), step = 23.18 GHz    (100 m%)
    hbstb: freq = 950.6 GHz   (99.8 %), step = 23.77 GHz    (100 m%)
    hbstb: freq = 975 GHz     (99.9 %), step = 24.38 GHz    (100 m%)
    hbstb: freq = 1 THz        (100 %), step = 25.01 GHz    (100 m%)
Gain margin = 20.9242 dB at frequency = 2.98454 GHz.
Phase margin = 65.7827 Deg at frequency = 624.908 MHz.
Total time required for hbstb analysis `hbstb': CPU = 5.95701 s, elapsed = 6.31638 s.
Time accumulated: CPU = 8.39362 s, elapsed = 9.96531 s.
Peak resident memory used = 99.9 Mbytes.

modelParameter: writing model parameter values to rawfile.

Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.
```

Figure 1.47: Phase Margin for LDO with Opamp

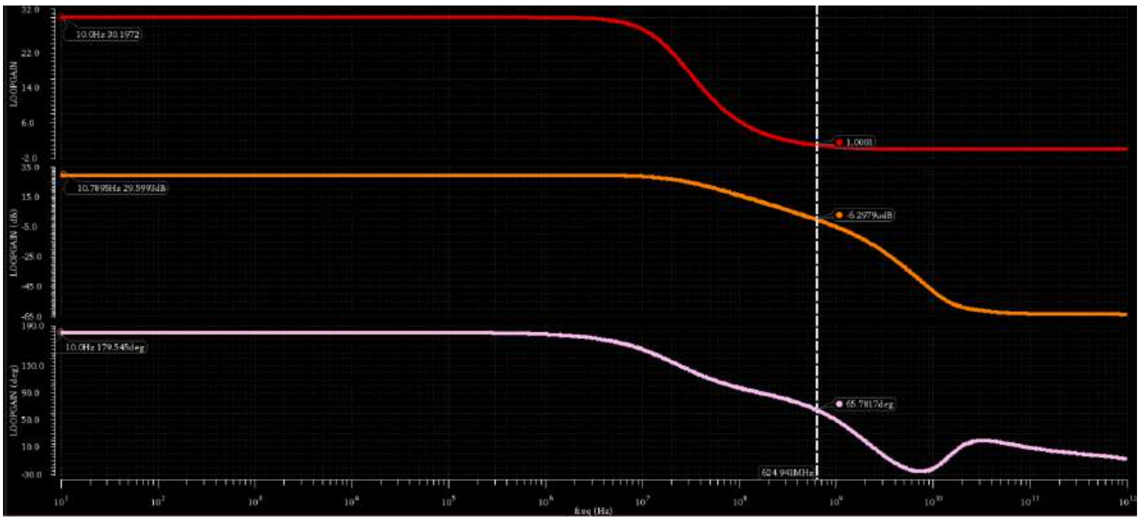


Figure 1.48: Loop Gain Plot for LDO with Opamp

Along with the above simulations, the LDO circuit with 1-stage opamp needs to be tested across process corners (SS, TT and FF), and we need to make sure that all MOSFETs remain in saturation. The key setup where the MOSFETs could get out of saturation are:

- When Vref = 0.8V, and the process corner is SS.
- When Vref = 1.2V, and the process corner is FF.

When simulated and analysed in Cadence, The NMOS M9 goes out of saturation (into the linear region) when Vref = 1.2V, and the process corner is FF. This is a problem, hence, we need to do something about it.

1.2.3 Final Design of the LDO circuit

The reason for NMOS M9 to get out of saturation is that its drain voltage is limited by the gate voltage of NMOS M5, due to the negative feedback present in the bias part of the opamp. Hence, the Vds of NMOS M9 becomes very less compared to Vdsat of NMOS M9. To resolve this issue, we can add an opamp in this particular negative feedback loop, so that the drain voltage of NMOS M9 can be fixed at a higher voltage value that we want it to be at. This way, even at the process corner FF, when Vref = 1.2V, the NMOS M9 will not go into saturation.

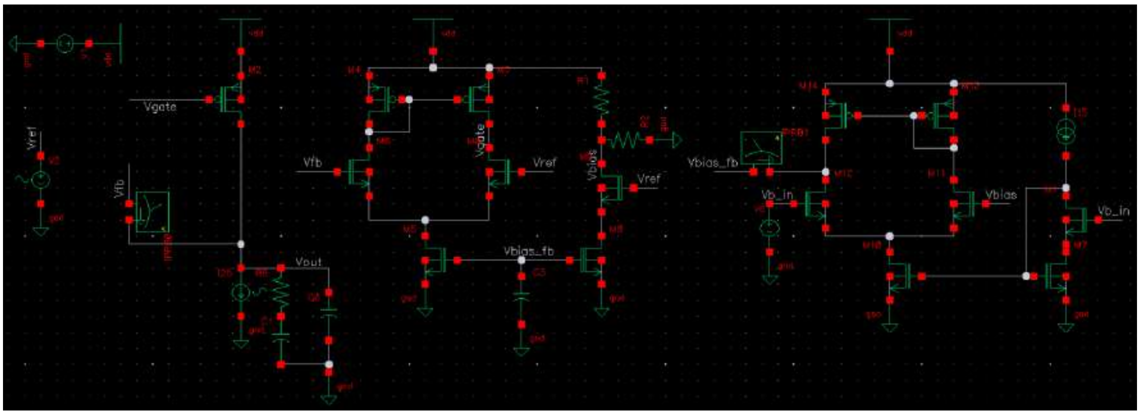


Figure 1.49: Schematic of Final Design of LDO

The above circuit shows the final design of the LDO. The rightmost opamp is for the bias negative feedback loop. This design of the LDO has all MOSFETs in saturation region across all the process corners, and across the entire range of Vref. Additionally, the bias current source in the main loop opamp has been replaced by a resistive divider, as for the right resistance, a resistor also acts like a current source, providing the required current. This replacement is because, an ideal current source exhibits infinite resistance, causing problems with the poles in the loop gain plots. We also added a capacitor of 412.84fF at *Vbias_fb* node to adjust the dominant pole for a higher Phase Margin.

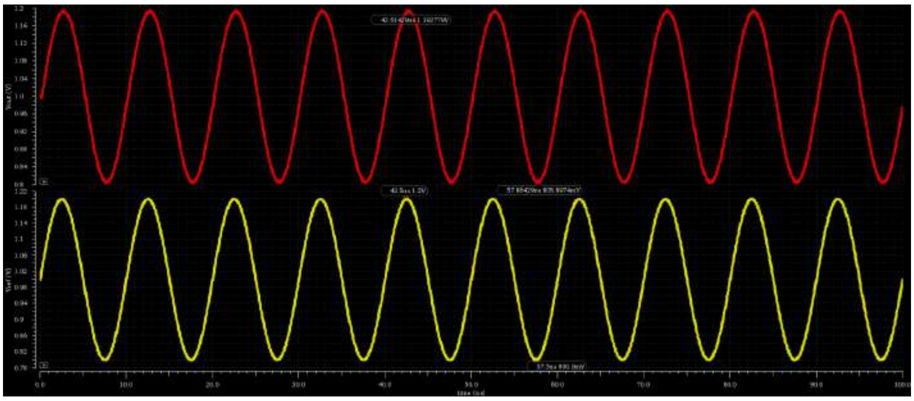


Figure 1.50: Transient Plot for Final Design of LDO

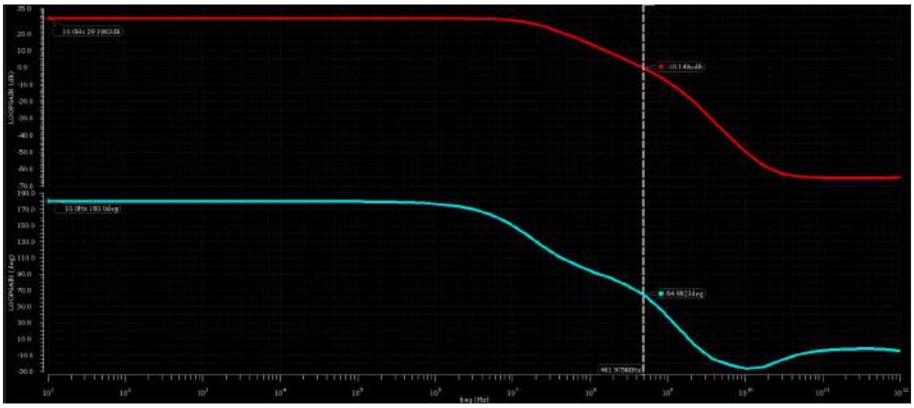


Figure 1.51: Bias loop Loof Gain Plot for Final Design of LDO

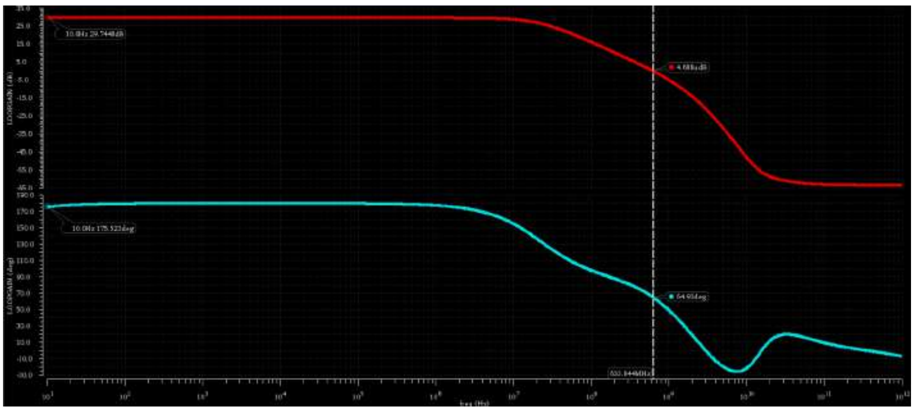


Figure 1.52: Loop Gain Plot for Final Design of LDO

The above plots show the transient plots of Vref and Vout, the loop gain plot for the bias loop and the main loop of the LDO. The bias loop has a gain magnitude of **28.834 V/V** or **29.2 dB**, and a PM of **65.12°** at a unity gain frequency of **478.5MHz**. The main loop gain magnitude is **30.71 V/V** or **29.745 dB**, with a PM of **64.93°** at a unity gain frequency of **633.816MHz**.

1.2.4 Layout Design of LDO

We start the layout design by first creating a schematic consisting of only the LDO components, all of them from the TSMC65GP library, and a symbol for the same.

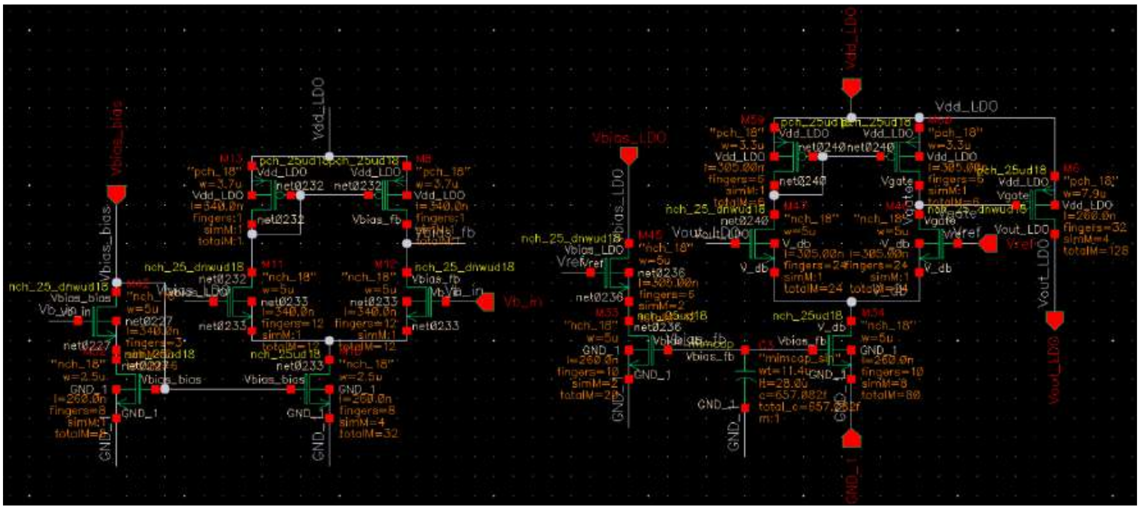


Figure 1.53: Schematic for LDO

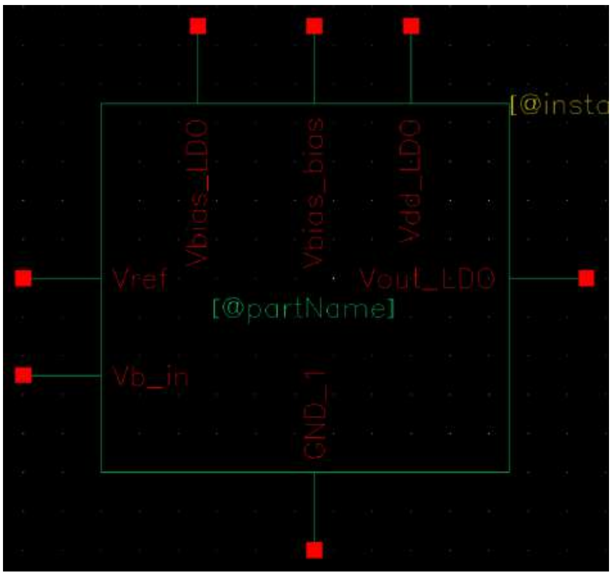


Figure 1.54: Symbol for LDO

The layout of the LDO circuit is as shown below.

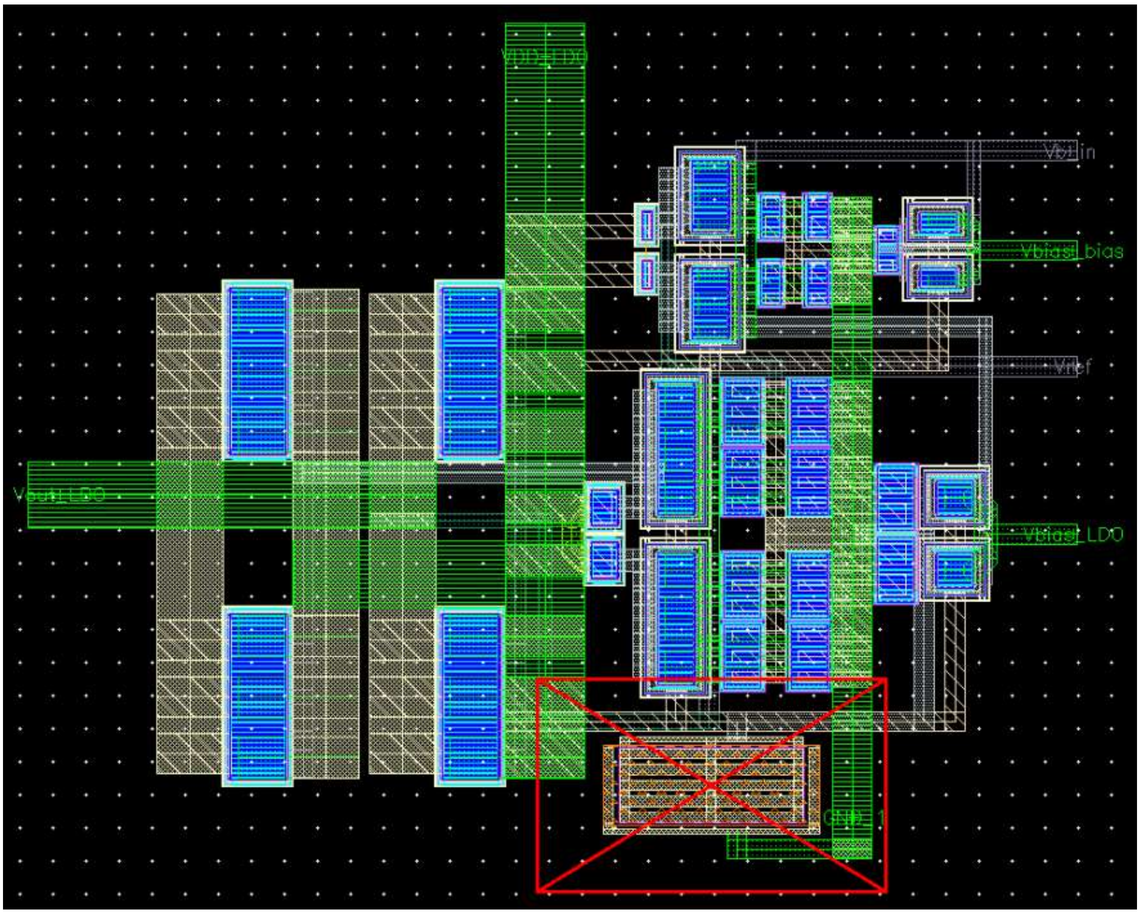


Figure 1.55: Layout for LDO

The input, output, bias and supply nodes of the circuit is as follows:

- **Vb_in, Vref** : Right side of the layout (Metal 4)(Inputs).
- **Vbias_LDO, Vbias_bias** : Right side of the layout (Metal 7)(Bias node).
- **Vout_LDO**: Left side of the layout (Output).
- **GND_1**: Metal 9 rail present vertically between MOSFETs towards the right (Ground node).
- **VDD_LDO**: Thickest Rail present vertically between MOSFETs (Supply node).

Another key feature to note in the above layout for the LDO is the new type of guard ring for the deep nwell NMOS. This guard ring contains a p-sub guard ring surrounded by an n-well guard ring with a deep nwell boundary around it. This is to properly design the deep nwell structure to isolate this NMOS from the surrounding components.

The DRC, LVS and PEX success results for the above layout are as shown below.

Figure 1.56: DRC of Layout Design for LDO Circuit

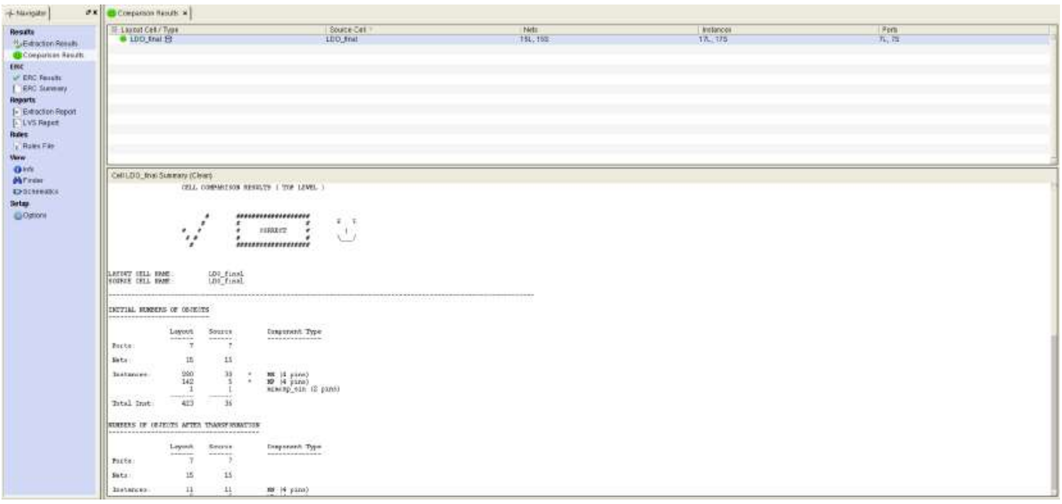


Figure 1.57: LVS of Layout Design for LDO Circuit

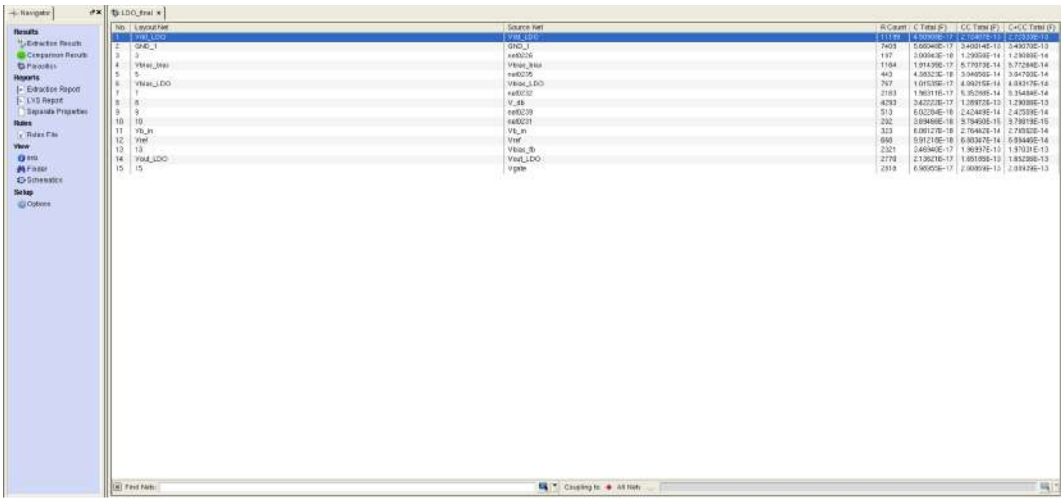


Figure 1.58: PEX of Layout Design for LDO Circuit

To test the RCC extracted netlist, we will need to test for loop gains and phase margins for the main loop and the bias loop of the LDO. Hence, we create another layout that brings out more nodes so that both the loops can be analysed without any issues. The below circuit shows the testbench with the LDO module with more pins. This can be used to analyse the circuit better. We will use this circuit to analyse the loops and other properties of the RCC extracted version of the LDO.

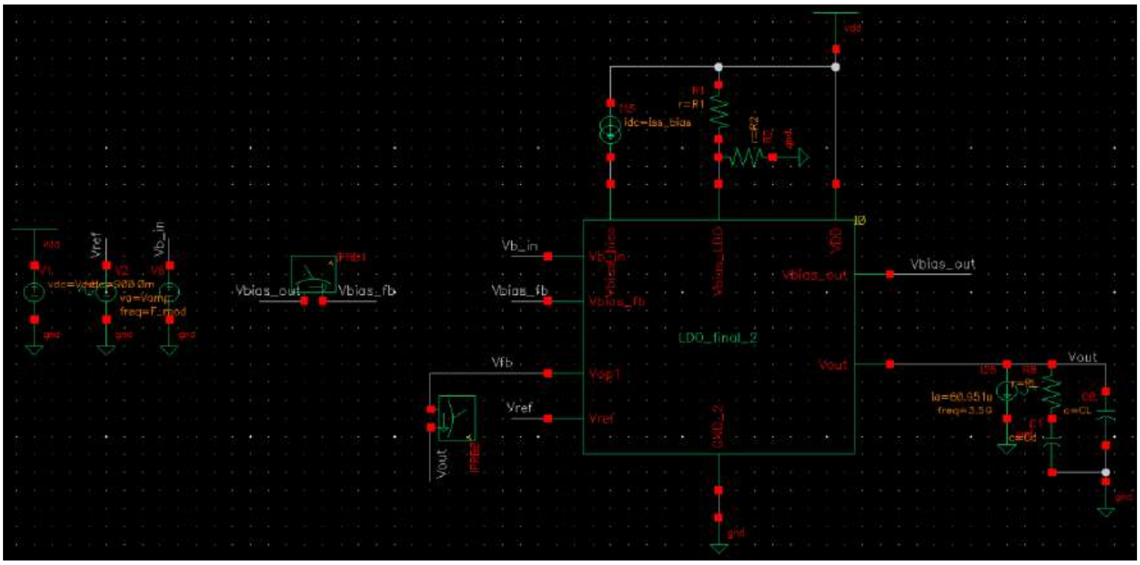


Figure 1.59: Schematic of Testbench for the LDO

The below plots show the transient plots of Vref and Vout, the loop gain plot for the bias loop and the main loop of the LDO. The bias loop has a gain magnitude of **30.47 V/V** or **29.6775 dB**, and a PM of **63.012°** at a unity gain frequency of **391.23MHz**. The main loop gain magnitude is **29.925 V/V** or **29.521 dB**, with a PM of **64.79°** at a unity gain frequency of **544.14MHz**.

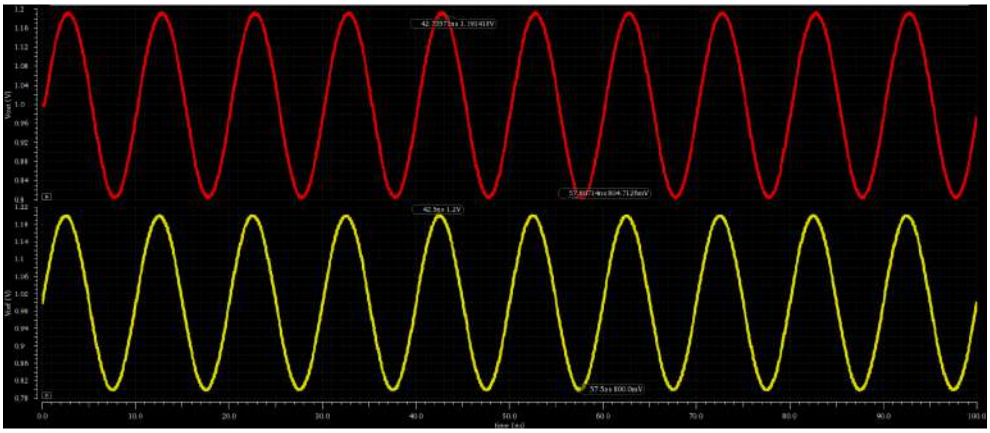


Figure 1.60: Transient Plot for RCC extracted netlist of LDO

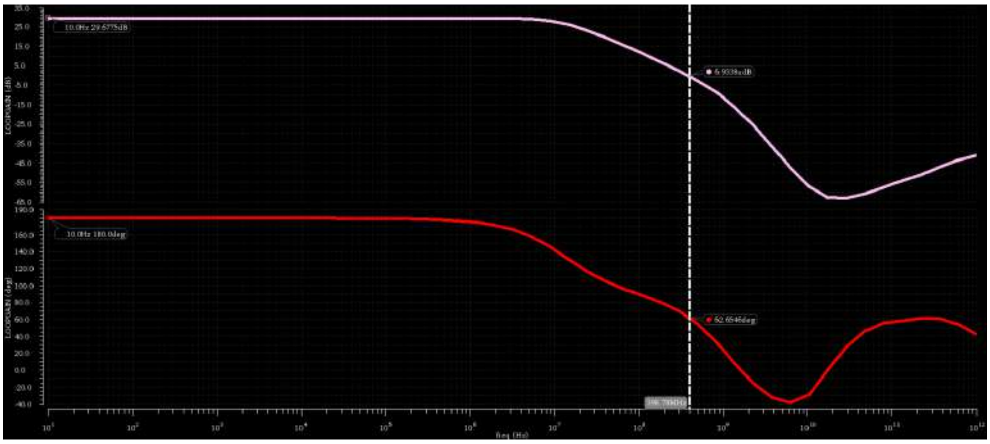


Figure 1.61: Bias Loop Gain Plot for RCC extracted netlist of LDO

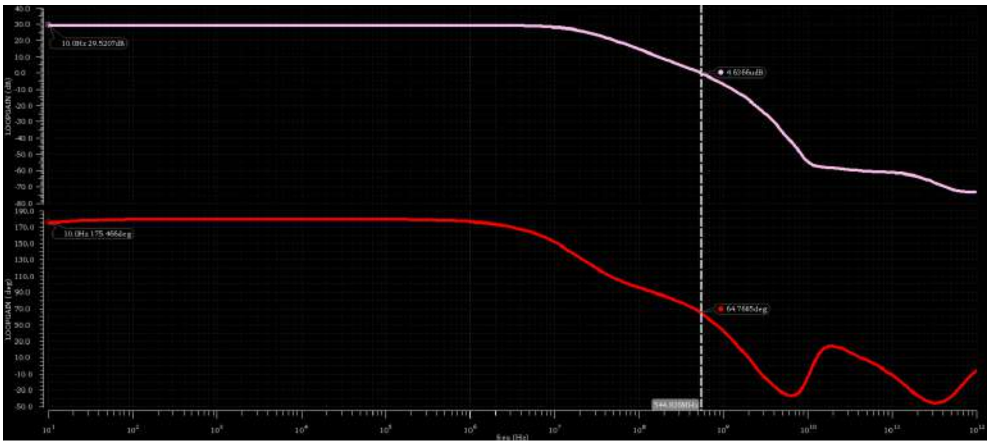


Figure 1.62: Loop Gain Plot for RCC extracted netlist of LDO

1.3 Integration of PA + PPA and LDO

Since both the PA + PPA and the LDO modules have been designed, including their layouts and RCC extracted netlist, we can move ahead with integrating both these modules. The below schematic shows the integration of both the modules.

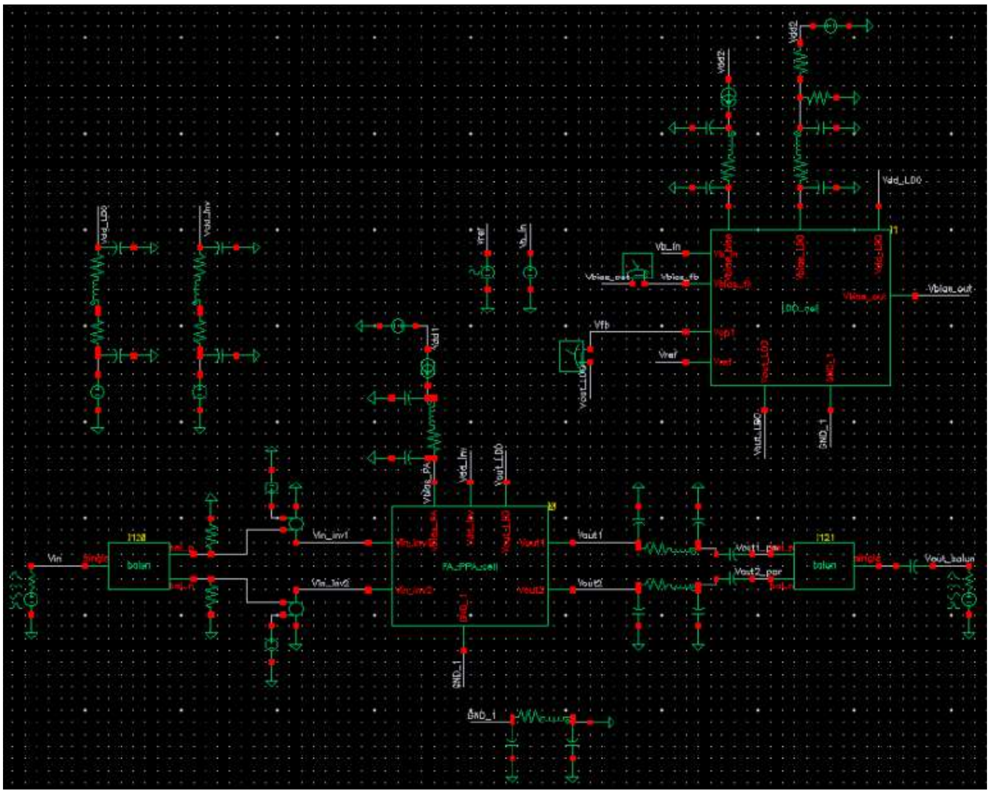


Figure 1.63: Schematic of Testbench for the LDO

The below plots show the transient plots of Vref and Vout_LDO and Vout_balun, the loop gain plot for the bias loop and the main loop of the LDO. The bias loop has a gain magnitude of **30.67 V/V** or **29.734 dB**, and a PM of **62.367°** at a unity gain frequency of **400.58MHz**. The main loop gain magnitude is **18.8 dB**, with a PM of **86.91°** at a unity gain frequency of **454.513MHz**.

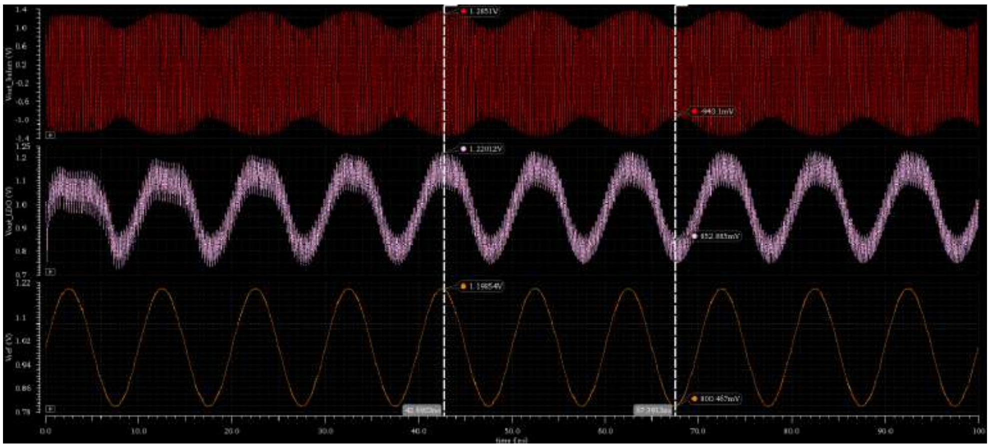


Figure 1.64: Transient Plot of PA + PPA + LDO

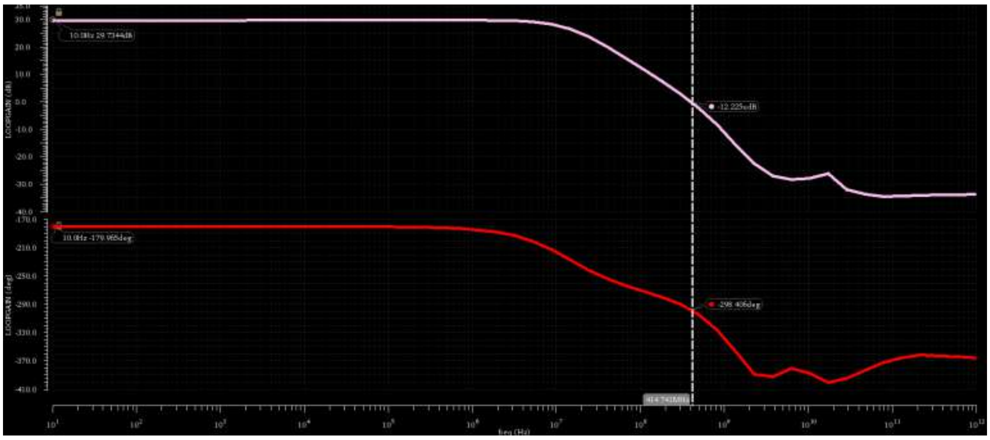


Figure 1.65: Bias Loop Gain Plot of PA + PPA + LDO

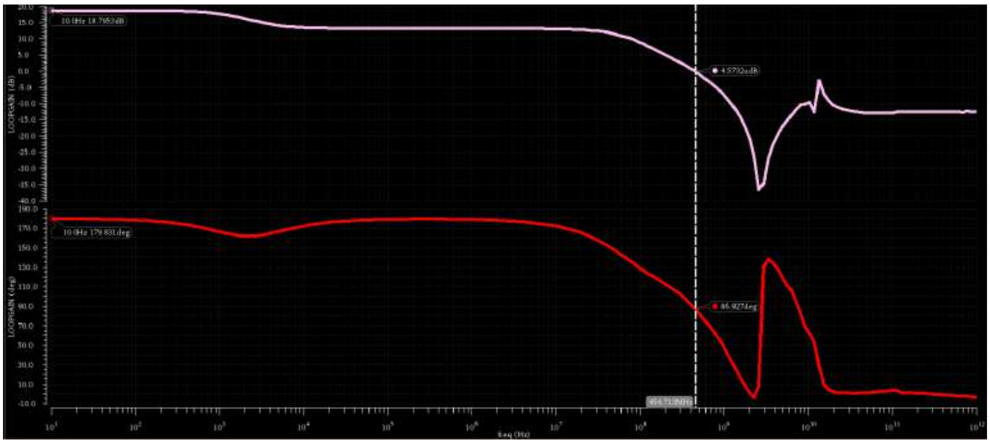


Figure 1.66: Loop Gain Plot of PA + PPA + LDO

An addition to the above circuit is the large capacitors and resistors at the supply nodes of the circuit, namely Vdd_LDO and Vdd_inv. The capacitors act as decoupling capacitors, blocking the higher frequencies present at the Vdd nodes, and the resistors are used as a damping factor to the Vdd nodes. Currently we have attached capacitors of **20pF** at Vdd_LDO and Vdd_inv nodes respectively. These capacitors are made of MOSFETs, known as mos capacitors (Moscaps). We will look into the design of this moscap in the next section. We have also attached, in series to the bond wire inductance, resistors of resistance **60**Ω and **100**Ω at Vdd_LDO and Vdd_inv nodes respectively.

The below plots shows the AC analysis of the nodes Vdd_LDO and Vdd_inv nodes. We have attached a current source of 1A AC magnitude current, and measured the voltage at these nodes. We would need a flat AC plot at both these nodes, to confirm that the supply nodes are indeed stable. As it can be seen from the plots, both Vdd_LDO and Vdd_inv nodes have flat AC plots.

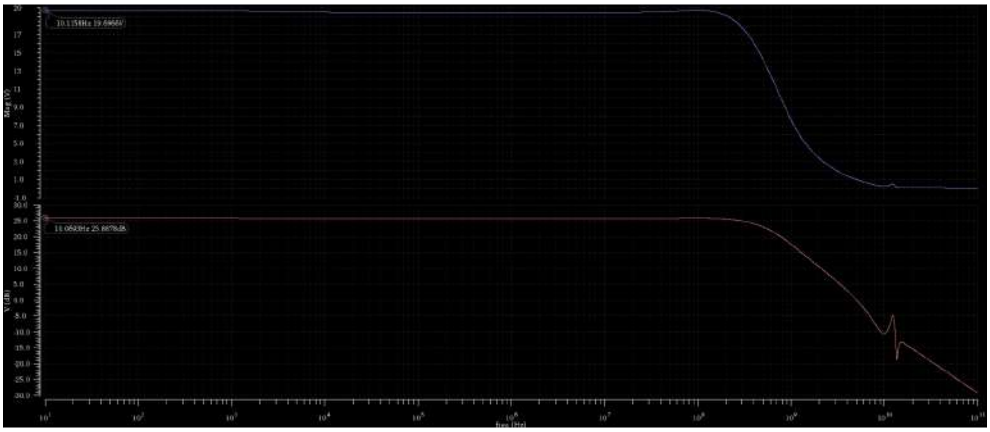


Figure 1.67: AC analysis of Vdd_LDO node of PA + PPA + LDO

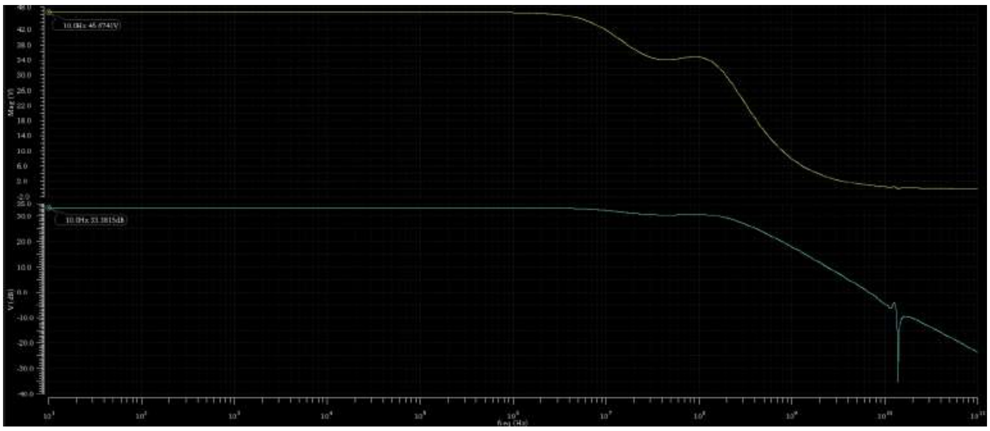


Figure 1.68: AC analysis of Vdd_inv node of PA + PPA + LDO

We need to create a moscap of capacitance 20pF to be used at our Vdd supply nodes. The below shows a unit of the moscap that has a capacitance of 476fF. Hence we connect 42 of such capacitors in parallel to get an overall capacitance of around 20pF. The Layout for this moscap capacitance is as shown below.

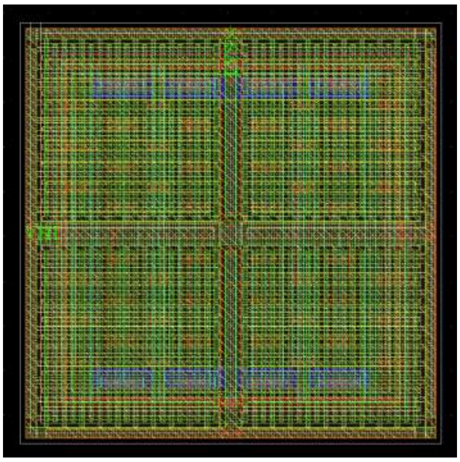


Figure 1.69: Single unit of Moscap

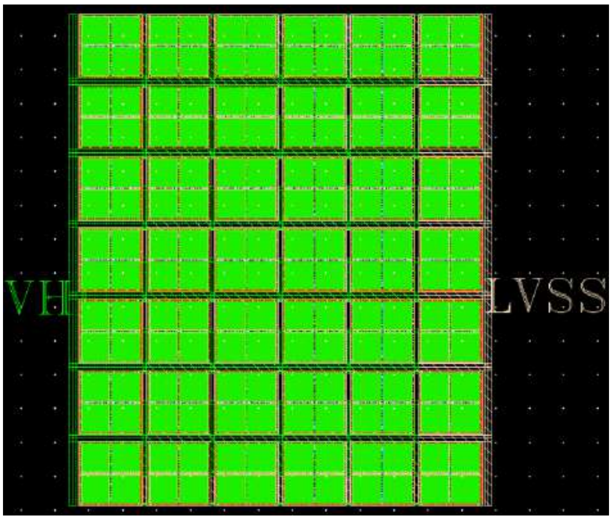


Figure 1.70: Moscap of 20pF capacitance

Since, we have tested PA + PPA separately, we can move ahead and design a completely integrated PA + PPA + LDO circuit, and also design the layout for this circuit. The schematic and Layout for the PA + PPA + LDO circuit is as shown below.

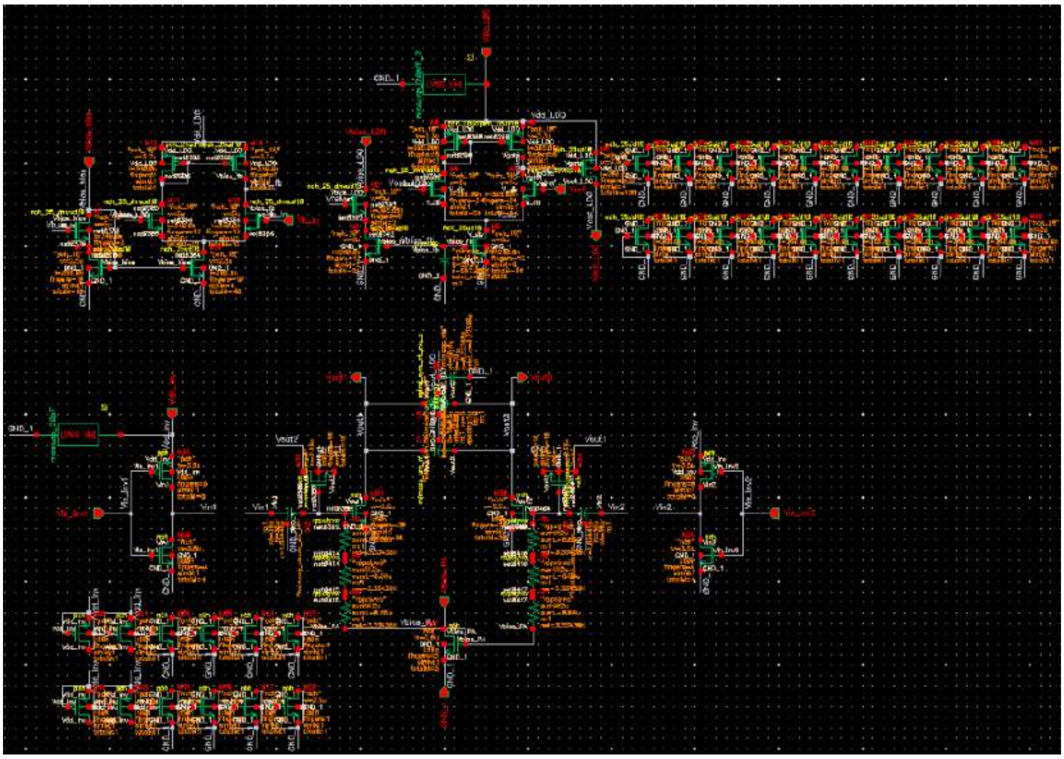


Figure 1.71: Schematic of PA + PPA + LDO

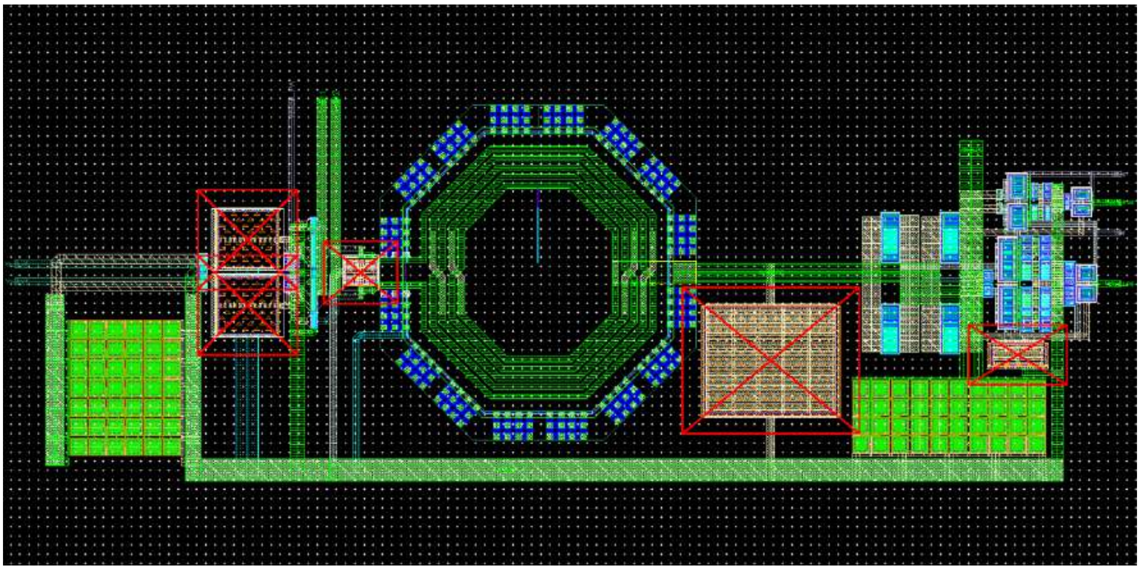


Figure 1.72: Layout of PA + PPA + LDO

The DRC, LVS and PEX success results for the above layout are as shown below.

Figure 1.73: DRC of Layout Design for PA + PPA + LDO Circuit

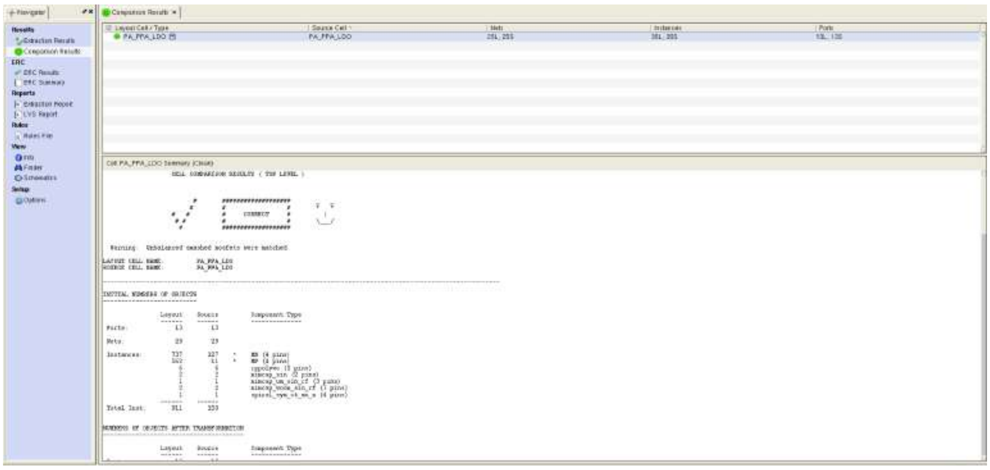


Figure 1.74: LVS of Layout Design for PA + PPA + LDO Circuit

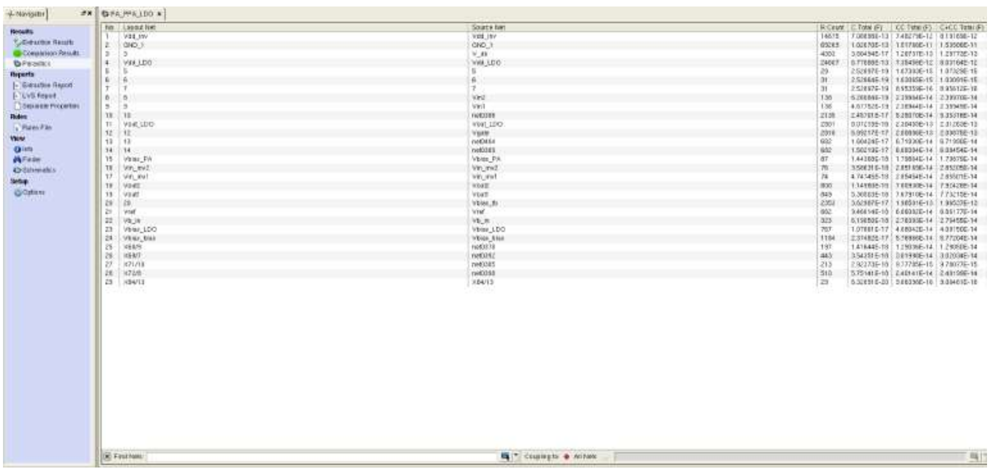


Figure 1.75: PEX of Layout Design for PA + PPA + LDO Circuit

We will simulate the RCC extracted netlist of the PA + PPA + LDO circuit from now on, to get the final specifications for our circuit.

Since, in the above circuit, we dont have access to the intermediary nodes inside LDO and PA + PPA, hence analysing the loop characteristic (Loop Gain, Phase Margin) might be difficult here. One way to do this, is to provide a step response at Vref (1v to 1.1V), and observe the output response of the LDO (This would be Vout_LDO - GND_1). This way we will be able to analyse the closed-loop output response of the LDO. If there isn't much ringing at the step for the output of the LDO, then it means that, the phase margin is very good for our circuit.

The output response will have oscillations at around 7GHz, because of the harmonics from the PA + PPA. Hence in *Matlab*, we use a moving average filter (movmean() function in *Matlab*), to filter out the oscillations, and get the average value at each point of time. This will tell us, if there is any ringing in the output response. The below plot shows the output response, with and without the moving average filter, along with the step input.

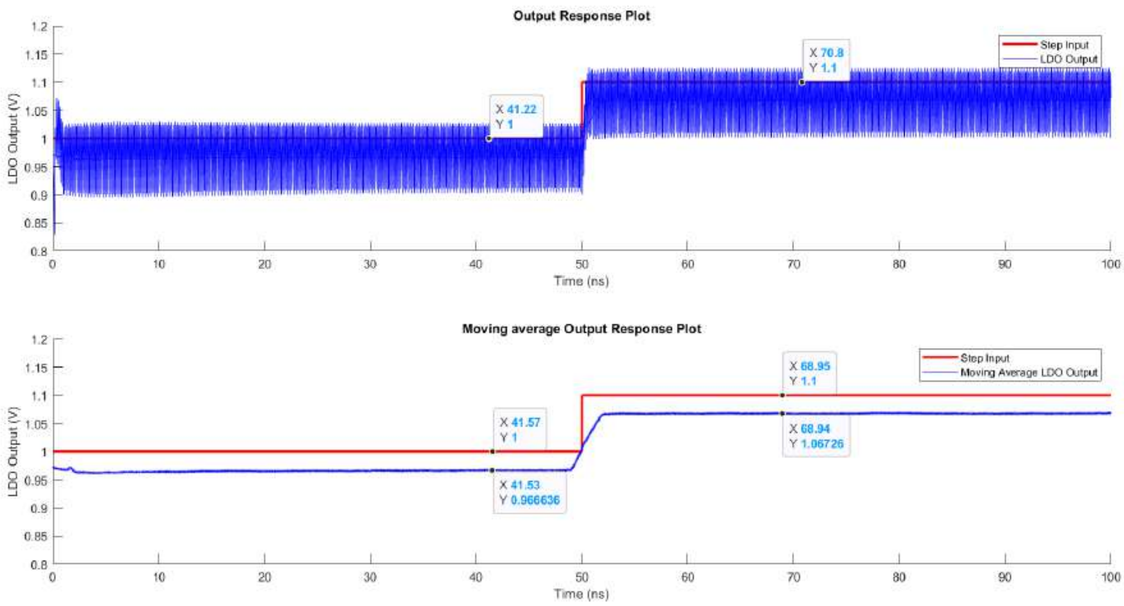


Figure 1.76: Output Response of the LDO for a Step Input

As evident from the above plot, there is very little ringing at the step. Hence, we can say that our main LDO loop has very good phase margin, and loop characteristics.

The below plot shows the transient analysis for Vout_balun, Vout_LDO - GND _1, and Vref, the AC Gain plot for the PA, the P1dB compression and the phase variation plot. The gain at 3.5GHz is **1.0852 V/V**, the P1dB is at **8.152 dBm** with a saturation power of **11.842 dBm**, at a phase variation of **0.318°**.

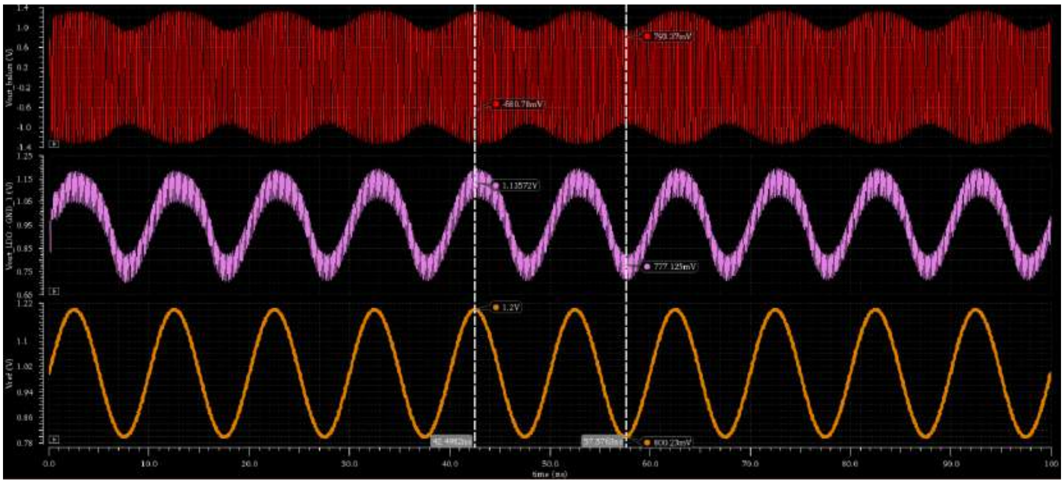


Figure 1.77: Transient analysis for RCC extracted netlist of PA + PPA + LDO

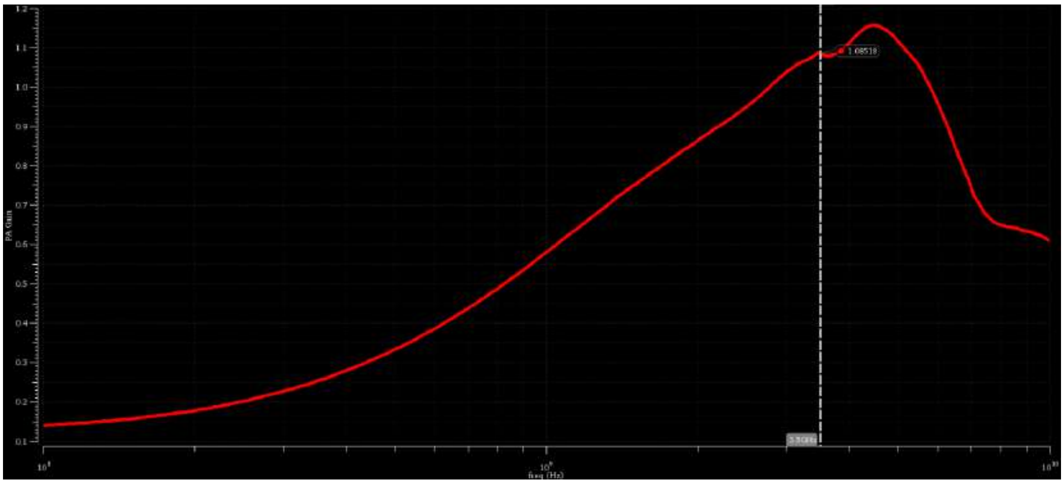


Figure 1.78: AC Gain plot for RCC extracted netlist of PA + PPA + LDO

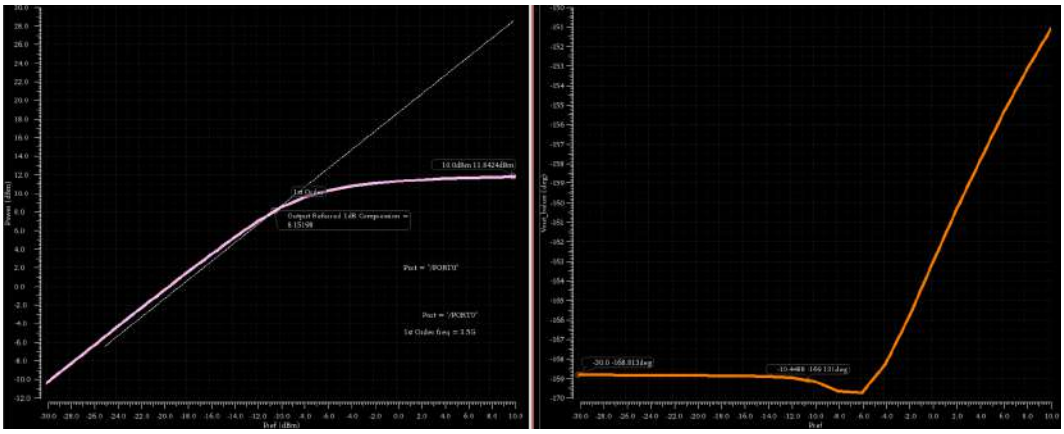


Figure 1.79: P1db Compression and Phase Variation plot for RCC extracted netlist of PA + PPA + LDO

CHAPTER 2

CONCLUSION

We have designed the RF Power Amplifier with Polar Modulation. The Phase Modulation will come through the PA inputs, and the Amplitude Modulation will come through the LDO that is designed along with the PA. We started off with the design of a simple PA, followed by the PA + PPA (Pre Power Amplifier). After that, we went ahead with the design of the LDO module for amplitude modulation. We have also designed the complete layout for the PA + PPA + LDO circuit, extracted the RCC netlist for the same, and have tested using the same as well, for various specifications of the PA.

Future Work

Following the complete design of the PA + PPA + LDO, we can start with the by providing phase and amplitude modulated signals as inputs to the PA. We can start off with a simple BPSK modulation, followed by a QPSK modulation. Once, the PA gives sufficient results to the above modulation schemes, we can go ahead with 16-QAM modulation schemes as well.

Once, the PA + PPA + LDO circuit design has been tested fully via simulations in cadence, we can move ahead with the tape-out process. After the chip has been fabricated, we can test the same in a lab, to make sure it provides the same sufficient results as it did in the simulations as well. This will ensure that our circuit design works well, and will withstand the temperature and environment variations in real life.