Design of an 800 MHz Voltage Controlled Oscillator

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Design of an 800 MHz Voltage Controlled Oscillator**, submitted by **ROHITH GORANTALA** (**EE18B008**), to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelors of Technology**, is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

This work presents a design topology for implementing Voltage Controlled Oscilltor. We need to design a Voltage controlled Oscillator operated at 800 MHz using TSMC 180nm Technology. From the help of Already designed Voltage controlled Oscillator in UMC 180nm which is converted to TSMC 180nm using porting between PDKs Scripts. At the end We need to design the Voltage Controlled Oscillator in TSMC 180nm such that it gives better performance compared with UMC 180nm Technology.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

UMC	United Microelectronics Corporation
TSMC	Taiwan Semiconductor Manufacturing Company
VCO	Voltage Controlled Oscillator
nMOS	N-channel MOSFET
pMOS	P-channel MOSFET
FOM	Figure of Merit
PDK	Process Design Kit

NOTATION

g_{mn}	Transconductance of nMOS
g_{mp}	Transconductance of pMOS
g_{ds}	Drain to source conductances
f_{osc}	Frequency of Oscillation
K_{VCO}	Change of frequency for unit change in Control Voltage
P_{dc}	Power Consumed
Δf	Offset frequency
Q	Quality Factor

CHAPTER 1

INTRODUCTION

1.1 VCO Architecture

A voltage-controlled oscillator (VCO) is an electronic oscillator whose output frequency is proportional to its input voltage. An oscillator produces a periodic AC signal, and in VCOs, the oscillation frequency is determined by voltage.Voltage-controlled oscillators come in various of topologies, including ring oscillators, relaxation oscillators, and LC oscillators. PLL applications benefit from the outstanding phase noise performance of LC oscillators. However, when compared to a ring oscillator, the circuit is bulky due to the size of the inductors and capacitors. A differential cross-coupled pair with a current mirror can be used to make an LC VCO. Complementary cross-coupled pairs (which include both nMOS and pMOS cross-coupled pairs) assist in boosting oscillation amplitude for the same current as nMOS or pMOS cross-coupled pairs.

A figure of merit can be used to determine the quality of VCO.

$$FOM = -L(\Delta f) + 20log\left(\frac{f_o}{\Delta f}\right) - 10log\left(\frac{P_{dc}}{1mW}\right)$$

Where Δf is the offset frequency, L(Δf) is the phase noise at the offset frequency, f_o is the oscillation frequency and P_{dc} is the power consumed in mW.

1.2 Complementary CMOS LC Oscillator

An LC VCO with nMOS cross-coupled transistors, inductors, and varactors is shown in Figure 1.1, which is biassed using a tail current source. The parasitic resistance observed in the LC tank contributes to the tank's inefficiencies. The cross coupled pair's negative resistance compensates for these losses. As seen in Figure 1.1, the transistors' drain current swings between 0 and I0. As a result, the amplitude of the oscillation produced will be I0 time impedance, which is R/2 in parallel with L/2 and 2C, as seen from the source. The effective impedance encountered by the current in the case of a complementary cross-coupled pair Figure 1.2 will be R in parallel with the L and C, increasing the amplitude of oscillation for the same current. The latter design is chosen since it provides greater oscillation amplitude for the same current.

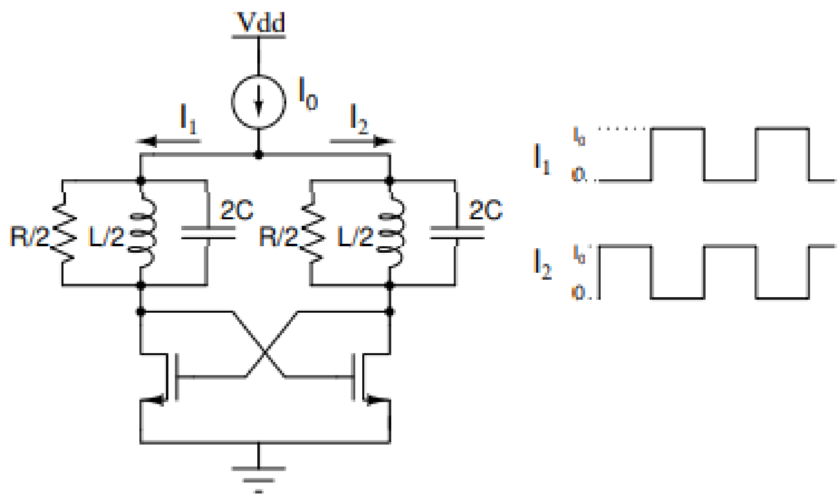


Figure 1.1: LC VCO using nMOS cross-coupled pair

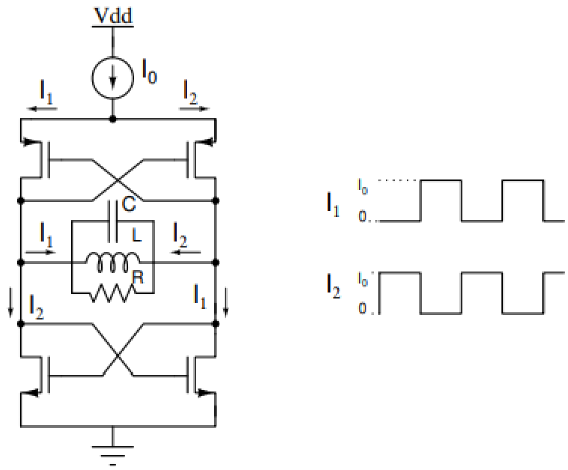


Figure 1.2: LC VCO using nMOS and pMOS cross-coupled pair

1.3 VCO Design

The frequency of oscillation was chosen to be $f_{osc} = 800$ MHz . The oscillation should have an appreciable amplitude and frequency range. The VCO should also have a good phase noise performance. Figure 1.3 shows the different components in the VCO.

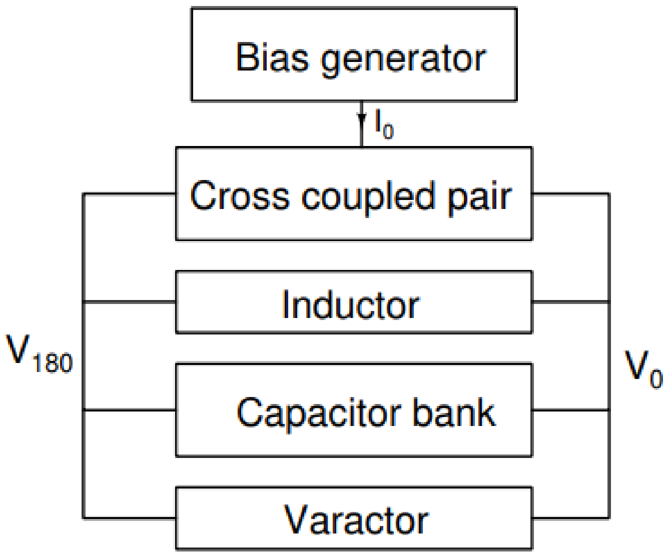


Figure 1.3: VCO Block diagram

CHAPTER 2

Conversion of UMC to TSMC

2.1 Schematic Porting

After figuring out the finally used UMC parameters I have used porting between PDK's for the conversion of UMC to TSMC. This process converts the Instances of UMC cells in to TSMC. This process is done in stepwise manner as mentioned in this document.

We have to list out the devices which were used in umc180 project and equivalent devices in tsmc180 project. We can get this list of devices which were used in that particular project from LVS Report summary file. Figure 2.1 shows the list of devices used in umc180 project and corresponding devices in tsmc180.

UMC180		TSMC180	
Library	**Device Name**	**Library**	**Device Name**
UMC180	N_18_MM	tsmc18	nmos2v_mac
UMC180	N_LV_18_MM	tsmc18	nmosmvt2v_mac
UMC180	P_18_MM	tsmc18	pmos2v_mac
UMC180	P_LV_18_MM	tsmc18	pmosmvt2v_mac
UMC180	MIMCAPS_MM	tsmc18	mimcap_2p0_sin
UMC180	RNHR1000_MM	tsmc18	rphripoly
UMC180	RNNPO_MM	tsmc18	rnhpoly
UMC180	NCAP_MM	tsmc18	mos_var_b

Figure 2.1: TSMC devices for corresponding UMC devices

We will use custom script to update devices to new library tsmc18. This script will take library as input and it will update all cells in Script.It will only support above mentioned devices only. If we want to add new devices, we can update the script as per the requirement. Script Usage is shown in the figure 2.2.

Figure 2.2: Script Usage for Schematic Porting

2.2 Layout Porting

In a Similar way Layout porting is also done with the help of Layermap file. The final Layer map file should contain all layer name and purpose from umc180 process and GDS Number and Purpose number from tsmc180 process. Refer figure 2.3 for sample layer map file. This process is also done in stepwise manner as mentioned in this document.

Contact and Via size are different for both process. So they will give more DRC Errors. By using a script,we will update contact and Via sizes.

Device layer sizes also different in both the process. Using This Other script, it either shrink or enlarge shapes, It is also won't check for absolute sizes. We have to run these for library only once. Script usage is shown in figure 2.4.

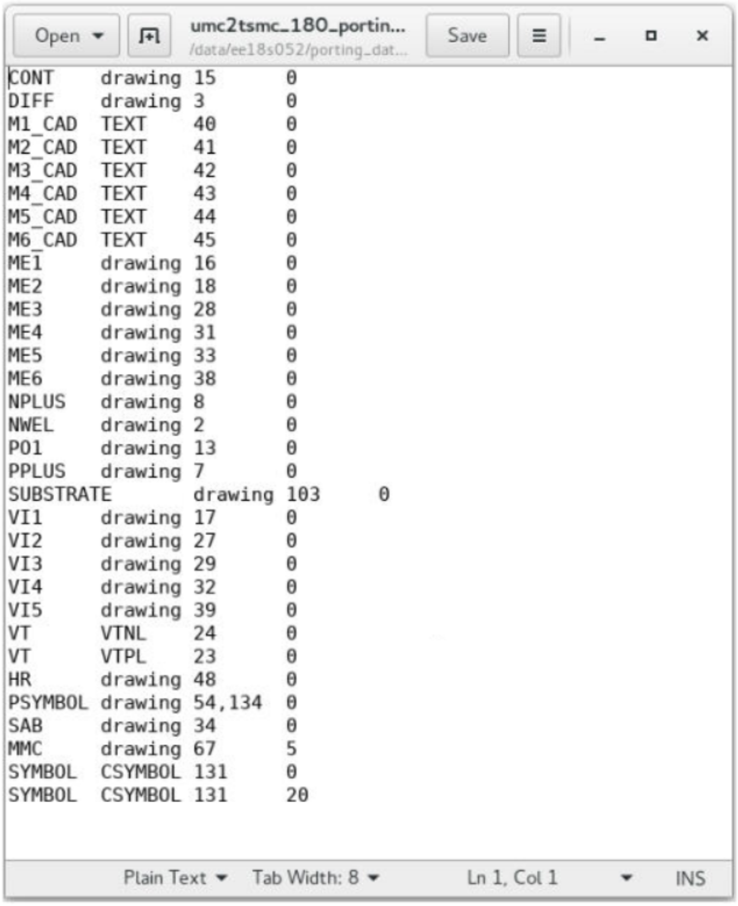


Figure 2.3: Layermap file

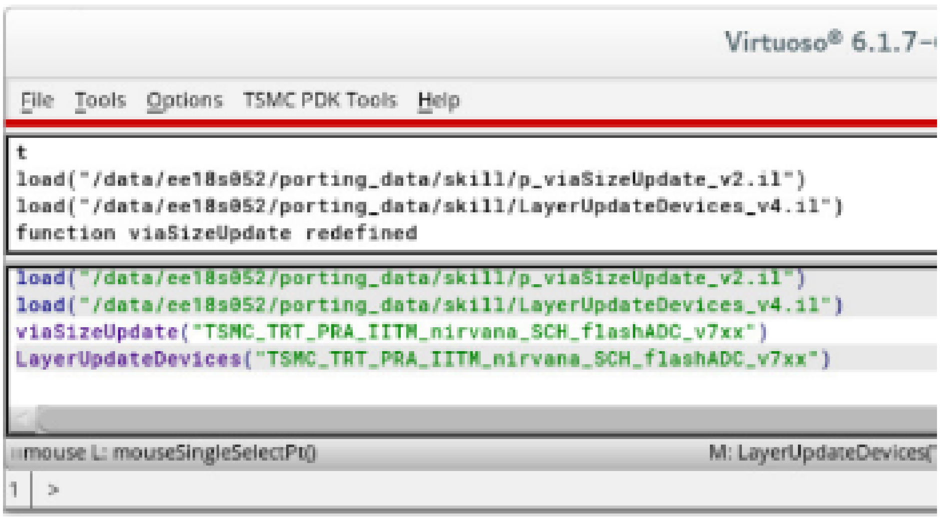


Figure 2.4: Script Usage for Layout Porting

2.3 Issues after porting

There are some Instances/Devices which are not mentioned in the figure 2.1 but still used in the Schematic for building VCO. Below are the device names of the instances which are not converted to tsmc through porting.

UMC	**TSMC**
RHNR_RF	rphripoly_rf
MIMCAPM _RF	mimcap_2p0_sin_3t
VARMIS _18 _RF	moscap _rf

Table 2.1: The table shows the list of Instances which are used as replacement in TSMC for the above instances in UMC180

The TSMC devices mentioned above are replaced at corresponding UMC devices with same values of property(for example: Resistance, capacitance).

CHAPTER 3

TSMC180nm VCO

After Converting entire schematic from UMC180 to TSMC180. The results weren't the same or better than UMC180 as their is difference in the device properties. As there are some replaced components with different device properties. Also we Know Quality Factor plays important role in having better phase noise.Some Changes have been Made in the device parameters to achieve better performance than UMC180.

3.1 VCO Design

3.1.1 Inductor

The LC tank should have a high quality factor(Q) for better phase noise performance . At 800 MHz the Q of the tank is dominated by the inductor. The inductor's Q is proportional to the value of the inductance. High inductance values, on the other hand, will take up a lot of space and require a lengthy wire, which will have a higher resistance. Figure 3.2 depicts the layout of the inductor. The width and spacing between the turns should be adjusted to increase the Q of the inductor. The figure below demonstrates why the value was chosen i.e., width of wire = 20μm. L = 12.749nH.

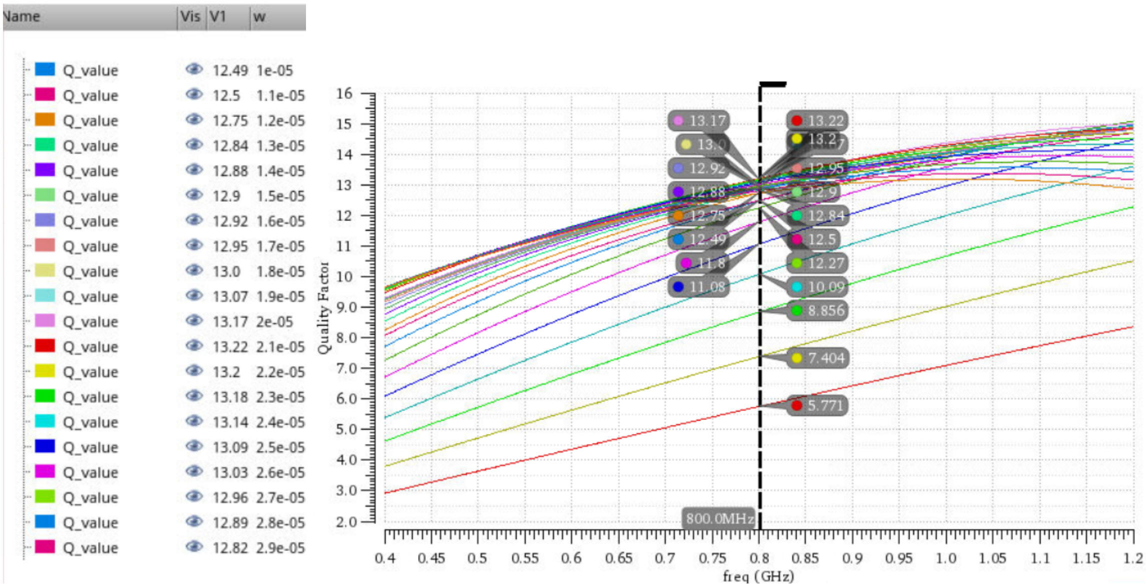


Figure 3.1: Pattern of Quality Factor

3.1.2 Cross Coupled Oscillator

The parallel resistance offered by the LC tank will dampen the oscillations. A negative resistance is introduced using a cross coupled pair to compensate for the losses, as shown in Figure 3.2. The LC tank contributes nearly 814 Ω to the circuit. The cross-coupled pair should generate a negative resistance of R_{neg} with a magnitude smaller than 814 Ω, resulting in a negative effective resistance. The negative impedance provided by the cross-coupled pair,

$$R_{neg} = \frac{-2}{g_{mn} - gds} \,||\, \frac{-2}{g_{mp} - gds}$$

The g_{mn} and g_{mp} were adjusted to give the R_{neg} to -134Ω.

M1=M2=1*20*3μ/180n

M3=M4=1*20*1.6μ/180n

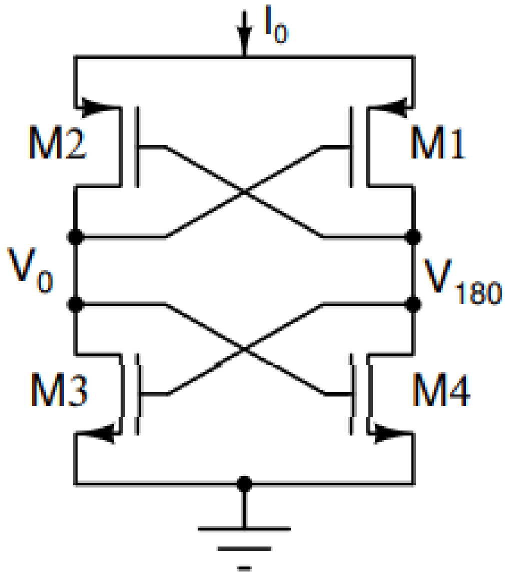


Figure 3.2: Complementary Cross Coupled Pair

3.1.3 Capacitor Bank

From the obtained value of L, the capacitor value required was found to be 3.104 pF.The total capacitance is implemented with a fixed capacitor of value 1.152 pF and a 3 bit capacitor bank of LSB equating to 330 fF to accommodate for variation in capacitor values. During turn on and off, the switch sizes were changed to provide a high Q capacitor bank. If the control bit ct1 is low, the MOSFET M1 M2 is turned 'ON' because ct1b is high. As a result, it adds a capacitor C3 in series with C4 across the terminals, modifying the effective capacitance across the terminals. When the other switches are turned off, a large resistance and a low capacitance (relative to the overall capacitance) are introduced in parallel across the terminal. The *mim_cap_sin_3t* was used for the implementation of the capacitor bank.

Values of newly replaced *mim_cap_sin_3t* are adjusted such that VCO produces the desired tuning range.

M1=M2=M3=M4=M5=M6=$10\mu/0.18\mu$

C1=C6=329.4fF * 4,C2=C5=329.4fF * 2, C3=C4=329.4fF * 1

R1=R2=15.18K, R3=R4=14.14KΩ, R5=R6=13.23KΩ

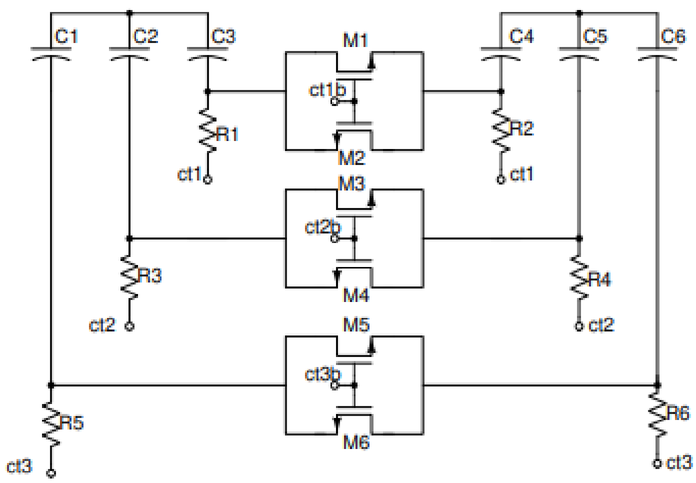


Figure 3.3: Capacitor Bank

3.1.4 Varactor

A varactor is connected in parallel with the capacitor as we need to alter the oscillation frequency with a control voltage. The varactor varies the capacitor's value according to the applied voltage. The varactor's minimum change in capacitor value should be greater than the capacitor bank's LSB.

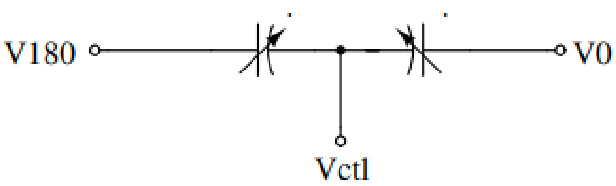


Figure 3.4: Varactor

CHAPTER 4

Performance of VCO

HB simulations were run on the designed VCO to verify the operation of the VCO at different PVT variations.

4.1 Schematic Results

The following values for the respective were obtained from the schematic:

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise@ offset of 100KHz(dBc/Hz)	Tuning Range(MHz)
TT	1.8	0	0	360	5.548	1405	-110.4	688 - 929
	0	1.8	1.8	598	5.577	1391	-109.2	
	0	1.8	0	807	5.543	1398	-108.2	
	0	0	1.8	1140	5.476	1416	-108.4	
SS	1.8	1.8	0	301	4.625	1250	-109.2	648 - 879
	1.8	0	1.8	546	4.623	1248	-106.6	
	1.8	0	0	761	4.596	1259	-105.7	
	0	1.8	1.8	1131	4.57	1274	-106.8	
FF	0	1.8	0	439	6.782	1546	-105	730 - 978
	0	0	1.8	677	6.806	1537	-106.1	
	0	0	0	888	6.749	1543	-106.2	

Table 4.1: Schematic Simulation Results of VCO

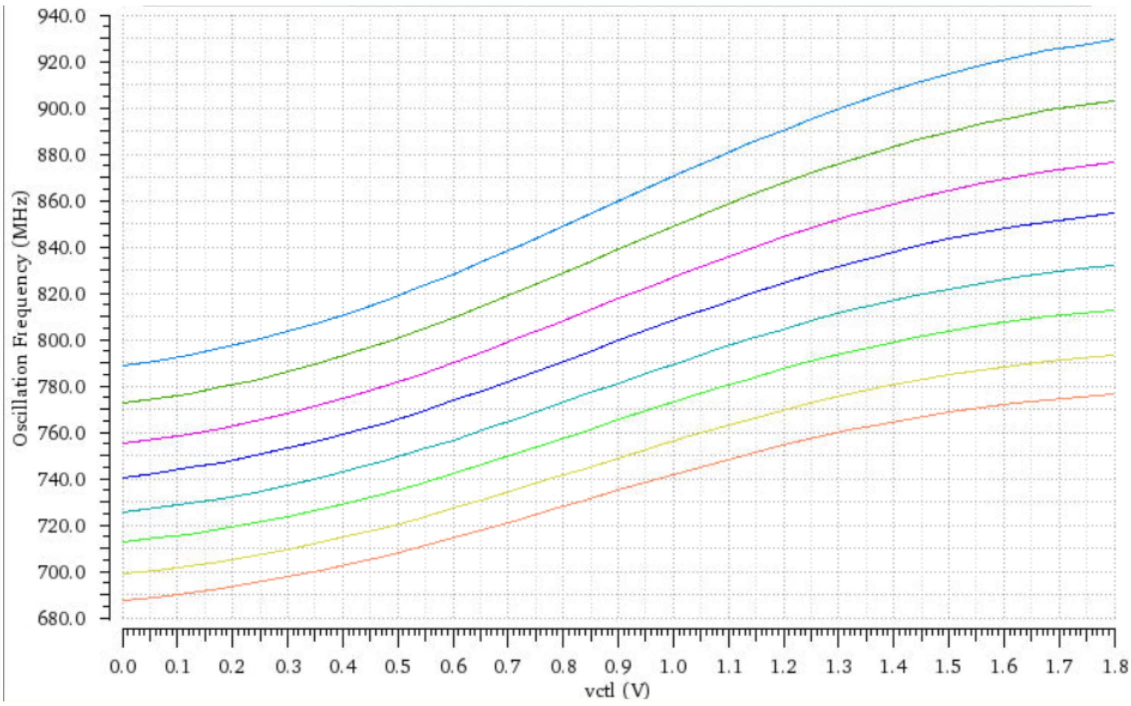


Figure 4.1: Frequency characteristics in TT corner at 50^o C

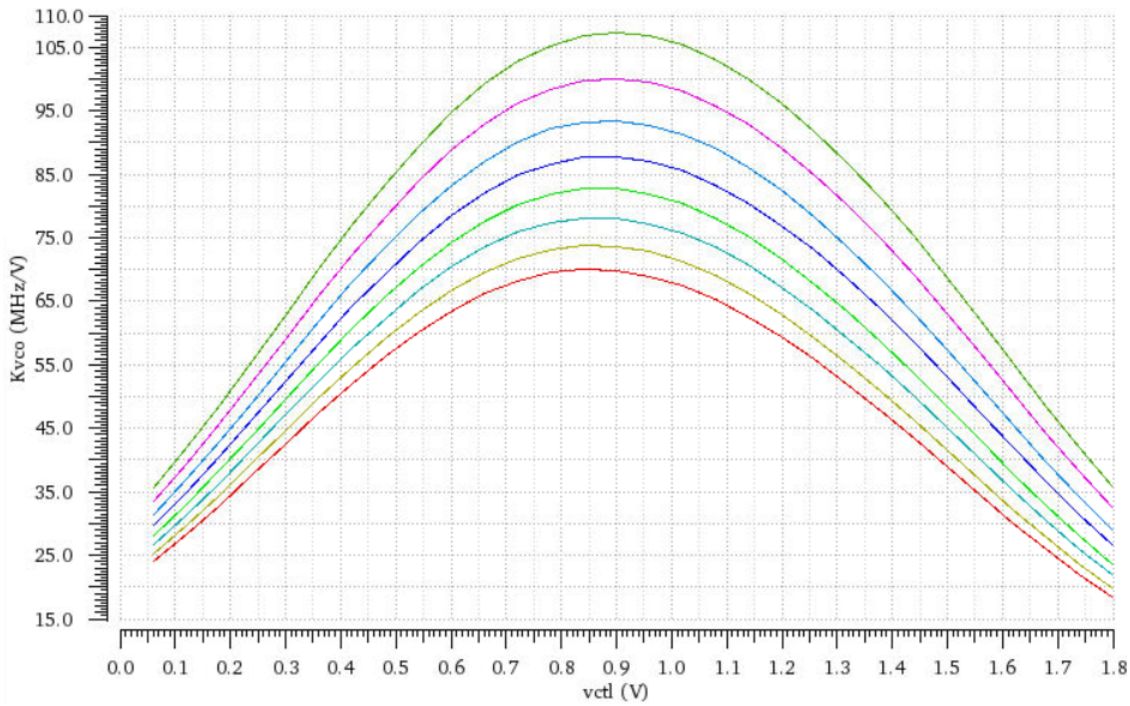


Figure 4.2: K_{VCO} characteristics in TT corner at 50^oC

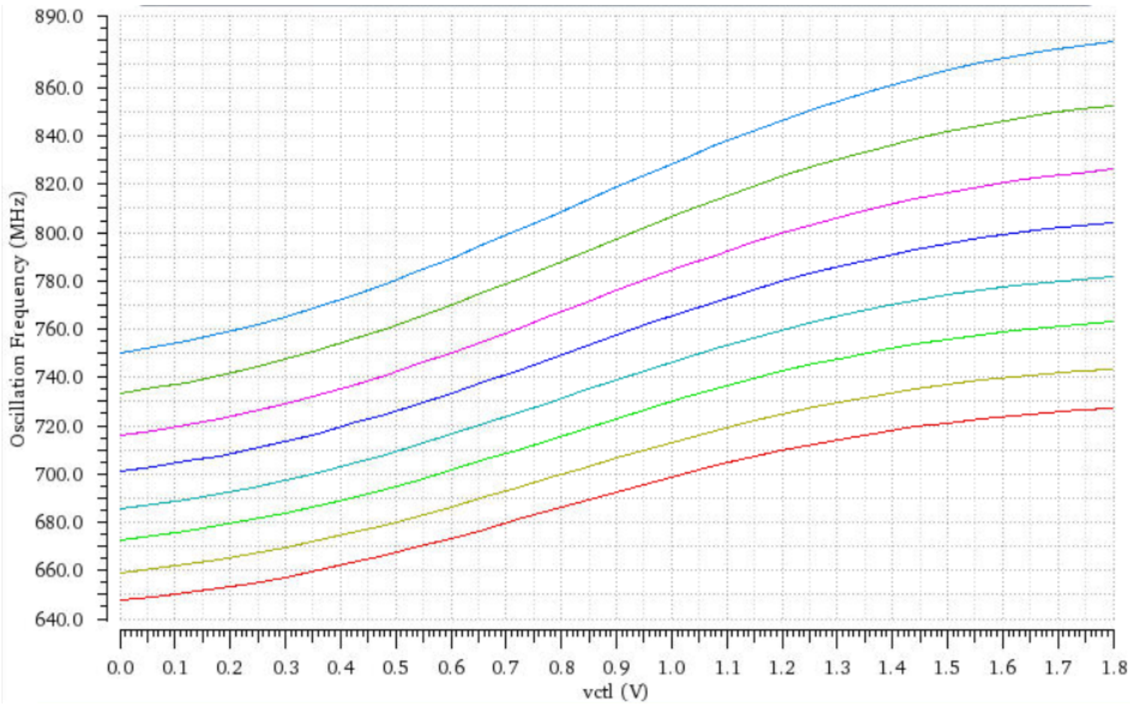


Figure 4.3: Frequency characteristics in SS corner at 100^o C

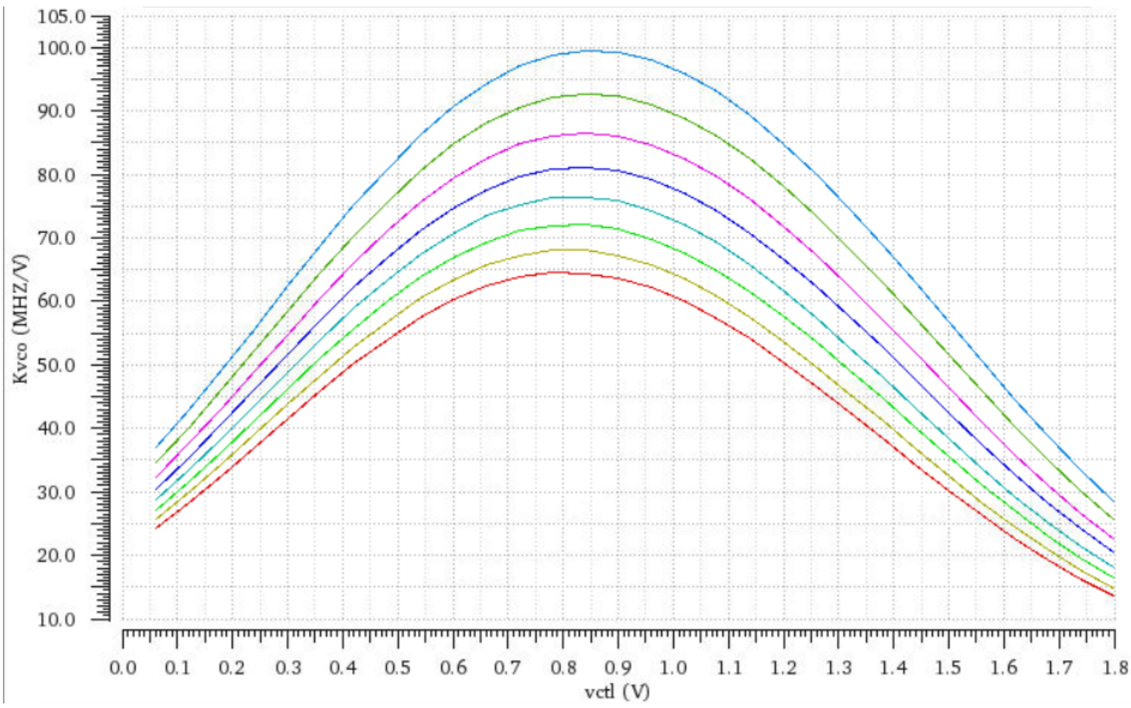


Figure 4.4: K_{VCO} characteristics in SS corner at 100^{o}C

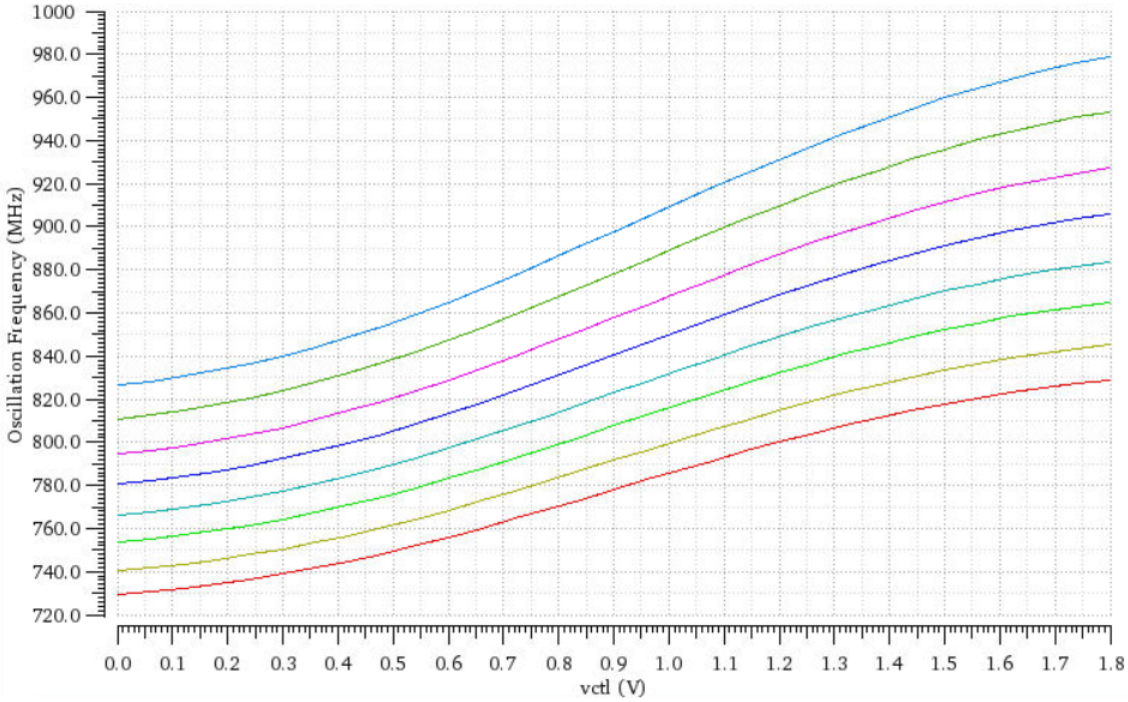


Figure 4.5: Frequency characteristics in FF corner at 0^o C

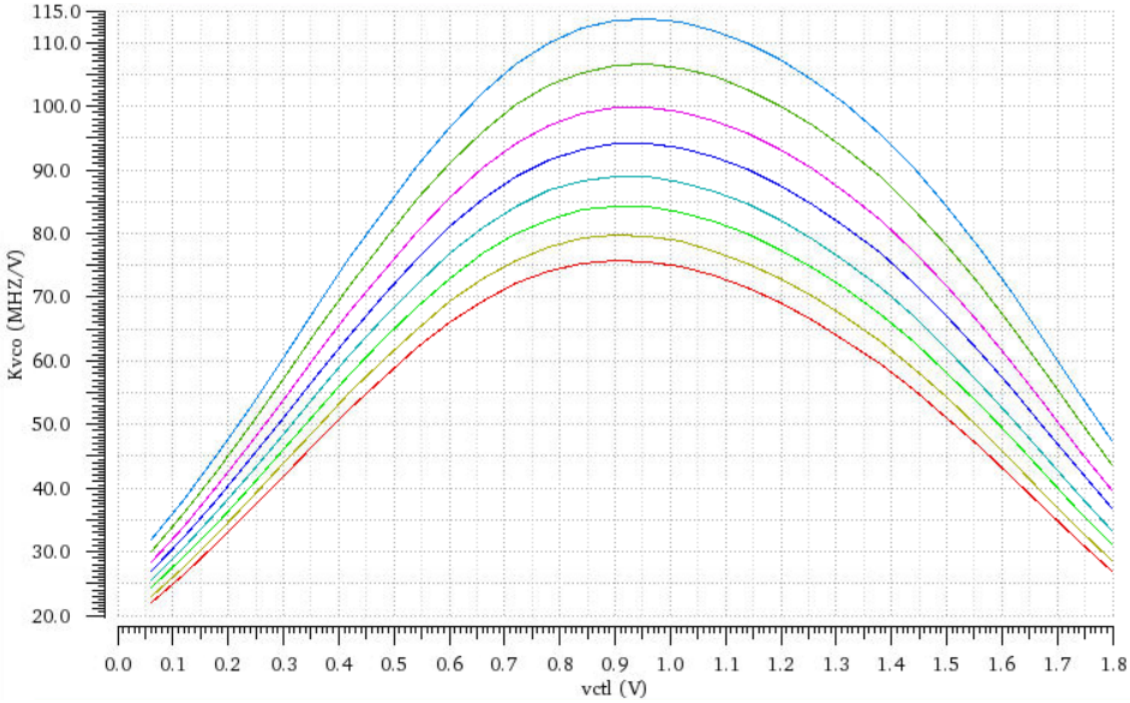


Figure 4.6: K_{VCO} characteristics in FF corner at 0^oC

4.2 Layout of VCO

A new Layout from Scratch has been created As there are replaced devices which are not converted through layout porting. Devices have different properties and layer terminals. Layout has been created without the inductor as its giving some evaluation errors which is the same case with UMC180.

Figure 4.1 shows the layout of the TSMC180 Schematic.

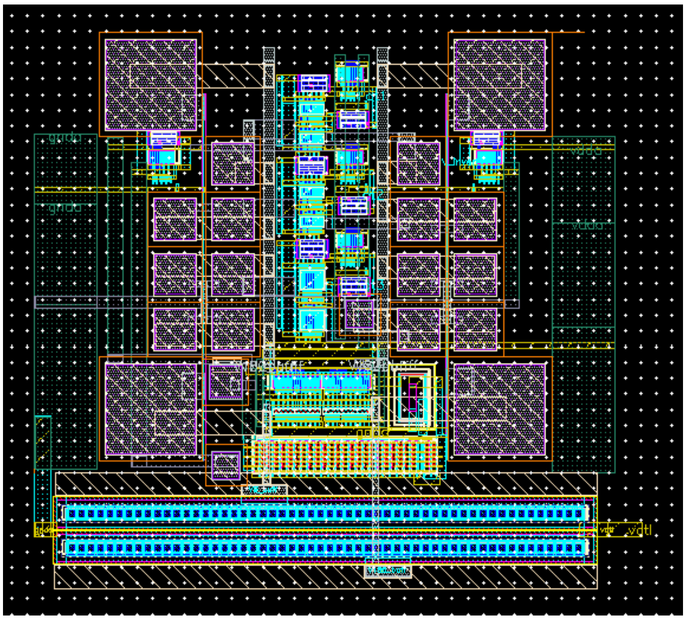
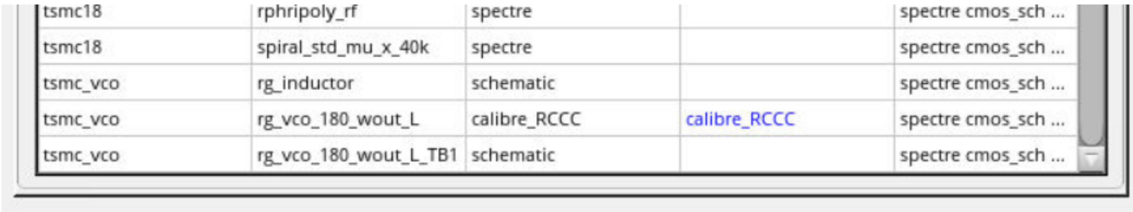


Figure 4.7: Layout Version 1 TSMC180

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise@ offset of 100KHz(dBc/Hz)
TT	1.8	1.8	0	254	5.259	401.1	-94.53
	1.8	0	1.8	512	5.239	493.4	-90.74
	1.8	0	0	687	5.207	576.9	-91.18
	0	1.8	1.8	948	5.171	657.2	-96.05
	0	1.8	0	1313	5.126	717.9	-104.7

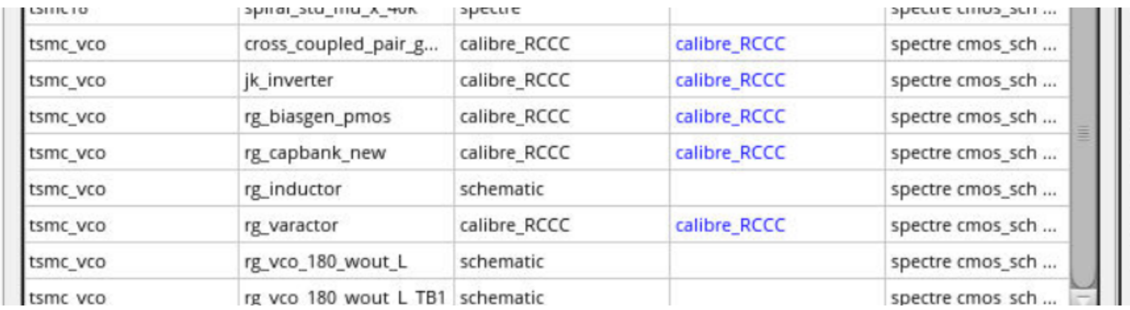
Table 4.2: Layout Simulation Results of VCO

After Running the config with the RC Extracted layout the results are not as expected. there has been increase in the phase noise. To figure out the problem, individual blocks which are Capacitor bank, Cross coupled pair, Varactor, Current mirror and inverters are put RC extraction instead of putting entire layout RC extraction as shown in the figure 4.8 and 4.9.



tsmc18	rphripoly_rf	spectre		spectre cmos_sch ...
tsmc18	spiral_std_mu_x_40k	spectre		spectre cmos_sch ...
tsmc_vco	rg_inductor	schematic		spectre cmos_sch ...
tsmc_vco	rg_vco_180_wout_L	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	rg_vco_180_wout_L_TB1	schematic		spectre cmos_sch ...

Figure 4.8: Config settings where entire VCO is RC EXtracted



tsmc18	spiral_std_mu_x_40k	spectre		spectre cmos_sch ...
tsmc_vco	cross_coupled_pair_g...	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	jk_inverter	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	rg_biasgen_pmos	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	rg_capbank_new	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	rg_inductor	schematic		spectre cmos_sch ...
tsmc_vco	rg_varactor	calibre_RCCC	calibre_RCCC	spectre cmos_sch ...
tsmc_vco	rg_vco_180_wout_L	schematic		spectre cmos_sch ...
tsmc_vco	rg_vco_180_wout_L_TB1	schematic		spectre cmos_sch ...

Figure 4.9: Config settings where individual blocks are RC EXtracted

Results after putting individual blocks in RCCC:

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise@ offset of 100KHz(dBc/Hz)
TT	1.8	1.8	0	254	5.942	1238	-110
	1.8	0	1.8	512	5.87	1266	-107.5
	1.8	0	0	687	5.791	1297	-106.7
	0	1.8	1.8	948	5.739	1312	-106.5
	0	1.8	0	1313	5.576	1370	-108.9

Table 4.3: Individual Blocks RC Extracted Simulation Results of VCO

From the above tables we can say that the noise is due to interconnects of these blocks with the capacitors and resistors as shown in the figure.

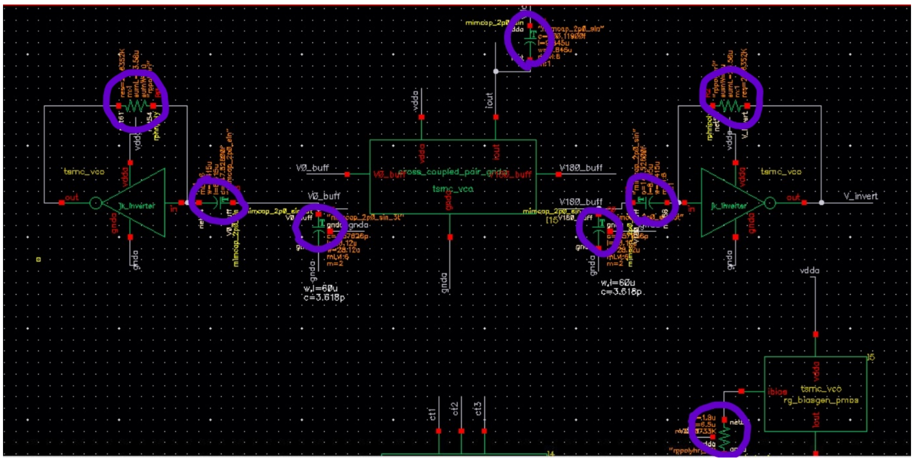


Figure 4.10: Resistors and capacitors connected between blocks

Even after trying to increase width of the metals to reduce the resistance didn't improve much. so Another version of layout has been created to tackle the noise. Figure 4.11 shows the another version of layout.

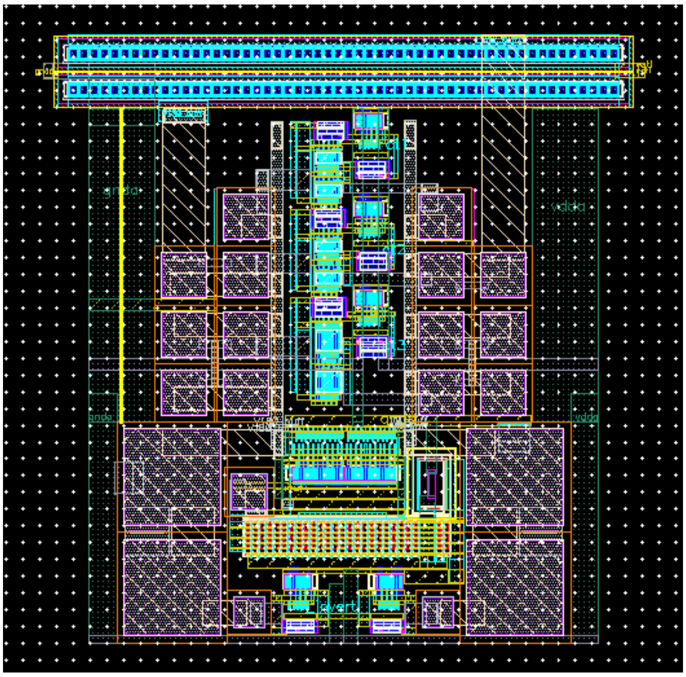


Figure 4.11: Layout Version 2 TSMC180

Final Results After Simulating the second version of Layout:

Corner	Ct3 (V)	Ct2 (V)	Ct1 (V)	Vctl (mV)	Power (mW)	Vpp (mV)	Noise@ offset of 100KHz(dBc/Hz)	Tuning Range(MHz)
TT	1.8	1.8	0	254	6.006	1134	-108.8	683 - 906
	1.8	0	1.8	512	5.931	1170	-106.2	
	1.8	0	0	687	5.854	1202	-105.6	
	0	1.8	1.8	948	5.763	1239	-106	
	0	1.8	0	1313	5.612	1300	-108.7	
SS	1.8	1.8	1.8	456	4.862	974.8	-102.2	640 - 855
	1.8	1.8	0	640	4.81	1026	-102.2	
	1.8	0	1.8	901	4.75	1076	-103.4	
	1.8	0	0	1343	4.647	1153	-108.1	
FF	0	1.8	1.8	555	7.288	1331	-108.6	728 - 959
	0	1.8	0	721	7.198	1357	-108.1	
	0	0	1.8	952	7.072	1388	-107.9	
	0	0	0	1195	6.899	1432	-108.2	

Table 4.4: Layout Simulation Results of VCO

CHAPTER 5

UMC vs TSMC

As Mentioned in the first chapter, Quality of VCO is determined by the FOM.

$$FOM = -L(\Delta f) + 20log\left(\frac{f_o}{\Delta f}\right) - 10log\left(\frac{P_{dc}}{1mW}\right)$$

Where Δf is the offset frequency, L(Δf) is the phase noise at the offset frequency, f_o is the oscillation frequency and P_{dc} is the power consumed in mW.

Phase noise is taken at offset frequency of 100KHz.

5.1 Schematic Comparision

Freq(MHz)	Phase Noise		Power(mW)		Amplitude(mV)		FOM	
	UMC	TSMC	UMC	TSMC	UMC	TSMC	UMC	TSMC
740	-108.901	-108.735	6.194	5.466	885	1430	178.4	178.7
780	-107.688	-108.003	6.062	5.319	944	1480	177.7	178.6
820	-107.254	-107.406	5.963	5.373	999	1470	177.8	178.4
860	-106.201	-106.495	5.867	5.16	1051	1530	177.2	178.1
900	-105.045	-105.809	5.792	5.126	1090	1538	176.5	177.8
928	-103.133	-103.521	5.744	5	1119	1582	174.9	175.9

Table 5.1: Schematic Results Comparision

5.2 Layout Comparision

Inputs implies ct3—ct2—ct1 values for example: 101 means Ct3 = 1.8 V, Ct2 = 0 V, Ct3 = 1.8V

Corner	Inp	Vctl (mV)	Phase Noise		Power(mW)		Amplitude(mV)		FOM(dB)	
			UMC	TSMC	UMC	TSMC	UMC	TSMC	UMC	TSMC
TT	110	254	-107.8	-108.8	6.29	6.006	939	1134	177.8	178.8
	101	512	-105.1	-106.2	6.3	5.931	933	1170	175.2	176.3
	100	687	-104.8	-105.6	6.28	5.854	929	1202	174.9	175.7
	011	948	-106.1	-106	6.29	5.763	955	1239	176.1	176.2
	010	1313	-108.4	-108.7	6.27	5.612	940	1300	178.4	179.1
SS	111	456	-102	-102.2	4.9	4.862	828	974.8	175.8	173
	110	640	-101.5	-102.2	4.9	4.81	828	1026	176	173
	101	901	-103.6	-103.4	4.9	4.75	824	1076	175.4	174.3
	100	1343	-108.3	-108.1	4.89	4.647	830	1153	175	179.2
FF	011	555	-106.9	-108.6	8.17	7.288	1057	1331	173.1	178
	010	721	-107	-108.1	8.15	7.198	1057	1357	172.6	177.5
	001	952	-106.5	-107.9	8.15	7.072	1064	1388	174.8	177.4
	000	1195	-106.1	-108.2	8.09	6.899	1078	1432	179.4	177.9

Table 5.2: Layout Results Comparision

5.3 Summary

From the above observations we can clearly see TSMC180nm VCO has better performance than UMC180nm VCO. There are some cases where it degrades but we can get the frequency same as UMC with better FOM. As you can see from the tables, In every aspect which are phase noise, power and Amplitude, TSMC VCO has better figures than UMC VCO.

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