A REFLECTIVE TYPE PHASE SHIFTER in 65 nm CMOS PROCESS FOR MILLIMETER WAVE RANGE APPLICATIONS

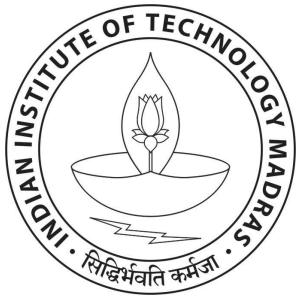
A Project Report

submitted by

SUHAIB PULLAT

in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
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THESIS CERTIFICATE

This is to certify that the thesis titled **A REFLECTIVE TYPE PHASE SHIFTER in 65nm PROCESS FOR MILLIMETER WAVE RANGE APPLICATIONS**, submitted by **SUHAIB PULLAT**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

This paper presents a millimeter wave CLC π load based passive reflective type phase shifter implemented in silicon with a phase shift of more than 360 degrees. A single ended reflective type phase shifter usually consists of 90-degree coupler and two identical passive reflective loads. This RTPS consists of a Lange coupler designed in RFIC and a reactive CLC π load. The chip was designed on the 65 nm CMOS process with a chip area of 650um x 425um. It achieves a wide phase shifting range of 390° with phase resolution less than 5 degrees and insertion loss of 6.6dB to 32dB at 28 GHz

To achieve a phase shift of 360 degrees a CLC π network load was used with two tunable capacitor loads. Resolution of fewer than 5° is accomplished using capacitors in the range of few femtofarads in capacitor bank along with a varactor to keep the phase shift between successive switch points less than 5°. Capacitor banks were used instead of a varactor to get wide phase shift and dense phase shifting angles. A Lange coupler was designed in the 65nm process to get wideband respond around the center frequency of operation.

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ABBREVIATIONS

RTPS	Reflective Type Phase Shifter
mm	Millimeter
RFIC	Radio Frequency Integrated Circuits
CMOS	Complementary Metal Oxide Semiconductor
TSMC	Taiwan Semiconductor Manufacturing Company
DRC	Design Rule Check
PDK	Process Design Kit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

CHAPTER 1

INTRODUCTION

1.1 Introduction

Phase shifters are used to change the phase of transmission phase angle or received phase angle of radio frequency signals. The input signal phase is shifted in phase at the output based on the phase shifting configuration. Phase shifters are widely used in many RF and microwave systems. Applications of phase shifters include beamforming of the array antenna in RADAR, imaging systems and millimeter wave wireless communications. It is an important part of advanced communication topology like 5G.

Phase shifters play a key role in a phased array system since it governs the beamforming quality and steering capabilities. A high-performance phase shifter should achieve a low insertion loss (IL), a wide phase shifting range, dense phase shift angles, and good input/output matching. Phase shifters can be classified as passive or active. Passive phase shifters provide benefits like no DC power consumption, High linearity which is essential for large scaled and power constrained phased array systems.

Common types of passive phase shifter topology are switched line, traveling wave, switched filter and reflection type. Switched line and traveling wave topologies require multiple transmission lines, in turn, require a large area. Switched filter topology lacks from dense phase shifting angles. Among passive phase shifters, reflective type phase shifter (RTPS) have unique advantages which include moderate size, continuous and dense phase shift. Therefore RTPS is an excellent candidate for phased array systems.

1.2 Objectives

The broader objective of this project is to build an RTPS in hardware and test it on board with the specifications given below

- Wide phase shifting range (More than 360°)

- Dense Phase Angles (Adjacent Phase shift is less than 5°)
- Good Input and Output Matching (Less than -10dB)
- Low Insertion loss

A single ended, phase shifter usually consists of a 90° coupler and two tunable reflective loads. In this project, I would like to implement a Lange coupler in place of traditional couplers [1] like branch line coupler and a CLC π network as the reflective load. Since Lange coupler is a distributed transmission line circuit, its loss in high frequency is very less compared to lumped element couplers and it has wideband response around the center frequency of operation. Owing to these advantages Lange coupler was preferred over traditional couplers. There are various types of reflective loads available which are described below in detail. Popular reflective load topologies include tunable capacitors, series LC resonators, parallel LC resonators, and CLC π networks. Among which CLC π network with two tunable capacitor banks was used to achieve more than 360° phase shift.

1.3 Organization of the thesis

This thesis is organized as follows. Chapter 2 first presents the working principle of an RTPS in detail. In chapter 3, the Lange coupler and its design in 65nm and corresponding results are described in detail. In chapter 4 several reported RTPS passive reflective loads, their load impedance tuning ranges and the phase shifting range limits are explained briefly. Next, in chapter 5 the design procedure for CLC π network based reflective load is explained. The layout and simulation results for the entire RTPS were presented in chapter 6.

CHAPTER 2

WORKING PRINCIPLE OF REFLECTIVE TYPE PHASE SHIFTER

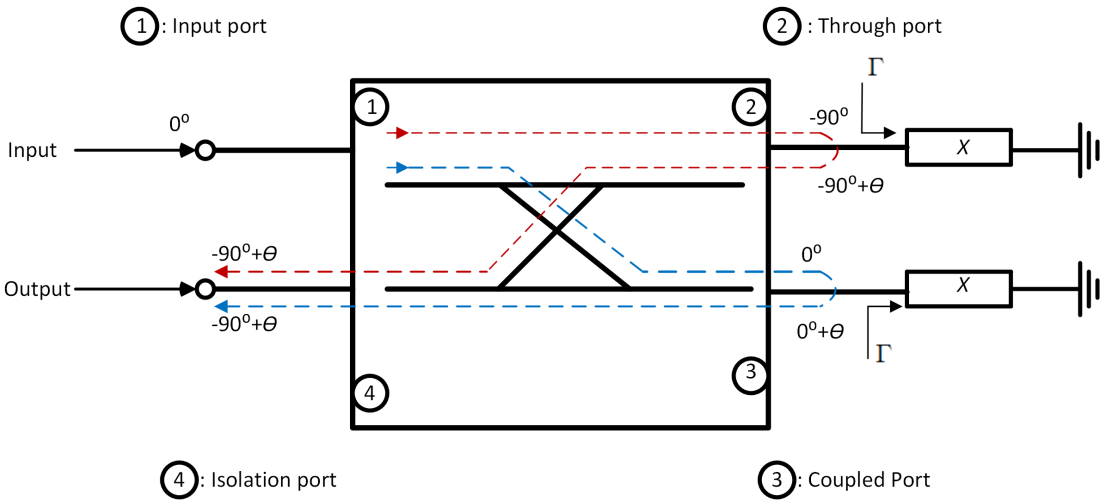

Figure 2.1: Block Diagram Representation of an RTPS

This chapter discusses the working principle of a typical RTPS [3] in detail. Figure 2.1 gives a block diagram representation of a reflective type phase shifter. A typical phase shifter consists of a 3dB quadrature hybrid coupler and two identical reflective loads [4]. The Reflective load itself can produce the required phase shifts. But it is a single port device. So the phase shifted wave has to be guided from the input port to another port say output port so it can be propagated into the next stages of RF blocks.

Here comes the use of 3dB quadrature coupler. It contains 4 ports. 3 dB coupler is symmetric concerning input port and output port. Assuming both 3dB quadrature hybrid coupler and reflective loads are loss-less the incoming RF signal is first split into two parts with equal power and one part travels into through port with -90° phase difference and another part travels into coupled port with 0° phase difference. Both signals completely reflect with some phase change Θ. These reflected signals will travel into the output port from through and coupled ports with 0° and -90° phase differences respectively. So the wave reaching an output port with equal amplitude and equal phase

traveled through two different paths get combined and move into the next stages of the RF circuit. The amplitude and phase of reflected wave either at the coupled or through port is

$$V_2out = V_2in * \Gamma \tag{2.1}$$

Where Γ is the reflection coefficient

$$\Gamma = \frac{X - Z_0}{X + Z_0} = |\Gamma| \angle \Theta \tag{2.2}$$

Where X is the reflective load and Z_0 is the characteristic impedance of coupler.

If the load is loss less

$$\Gamma = 1 < -2 \tan^{-1}(\frac{X}{Z_0}) \tag{2.3}$$

Thus equation 2.3 can be written as

$$V_2out = V_2in * 1 < -2 * tan^{-1}(\frac{X}{Z_0}) \tag{2.4}$$

i.e., the wave hitting at through port or coupled port comes back with a phase change of $\Theta = -2 * \tan^{-1}(\frac{X}{Z_0})$. In addition to the phase shift of $\Theta, -90^\circ$ of phase difference is offered by the 3dB quadrature hybrid. So the wave reaching the output port of the phase shifter is changed with a total phase of -90+Θ with reference to the input RF wave. This concept of phase change can be used to implement an RTPS. To get 360 degrees of phase shift the reflective load is varied from minimum (X_{min}) to maximum (X_{max}) and the phase shifting range is given by

$$\Delta\Theta = \Theta(X_{max}) - \Theta(X_{min}) = 2 * tan^{-1}(\frac{X_{max}}{Z_0}) - 2 * tan^{-1}(\frac{X_{min}}{Z_0}) \tag{2.5}$$

To achieve a wide phase shifting range $\Delta\Theta$ should be maximized.

For the 3dB quadrature hybrid coupler a Lange coupler is designed and for the reflective load used is a CLC pi network with two tunable capacitor banks to achieve 360° wide phase shift. The next chapters describe the design of Lange coupler and various reflective loads and design and analysis of the proposed CLC π network with two tunable capacitor banks.

CHAPTER 3

LANGE COUPLER

3.1 Transmission Lines in RFIC

At extremely high frequencies lumped elements do not behave properly and only offer very low-quality factors leading to higher losses in high-frequency circuits. In these cases, transmission line circuits are preferred over lumped element circuits as explained in [7]. But transmission lines are not good in terms of chip area due to their relatively larger sizes. For the higher end of mm-wave applications transmission lines are inevitable. Even at low frequencies, RFIC designers can make use of certain features of transmission lines to implement lumped elements. In this project, a 3dB quadrature hybrid is implemented as a transmission line circuit called Lange coupler named after Julius Lange [5].

The typical CMOS dielectric metal structure used in RFICs consists of metal layers embedded within a multiple layer dielectric above the silicon substrate. The number of metals layers varies with respect to CMOS processes. In the 65nm process, there are 10 layers of metal. Among these 10 metal layers, topmost layers are thicker than lower layers. So the top layers have the lowest conductor loss and are thus preferred for transmission lines. By using multiple metal layer structure of CMOS process two conductor or multiple conductors printed transmission line circuits can be formed which can be used for mm-wave RFICs. Complicated circuits can be realized using metal layers as transmission lines. It also allows horizontal and vertical integration resulting in compact and high-density circuit integration.

Lange coupler was originally implemented by Julius Lange in 1969 on microstrip lines. It is a tight coupling, low loss, broadband quadrature hybrid. To obtain tight coupling inter-digitation of metal layers was used. The original structure was unfolded which in turn reduced the number of via.

3.2 Coupled Line Directional Couplers

Lange coupler is a coupled line directional coupler [6]. When two unshielded transmission lines are close power can be coupled from one line to the other due electromagnetic interactions. Such lines are referred to as coupled transmission lines. Directional couplers based on the coupling between two or more parallel transmission lines are some of the most basic couplers that find popular use in RF circuits. In principle, there are two kinds of coupling in parallel transmission lines: edge and broadside coupling which are shown in figure 3.1. Edge coupling is the coupling along the edge of the coupled lines while broadside-coupling is the coupling across the full or partial width of the coupled lines. Broadside-coupling is suitable for weak, moderate and strong coupling and requires the use of multiple metal layers that are readily available in CMOS structures. On the other hand, edge-coupling needs only a single metal layer and is applicable only for weak and moderate coupling.

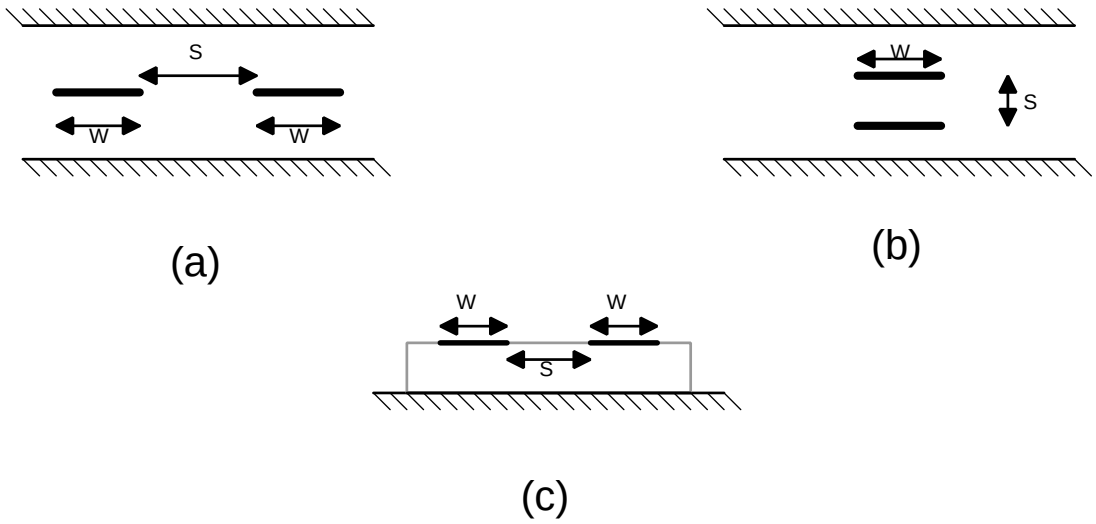

Figure 3.1: Various coupled transmission Line topologies (a)Coupled strip line (edge coupled) (b)Coupled strip line (Broadside coupled) (c)Coupled microstrip line

Generally, it is difficult to achieve 3dB or 6dB coupling. One way to increase edge coupling is to use several lines parallel to each other. So that the fringing field at both edges contributes to the coupling. One of the practical implementations of this idea was Lange coupler where four parallel lines are used with interconnections to provide tight coupling. This coupler can achieve 3dB coupling. There is a 90-degree phase difference between through and coupled ports, so it is a quadrature hybrid. The main disadvantage of the Lange coupler is probably practical, as the lines are very narrow and

close together, and the required bonding wires across the lines increases complexity. This type of coupled line geometry is also referred to as inter digitized, such structures can also be used for filter circuits.

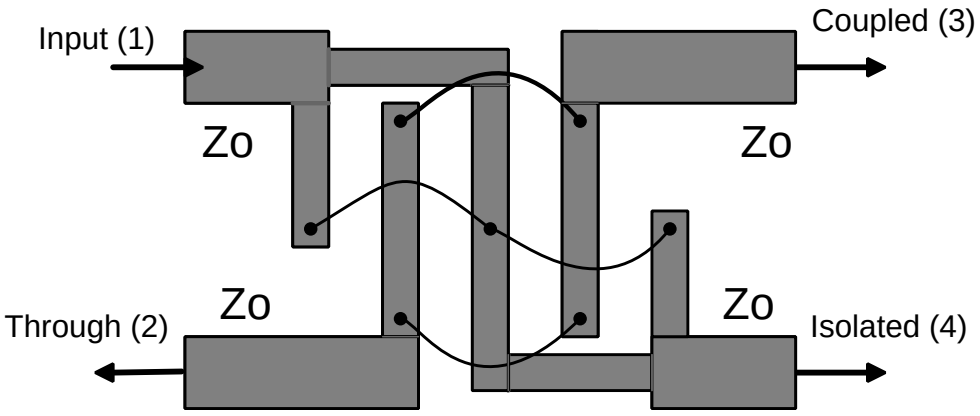

Figure 3.2: Folded Lange Coupler

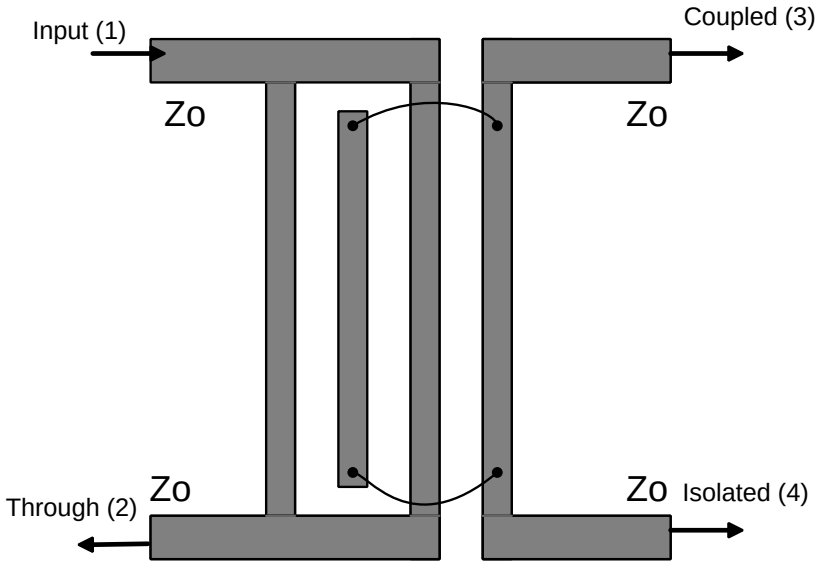

Figure 3.3: Unfolded Lange Coupler

The folded and unfolded versions of Lange coupler have shown in figure 3.2 and 3.3 respectively. The unfolded version of Lange coupler works in the same as that of folded version, but it is easier to model with an equivalent circuit. With the use of tightly stacked multiple metal layers available in CMOS process Lange coupler can be implemented on the silicon CMOS process also. It implements an unfolded Lange coupler in a broadside-coupled structure to facilitate significant size reduction through meandering while simultaneously enhancing the performance through tight broadside coupling. The proposed four-finger Lange coupler designed in TSMC 65nm process is

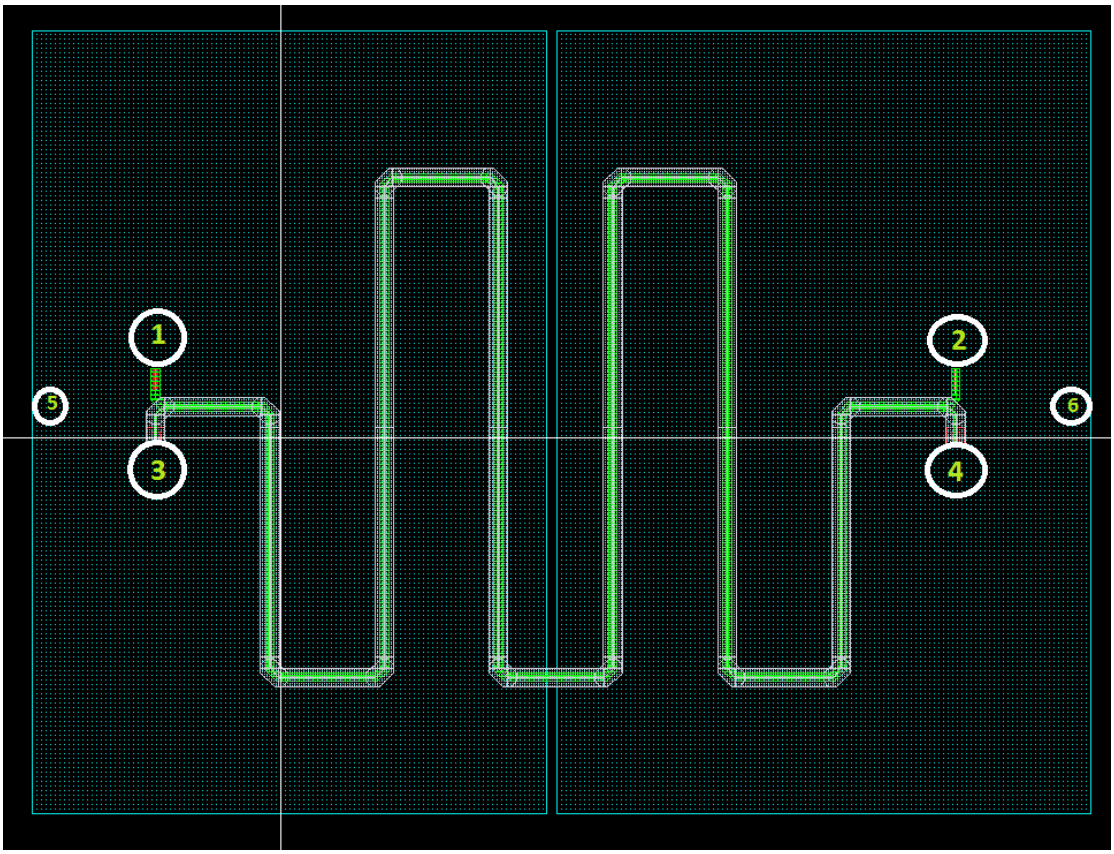

Figure 3.4: Layout of Lange coupler

shown in figure 3.4. It has 6 ports. 4 coupler ports and two ground plane connections from the midpoint of each ground plane. Ports of Lange coupler are

1. Input port
2. Through port
3. Coupled port
4. Output port

Port number 5 and 6 used for ground plane connections.

3.3 Design Procedure of Lange Coupler

Original Lange coupler was designed in strip line which is having the same characteristics for finger metals with respect to the substrate. But in the TSMC CMOS process, each metal layer is having different characteristics such as resistance, thickness, etc with respect to the p substrate. Also, there is a minimum width requirement

for each metal line to pass DRC rules as given below in Table 3.1. And topmost layers are having least resistance thus low loss compared to lower layers.

Metal Layer	**Minimum Width in μ m**
Metal 10 or AP	3
Metal 9	2
Metal 8	0.4
Metal 2-7	0.1
Metal 1	0.09

Table 3.1: Minimum Width of Metal Layers in tsmc 65nm process

Considering these factors the design of Lange coupler was carried out based on [2]. For a four-line directional coupler, the top four layers can be used as coupler layers. Because they are having a low loss. Alternate layers were connected using vias. The electrical length of each line can be calculated from $\lambda/4$ length requirement. Which is obtained as 1358μm at the center frequency of operation 28 GHz Length of the lines should be $\lambda/4$ to obtain a -90° phase difference between input-through and/or coupled-output port.

$$L = \frac{\lambda}{4} \tag{3.1}$$

$$\lambda = \frac{c}{f.\sqrt{\epsilon_r}} \tag{3.2}$$

where λ is the wavelength of EM wave, L is the length of the coupler layer, c is the velocity of light in space, f is the frequency of EM wave and ϵ_r is the relative permittivity of light in the SiO_2 dielectric layer. After calculating the length of coupler layers meandering was done to minimize the chip area as shown in figure 3.4. The entire layout was performed using skill programming language available in cadence. So that it is made easy to tweak the parameter to get desired performances.

Four-line directional coupler based Lange coupler was derived from the two-line directional coupler. Consider a two-line transmission line with a characteristic impedance of 50 Ω. These two line coupler converted into four-line coupler by halving the width of each layer without changing the length. Thus characteristic impedance of each port does not change. So for a 50 Ω input and output impedance matching the characteristic impedance of each coupler layer has to be 100 Ω. So connecting the alternate layers in parallel would give 50 Ω characteristic impedance at input and output. The width of

each layer has to be found out separately because the properties of each layer are different from the other. Also, the distance between the substrate and each layer is different. Initially the four layers were paired as AP-M8 and M9-M7. Full-wave electromagnetic simulations were performed using EMX which is a planar 3D, integral equation solver that uses a very accurate representation of Maxwell's equations aiming to find suitable widths for each layer. Width of each layer then found out to get 100 Ω impedance as follows

Metal Layer	**Width Required for 100 Ω(m)**
Metal 10 or AP	5.3
Metal 9	2
Metal 8	0.4
Metal 7	0.9

Table 3.2: Width Required for 100 Ω for each Metal Layer

For M9 with a width 0f 2μ m (minimum possible width) Z11 (Re)= 75 Ω. So the width of M7 was reduced to minimum width (0.1 μ m) get higher resistance in parallel with M9. The specifications for Lange coupler was simulated after this. The coupling (-3.2dB) was more than through (-7.4dB) the phase shift between through and coupled port was -95°. To reduce the coupling M6 (AP-M8 pair and M9-M6 pair) was used instead of M7 with a width of 0.1 μ m. The coupling got reduced (-3.81 dB) and through (-5.51 dB) got improved. Length of Lange coupler reduced to 1090 μ m to adjust the phase shift and width of M6, M9 and AP was increased to get coupling and through equal. To improve the performances further i.e. making amplitude imbalance close to 0dB the layers again changed. Finally the AP-M5 and M9-M7 pair of layers with below mentioned widths gave -4.325 dB coupling, -4.54 dB through and -90° of phase difference between input-through and/or coupled-output port pairs.

Metal Layer	**Width Required for 100 Ω (μ m)**
Metal 10 or AP	7
Metal 9	2
Metal 5	2.5
Metal 7	0.1

Table 3.3: Final width of coupler layers used

3.4 Ground Plane For Lange Coupler

Silicon substrate used in RFICs has a dielectric constant of 11.7 and low resistivity of 10^3 to 10^5 Ω-cm which results in substantial dielectric loss especially in RF range. To reduce the loss transmission lines should be completely or at least partially shielded from the silicon substrate. So that a ground plane in one of the bottom metal layers should be present below coupler layers. The ground plane layer is chosen depending on the desired performances such as characteristic impedance or dielectric loss etc. This bottom ground plane should be sufficiently wide enough to prevent electrical signals coming from top layers leaking into the substrate. However, as the ground plane approaches the top conductor, both the characteristic impedance and effective dielectric constant increase because more of the electric field lines penetrate the silicon substrate whose relative dielectric constant is higher than that of the SiO_2 dielectric. Thus for the ground plane, M1 is preferred over other layers to reduce the substrate loss.

3.5 Results of Lange coupler

The total chip space used for Lange coupler is 260 μm x 360 μ m. The size reduction is achieved through meandering as mentioned earlier. Simulated results are tabulated in table 3.4. Results are shown in figures 3.5, 3.6 and 3.7. Simulated results are -4.325 dB coupling, -4.54dB through, 12.5dB isolation, more than 14.5 dB return loss at the output and more than 17.5 dB return loss at the input. The simulated amplitude imbalance is 0.16 dB while the measured phase imbalance is -90 $\pm$ 3 degrees over 22 to 34 GHz frequency range. The excess loss is due to the conductor losses of M5 and M7. It is obvious that Lange coupler even on a lossy silicon substrate exhibits superior performance. Results of Lange coupler at the center frequency of operation, 28 GHz are tabulated in Table 3.4

Parameter	Value
S11 (Input Matching)	-17.62 dB
S33 (Output Matching)	-14.54 dB
S41 (Isolation)	-12.48 dB
S21 (Through)	-4.54 dB
S31 (Coupling)	-4.325 dB
S21 deg (Phase Difference Between Input and Through Ports)	-91.7°
S31 deg (Phase Difference Between Input and Coupled Ports)	-1.8°
S21 deg (Phase Difference Between Through and Coupled Ports)	-89.9°
Bandwidth	22 to 32 GHz dB

Table 3.4: Performance Parameters of Lange Coupler

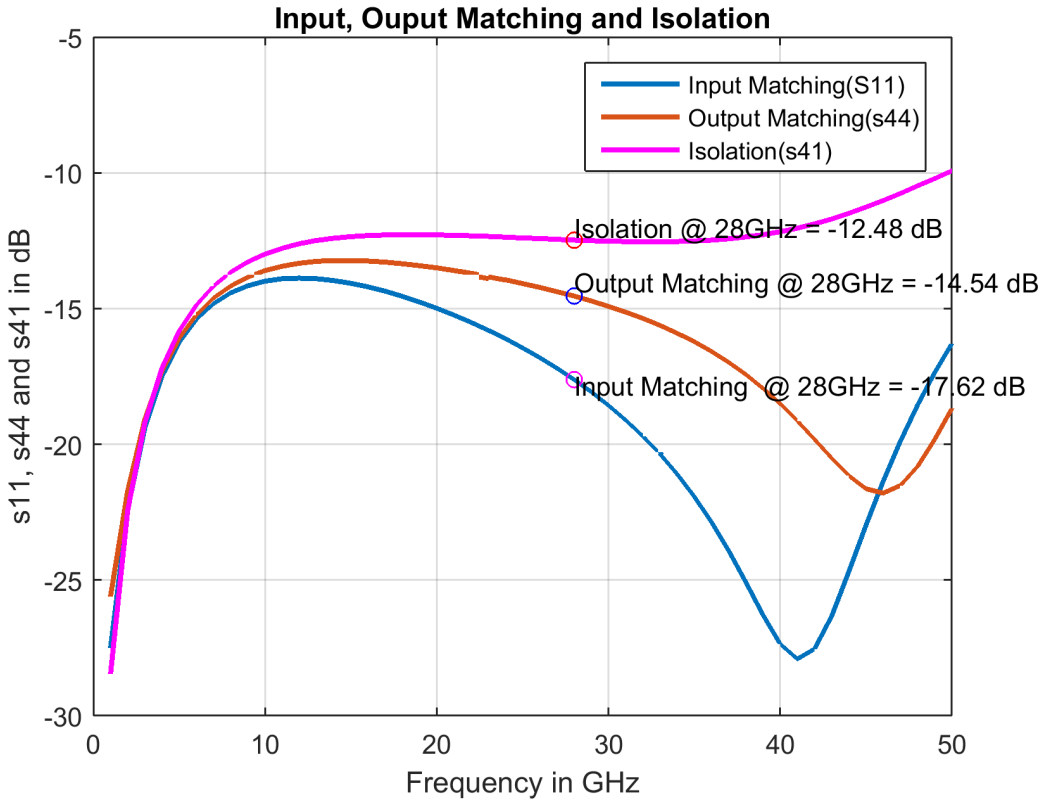

Figure 3.5: Input,Output Matching and Isolation

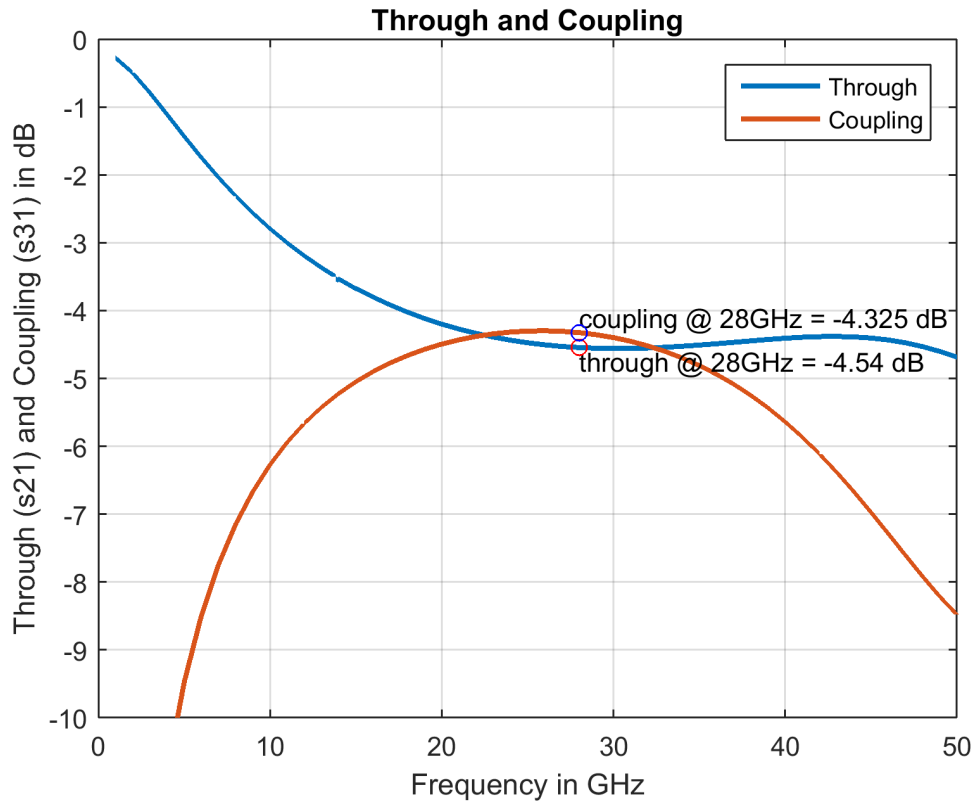

Figure 3.6: Coupling and Through

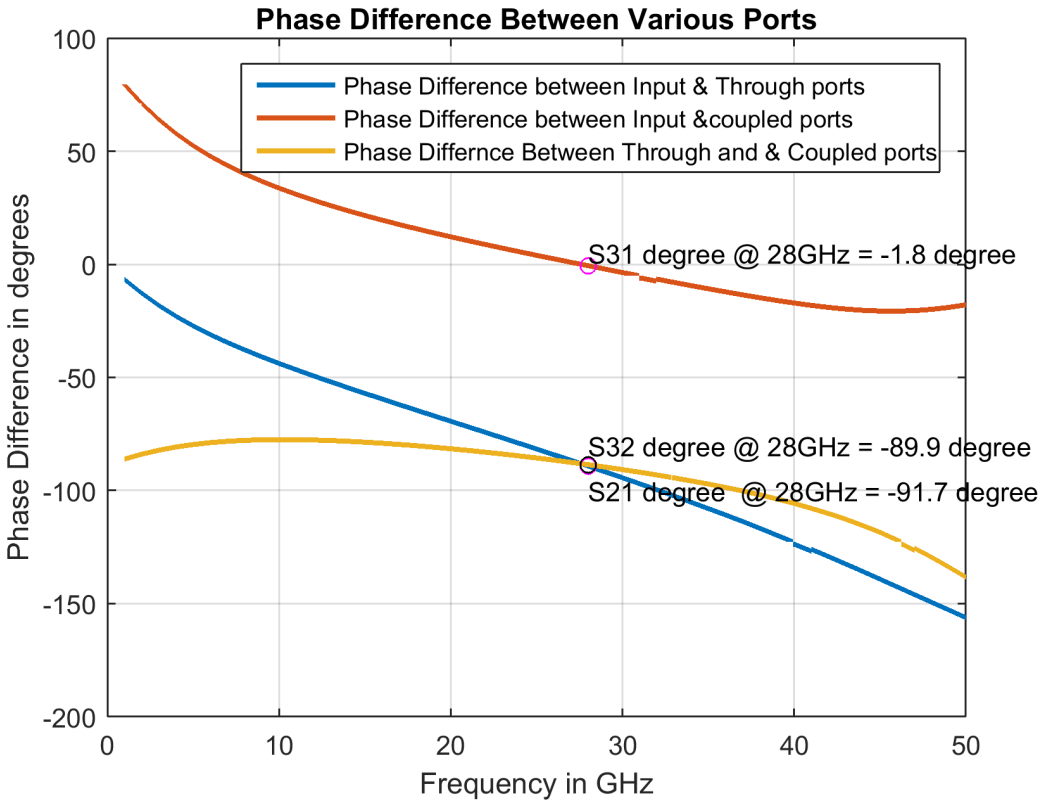

Figure 3.7: Phase Plots of Lange Coupler

CHAPTER 4

VARIOUS REFLECTIVE LOADS

4.1 Introduction

There are various types of reflective loads available to be used in phase shifters. Like

1. Capacitive load (varactor or Capacitor bank)
2. Series LC load
3. Parallel resonance LC load
4. CLC π network with single tunable capacitors
5. CLC π network with two tunable capacitors

Generally, a load is chosen based on the phase shifting range needed. In this project to achieve a 360° phase shift, a CLC π network with two tunable capacitor banks is chosen as the reflective load. The use of a capacitor bank instead of a varactor provides a wide phase shifting range and dense phase angles. But a capacitor bank introduces more loss in the circuit. Analysis of the various reflective loads is given below with the assumption that both coupler and reflective loads are lossless. In this chapter, various types of reflective loads are described briefly.

4.2 Capacitive Load

The capacitive load is the simplest of all reflective loads. It has a tunable varactor or a capacitor bank. Due to change in the capacitive reactance phase of the reflected wave also changes. Figure 4.1 shows a capacitive load and its load impedance tuning trajectory on a Smith chart for a lossless circuit. The load impedance X of the capacitance lies in the bottom half of the Smith chart. Capacitance can be varied from C_{min}

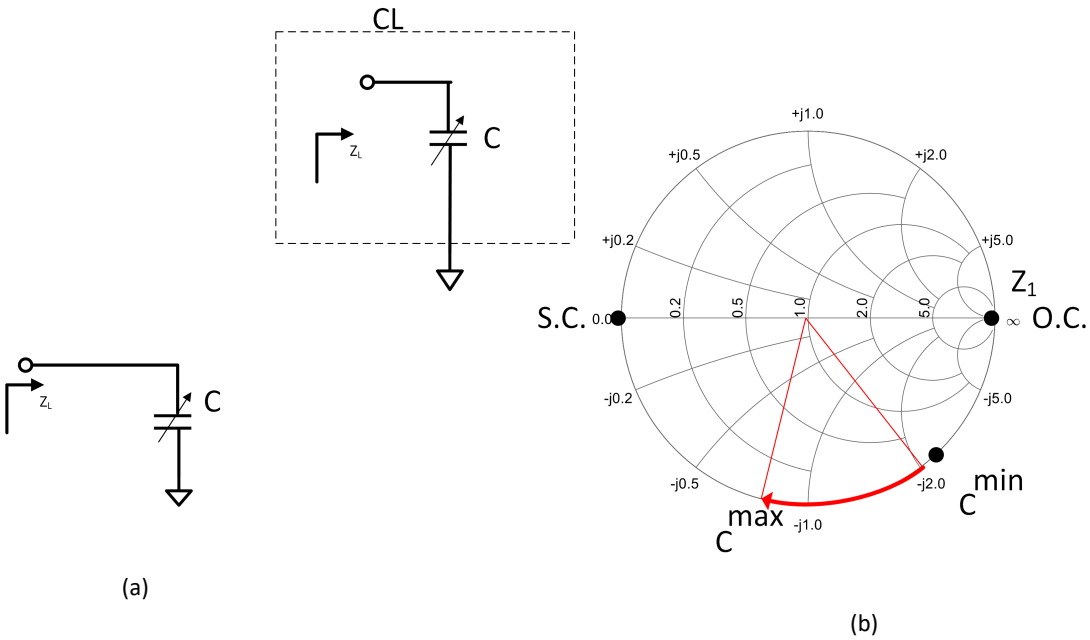

Figure 4.1: (a)Capacitive Load and it's (b) Load Impedance Trajectory

to C_{max}.Thus the phase shift provided by a capacitive load is determined by C_{min} and C_{max}. For a capacitive load, the total phase shift can be expressed as

$$\Delta\Theta = 2tan^{-1}(\frac{1}{Z_0\omega_0 C_{max}}) - 2tan^{-1}(\frac{1}{Z_0\omega_0 C_{min}}) \tag{4.1}$$

Assume $\alpha = \frac{C_{max}}{C_{min}}$ then equation 4.1 can be rewritten as

$$\Delta\Theta = 2tan^{-1}(\frac{1}{Z_0\omega_0 \alpha C_{min}}) - 2tan^{-1}(\frac{1}{Z_0\omega_0 C_{min}}) \tag{4.2}$$

This can be further simplified as

$$\Delta\Theta = 2tan^{-1}(\frac{Z_0\omega_0 C_{min}(\alpha - 1)}{\alpha(Z_0\omega_0 C_{min})^2 + 1}) \tag{4.3}$$

From equation 4.3 we can find out the optimum value of C_{min} such that total phase shift due to a single tunable capacitor is maximized. For the varactor available from PDK (Process design kit)are having lower $\frac{C_{max}}{C_{min}}$ ratios. But in the case of capacitor banks, we have an additional degree of freedom on $\frac{C_{max}}{C_{min}}$ ratio. So to achieve a wider phase shift capacitor banks are preferred over varactor.

4.3 Series LC Resonant Load

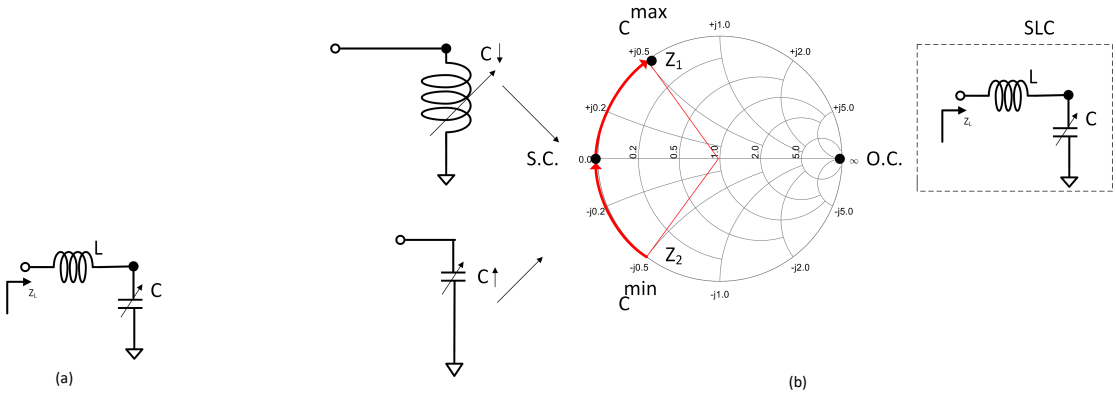

Figure 4.2: (a) Series LC Resonant Load and it's (b) Load Impedance Trajectory

To further extend the phase shifting range series LC loads are used in RTPS. Series LC loads can produce a single resonance i.e. short circuit for the load impedance. A series LC resonant load and its load impedance tuning trajectory are shown in figure 4.2 Increasing capacitance makes the load impedance move towards inductive nature and forming a series resonance. The total phase shift of a series LC load can be calculated by the phase difference achieved by changing the capacitor from C_{min} to C_{max}.

The looking in impedance of a series load is given by

$$X = \frac{\omega^2 LC - 1}{\omega_0 C} \tag{4.4}$$

The phase shifting range of series LC load can be given by

$$\Delta\Theta = 2tan^{-1}(\frac{\omega^2 LC_{max} - 1}{Z_0\omega_0 C_{max}}) - 2tan^{-1}(\frac{\omega^2 LC_{min} - 1}{Z_0\omega_0 C_{min}}) \tag{4.5}$$

4.4 Parallel LC Load

The parallel LC circuit also can be used for RTPS. Parallel LC can produce a single resonance point i.e. an open circuit for the load impedance. A parallel LC resonant load and its load impedance tuning trajectory are shown in figure 4.3. If the capacitance is at C_{min} the effective looking in impedance will be an inductive reactance. As the capacitance is increased the load will move towards the capacitive region. At some point, a parallel LC load forms a resonance and the load impedance will become infinity. If

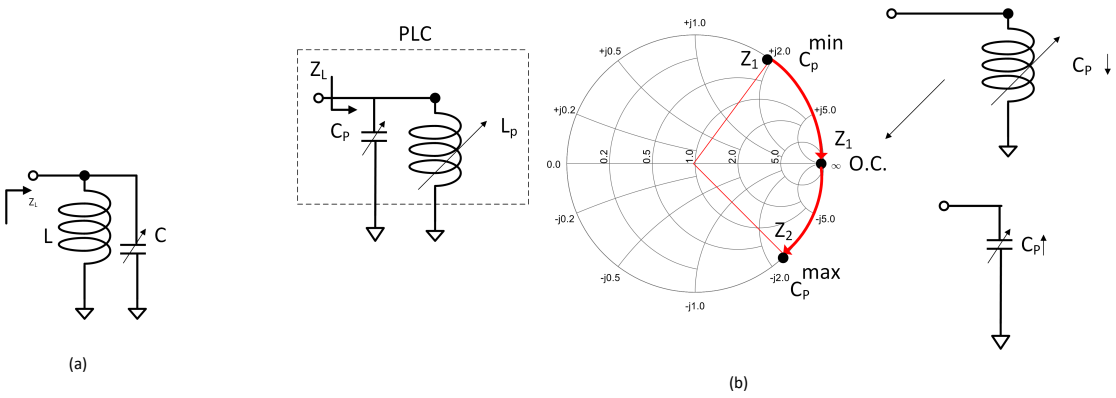

Figure 4.3: (a) Parallel LC Resonant Load and it's (b) Load Impedance Trajectory

we further increase the capacitance the effective impedance will be a capacitive reactance. Similar to the series LC load the phase shifting range of parallel LC load also determined by the phase difference achieved by changing the capacitor from C_{min} to C_{max}.

The looking in impedance of a parallel LC load is given by

$$X = \frac{\omega_0 L}{1 - \omega^2 LC} \tag{4.6}$$

The phase shifting range of parallel LC load is given by

$$\Delta\Theta = 2tan^{-1}(\frac{\omega_0 L}{Z_0(1 - \omega^2 LC_{max})}) - 2tan^{-1}(\frac{\omega_0 L}{Z_0(1 - \omega^2 LC_{min})}) \tag{4.7}$$

4.5 CLC π network with single tunable capacitor

A CLC π network has additional degree of freedom compared to above discussed reflective loads. So it can provide more than $180°$ phase shift. If the capacitor bank is tuned extensively it can produce two resonance points i.e. open circuit and short circuit. A CLC π network with single tunable capacitor and its load trajectory for a loss less network are shown in figure 4.4. Total looking in impedance is given by

$$X = \frac{1 - \omega_0^2 LC_2}{\omega_0(C_1 + C_2 - \omega_0^2 LC_2 C_1)} \tag{4.8}$$

Suppose the capacitor bank C2 is at its minimum value, $C2_{min}$ the total looking in impedance will be capacitive reactance. If we increase the capacitance C2 the total

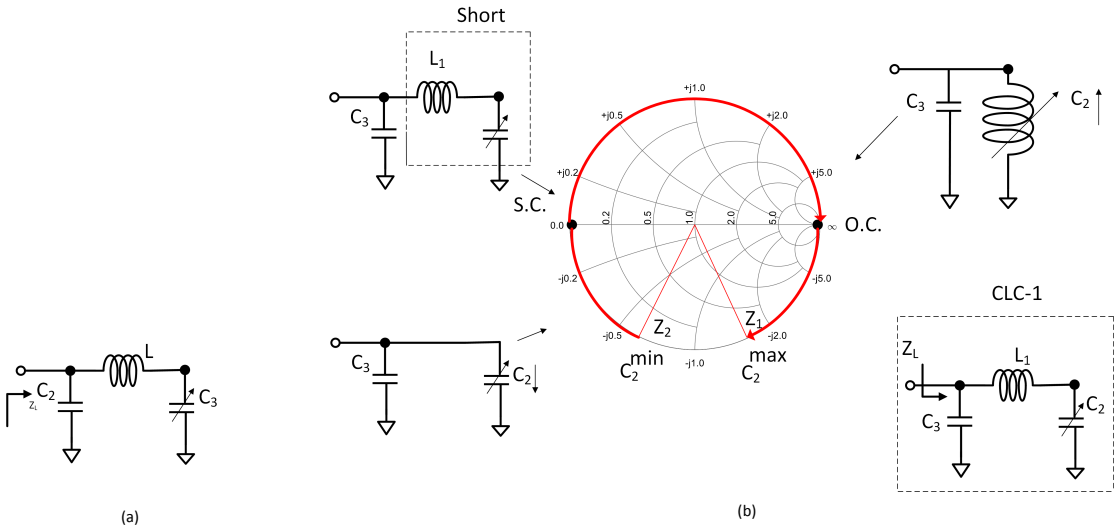

Figure 4.4: (a) CLC π network with single tunable capacitor and its (b) Load Impedance Trajectory

impedance will move towards the inductive region as shown in the Smith chart. Once the L C_2 series resonance happens the impedance will become zero introducing a short circuit. On further increasing the capacitance X will become inductive. And by extensively increasing the capacitance C_2 we can produce the open circuit resonance also again moving the looking in impedance to capacitive reactance. The fixed value of C1 also determines the starting and ending points of the phase shift.

The total phase shifting range of CLC π network is given by

$$\begin{aligned}\Delta\Theta = 2tan^{-1}(\frac{1-\omega^2 LC3_{max}}{Z_0\omega_0(C2+C3_{max}-\omega^2 LC3_{max}C2)}) \\ -2tan^{-1}(\frac{1-\omega^2 LC3_{min}}{Z_0\omega_0(C2+C3_{min}-\omega_0^2 LC3_{min}C2)})\end{aligned} \tag{4.9}$$

4.6 CLC π network with two tunable capacitors

A CLC π network type of reflective load has an additional degree of freedom to achieve a wide phase shifting range compared to previously discussed reflective loads. It allows both C1 and C2 tunable to get a 360° phase shift.

A CLC π network load and its load impedance trajectory for a loss less circuit in figure 4.5. The total impedance looking in is given by

$$X = \frac{1-\omega_0^2 LC_2}{\omega_0(C_1+C_2-\omega_0^2 LC_2C_1)} \tag{4.10}$$

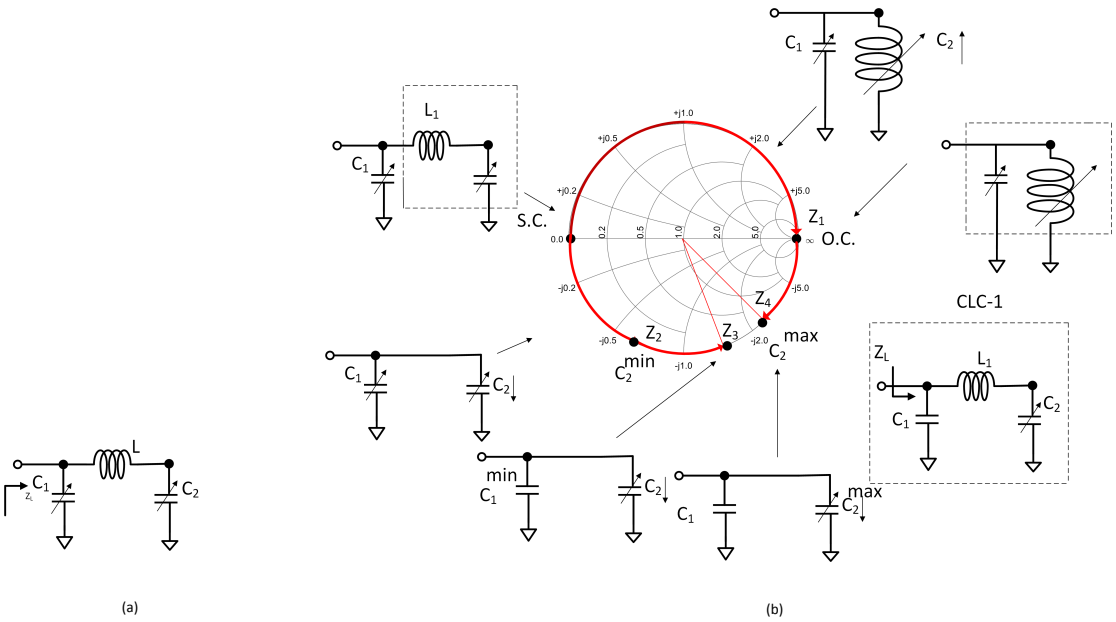

Figure 4.5: (a) CLC π network with two tunable capacitors and its (b) Load Impedance Trajectory

Suppose both the capacitor banks are at their minimum value of $C2min$ and $C1_{min}$. Then the effective looking in impedance will be capacitive. If we increase the value of C2 the total impedance X will move towards the inductive region as shown in the Smith chart. Once the LC_2 series resonance happens the impedance will become zero introducing a short circuit which is shown in the Smith chart. If we further increase the C_2 the total impedance will become inductive. Once the C2 has reached its maximum value, $C2_{max}$ we have to increase $C1$ from minimum to maximum. As we increase C_1 the LC_1 parallel resonance will form an open circuit. If we increase C_1 further the total reactance will become capacitive again and can cross the minimum point. So $360°$ phase shift is achieved. Choose the minimum and maximum values for C1 and C2 such that $360°$ phase shift is achievable. The total phase shift in terms of minimum and maximum capacitance of C1 and C2 is given by

$$\Delta\Theta = 2tan^{-1}\left(\frac{1-\omega^2 LC2_{max}}{Z_0\omega_0(C1_{max}+C2_{max}-\omega^2 LC2_{max}C1_{max})}\right) - 2tan^{-1}\left(\frac{1-\omega^2 LC2_{min}}{Z_0\omega_0(C1_{min}+C2_{min}-\omega_0^2 LC2_{min}C1_{min})}\right) \tag{4.11}$$

CHAPTER 5

CLC-2 REFLECTIVE LOAD DESIGN

A two tunable capacitor bank CLC π network contains two capacitor banks which may be either identical or not, an inductor and the MOSFET switch biased in the linear region of operation. Both capacitor bank has different minimum fixed capacitance and identical binary weighted capacitors for the simplicity of design. A fixed minimum capacitance gives additional freedom of design as described later. Other design parameters are inductance value and width and length of MOSFET switches.

5.1 Design Procedure

Assume

$$\alpha = \frac{C_{max}}{C_{min}} \tag{5.1}$$

Where C_{min} = Fixed minimum capacitance in the capacitor bank

For a capacitor, Capacitive reactance

$$X = \frac{1}{\omega_0 C_{min}} \tag{5.2}$$

The phase shifting range of a capacitor bank is given by

$$\Delta\Theta = 2tan^{-1}(\frac{1}{Z_0\omega_0 C_{max}}) - 2tan^{-1}({}_0C_{min}) \tag{5.3}$$

Using equation 5.1

$$\Delta\Theta = 2tan^{-1}(\frac{1}{Z_0\omega_0\alpha C_{max}}) - 2tan^{-1}(\frac{1}{Z_0\omega_0 C_{min}}) \tag{5.4}$$

$$\Delta\Theta = 2tan^{-1}(\frac{Z_0\omega_0 C_{min}(\alpha-1)}{\alpha(Z_0\omega_0 C_{min})^2+1}) \tag{5.5}$$

To get a wide phase shift range $\Delta\Theta$ should be maximized. To find the optimum value of C_min for which $\Delta\Theta$ is maximized, take derivative of $\Delta\Theta$ w.r.t C_{min}

$$\frac{d(\Delta\Theta)}{dC_min} = 0 \tag{5.6}$$

Thus optimum value of C_{min} in terms of α found out to be

$$C_{min} = \frac{1}{\sqrt{\alpha}.Z_0.\omega_0} \tag{5.7}$$

From equation 5.1

$$\alpha = \frac{C_{min} + 2^{N-1}C_{LSB}}{C_{min}} \tag{5.8}$$

where N =Number of capacitors in capacitor bank and C_{LSB} =LSB capacitance of capacitor bank

$$\alpha = 1 + \frac{2^{N-1}C_{LSB}}{C_{min}} \tag{5.9}$$

Using equation 5.7

$$\alpha = 1 + 2^{N-1}C_{LSB}\sqrt{\alpha}Z_0\omega_0 \tag{5.10}$$

Solve the above quadratic equation to find the value of α then C_{min}
Assume β = $\frac{C1_{min}}{C2_{min}}$ Phase shifting range of CLC-2 network can be expressed as

$$\begin{aligned}\Delta\Theta = 2tan^{-1}(\frac{1-\omega^2LC2_{max}}{Z_0\omega_0(C1_{max}+C2_{max}-\omega^2LC2_{max}C1_{max})}) \\ - 2tan^{-1}(\frac{1-\omega^2LC2_{min}}{Z_0\omega_0(C1_{min}+C2_{min}-\omega_0^2LC2_{min}C1_{min})})\end{aligned} \tag{5.11}$$

Optimum Value of L can be found out by taking derivative of $\Delta\Theta$ w.r.t L

$$\frac{d(\Delta\Theta)}{dL} = 0 \tag{5.12}$$

$$\mathrm{L}_{opt} = \frac{\sqrt{\beta(\omega_0 Z_0 C2_{min})^2(\beta(\alpha C2_{min})^2[1+(\omega_0 Z_0(1+\beta))^2]+\beta-2\alpha)+1)}\alpha\beta(1+\beta)(\omega_0 Z_0 C2_{min})^2)-1}{\alpha(\alpha+1)(\beta{\omega_0}^2 Z_0 C2_{min})^2 C2_{min}} \tag{5.13}$$

These equations are simultaneously solved using MATLAB and simulation using cadence were run to find out suitable values of capacitance values and inductance. From the simulations, it was sound out that 6-bit capacitor bank was most suitable for the implementation of an RTPS along with a varactor to achieve dense phase angle. The circuit of the designed capacitor bank is shown in figure 5.1. Since both capacitor banks are 6 bits and each of them switched individually there are 128 phase settings or switch points in total.

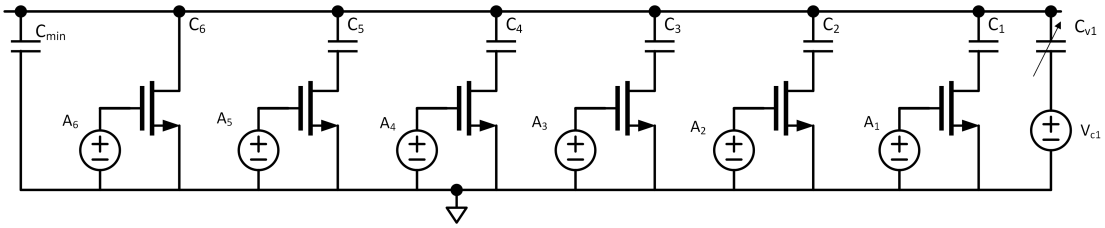

Figure 5.1: Capacitor bank circuit

5.2 Linear Switch Design

For switching the capacitor bank MOSFETs (NMOS rf due to its low ON resistance for the same size) devices are used in the linear region of operation. Switches in the linear region give good linearity for overall circuit and there is no DC current flow in the circuit. Design parameters of a switch are its width and channel length. The switch is designed after considering it's ON capacitance, OFF capacitance, ON resistance and OFF resistance.

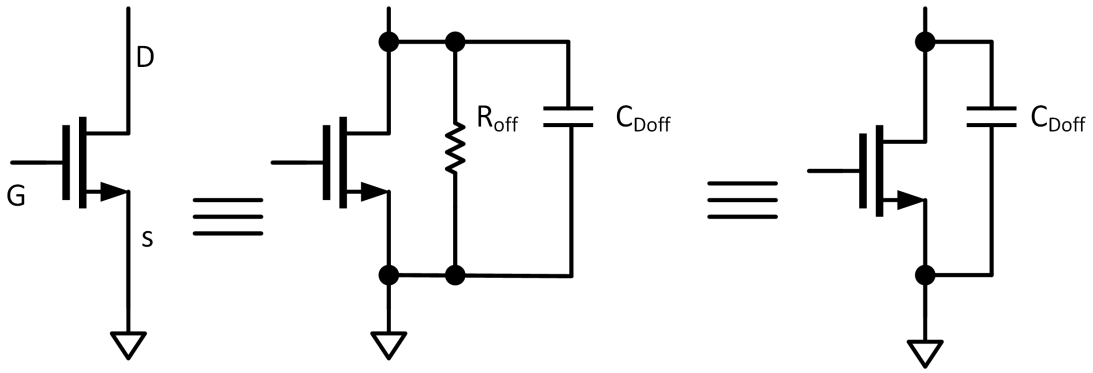

Figure 5.2: MOS switch in ON state and its equivalent circuit

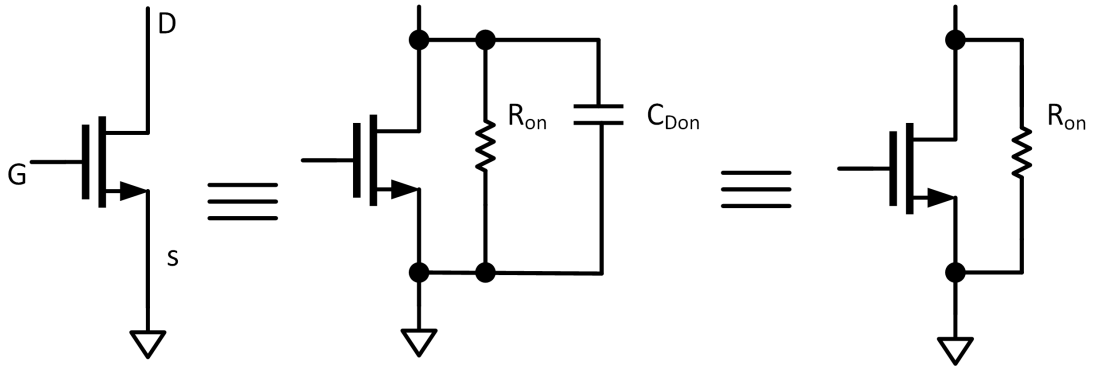

Figure 5.3: MOS switch in OFF state and its equivalent circuit

MOSFET switch and its equivalent circuits are shown for ON conditions in figure 5.2. When the switch is ON the total impedance at the drain node of NMOS is an ON resistance (R_{on}) in parallel with ON drain capacitance C_{Don}. In which R_{on} falls in the range of 10's of Ωs and capacitive reactance of C_{Don} falls in the ranges of few KΩs at the center frequency of operation. So the approximate impedance looking in at the drain of NMOS is R_{on}.

$$Z_{on} = R_{on}||\frac{1}{j\omega_0 C_{Don}} \approx R_{on} \tag{5.14}$$

MOSFET switch and its equivalent circuits are shown for OFF conditions in figure 5.3. When the switch is OFF the total impedance at the drain node of NMOS is an OFF resistance (R_{off}) in parallel with OFF drain capacitance C_{Doff}. In which R_{off} falls in the range of few MΩs and capacitive reactance of C_{Doff} falls in the ranges of few KΩs at the center frequency of operation. So the approximate impedance looking in at the drain of NMOS is $\frac{1}{j\omega C_{Doff}}$.

$$Z_{on} = R_{off}||\frac{1}{j\omega_0 C_{Doff}} \approx \frac{1}{j\omega_0 C_{Doff}} \tag{5.15}$$

ON resistance of the MOS switch in the linear region of operation is given by

$$R_{on} = \frac{L}{W\mu_n C_{ox}(V_G - V_D - V_T)} \tag{5.16}$$

As the R_{on} increases insertion loss of the circuit increases and R_{on} is proportional to $\frac{L}{W}$.

As the C_{Doff} increases the total phase shift of the circuit decreases and C_{Doff} is pro-

portional to W and L.

From the above two requirements, it is evident that we need to reduce both R_{on} and C_{Doff}. Since both parameters are proportional to L, the value L is kept minimum i.e. 60nm. There is a contradictory requirement in the case of the width of MOSFET used. To reduce the loss W should be increased and to increase the total phase shift W should be decreased. Suitable width of MOSFET found out by running simulations such that 360° phase shift is achieved such that loss is minimized. After finding the width of MOSFET switch in series with C_{LSB} binary weighted fingers were used for binary weighted capacitors.

5.3 Results of Reflective Load

The reflection coefficient (figure 5.4) and the phase shift between successive points for both capacitor banks(5.5 (a) and (b)) are shown below. Since the load is not ideally

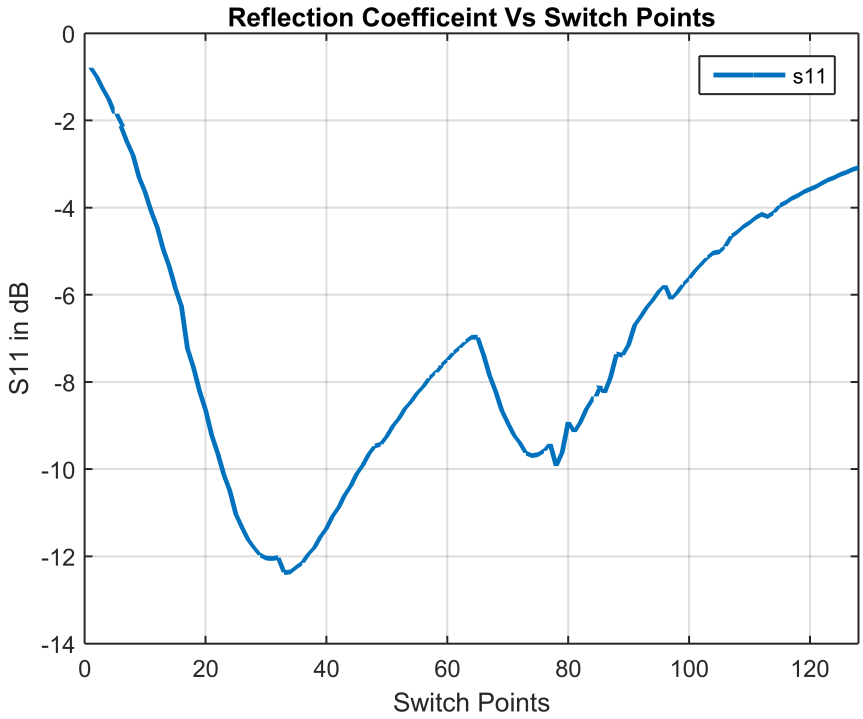

Figure 5.4: Reflection coefficient of reflective load

reactive some part of the signal gets dissipated in the reflective loads. Since the return loss is very high (s11 > -12.2 dB)we can say that most of the wave gets reflected into the input port. The phase shift between successive points is shown below. These results are without using the varactor which is used to achieve the 5° resolution. The highest

phase shift between adjacent switch points due to C2 capacitor bank is 7.4° and that of C1 capacitor bank is 8.3°.

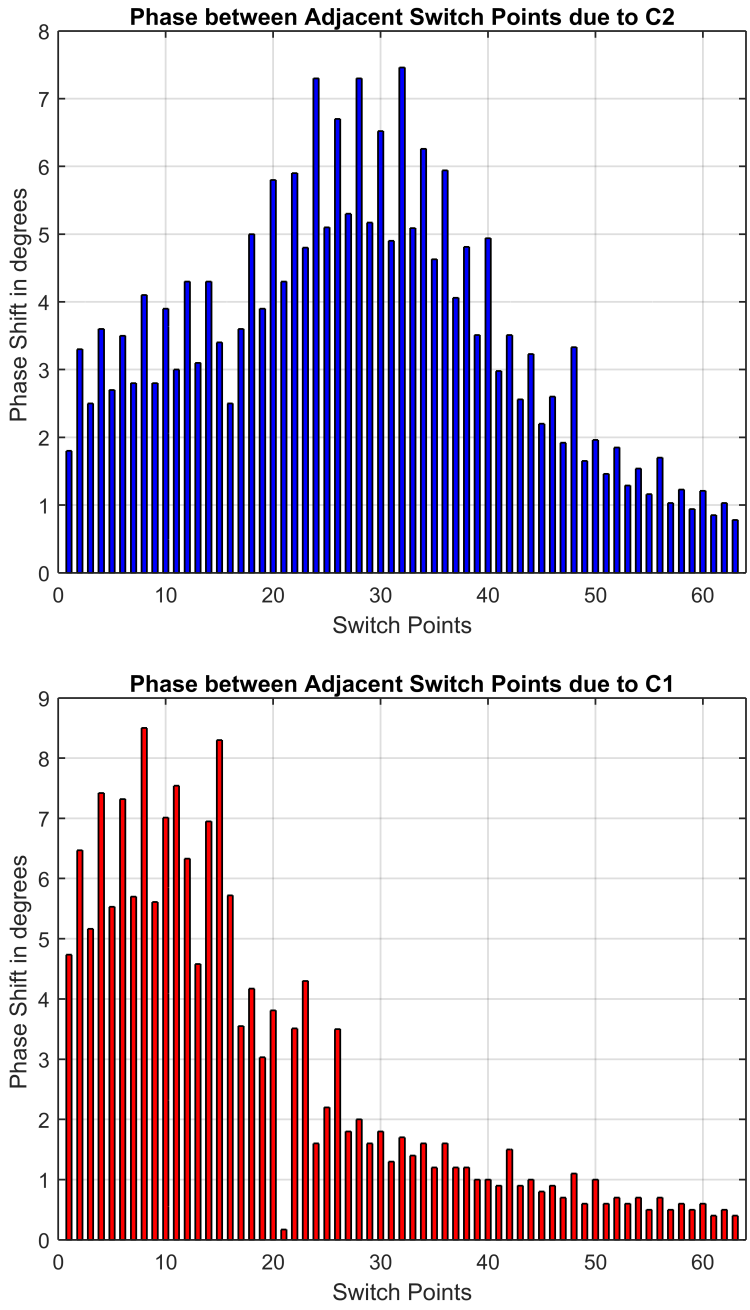

Figure 5.5: Phase shift between adjacent points due to capacitor bank (a) C2 and (b) C1

CHAPTER 6

LAYOUT AND RESULTS OF REFLECTIVE TYPE PHASE SHIFTER

6.1 Layout and results of RTPS

A snapshot of the RTPS and the two capacitor banks are shown in figure 6.1 and 6.2. In the layout, a 1.5 turn inductor is chosen to reduce the wiring parasitic between the Lange coupler and reflective load.

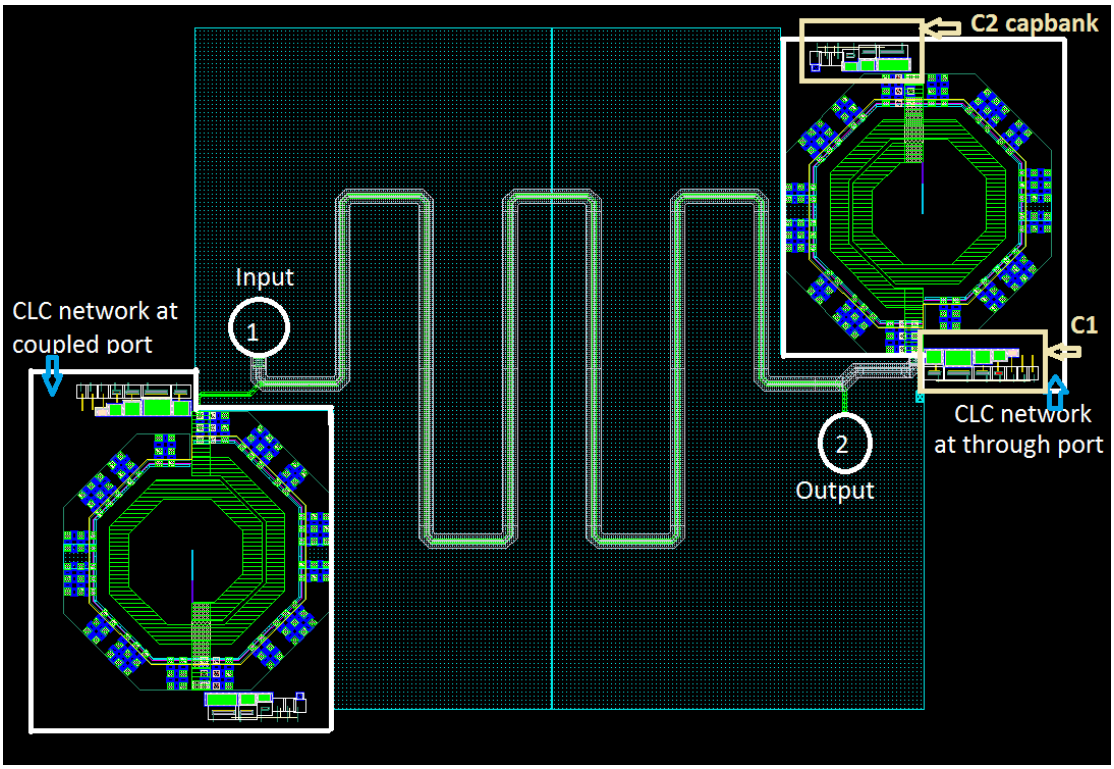

Figure 6.1: Layout of RTPS

Results of the proposed RTPS are shown below from figure 6.3 to 6.6 .Also phase shift between adjacent switching points after including the varactor which is used to get dense phase angles are shown in figure 6.7. A summary of the results are given in table 6.1.

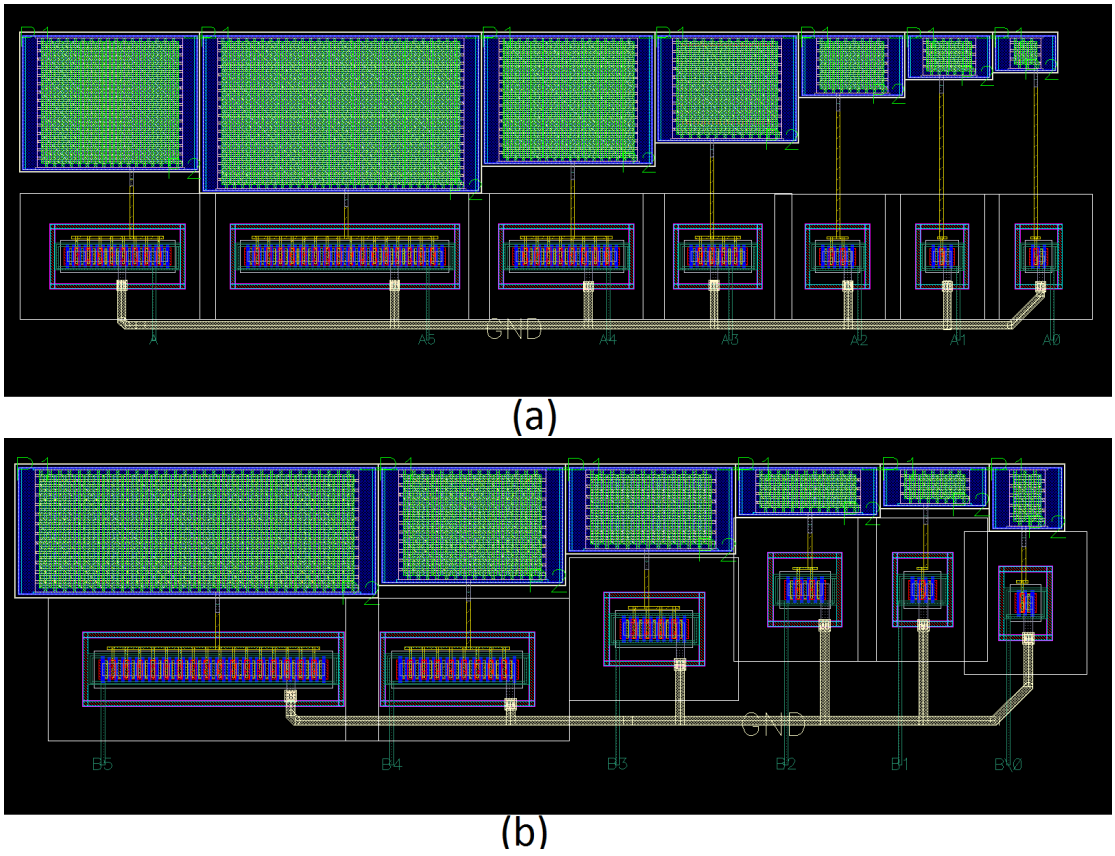

Figure 6.2: Layout of capacitor banks (a) C1 (b) C2

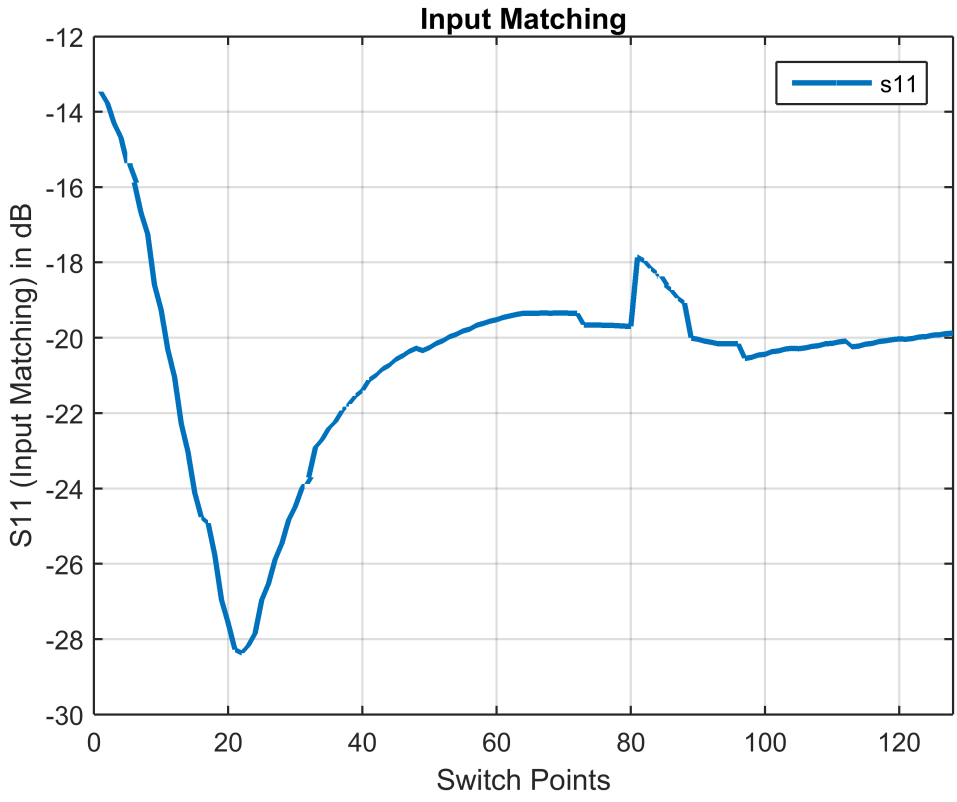

Figure 6.3: Input matching of phase shifter

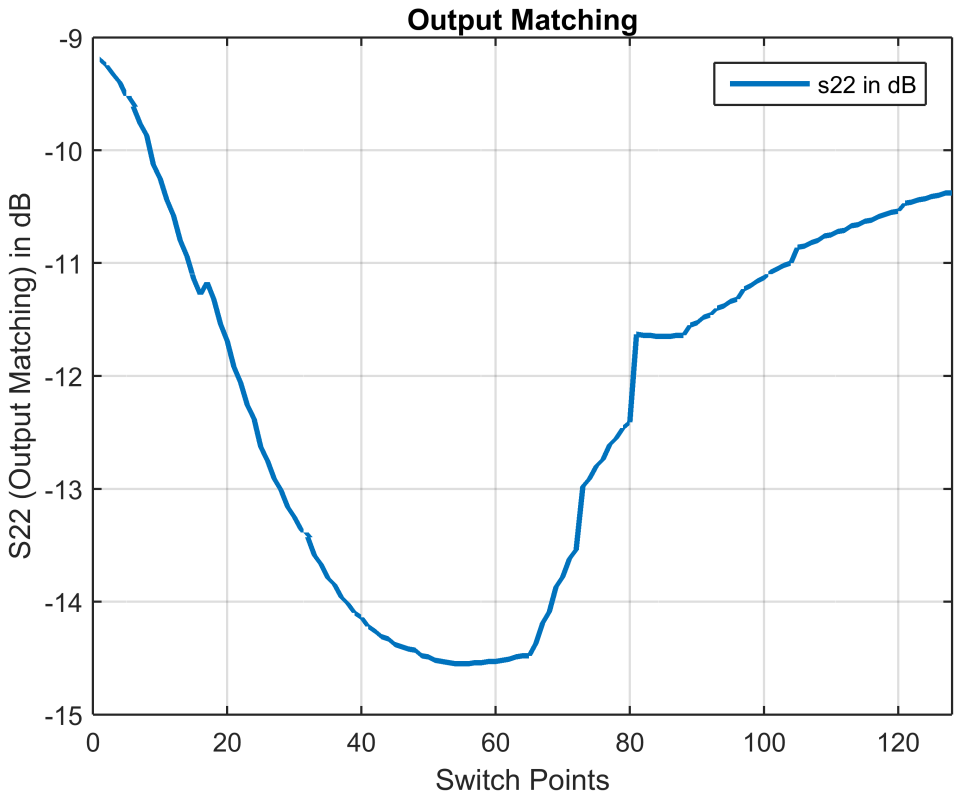

Figure 6.4: Output matching of phase shifter

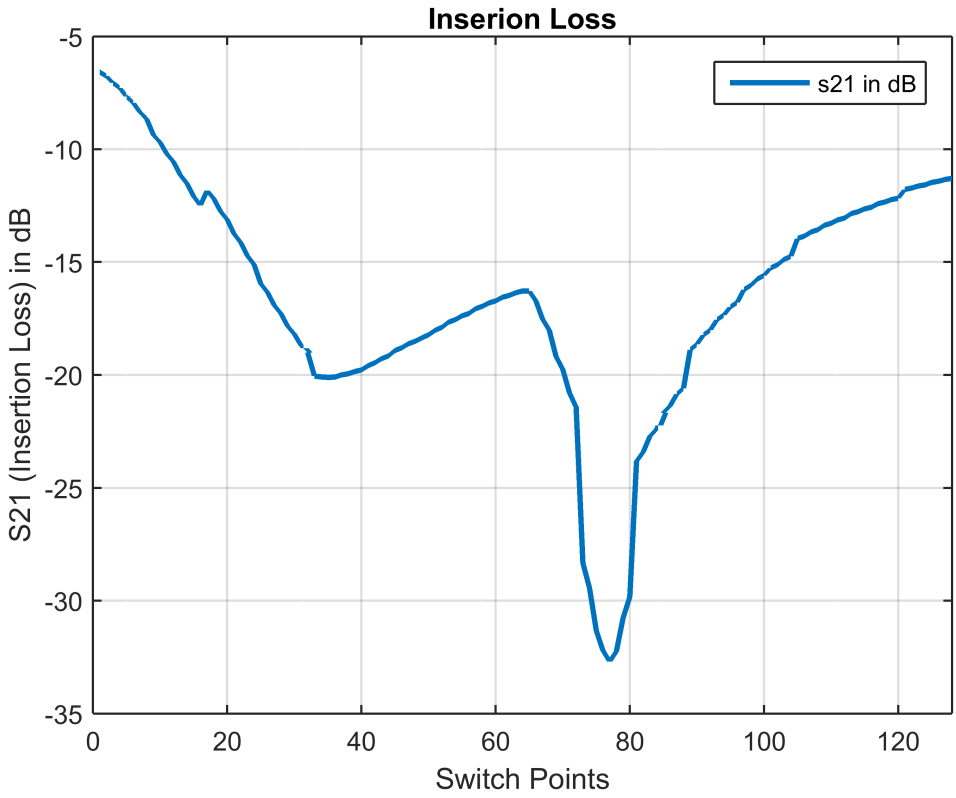

Figure 6.5: Insertion Loss of phase shifter

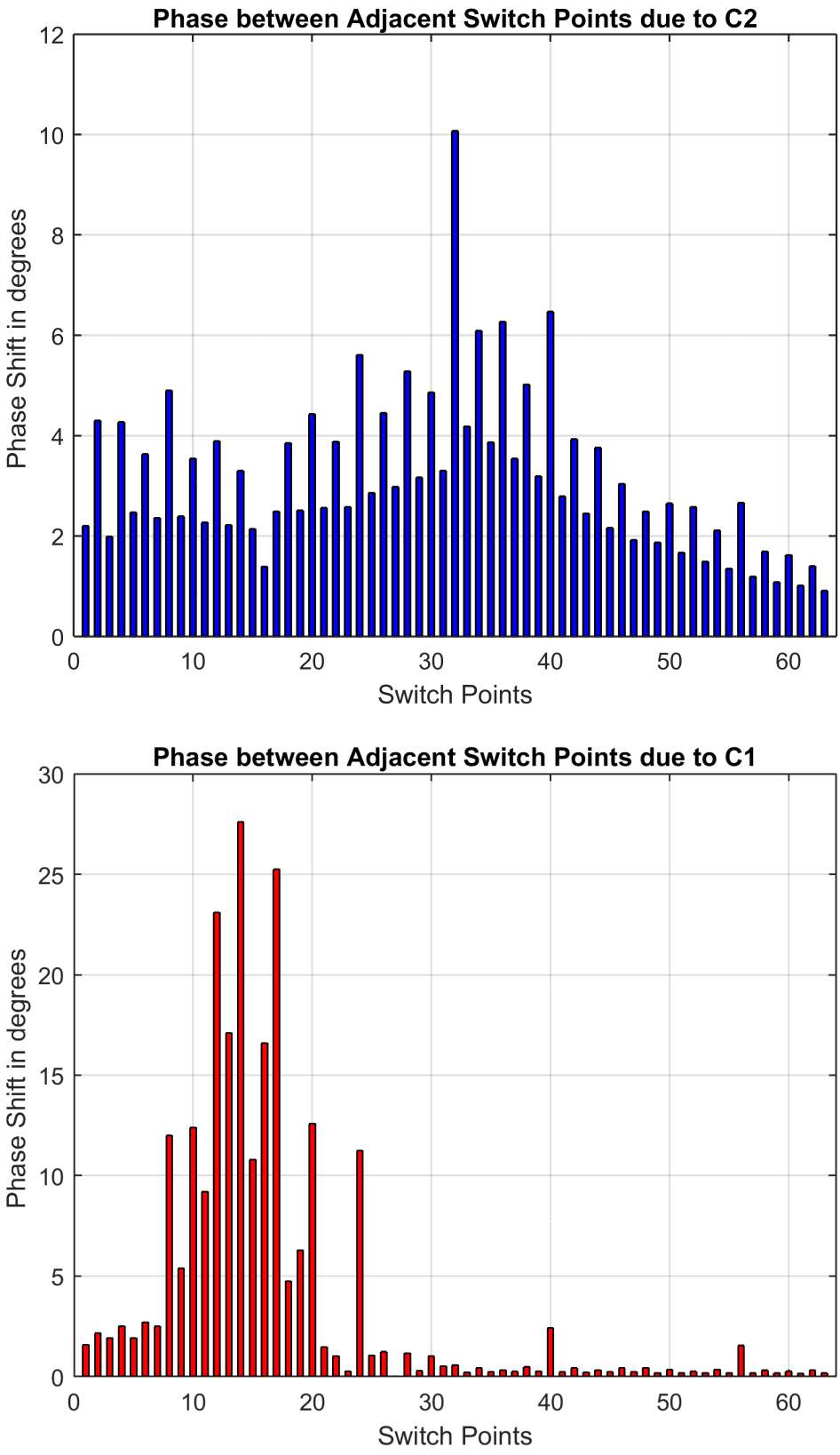

Figure 6.6: Phase shift between adjacent points due to capacitor bank (a) C2 and (b) C1

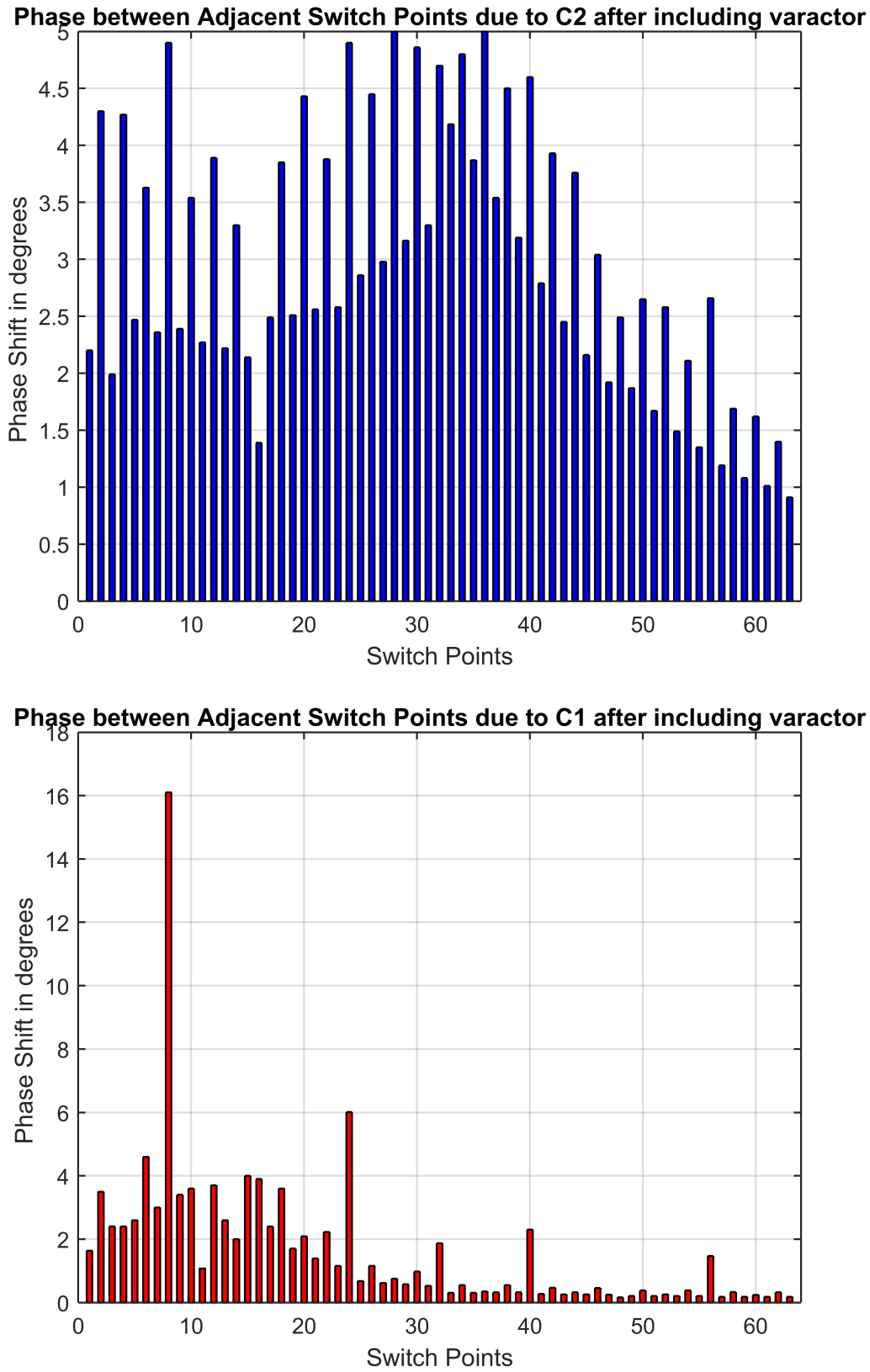

Figure 6.7: Phase shift between adjacent points due to capacitor bank (a) C2 and (b) C1 after including the varactor

Parameter	Due to C2	Due to C1
Phase shift	102.5° to -91.5°	-91.5° to 72°
Highest phase shift between adjacent switching points	10 °	27.5°
S11 (Input Matching)	<-13.47 dB	<-17.85 dB
S22 (Output Matching)	<-9.2 dB	<-10.37 dB
S21 (Insertion Loss)	-6.6 to -20.1 dB	-11 to -32.1 dB

Table 6.1: Performance Parametersof RTPS

6.2 Comparison of proposed RTPS with references

Performance metrics of proposed RTPS compared with that of references are given in Table 6.2. The implemented RTPS achieves a 390° of wide phase shifting range with good input matching and output matching (Return loss less than 13.5dB and 9.2dB). Even though phase resolution is 16° this situation happens for only one phase setting. For other phase settings, a phase resolution of less than 5° can be achieved using the varactor.

[Reference]	[3]	[4]	[8]	This work
Process	65nm CMOS	130nm BiCMOS	65nm CMOS	65nm CMOS
Frequency (GHz)	28	62	61	28
Phase Range (°)	360°	367°	360°	390°
Phase Resolution (°)	11.25 °	-	22.5 °	16°
Input Return Loss (dB)	6.7	10.4	13	13.47
Output Return Loss (dB)	11	10.4	8	9.2
Insertion Loss(dB)	7.45 to 8.05	3.7 to 10.3	-	6.6 to 32.1

Table 6.2: Comparison of performance metrics with references

CHAPTER 7

CONCLUSION

The main performance parameters of an RTPS are input, output matching, insertion loss, wide phase shift range and dense phase angles. Due to the use of Lange coupler input matching and output matching were superior compared to the phase shifter which used a lumped element coupler. varactor produce low loss compared to capacitor banks. Even though the capacitor bank has a higher loss it can achieve wide phase shift range and dense phase angles. A CLC π network based reflective load with two tunable capacitor banks were used with LSB capacitors in the ranges of few femtofarads.

The proposed phase shifter achieved a 390.5° with a phase shift between adjacent switching points less than 5° except at two points (16° and 6°) for C1 capacitor bank with a maximum insertion loss of 32.1 dB.

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