10-bit 100MSPS SAR ADC in TSMC 65nm GP process

A Project Report

submitted by

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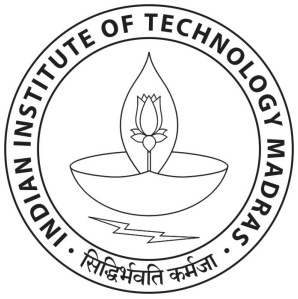
in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
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MAY 2019

THESIS CERTIFICATE

This is to certify that the thesis titled **10-bit 100MSPS SAR ADC in TSMC 65nm GP process**, submitted by **Pallat Aravind**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

A 100MS/s SAR ADC in TSMC 65nm GP process is presented here. The architecture uses monotonic switching where the input common mode voltage is gradually grounded as the conversion is achieved.At a 1.2-V supply and 100 MS/s, the ADC achieves an SNDR of 59.0 dB and consumes 0.685 mW, resulting in a figure of merit (FOM) of 11.72 fJ/conversion-step.

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ABBREVIATIONS

SAR	Successive Approximation Register
ADC	Analog to Digital Converter
SNR	Signal to Noise ratio
SNDR	Signal to Noise and Distortion ratio
ENOB	Effective Number of Bits
SFDR	Spurious Free Dynamic Range
FFT	Fast Fourier Transform

CHAPTER 1

SAR ARCHITECTURE

1.1 Monotonic Switching Procedure

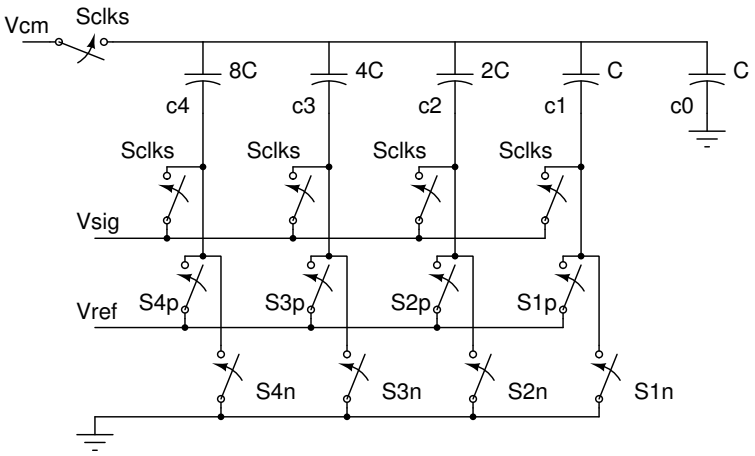

Figure 1.1: Capacitor Bank Bottom plate sampling

A single sided sample capacitor bank for bottom plate sampling is shown in Fig. 1.1. Conventional SAR switching procedure for a 4-bit ADC is shown in Fig. 1.2. In the conventional switching procedure the input signal (differential) is sampled onto the bottom plates of the binary weighted capacitors. At the end of the sampling phase, the common mode voltage fed to the top plate is turned off and all the bottom plates voltages except the MSB capacitor(c4) are set to ground. Based on the decisions made by the comparator during successive bit resolution the procedure evolves as shown in Fig 1.2.

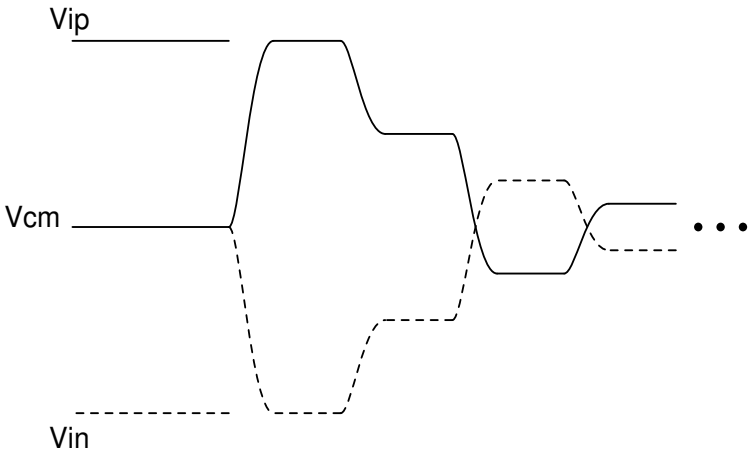

Figure 1.2: Conventional Switching procedure

In each step one of the capacitor's bottom plate voltage is set to Vref and then tested with the comparator. This method spends unnecessary power when a bottom plate voltage has to be reset to ground. An improvisation of this method is the monotonic switching procedure in which the signal is sampled onto the top plate of the capacitor as opposed to the bottom plate. The capacitor bank arrangement is shown in Fig.1.3 and monotonic swithcing procedure is shown in Fig.1.4. With this method, in any step the bottom plate voltage need not compulsorily be set to Vref before testing with the comparator. After each step only one of the differential capacitor pair is switched to ground. It is evident that the number of transitions is always constant irrespective of the input voltage and also the number of transitions in monotonic switching procedure is always equal to the best-case scenario in the conventional method (excluding the compulsory initial step in conventional method).

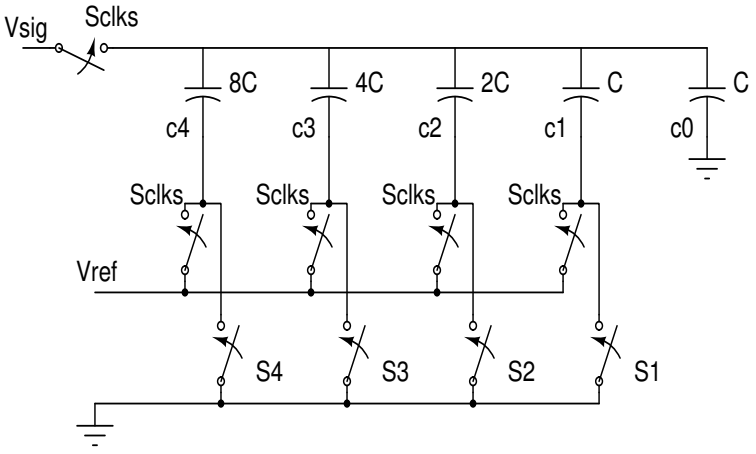

Figure 1.3: Capacitor bank top plate sampling

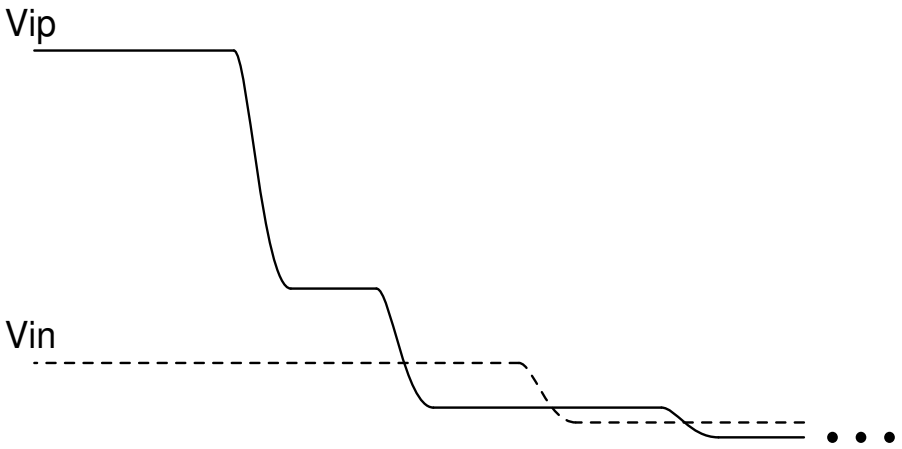

Figure 1.4: Monotonic Switching Procedure

1.1.1 Pros and Cons of Monotonic Switching Procedure

Pros

- The power consumption in monotonic switching procedure is less when compared to conventional switching.

- Since the common mode voltage of the comparator changes for every bit resolution, the reference voltage and dynamic range will determine the common mode voltage value at the input.

- Since the input signal is sampled directly onto the top plate capacitors, the first conversion directly happens with the input signal and only 9 bottom plate voltages need to be changed during the bits resolution.

- Inverter switches are sufficient to control the bottom plate voltage of the capacitors.

- The absolute voltage of the top plate of LSB capacitor bank (consisting of capacitors 5, 4, 3, 2) is moot at the top plate of the MSB capacitor bank (consisting of capacitors 10, 9, 8, 7, 6). Thus it can be reset to Vdd in sampling phase, which can help in reducing the input capacitance of the SAR ADC.

Cons

- The input common mode of the differential signal for the comparator changes over the 10 cycles of SAR logic. This causes the input referred offset of the comparator to change over the 10 cycles which can degrade INL and DNL of the ADC.

- The drain capacitor of the bootstrapped switch and the gate capacitance of the comparator introduce gain errors. This poses a limitation on the size of the transistors that can be used for the sampling switch and the comparator's primary differential pair.

1.2 Capacitor Bank

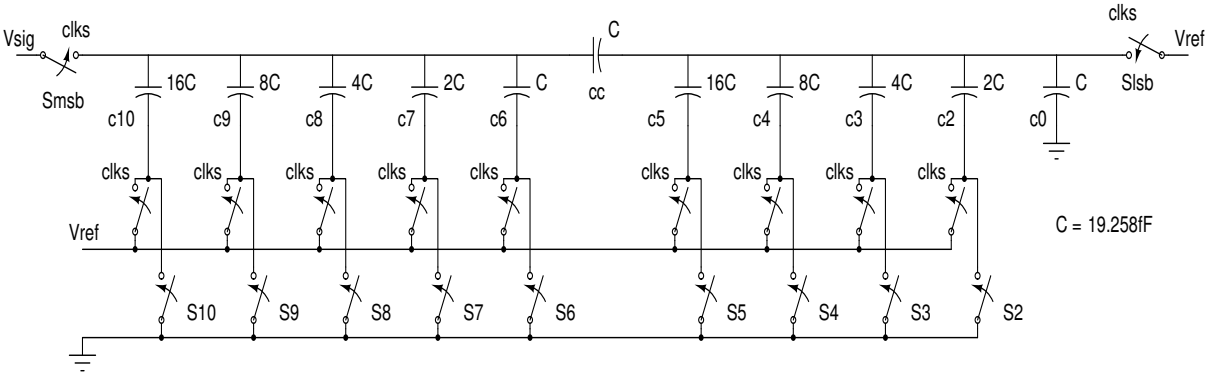

Figure 1.5: 10 bit Capacitor bank used for monotonic switching

The schematic of the capacitor bank is shown in Fig. 1.5. Conventionally to get a resolution of 10 bit, a binary weighted capacitor array going from weight 1 to 512 is used. To reduce the total capacitance, the array is divided into two banks coupled by a capacitor with weight 1. This is shown in Fig. 1.5. It can be seen that the effective weight calculated at the top plate of the MSB bank (consisting of capacitors 10, 9, 8, 7, 6) is still approximately binary.

Here routing parasitic capacitance at the top plate of LSB bank (consisting of capacitors 5, 4, 3, 2, 0) impact the accuracy of the weights of the capacitors. To reduce the effect of this parasitic capacitor, capacitor-c0 is removed and the required capacitance is obtained from the parasitic capacitance itself. It can be observed that the sensitivity of the weights (calculated at MSB bank top plate) to this parasitic capacitance is very less, but this arrangement is better than the arrangement with the capacitor-c0.

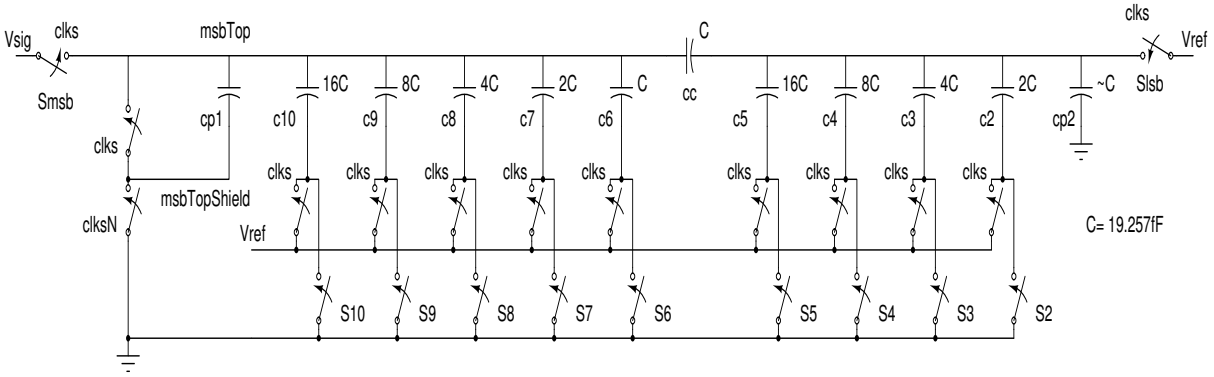

Figure 1.6: Capacitor c0 routed as parasitic capacitance in fig 1.5

In other words, the accuracy of the weights is better with only the parasitic capacitor approximately matched to the unit capacitor, as compared to the other case in which there is capacitor-0 and parasitic capacitance. This is because, even with minimum width routing, the parasitic capacitance cannot be reduced to a value much lesser than unit capacitor.

As mentioned in Section 1.1 of monotonic swithcing procedure, the parasitic capacitance at the MSB bank will lead to gain error. In bottom plate sampling, this is not a problem because the signal and the DAC voltages are both scaled by the same factor. The comparator will now have to resolve a smaller voltage difference, but it can easily be taken into account in comparator design. This can be emulated in monotonic switching procedure by the following method. The metal-routing of the MSB top plate node (call this node as msbTop) can be shielded from ground by routing another metal layer exactly below, so that the node msbTop does not have any parasitic to substrate, and all the parasitic capacitance is between msbTop and it's shielding node (call it msbTopShield). This new node msbTopShiled is charged to signal voltage in the charging phase and connected to ground when the comparisons start. This scales the input voltage exaclty by the same factor as the DAC voltages, and thereby imitating the bottom plate sampling. However this method works only for the routing parasitic capacitance and does not work for the input gate capacitance of the comparator and drain capacitance of the sampling switch.

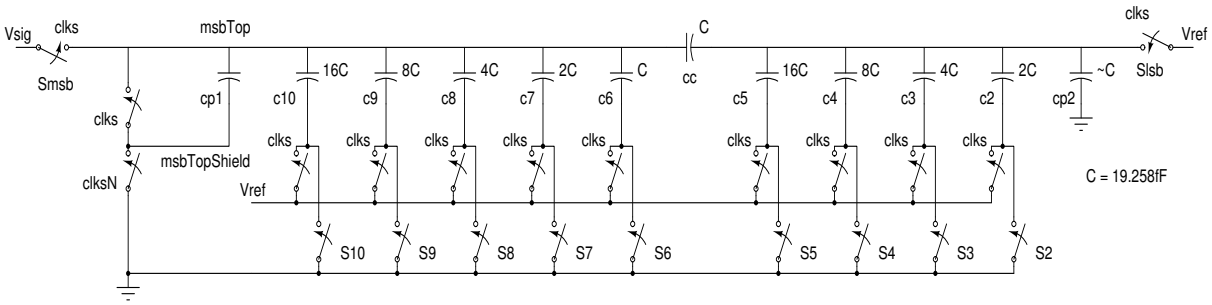

Figure 1.7: Capacitor Bank with MSB shielding node to reduce gain error

Instead of connecting the shielding node directly to signal voltage in sampling phase, it is connected to MSB top plate node. This is because the the sampling switch and the capactor bank act as a filter and hence at high frequencies the signal voltage and the sampled voltage may be slightly different. The above mentioned method is shown in Fig. 1.7.

1.3 Bootstrapped Switch

The bootstrapped switch shown in figure 1.8 is used for sampling the input signal onto the top plate of the MSB capacitor bank. During sampling phase the LSB bank is reset to Vref. The bootstrap switch shown in the fig 1.8 generates Vsig + Vdd for the sampling switch (M9) during sampling phase and $\frac{-Vdd}{2}$ during evaluation phase.

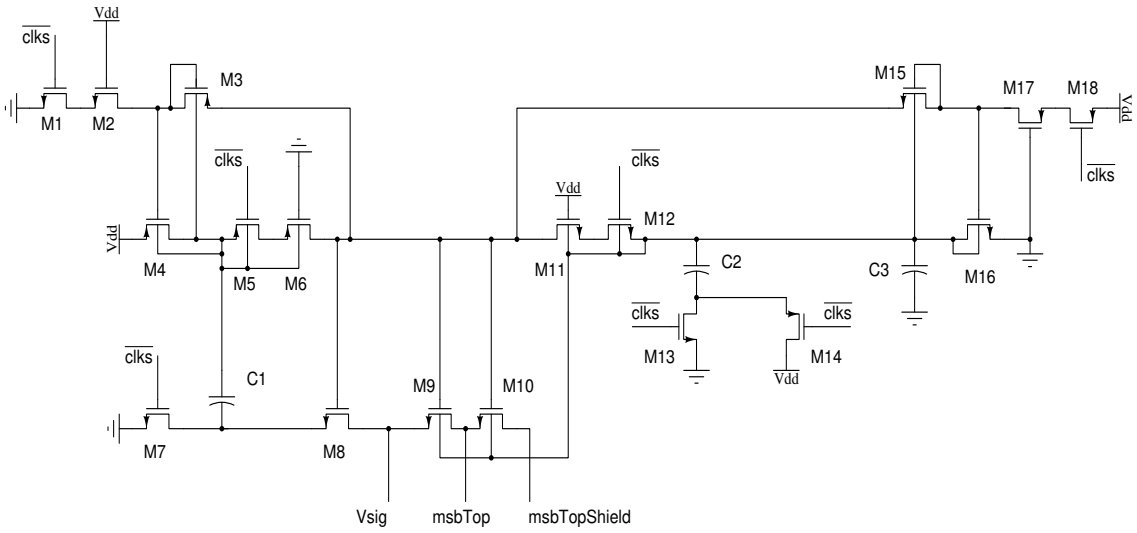

Figure 1.8: Bootstrap switch to sample signal onto capacitor bank

The bootstrapped switch is designed such that the voltage difference across any two

Component	Width(μm)	Length(μm)
M1,2,4,7,8,11,12,13,14,15,16,17,18	0.24	0.06
M3,5,6	0.48	0.06
M9	5	0.06
M10	0.6	0.06
C1	4	4
C2	2	2

Table 1.1: Sizes of Bootstrapped switch elements

terminals of the transistors do not exceed the nominal voltages by large percentages. C1 is charged to a potential difference of Vdd when clks is low. When clks goes high, the bottom plate of C1 is connected to signal, and top plate generates the required gate voltage equal to -Vdd+Vsig (it is scaled down due to parasitic capacitance). This strategy is used to keep the on resistance of M9 constant irrespective of the input signal voltage.

C2 generates a gate (and bulk) voltage of $\frac{-Vdd}{2}$ when C1 is getting charged to Vdd. This is the phase when the SAR ADC is resolving the bits. Drain-source leakage current of M9 can reduce the performance of the ADC, to prevent this the gate and bulk of M9 (and M10) are taken down to about -Vdd/2. C3 is adjusted after layout such that $\frac{-Vdd}{2}$ is generated even after including the effect of parasitic routing capacitance.

As mentioned before in Section 1.2 when clks is low (charging phase of ADC), msbTopShield is connected to msbTop node. This switch is also bootstrapped and is shown as M10 (switch to connect msbTopShiled to ground is not shown here).

1.4 Dynamic Comparator

The schematic for the dynamic comparator is shown in Fig. 1.9. The topology was chosen as it has a better noise performance over a conventional strong arm latch. As mentioned in Section 1.1, larger the size of the PMOS differential pair M4, M5, larger is the input capacitance of the comparator. Since this capacitance causes gain error, size of the PMOS differential pair cannot be increased indefinitely. Thus to meet the noise requirements, extra capacitance C1 and C2 are added at the drain of M4 and M5. Here C1 and C2 are NMOS capacitors. The capacitance C1 and C2 are connected between Vdd and drain, this is because, as the potential difference across NMOS capacitance increases from 0 to Vdd the capacitance increases. This arrangement ensures that the changes in capacitance do not oppose the regeneration process. Initially the potential difference across the capacitors is Vdd and have the maximum possible capacitance. As the comparator regenerates the differential input, the voltages at the drains of M4 and M5 start to increase, thus reducing the voltage difference across capacitors C1 and C2. As voltage difference reduces, the capacitance also reduces, and the arm which is rising faster has a lesser capacitance. This means that the changes in capacitance values do not oppose the regeneration process.

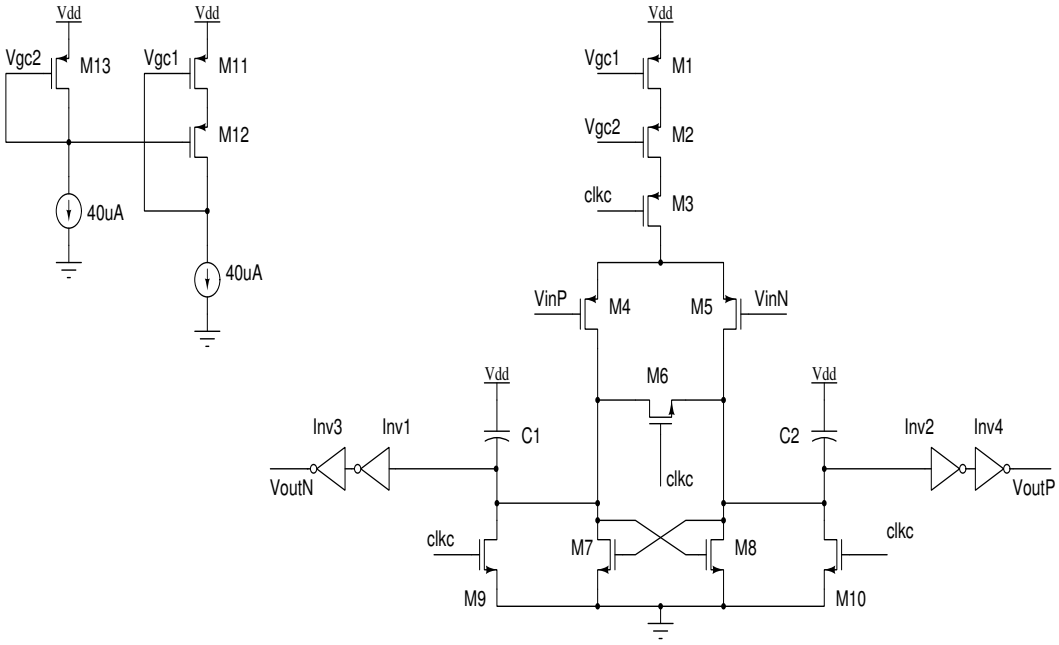

Figure 1.9: Clocked Comparator with a current source

Component	Width(μm)	length(μm)
M1, M2	6	0.06
M3	2.4	0.06
M4, M5	1.68	0.06
M6	0.12	0.06
M7, M8	1.92	0.06
M9, M10	1.2	0.06
Inv1,2	1.2	0.06
Inv3,4	2.4	0.06
C1, C2	2	1

Table 1.2: Comparator component sizes

The drains of M4 and M5 are reset to ground after each decision. Extra inverters 1 to 4 are added to ensure rail to rail outputs. Although M9 and M10 are used to reset drains of M4 and M5, at high speed the reset-voltage may not be same for both branches. M6 is used to ensure that the two arms are reset to the same exact voltage during sampling phase and at the end of every conversion cycle.

The coupling effect due to the drain capacitance of the sampling switch can result in unequal charges which introduces dynamic offset and in turn degrades the ADC performance. Inorder to avoid this two transistors M1, M2 in cascocde-like arrangement are used to source a nearly constant average current irrespective of the input common mode voltage. As mentioned in Section 1.1, the input common mode voltage of comparator falls from half Vref to near-zero voltages as the bits are resolved. The bias current needs to be kept constant to keep the input referred offset constant over different common mode voltages [1]. Offset in this comparator causes only a dc offset and does not affect the performance of the ADC, however if the offset changes over different common mode voltages(dynamic offset), then that can degrade the performance. It can be observed that when clkc is high, the current sources are not in saturation region, however they ensure that the maximum possible current flow through the pmos differential pair M4 and M5.

Enlarging the size of the comparator can also improve the dynamic offset but at the expense of power and degradation of speed. Another offset error which can degrade the ADC linearity performance is dynamic memory offset. When the compared voltage difference is not sufficiently large enough to resolve the bit the next conversion cycle will see the input comparator voltage lesser than what it should see. Glitches in clkc will introduce this error due to which linearity degrades.

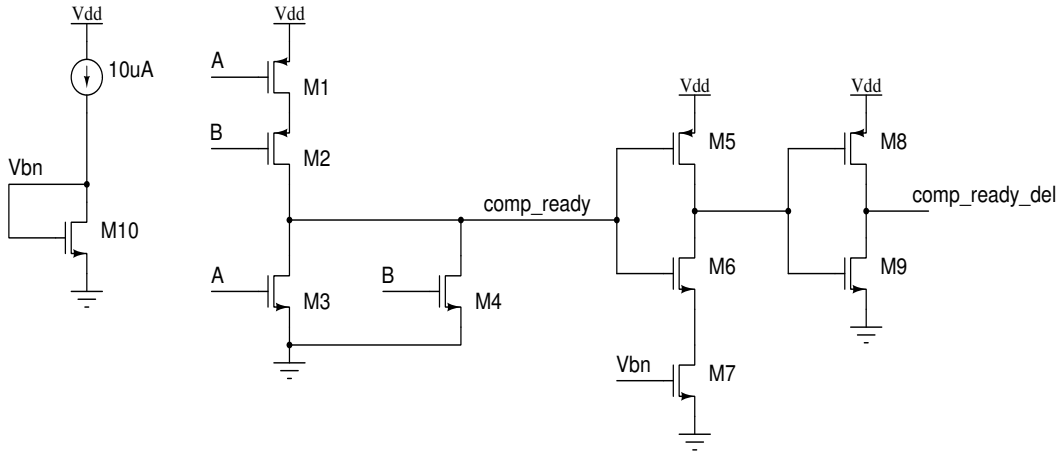

Figure 1.10: Delay Block

M1 to M4 in Fig. 1.10 form a NOR gate. The outputs of comparator are connected to terminals A and B, the output of NOR gate is named as comp-ready. When comparator is reset, both outputs of comparator are zero and when a regeneration is complete, one of them is high and the other is low. Thus falling edge of comp-ready indicates the completion of a decision, and based on this edge, the digital block samples and stores the output of comparator and changes the switch configuration accordingly. A buffer is used to delay comp-ready. The delay of the buffer is adjusted such that the comparator is activated only after the top plate voltage of capacitor bank has settled. As shown in Fig. 4 a finite amount of time is needed before the voltages settle after the changes in switch configurations have been applied. The delay from comp-ready to comp-ready-del is the least possible delay at the falling edge of comp-ready. The comparator consumes a static current when the decision is completed (as opposed to only dynamic current consumption in conventional strong arm latch). Having lesser delay between falling edge of comp-ready and rising edge of clkc helps in reducing the power consumption of the comparator.

1.5 SAR CONTROL LOGIC

To generate required clock signals for switching circuit asynchronous control circuit is used internally in the ADC. Conventional digital logic is shown in Fig. 1.11. It is evident that the delay from comp-ready to sw(n) is dominated by two flip-flop delays (comp-ready to clk(n) and clk(n) to sw(n)). Accommodating two flip-flop delays is problematic at high speeds. To solve this problem, a new arrangement is used as shown in Fig. 1.12. Instead of generating the required clock at the falling edge of comp-ready (when delay is crucial), required clock-enable's are generated at the rising edge of comp-ready. Thus when falling edge of comp-ready arrives, the delay from comp-ready to clk(n) is caused only due to a nor gate. And total delay from comp-ready to sw(n) is due to a nor gate and a flip flop.

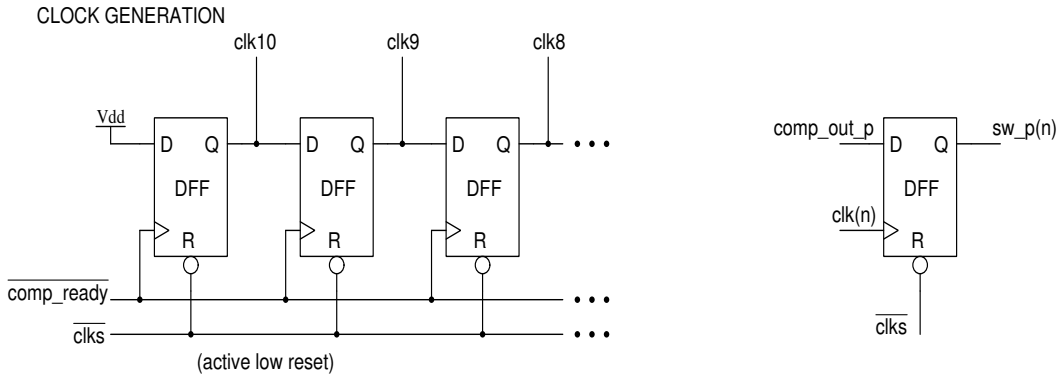

Figure 1.11: Conventional SAR logic

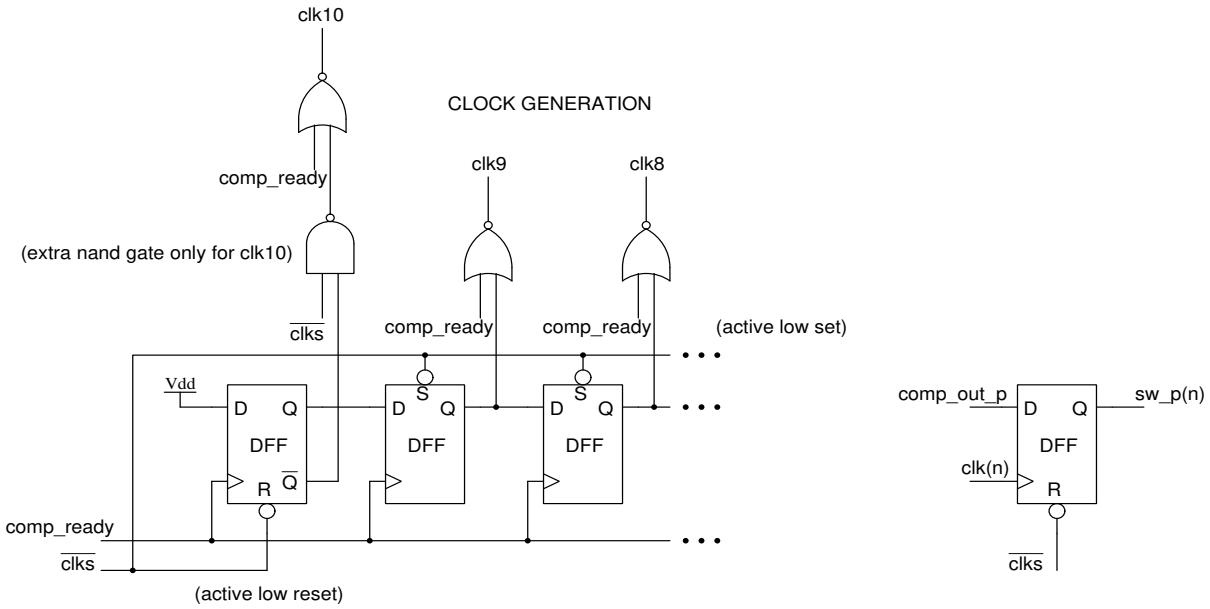

Figure 1.12: Proposed SAR logic

Since flip flop delays are significantly larger than combinational logic delays, the new arrangement shown in Fig. 1.12 has lesser delay as compared to Fig. 1.11. Extra nand gate is inserted only for comp-ready to clk10 path. This is to make sure that clk10 is activated only after clks becomes low. Since the number of gates is not very high, the leakage power consumption is not a problem. Standard cells from the foundry were used for the layout of the control logic block. The timing diagram of the generated clocks is shown in fig 1.13. Clk1 to clk10 is used to sample the digital output codes of comparator and serve as control signal for the switches across the capacitor bank for monotonic switching procedure.

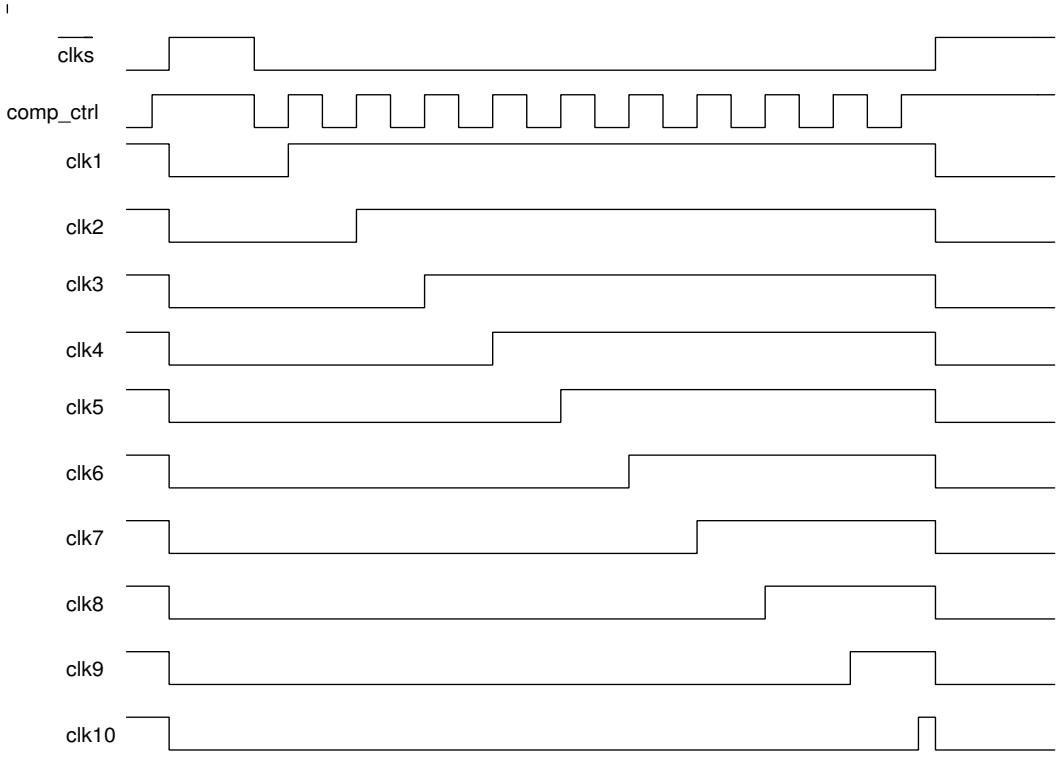

Figure 1.13: Timing diagram of control Logic

CHAPTER 2

LAYOUT AND SIMULATION RESULTS

The SAR ADC is laid out in TSMC 65nm technology using cadence virtuoso tool. Area occupied by the core of SAR ADC is 276μm * 135μm. The layout of different blocks is shown below.

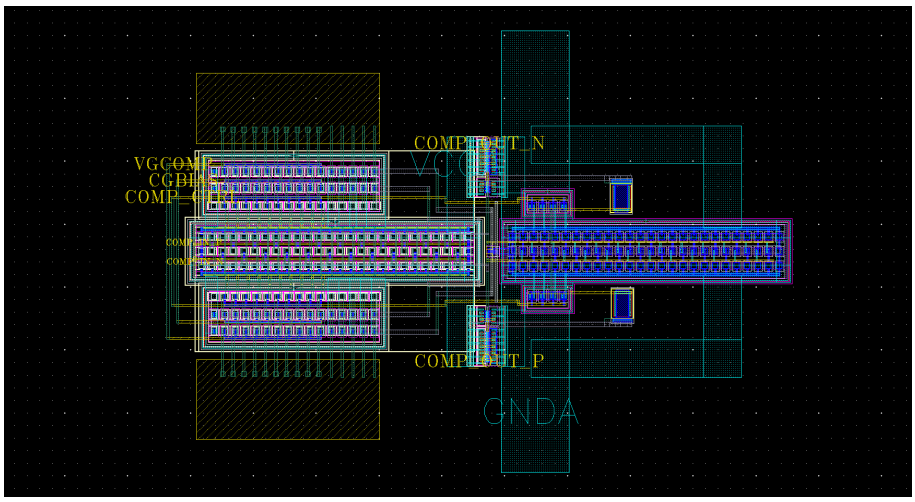

Figure 2.1: Layout of comparator

The input pair and regenerative transistors are layed-out by interdigitising technique to reduce mismatch.

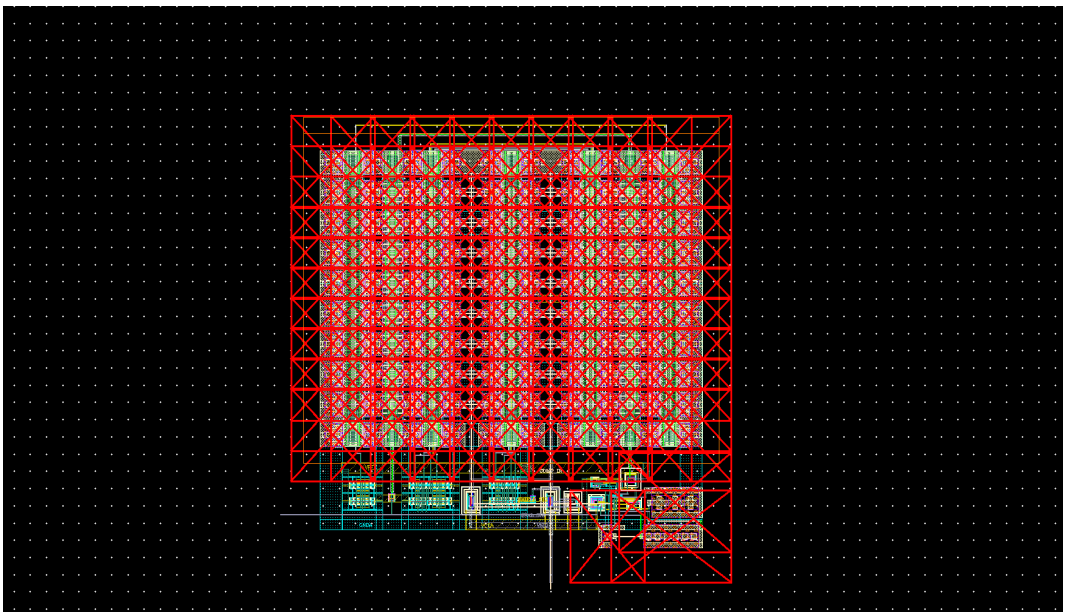

Figure 2.2: layout of capacitor bank with the bootstrapped switch

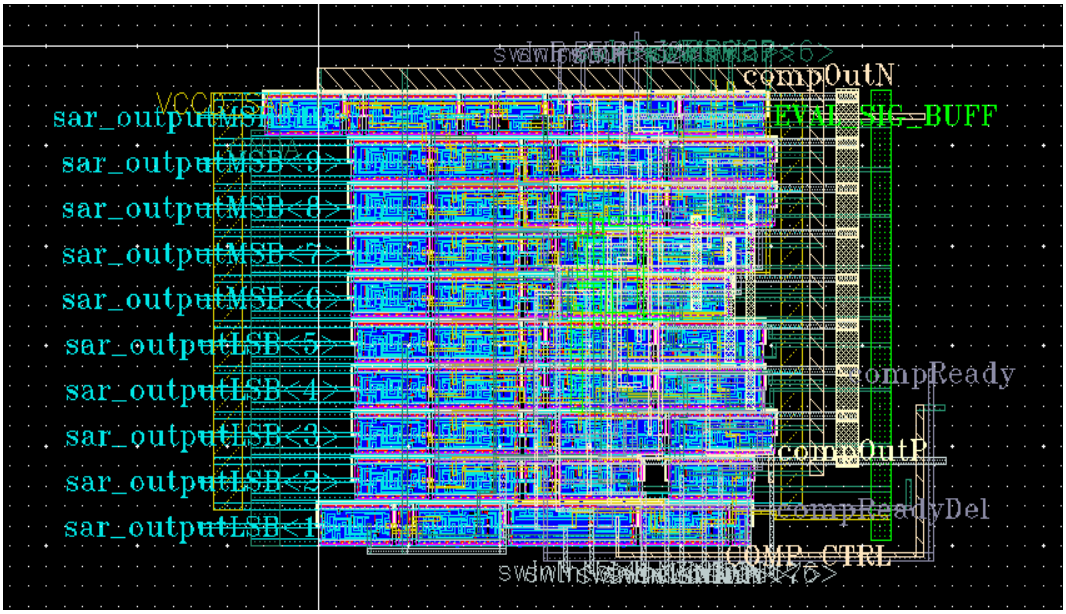

Figure 2.3: Layout of SAR control logic

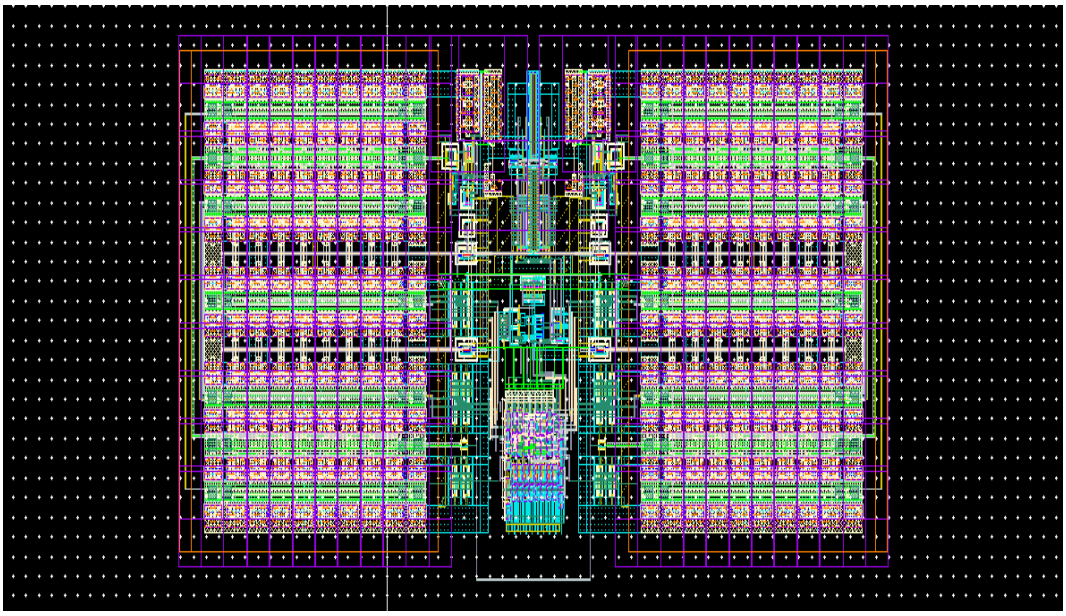

Figure 2.4: Layout of SAR ADC core

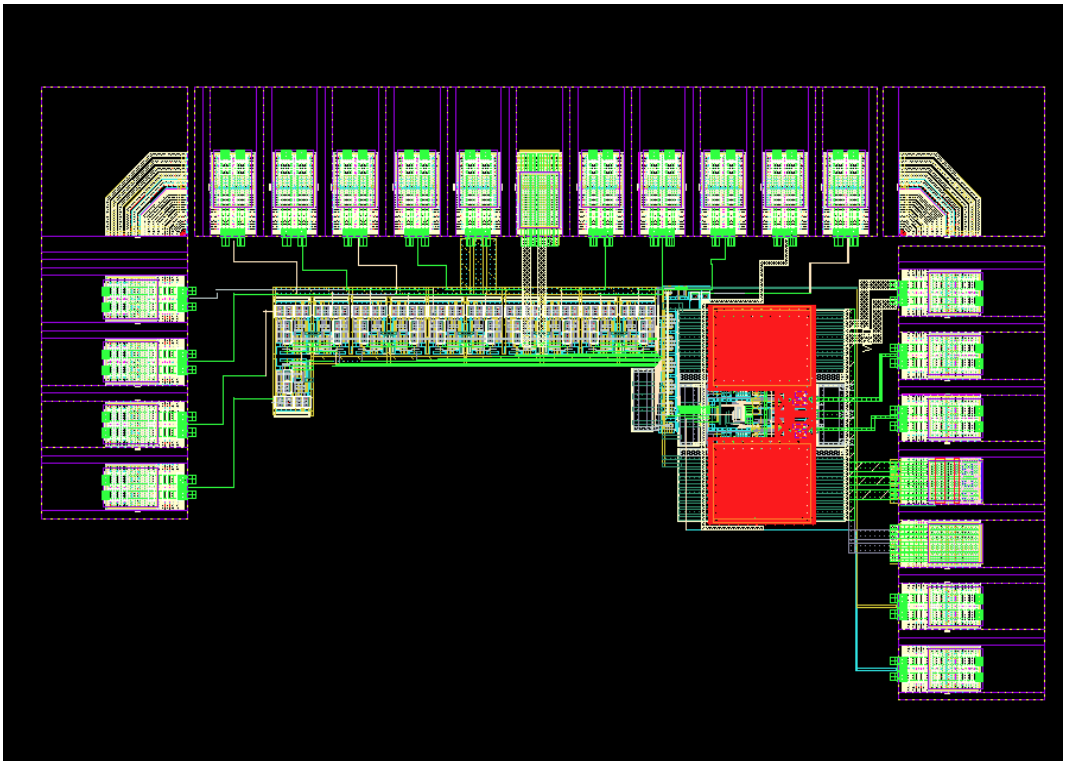

Figure 2.5: Full chip layout with I/O pads

2.1 Simulation Results

Nominal Supply voltage = 1.2V

Input applied for full scale output = 580mV amplitude(1160mV_{pk-pk} differential amplitude)

2.1.1 Inverter Switches

Unit inverter details:

PMOS: 480n/60n

NMOS: 720n/60n (lvt)

These inverter units are scaled appropriately to obtain all of the switches. Worst case settling time is observed at SS corner (equivalent to 10*RC time) and is found to be: 54.5 ps

2.1.2 Capacitor Bank

The unit capacitance = 19.258$\pm$16.5 $\%$fF MIM capacitor. $\sqrt{KT/C}$ noise was found to be 89.18μV at 300K temperature.

2.1.3 Comparator

Noise of the comparator has been simulated by pss/pnoise method. It gives better noise estimation than extensive transient noise simulation[3]. From the noise summary of cadence tool it was observed that flicker noise of the input differential pair and the regenerative pair are major noise contributors . A monte carlo simulation was run for 500 samples to find the offset of the dynamic comparator and is shown in table 2.1.

Parameter	Value
Input Referred Noise (rms)	700uV
Input Referred Offset due to mismatch	9.71mV

Table 2.1: Comparator noise and mismatch performance

2.1.4 SAR ADC Dynamic Performance

Fully assembled SAR ADC was simulated with R+C+CC parasitics extracted netlist for a single ended sinusoidal input of 580mV amplitude with common mode voltage of 600mV. The ADC has been simulated across various corners given in table 2.1 and 2.2. The power consumed by the core blocks is shown in table 2.3. A 256 point FFT digital output spectrum simulated across TT corner is shown in figure 2.6

Parameters	SF	SS	FF	FS	TT
ENOB (bits)	9.49	9.58	9.35	9.512	9.51
SINAD (dB)	58.91	59.45	58.04	59.03	59.02
SFDR (dBc)	66.81	67.96	66.1	65.13	66.59

Table 2.2: ADC dynamic performance at $\frac{13}{128}*$100MHz input frequency

Parameters	SF	SS	FF	FS	TT
ENOB (bits)	9.31	9.38	9.27	9.4	9.26
SINAD (dB)	57.85	58.22	57.6	58.38	57.52
SFDR (dBc)	63.67	63.23	62.5	64.75	63.83

Table 2.3: ADC dynamic performance at $\frac{61}{128}*$100MHz input frequency

Block	Power Consumption (μW)
Comparator	210
Capacitor Bank	30
Delay block + Core Buffers	200
SAR Control Logic	245
Total	685

Table 2.4: Power consumed from various blocks

The figure of merit is calculated with the formula: FOM = $\frac{Power}{2^{ENOB}*min[fs,2*ERBW]}$

FOM = $\frac{685*10^{-6}}{2^{9.26}*100*10^{6}}$ = 11.72fJ/conversion.

A transient noise analyses was run for 4 cycles of 256 points and the mean of the parameters were considered as the dynamic performance with random noise generated from the ADC. The dynamic performance parameters measured are as follows:

ENOB = 9.336 (bits)

SINAD = 57.96 dB

SFDR = 67.24 dBc

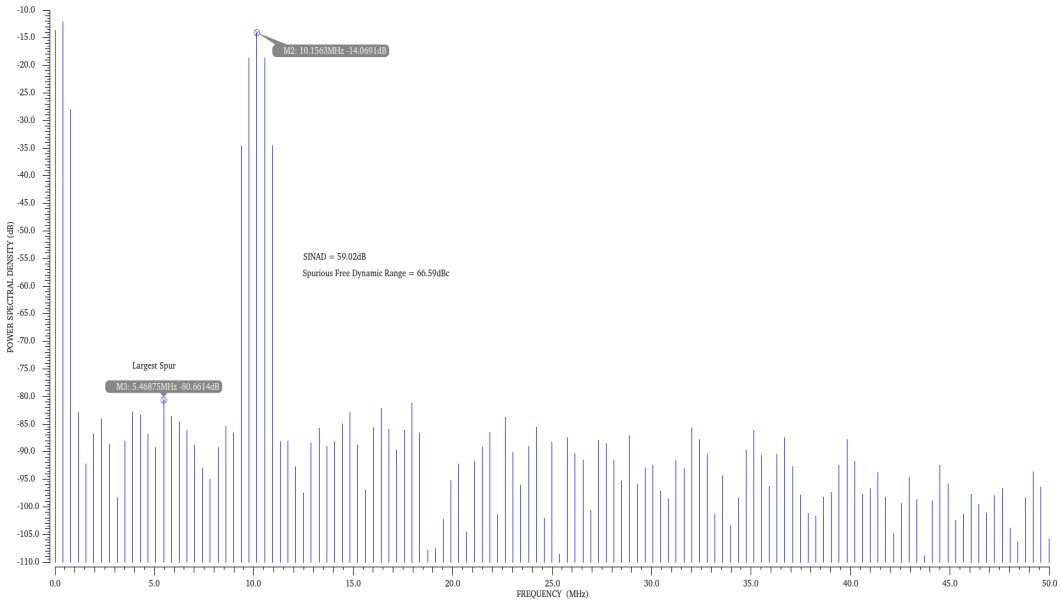

Figure 2.6: 256 point-FFT Digital output spectrum across TT corner

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