

Hardware Implementation of Layermapping and Precoder for 5G NR Transmitter Chain

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Hardware Implementation of Layermapping and Precoder for 5G NR Transmitter Chain**, submitted by **HARISH MANCHE**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Vivado HLS, Xilinx SDK, Layermapping, Precoder.

The current trend in digital design is to accelerate the design and developmental cycles without compromising on verification. One of the key factor underlying the concept is to raise the abstraction level from the traditional RTL level which are time consuming, and difficult to debug. HLS tools are an attractive proposition for the rapid prototyping of the systems and bridges the gap between development times and time to market. HLS tools automatically transforms the algorithms written in C, C++ to RTL implementations.

In this thesis I am presenting the implementation of Layermapping and Precoder blocks of 5G transmit chain using Vivado HLS tool and Xilinx Design Suites including Vivado IP Integrator and Xilinx SDK. In order to improve the performance of the hardware, various optimizations like data flow, pipelining, array partitioning are used. The challenge was to achieve the required performance through minimized iteration interval with minimum resource usage. The hardware generated is successfully integrated with other blocks in the transmit chain and tested using Zynq Ultrascale evaluation board.

NOTE : Due to confidentiality of 5G Testbed Project, Unable to submit complete details about the project. For further information, contact **Dr. Radha Krishna Ganti**

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