SOLAR PV FED SINGLE STAGE DC-AC CONVERTER WITH HIGH FREQUENCY AC-LINK

A Project Report

submitted by

RICHU RACHEL

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THESIS CERTIFICATE

This is to certify that the thesis titled **Solar PV fed Single Stage DC-AC Converter with High Frequency AC-Link**, submitted by **Richu Rachel**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the project work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Lakshminarasamma N
Project Guide
Associate Professor
Dept. of Electrical Engineering
IIT-Madras, 600036

Place: Chennai

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ABSTRACT

KEYWORDS: Solar PV fed single stage DC-AC converter, cycloconverter, MPPT

The penetration of renewable sources-generated electrical energy into the grid is increasing exponentially due to the high energy demand. Solar PV being one of the promising renewable sources of energy is widely used in home applications, water pumping, street lightning, supplying telecommunication transmitters, etc. Since the direct connection of PV system to the grid is not possible, efficient power conversion systems are required to transfer the power from solar PV system (DC) to the grid (AC). The solution of the DC-AC grid-connected converter is expected to have HF transformer isolation, high efficiency, reduced EMI, low output THD and unity output power factor.

For DC-AC conversion, conventional practise is to use a PWM bridge converter with HF AC-link followed by diode bridge rectifier, which gives a regulated high voltage DC, followed by a voltage source inverter which converts the regulated DC to the required AC output. But PWM bridge converters have limitations in switching at high frequency due to the hard switching nature, thereby increasing the output filter size. Therefore phase shifted converters are preferred which retains the features of PWM converters and in addition provides soft switching. Therefore, single stage DC-AC converter with sinusoidal phase shift full bridge converter as the front end followed by cycloconverter is preferred. This converter could be used as replacement for the conventional two stage inverter.

The operation and analysis of the DC-AC converter with cycloconverter switching at line frequency and combined line/high frequency are presented in this thesis. The control configuration implementation for single stage DC-AC converter with a sinusoidal phase shifted front end followed by a cycloconverter is presented which ensures soft transitions for all the semiconductor devices. The comparison of line frequency switching and combined line/high frequency switching of cycloconverter devices of single stage DC-AC converter in terms of performance and efficiency is presented. Analytical

expressions for the computation of losses in the full bridge converter and cycloconverter switched at line frequency and combined line/high frequency are proposed. The control, analysis, and mathematical expressions are verified in simulations and 500 W single stage DC-AC converter experimental prototype. Modelling and controlling of the PV fed DC-AC converter is done in synchronous reference frame so that well-proven PI controllers could be just like DC systems. Conventional Perturb & Observe MPPT algorithm is used for tracking the maximum power point. Test waveforms of different irradiances are given as input to test the performance of the system, results obtained are presented.

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ABBREVIATIONS

FB	Full Bridge
HF	High Frequency
EMI	Electromagnetic Interference
PWM	Pulse width Modulation
VSI	Voltage Source Inverter
LF	Line Frequency
PSFB	Phase Shifted Full Bridge
THD	Total Harmonic Distortion
ZVS	Zero Voltage Switching
SCR	Silicon Controlled Rectifier
ESR	equivalent Series resistance
DSP	Digital Signal Processor
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PV	Photovoltaic
MPPT	Maximum Power Point Tracking

NOTATION

$i_p(t)$	Primary transformer current
$i_L(t)$	output inductor current,
$i_{mag}(t)$	Transformer magnetising current
n	Turns ratio
L_{lk}	Leakage inductance of the transformer
C_T	Winding capacitance of the transformer
C_{MOS}	Output capacitance of MOSFET
V_{dc}	Input DC voltage
T_{DT}	Dead time
V_0	Output voltage
L_f	Output filter Inductance
D	Total phase shift given between S_1 and S_3
D_{eff}	Effective duty
ΔD	Duty loss
f_s	Switching frequency
R_0	Load resitance
$v_L(t)$	Voltage across the filter inductor
T_s	Switching period
I_{RMS1}	RMS current through switches $S1$
I_{RMS4}	RMS current through switches S_4
I_{avg1}	Average current through the body diodes of $S1$
I_{avg4}	Average current through the body diodes of S_4
V_f	Forward voltage drop of the body diode of the MOSFET
R_{dsON}	On state resistance of MOSFET
P_c	Total conduction loss in FB converter
P_D	Total conduction loss due to V_f of body diode in FB converter
P_{RdsON}	Total conduction loss due to R_{dsON} in FB converter
$P_{S1,S2}$	Conduction losses due to R_{dsON} in switch S_1 or S_2
$P_{S3,S4}$	Conduction losses due to R_{dsON} in switch S_3 or S_4
$P_{D1,D2}$	Conduction losses due to forward voltage drop of body diode in switches S_1 or S_2
$P_{D3,D4}$	Conduction losses due to forward voltage drop of body diode in switches S_3 or S_4
I_m	Peak output current of single stage DC-AC converter
ω	Line frequency in radians
N	Transformation ratio
$P_{cond_{lf}}$	Conduction loss in cycloconverter when it is switched at line frequency
I_{lrms}	RMS current through switch S_{1B} when cycloconverter is switched at line frequency
I_{lavg}	Average current through body diode of switch S_{1B} when cycloconverter is switched at line frequency
$P_{cond_{l/hf}}$	Conduction loss in cycloconverter when it is switched at combined line/high frequency
I_{rms}	RMS current through switch S_{1B} when cycloconverter is switched at

	combined line/high frequency
I_{havg}	Average current through body diode of switch S_{1B} when cycloconverter is switched at combined line/high frequency
V_α	α-axis component of voltage vector
V_β	β-axis component of voltage vector
V_d	d-axis component of voltage vector
V_q	q-axis component of voltage vector
i_d^*	Reference for d-axis grid current
i_d^*	Reference for q-axis grid current
P_{pv}	PV power
I_0	Reverse saturation current of the diode
q	charge of the electron
k	Boltzmann's constant
T	Absolute temperature
V_{oc}	Open circuit voltage of PV module
I_{sc}	Short circuit current

CHAPTER 1

INTRODUCTION

Global demand for energy is rising. With the bulk of the demand coming from developing countries, energy consumption is expected to increase multifold in the near future. Oil, coal and gas being the major sources of energy increases threat to the environment due to the high level of pollution it causes. Therefore, there is a high increase in demand to switch to alternate options like the renewable sources.

1.1 Motivation

Renewable energy resources such as wind, tidal, solar have gained a lot of popularity as they contribute to clean power, minimizing fossil fuel consumption, and lowering the emission of greenhouse gases. The current power system is undergoing a considerable amount of changes, because more renewable energy based power conversion systems are connected to the low voltage distribution systems as distributed generators due to their environment friendliness and reliability. Therefore, there is an increased requirement for highly efficient power converters.

1.2 Objective

The main objective of this thesis is to study and design a solar PV fed single stage DC-AC power converter with higher efficiency which can be integrated with the grid.

1.3 Literature Review

Solar PV fed DC-AC converter connected to grid consists of PV modules, a high gain DC-AC converter and the grid. Brief description of PV and converter topologies are discussed in the this section.

1.3.1 Solar PV

Solar cells are essentially semiconductor junctions which convert energy from sunlight to electrical energy. Due to the low-voltage of an individual solar cell (typically 0.5V) [1] several cells are wired in series, thus composing a photovoltaic module or solar panel. Modules can be strung together into a photovoltaic array. In order to convert the solar energy to electrical power in optimum way, the system often consists of multiple components, including the PV modules, mechanical connections, and electrical power conditioning units, the combination of all these parts is a so-called photovoltaic system (PV system). The single diode model of the solar cell [2], [3] is shown in Fig. 1.1. A mathematical expression for the solar cell equivalent circuit can be obtained from Kirchhoff's current law given by (1.1):

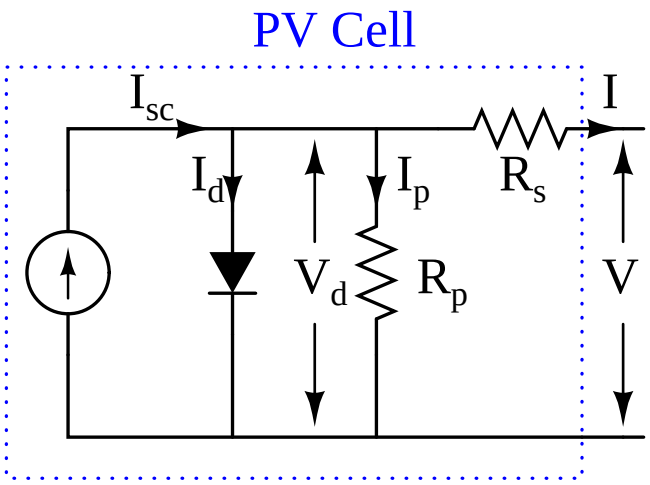


Figure 1.1: Solar cell equivalent circuit

$$I_{sc} = I_d + I_p + I \tag{1.1}$$

where I, I_d and I_p are the cell output current, diode current and the shunt resistance current, respectively. The current through each equivalent circuit element is governed by the voltage across them, so the diode current is given by (1.2).

$$I_d = I_0(e^{\frac{qV_d}{kT}} - 1) \tag{1.2}$$

$$V_d = V + IR_s \tag{1.3}$$

where,

I_0 is the reverse saturation current of the diode,

q is the charge of the electron,

k is Boltzmann's constant,

T is absolute temperature.

At 25^0 C, the factor $\frac{kT}{q} \approx 26\ mV$. By substituting equation (1.2),(1.3) in (1.1),we obtain,

$$I = I_{sc} - I_0(e^{\frac{qV_d}{kT}} - 1) - \frac{V_d}{R_p} \tag{1.4}$$

The solar cell is characterized by its maximum open circuit voltage (V_{oc}) at zero output current and its short circuit current (I_{sc}) at zero output voltage. The cell delivers maximum power P_{max} when operating at a point on the characteristic where the $I.V$ product has a maximum value. The solar cell characteristics change with solar irradiance and cell temperature as shown in Fig. 1.2.

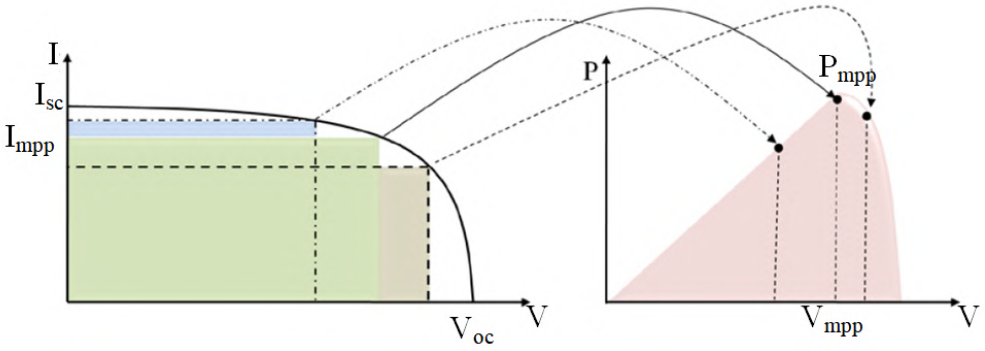


Figure 1.2: Relationships between ($I\ vs.\ V$) curve and ($P\ vs.\ V$) curve

1.3.2 DC-AC Converters

The DC-AC converter is expected to have soft switching, high efficiency, reduced EMI, low output THD and unity output power factor. Figure 1.3 shows some of the high gain, isolated DC-AC converters [4].

DC-AC conversion as shown in Fig. 1.3 can be done using Flyback/forward, push-pull, full/half bridge converters [5]. The flyback/forward converters are limited in small power applications due to drawbacks like single-ended, unipolar flux excitation and high voltage/current switch rating. The switches in a push-pull inverter have a high voltage rating. Also, it needs a center-tapped transformer. The half-bridge and full-

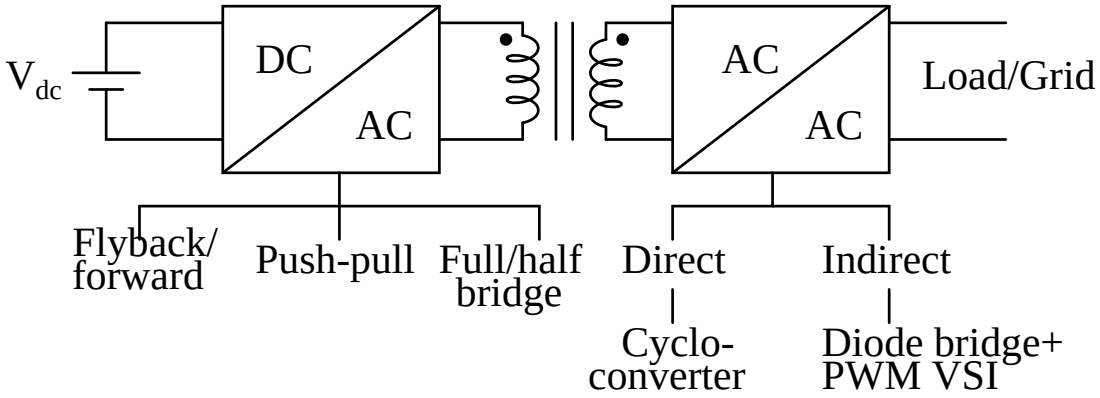


Figure 1.3: High gain, isolated DC-AC Converters

bridge (FB) high frequency (HF) inverters are widely used topologies for DC-AC inversion [5, 6]. Some of the control schemes that can be used in the FB converter are unipolar PWM, bipolar PWM, sinusoidal phase shift PWM, etc. Unipolar and bipolar PWMs have the disadvantage of conversion of DC to low frequency AC, which demands a low frequency transformer for step up purpose. Therefore the size of the transformer will be large. Therefore, FB converter is usually controlled to convert DC to HFAC preferably with soft switching characteristics. Generally, HFAC to LFAC conversion is done using a diode bridge rectifier along with a PWM VSI as in Fig. 1.4 . This involves 2 stages in itself, increasing number of power conversion stages thereby reducing overall efficiency. In addition, it is observed that a large DC link is required in this case, increasing the total size of the converter. Another option is to go for a cy-

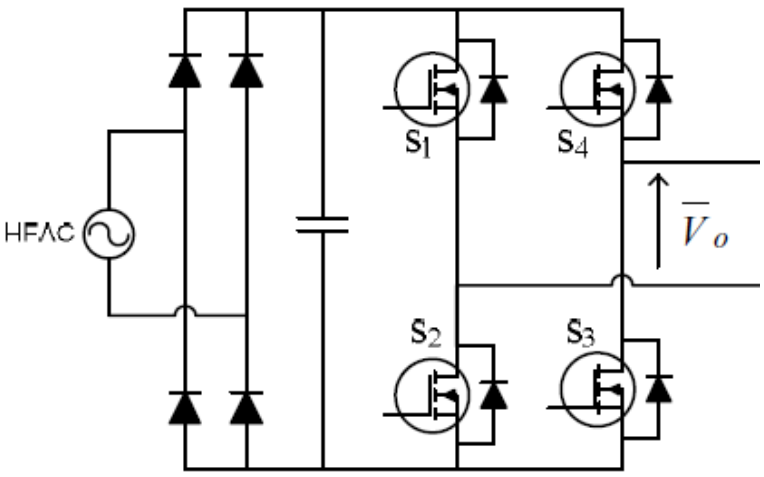


Figure 1.4: Conventional HFAC-LFAC stage

cloconverter that directly converts the HFAC to LFAC. A single phase matrix converter

can be configured as a cycloconverter to allow bi-directional power flow as shown in Fig. 1.5 [4, 7]. Four switches in the matrix converter allow bi-directional current flow and have bipolar voltage blocking capability. Since a single switch with these characteristics are not available in the market, each switch in the matrix converter is realized as a combination of two MOSFETs in anti-series, or two SCRs in anti-parallel, or with a combination of four diodes and a MOSFET as in Fig. 1.5 [4, 8]. In this project two MOSFETs in anti-series is used. Due to the aforementioned advantages single stage DC-AC converter with a FB converter coupled with a 2×2 matrix converter based cycloconverter through a HF transformer link is selected for this project.

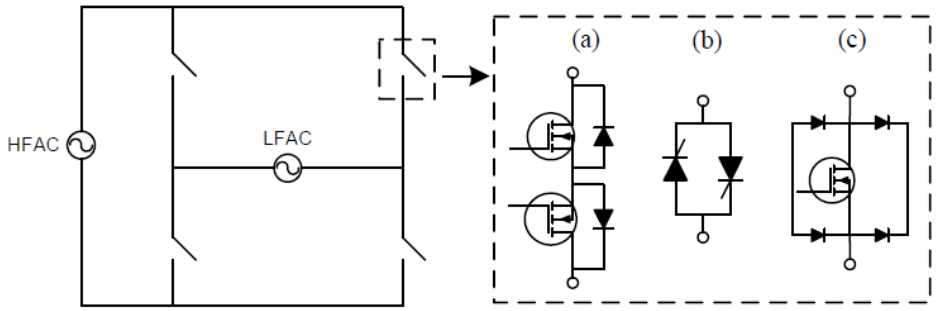


Figure 1.5: Cycloconverter

1.3.3 Grid Connection

The output of the single stage DC-AC converter contains harmonics. In order to obtain a perfect sine wave of current and voltage, a filter between the converter and grid is used. Commonly used filters in grid-connected systems are [6] L and LCL. L filter is a first-order filter with attenuation 20dB/decade over the whole frequency range. Whereas LCL provides better attenuation of 60dB/decade. It provides better decoupling between the filter and the grid impedance and lower switching frequency for the converter can be used. Since the converter is switched at very high frequency, it is possible to use a simple L filter to eliminate the switching harmonics.

1.4 Organization of Thesis

Chapter 2 presents the phase shift full bridge (PSFB) converter used for DC-DC converters. Different operating modes of the converter are explained.

Chapter 3 presents the simulation and hardware results of the 500 W, 48 V/400 V PSFB converter.

Chapter 4 discusses different control schemes for a single stage DC-AC converter. Operation of the converter with sinusoidal phase modulated full bridge converter and the cycloconverter switched at line/high frequency is described in detail. Loss budgeting is also done.

Chapter 5 presents the hardware implementation of the 500 W 48 V/230 V single stage DC-AC converter. Simulation and experimental results are also presented.

Chapter 6 deals with the modelling of the grid connected converter along with the controller design procedure. It also gives a brief overview on transformations to the synchronous rotating frame. Simulation results of the solar PV fed single stage DC-AC converter is also presented.

Chapter 7 summarizes the work carried out in this project and it also gives an outlook of further research that can be carried out based on this thesis.

CHAPTER 2

Phase Shift Full Bridge Converter

The achievement of efficient high frequency power conversion requires reduction of switching losses [9]. Therefore converters with soft switching is preferred rather than going for snubber circuits which requires additional circuitry. Conventional resonant converters achieve soft switching by suitably adding resonating LC tank circuits to the original PWM topologies. Due to the high current and voltage stresses resulting in high conduction losses in resonant converters, resonant transitions converters are preferred. The resonant transition converters combine the characteristics of both the resonant converters and the PWM converters.

PSFB converters belongs to the class of resonant transition converters that are commonly used in high gain, high power applications. All the switches in the converter operate under zero voltage switching (ZVS) without using any additional active devices. The leakage inductance of the transformer and output capacitance of the MOSFETs provides ZVS. Inorder to achieve ZVS for all the switching devices, the two legs of the bridge are operated with a phase shift. This allows a resonant discharge of output capacitances of MOSFETs and forces the conduction of each MOSFET's antiparallel diode prior to the conduction of the MOSFET [9]. The peak current in this converter is lesser when compared to the load resonant converter, so it is preferred for low input voltage, high power applications [10].

In this chapter the converter operation for the one half of switching cycle is described. Principal operating waveforms of the converter are shown in Fig. 2.2. Devices conducting in each interval are shown in Table 2.1 for the given switching scheme for one half of the switching cycle.

2.1 Converter Operating Modes

A PSFB converter is shown in Fig.2.3. The gating signals to the switches are shown in Fig. 2.2. Gating signals to S_1, S_2 and S_3, S_4 are complementary pairs. Phase shift is given between S_1 and S_3 to achieve ZVS for all switches. The different operating modes of the converter are explained in detail in the following section. The dead time between the gating signals and duty loss intervals are exaggerated for easy understanding.

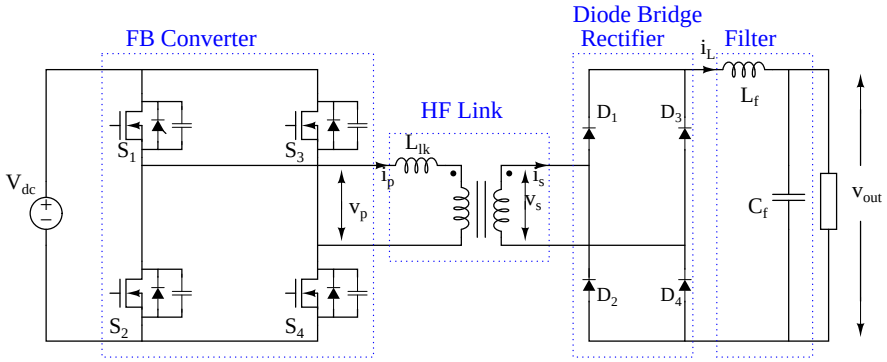


Figure 2.1: Phase shift FB converter

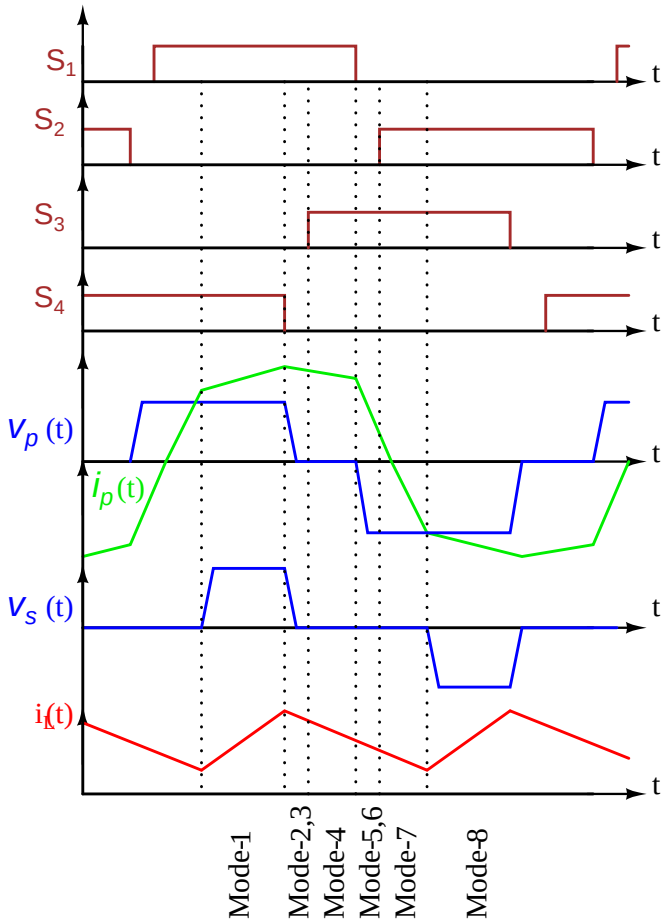


Figure 2.2: Principal operating waveforms of PSFB converter

Mode-1

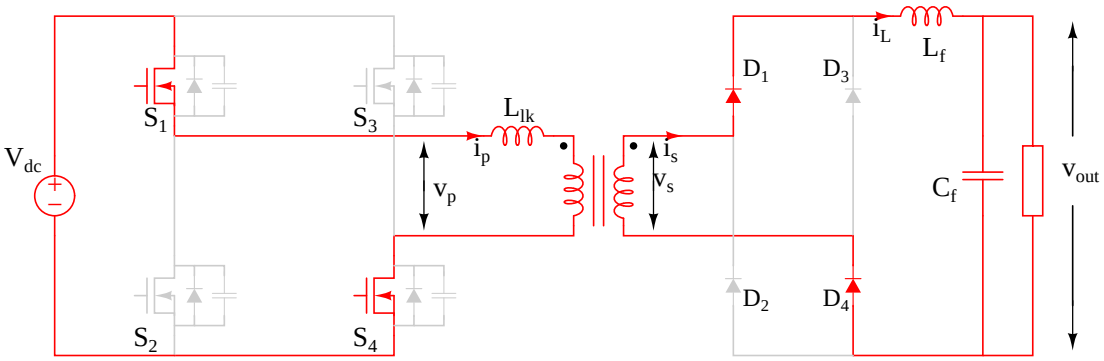


Figure 2.3: Mode-1

In this mode [Fig. 2.3], S_1, S_4 are ON and S_2, S_3 are OFF. Therefore the voltage across the transformer primary as well as the secondary is positive. Thus diodes D_1 and D_4 are in forward biased condition. Current through the primary of the transformer is the sum of the reflected output inductor current and the magnetizing current. Magnetizing current is relevant in PSFB since it helps achieve ZVS during light load conditions. It is of more importance in converters where the PSFB is used for stepping down DC voltage rather than in step up applications.

Expression for $i_p(t)$ is

$$i_p(t) = \frac{i_L(t)}{n} + i_{mag}(t) \tag{2.1}$$

where,

$i_p(t)$ is the primary transformer current,

$i_L(t)$ is the output inductor current,

$i_{mag}(t)$ is the transformer magnetizing current

n is the turns ratio.

Mode-2

This mode [Fig. 2.4] starts when S_4 is turned OFF. Therefore output capacitance of S_4 starts charging and output capacitance of S_3 starts discharging. The dead time between gating pulses of S_3 and S_4 are such that energy in the leakage inductance of transformer is used to charge and discharge the output capacitance within this time. Energy availability is more at this instant since the output inductor current is at its maximum. Therefore faster transition will happen in right leg switches as compared to left

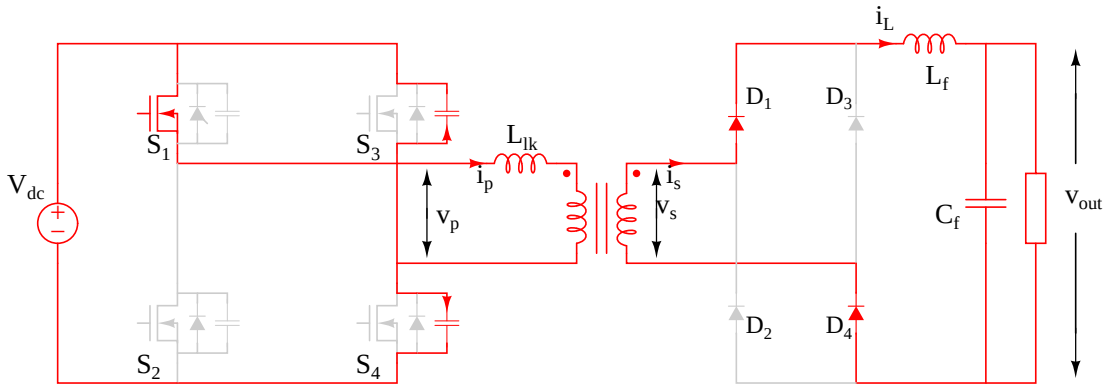


Figure 2.4: Mode-2

leg switches due to the increased energy available. The leakage inductance of the transformer should be designed such that ZVS can be attained for the required load range. For achieving ZVS, energy available in the leakage inductance should be more than the energy required to charge and discharge the output capacitance of the switch as well as the winding capacitance of the transformer as given in (2.2)

$$\frac{1}{2}L_{lk}i_p^2 > \frac{1}{2}C_T V_{dc}^2 + \frac{4}{3}C_{MOS}V_{dc}^2 \tag{2.2}$$

where,

L_{lk} is the leakage inductance of the transformer,

C_T is the winding capacitance of the transformer,

C_{MOS} is the output capacitance of MOSFET,

V_{dc} is the DC voltage.

Mode-3

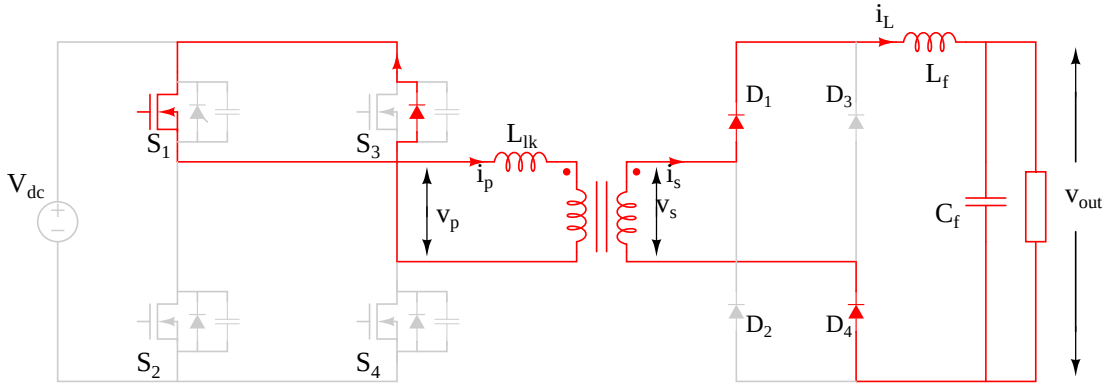


Figure 2.5: Mode-3

This mode [Fig. 2.5] starts when the output capacitance is fully discharged and the body diode of the switch conducts. Now the switch can be turned ON under ZVS condition. Dead time is set such that it ensures the output capacitance of S_3 is fully discharged and body diode of S_3 starts conducting. Expression for dead time is given in (2.3)

$$T_{DT} = \frac{\pi}{2}\sqrt{L_{lk}C} \tag{2.3}$$

where $C = C_{MOS} + C_T$.

Conduction of the body diode of S_3 starts the freewheeling interval.

Mode-4

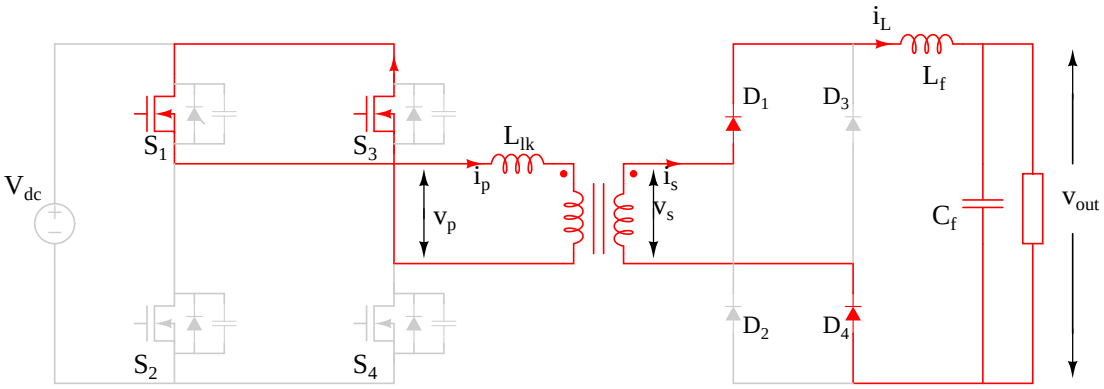


Figure 2.6: Mode-4

In this mode [Fig. 2.6] S1 and S3 are conducting. The converter is still in freewheeling mode. The transformer primary voltage is zero and the transformer primary current is still positive. Inductor current decreases with a slope of $\frac{V_{out}}{L_f}$. Although voltage across the transformer secondary is zero, only D_1 and D_4 conducts.

Mode-5

This mode starts [Fig. 2.7] when there is a high to low transition for switch S_1. Energy in the leakage inductance is used to charge output capacitance of S_1 and discharge output capacitance of S_2. Therefore the transformer primary voltage starts increasing in the negative direction to the DC voltage. This mode initiates the transition interval, transition from freewheeling to energy transfer interval. Current in the transformer secondary starts falling. Current starts flowing through D_2, D_3, while it decreases through

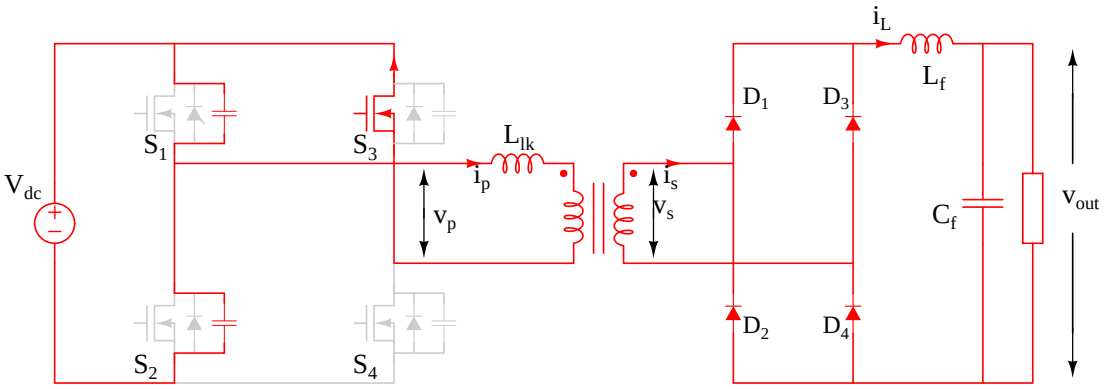


Figure 2.7: Mode-5

D_1, D_4. Thus, all the diodes start conducting in this interval. Therefore the transformer secondary voltage is zero.

As already seen the output inductor current is less due to which energy available is less, therefore the transition is slower in left leg compared to right leg. Therefore, higher dead time can be given in order to ensure that the output capacitances of S_1 and S_2 are charged and discharged fully within the given time interval.

Mode-6

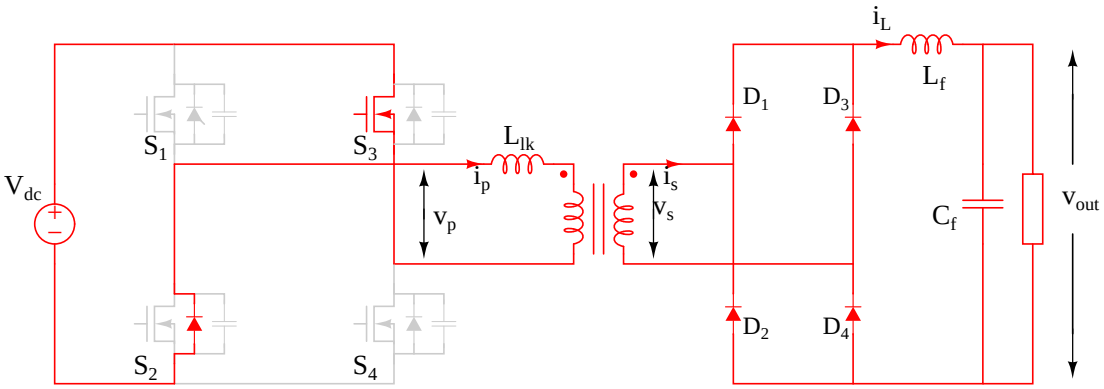


Figure 2.8: Mode-6

In this mode [Fig. 2.8] the body diode of S_2 starts conducting when the output capacitance of the switch is fully discharged. Now the switch can be turned ON under ZVS conditions. The transformer current keeps decreasing. Transformer secondary voltage remains zero.

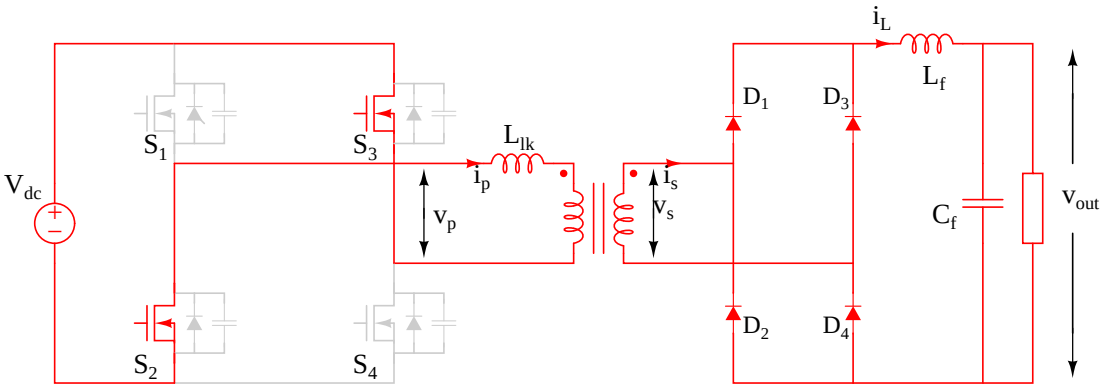


Figure 2.9: Mode-7

Mode-7

This mode [Fig. 2.9] starts with the conduction of switch S_2. The transformer current keeps decreasing and changes its direction within this interval. Transition interval continues till all the diodes are conducting. End of the transition interval marks the end of mode-7. Mode 5,6,7 shows the duty loss due to the leakage inductance of the transformer. Therefore, the effective duty D_{eff} can be expressed as

$$D = D_{eff} + \Delta D \tag{2.4}$$

where,

ΔD is the loss in duty,

D is the total phase shift given between S_1 and S_3.

$$D_{eff} = \frac{D}{1 + \frac{4N^2 L_{lk} f_s}{R_0}} \tag{2.5}$$

where,

f_s is the switching frequency,

N is the transformation ratio,

R_o is the load resistance.

Mode-8

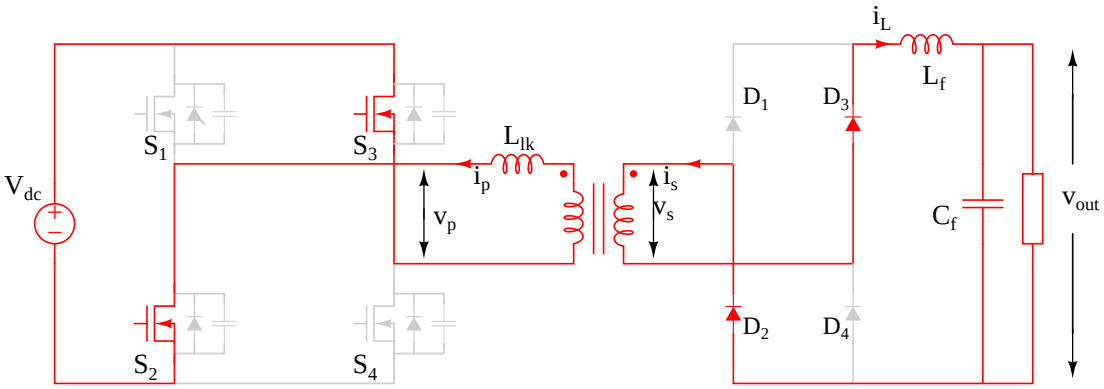


Figure 2.10: Mode-8

Mode-8 [Fig. 2.10] starts when the transition interval ends. Switches S_2, S_3 is conducting. Diodes D_1, D_4 is not conducting. Transformer secondary voltage is negative. Diodes D_2, D_3 are still conducting, resulting in energy transfer. Inductor current increases.

Modes	FB Converter	Diode Bridge Rectifier
1	S_1, S_2	D_1, D_4
2	S_1, C_3, C_4	
3	S_1, D_{S3}	
4	S_1, S_3	
5	C_1, C_2, S_3	D_1, D_2, D_3, D_4
6	D_{S2}, S_3	
7	S_2, S_3	
8	S_2, S_3	D_2, D_3

Table 2.1: Modes of operation of PSFB for one half of switching cycle

Different modes of operation and the conducting devices of FB converter and diode bridge rectifier for one half of switching cycle are tabulated as shown in Table. 2.1.

2.1.1 Steady State Voltage Gain

Phase shifted full bridge converter is a buck derived topology. Voltage seen across the inductor is at twice the switching frequency. Therefore for analysis only half of the switching cycle is considered. Expression for voltage across the inductor is given as

$$v_L(t) = -V_o \quad for\ \Delta D\frac{T_s}{2}$$

$$v_L(t) = nV_{dc} - V_o \quad for\ D_{eff}\frac{T_s}{2}$$

$$v_L(t) = -V_o \quad for\ (1-D)\frac{T_s}{2}$$

According to volt-second balance,

$$< v_L(t) >= -V_o\Delta D + (nV_{dc} - V_o)D_{eff} - V_o(1-D) \tag{2.6}$$

$$0 = -V_o(\Delta D + D_{eff} + 1 - D) + (nV_{dc})D_{eff}$$

Therefore, expression for output voltage is

$$V_o = nV_{dc}D_{eff} \tag{2.7}$$

CHAPTER 3

Simulation and Experimental Results

In this chapter the simulation and experimental results pertaining to the PSFB converter will be discussed. Relevant waveforms showing the characteristics of the PSFB converter are presented.

The specifications of the DC-DC converter is shown in Table 3.1.

Table 3.1: Specifications of PSFB converter

Specifications	
Power rating	500 W
DC input voltage	45 V-52 V
Switching frequency	100 kHz
DC output voltage	400 V
Turns ratio of transformer	12
Leakage inductance of transformer	0.7 μH
Load Resistance	320 Ω

3.1 Simulation Results

A 500 W, 48 V/400 V DC-DC converter was simulated in MATLAB Simulink. The simulation analysis is based on some assumptions like the transformer block is considered ideal. The magnetizing inductance, leakage inductance, and winding resistances are added externally. Winding resistances of the output filter inductor and ESR of the output filter capacitor are neglected. Output capacitance of the MOSFET given in the datasheet is included for the analysis. Output capacitance of the diode resonates with the leakage inductance of the transformer and high frequency oscillations occur which is observed in the hardware results. But for easy analysis capacitance of the diodes are not included.

Fig. 3.1 shows the gating signals for the switches along with the transformer primary voltage, current and transformer secondary voltage, voltage across the inductor,

inductor current. Phase shift between switches S_1, S_3 is fixed according to the steady state voltage gain required. Dead time between the complementary pair of switches S_1, S_2 and S_3, S_4 are chosen such that output capacitance of the switch to be turned ON is fully discharged within the time delay. Duty loss due to the presence of leakage inductance of the transformer is observed from the waveform.

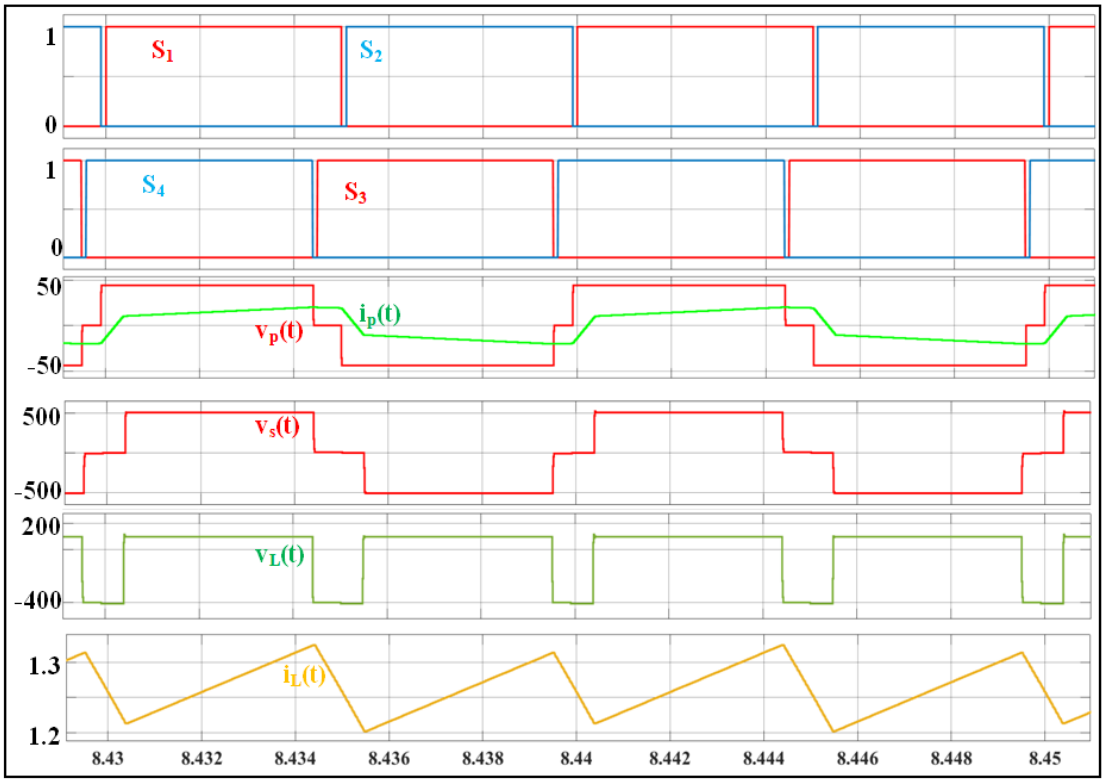


Figure 3.1: Simulation Results: Gating signals of S_1, S_2, S_3, S_4, transformer primary voltage $v_p(t)$ and transformer primary current $i_p(t)$, transformer secondary voltage $v_s(t)$, voltage across the inductor $v_L(t)$, inductor current $i_L(t)$.

Fig. 3.2 shows the output current $i_o(t)$, inductor current $i_L(t)$, transformer secondary current $i_s(t)$, current through the diodes D_1, D_2, D_3, D_4. Here we can see that all diodes conduct during the transition interval, which infact results in the duty loss. The simulation results obtained are as expected.

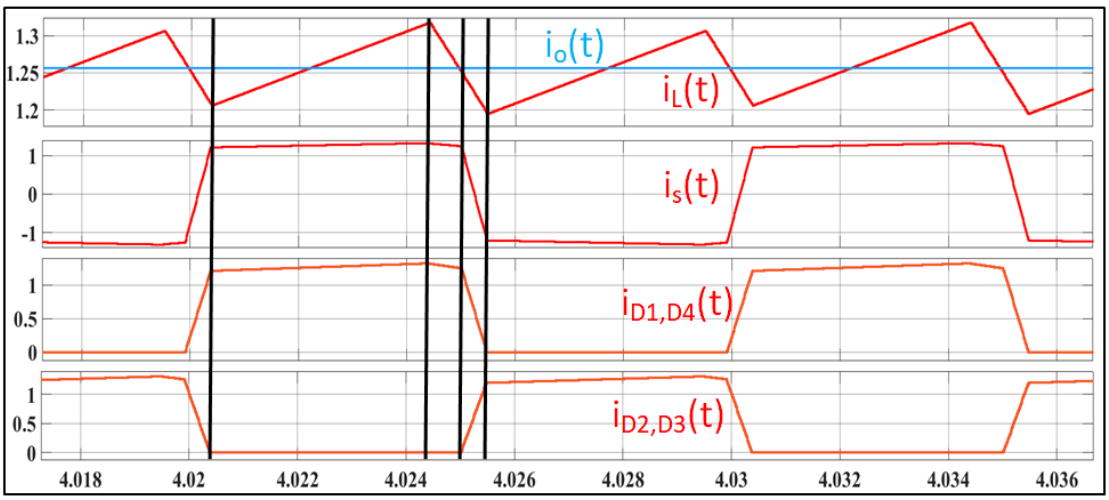


Figure 3.2: Simulation Results: Output current $i_o(t)$, inductor current $i_L(t)$, transformer secondary current $i_s(t)$, current through the diodes D_1, D_2, D_3, D_4.

Figures 3.3, 3.4, 3.5, 3.6 show the gating signal, current through the switch and voltage across the switch. Current from drain to source is considered as positive direction of current. It is seen that gating signals are applied to each switch when the current through them is negative, which ensures that the body diode is already in conduction while the gating signal is applied. Therefore, the switches are turned ON at ZVS condition as inferred from the simulation results. It is evident from these waveforms that switches S_3, S_4 attain ZVS easily than S_1, S_2 due to the availability of more energy in the leakage inductor of transformer at the time of turn ON transition of respective switches.

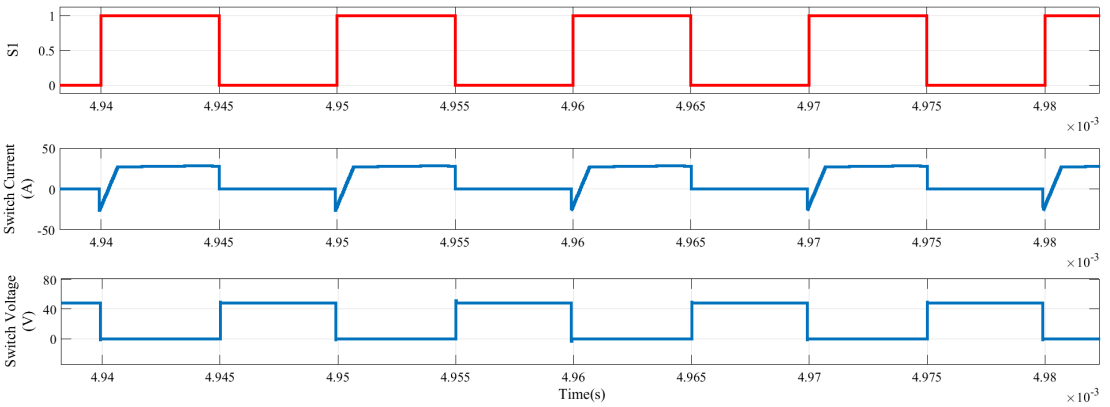


Figure 3.3: Simulation results: Gating signal of S_1, switch current (A),$i_{S1}(t)$, drain to source voltage (V) of the switch, $v_{ds}(t)$.

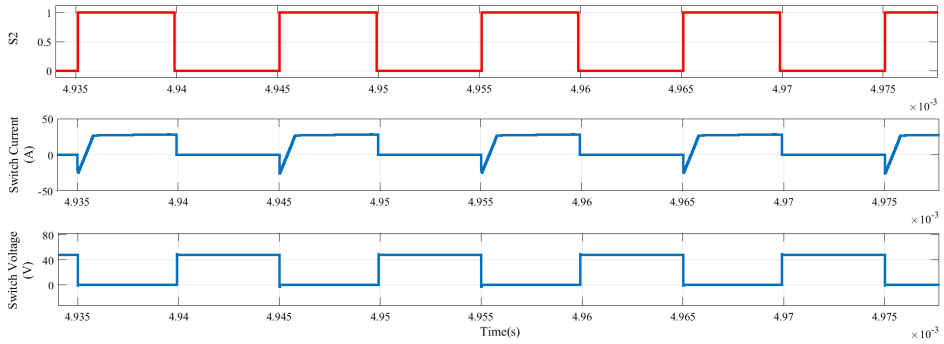


Figure 3.4: Simulation results: Gating signal of S_2, switch current (A),$i_{S2}(t)$, drain to source voltage (V) of the switch, $v_{ds}(t)$.

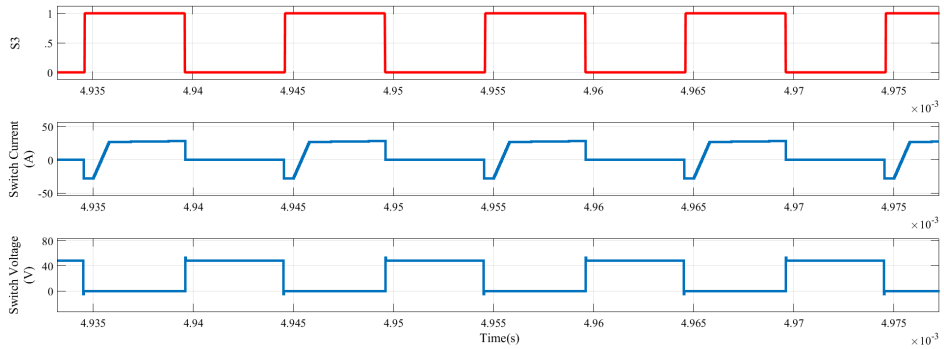


Figure 3.5: Simulation results: Gating signal of S_3, switch current (A),$i_{S3}(t)$, drain to source voltage (V) of the switch, $v_{ds}(t)$.

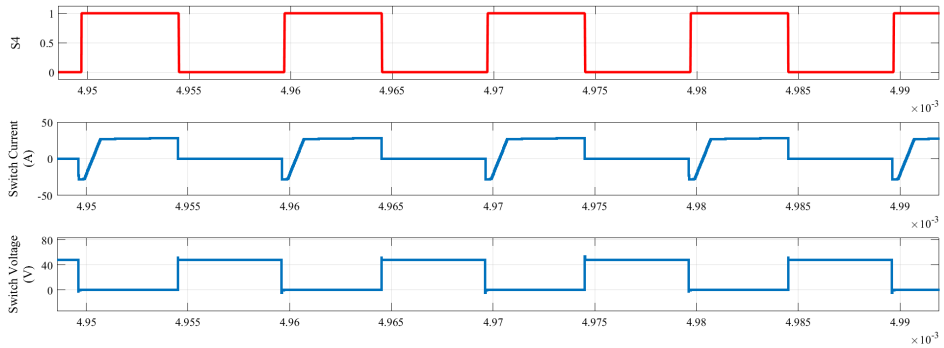


Figure 3.6: Simulation results: Gating signal of S_4, switch current (A),$i_{S4}(t)$, drain to source voltage (V) of the switch, $v_{ds}(t)$.

3.2 Experimental Results

A prototype of 500 W, 48V/400V DC-DC converter was built and tested in the lab. The key control device used is an TMS320F28335 DSP board which is based on Texas Instrument's C2000 series DSP chip. This DSP CPU has a internal clock of f_{clock} = 150 MHz. Waveforms obtained while testing the prototype for rated conditions with resistive load are shown.

In this project, MOSFET IXTH200N10T is used as the switching device in the FB converter. Since the switches in each leg are complementary and they operate at 50% duty, bootstrap IC IR2110 is used. IR2110 is high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Therefore one IC drives two switches in one leg of the FB converter. Inorder to provide isolation between the power ground and signal ground opto isolator, HCPL-3120 is used. Design of the high frequency transformer is given in the appendix. Diode used in the diode bridge rectifeir is RHRP15120 which is rated for 15A, 1200V. However as mentioned earlier due to the oscillations caused by leakage inductance, stray inductances, diode output capacitances and transformer winding capacitances, peak voltage across the diodes are much higher than the rating of the diodes as seen in Fig. 3.10a. Therefore instead of one diode in the diode bridge rectifier as shown in the circuit diagram (Fig. 2.1), two diodes in series is used for the experiment. This arrangement leads to increased conduction loss due to higher forward voltage drop of diode. Output filter consists of 3 mH inductor and 10 μF capacitor. Design of the output filter inductor is given in the appendix.

Fig. 3.7 shows the gating signals to S_1, S_3. S_1 is taken as the reference, S_3 is given a phase shift of 0.8, where phase shift of 1 corresponds to π rad. Figures 3.8a, 3.8b shows the complementary gating signals for both the legs of the FB converter.

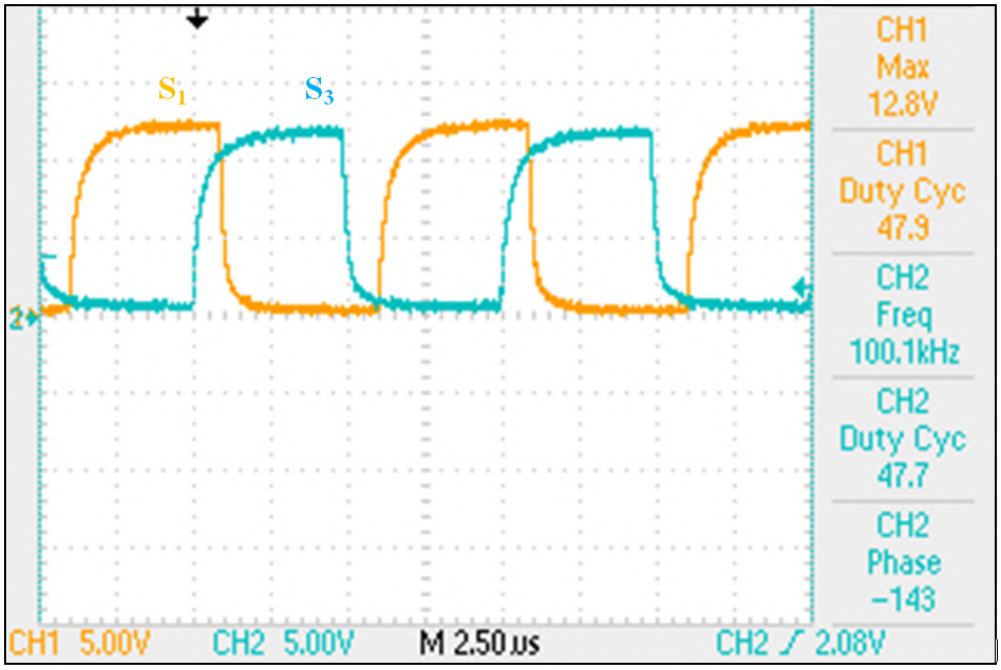
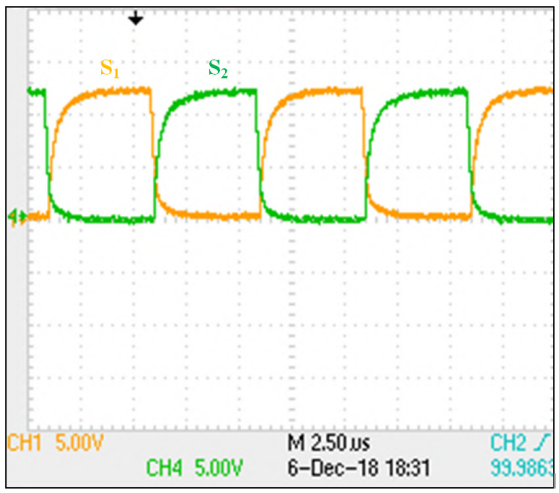
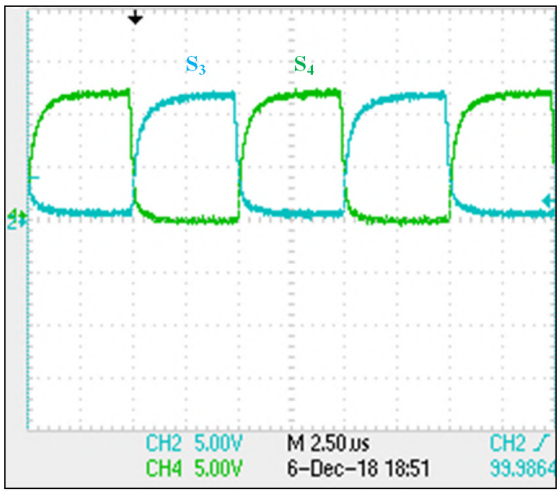


Figure 3.7: Hardware results: Phase shifted gating signals of S_1 and S_3



(a) Scale: $v_g s(t)$ of S_1: 5 V/div, $v_g s(t)$ of S_2: 5 V/div



(b) Scale: $v_g s(t)$ of S_3: 5 V/div, $v_g s(t)$ of S_4: 5 V/div

Figure 3.8: Hardware results: Gating signals for FB converter

Fig. 3.9 shows the transformer primary voltage $v_p(t)$ and transformer primary current $i_p(t)$. Fig. 3.10a shows the voltage across the diode. It is clear that the peak of the voltage is 1.3 kV, due to which two diodes in series was used in the hardware. Fig. 3.10b shows the transformer secondary voltage $v_s(t)$ and transformer primary current $i_p(t)$.

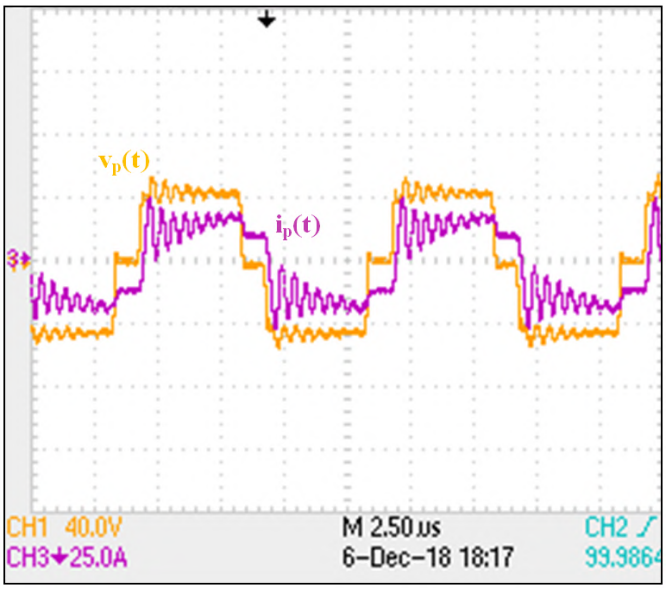
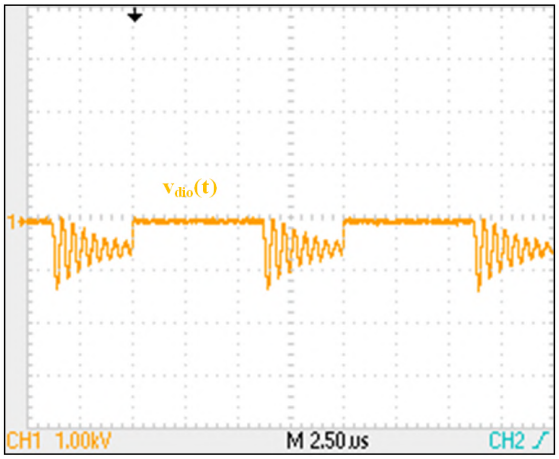
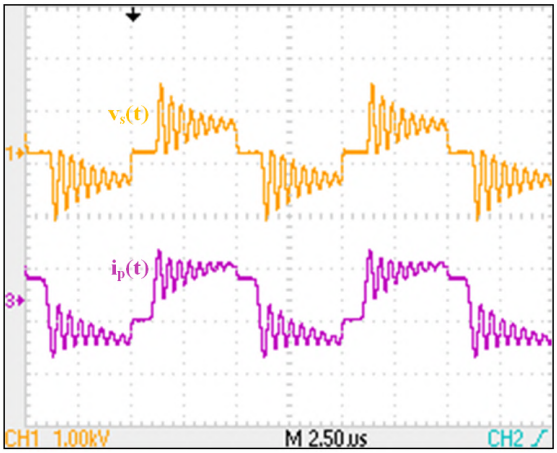


Figure 3.9: Hardware results: Transformer primary voltage $v_p(t)$ and transformer primary current $i_p(t)$. Scale: $v_p(t)$: 40 V/div, $i_p(t)$: 25 A/div



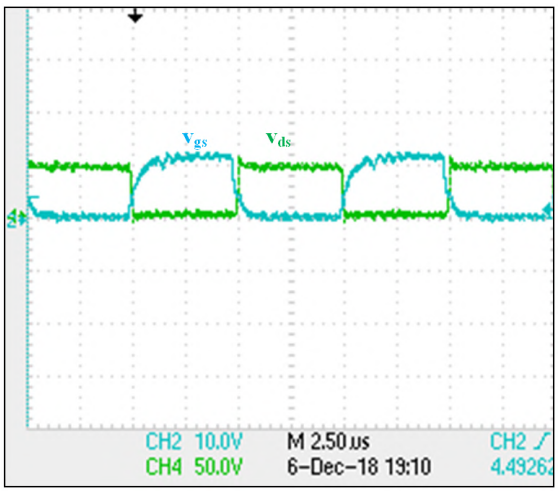
(a) Scale: $v_{dio}(t)$: 1000V/div



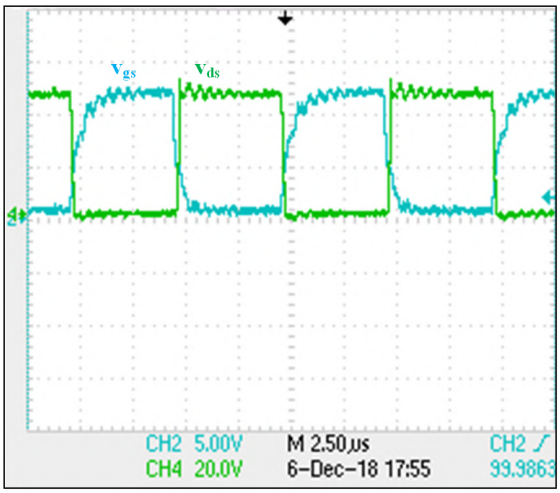
(b) Scale: $v_s(t)$: 1000 V/div, $i_p(t)$: 25 A/div

Figure 3.10: Hardware results: Diode voltage $v_{dio}(t)$, Transformer secondary voltage $v_p(t)$ and transformer primary current $i_p(t)$.

Figures 3.11a, 3.11b show drain to source voltage $v_{ds}(t)$ and gate to source voltage $v_{gs}(t)$ of switches S_1, S_3. It is clear that $v_{gs}(t)$ reaches its threshould value only after the $v_{ds}(t)$ approaches to zero. Therefore the swicthing happens at ZVS conditions. The transformer primary current $i_p(t)$ and gate to source voltage $v_{gs}(t)$ of switches S_1, S_3 in Figures 3.12a, 3.12b show that gating signals are given to the switches when the current through them is negative, forcing the body diode to conduct.

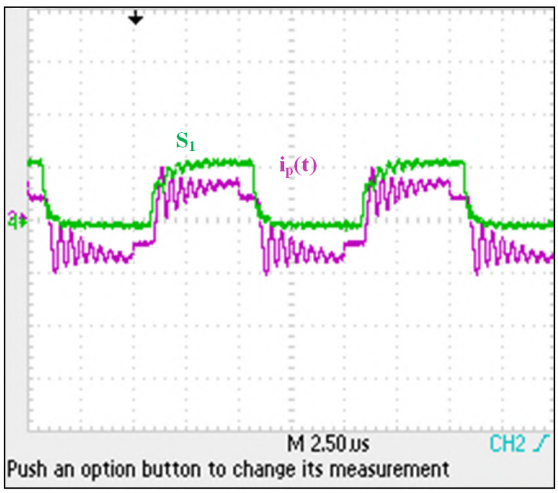


(a) Scale: $v_gs(t)$ of S_1: 10 V/div, $v_ds(t)$ of S_1: 50 V/div

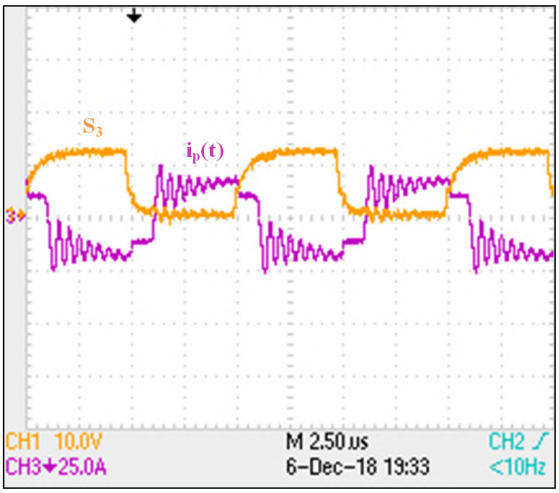


(b) Scale: $v_gs(t)$ of S_3: 5 V/div, $v_ds(t)$ of S_3: 20 V/div

Figure 3.11: Hardware results: Drain to source voltage and gate to source voltage of switches S_1, S_3



(a) Scale: $i_p(t)$: 25A/div, $v_{gs}(t)$: 10V/div



(b) Scale: $i_p(t)$: 25A/div, $v_{gs}(t)$: 10V/div

Figure 3.12: Hardware results: Transformer primary current $i_p(t)$ and gate to source voltage $v_{gs}(t)$ of switches S_1, S_3

CHAPTER 4

Single Stage DC-AC Converter

Single stage DC-AC converter with HFAC link is employed in low input voltage fed renewable energy applications due to high efficiency, high power density and less component count [11–13]. Single stage DC-AC converter consists of FB converter and a cycloconverter with HFAC link [11–15]. In this project the diode bridge rectifier in the PSFB converter is replaced with a cycloconverter to obtain the single stage DC-AC converter as shown in Fig. 4.1.

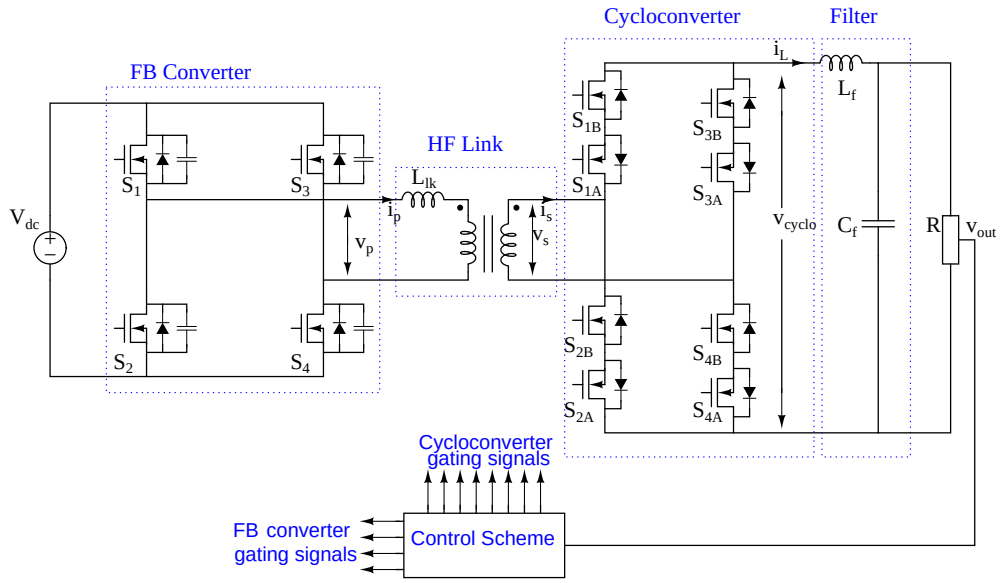


Figure 4.1: Single stage DC-AC converter

4.1 Converter Operation

The switches S_1, S_2, S_3 & S_4 forms the FB converter and S_{1A}, S_{1B}, S_{2A}, S_{2B}, S_{3A}, S_{3A}, S_{4A} & S_{4B} forms the cycloconverter. FB converter converts DC to HFAC. The output of the FB converter is a quasi square wave whose pulse width varies sinusoidally as shown in Fig 4.3. The FB converter output voltage is stepped up with the HF link transformer. Therefore the overall size of the transformer is smaller. The output of the transformer is the input to the cycloconverter which then converts the HFAC to the LFAC (50Hz). The

output filter (L,C) then eliminates the switching harmonics, thus giving the required AC output.

4.2 Converter Control Schemes

The output voltage of the single stage DC-AC converter can be controlled either using FB converter or using cycloconverter. The output voltage is controlled by sinusoidal PWM scheme in the cycloconverter, while switching the FB converter at fixed 50% duty [12]. However, this control scheme is to be designed to ensure smooth current commutation for the cycloconverter switches at all load variations. Much simpler control method is to control the FB converter and use the cyclocnverter only for the frequency conversion. The latter is explained in the following sections.

4.2.1 FB Converter

Control of FB converter is done to convert the DC to HFAC. It can be done either by using duty controlled PWM or sinusoidal phase-shift PWM. Advantages and disadvantages of both the schemes are briefly explained in this section.

Duty controlled PWM

In this control scheme, duty cycle of each gating signal is varied sinusoidally as shown in Fig. 4.2. Here the diagonal switches are switched together to get the required output. Limitation in attaining lower duty ratios is observed due to the turn ON and turn OFF time of switch, propagation delay of the driver ICs and isolators used. Also, bootstrap ICs cannot be used for the gate drive since time required to charge the boostrap capacitance will be lower for lower duty. In addition soft switching is also not achieved in this control scheme leading to higher switching losses. Therefore sinusoidal phase shift PWM is used for the conversion of DC to HFAC in the FB converter. This is explained in the next section.

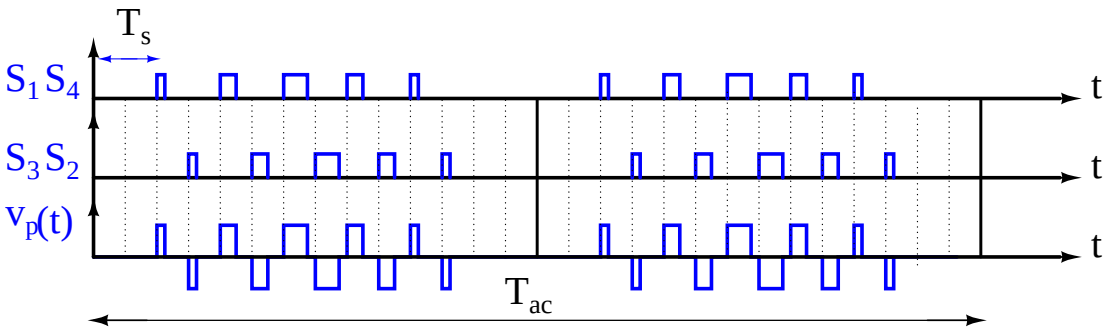


Figure 4.2: Duty controlled PWM scheme

Sinusoidal Phase Shift PWM

The gating signals for the FB converter switches as in [11] are shown in Fig. 4.3. All the switches are operated at 50% duty. Instead of switching the diagonally opposite switches together, a phase shift is given between the left leg (S_1, S_2) and the right leg (S_3, S_4), and it is varied sinusoidally. This phase shift determines the operating duty of the FB at that time. Switches S_1, S_2 and S_3, S_4 are complementary pairs. Leakage inductance of the transformer is designed such that the switches achieve ZVS turn ON for a wide range of line frequency and load. Thus soft switching of the FB converter switches improves the total efficiency, and reduces the current spikes accross the devices. The phase modulation is done in such a way so as to control the RMS of the AC output voltage.

4.2.2 Cycloconverter

With sinusoidal phase-shift control in the FB converter, the cycloconverter switches could be switched at line frequency, high frequency or combined line/high frequency. With the line frequency switching of the cycloconverter switches, control is simple [10, 12]. However, conduction loss due to body diode is high, reducing the efficiency of the converter. With high frequency switching, complexity of the control increases, but conduction loss due to body diode is reduced [12]. Therefore, it is preferred to use combined line/high frequency switching for improved efficiency and reduced complexity [11, 12]. The control schemes are explained in detail in the following sections.

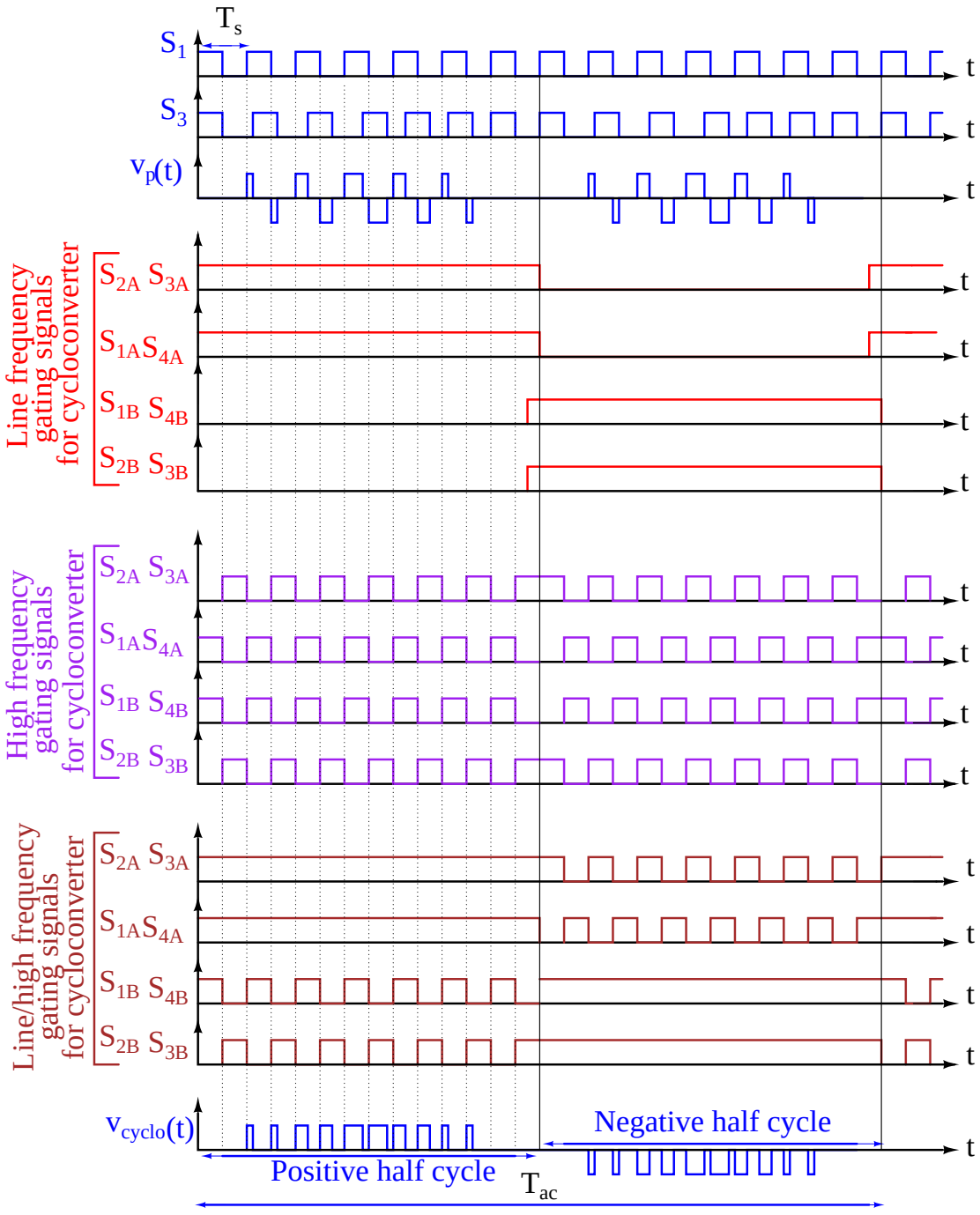


Figure 4.3: Principal operating waveforms and gating signals for switches

Line Frequency Switching in Cycloconverter

In this control scheme, switches in the cycloconverter side are operated at 50 Hz as in [10], thereby reducing the switching loss in cycloconverter side as shown in Fig. 4.3. During the positive half cycle of the output voltage, switches S_{1A}, S_{2A}, S_{3A}, S_{4A} are turned ON and for the negative half cycle, switches S_{1B}, S_{2B}, S_{3B}, S_{4B} are turned ON as shown in Fig. 4.3. Therefore, during positive half cycle, when the input current to cycloconverter is positive, S_{1A}, body diode of S_{1B}, S_{4A}, body diode of S_{4B} conducts and when the input current is negative body diode of S_{2B}, S_{2A}, body diode of S_{3B}, S_{3A} conducts. Similarly, during the negative half cycle of the output, when the input current to cycloconverter is positive, S_{2B}, body diode of S_{2A},S_{3B}, body diode of S_{3A} conducts and when the input current is negative body diode of S_{1A}, S_{1B}, body diode of S_{4A}, S_{4B} conducts. In this configuration, irrespective of the mode of operation of the FB converter, current from the secondary of the transformer always has a path to flow. In addition, at the end of every half cycle of the output voltage, an overlap interval is provided for the cycloconverter switches as shown in Fig. 4.3 so that the inductor current does not fall abruptly to zero. Thus the issue of high voltage spikes across the devices is eliminated. The configuration implemented for the gating signals ensures smooth transitions for all the semiconductor devices on the cycloconverter side and phase shifted front end. This control scheme is very simple, but conduction of body diode will lead to higher conduction losses, thereby reducing the efficiency of converter especially at higher power rating. One of the advantages of this control implementation is that the switching losses are minimal.

High Frequency Switching in Cycloconverter

The gating signals for the cycloconverter are shown in Fig. 4.3 as in [16]. All the switches are switched at 50 kHz and operates with 50% duty. During the positive half cycle of output, gating signals of S_{1A}, S_{1B}, S_{4A}, S_{4B} follows the gating signal of S_1. Likewise, during the negative half cycle of output, gating signals of S_{2A}, S_{2B}, S_{3A}, S_{3B} follows the gating signal of S_1. Gating signals of S_{2A}, S_{2B}, S_{3A}, S_{3B} are complementary to that of S_{1A}, S_{1B}, S_{4A}, S_{4B} throughout the line frequency cycle. The leakage inductance in the HF transformer and the output filter inductance acts as current sources. Therefore, during the switching transitions in the cycloconverter, high

volatge spikes occur leading to device damage. Therefore the switches are provided with suitable overlap (not shown in Fig.4.3) so that the output inductor current is not interrupted. However this is not true for the HF transformer leakage inductance. Therefore every switch interruption will produce an overvoltage across L_{lk}. It is necessary to absorb the leakage energy to limit the overvoltage. Therefore additional snubber circuit should be provided for absorbing the leakage energy [16]. Thus, this control scheme requires additional circuitry and complex control scheme to achieve required output. With combined line/high frequency switching, the gating signals could be configured to ensure soft switching (turn on and turn off) of all the switches of the cycloconverter. This is discussed in detail in the next section.

Combined Line/High Frequency Switching in Cycloconverter

The gating signals for the cycloconverter as in [11] are shown in Fig. 4.3. One set of four switches are always kept ON and the other set of four switches are switched at 50 kHz for each half cycle. During the positive half cycle of output, S_{1A}, S_{2A}, S_{3A}, S_{4A} are turned ON and S_{1B}, S_{2B}, S_{3B}, S_{4B} are switched at 50 kHz. Gating signals for S_{1B}, S_{4B} are same as that of S_1. Gating signals of S_{1B}, S_{4B} and S_{3B}, S_{2B} are complementary. Likewise, during the negative half cycle, S_{1B}, S_{2B}, S_{3B}, S_{4B} are turned ON and S_{1A}, S_{2A}, S_{3A}, S_{4A} are switched at 50 kHz. Gating signals for S_{2A}, S_{3A} are same as that of S_1. Gating signals of S_{2A}, S_{3A} and S_{1A}, S_{4A} are complementary. Due to the presence of the leakage inductance of the transformer there is a duty loss which is shown in Fig. 4.4. Secondary voltage of the transformer as shown in Fig. 4.4 is given as input to the cycloconverter. All the switches have ZVS turn ON since the gating pulses are given to the switches during the transition interval, which is explained in the next section. As shown in Fig. 4.4 switches are turned OFF while there is current flowing through it, forcing the body diode of the switch to conduct, therefore voltage across the switch during turn OFF will be the body diode drop resulting in negligible turn OFF loss. Thus switching loss in this control implementation is minimal. Here, the conduction loss will be lesser since the switches are conducting instead of the body diode. Thus overall loss is less compared to the line frequency switching scheme in cycloconverter. Also, at every half cycle, there is an inherent overlap interval due to which the inductor current gets ample time to reduce to zero thereby eliminating the occurrence of any voltage

spikes across the device. This control scheme is relatively simple and achieves higher efficiency compared to the line frequency switching scheme.

4.3 Converter operation with sinusoidal phase modulated FB converter and combined line/high frequency switching of cycloconverter

Converter operation with sinusoidally phase modulated FB converter and cycloconverter switched at combined line/high frequency is explained in the following sections. The converter operation for the positive cycle of the AC voltage is analyzed based on the switching modes described in one half of switching period as shown in Fig. 4.4. Devices conducting in each interval is shown in Table 4.1 for the switching scheme assuming the switching cycle taken belongs to the positive half cycle of output voltage.

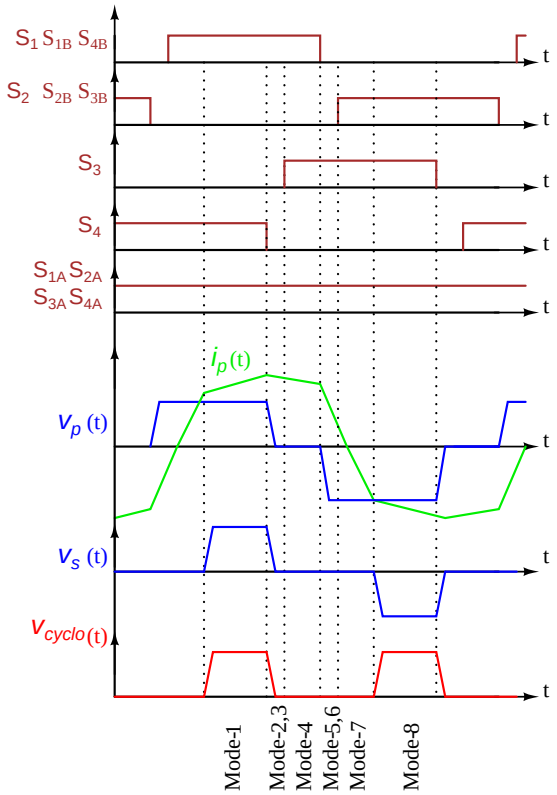


Figure 4.4: Principal operating waveforms in one switching cycle of positive half cycle of output voltage

Mode-1

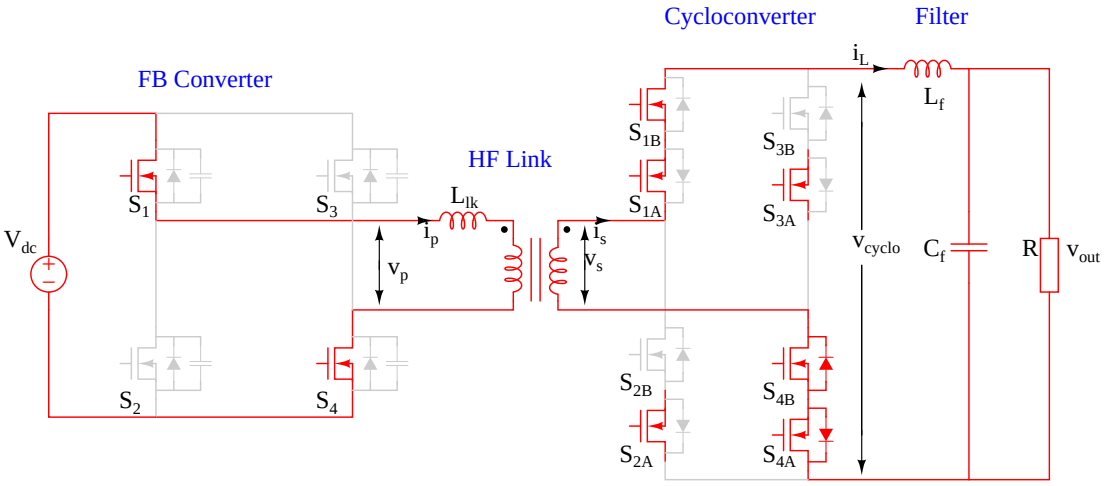


Figure 4.5: Mode-1

During this mode [Fig.4.5], switches S_1, S_4, S_{1A}, S_{2A}, S_{3A}, S_{4A}, S_{1B} and S_{4B} are ON. The transformer primary current $i_p(t)$, transformer primary and secondary voltages $(v_p(t), v_s(t))$ are positive. Output current is positive and flows through switches S_{1A}, S_{1B}, S_{4A}, S_{4B} and the transformer secondary.

Mode-2

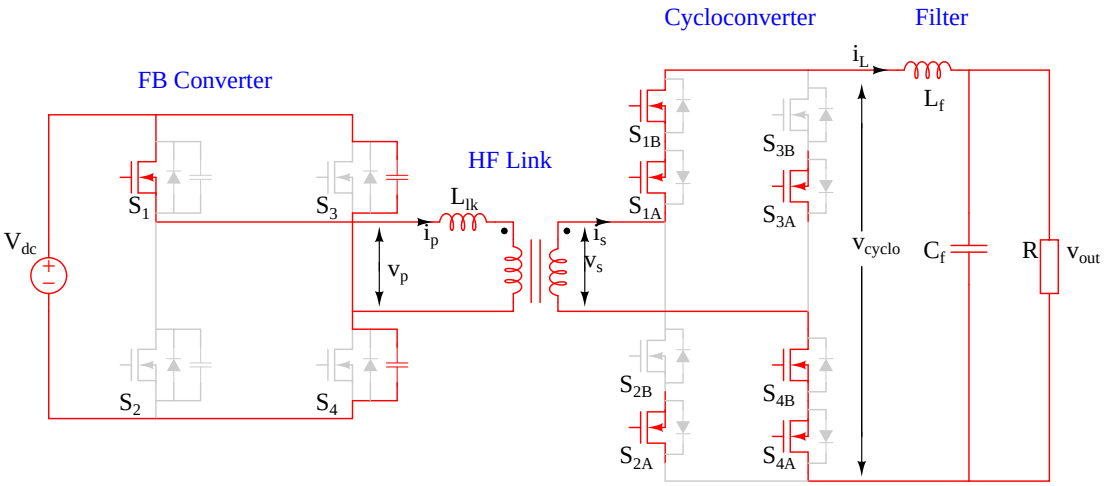


Figure 4.6: Mode-2

At the beginning of this interval [Fig.4.6], the gate voltage of S_4 undergoes a high-to-low transition. As a result, the output capacitance of S_4 begins to accumulate charge, while the output capacitance of S_3 begins to discharge. The transformer primary and secondary voltage starts falling to zero. Once the voltage across S_3 goes to zero, it can

be turned on under ZVS. The transformer primary current i_p and the load current i_{out} continue to flow in the same direction. Leakage inductance of transformer is designed such that sufficient energy is available to charge and discharge the output capacitances of switches S_3 and S_4.

Mode-3

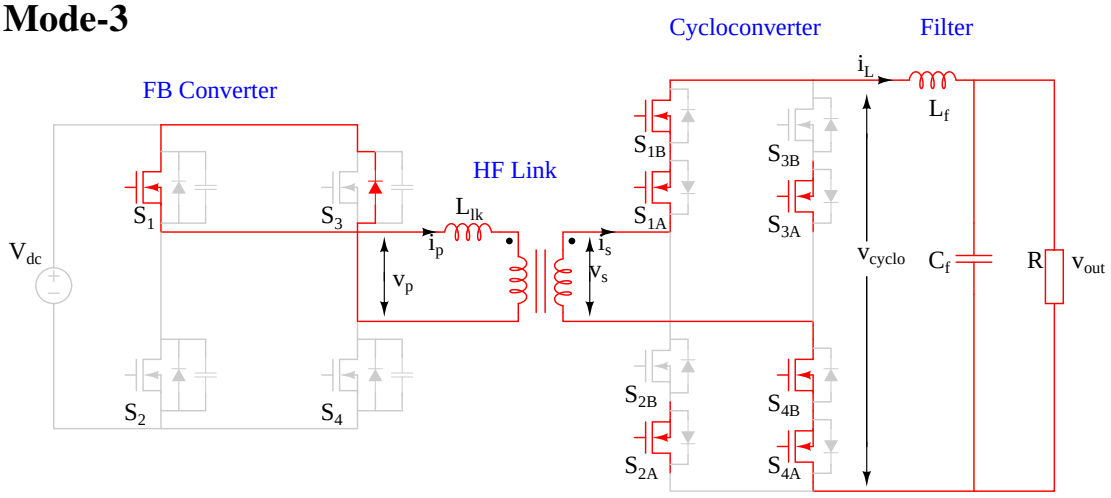


Figure 4.7: Mode-3

This mode [Fig.4.7] initiates when S_4 turns off. The transformer primary current is still positive and freewheel through body diode of S_3. Moreover, the load current continues to flow in the same direction as in Mode 2. The transformer primary and secondary voltages are zero. Dead time between the gating pulses to S_4 and S_3 is chosen in such a way so that output capacitance of S_3 is fully discharged and its body diode start conduction, thereby turning ON S_3 under ZVS.

Mode-4

In this mode [Fig.4.8], S_3 is turned ON. The transformer primary current freewheels through switches S_1 and S_3. The transformer voltages remain zero and the transformer primary current continues to flow in the same direction.

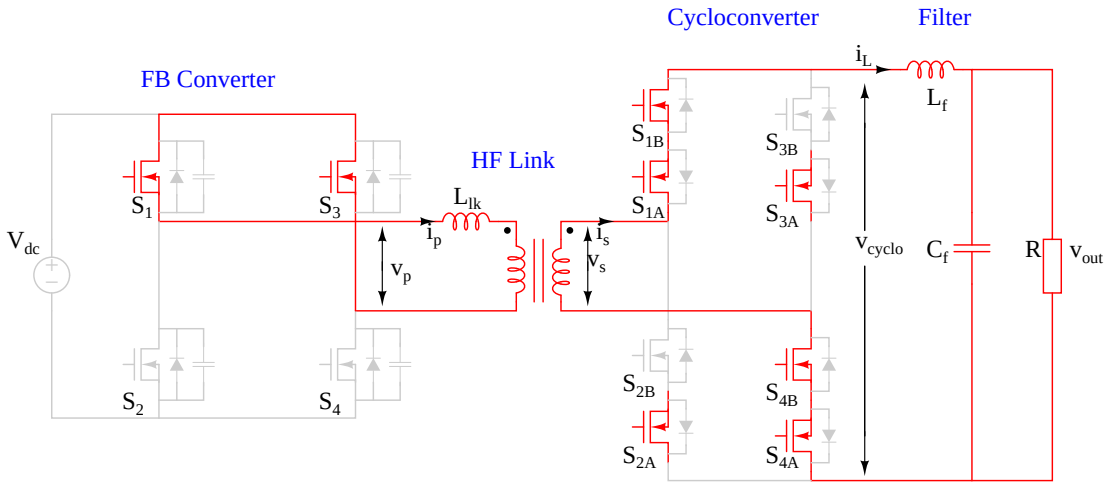


Figure 4.8: Mode-4

Mode-5

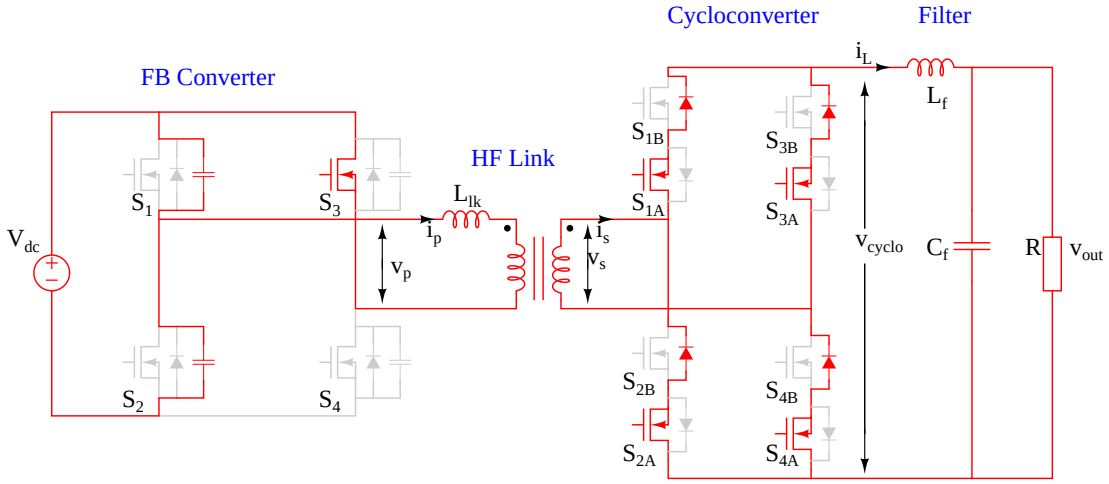


Figure 4.9: Mode-5

This mode [Fig.4.9] starts when the gate voltage of S_1,S_{1B} and S_{4B} undergoes a high-to-low transition. As a result, the output capacitance of S_1 begins to accumulate charge, while the output capacitance of S_2 begins to discharge. The transformer primary volatge starts increasing in negative direction. The transformer current is still in the same direction but starts falling. In the cycloconverter side, switches $S_{1A}, S_{2A}, S_{3A}, S_{4A}$ and body diodes of $S_{1B}, S_{2B}, S_{3B}, S_{4B}$ conducts. This initiates the freewheeling period for the cycloconverter. The transformer secondary voltage remains zero due to the presence of the leakage inductance of the transformer. Therefore the voltage across the switches in the cycloconverter are zero. Since the body diodes of switches S_{1B}, S_{4B} are conducting, the turn OFF of these switches happens at zero/low voltage.

Mode-6

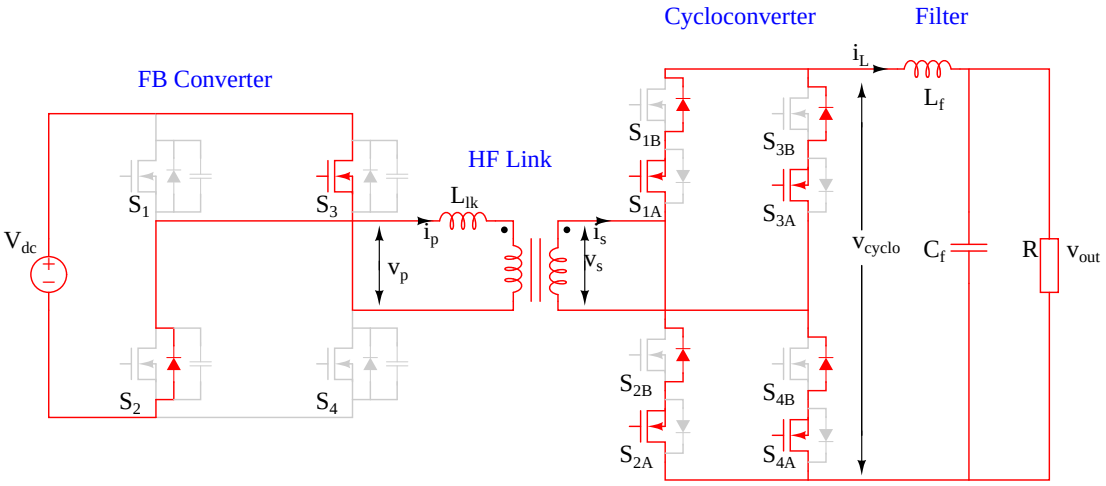


Figure 4.10: Mode-6

This mode [Fig.4.10] initiates when S_1 turns off. The transformer primary current is still positive and freewheel through body diode of S_2. The transformer primary voltage reaches it negative maximum and secondary voltage remain zero. Now S_2 can be turned ON under ZVS condition as the body diode of the switch is already in conduction. The transformer secondary voltage remains zero therefore the volatge across the switches are also zero. Therefore the switches S_{2B}, S_{3B} also can be turned ON at zero/low voltage. Cycloconverter continues to be in the freewheeling period.

Mode-7

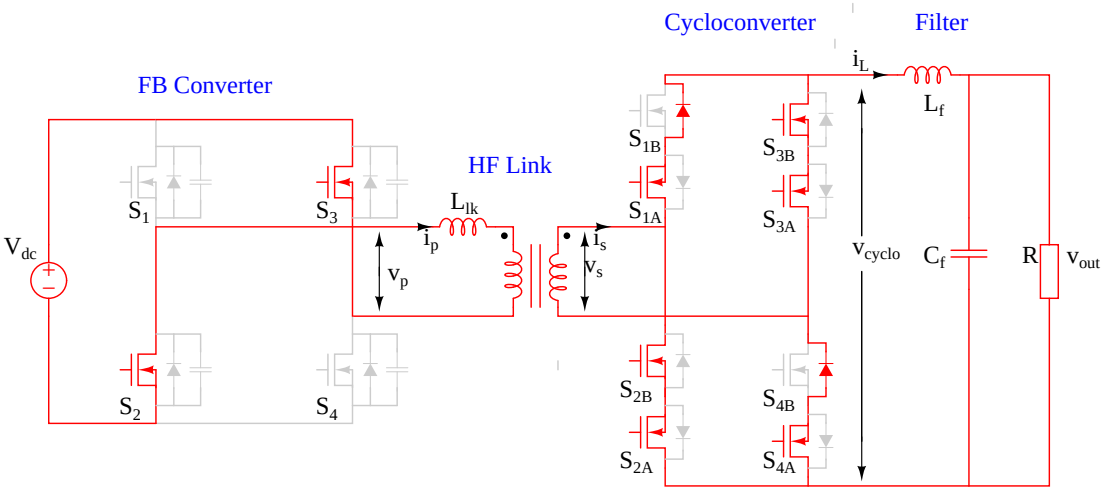


Figure 4.11: Mode-7

This mode [Fig.4.11] starts when S_2,S_{2B}, S_{3B} are ON. The transformer primary cur-

Table 4.1: Modes of operation of cycloconverter and conducting devices in one half of switching period in positive half cycle of output voltage

Modes	FB Converter	Cycloconverter
1	S_1, S_2	$S_{1A}, D^*_{1B}, S_{4A}, D^*_{4B}$
2	S_1, C_3, C_4	
3	S_1, D_3	
4	S_1, S_3	
5	C_1, C_2, S_3	$S_{1A}, D_{1B}, S_{2A}, D_{2B}, S_{3A}, D_{3B}, S_{4A}, D_{4B}$
6	D_2, S_3	
7	S_2, S_3	$S_{1A}, D_{1B}, S_{2A}, D^*_{2B}, S_{3A}, D^*_{3B}, S_{4A}, D_{4B}$
8	S_2, S_3	$S_{2A}, D^*_{2B}, S_{3A}, D^*_{3B}$

*Indicates channel conduction instead of body diode of the MOSFET

rent changes its direction to become negative. The transformer secondary voltage still remains zero. This interval marks the end of freewheeling period for the cycloconverter. The duty loss due to the presence of leakage inductance of the transformer can be seen in modes 5, 6 and 7.

Mode-8

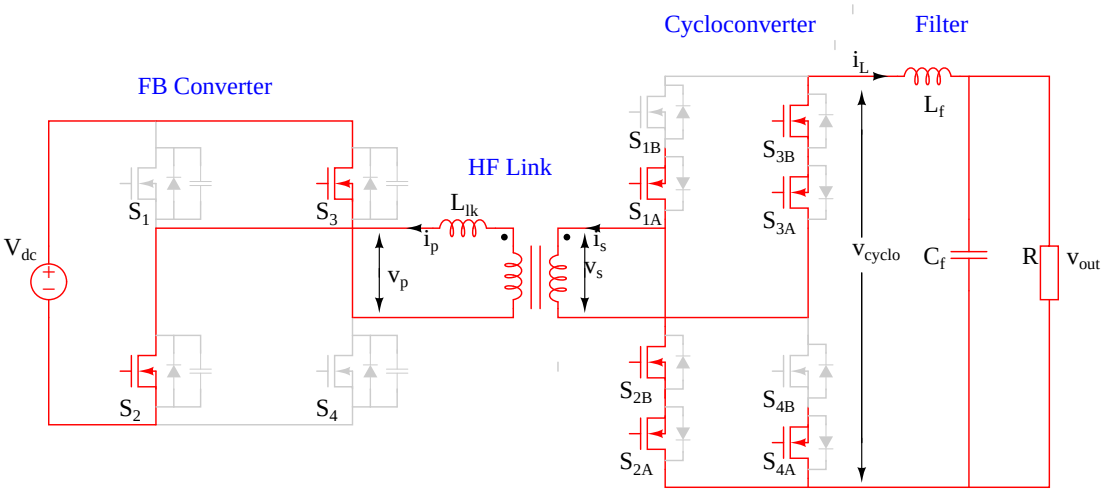


Figure 4.12: Mode-8

During this mode [Fig.4.12], switches S_2,S_3,$S_{1A}, S_{2A}, S_{3A}, S_{4A}, S_{2B}$ and S_{3B} are ON. The transformer primary current $i_p(t)$, transformer primary and secondary voltages $(v_p(t), v_s(t))$ are negative. Output current is positive and flows through switches S_{2A}, S_{2B},S_{3A}, S_{3B} and the transformer secondary.

4.4 Budgeting of Loss

4.4.1 FB Converter

Conduction loss in FB converter comprises of the losses due to the ON state resistance, R_{dsON} and the body diode conduction of MOSFETs. Therefore, the total conduction loss P_c is computed as

$$P_c = P_{RdsON} + P_D \tag{4.1}$$

where,

$$P_{RdsON} = 2.(P_{S1,S2} + P_{S3,S4}) \tag{4.2}$$

$$P_D = 2.(P_{D1,D2} + P_{D3,D4}) \tag{4.3}$$

$P_{S1,S2}$, $P_{S3,S4}$ represents the conduction losses due to R_{dsON} and $P_{D1,D2}$, $P_{D3,D4}$ represents the conduction losses due to forward voltage drop of body diode in switches S_1 and S_4 respectively. Losses in the switches S_1 and S_2 are same. Similar is the case for S_3 and S_4. $P_{S1,S2}$, $P_{S3,S4}$, $P_{D1,D2}$, $P_{D3,D4}$ are computed using equations given below [9, 11, 17].

$$P_{S1,S2} = I_{RMS1}^2 * R_{dsON} \tag{4.4}$$

$$P_{S3,S4} = I_{RMS4}^2 * R_{dsON} \tag{4.5}$$

$$P_{D1,D2} = V_f * I_{avg1} \tag{4.6}$$

$$P_{D3,D4} = V_f * I_{avg4} \tag{4.7}$$

where,

I_{RMS1} is the RMS current through switches $S1$,

I_{RMS4} is the RMS current through switches S_3,

I_{avg1} is the average current through the body diodes of $S1$,

I_{avg4} is the average current through the body diodes of S_4,

V_f represents the forward voltage drop of the body diode of the MOSFET. Expressions for I_{RMS1}, I_{RMS4}, I_{avg1}, I_{avg4} are derived as follows.

Assumptions made:

1.Filter inductor is large, therefore,

(i). Using small ripple approximation, inductor current and load current are same.

(ii). i_1=i_2=i_3

2. Eventhough switch is ON, all the negative currents flow through the body diode.

3. Dead time between the switches are not considered.

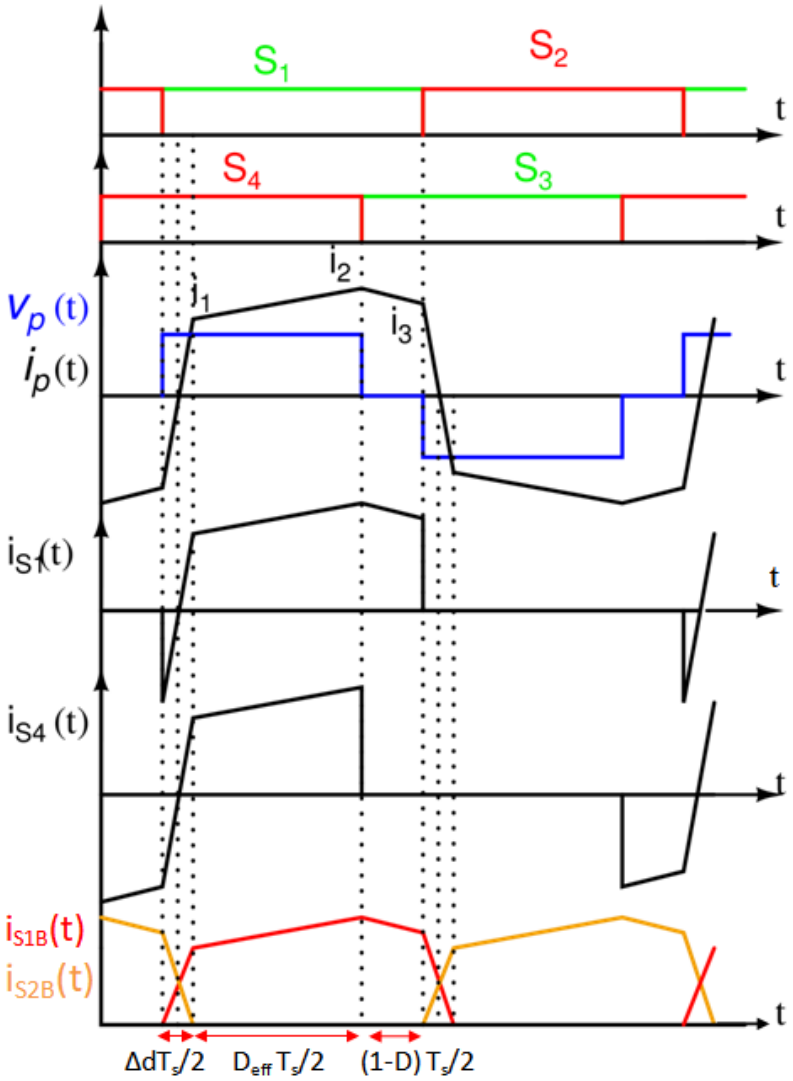


Figure 4.13: Operating waveforms of a single stage DC-AC converter

For a DC-AC converter the output current is sinusoidal. According to assumption (1),

$$i_L = I_m \sin \omega t \tag{4.8}$$

$$D = D_m \sin \omega t \tag{4.9}$$

$$D_{eff} = \frac{D}{1 + \frac{4N^2 L_{lk} f_s}{R_0}} \tag{4.10}$$

$$\Delta d = D - D_{eff} \tag{4.11}$$

where,

i_L is the inductor current,

I_m is the peak output current,

ω is the line frequency in radians

D_m is the modulation index,

D is the phase shift between S_1 and S_3 in a switching cycle,

Δd is the loss in duty due to the leakage inductance of transformer $L_l k$,

$D_e f f$ is the effective duty obtained after the duty loss in a switching cycle,

N is the transformation ratio,

f_s is the switching frequency,

R_0 is the load resistance.

Therefore, the RMS currents can be derived as sum of the RMS currents of all the switching cycles. Thus from Fig. 4.13 we obtain,

$$I_{RMS1} = \sqrt{\frac{T}{T_{ac}} \sum_{n=1,n\ odd}^{fsw/f} (\frac{I_1[(n-1)T_s]}{\sqrt{3}})^2 * \frac{\Delta d}{2} + I_1^2[(n-1)T_s] * D_{eff} + I_1^2[(n-1)T_s] * (1-D)} \tag{4.12}$$

$$I_{RMS4} = \sqrt{\frac{T}{T_{ac}} \sum_{n=1,n\ odd}^{fsw/f} (\frac{I_1[(n-1)T_s]}{\sqrt{3}})^2 * \frac{\Delta d}{2} + I_1^2[(n-1)T_s] * D_{eff}} \tag{4.13}$$

Average value can be found by finding the area under the curve. Thus,

$$I_{avg1} = \frac{T}{T_{ac}} \sum_{n=1,n\ odd}^{f_{sw}/f} \frac{I_1[(n-1)T_s]}{2} \frac{\Delta d}{2} \tag{4.14}$$

$$I_{avg4} = \frac{T}{T_{ac}} \sum_{n=1,n\ odd}^{f_{sw}/f} \frac{I_1[(n-1)T_s]}{2} \frac{\Delta d}{2} + I_1[(n-1)T_s] * (1-D) \tag{4.15}$$

where, $I_1(t)$ is approximated as $Ni_L(t)$.

4.4.2 Cycloconverter

Line Frequency Switching

Since switching loss in this scheme is negligible because of ZVS/ZCS during the switching, conduction loss becomes a major part of losses. Major conduction loss occurs due to body diode conduction and the MOSFET on-resistance, R_{dsON}. The values of R_{dsON} and V_f as given in the MOSFET datasheet are used for the analysis.

For the loss analysis in the cycloconverter, above mentioned assumptions are made. To make the computation more accurate, the sinusoidal variation within the switching cycle is taken into account. When cycloconverter is switched at line frequency, current through the switches and body diodes are identical for both the AC half cycle. Also, the conduction losses in all the switches are same due to the symmetry of waveform as in Fig. 4.13, therefore expressions for RMS and average currents through the switch S_{1B} over one AC half cycle is obtained as

$$I_{lrms} = \sqrt{\frac{1}{T_{ac}/2} \sum_{n=1,n\ odd}^{fsw/f} (I_1^* + I_2^*)} \tag{4.16}$$

where I_1^* and I_2^* are

$$I_1^* = \int_{(n-1+\Delta d)T_s/2}^{nT_s/2} i_L^2 dt \tag{4.17}$$

$$I_2^* = (\frac{i_L[(n-1+\Delta d)T_s/2)]}{\sqrt{3}})^2 \frac{\Delta d T_s}{2} + (\frac{i_L[nT_s/2]}{\sqrt{3}})^2 \frac{\Delta d T_s}{2} \tag{4.18}$$

$$I_{lavg} = \frac{1}{T_{ac}/2} \sum_{n=1,n\ odd}^{f_{sw}/f} (I_3^* + I_4^*) \tag{4.19}$$

where I_3^* and I_4^* are

$$I_3^* = \int_{(n-1+\Delta d)T_s/2}^{nT_s/2} i_L dt \tag{4.20}$$

$$I_4^* = \frac{1}{2} i_L[(n-1+\Delta d)T_s/2] \frac{\Delta d T_s}{2} + \frac{1}{2} i_L[nT_s/2] \frac{\Delta d T_s}{2} \tag{4.21}$$

Thus conduction loss in cycloconverter when switched at line frequency is

$$P_{cond_{lf}} = 8 * (I_{lrms}^2 * R_{dsON} + V_f * I_{lavg}) \tag{4.22}$$

Calculated conduction loss of the cycloconverter at 500 W output power is 13.26 W. Efficiency of 95.75% is achieved experimentally at 500 W.

Combined Line/High Frequency Switching

In this control scheme, all the switches have ZVS turn ON, thereby reducing switching loss. Conduction loss in body diode is negligible. Thus conduction losses are mainly due to MOSFET on-resistance. When cycloconverter is switched at line/high frequency, current through the switches and body diodes are not identical for both the AC half cycles. Therfore expressions for RMS and average currents through the switch S_{1B} for positive AC half cycle, when S_{1B} is switched at high frequency, is obtained as RMS current for the switch is given by

$$I_{hrms} = \sqrt{\frac{1}{T_{ac}/2} \sum_{n=1,n\ odd}^{fsw/f} (I_5^* + I_6^*)} \tag{4.23}$$

where I_5^* and I_6^* are

$$I_5^* = \int_{(n-1+\Delta d)T_s/2}^{nT_s/2} i_L^2 dt \tag{4.24}$$

$$I_6^* = (\frac{i_L[nT_s/2]}{\sqrt{3}})^2 \frac{\Delta d T_s}{2} \tag{4.25}$$

Expression for the negative AC half cycle is same as the expression for RMS current when cycloconverter is switched at line frequency. Therefore, total RMS current over one AC cycle is

$$I_{rms} = \sqrt{I_{hrms}^2 + I_{lrms}^2} \tag{4.26}$$

Expression for average current for positive half cycle is,

$$I_{havg} = \frac{1}{T_{ac}/2} \sum_{n=1,n\ odd}^{f_{sw}/f} \frac{1}{2} i_L[nT_s/2] \frac{\Delta d T_s}{2} \tag{4.27}$$

Thus, conduction loss when cycloconverter is switched at line/high frequency is

$$P_{cond_{l/hf}} = 8 * (I_{rms}^2 * R_{dsON} + V_f * I_{havg}) \tag{4.28}$$

Calculated conduction loss at 500 W output power is 3.28 W. Efficiency at 500 W output power is found to be 97.5% experimentally. Thus, efficiency improvement of 1.8% is found at 500 W power which is in agreement with the calculated values.

Figures 4.14, 4.15 show the variation of conduction loss as a function of switching frequency and rated power for line frequency as well as combined line/high frequency switching in cycloconverter.

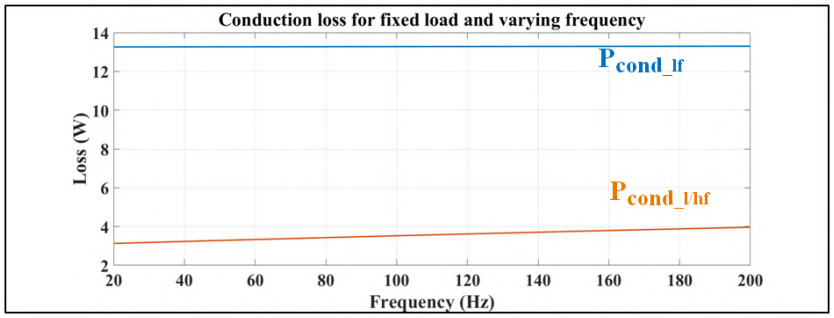


Figure 4.14: Conduction loss as a function of switching frequency

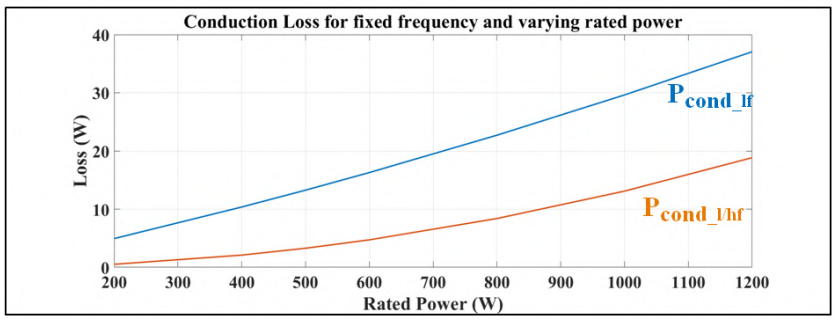


Figure 4.15: Conduction loss as a function of rated power

CHAPTER 5

Hardware Implementation and Results

Fig. 5.1 shows the block diagram of DC-AC converter with high frequency link. In this system, the input dc voltage is converted into high frequency ac voltage, isolated by a high frequency transformer and converted from high frequency to low frequency ac voltage by a cycloconverter. Operation and working of the converter is already discussed in the above sections.

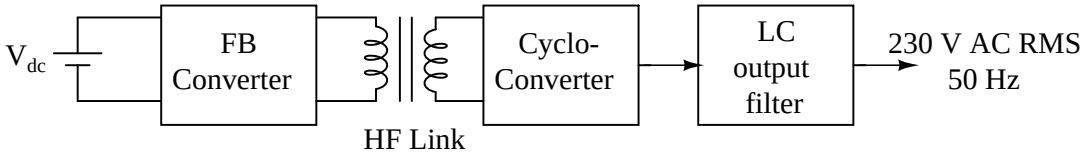


Figure 5.1: Block diagram of the single stage DC-AC converter

The specifications of the DC-AC converter is shown in Table. 5.1

Table 5.1: Specifications of single stage DC-AC converter

Specifications	
Power rating	500W
DC input voltage	45V-52V
Switching frequency	50kHz
AC output voltage	230V rms
Output frequency	50Hz

5.1 Device selection

5.1.1 FB Converter

The switches operate at high frequency, blocks positive voltage at 48 V and passes both positive and negative currents of 27 Amps. Therefore switch with lower ON state resistance is preferred to lower the conduction losses. MOSFET IXTH200N10T switching device is suitable for the above conditions, and is used. The conduction, blocking and

switching losses raise the junction temperature of the device. To limit the junction temperature of the device, proper thermal design has to be made. In the front end converter all the four MOSFET devices are mounted on the same heat sink. Each MOSFET switch ON state resistance is 5.5 Ω. Total conduction loss in the front end converter is sum of H bridge (S1, S2, S3 & S4) and boost stage (S1 & S2). The junction temperature of the device should be less than 110^o C. Fig. 5.2 shows the FB converter along with the gate driver circuit, where 1,2,3,4 are the switches S_1, S_2, S_3, S_4.

Gate Circuit for FB Converter

Since the FB converter switches S_1, S_2 and S_3, S_4 are complementary pairs and operate at 50% duty cycle, bootstrap ICs are used for gate drive. Bootstrap IC used is IR2110. 5,6 in Fig. 5.2 shows the gate driver IC.

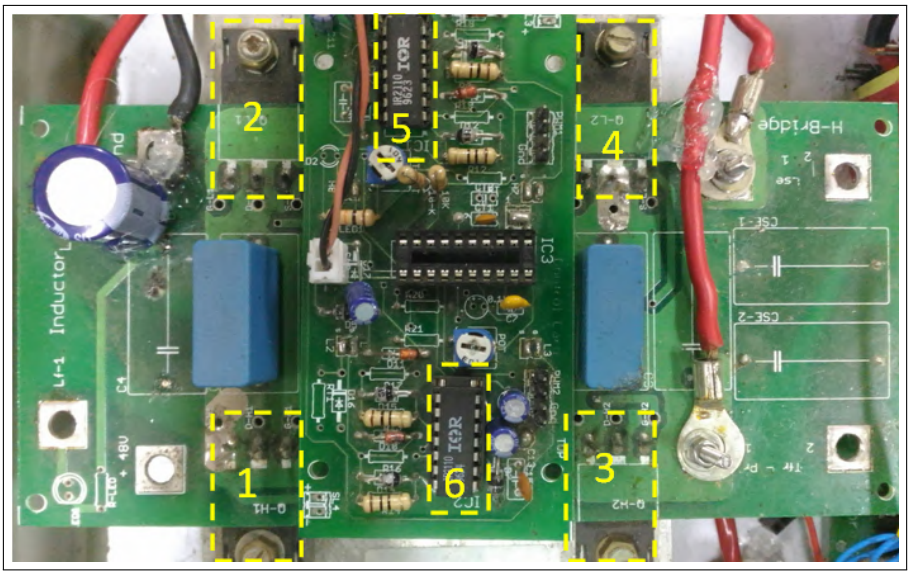


Figure 5.2: Hardware setup: FB converter

5.1.2 HF Transformer

The HF transformer steps up the FB converter output voltage. It handles 500 W at 50 kHz. The transformer is designed with ferrite core. 50 kHz HF transformer size is very small compared to 50 Hz cycle transformer. One of the critical requirement of the HF transformer is the low leakage inductance between the primary and secondary windings. This requirement is obtained by sandwich type winding.

5.1.3 Cycloconverter

The cycloconverter converts HFAC to LFAC. The switches in a matrix converter configured as cycloconverter, have to block bidirectional voltages and pass bidirectional currents. Such a four quadrant switch is shown in Fig. The cycloconverter employs four such four quadrant switches. In all 8 MOSFETs are used in the cycloconverter. Due to the leakage inductance of transformer and output capacitances of switches these switches of cycloconverter will be subjected to higher voltage spikes. Therefore switches of high blocking voltage should be selected. But the output capacitances of the switches will be higher, also the gate charge requirement as well as reverse recory time is high. Therefore it is preferred to use SiC MOSFETs. C2M0160120D SiC MOSFET is used. Fig. 5.3 shows the cycloconverter switches mounted on heat sink [indicated by (1)].

Gate Circuit for Cycloconverter

Each switch in the matrix converter should have separate isolated gate drive circuit. FAN7385 IC is used for driving each switch (one switch is 2 MOSFETs in anti-series).

5.1.4 Output Filter

The output filter of the cycloconverter is made up of an LC low pass filter. The dominant harmonics present will be near double the switching frequency. Alternately the corner frequency of filter (2.9 kHz) may be taken to be between 50 Hz and 50 kHz. The output filter consists of 3 mH and 1 μF. Fig. 5.3 shows the output inductor [indicated by (2)] and capacitor [indicated by (3)] used as filter.

5.1.5 Control Strategy

Texas Instrument DSP TMS320F28335 is the controller used for the implementation. All the four switches of FB are operated at 50% duty ratio. Leg 1 (S_1 & S_2) is taken with reference phase of 0 rad. The phase of Leg 2 (S_3 & S_4) is varied sinusoidally with respect to Leg 1. Phase shift variation is from 0 to π rad with step size increment of 0.0628 rad every switching cycle. Cycloconverter switches are switched at combined

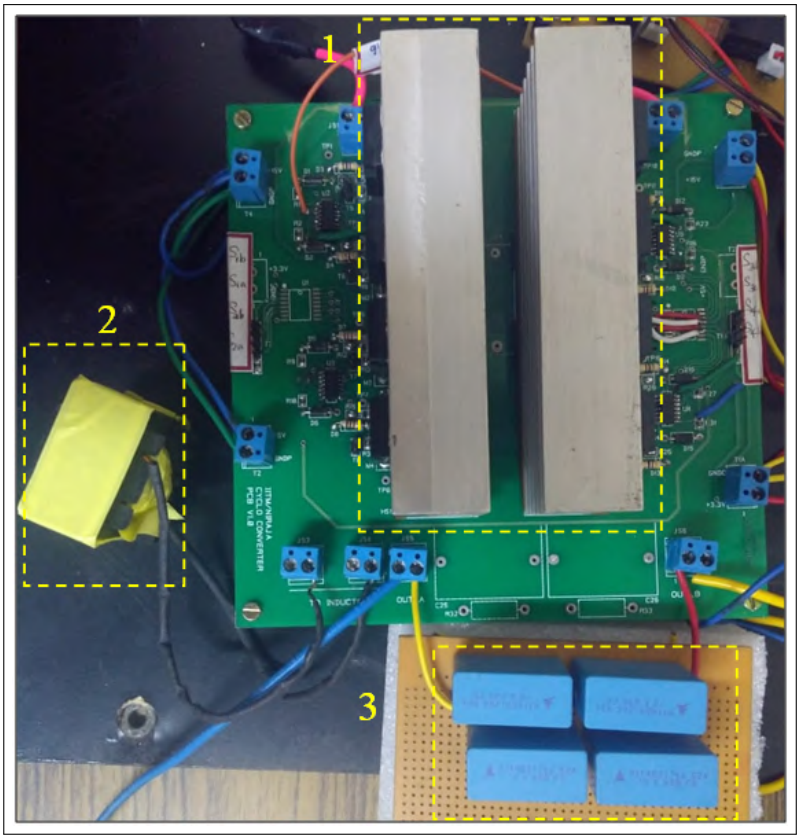


Figure 5.3: Hardware setup: Cycloconverter with output filter

line/high frequency as already discussed. The built-in ePWM modules are used to generate the 12 pulses to switches of FB and cycloconverter. Synchronisation of the gating pulses to FB converter and cycloconverter has to be done to ensure smooth commutation.

5.2 Simulation Results

A 500 W, 48 V DC/230 V AC RMS, single stage DC-AC converter was simulated in MATLAB Simulink. Relevant waveforms showing the characteristics of the converter are presented.

Fig. 5.4 shows the primary transformer current $i_p(t)$, transformer primary voltage $v_p(t)$, transformer secondary voltage $v_s(t)$, output of the cycloconverter $v_{cyclo}(t)$ and output voltage $v_o(t)$ for rated conditions. It is seen from the figure that HF transformer provides the required gain ($v_s(t)$), cycloconverter controls the frequency ($v_{cyclo}(t)$) and the LC filter gives the required AC output $v_o(t)$ as expected. Fig. 5.5 shows the output current

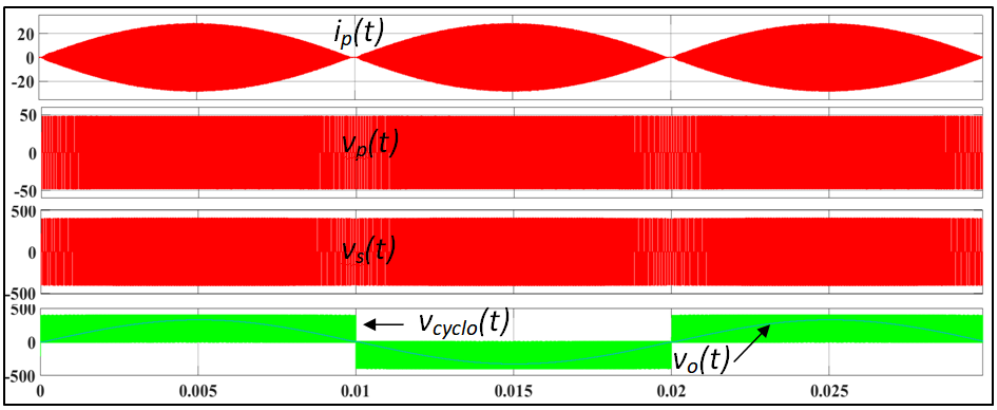


Figure 5.4: Simulation Results: Primary transformer current $i_p(t)$, transformer primary voltage $v_p(t)$, transformer secondary voltage $v_s(t)$, output of the cycloconverter $v_{cyclo}(t)$ and output voltage $v_o(t)$

$i_o(t)$, filter inductor current $i_L(t)$ and secondary transformer current $i_s(t)$. $i_s(t)$ has a high frequency variation and a sinusoidal variation at 100 Hz frequency, $i_L(t)$ contains the 50 Hz sinusoidal variation with switching ripple.

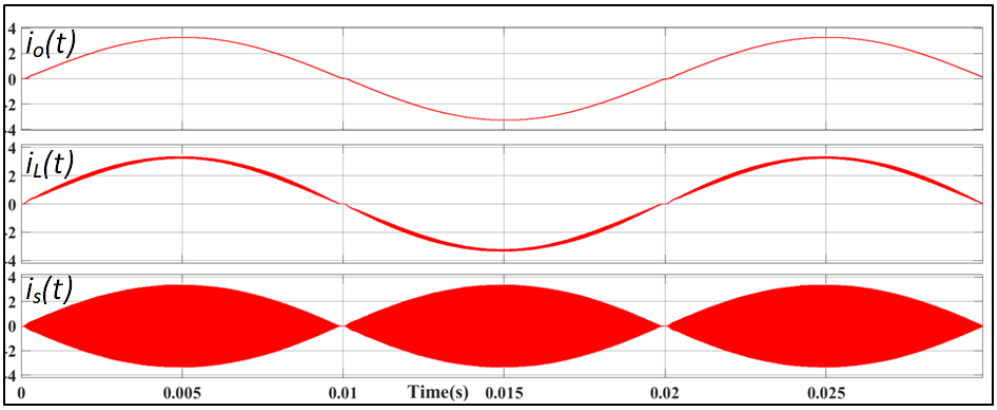


Figure 5.5: Simulation Results: Output current $i_o(t)$, inductor current $i_L(t)$, secondary transformer current $i_s(t)$.

Fig. 5.6 shows the current $i_{DS}(t)$ and voltage $v_{DS}(t)$ across the switches S_{1A}, S_{1B}. Current through the drain to source of the switch is considered as positive direction of current. Fig. 5.7 is an enlarged view of the same result. Since the switch S_{1A} is ON for the positive LFAC half cycle, the $v_{DS}(t)$ is zero. Therefore the switch S_{1B} has to block the full transformer secondary voltage that appears across it. It should be taken care of while selecting the switch.

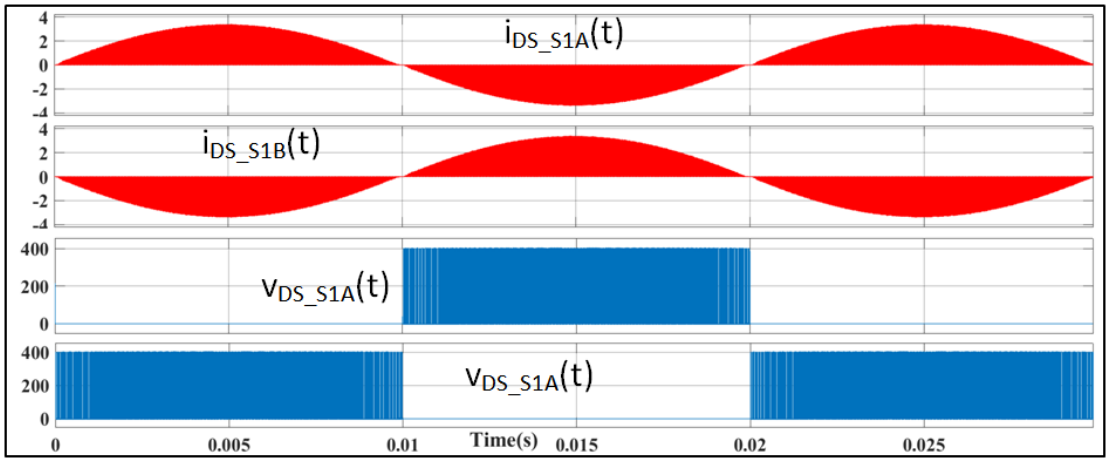


Figure 5.6: Simulation Results: Current $i_{DS}(t)$ and voltage $v_{DS}(t)$ across the switches S_{1A}, S_{1B}.

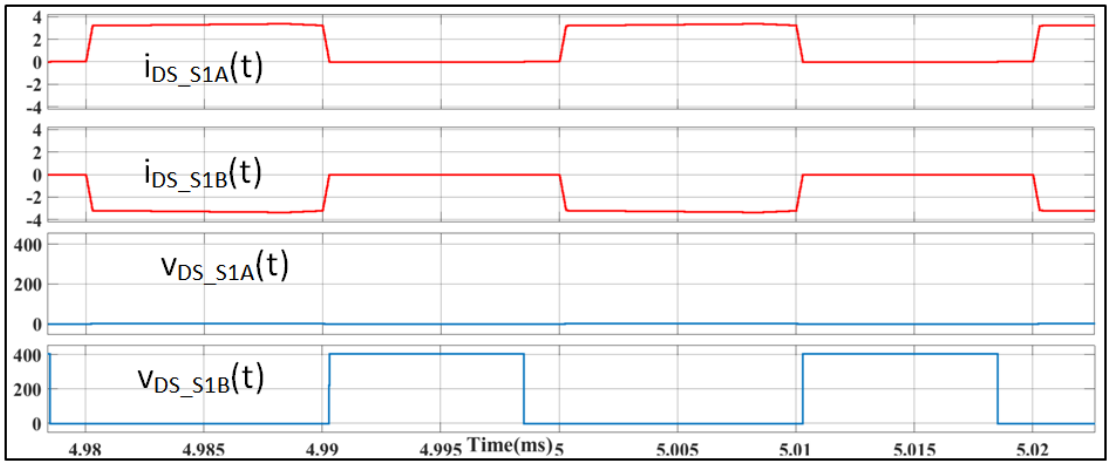


Figure 5.7: Simulation Results: Enlarged view

Fig. 5.8 shows the primary transformer current $i_p(t)$, transformer primary voltage $v_p(t)$, transformer secondary voltage $v_s(t)$. Due to the leakage inductance of the transformer, duty loss in the secondary voltage is observed as already discussed. Fig. 5.9 shows the switch currents of S_1, S_3 at maximum phase shift and Fig. 5.10 at a different instant. From these figures it is clear that, achieving ZVS is easy for S_3 due to higher energy available.

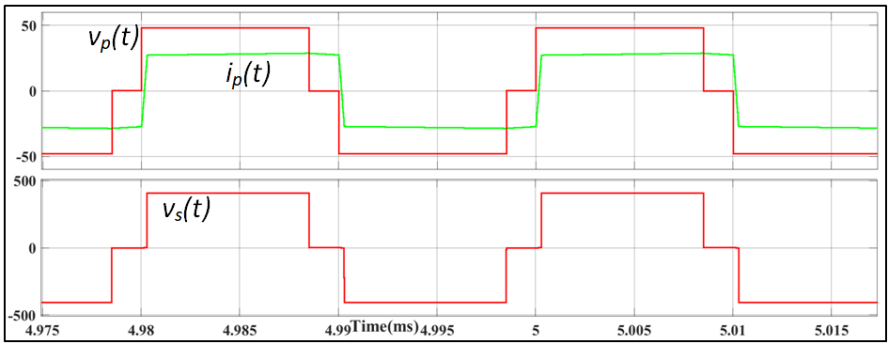


Figure 5.8: Simulation Results: Primary transformer current $i_p(t)$, transformer primary voltage $v_p(t)$, transformer secondary voltage $v_s(t)$

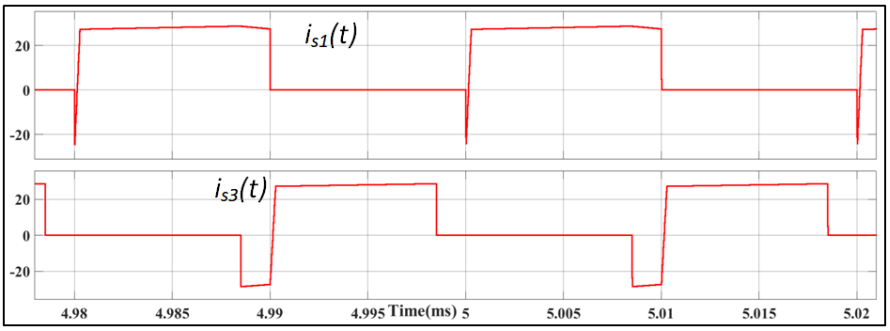


Figure 5.9: Simulation Results: Switch currents of S_1, S_3 at maximum phase shift

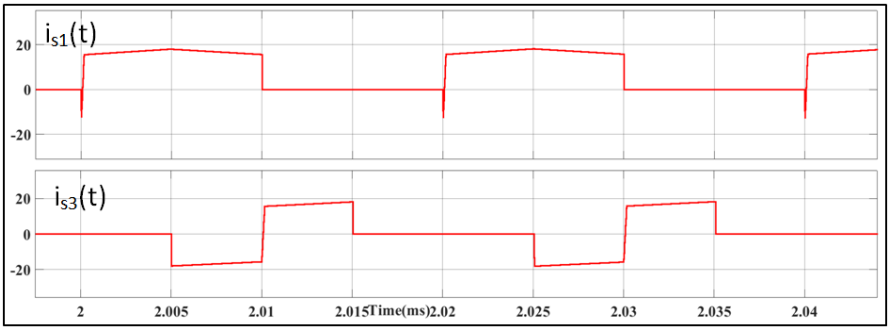


Figure 5.10: Simulation Results: Switch currents of S_1, S_3

Since the converter can supply only active power to the load, an additional capacitance is required to supply the reactive power when the load is inductive. The LC filter for resistive loads was designed for a cut-off frequency of 3 kHz (3 mH, 1 μF). Additional 19 μF was added to feed the RL load of 40 Ω, 40 mH. The output voltage and current waveform for the RL AC load of 40 Ω, 40 mH is shown in Fig. 5.11. Therefore we can conclude that filter requirement keeps changing according to the load. A common filter design cannot be arrived at for both R and RL loads.

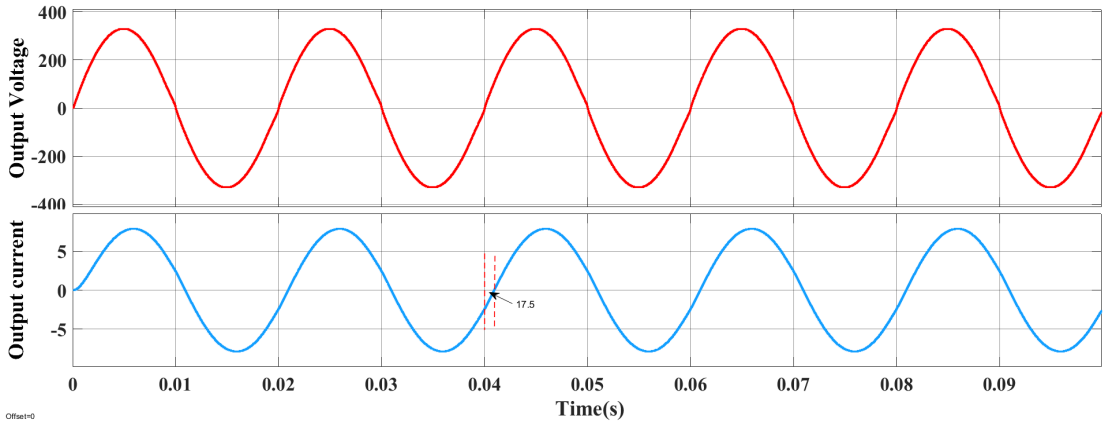


Figure 5.11: Simulation Results: Output voltage and current at RL (40 Ω ; 40 mH) load

5.3 Experimental Results

A prototype of a 500 W single stage DC-AC converter was built and tested in the lab as shown in Fig. 5.12 . The key control device used is TMS320F28335 DSP board.

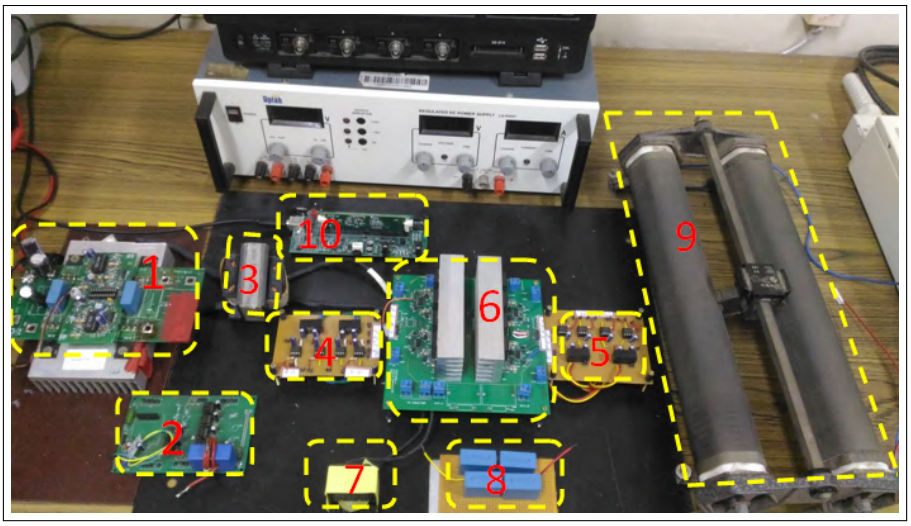
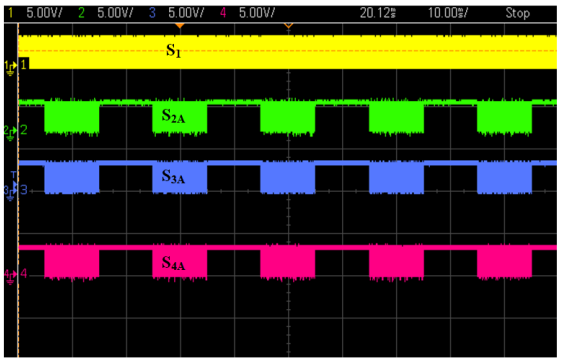
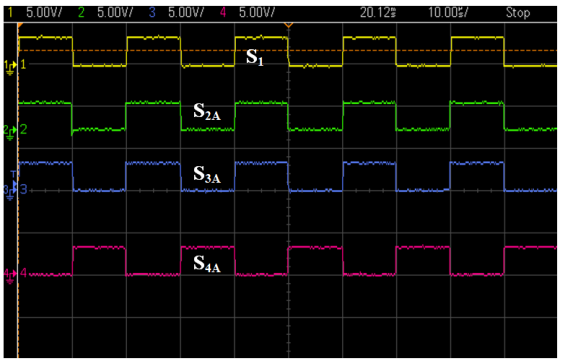


Figure 5.12: Hardware test setup. (1). DC side FB converter, (2). Isolator board for FB converter, (3). HF transformer, (4,5). Isolator boards for cycloconverter, (6). AC side cycloconverter, (7). Filter Inductor, (8). Filter capacitor, (9). Rheostat, (10). Controller Board

Fig. 5.13a shows the gating signals of $S_1, S_{2A}, S_{3A}, S_{4A}$ from DSP when cycloconverter is switched at combined line/high frequency as explained earlier. Fig. 5.13b shows an enlarged view of negative LFAC half cycle. It is clear that gate pulses of S_{2A}, S_{3A} is same as that of S_1.



(a) Gating signals. Scale: Gating signals from the DSP: 5V/div



(b) Enlarged view of gating signals. Scale: Gating signals from the DSP: 5V/div

Figure 5.13: Hardware results: Gating signals of $S_1, S_{2A}, S_{3A}, S_{4A}$

Figures 5.14, 5.15, 5.16 shows hardware results at the rated conditions. Results obtained validates the simulation results presented. Figures 5.17a-5.24b prove that the switching loss in all the cycloconverter switches are zero.

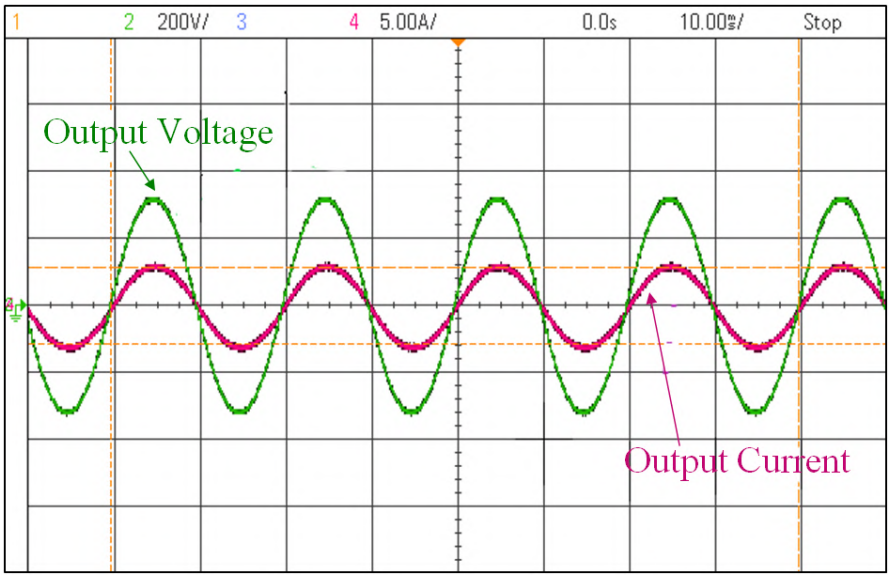


Figure 5.14: Hardware results: Output voltage and current waveform of the single stage DC-AC Converter, Scale:Output voltage:200V/div, Output current:5A/div

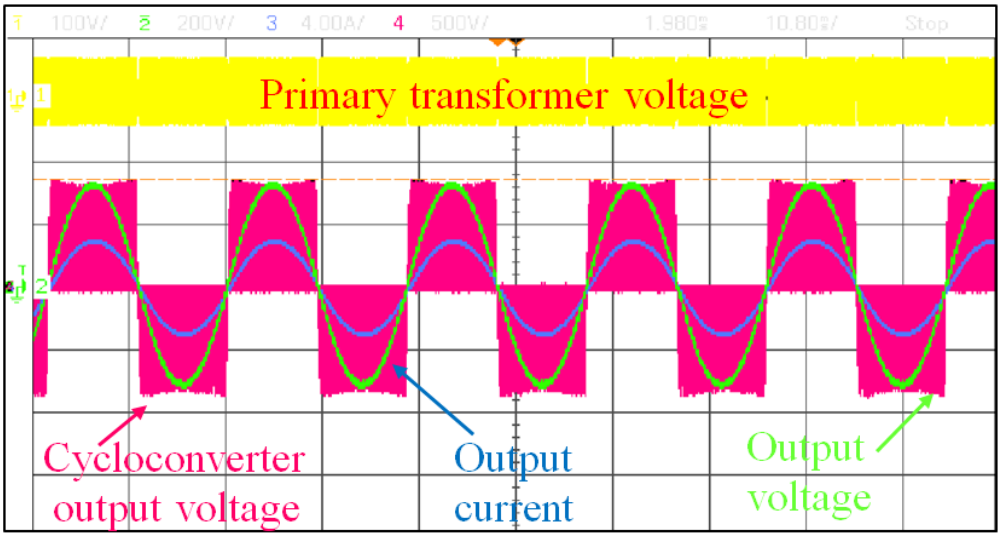


Figure 5.15: Hardware results: $v_p(t)$, $v_{cyclo}(t)$, $v_o(t)$, $i_o(t)$ waveforms of the converter for rated conditions, Scale:$v_p(t)$:100V/div, $v_{cyclo}(t)$:500V/div, $v_o(t)$:200V/div, $i_{o(t)}$:4A/div

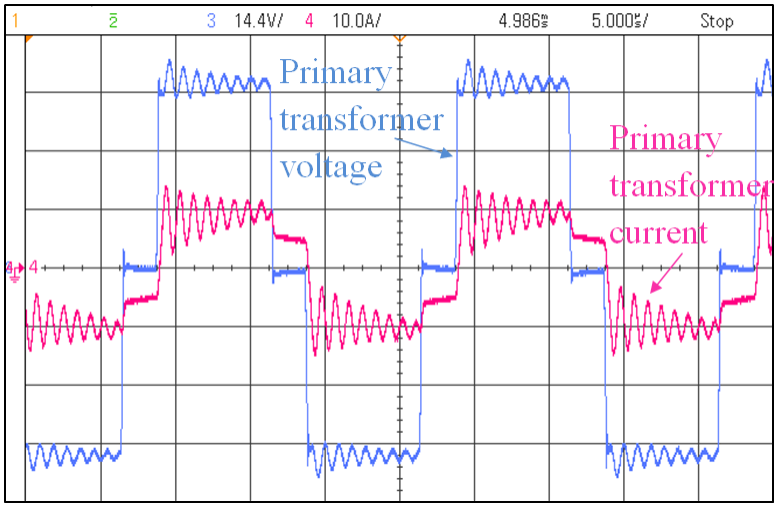
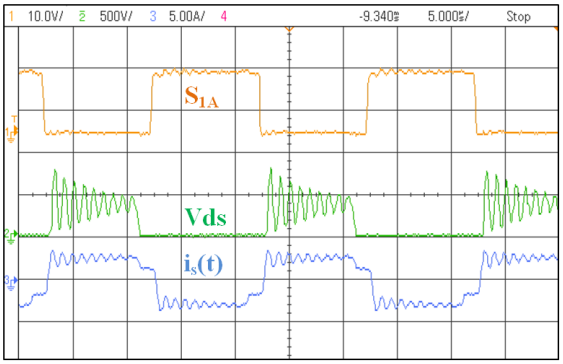
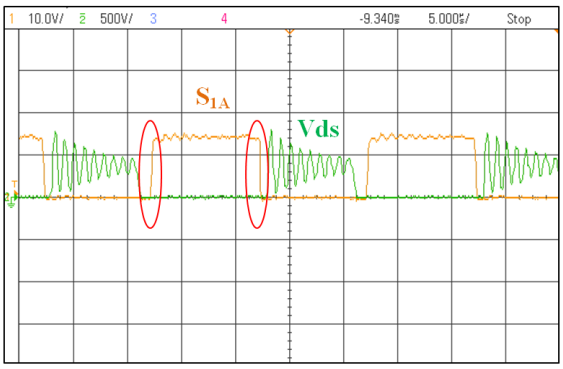


Figure 5.16: Hardware results: Primary transformer current and pole to pole voltage waveform, Scale:$v_p(t)$:14.4V/div, $i_p(t)$:10A/div

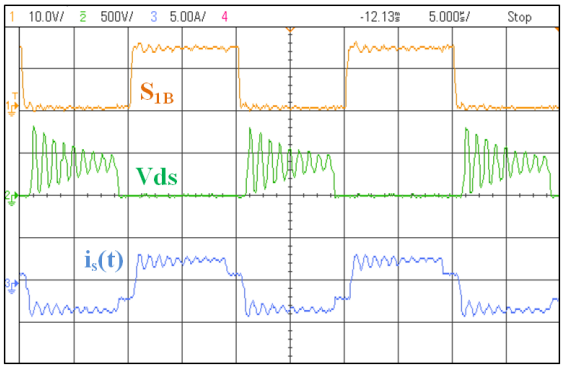


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

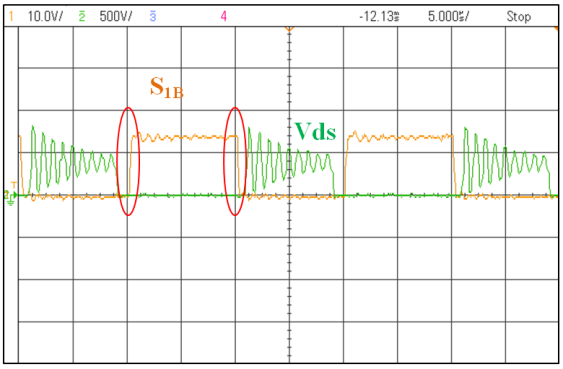


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.17: Hardware results: Switching transitions of S_{1A} in negative half cycle of output

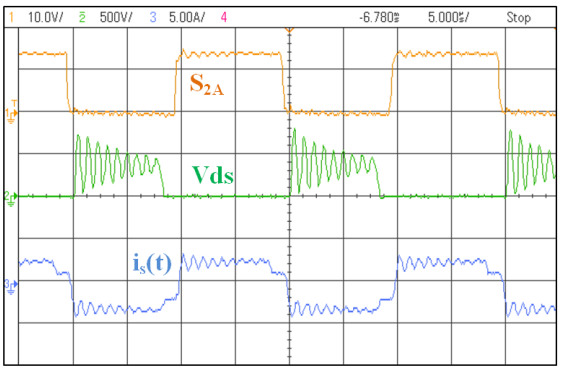


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

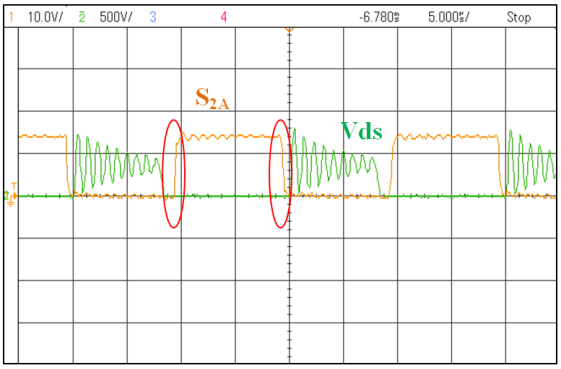


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.18: Hardware results: Switching transitions of S_{1B} in positive half cycle of output

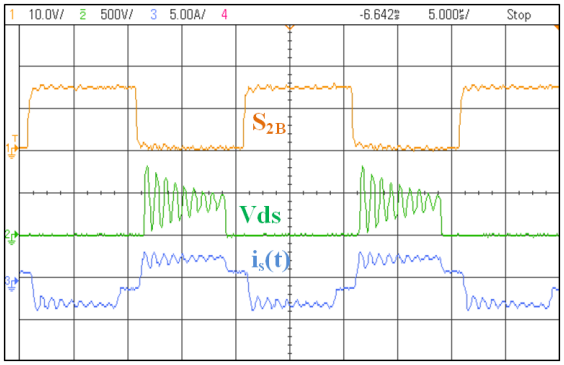


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

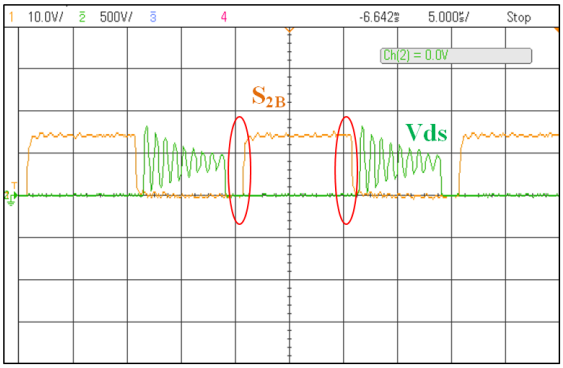


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.19: Hardware results: Switching transitions of S_{2A} in negative half cycle of output

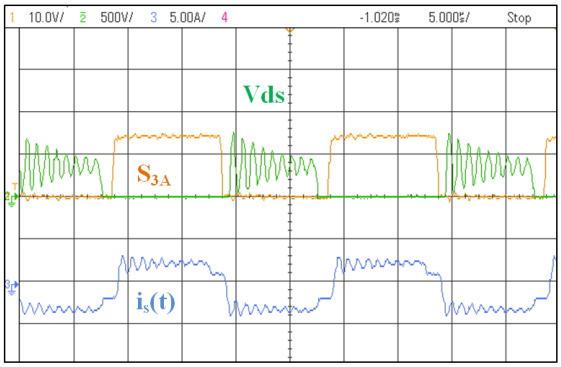


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

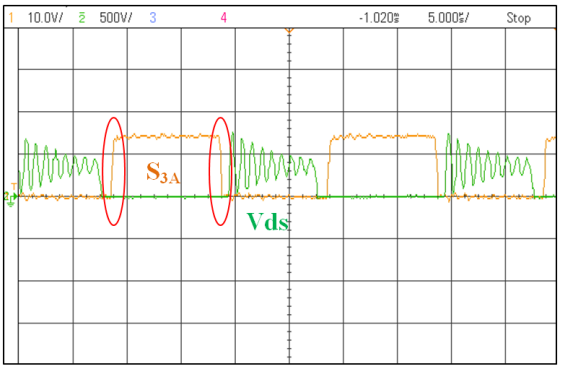


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.20: Hardware results: Switching transitions of S_{2B} in positive half cycle of output

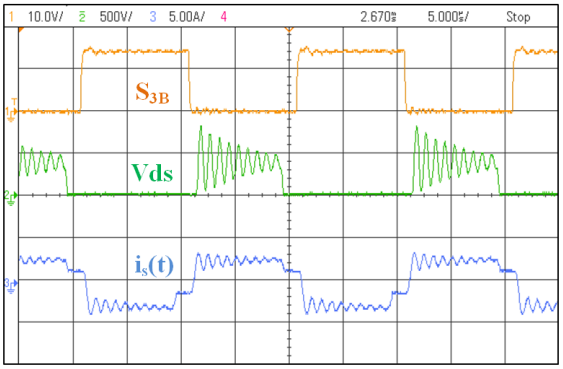


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

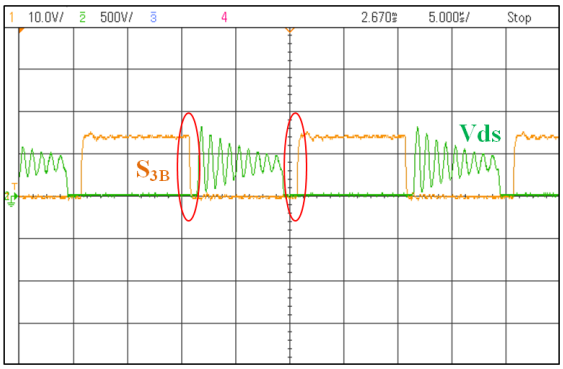


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.21: Hardware results: Switching transitions of S_{3A} in negative half cycle of output

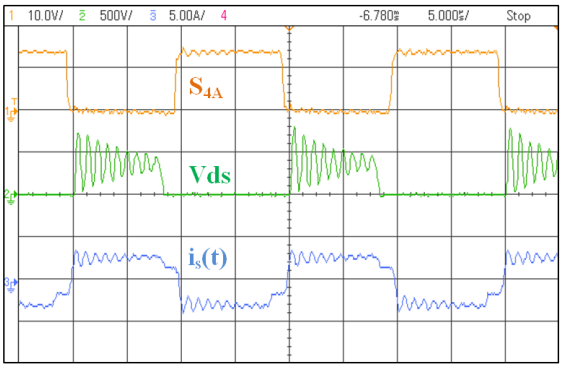


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

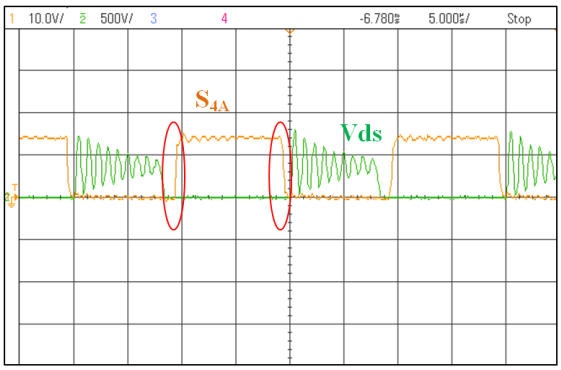


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.22: Hardware results: Switching transitions of S_{3B} in positive half cycle of output

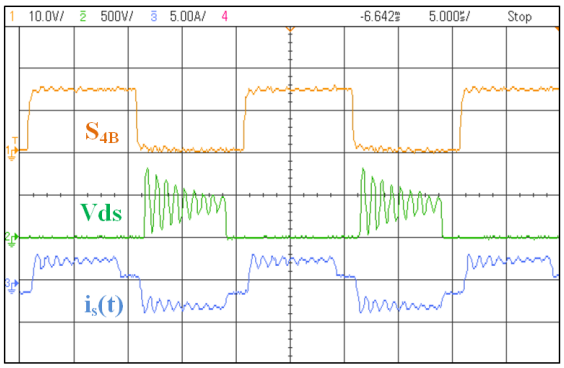


(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div

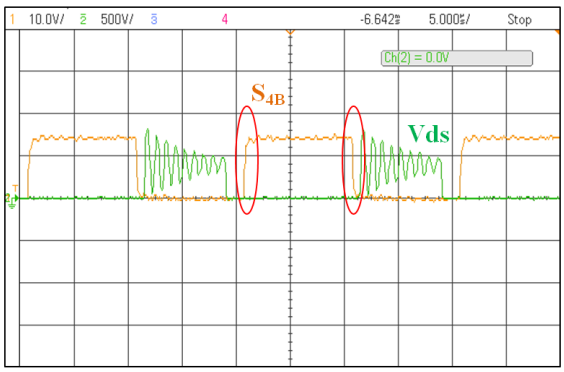


(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.23: Hardware results: Switching transitions of S_{4A} in negative half cycle of output



(a) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div, $i_s(t)$:5 A/div



(b) Scale: $v_{ds}(t)$: 500 V/div, $v_{gs}(t)$: 10 V/div

Figure 5.24: Hardware results: Switching transitions of S_{4B} in positive half cycle of output

CHAPTER 6

Solar PV fed Single stage DC-AC Converter

In this chapter modeling of a single stage DC-AC Converter connected to grid is discussed. The modeling and controller design is carried out in the rotating dq reference frame and is explained in the following sections.

6.1 Synchronous Rotating Frame

In single-phase systems, the transformation to dq0 is not immediate like three-phase systems, because they have only one phase variable while Park transform ($\alpha\beta - dq$) requires at least two orthogonal phase variables [18]. The advantage in synchronous rotating frame is that well-proven PI controllers can be used, as DC variables need to be controlled and an independent PQ control is achieved. A fictitious phase variable orthogonal to the real phase variable can be obtained by a T/4 transport delay or by Hilbert transform. Since the voltage vector rotates with an angular speed of w with respect to a stationary reference frame in the anti-clockwise direction, a synchronous dq reference frame which rotates with an angular speed of ω in the anti-clockwise direction is chosen. Here the synchronous reference frame is selected in such a way that grid voltage vector (V) is aligned along d-axis so that its component along q-axis is zero. This is achieved with the help of a phase locked loop (PLL). Since grid voltage space vector (V) and dq axis rotating at same speed ω as shown in Fig. 6.1, these are seemed to be stationary with respect to each other, thus grid voltage vector appears as a DC quantity in dq reference frame.

Therefore a voltage vector can be formed assuming the rotating frame is aligned with α axis,

$$V = (V_\alpha + jV_\beta)e^{-j\omega t} \tag{6.1}$$

where,

V represents the voltage vector,

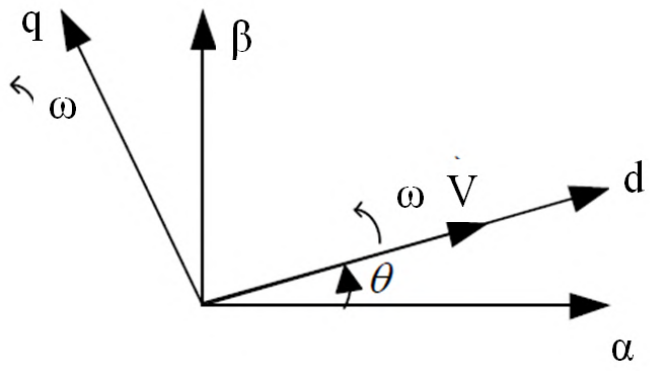


Figure 6.1: $\alpha\beta$ and dq frames representation

V_α is the actual single-phase voltage vector,

V_β is the fictitious phase voltage vector generated.

$$V = V_d + jV_q \tag{6.2}$$

Equating both the equations we get,

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} cos\omega t & sin\omega t \\ -sin\omega t & cos\omega t \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{6.3}$$

6.2 Mathematical Modelling of Grid-connected DC-AC converter

The converter is connected to the grid through an L filter (Fig. 6.2), KVL can be written in $\alpha\beta$ frame as

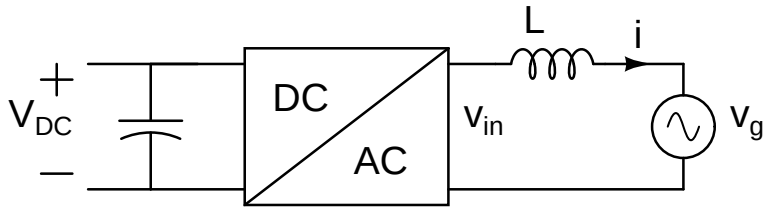


Figure 6.2: Grid connected converter with L filter

$$-v_{in_{\alpha\beta}}(t) + L\frac{di_{g\alpha\beta}(t)}{dt} + v_{g_{\alpha\beta}}(t) = 0 \tag{6.4}$$

Using the transformation in (6.3) we can convert (6.4) to dq frame. Rearranging the terms we get

$$L\frac{d}{dt}\begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} = \begin{bmatrix} 0 & \omega L \\ -\omega L & 0 \end{bmatrix} \begin{bmatrix} i_d(t) \\ i_q(t) \end{bmatrix} + \begin{bmatrix} V_{ind}(t) \\ V_{inq}(t) \end{bmatrix} - \begin{bmatrix} V_{gd}(t) \\ V_{gq}(t) \end{bmatrix} \tag{6.5}$$

From (6.5), we can see that in the dq frame, the d and q differential equations are dependent due to the cross-coupling terms $\omega L i_q(t)$ and $\omega L i_d(t)$.

6.3 Control strategy

The control block diagram for the solar PV fed single stage DC-AC converter is shown in Fig. 6.3 [19]. The objectives of the control is to control the real power flow from PV to the grid along with maintaining DC bus voltage at a V_{mpp} given by the MPPT algorithm. MPPT is the algorithm adopted to extract the maximum power from the renewable source.

In Fig. 6.3, V_{dc} and V_{dc}^* are the actual and reference DC bus voltage respectively, i_d and i_q are the d and q-axis component of the line current vector in the dq reference frame, i_d^* and i_q^* are the reference for d and q-axis component of the line current vector in the dq reference frame, V_{gd} and V_{gq} are d and q-axis component of the grid voltage vector in the dq reference frame.

Reference DC voltage is given by MPPT algorithm. In literature, there are several MPPT algorithms like the perturb and observe (P&O) methods, incremental conductance methods, hill climbing algorithm, short circuit current control, open circuit voltage control [20],[21],[22],[23]. In this project P & O is used. Flow chart of the algorithm is shown below. Once the reference DC voltage is obtained from the MPPT, it can be regulated using a PI controller, which takes the difference between actual DC bus voltage and reference DC value as the input. The output of the DC bus voltage controller will be the reference for i_{d1}^* controller. i_d controller controls the real power flow from the grid, since i_d is a measure of real power (P) as shown in (6.6). i_d^* contains i_{d1}^* to regulate the DC volatge and i_{d2}^* as a feedforward term as shown in Fig. 6.3. Reactive

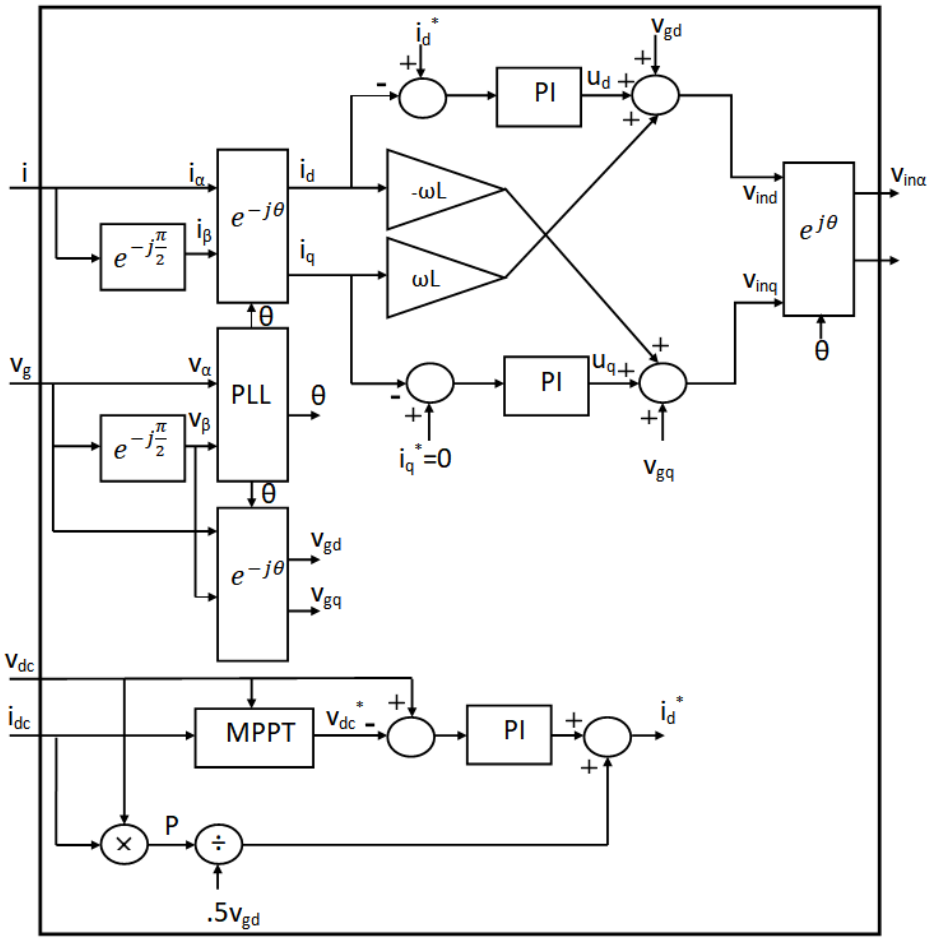


Figure 6.3: Synchronous PI dq current control of grid connected DC-AC converter

power Q^* is set to zero.

$$P = \frac{1}{2}(v_d i_d + v_q i_q) \tag{6.6}$$

$$Q = \frac{1}{2}(v_q i_d - v_d i_q) \tag{6.7}$$

Therefore, if we make v_q as zero we can control P and Q independently using i_d and i_q respectively.

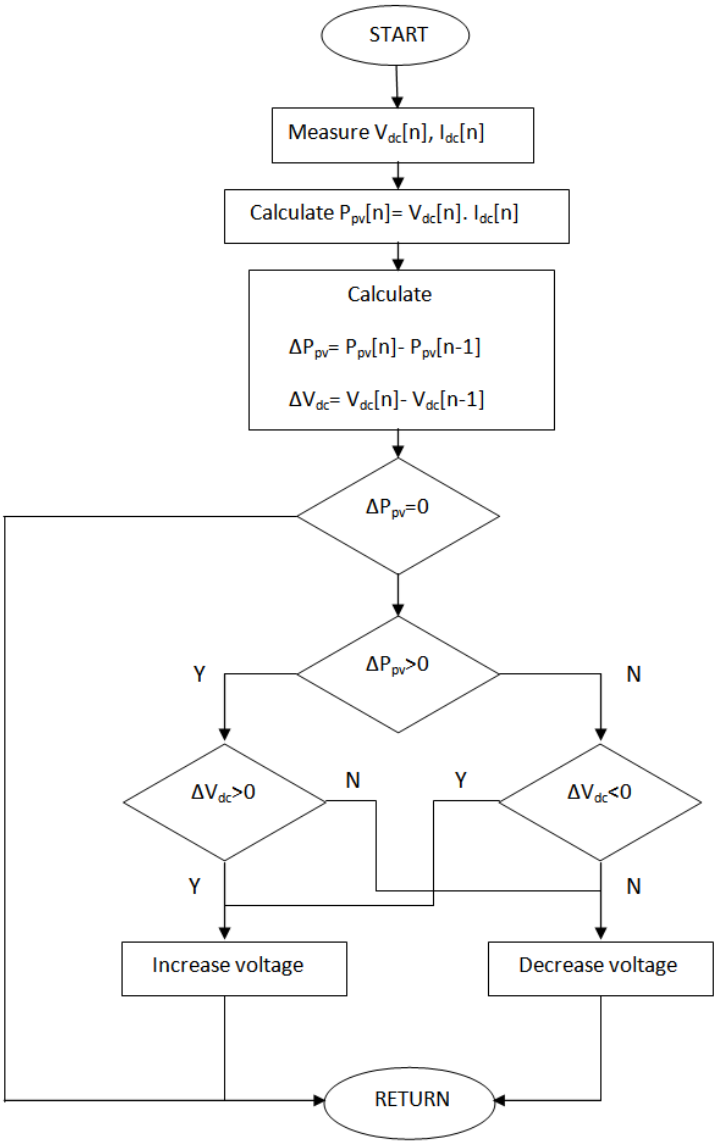


Figure 6.4: MPPT algorithm

6.3.1 Current controllers

We have already obtained the mathematical model of the DC-AC converter connected to grid in (6.5). Thus, we get the equations,

$$L\frac{di_d(t)}{dt} = \omega L i_q(t) + v_{ind}(t) - v_{gd}(t) \tag{6.8}$$

$$L\frac{di_q(t)}{dt} = -\omega L i_d(t) + v_{inq}(t) - v_{gq}(t) \tag{6.9}$$

Assuming new control variables u_d, u_q as

$$L\frac{di_d(t)}{dt} = u_d(t) \tag{6.10}$$

$$L\frac{di_q(t)}{dt} = u_q(t) \tag{6.11}$$

Taking Laplace transform, we get the plant transfer function for the current controllers as,

$$\frac{i_d(s)}{u_d(s)} = \frac{1}{sL} \tag{6.12}$$

$$\frac{i_q(s)}{u_q(s)} = \frac{1}{sL} \tag{6.13}$$

The derived controller block diagrams for both i_d and i_q controllers are shown in figures 6.5 and 6.6 respectively.

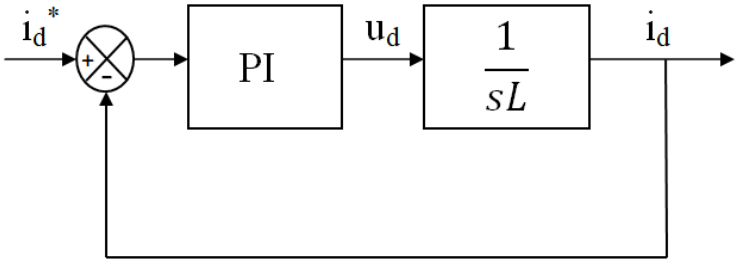


Figure 6.5: Block diagram for i_d controller

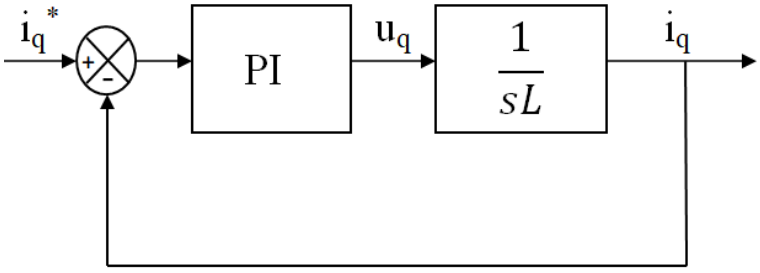


Figure 6.6: Block diagram for i_q controller

Substituting (6.10), (6.11) in (6.8), (6.9) and rearranging the terms, we obtain

$$v_{ind}(t) = u_d(t) + v_{gd}(t) - \omega L i_q(t) \tag{6.14}$$

$$v_{inq}(t) = u_q(t) + v_{gq}(t) + \omega L i_d(t) \tag{6.15}$$

Converting $v_{ind}(t)$, $v_{inq}(t)$ back to $\alpha\beta$ frame, we obtain $v_{in\alpha}(t)$ that is selected as the reference signal which has to be scaled to get the modulating signal.

6.3.2 DC Voltage Controller

Solar PV power is a non-linear function of DC-link voltage, temperature and irradiation levels. The real power from the PV system and DC-link voltage can be controlled by current i_d. Considering only real power from the PV array and the PV system, the dq frame based power balance equation is

$$P_{out} = P_{pv} - P_{DC-link} \tag{6.16}$$

$$\frac{1}{2} v_{gd} i_d = P_{pv} - V_{DC} C \frac{dv_{DC}}{dt} \tag{6.17}$$

Assumption of $i_d \approx i_d^*$ [24] is made since the time constant of the current controller is very small. Assuming

$$i_d^* = i_{d1} + r \frac{P_{pv}}{\frac{1}{2} v_{gd}} \tag{6.18}$$

where i_{d1} is a control variable, r can be 0 or 1 depending on whether feed-forward control is used or not.

Substituting (6.18) in (6.17) we get,

$$\frac{1}{2} v_{gd} i_{d1} = (1 - r) P_{pv} - V_{DC} C \frac{dv_{DC}}{dt} \tag{6.19}$$

Therefore if feed-forward control is used, that is $r = 1$, then,

$$\frac{1}{2} v_{gd} i_{d1} = -V_{DC} C \frac{dv_{DC}}{dt} \tag{6.20}$$

Therefore current controller can be designed without affecting the PV power. From (6.20), when the DC bus voltage raise, the positive difference between the DC bus

voltage and the reference DC bus voltage is used by a PI regulator to generate the reference Id current. In this case the reference i_{d1}^{*} current is increased to raise the active power flow injected into the grid. Differently, the DC bus voltage decrease, the negative difference between the DC bus voltage and the reference DC bus voltage is computed by PI to decrease the reference i_{d1}^{*} component and then the active power injected into the grid.

6.4 Simulation Results

Simulation of the grid connected solar PV fed single stage DC-AC converter is done in MATLAB/Simulink. Solar cell characteristics change with temperature and irradiance. PV array block available in MATLAB/Simulink was used to define a user-defined PV array. Details of the PV block are given in Table. 6.1. Two such PV modules are connected in parallel in the simulation. Figures 6.7, 6.8 show the PV array characteristics varyiations with irrandiance and temperature.

Table 6.1: Block Parameters of 1 PV module in MATLAB/Simulink

Characteristics of 1 PV module	
V_{mpp} (V)	48
V_{oc} (V)	60
I_{mpp} (A)	15
I_{sc} (A)	20
Temperature coefficient of Voc (% deg.C)	-0.229
Temperature coefficient of Isc (% deg.C)	0.030706

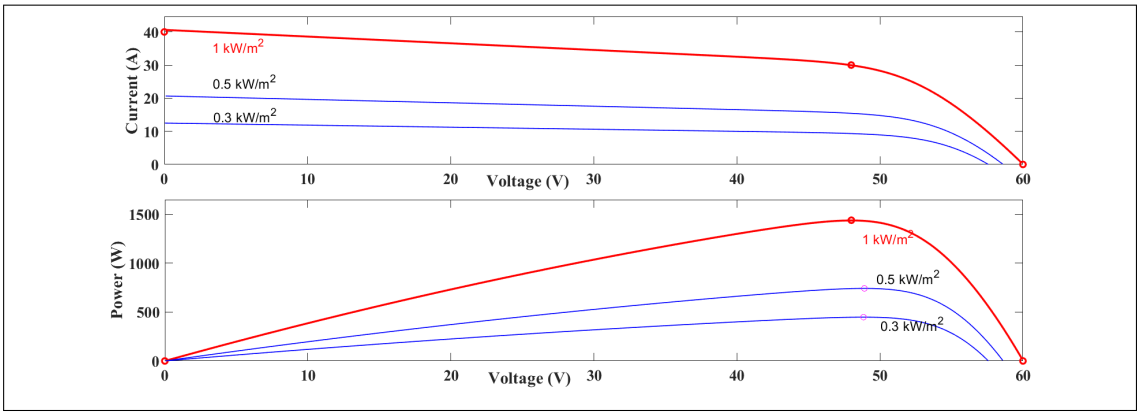


Figure 6.7: $P\ v/s\ V$ and $I\ v/s\ V$ curve at 25^0C and specified irradiances

From Fig. 6.7, maximum power point of the PV array is around 1.44 kW. The maximum power operating point is close to the knee area in the I-V curve. The maximum

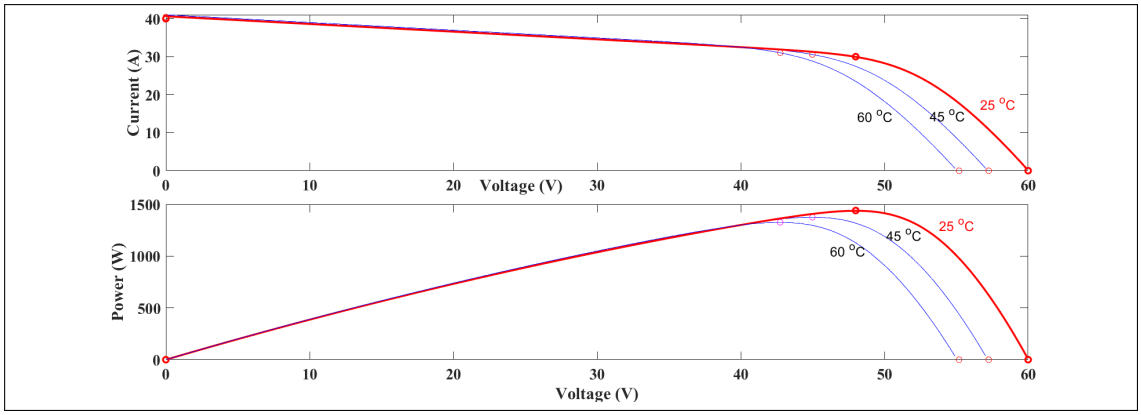


Figure 6.8: $P\ v/s\ V$ and $I\ v/s\ V$ curve at 1000 W/m^2 and specified temperatures

power output (MPP) from the PV module is not constant and changes with irradiance and temperature. The control system must therefore track the MPP continuously in order to ensure that the module always provides maximum power. MPPT algorithm used in this simulation is conventional P & O where the step size is constant. More accurate and faster response can be obtained by using other MPPT algorithms where the step size is changed according to different zones (MPP zone, NON-MPP zone)[] of operation.

Another parameter to be taken care of is the selection of DC-link capacitor. The value of the DC-link capacitor selected should be high enough to limit the voltage fluctuations in the input side. A capacitor of $80\ mF$ is used in the simulation. The DC voltage should be kept close to the MPP voltage to extract maximum power from PV. This is done by controlling the i^*_{d1} thereby controlling the output power.

Results at constant irradiance and temperature

The grid connected solar PV fed converter was examined initially with a constant irradiance of 1000 w/m^2 and constant temperature of 25^0C. The results for the same are shown.

The control is done in dq reference frame. Fig. shows the $v_\alpha(t)$, $v_\beta(t)$,$v_d(t)$, $v_q(t)$. $v_\beta(t)$ is obtained from $v_\alpha(t)$ by using the Hilbert transfer function shown in (6.21).

$$H(s) = \frac{1 - \dfrac{s}{w_c}}{1 + \dfrac{s}{w_c}} \tag{6.21}$$

where w_c = 314 rad/s.

Angle obtained from the output of PLL is used for the transformation of $\alpha\beta$ to dq frame. Output of the PLL is given in Fig. . Simulink PLL block is used in the simulation.

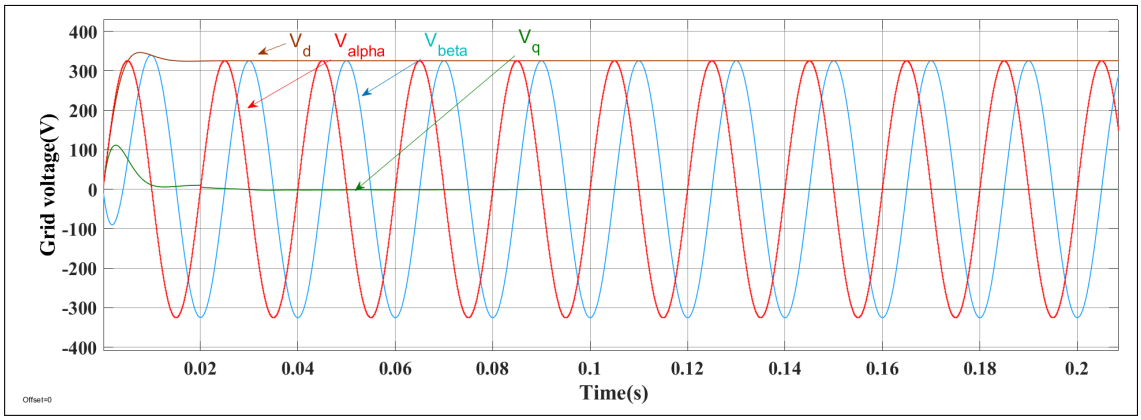


Figure 6.9: $\alpha\beta$ to dq transformations

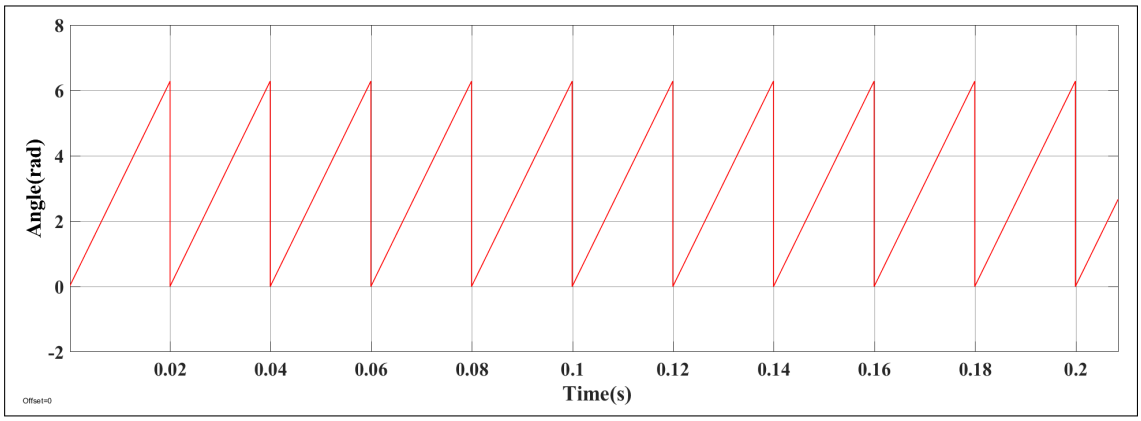


Figure 6.10: Simulation Results: Response of PLL

Fig. 6.11 shows the output voltage and current waveforms. It is evident that they are in phase with each other thus ensuring unity power factor. The PV system output should have low current-distortion levels to insure that no adverse effects are caused to other equipment connected to the utility system. The levels given in Fig. 6.12 are accepted. In addition, the allowable amount of injected DC current into the grid are rather small inorder to avoid saturation of the distribution transformers. According to standards IEEE 1574 and IEC 61727 DC current injection levels should be less than 0.5% and 1% of the output RMS current respectively. From the FFT shown in Fig. 6.13 we can see that THD is 2.85% which is well within the limits. Third harmonic component of 2.63% of fundamental is observed, which is permissible. Rest of the harmonic components are less than 0.2%. DC current is 0.05% of fundamental.

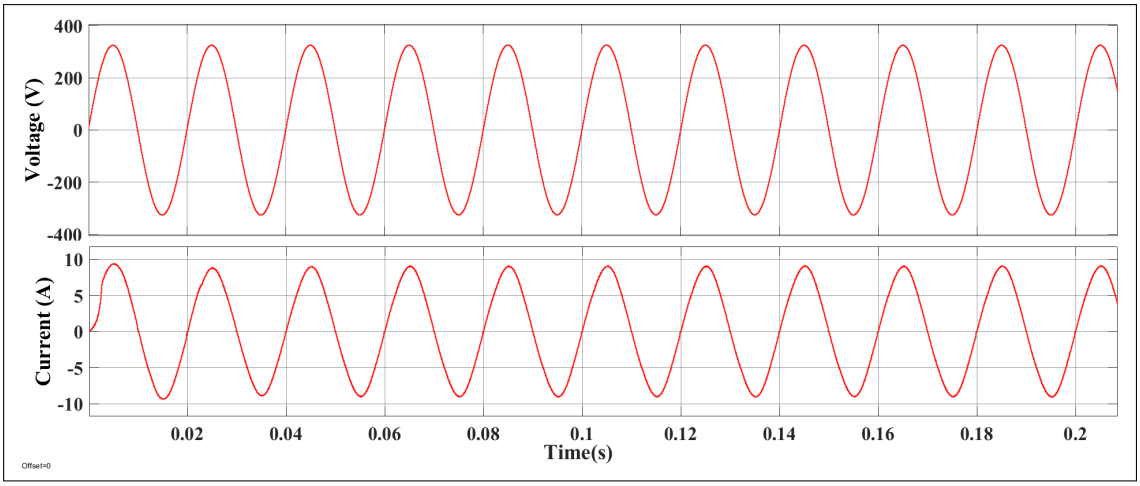


Figure 6.11: Simulation Results: Grid voltage and current

IEEE 1547 and IEC 61727						
Individual harmonic order (odd)[a] (%)	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	Total harmonic distortion THD (%)
	4.0	2.0	1.5	0.6	0.3	5.0

[a]Even harmonics are limited to 25 % of the odd harmonic limits above.

Figure 6.12: Simulation Results: Maximum current harmonics

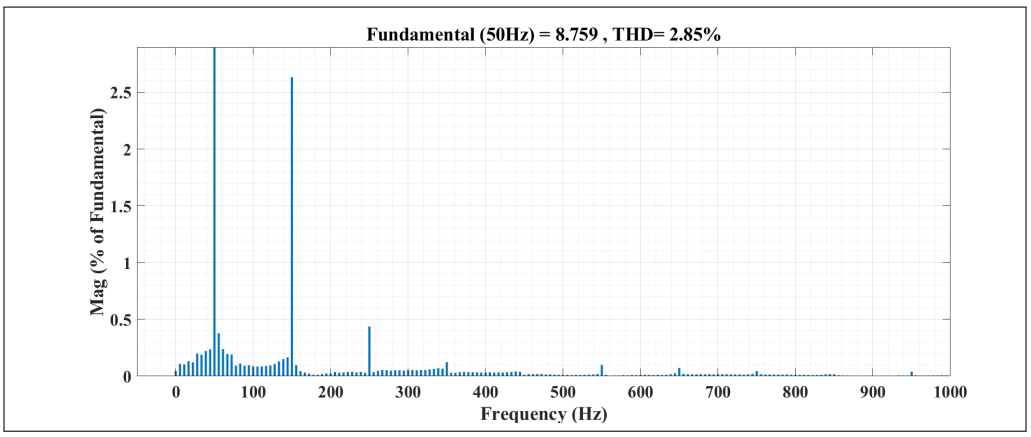


Figure 6.13: Simulation Results: FFT analysis of grid current

Fig. 6.14 shows the PV voltage, current and power. It is observed that the DC voltage is maintained very close to 48 V, which is the V_{mpp}. Thus maximum power is being delivered by the PV source. PV power is maintained at the MPP region close to $1.44\ kW$.

Fig. 6.15 shows the instantaneous AC output power supplied to grid and its average taken over 100 Hz is shown. It is seen that at steady state the average power is close to 1.425 kW, thus transferring maximum power from PV to grid.

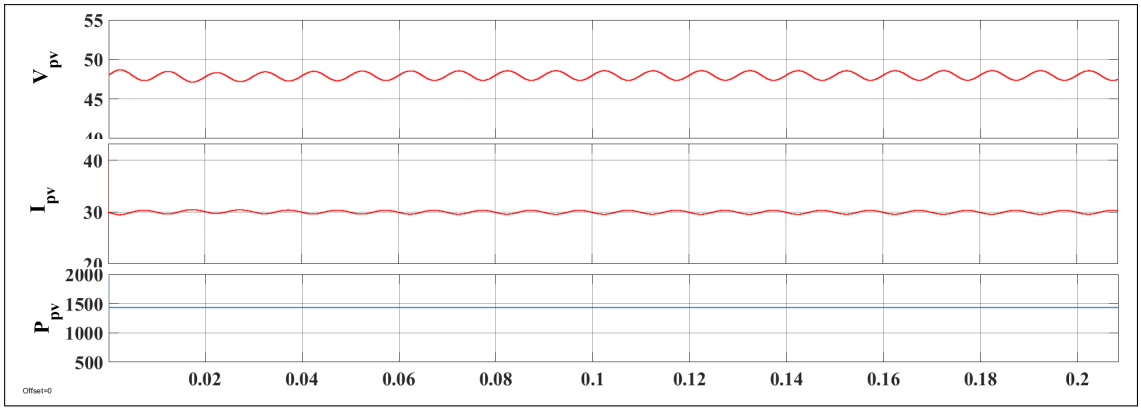


Figure 6.14: Simulation Results: PV voltage, current and power

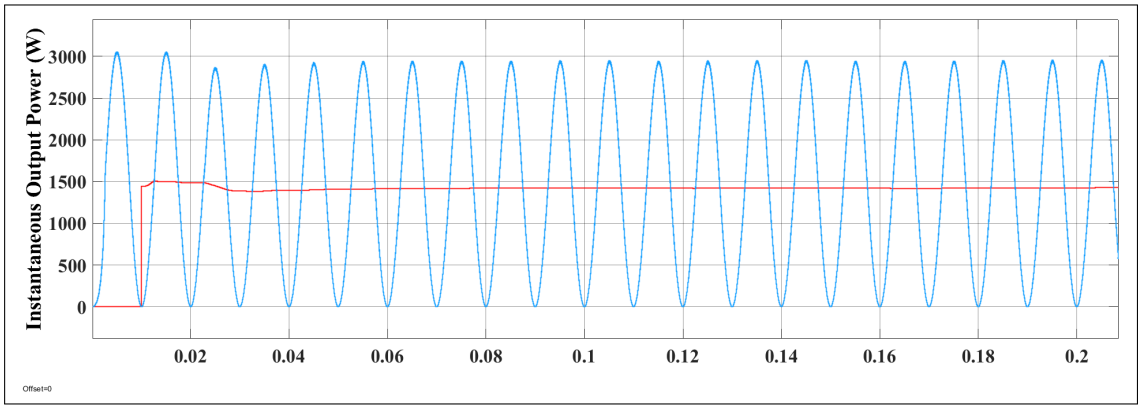


Figure 6.15: Simulation Results: Instantaneous output power

Results at constant temperature and ramp change in irradiance

Waveform given in Fig. 6.16 is used to test the performance of the system. Initially, irradiation level (I_r) is kept at 1000 W/m^2 and at $t = 0.15s$, the irradiation level is ramped down to 300W/m2 level with a specific negative slope. During the dwell time of 0.2s I_r is kept constant at 300 W/m^2, and afterwards, it is ramped up to 1000 W/m^2 with a constant positive slope and kept at 1000 W/m^2 constant as shown in Fig. 6.16.

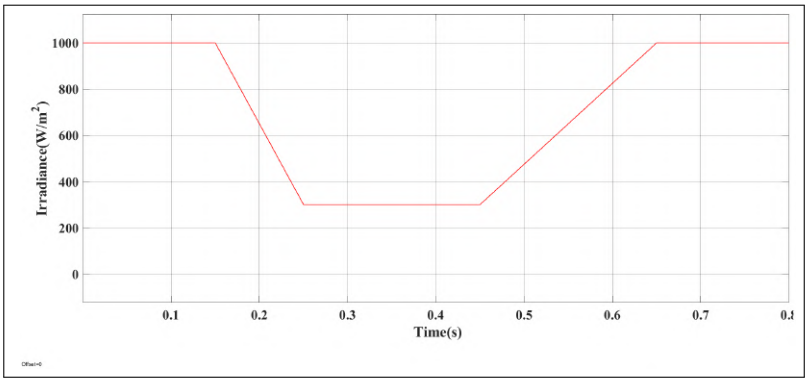


Figure 6.16: Simulation Results: Waveform for ramp change in irradiance

Fig. 6.17 shows the grid voltage and currents for the irradiance change. The grid currents are in phase with grid voltages satisfying the unity power factor operation. Also the grid currents track their reference currents with great success thus keeping the PV voltage at V_{mpp}.

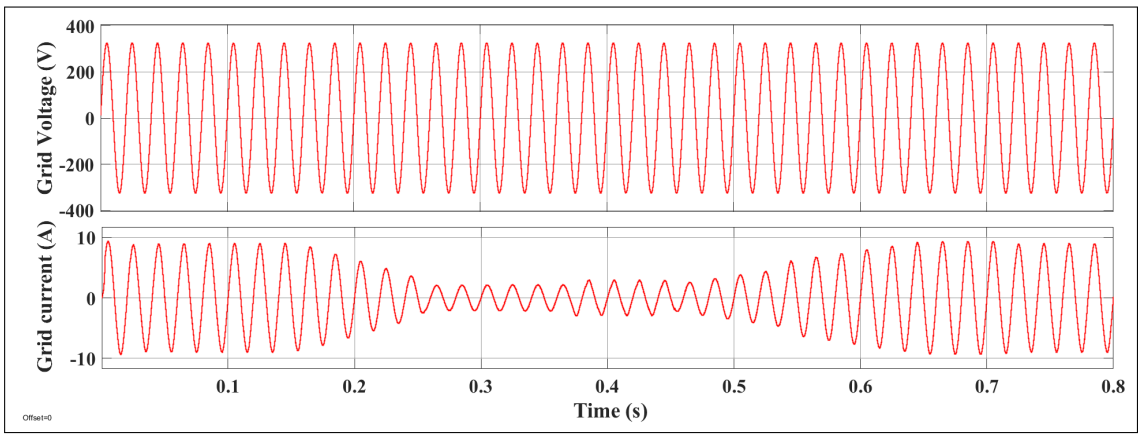


Figure 6.17: Simulation Results: Grid voltage and current

Fig. 6.18 shows the PV voltage, current and power. It is observed that the PV voltage is maintained at 48 V, i.e, V_{mpp} during the initial settling time when constant irradiance of 1000 W/m^2. When there is a ramp change in the irradiance from 1000 W/m^2 to 300 W/m^2, the PV voltage closely tracks the V_{mpp} and settles at 48.8 V, i.e, V_{mpp} at 300 W/m^2. It takes almost 0.1 s to settle. After the irradiance change back from 300 W/m^2 to 1000 W/m^2, PV voltage settles back at 48V.

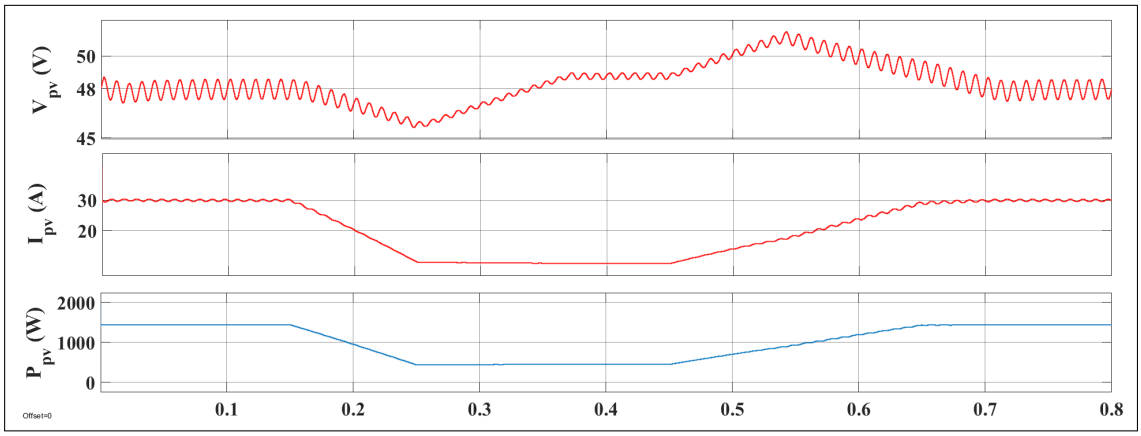


Figure 6.18: Simulation Results: PV voltage, current and power

Fig. 6.19 shows the instantaneous AC output power supplied to grid and its average taken over 100 Hz is shown. It is seen that at steady state, the average power is close to maximum power available at each the irradiance level.

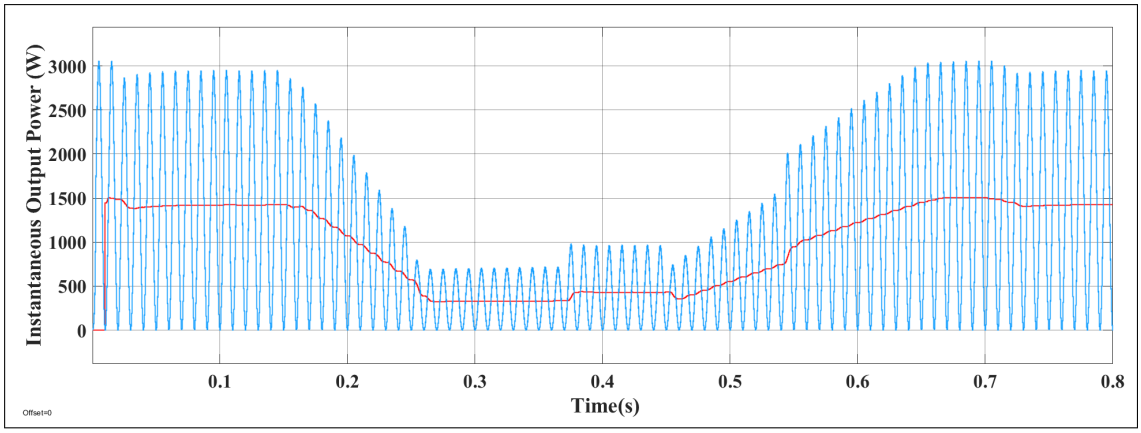


Figure 6.19: Simulation Results: Instantaneous output power

Results at constant temperature and steep change in irradiance

Waveform in Fig. 6.20 is used to test the performance of the system. Initially, irradiation level (Ir) is kept at 1000 W/m^2 and at $t = 0.11s$, a step change is applied and it is reduced from 1000 W/m^2 to 500 W/m^2 as shown in Fig. 6.20.

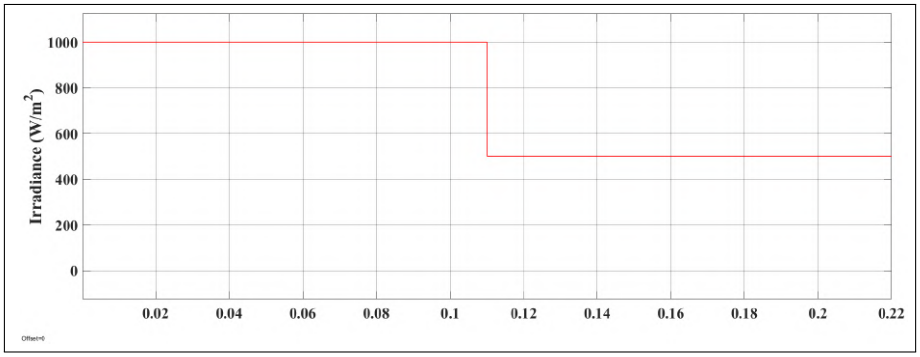


Figure 6.20: Simulation Results: Waveform for steep change in irradiance

Fig. 6.17 shows the grid voltage and currents for the irradiance change. The grid currents are in phase with grid voltages satisfying the unity power factor operation.

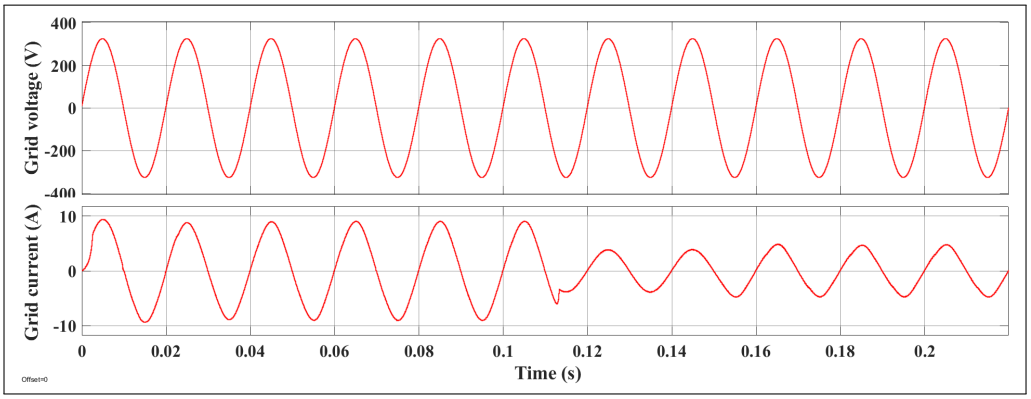


Figure 6.21: Simulation Results: Grid voltage and current

Although there is a distortion in the grid current when there is sudden dip in the irradiance, they track their reference currents thus keeping the PV voltage at V_{mpp}.

Fig. 6.22 shows the PV voltage, current and power. It is observed that the PV voltage is maintained at 48 V, i.e, V_{mpp} during the initial settling time when constant irradiance of 1000 W/m^2. When there is a steep change in the irradiance from 1000 W/m^2 to 500 W/m^2, the PV voltage closely tracks the V_{mpp} and settles at 48.9 V, i.e, V_{mpp} at 500 W/m^2. It takes almost 0.05 s to settle.

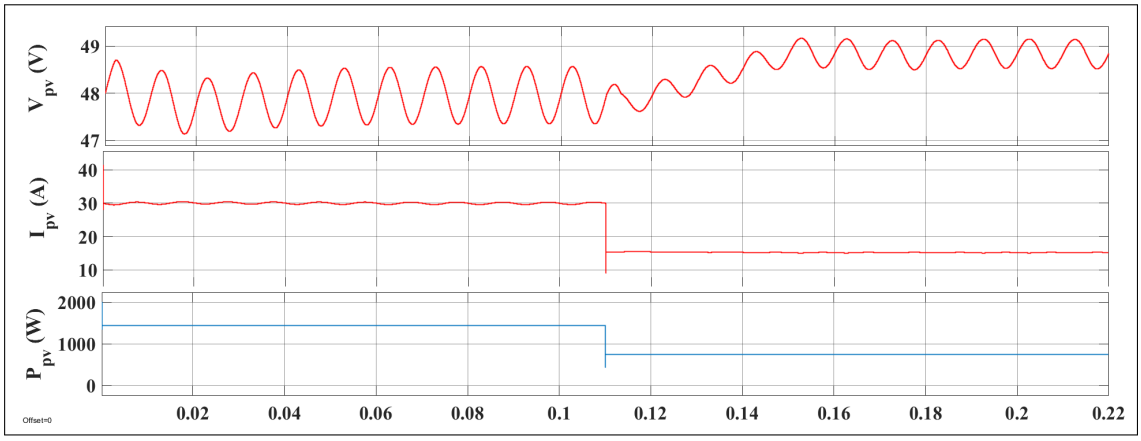


Figure 6.22: Simulation Results: PV voltage, current and power

Fig. 6.23 shows the instantaneous AC output power supplied to grid and its average taken over 100 Hz is shown. It is seen that at steady state, the average power is close to maximum power available at each the irradiance level. The initial dip in power is because power was used to regulate the voltage at V_{mpp}. Once it reached steady state, we can see that power close to maximum power is fed to grid (725 W).

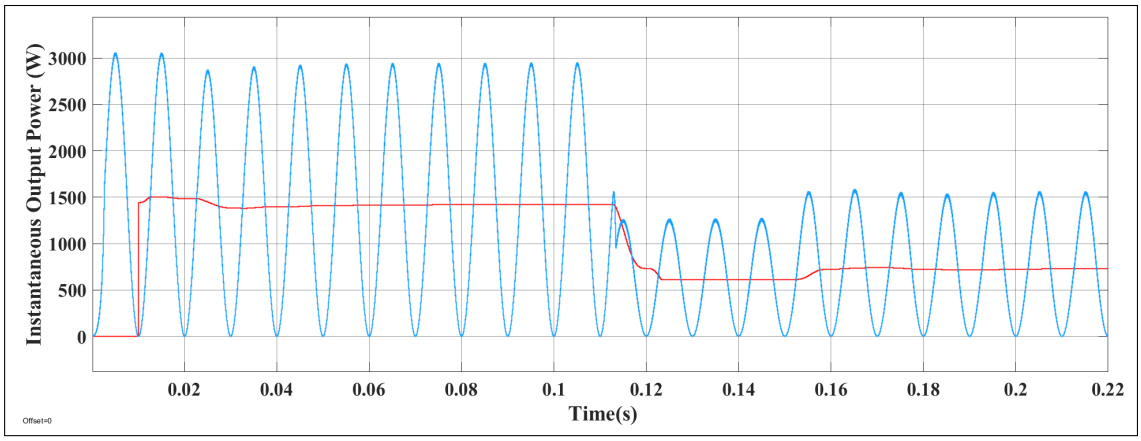


Figure 6.23: Simulation Results: Instantaneous output power

CHAPTER 7

Conclusion

7.1 Summary of Present Work

The main objective of this project was to develop a single stage DC-AC converter for solar PV fed applications. The single stage DC-AC converter consists of a sinusoidal phase shifted FB converter and a cycloconverter. Different control schemes for cycloconverter when FB converter is sinusoidally phase modulated are discussed in detail. Operating modes of the single stage DC-AC converter with sinusoidal phase modulated FB converter and combined line/high frequency switching of cycloconverter is described to prove that swicthing loss in cycloconverter is nil. Therefore, it is concluded that the combined line/high frequency switching in cycloconverter is efficient than line frequency switching. Combined line/high frequency switching has the advantages of no switching loss and lesser complexity. Simulation and experimental results are presented to validate the same. Mathematical model for the grid connected converter is developed in dq frame and controller design is done for the same. Simulation for solar PV fed single stage DC-AC converter when connected to grid is done and the results are presented. Obtained results for different input test waveforms show that the system offers very fast response and good accuracy for all operating conditions. In addition, the grid currents injected to the grid are sinusoidal with low distortion level.

7.2 Future Scope

With increasing demand for the renewable energy sources, efficient power converters are required.

The solar PV fed single stage DC-AC converter considered in this project is connected to grid using L filter. Although the THD requirements are fulfilled, better THD can be obtained using LCL filter. Modelling and controller design of the solar PV fed single stage DC-AC converter with LCL filter connected to grid can be done considering the non idealities like switch ON state resistances and output capacitances, stray resistances of the filter inductors and grid impedance. MPPT algorithm can be modified such that more accurate and fast response is obtained. With fine tuning of controllers, quality of the waveforms can be improved. Since PV source is intermittent in nature, it would be good to integrate it with energy storage option. Grid considered in this project is an infinite grid. So, there remains a good scope of integrating the solar PV fed single stage DC-AC converter with energy storage and connecting them to microgrids along with efficient energy management.

APPENDIX A

Inductor Design

The design of inductor requires, determination of size of the wire, size and shape of the magnetic core to be used and number of turns to obtain required inductance. Rated current determines the size of wire. The size and shape of magnetic core is determined such that the peak flux is carried safely by the core without saturation and the required size of the conductors are safely accommodated in the core.

Designing an inductor of L Henry, capable of carrying an rms current of I_{rms} and peak current of I_p involves the folllowing steps.

1.Selection of core

Compute the area product using eq

$$A_c A_w = \frac{L I_p I_{rms}}{k_w B_m J} \tag{A.1}$$

where A_c is the core area,

A_w is the window area,

k_w is the winding factor,

B_m is the flux density

J is the current density of the material. Select a core from core tables with the required $A_c A_w$.

2. Determination of number of turns

For the selected core, calculate the number of turns,

$$N = \frac{L I_p}{B_m A_c} \tag{A.2}$$

Select nearest whole number of N.

3. Determination of size of wire

Compute

$$a_w = \frac{I_{rms}}{J} \tag{A.3}$$

Select nearest whole number of wire guage and a_w* from wire table. If the calculated value corresponds to a thick wire, then practically winding the wire becomes a difficult task. Therefore we use thinner wires and then use it in parallel, like bundled conductors so that they can still carry the rated current.

Air gap required in the core is computed as

$$l_g = \frac{\mu_0 N I_p}{B_m} \tag{A.4}$$

APPENDIX B

Transformer Design

The design of transformer requires determination of size of wire and number of turns to be used for primary and secondary windings, core to be used, magnetizing inductance of the transformer.

Designing a transformer of given VA, V_1, V_2, J, B_m, k_w, and f involves the following steps.

1. Selection of core.

Compute the area product

$$A_c A_w = \frac{VA}{2fk_w JB_m} \tag{B.1}$$

Select the smallest core from the core tables having an area product higher than obtained in eq(1).

2. Determination of number of turns in primary and secondary of the transformer.

For the selected core, compute the number of turns

$$N_1 = \frac{V_1}{4fB_m A_c} \tag{B.2}$$

$$N_2 = \frac{V_2}{4fB_m A_c} \tag{B.3}$$

Select the nearest higher whole number to that obtained in eq (4), for the primary and secondary turns.

3. Determination of size of wire.

Compute the wire size for secondary and primary.

$$a_{w1} = \frac{I_1}{J} \tag{B.4}$$

$$a_{w2} = \frac{I_2}{J} \tag{B.5}$$

Select nearest whole number of wire guage and a_w* from wire table. Compute the length of secondary and primary turns, from the mean length per turn of the core tables. Resistance can be found from the wire tables.

4. Computation of the magnetizing inductance.

Reluctance can be calculated as

$$R = \frac{l_c}{A_c \mu_0 \mu_r} \tag{B.6}$$

Magnetizing inductance,

$$L_m = \frac{N_2}{R} \tag{B.7}$$

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