Efficient Hardware Design for SC-FDMA & 5G on FPGAs

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Efficient Hardware Design for SC-FDMA & 5G on FPGAs**, submitted by **Raghavendra Goli**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Due to confidentiality, the project was submitted to **Dr. Radhakrishna Ganti**. Please contact **rganti@ee.iitm.ac.in**