# Hardware Implementation of 5G NR Scrambler, Modulation and PSS detection

*A Project Report*

*submitted by*

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*in partial fulfilment of the requirements*
*for the award of the degree of*

## MASTER OF TECHNOLOGY

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# THESIS CERTIFICATE

This is to certify that the thesis titled **Hardware Implementation of 5G NR Scrambler, Modulation and PSS detection**, submitted by **O.V.R PHALGUN RAM**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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**Due to confidentiality issues, thesis is submitted to Dr.Radhakrishna Ganti. Kindly contact the professor for the complete thesis.**

# REFERENCES

[1]  3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Physical channels and modulation (Release 15) (3GPP TS 38.211 V15.1.0 (2018-03)).

[2]  Xilinx, Vivado Design Suite User Guide High-Level Synthesis (UG902). Xilinx (v2018.1) User Guide, 2018.

[3]   Xilinx, Vivado Design Suite User Guide Implementation (UG904). Xilinx (v2018.1) User Guide, 2018.

[4]   https://www.sharetechnote.com/html/5G/5G_SS_Block.html