Hardware Implementation of 5G Data Channel Encoder

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **Hardware Implementation of 5G Data Channel Encoder**, submitted by **Sowmika Nandamuri**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: 5G, Xilinx, Vivado HLS, ZCU111

Vivado HLS converts the code written in C, C++ and system C languages to RTL implementation which can be synthesized into a Xilinx FPGA. One important advantage of using HLS for designing is the directives available in HLS which allow high performance hardware implementations at a high level abstraction. And development of these modules in HLS takes less time compared to the traditional HDL languages. Verification of timing requirements and resource utilization can also be done on HLS.

In this thesis, I present hardware implementation of 5G Data Channel Encoder which is realized with Vivado HLS tool and verified on Vivado IP Integrator. Both the softwares are from Xilinx. Modules are first designed as per requirements in Vivado HLS. Once the module meets performance requirements it is exported as an IP. These IPs are then integrated and tested on Vivado IP Integrator. Zynq Ultrascale+ RFSoC Evaluation board (ZCU111) from Xilinx is used for verifying functionality of the modules.

CHAPTER 1

Introduction

Data Channel Encoder is the first module in 5G NR physical (PHY) layer which takes in a transport block of data bits of dynamic size delivered from MAC layer and gives out interleaved encoded bits to scrambler. The transport block(TB) is segmented into code blocks(CB) based on the code rate and total no. of bits in the TB, this is called as code block segmentation. Each CB goes through a sequence of steps in the module before being transmitted to the scrambler. After segmentation CRC is attached to each code block separately if there are more than one CB in the TB. CRC attachment is done on each CB to enable error detection. Later it is sent to LDPC (Low-Density Parity Check) encoding for error correction followed by rate matching and bit interleaving modules before sending them to the scrambler module which is the next in the transmitter chain. Data channel encoder enables the detection and thereby correction of errors if any are detected in the receiver chain by LDPC Decoder.

Due to confidentiality issues only abstract is uploaded. Complete thesis has been submitted to Dr. Radha Krishna Ganti. Kindly contact professor for full thesis.

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