DESERIALIZER

A Project Report

submitted by

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in partial fulfilment of the requirements

for the award of the degree of

MASTER OF TECHNOLOGY

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESERIALIZER**, submitted by **M Kiran Kumar**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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I would like to take this opportunity to thank my lab mates Deepthi, Gautham and Sreenivasa Rao for their assistance while doing the project.Thanks to my parents for their tireless support throughout my life.

ABSTRACT

As semiconductor fabrication technology develops, the demand for higher transmission data rates constantly increases; thus there is an urgent need for a power-efficient, robust and broad bandwidth chip-to-chip communication method. A lot of work has been done to address this issue as researchers strive for more integrated inter-IC communication technology with CMOS. A high-speed serial link can help meet this goal.

In this thesis, forwarded clock Serial Link Receiver Architecture is described. It consists of equalizer, phase recovery unit (PRU), phase looked loop (PLL) and deserializer(DES).Design of PLL,BBPD,Which is a part of PRU and DES is shown. Mathematical formulations of the negative feedback loop, stability and noise analysis of the entire PLL having a reference frequency of 15MHz -75MHz and output frequency of 105MHz - 525 MHz with it's blocks implemented at transistor level in SCL 180 nm technology are discussed and a short discussion on 1:7 Deserializer architectures is presented. In addition to this BBPD implementation is discussed .Finally, some future work to be done to make it a complete receiver is presented.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

SERDES	Serializer and Deserializer
PLL	Phase Looked Loop
DLL	Delay Looked Loop
PRU	Phase Recovery Unit
BBPD	Bang-Bang Phase Detector
DLF	Digital Loop Filter
PRPLL	Phase Rotating Phase Looked Loop
PSRR	Power Supply Rejection Ratio
PSD	Power Spectral Density
NTF	Noise Transfer Function
PFD	Phase Frequency Detector
CP	Charge Pump
LF	Loop Filter
VCO	Voltage Controlled Oscillator
VCDL	Voltage Controlled Delay Line
Tx	Transmitter
Rx	Receiver
PI	Phase Interpolator
JTOL	Jitter Tolerance
JTRAN	Jitter Transfer
BBPD	Bang-Bang Phase Detector
CDR	Clock and Data Recovery Unit
DFF	D-Flip flop
SA	Sense Amplifier
CSAs	Cascade of Sense Amplifiers

CHAPTER 1

INTRODUCTION

1.1 Motivation

CMOS technology exploration and scaling allows higher processing speeds than ever in minimum silicon area. For instance, AMD's Ryzen Threadripper 2990WX in 12 nm technology can be clocked at 3-4.2 GHz. Having 32 cores and 64 threads in it, data processing speed can be much higher than clock rate.

High throughputs make use of higher processing speeds and permit to produce large amount of data, so does the on-chip bandwidth. Off-chip data rate should also be scaled accordingly to increase the system bandwidth.Parallel lines can enhance the off-chip data rate. Despite increase in total data rate, deterministic unbound jitter due to cross talk also increases as the density of parallel lines and data rate per channel becomes greater.

Increasing the signal power does not alleviate this problem as the crosstalk increases with increase in signal to noise ratio. Hence, the plausible solution seems to be increasing the data rate per link so called serial link by multiplexing the parallel data using a serializer. Some of the serial links include processor to memory(RDRAM, XDRAM, XDR2, DRAM), processor to peripheral(PCIe, Infiniband, USB3), processor to processor(Intel QPI, AMD Hypertransport) and networks(LAN, WAN, backplane routers).

1.2 Thesis Outline

The goal of this thesis is to provide design details of serial link Receiver in circuit level with scl 180 nm technology aiming at 315Mbps - 1.575Mbps data rates. chapters are organized as follows:

Chapter 2 Describes an overview of a high-speed serial link

Chapter 3 Deals with design and implementation of each building block in the PLL and mathematical description of loop analysis, design procedure and noise analysis of PLL.

Chapter 4 Deals with implementation of sense amplifier based D-Flip flop

Chapter 5 Deals with design and implementation of Deserilalizer architectures and their drawbacks.

Chapter 6 provides an overview of PRU building blocks and their results.

Chapter 7 summarizes the thesis with the work completed and suggests future work to be done

CHAPTER 2

SERIAL LINKS OVERVIEW

Serial links are widely used in processor-to-memory (GDDR5, DDR4 RAMs), processor-toperipheral (PCIe, USB 3.1, Thunderbolt), processor-to-processor and network communications. They serve as a good alternative to parallel links when the aim is to reduce on-chip area, overcome cross-talk and data skew and reduce manufacturing costs (single line against multiple lines of communication).

2.1 Introduction on Serial Links

Typical serial link (SERDES) consists of transmitter(Tx),channel and receiver(Rx) as shown in figure 2.1

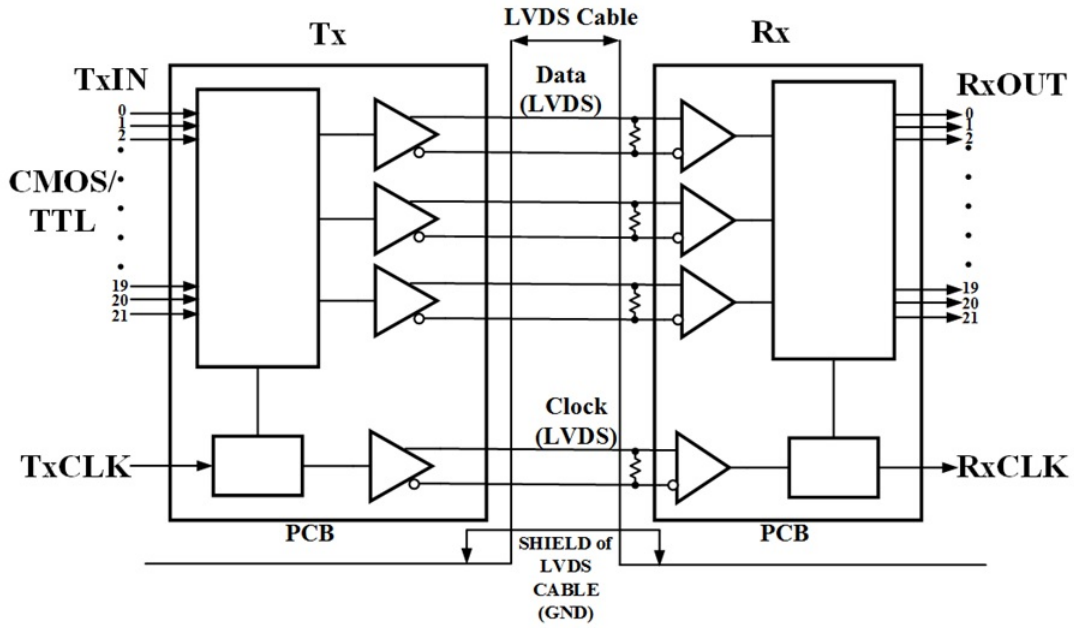

Figure 2.1: Block Diagram of SERDES

Transmitter: Every serial link transmitter should have the following features: It's impedance should be independent of the output swing and it is matched to characteristic impedance of channel to avoid signal reflections.It should support various ways of

equalization and it's output swing should be adjustable to accommodate both low loss and high loss channels.Transmitter mainly consists of serializer,pre-driver,output driver and PLL. Serializer uses clock from PLL to convert input parallel data sequences with lower data rates into a single bit stream of higher data rate.According to serialized data bit pattern, Pre-driver generates required swing at the input of output driver such that impedance of output is matched to characteristics of channel.as mentioned above output driver matches transmitter's output impedance with characteristic impedance of channel.Equalization in the transmitter can be either in the output driver or while serializing data itself.

Channel: It is a medium by which data can be sent from transmitter to receiver.Usually channel exhibits low pass characteristics and it's cutoff frequency decides the highest data rate that can be transmitted through it and also depends on receiver's ability to equalize the amount of loss incurred in the channel.

Receiver: The job of receiver is to convert the transmitted higher data rate differential swings into full swings without any bit errors and back convert serial higher data bit stream to parallel lower data rate bit patterns.Receiver mainly consists of equalizer depending on channel output, clock and data recovery unit(CDR) and deserializer. CDR recovers clock from the data and synchronizes it with recovered clock.Deserializer converts serial data with higher data rate to parallel data sequences with lower data rate.

2.2 Proposed Serial Link Receiver Architecture

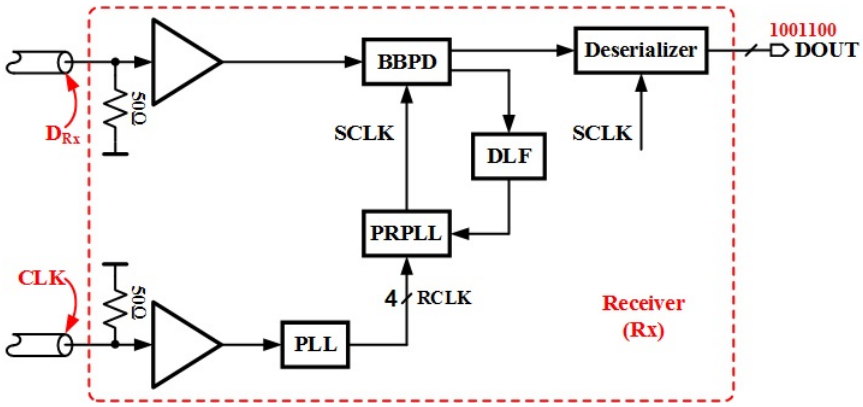

Figure 2.2: Proposed Receiver Architecture

Proposed forwarded clock receiver architecture consists of PLL, Equalizer, PRPLL based Phase Recovery Unit and Deserializer.Since the clock is forwarded, through additional channel, clock of required frequency can be recovered from PLL.Equalizer helps to make the eye opening better for sampling. The phase and data recovery (PRU) unit is a phase rotating phase-locked loop (PRPLL) based PRU.The PRU is placed on the receiver's end after equalizer and its function is to adjust the sampling clock phase such that the incoming data is sampled at correct instant to obtain data recovery.this kind of PRU consists of Bang-Bang Phase Detector(BBPD), Digital Loop Filter(DLF) and Phase Rotating PLL,which takes input recovered clock phases from PLL. Finally, the job of deserializer is to convert serial data with higher data rate to parallel data sequences with lower data rate.Analysis and Implementation of above mentioned blocks is discussed in this thesis.

Sl.NO	Description	Specification
1	Supply Voltage	1.8
2	Clock	15MHz-75MHz
3	LVDS channel Data Rate	105Mbps-525Mbps
4	LVDS common mode voltage	1.2
5	LVDS Swing	325mV
6	Load at CMOS or TTL load	C_L=8pF
7	LVDS O/P low to high transition time	1.5ns
8	LVDS O/P high to low transition time	1.5ns
9	Operating Temperature range	-40°C - +125°C

Table 2.1: Specifications of UT54LVDS218 Deserializer

CHAPTER 3

PLL BUILDING BLOCKS AND ANALYSIS

PLL is nothing but a negative feedback loop which can lock to desired output phase and frequency with respect to reference signal. Basic building blocks of PLL are shown in figure 3.1

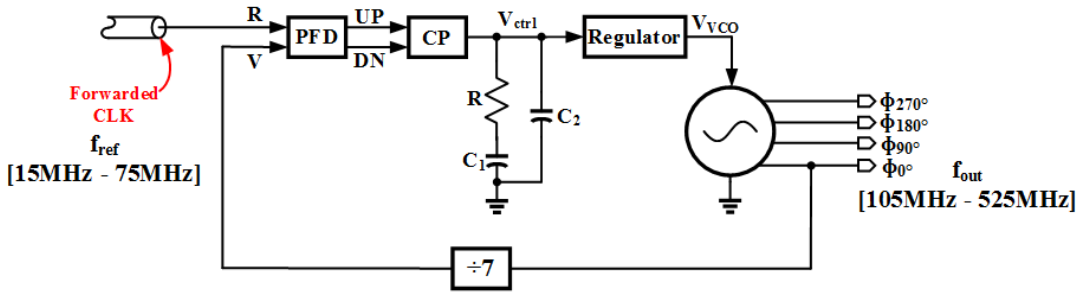

Figure 3.1: PLL Block Diagram

3.1 Basic PLL Building Blocks

3.1.1 Phase Frequency Detector(PFD)

It is the primary block of a phase locked loop, which compares phase and frequency of divided signal with the reference signal and generates accordingly UP and DN pulses based on the difference between the two signals,which will be fed to next block called charge pump(CP).

3-state PFD has a problem called dead-zone,which means small phase differences at the input cannot be detected by the PFD owing to the fact that it's reset time is small.

NAND Based PFD as shown in figure 3.2 can prevent the problem of dead-zone by having more reset delay sothat UP and DN pulses are properly generated and this configuration detects small phase differences and hence improves the frequency acquisition range. Reset delay of this configuration is given by $\mathrm{T_{RST}} = 2\mathrm{T_{NAND2}} + \mathrm{T_{NAND4}}$.

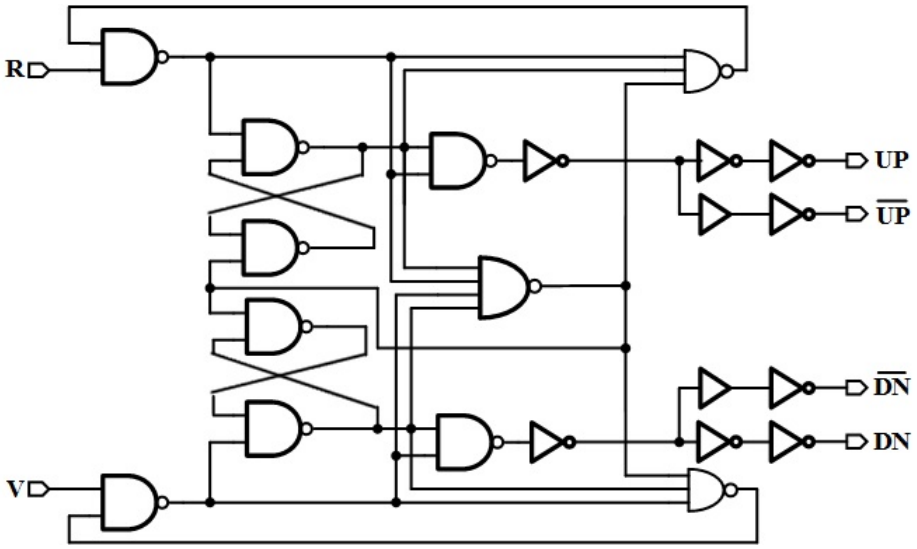

Figure 3.2: NAND PFD topology

3.1.2 Charge Pump(CP)

It pushes the current into loop filter and pulls out from it depending on UP and DN pulses generated from PFD.Differential charge pump topology is used to reduce switching transients, which will inject some charge into loop filter there by it results in change control voltage(V_{ctrl}).

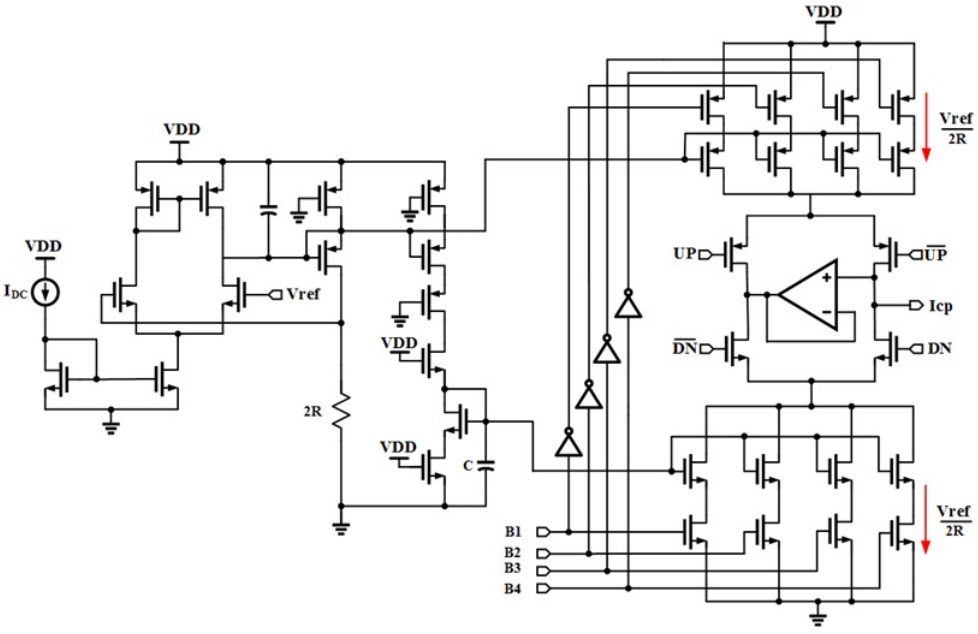

Figure 3.3: Differential charge pump topology with current steering DAC

In the above topology, four bits are used to control the current flowing into loop filter. as a result one can have tunability over loop bandwidth.

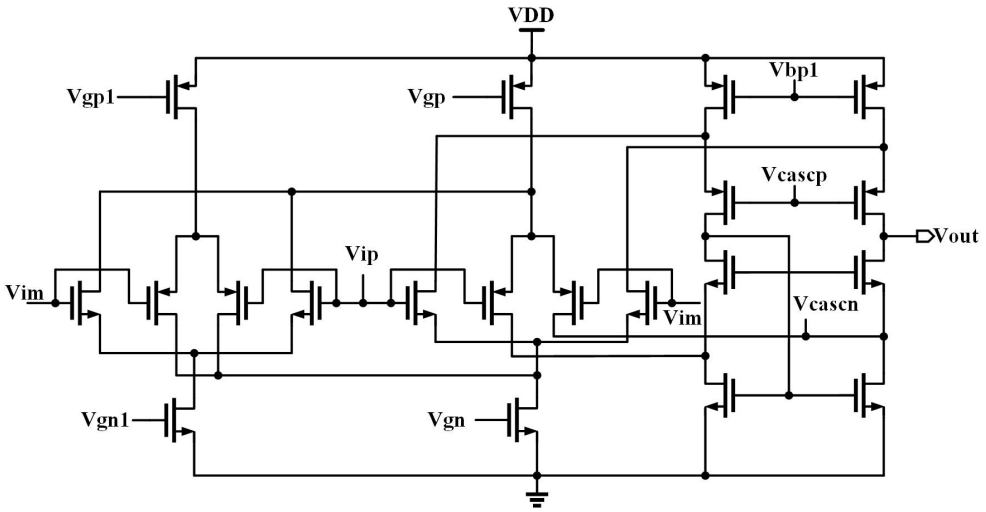

Figure 3.4: Wide input common mode range Op-Amp

Since (V_{ctrl}) varies from 0.68V to 1.5V for 105MHz to 525MHz,unity feedback opamp should have wide input common mode range. Complementary NMOS and PMOS input pair and dummy NMOS and PMOS pair is present. When the common mode range is [0,0.9V],PMOS pair will function and when common mode range is [0.9,1.8],NMOS pair will function.but,When Exactly common mode is 0.9V,both pairs will function causing to have double the trans conductance.With the help of dummy pair, uniform trans conductance is maintained through the input common mode range.The dummy NMOS and PMOS pair will be active and reduces the bias currents through the input pairs when the common-mode voltage is 0.9V. The dummy pair will be inactive when the common-mode voltage is other than 0.9V. .

3.1.3 Loop Filter

It generates control voltage depending on CP output.It basically adds one zero and two poles.Transfer function of loop filter is given by

$$G(s) = \frac{1 + \frac{s}{\omega_z}}{s(1 + \frac{s}{\omega_p})}$$

where $\omega_z = \frac{1}{RC_1}$ and $\omega_p = \frac{C_1+C_2}{RC_1C_2}$

pole ω_p is introduced to reduce ripple in control voltage due to this reference spur is reduced at the output. Note that I_{cp}, R, $C_1 and\, C_2$ values are chosen based on phase margin (ϕ_m) and loop bandwidth.

3.1.4 Regulator

It is a closed loop circuit which suppress the noise coming from power supply.It is added in series with the loop filter. Regulator loop employs operational amplifier and pass transistor as shown in figure 3.4

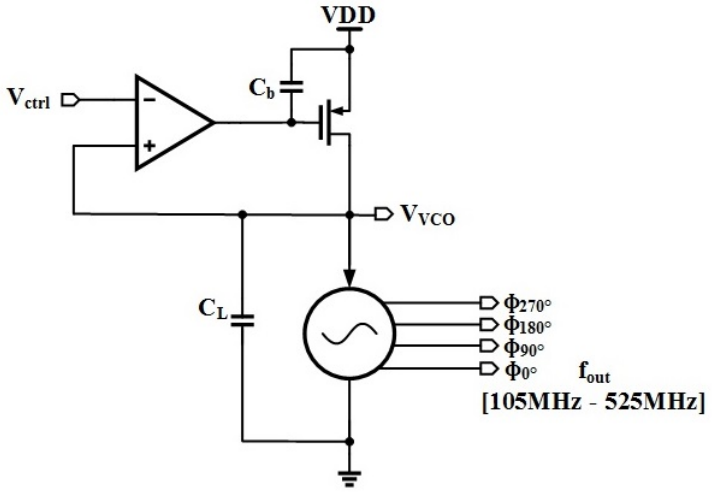

Figure 3.5: Regulator Loop with VCO

C_b and C_L will add poles and zeros in regulator loop.Both the capacitor values are chosen such that better ϕ_m and PSRR are achieved.It is observed that from V_{ctrl} to V_{vco} is a low pass filter.

$$\frac{V_{vco}}{V_{ctrl}} = \frac{1}{1+\frac{s}{\omega_{reg}}}$$

ω_{reg} must be far away from PLL loop bandwidth.If it comes insides, it will effect the stability of PLL itself and there by phase margin will change.

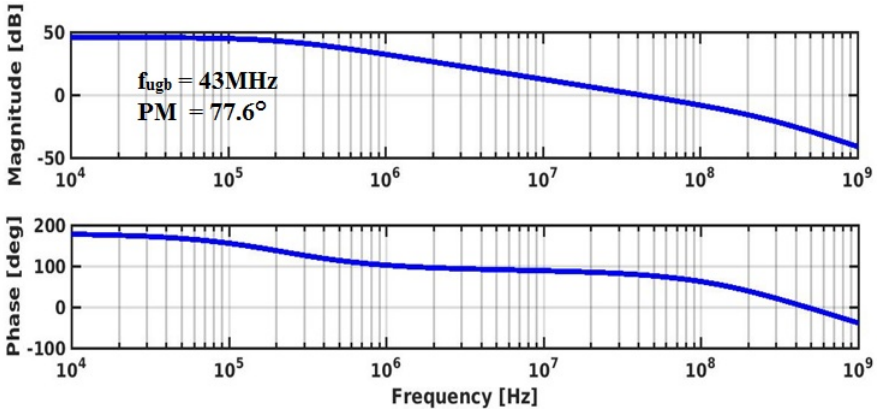

Figure 3.6: Loop Gain and Phase Margin of Regulator at TT27°C @ 525MHz

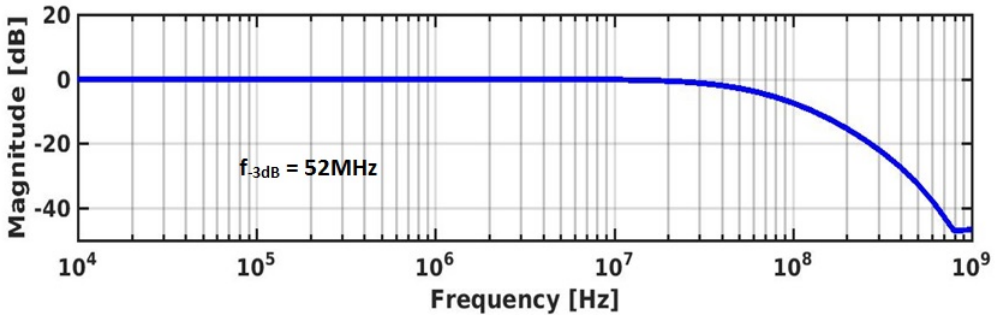

Figure 3.7: CLBW from V_{ctrl} to V_{vco} at TT27°C @ 525MHz

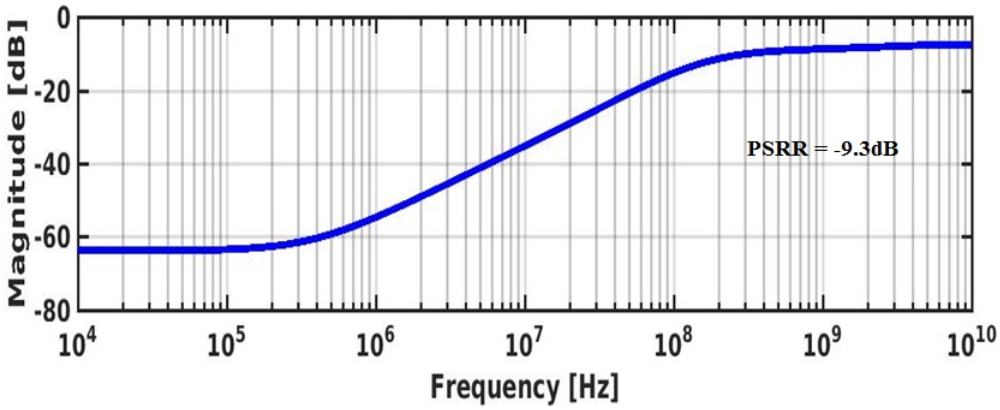

Figure 3.8: PSRR at TT27°C @ 525MHz

3.1.5 Voltage Controlled Oscillator(VCO)

It generates periodic waveforms whose frequency varies with respect to V_{ctrl}. If V_{ctrl} increase, output frequency increases and vice versa. Eight inverter based Pseudo differential ring oscillator with cross coupled inverters is designed as shown in figure 3.5 such that it's output frequency varies from [105MHz - 525MHz] with V_{ctrl} range being [0.68V - 1.48V] across process and temperature.

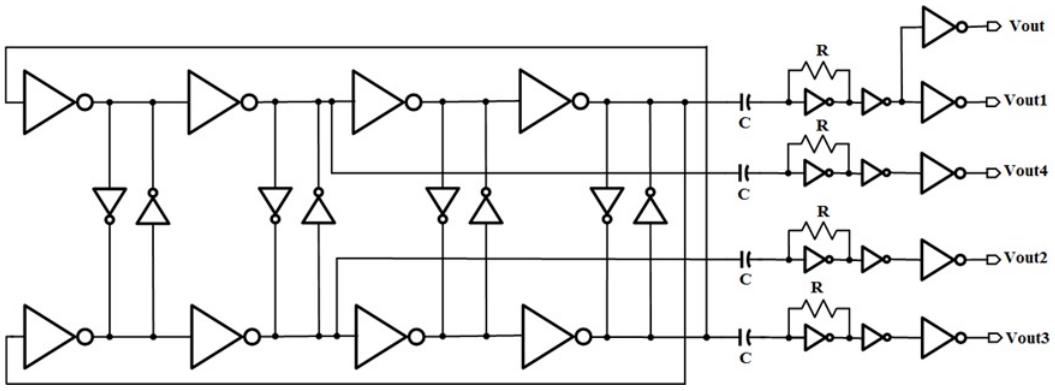

Figure 3.9: Pseudo Differential Ring Oscillator

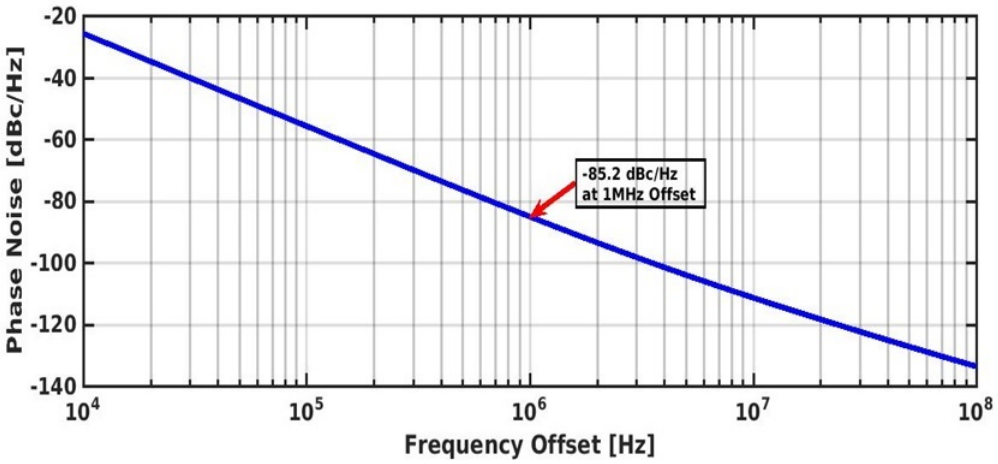

Figure 3.10: PSD of VCO at TT27°C @ 525MHz

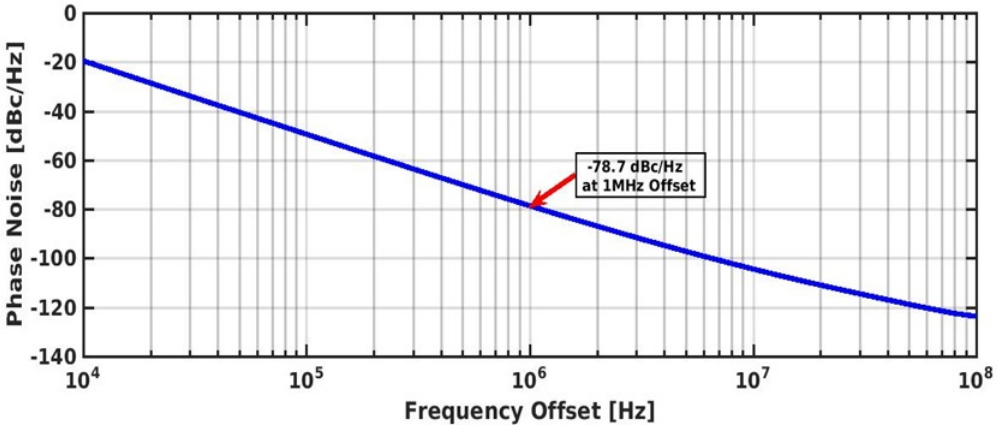

Figure 3.11: PSD of VCO at TT27°C @ 105MHz

Corner	f_{out}	K_{VCO}[MHz/V]	PM	CLBW[MHz]	PSRR[dB]
SS125°C	105MHz	1200	79°	25	-7.75
SS125°C	525MHz	430	81°	37	-7.16
TT27°C	105MHz	1400	78.4°	31	-7.8
TT27°C	525MHz	660	77.6°	52	-9.3
FF-40°C	105MHz	1100	77°	39	-7.8
FF-40°C	525MHz	925	75.8°	70	-9.3

Table 3.1: Summary on Regulator Loop with VCO

3.1.6 Frequency Divider

It divides higher output frequency to lower frequency to match it with reference frequency to have feedback action.Since f_{ref} is [15MHz - 75MHz] and f_{out} is [105MHz - 525MHz] , divide by 7 counter is expected to be used. Synchronous divide by 7 counter as shown in figure 3.6 is designed to have 50 percent duty cycle.

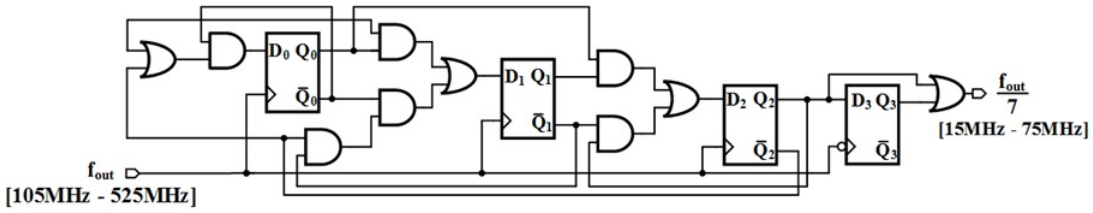

Figure 3.12: Divide by 7 counter

3.2 PLL Loop Dynamics

This section includes small signal model, stability analysis of the loop, design procedure and noise analysis of PLL.

3.2.1 Small Signal Model of PLL

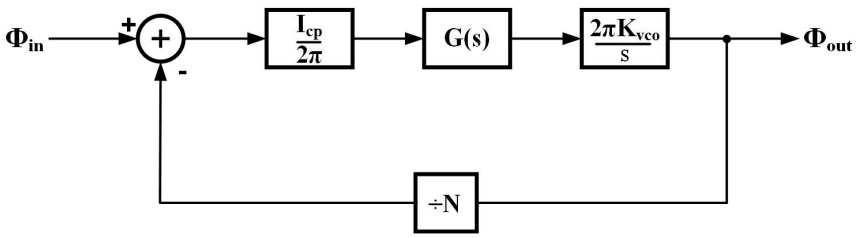

Figure 3.13: Small Signal Model of PLL

$$G(s) = \frac{1 + \frac{s}{\omega_z}}{s(1 + \frac{s}{\omega_p})}$$

$$LG(s) = \frac{I_{cp}RK_{vco}}{N(C_1 + C_2)} \times \frac{1 + \frac{s}{\omega_z}}{s^2\left(1 + \frac{s}{\omega_p}\right)}$$

Loop Gain has one zero $\omega_z = \frac{1}{RC_1}$, two poles at origin and another pole $\omega_p = \frac{C_1+C_2}{RC_1C_2}$

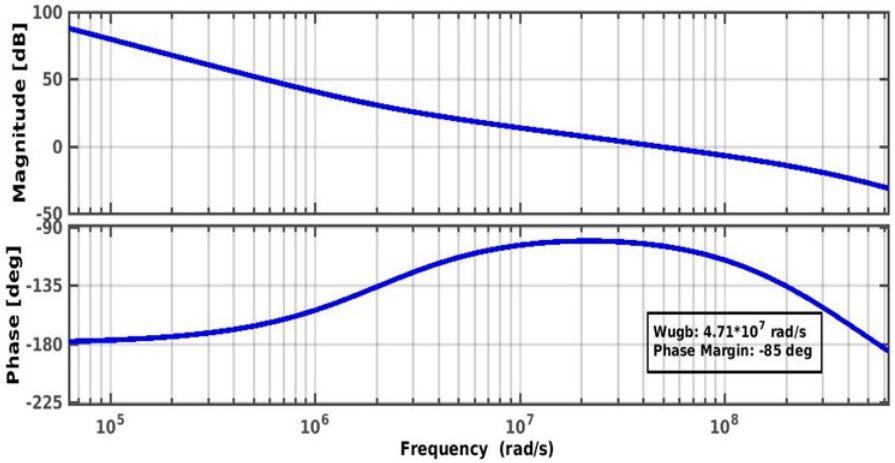

Figure 3.14: Loop Gain and Phase Plot at TT27°C @ 525MHz

3.2.2 Stability of the Loop

Phase Margin(ϕ_m) of a loop must be maintained as high as possible for better loop stability and for continuous time approximation to be valid , Loop bandwidth must be less than or equal to $\frac{f_{ref}}{10}$.

Phase margin expression is given by

$$\phi_m = \tan^{-1}(\frac{\omega_{ugb}}{\omega_z}) - \tan^{-1}(\frac{\omega_{ugb}}{\omega_p}) \tag{3.1}$$

Condition for maximum flat phase margin:

$$\frac{d\phi_m}{d\omega_{ugb}} = 0 \tag{3.2}$$

which gives the following results

$$\omega_{ugb} = \sqrt{\omega_z * \omega_p} \tag{3.3}$$

$$\frac{\omega_{ugb}}{\omega_z} = \sqrt{1 + \frac{C_1}{C_2}} \tag{3.4}$$

$$\left(\frac{\omega_{ugb}}{\omega_z}\right)^2 - 2 * \tan(\phi_m) * \left(\frac{\omega_{ugb}}{\omega_z}\right) - 1 = 0 \tag{3.5}$$

3.3 PLL Noise Analysis

Each building block contributes noise to the output in PLL in addition to contribution from reference input noise. NTFs are found from each noise source to output and so found PSDs.Upon summing up all the PSDs,Resultant PSD is obtained and integrating area under the curve gives the total output jitter.

Following are the NTFs from Reference, Charge Pump, Resistor, VCO to output respectively.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{N \times LG}{1 + LG}$$

$$\frac{\phi_{out}}{I_{n,cp}} = \frac{2\pi}{I_{cp}} \times \frac{\phi_{out}}{\phi_{in}}$$

$$\frac{\phi_{out}}{v_{n,R}} = \frac{C_1 s}{1 + \frac{s}{\omega_z}} \times \frac{\phi_{out}}{I_{n,cp}}$$

$$\frac{\phi_{out}}{\phi_{vco}} = \frac{1}{1 + LG}$$

Squaring of NTFs gives transfer function for PSDs and hence by feeding in input PSDs due to Reference, CP, R, VCO, one can find the output PSDs there by the resultant PSD,which upon integrating area under it gives the final output jitter.

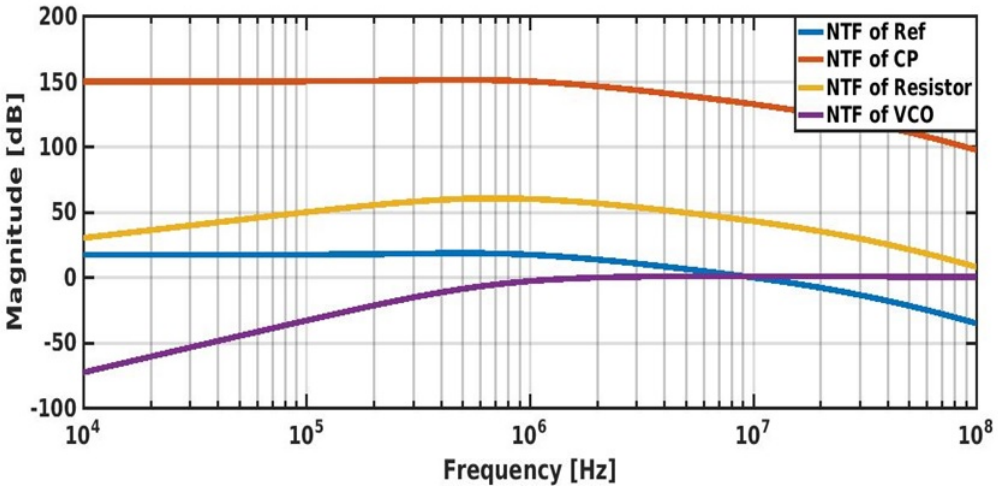

Figure 3.15: NTFs at TT27°C @ 525MHz

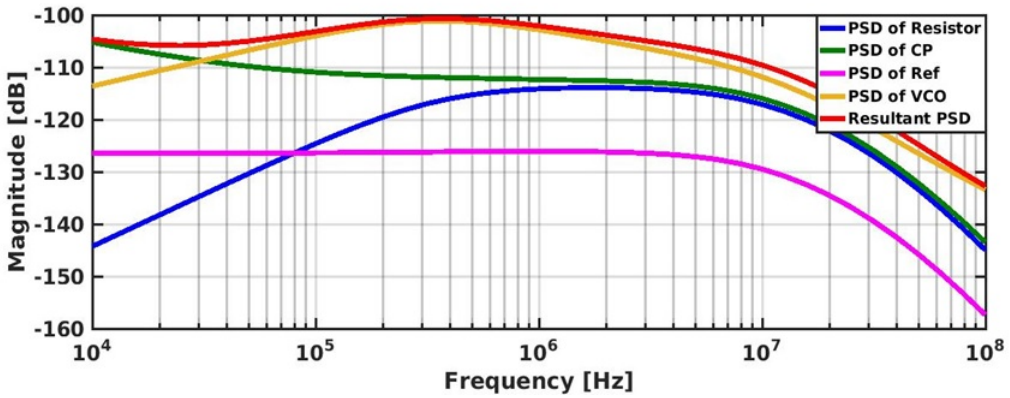

Figure 3.16: PSDs at TT27°C @ 525MHz

3.4 Design Procedure of Loop Parameters

by setting phase margin (ϕ_m) = 85°, $\frac{C_1}{C_2}$ and ω_z can be found from equations 3.4 and 3.5. by choosing R = 30KΩ, from $\omega_z = \frac{1}{RC_1}$ expression, C_1 value is found to be 16.26pF, Hence C_2 value is found to be 31fF.Upon making LG(s) = 1 and substituting R, C_1, C_2, found I_{cp} = 16.26μA

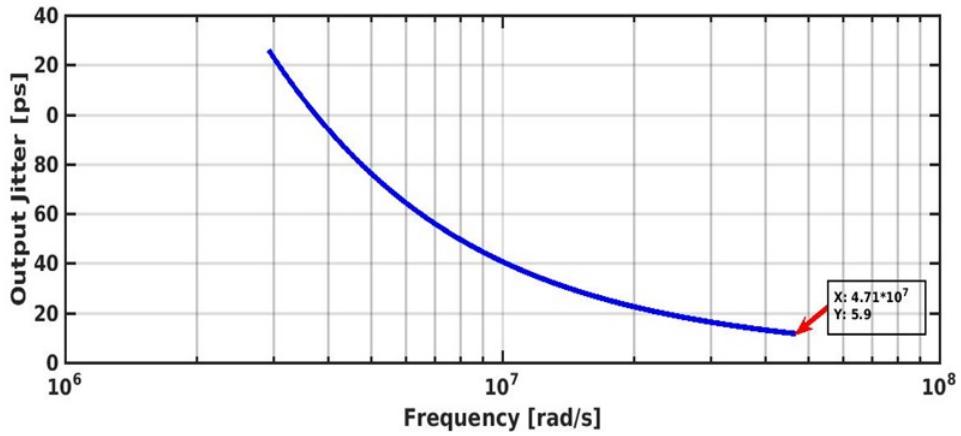

Figure 3.17: jitter Vs ω_{ugb} at TT27°C @ 525MHz

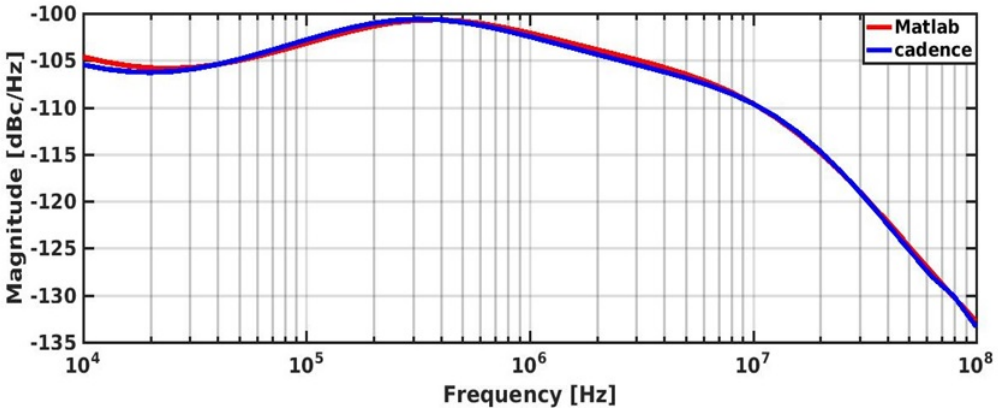

Figure 3.18: Resultant PSD (Matlab Vs cadence) at TT27°C @ 525MHz

Area under above PSD is found to be 5.9ps.

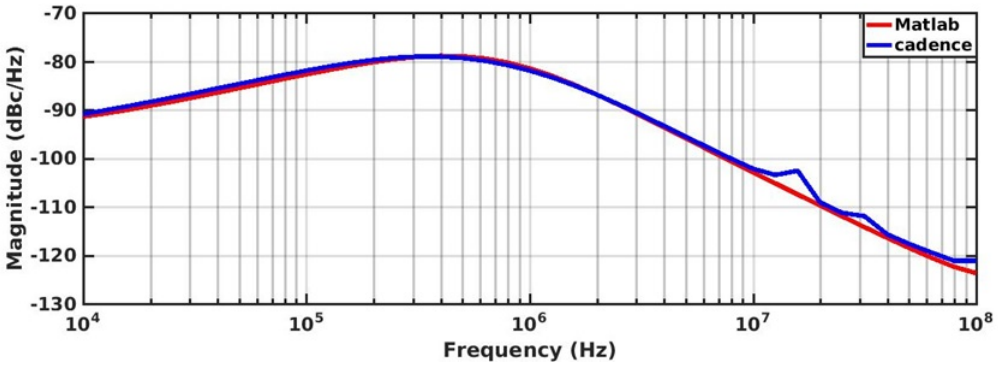

Figure 3.19: Resultant PSD (Matlab Vs cadence) at TT27°C @ 105MHz

Area under above PSD is found to be 197ps.

Corner	f_{out}	ω_{ugb}	Output Jitter	Power Consumption
SS125°C	105MHz	1.5MHz	204ps	0.81mW
SS125°C	525MHz	7.5MHz	5.6ps	1.25mW
TT27°	105MHz	1.5MHz	197ps	0.76mW
TT27°	525MHz	7.5MHz	5.9ps	1.1mW
FF-40°	105MHz	1.5MHz	157ps	0.72mW
FF-40°	525MHz	7.5MHz	8.5ps	0.97mW

Table 3.2: Summary on Jitter numbers and Power Consumption of PLL

CHAPTER 4

SENSE AMPLIFIER BASED D-FLIP FLOP

D-Flip flop is one of the basic building blocks while implementing deserializer and bang-bang phase detector(BBPD) in serial link receiver.Since the receiver receives data in the form of differential swings of smaller amplitude if channel losses are high, one has to convert small differential swing to full swing by amplifying it.This kind of amplification can be done by an element called 'Sense Amplifier'. It is nothing but a Strong-ARM latch, which is a clocked circuit, whose output lasts for half a clock period.In order to hold output for full clock period, RS latch will be cascaded with Strong-ARM latch as shown in figure 4.1

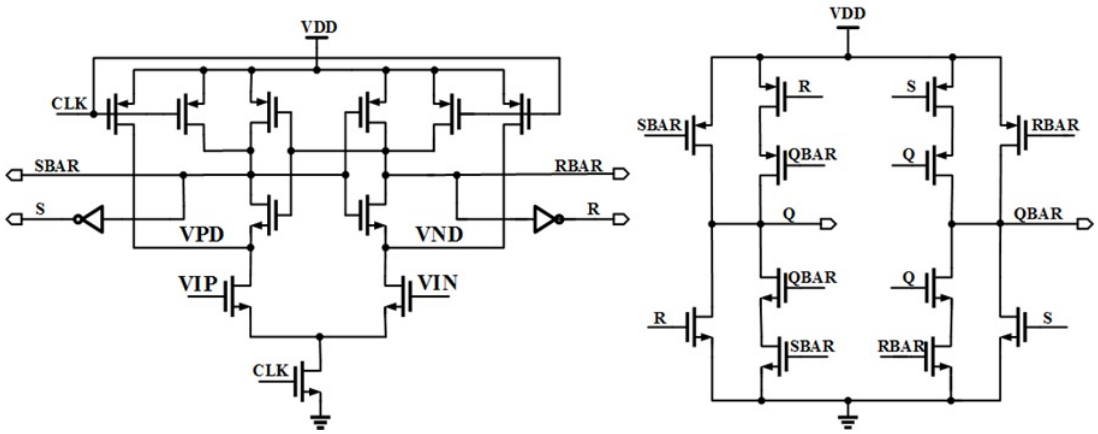

Figure 4.1: Sense Amplifier Based D-Flip flop

Operation of Strong-ARM latch is as follows: When clock is low, all the intermediate nodes RBAR, SBAR, VPD, VND will be reset to VDD. When clock is high and VIP > VIN ,initially both nodes VPD, VND will charge, but the discharge rate at VPD is faster than that of VND. as soon as VPD is slightly less than VDD-Vth_n,NMOS will turn ON and starts discharging node voltage at SBAR.The moment node voltage at SBAR goes one Vth_p, top PMOS will turn on and finally makes RBAR to charge to VDD and in the process of reaching to VDD, it will turn off PMOS on the other side.The voltage at node SBAR is continuously discharged and finally reaches to 0.If VIN > VIP , SBAR will be set to VDD and RBAR will be set to 0.

This process of both the node voltages start discharging and after some time one will be set to VDD and another will be set to 0 is called 'Regeneration' as depicted in figure 4.2.

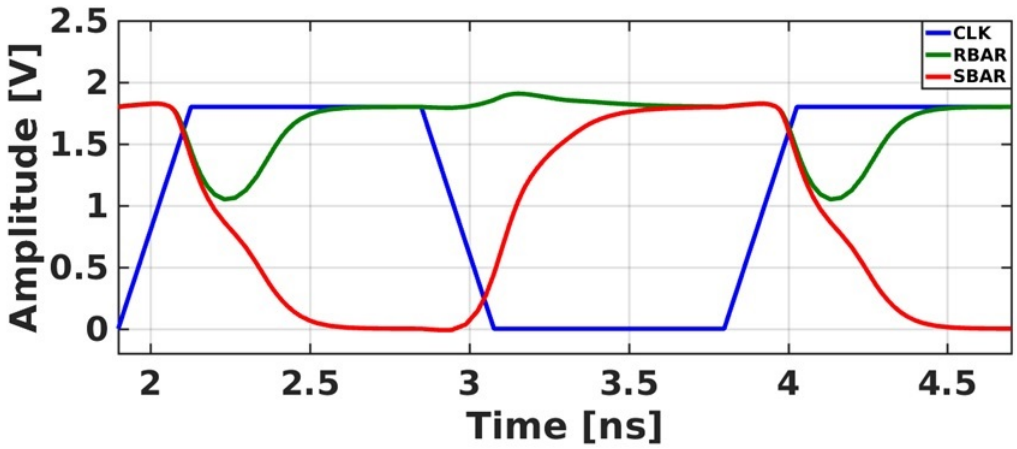

Figure 4.2: Output of Strong-ARM latch when V_{id} = 20mV

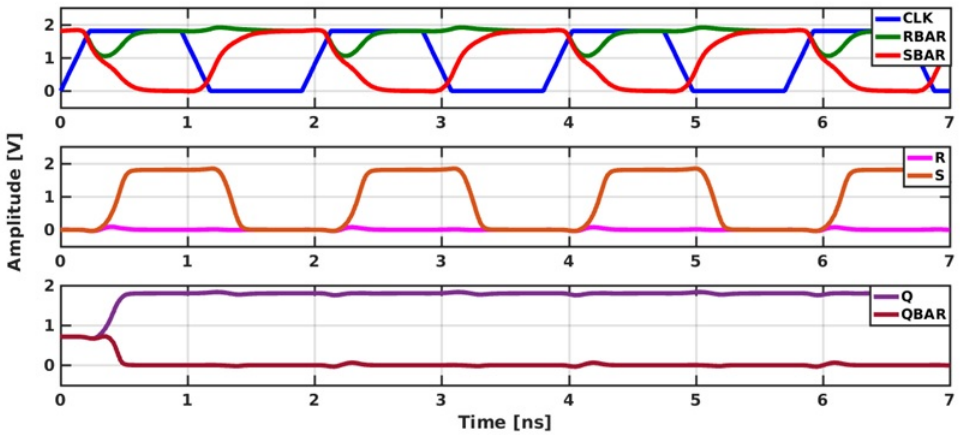

Figure 4.3: Output of Strong-ARM latch and RS latch when V_{id} = 20mV

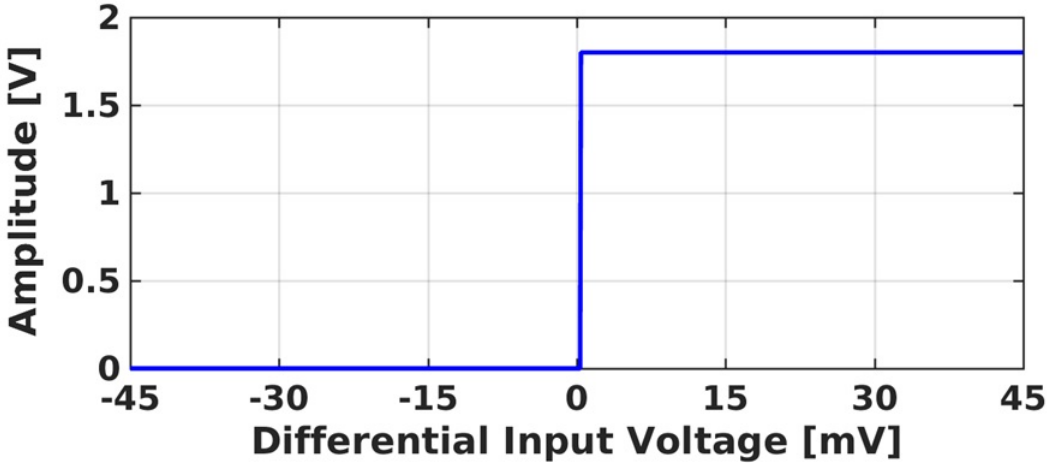

Figure 4.4: Ideal Sense Amplifier based DFF characteristics.jpg

Ideally sense amplifier should resolve smaller input differential voltage effectively.but process mismatch among transistors themselves creates some offset, which could be positve or negative.Cancellation of offset is very much need while trying to resolve smaller input differential voltage. Monte Carlo simulation is to be run to know standard deviation of offset value, which was found to be 8.6mV.In order to cancel 3σ offset, capacitive compensation technique is used as in figure 4.5

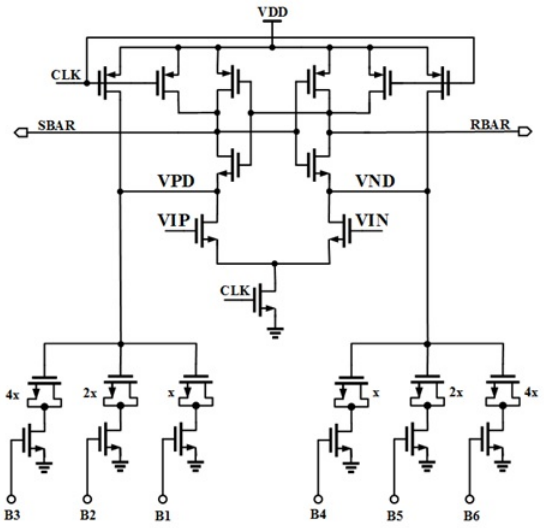

Figure 4.5: SA with Offset Compensation

Both the nodes VPD and VND have capacitive banks each controlled by 3 bits and effectively it is 4 bit capacitive bank with a step size 2.8fF. Capacitance mismatch across both the nodes will be created such that the offset will get cancelled. with 4 bit capacitve bank having step size of 2.8fF, Offset can be compensated from -26mV to 26mV.

In order to resolve even smaller differential swings, cascading of sense amplifiers will help.Upon cascading them, the gain of amplification process increases, which will help to increase the sensitivity of the overall cascaded system as shown in figure 4.6

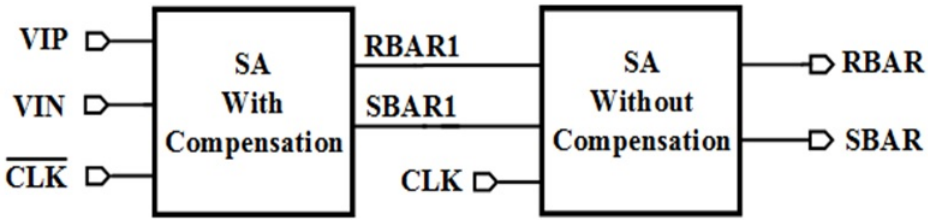

Figure 4.6: Cascade of SAs

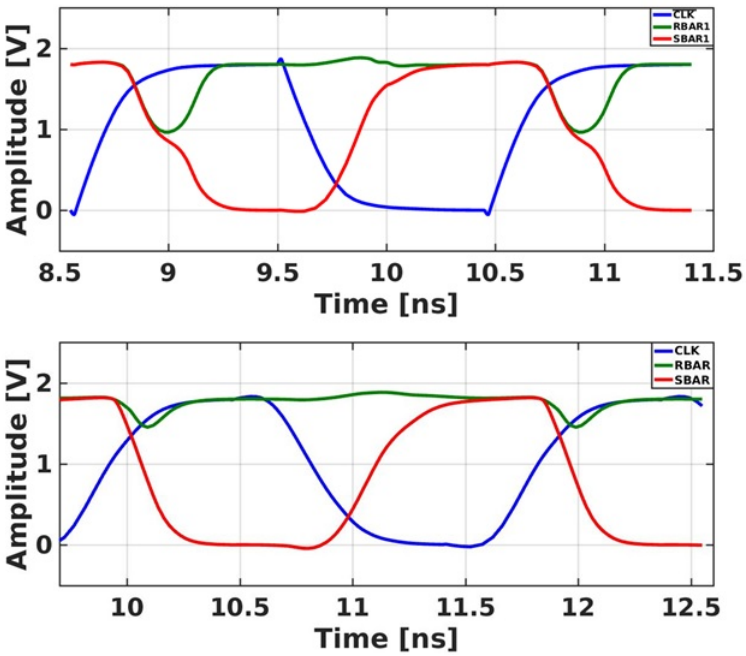

Figure 4.7: Output of CSAs when V_{id} = 10mV

Mostly cascaded sense amplifiers followed by RS latch configuration is in BBPD,where the flip flops have to resolve smaller differential swing data and edge sample.

CHAPTER 5

DESERIALIZER ARCHITECTURES

5.1 Overview

Deserializer is a block, which converts high speed serial data to parallel data with lower data rates.Several architectures are existing to do this job.Traditional 1:N DEMUX suffice the purpose for even number of bits,but In case of converting a stream of odd number of bits to parallel stream of data, this 1:N DEMUX is not used. Following are the proposed architectures to convert odd number of serial bits to parallel data bits.

5.2 Sample and Hold based 1:7 Deserializer

It samples the data when clock phases are high and hold it, if atleast one of the clock phases are low.Since 7 bits of serial data with data rates 105Mbps to 525Mbps to be converted to parallel data with data rates 15Mbps to 75Mbps,one has to have sampling process to be done at the rate of 105MHz to 525MHz. Basic unit cell of sample and hold based deserializer is as in figure 5.1

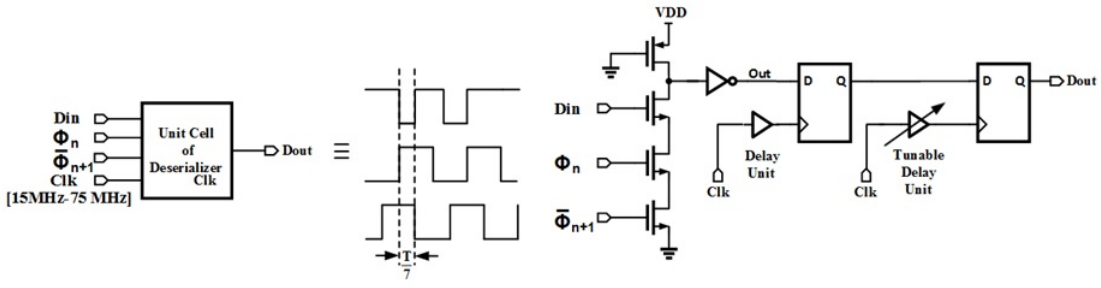

Figure 5.1: Basic Unit Cell of SH based 1:7 Deserializer

Delay Locked Loop(DLL) generates seven phases with a phase shift corresponding to $\frac{T}{7}$, where T is the time period that the parallel data should have after serial to parallel conversion.Sampling is done well within one seventh of T and data is held for $\frac{T}{7}$. after $\frac{T}{7}$, output(Out) will be reset to 0.Sampling of output(Out) data has to be done before it

gets reset to 0.D-Flip flop clocking at 15MHz to 75MHz samples and holds data over a period of T.Like wise 7 bits of data will be sampled.Data bits at the output D-Flip flops have phase shift corresponding to $\frac{T}{7}$ and synchronization of bits to one seventh of data rate can be done using seven D-Flip flops clocking at 15MHz to 75MHz.Tunable delay element is required to have proper phase alignment of clock while sampling the data bits. Fixed delay element may also be used depending clock to Q delay of Flip flops. Problems with this architecture are as follows:Phases must be generated DLL with $\frac{T}{7}$ spacing apart over wide frequency range,which is difficult to do.Voltage level at output of sampling unit drops at low frequencies and as a result of this, glitches will be observed at the output. This may lead to bit errors while sampling using D-Flip flop.Sample and Hold based 1:7 Deserializer is as shown in figure 5.2

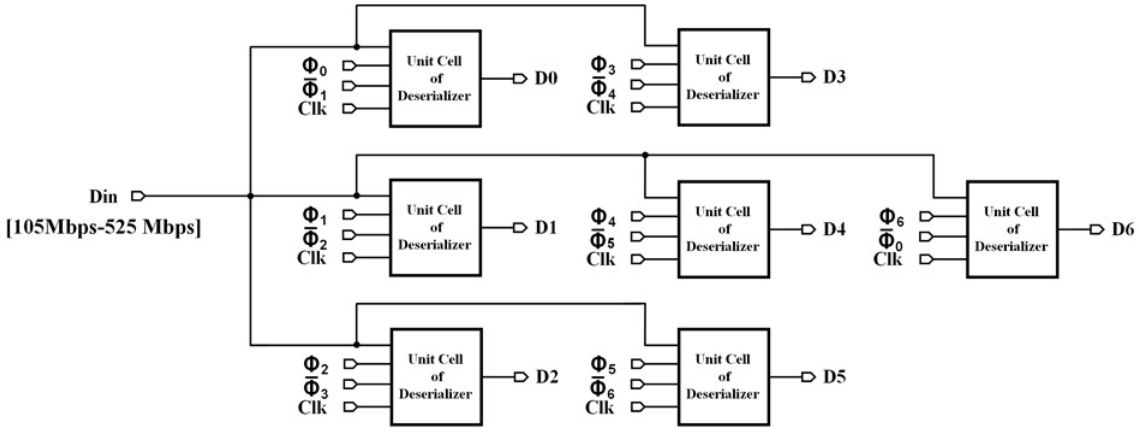

Figure 5.2: Sample and Hold based 1:7 Deserializer

5.3 D-Flip flop based 1:7 Deserializer

This architecture uses 14 D-Flip flops as shown in figure 5.3. seven D-Flip flops all clocking at 105MHz - 525MHz samples and shifts the data bits.by the time rising clock edge of 15MHz - 75MHz comes, all seven bits will be available at the outputs of seven D-Flip flops respectively and then clock all seven data bits with the rising edge of 15MHz - 75MHz clock.Here Negative edge triggered D-Flip flop is used to generate rising edge of sampling close to middle of the data period so that there won't be any setup and hold violations at the input of filp flops and there by synchronization to $\frac{1}{7}$th of the date rate happens properly.

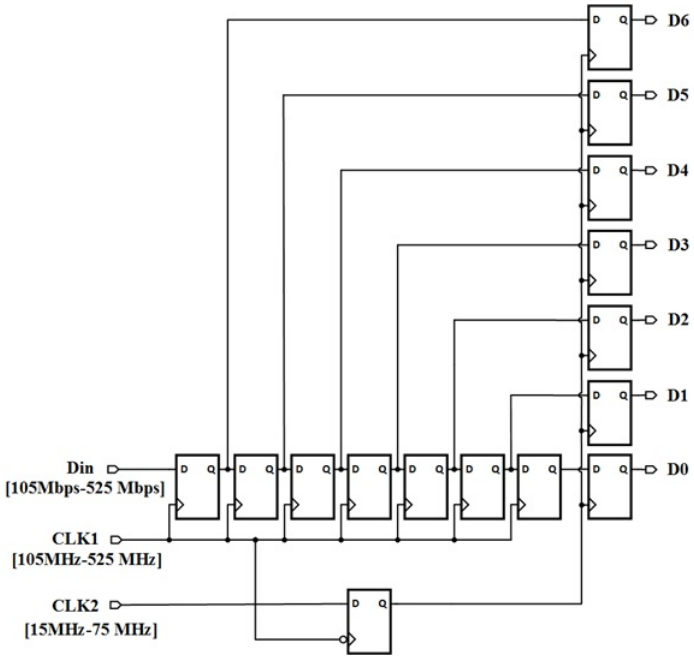

Figure 5.3: D-Flip flop based 1:7 Deserializer

This architecture doesn't need seven phases,which will be very difficult to generate over wide frequency range.

Note that D-Flip flops used in both the architectures are Sense-Amplifier based D-Flip flops as discussed in chapter 4.

CHAPTER 6

PHASE AND DATA RECOVERY UNIT ARCHITECTURES

6.1 General Description of PRU

It is important to process the received data properly to extract the information.Data is transmitted through channel in the form common mode voltage(V) and differential voltage swing(mV).Due to losses in the channel, small differential swing is received.Extraction of information can not be done without processing it further.Here comes the importance of detecting small differential swings after equalization and converting them to full swing voltage levels.to do this job, one has to sample the data of small differential swing.eye opening will be much smaller,if loss in channel is high.If sampling happens close to the center of the eye, better will be decision making and one can also avoid setup and hold violations.

A clock of frequency 15MHz - 75MHz is transmitted through fourth channel with the other three channels carrying data at 105MHz to 525MHz.It comes under forwarded clock architecture,where clock of required frequency 105MHz to 525MHz can be recovered from PLL.Clock recovery done by PLL is not enough,but to align it's phase to the center of the data period is important to sample the data.Alignment of sampling phase with respect to center of data period can be done by the circuity called 'Phase Recovery Unit'. some of the phase recovery techniques are listed below

6.2 VCDL Based PRU

It uses voltage controlled delay line(VCDL),whose input is a recovered clock from PLL and phase shift of this clock can happen by changing supply to delay line in feedback loop.Since data rates are 105MHz to 525MHz,delay line,whichshould wide tunable range from 2ns to 10ns approximately without duty cycle distortion,is difficult to implement.Hence this architecture can not be employed here.

6.3 PRPLL based PRU

This architecture decouples jitter transfer(JTRAN) bandwidth from jitter tolerence(JTOL) corner frequency, eliminates jitter peaking, and removes JTRAN dependence unlike phase interpolator(PI) based PRU. It also employs phase interpolation technique,but with with improved linearity. PRPLL based PRU consists BBPD, DLF, XOR gates with current weights, loop filter, and VCO as shown in figure 6.1

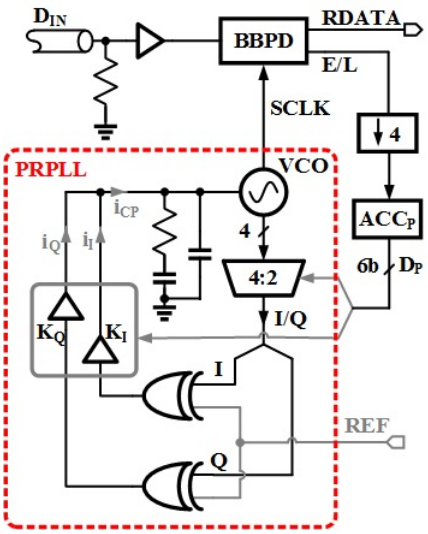

Figure 6.1: PRPLL based PRU

6.3.1 Bang-Bang Phase Detector(BBPD)

It is a nonlinear binary PD,which produces Early[DN] or Late[UP] signals depending on phase alignment of rising edge of sampling clock with respect to the center of bit period.If the rising edge of sampling clock is to the right from center of the bit period,It will produce Late[UP] pulse and vice versa.

It produces Early or Late pulses over full clock period and it only provides sign information of phase error.It takes two data samples and one edge sample, makes a comparison about the phase alignment and generates UP or DN pulses.Implementation of BBPD using D-Flip flops is shown in figure 6.2

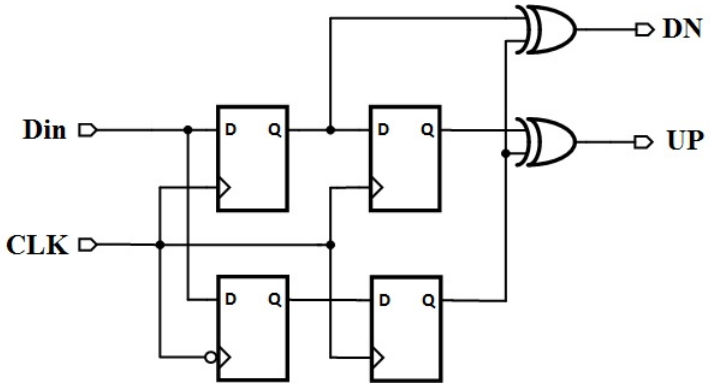

Figure 6.2: BBPD

D-Flip flops used above are sense amplifier based D-Flip flops.Since filp flops facing data stream have to resolve edge sample of very small differential swing and even data sample of small differential swing if channel losses are high, cascade of sense amplifiers followed by RS latch will be in the two flip flops and offset compensation is needed to make decision properly for small differential swings as shown in figure 6.3

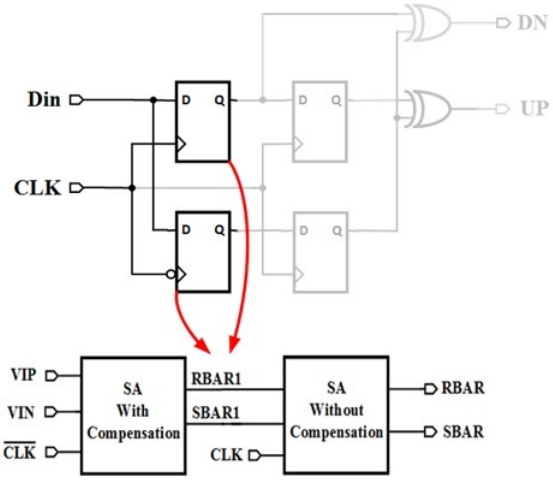

Figure 6.3: BBPD using D-Flip flops with offset compensation

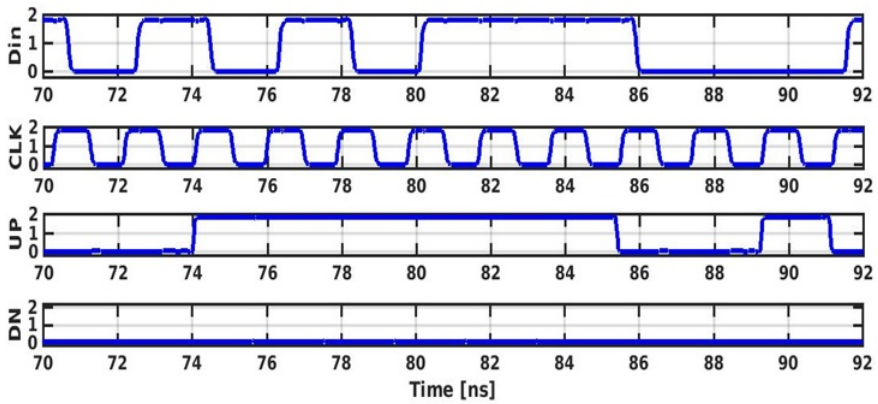

Figure 6.4: BBPD Output When Clock is Late

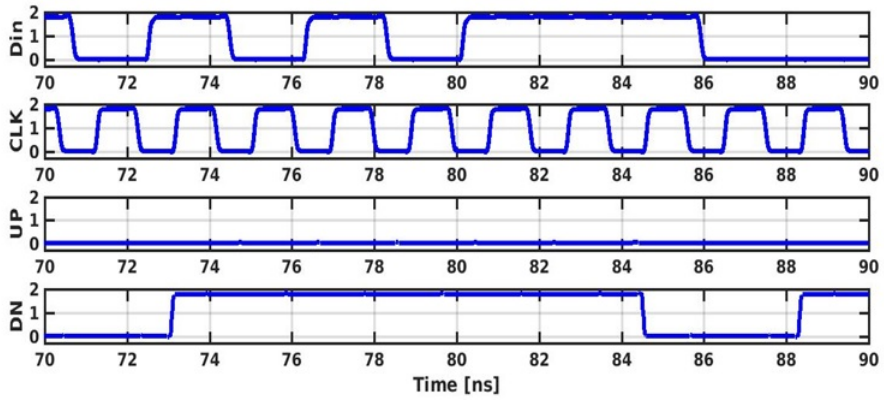

Figure 6.5: BBPD Output When Clock is Early

6.3.2 Phase Rotating PLL

PRPLL consists of XOR phase detectors and CP together with current weights, Loop filter, VCO.Design of PRPLL and it's small signal analysis is yet to done.

6.3.3 Digital Loop Filter(DLF)

Digital Loop Filter(DLF) is nothing but a Digital Accumulator,which will take BBPD's output,accumulate the values and generate digital code.MSBs of the digital code will be used to select two of four phases of VCO and remaining Digital bits (LSBs) will be used for current weights in combined (XOR-CP) unit.DLF implementation is yet to be done.

CHAPTER 7

SUMMARY AND FUTURE WORK

Summary:

Proposed forwarded clock receiver architecture has the following blocks namely equalizer,phase locked loop, phase recovery unit and deserializer.

Design of PLL with output frequency range [105MHz-525MHz] is done.

Design of 1:7 DFF based Deserializer is done.

Design of BBPD,which is a part of phase recovery unit is done.

Future Work:

Analysis and Design of PRPLL is to be done.

Design of Digital Loop Filter(DLF) is to be done.

Equalizer implementation at the front end of the receiver is to be done.

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