Wideband RF Transmitter in TSMC 65nm technology working from 100MHz to 12GHz

A THESIS

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KASYAP V KARUN

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THESIS CERTIFICATE

This is to certify that the thesis titled with **Wideband RF Transmitter in TSMC 65nm technology working from 100MHz to 12GHz,** submitted by **KASYAP V KARUN** to Indian Institute of Technology, MADRAS for the award of the degree of Master of Technology, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. S. Aniruddhan
Research Advisor
Associate Professor
Dept. of Electrical Engineering
IIT Madras

Place: Chennai

Date:

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ABSTRACT

KEYWORDS: RF Transmitter; IQ-Channel; Passive Mixer; Series peaking; Shunt peaking; Power Amplifier

The RF transmitters have been progressively implemented with different circuit topologies and with different supply voltages at different frequency bands. But the implementation of RF transmitter which can be flexibly used for different frequency bands are not yet available in the market and is the main motive of this work. The RF transmitter in this work comprises of four blocks namely Mixer, LO Buffer, Pre-PA and Power Amplifier (PA) stages. The parasitic components of the circuit and the chip package were the main limitations to further enhance the transmitter performance. The introduction of bandwidth extension using series and shunt peaking of the inductors helped to overcome the bandwidth limitations due to some of the parasitic components especially in passive IQ-mixer and in power amplifier. It has been clear that the implementation of the entire circuit in differential manner would enhance the removal of common mode noise and it would be better to choose the same rather than going for single ended topology. There were requirement of iteration between the schematic and layout twice to choose the presently designed circuit parameters.

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ABBREVIATIONS

PVT	Process, Voltage and Temperature
LO	Local Oscillator
IQ	In-Phase and Quadrature Phase
PA	Power Amplifier
BB	Base Band
R+C+Cc	Resistor + Capacitor + Coupling Capacitor

NOTATIONS

R_{on}	On-resistance
C_{dd}	Drain Capacitance
C_{ss}	Source Capacitance
C_{in}	Input Capacitance
ω_{BB}	Baseband channel Angular Frequency
ω_{LO}	LO Channel Angular Frequency
L_d	Inductance connected to Drain terminal
L_{mix}	Inductance in Mixer circuit
g_{mp}	Transconductance of PMOS
g_{mn}	Transconductance of NMOS
r_{dn}	Drain to source small signal resistance of NMOS
r_{dp}	Drain to source small signal resistance of PMOS

CHAPTER 1

Introduction

The advancement in high frequency analog circuit design has enabled the communication field to be elevated to such an extent where the data transmission speed increases day by day. As the technology is getting scaled down to even nanometer scale, the area of the chip is also being scaled down. The need of high frequency transmission in devices like mobile phones led to the design of high frequency analog circuits. The performance of these circuits has to be tolerant to the PVT variations since it requires to be operated under wide range of temperature and voltage depending upon the external and internal effects on the devices. There are mainly two categories of circuits in a mobile communication system, namely

- Transmitter Section
- Receiver Section

Both of these together assembled in a device is termed to be transceiver section. A low pass message signal is modulated with a high frequency carrier signal and is amplified using a power amplifier to deliver as maximum power as possible to the transmitter antenna. The transmitter antenna whose impedance is equal to the intrinsic impedance of air is considered as the load of the power amplifier.

As the requirement of voltage gain increases, this leads to increased physical width requirement for the transistors and hence increased parasitic capacitance for the transistors. Increased parasitic effects lead to reduced band width limitations which may raise concerns over the performance of the circuit at higher frequency. Most of

the available Mixers and Power Amplifiers in the market are of narrow band limited and hence lead to changing the circuits once the frequency of operation is shifted. The band width of the mixer and the power amplifiers have to be increased using some band width extension technique such as series peaking and shunt peaking using inductors.

There are mainly two types of up/down conversion mixer topologies namely;

- Passive Mixer
- Active Mixer

The passive mixer does not have any amplifying portion in it but has better linearity and IIP3 values compared to active mixers consisting of an intrinsic amplifier in it. So the passive mixer is used usually wherever the linearity of the mixer matters superior to its voltage conversion gain.

The RF power amplifiers are available in the market for a very long time and have been targeted for mobile handsets due to its small size and less power dissipation. The power amplifiers are classified into multiple categories based on the conduction angle of the transistors in the power amplifier. Some of these are given below;

- Class-A Power Amplifiers (Conduction Angle =360º)
- Class-B Power Amplifiers (Conduction Angle =180º)
- Class-AB Power Amplifiers (180º < Conduction Angle < 360º)

The class-A power amplifiers can have a maximum power efficiency of 50% due to its intrinsic limitations but they have high fidelity due to 360º conduction angle. They are best suited for highly linear transmitter systems.

1.1 Prior Work

There are circuits available with narrow band width for the application of specific bands but those cannot be used for out of band applications due to the presence of either resonant circuits or parasitic components. The double balanced passive IQ-mixer was designed with an IIP3 value of 2dBm and 1dB compression point of -12dBm in CMOS 180nm technology [1].

Some Bluetooth Low Energy (BLE) systems (2017) used some novel form of passive IQ-mixer in the receiver to achieve higher 1dB compression point at the cost of increased number of transistors and hence at the cost of increased chip area. The mixer switches consists of both NMOS and PMOS in this one [2].

1.2 Our Contribution

We meant to obtain a wideband passive IQ-mixer and wideband power amplifier cum IQ-adder which works from 100MHz to 12GHz frequencies. The mixer is voltage mode passive IQ-mixer with quadrature phase shifted differential LO signals used to up convert the baseband signal to RF frequency. The mixer switches are made of NMOS and there is need of an LO buffer to drive the LO signals to the gate of the NMOS switches in the mixer. The parasitic effects of the NMOS switch and the subsequent stage limit the bandwidth of mixer to below 12GHz and has to be compensated using a series peaking inductor at each differential branches of I and Q counterparts of the mixer.

The IQ adder and power amplifier portions of the circuit are incorporated together to form a single circuit section with four bottom transistors to which the differential I and Q signals from the mixer is connected and two cascade transistors, each one connected

to the respective differential half. The adder cum PA section is biased using an external bias-tee which enables us to get maximum voltage swing at the drain of the cascoded transistors in the PA. The outputs from the bias-tees are then connected to the balun whose output is connected to the load antenna. It is expected to have 2-3dB loss from bias-tee and the balun each. This results in reduced output power in the antenna.

We used the bandwidth extension technique using inductor (both series peaking and shunt peaking) to improve the bandwidth of the mixer and the LO buffer. The IQ-adder cum PA section is designed such that its 3dB band width is much higher than 12GHz.

Three matching networks are required in the circuit, one at the input of the LO buffer, one in between the drain of cascoded transistor in the PA and the bias-tee and the third one is in between the bias-tee and the balun. The matching networks cannot be wideband from 100MHz to 12GHz and has to be replaced with new components depending upon the frequency of operation. The matching networks are off-chip and are flexible to undergo the changes as expected.

1.3 Outline of the thesis

The remainder of the thesis is organized as follows. Chapter 2 is focused on the general block diagram, the bias-tee and balun used and the type of package model used at some specific nodes. The chapter 3 is focused on the passive IQ-mixer topology, design procedure, possible limitations and its solutions. This chapter describes about the inductor series peaking concept to improve the bandwidth of the passive IQ-mixer. Chapter 4 deals with the topology and design procedure of the LO buffer along with the possible limitations and its solutions. The design procedure and significance of the self-biased inverter used as the pre-PA stage is given in Chapter 5. Chapter 6 is mainly

concentrated on the IQ-adder cum PA portion. It describes the topology and design procedure along with the drawbacks. We conclude the remarks and possible extension in our work in Chapter 7.

Chapter 2

Full Block Diagram and Off-Chip Components

This chapter describes about the off-chip components used including the off-chip matching networks. Section 2.1 deals with the description of in-built off-chip components used which were already available in the market and the topology of the matching networks used for input matching of LO buffer and for the output matching of power amplifier, both are crucial for proper working of the full transmitter section.

Section 2.2 describes about the matching networks used for different frequencies of operations at different nodes. Some nodes requires low pass matching network itself for matching due to DC operating point restrictions. Section 2.3 consists of the explanation of the operation of on-chip components, its significance and the full block diagram of on-chip components.

2.1 In-Built Off-Chip Components

The focus in this chapter is on the full block level diagram and the description about the off-chip components. Fig 2.1 shows the block diagram including both the off-chip and on-chip components.

Since the frequency of operation is from 100MHz to 12GHz, it is needed to use wide band balun and wide band bias-tee to make the entire on-chip and off-chip blocks other than the matching networks to be wideband. It is not possible to design wideband matching networks from 100MHz to 12GHz since the more dominant component in the output or input impedance of some nodes are capacitive in nature. The Table-2.1 describes the specifications of the bias-tee used during schematic and layout simulations.

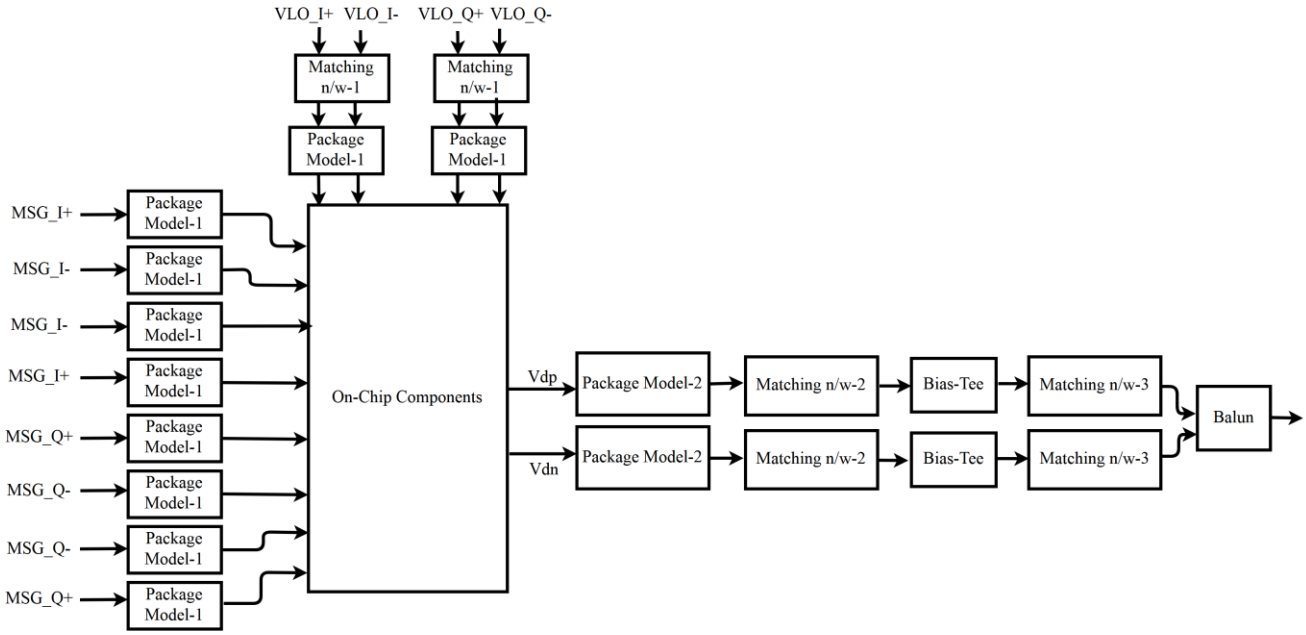

Fig 2.1: Full Block Diagram of the off-Chip components

Component	Frequency Range	Typical Insertion Loss	Typical Isolation	Maximum RF Power	Max Input DC Voltage	Max Input DC Current
TCBT-123+ from Mini Circuits	10MHz to 12GHz	0.8dB	15dB	30dBm	25V	200mA

Table-2.1: Specifications of Bias-tee used

Similarly, the Table-2.2 describes the specifications of the balun used during the simulation. Balun insertion loss has to be lesser similar to that in the case of bias-tee to obtain maximum possible modulated signal swing at the load antenna.

Component	Frequency Range	Typical Insertion Loss	Amplitude Balance	Phase Balance	Common Mode Rejection	Isolation
BAL-0026 from Marki microwave	300kHz to 26GHz	5.5dB	±0.5dB	±3º	30dB	24dB

Table-2.2: Specifications of the Balun used

2.2 Off-Chip Matching Network

The input nodes of LO buffer is to be matched to 50Ω single ended and the output node of PA should be matched in such a way that the imaginary component in the output impedance of PA should be negative of the imaginary part of the impedance looking into the output package model from the on-chip components. The output impedance of the PA will be a large resistive part in parallel with a capacitive component. This will result in maximum power transfer from the PA output node to the off-chip part through the chip output package. There should be another matching network in between the balun and the bias-tee to make sure the impedance matching with the load antenna. The matching network-1 and matching network-3 can be either low pass or high pass but the matching network-2 has to be low pass strictly since this section has to pass DC current through it. The circuit diagram of the matching networks used at each location is given in Fig 2.2 and Fig 2.3. The matching network between the chip package and bias-tee has to pass DC signal through it, hence the low pass matching networks is chosen.

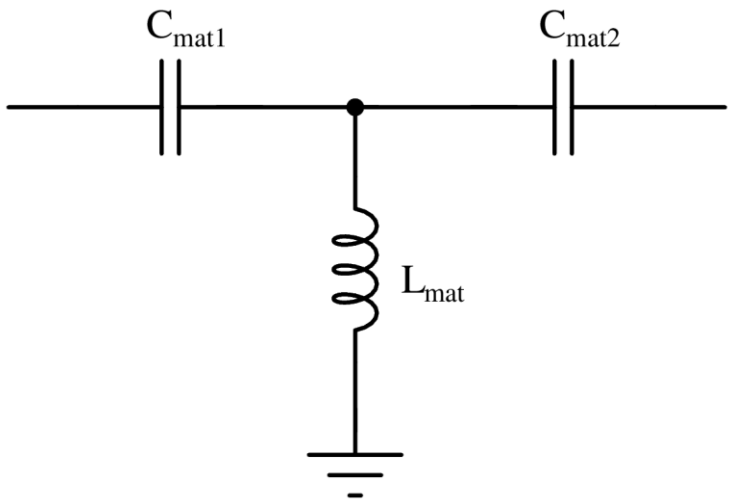

Fig 2.2: Circuit Diagram of High pass T-Matching network

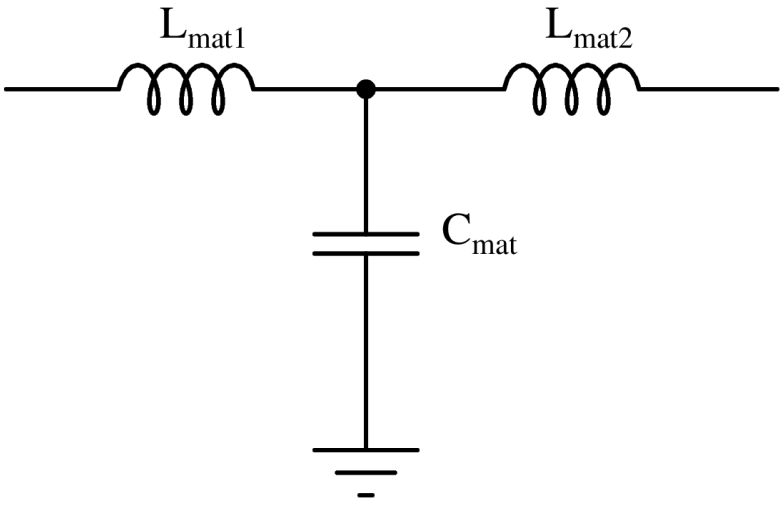

Fig 2.3: Circuit Diagram of Low pass T-Matching network

2.3 On-Chip Block Diagram

The on-chip part consists of a Passive IQ-Mixer, an LO Buffer to drive the mixer switches, Pre-PA stage in the form of self-biased inverter and the IQ-adder cum PA stage. The passive IQ-mixer consists of four differential branches, two differential I-

channels and two differential Q-channels which are driving the inputs of four self-biased inverters. The LO buffer is a differential single stage common source amplifier with an additional inductor in series with the drain resistors at each of the drain terminals. The LO buffer is also used twice, one for I-channel and the other for Q-channel. The Pre-PA stage is meant to relax the design constraints of the mixer due to the reduced input capacitance of the Pre-PA stage compared to the Adder cum PA stage. Reduced load capacitance for the mixer leads to reduced NMOS switch size for the same and in effect helps in reducing the size and bias current of the LO buffer. The Fig 2.4 depicts the full block diagram of the on-chip components involved in this project.

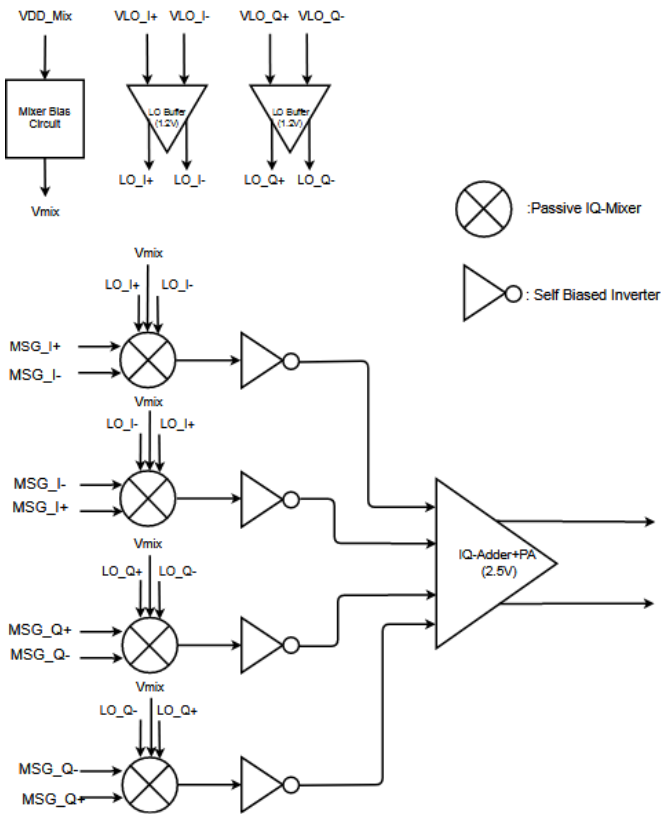

Fig 2.4: Full Block Diagram of On-chip components

Chapter 3

Voltage Mode Passive IQ-Mixer with series peaking Inductor for Bandwidth extension

This chapter briefly describes the topology and design procedure of the passive IQ-mixer initially. The passive IQ-mixer is modeled with passive components and ideal switches to theoretically explain its working and then the designing part comes. The possible limitations and its solutions are described in further sections.

Section 3.1 deals with introduction of the mixer topology and the modeling of the mixer with ideal resistor, ideal capacitor and ideal switch. The same section explains the theoretical voltage conversion gain and the mathematical basis of the modulation. Section 3.2 deals with the possible limitations to the mixer topology and its solutions. The usage of series peaking inductor is explained in the same section.

Section 3.3 discusses how the obtained mixer outputs as differential IQ-channel signals can be added together to get the actual mixer output. The detailed mathematical description of this part is included in this section.

Section 3.4 explains the design procedure and lists out the designed circuit parameters for the sake of better understanding of the mixer. The floor plan of the layout, the variation in the important parasitic component values between the schematic and layout extracted results and the fluctuations in the interested results are explained in section 3.5 with sufficient plots.

3.1 Circuit Topology and Passive Component Modeling

The passive IQ-mixer shown in Fig 3.1 has only one differential half of the four differential branches with two NMOS switches and two input bias resistors in each branch. Two of these differential branches belong to I-channel and the other two belong to the Q-channel.

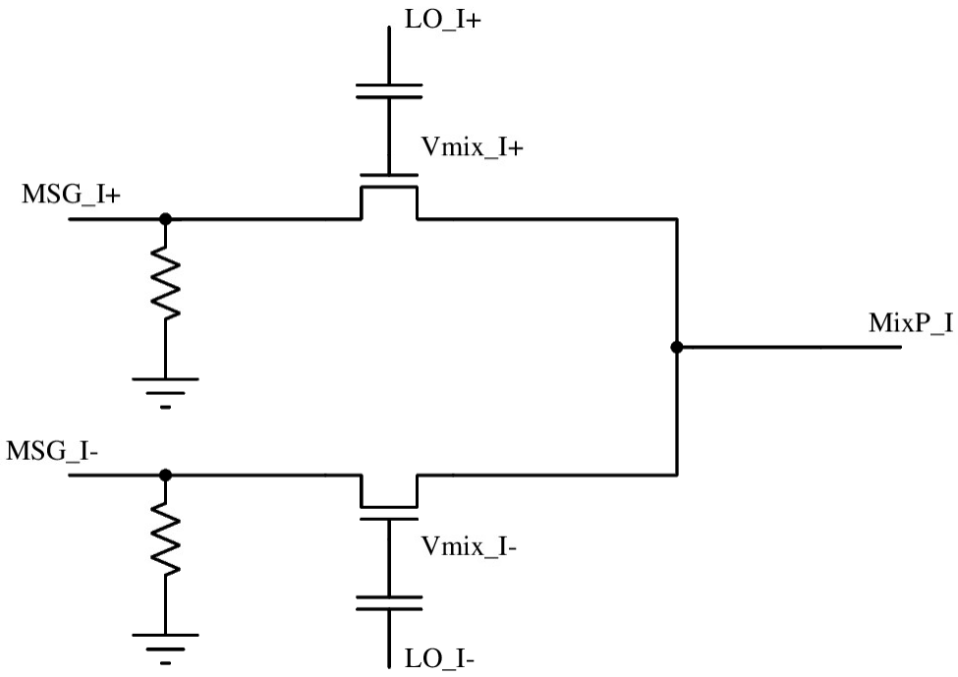

Fig 3.1: Circuit Diagram of Half Differential I-Channel of Passive IQ-Mixer

Since the mixer operation involves with frequencies up to 12GHz range, the parasitic components of the NMOS plays a vital role in deciding the 3dB band width of the mixer. Refer the Fig 3.2 which shows only the parasitic components involved in the mixer during its usual operation. The NMOS transistor is replaced with an ideal switch which is ON when the LO signal given to the gate terminal is high and is OFF when the LO signal a given to the gate terminal is low. The voltage levels for being called as high and low for LO signal are determined by the threshold voltage and the conductivity of the NMOS switch.

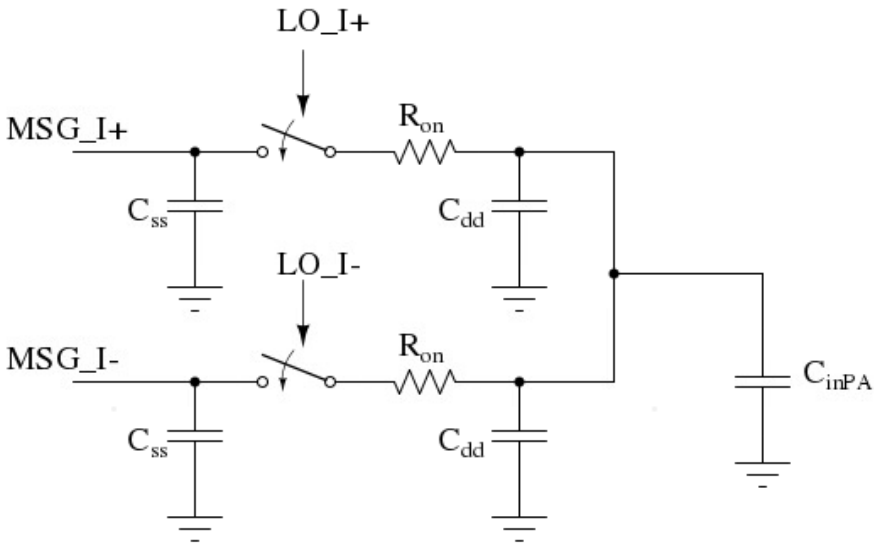

Fig 3.2: Diagram showing parasitic components involved in Mixer

The transfer function when the switch is ON and hence the 3dB band width of the mixer can be found out using the Fig 3.2. The voltage conversion gain (VC Gain) of the mixer with the parasitic effects incorporated is given in expression 3.1 [5].

$$\text{VC Gain} = \frac{2}{\pi} \times \frac{1}{SR(C_{in}+C_{dd})} \tag{3.1}$$

The 3dB band width of the 3rd order system is given in the below expression;

$$\text{3dB Band width} = \frac{1}{2\pi R(C_{in}+C_{dd})} \tag{3.2}$$

The voltage conversion gain versus frequency plot of the passive IQ-Mixer without the band width extension inductor is shown in Fig 3.3.

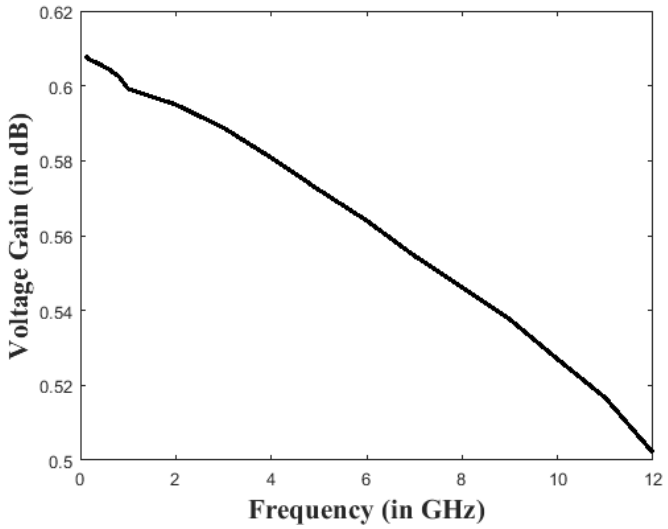

Fig 3.3: Voltage Conversion Gain v/s Frequency Plot of Mixer

3.2 Possible Limitations and its solutions

It is evident from the Fig 3.3 that the voltage conversion gain of the mixer reduces considerably due to the parasitic components involved. The input capacitance of the Power Amplifier plays a major role in it; this can be understood from the plot above. There is considerable decrease in the voltage conversion gain of the mixer at higher frequencies. The 3dB band width of the mixer is 14.5GHz only with this topology. This is enough for the proper operation of the mixer but this has to be as higher as possible to obtain almost constant output power dissipation in the full chain. Insertion of additional components to reduce the load capacitance of the mixer (here it's the input capacitance of the Power amplifier) is a possible solution to this limitation. The addition of inductor which provides additional positive imaginary component at the output of the mixer is a possible solution. The circuit diagram of one differential I-channel of the mixer will be updated to that in Fig 3.4 in order to accommodate the band width extension inductor in each of the differential branch [1].

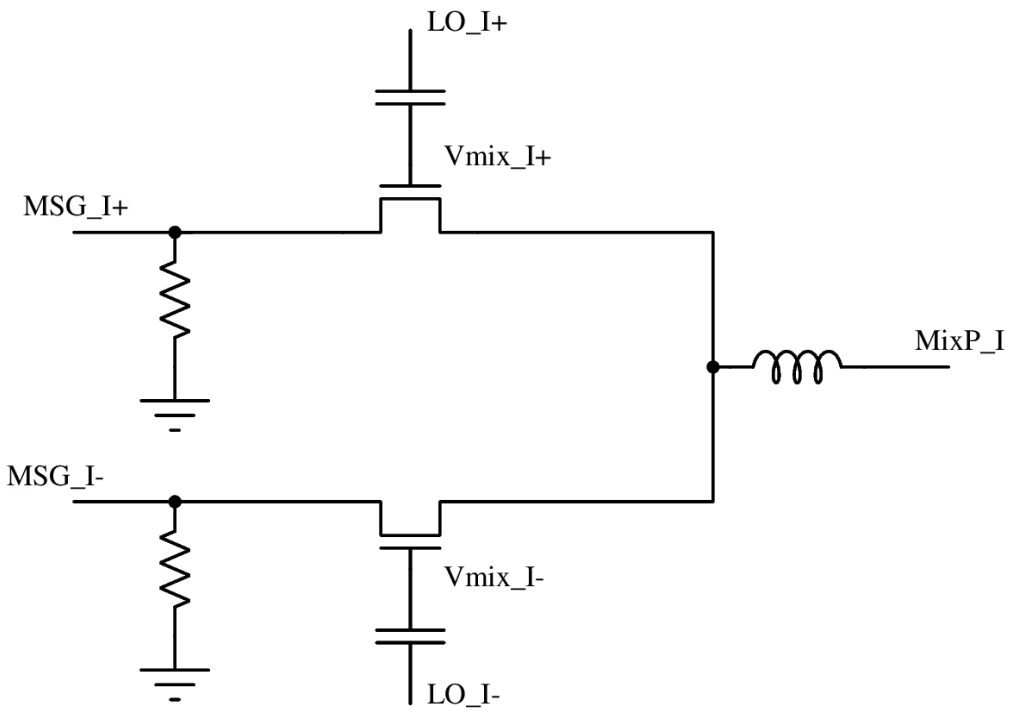

Fig 3.4: Single Differential I-Channel with Inductor

The inductor effect has to be considered now to find the new voltage conversion gain of the mixer. The circuit diagram in Fig 3.5 includes the parasitic components and the band width extension inductor of a single differential branch of I-channel of the mixer.

The voltage conversion gain of the passive IQ-mixer topology in Fig 3.4 is given in expression 3.3 and the updated 3dB band width in expression 3.4.

$$\text{VC Gain} = \frac{2}{\Pi} \times \frac{1}{s^3 LC_{in}C_{dd}R + s^2 LC_{in} + sLR(C_{in}+C_{dd}) + 1} \tag{3.3}$$

$$\text{3dB Band Width} = 1.41 \text{ x 3dB Bandwidth without BW Extension} \tag{3.4}$$

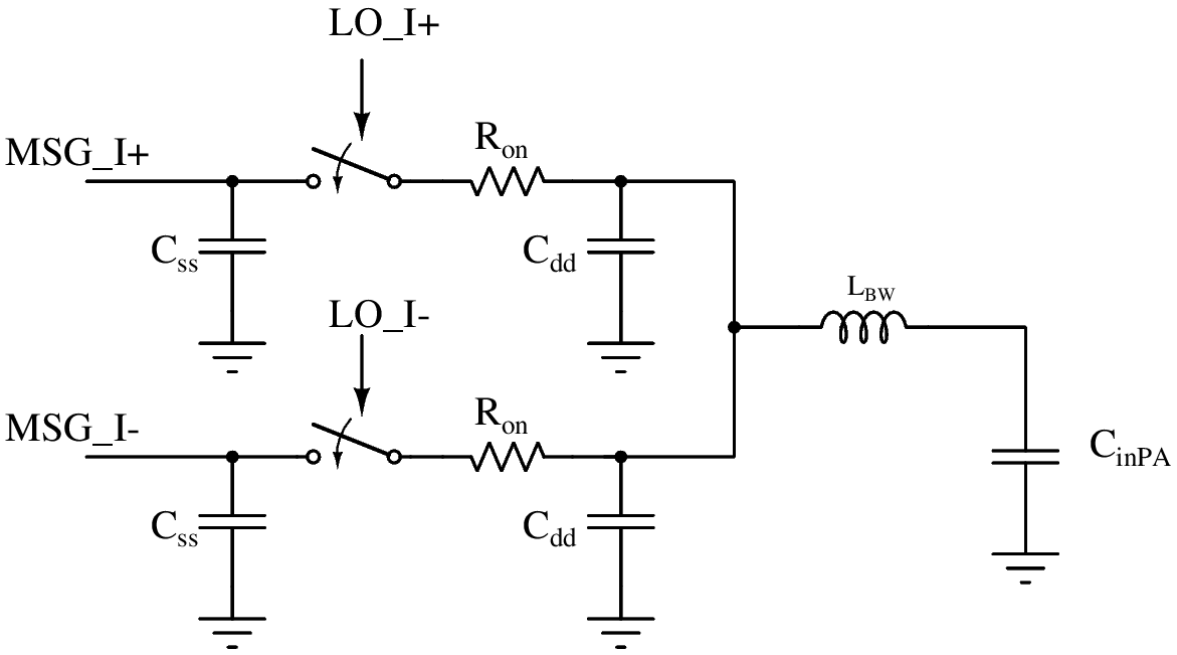

Fig 3.5: Mixer passive component representation with inductor

The insertion of inductor increases the bandwidth by 41% with the present ratio of the component values. The new voltage conversion gain versus frequency plot is shown in Fig 3.6.

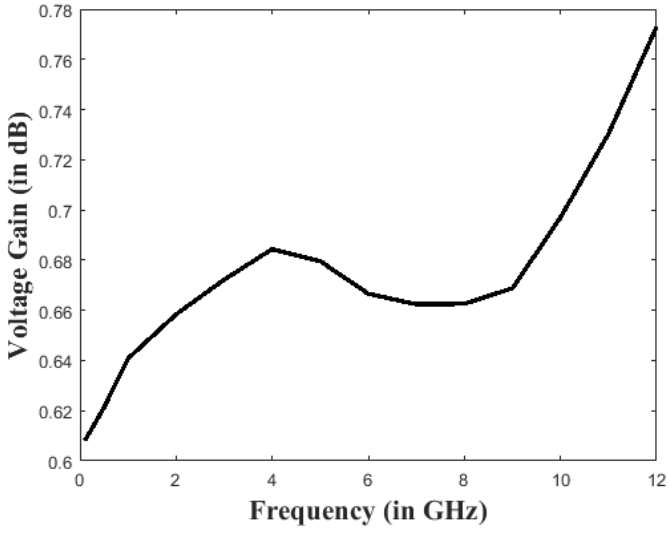

Fig 3.6: Voltage Conversion Gain v/s Frequency plot after the insertion of Inductor

3.3 Mathematical Basis of Operation

The full block diagram of the passive IQ-mixer is shown in Fig 3.7. It has four baseband input terminals (two for differential I-channel and two for differential Q-channel), four LO (Local Oscillator) input terminals and correspondingly four output terminals. Each of the mixer block gives a mixed output of both the RF signal (LO Signal) and the BB signal (Base band signal) but with each of them are spaced 90º apart in phase diagram. Since the given mixer is voltage mode mixer, there should be one transconductance stage after this to convert the output from voltage signal to current signal and the addition of these quadrature current signals can be easily achieved by shorting the desired nodes (Positive I-channel Output and positive Q-channel output have to be added together and similarly for negative I and Q channel signals) [3].

Let the voltage signals at each of the baseband nodes are given as below;

$$MSG\_I+ = A\cos(\omega_{BB}t),\ MSG\_I- = A\cos(\omega_{BB}t+180^{o})$$

$$MSG\_Q+ = A\cos(\omega_{BB}t+90^{o}),\ MSG\_Q- = A\cos(\omega_{BB}t+270^{o})$$

Similarly, the voltage signals at the LO nodes are given below;

$$LO\_I+ = B\cos(\omega_{LO}t),\ LO\_I- = B\cos(\omega_{LO}t+180^{o})$$

$$LO\_Q+ = B\cos(\omega_{LO}t+90^{o}),\ LO\_Q- = B\cos(\omega_{LO}t+270^{o})$$

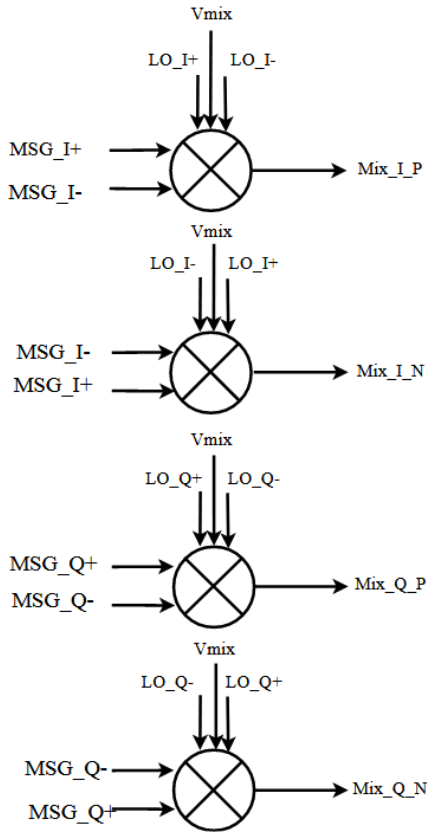

Fig 3.7: Full Block Diagram of Passive IQ-Mixer

The output voltage from the output node of the first mixer is given below;

$$Mix\_I\_P = [A\cos(\omega_{BB}t) \times B\cos(\omega_{LO}t)] + [A\cos(\omega_{BB}t+180^o) \times B\cos(\omega_{LO}t+180^o)]$$

$$= AB[\cos((\omega_{LO} - \omega_{BB})t) + \cos((\omega_{LO} + \omega_{BB})t)] \quad (3.5)$$

$$Mix\_I\_N = [A\cos(\omega_{BB}t+180^o) \times B\cos(\omega_{LO}t)] + [A\cos(\omega_{BB}t) \times B\cos(\omega_{LO}t+180^o)]$$

$$= AB[-\cos((\omega_{LO} - \omega_{BB})t) - \cos((\omega_{LO} + \omega_{BB})t)] \quad (3.6)$$

$$Mix\_Q\_P = [A\cos(\omega_{BB}t+90^o) \times B\cos(\omega_{LO}t+90^o)] + [A\cos(\omega_{BB}t+270^o) \times B\cos(\omega_{LO}t+270^o)]$$

$$= AB[\cos((\omega_{LO} - \omega_{BB})t) - \cos((\omega_{LO} + \omega_{BB})t)] \quad (3.7)$$

$$Mix\_Q\_N = [A\cos(\omega_{BB}t+270^o) \times B\cos(\omega_{LO}t+90^o)] + [A\cos(\omega_{BB}t+90^o) \times B\cos(\omega_{LO}t+270^o)]$$

$$= AB[-\cos((\omega_{LO} - \omega_{BB})t) + \cos((\omega_{LO} + \omega_{BB})t)] \quad (3.8)$$

The addition of the corresponding in-phase and quadrature components results in the following;

$$Mix\_I\_P + Mix\_Q\_P = ABcos((\omega_{LO} - \omega_{BB})t) \quad (3.9)$$

$$Mix\_I\_N + Mix\_Q\_N = -ABcos((\omega_{LO} - \omega_{BB})t) \quad (3.10)$$

3.4 Design Procedure

The design procedure is based on the fact that higher the width of transistor lower will be the mixer switch loss but higher will be the parasitic. The transistor width has to be lower in order to reduce the on-resistance of the transistor but the drain-bulk and drain-gate parasitic capacitance of the mixer will be increased correspondingly. This will result in reduced bandwidth. Hence transistor width has to be optimal in schematic which is found out via some wild assumption about the transistor parasitic and varying the transistor width in simulation once the required 3dB band width and voltage conversion gain are obtained.

Parameter	Value
Switch Width	40μm
C_{gg}	70.5fF
C_{dd}	31.5fF
On- Resistance (dc Analysis)	67.9Ω
Physical R at i/p	150Ω
BW Extension Inductor	1.03nH
Load Capacitance	98.7fF
Simulated 3dB BW without Inductor	15.5GHz
Theoretical 3dB BW with Inductor	21.7GHz
Simulated 3dB BW with Inductor (in Layout)	16.4GHz

Table-3.1: Circuit Parameters of the Mixer

3.5 Layout and Extracted Results

The screenshot of the entire mixer layout is shown in Fig 3.8. The layout has to be symmetrical since the circuit itself is differential. The large size of band width extension inductors used limits the layout area to a considerably larger minimum value.

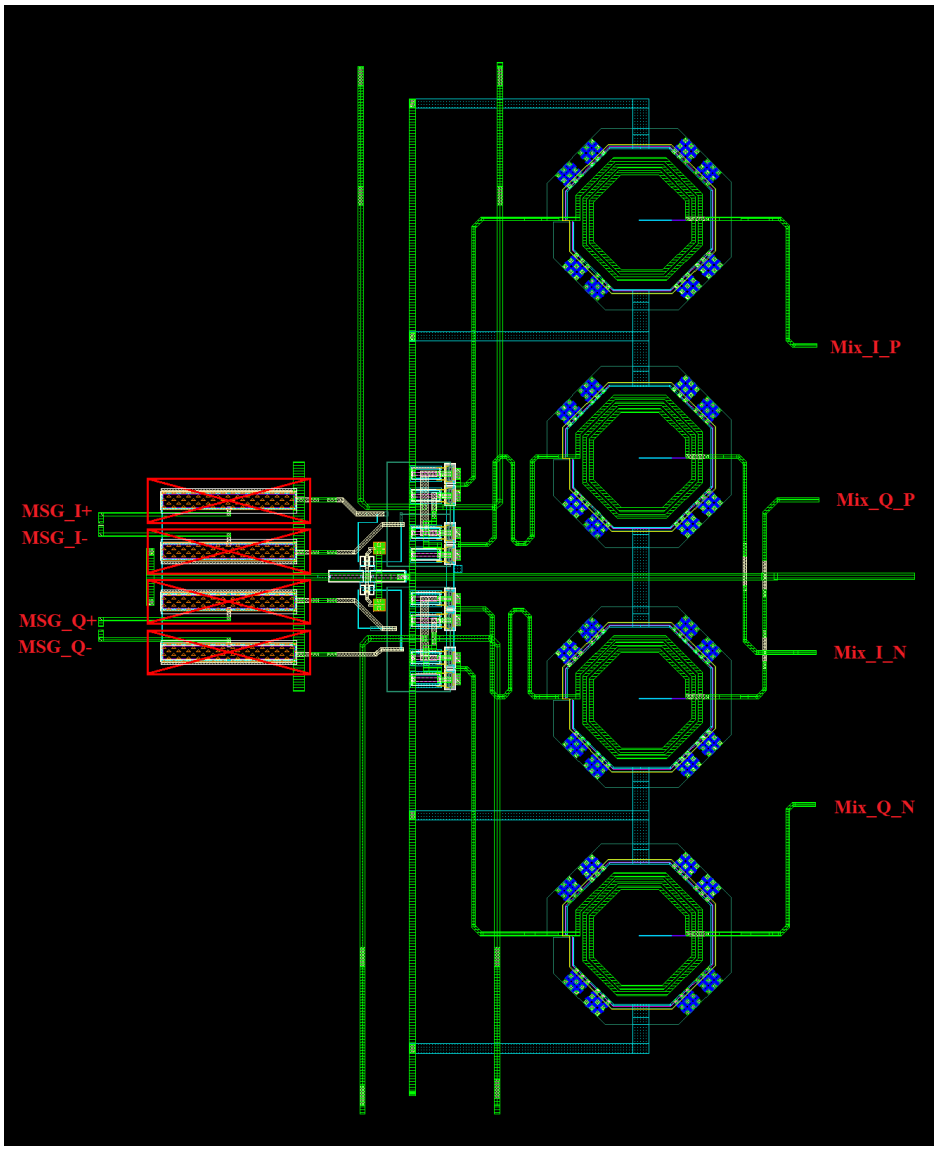

Fig 3.8: Layout of the Passive IQ-Mixer

The R+C+Cc extracted results of layout shows some significance difference in the mixer performance and the mixer switch size and the inductor values are iterated between layout and schematic to reach the final designed values. The comparison of parasitic capacitance values of the mixer nodes in schematic and in layout are given in Table-3.2.

Node	**Schematic**	**Only C**	**Only C_C**	**C+C_C**
MSG_I+	30.2fF	9.1fF	36.3fF	45.4fF
MSG_I-	30.2fF	8.1fF	33.6fF	41.7fF
MSG_Q+	30.2fF	9fF	37.5fF	46.5fF
MSG_Q-	30.2fF	8.1fF	34.1fF	42.2fF
Gate_I+	70.5fF	44.2fF	60.9fF	105.1fF
Gate_I-	70.5fF	35.7fF	62.6fF	98.3fF
Gate_Q+	70.5fF	43.7fF	65fF	108.7fF
Gate_Q-	70.5fF	38fF	60.4fF	98.4fF
Drain_I+	31.7fF	30.9fF	26.9fF	57.8fF
Drain_I-	31.7fF	17.4fF	25.7fF	43.1fF
Drain_Q+	31.7fF	17.4fF	25.7fF	43.1fF
Drain_Q-	31.7fF	31fF	26.9fF	57.9fF

Table-3.2: Layout Extracted parasitic capacitance values

Chapter 4

LO Buffer with Shunt Peaking Inductor

This chapter briefly explains the LO buffer working in 1.2V supply voltage. The topology of LO buffer is simply a differential common source amplifier with an additional shunt peaking inductor at the drain terminals. The section 4.1 describes the LO buffer topology, its modeling with ideal passive components and ideal VCCS and the theoretical voltage gain and theoretical band width expression. The same section describes the effect of parasitic components in the LO buffer operation.

The section 4.2 is included with the design procedure and the designed circuit parameters of LO buffer. The description about the floor plan of layout, extracted results and comparison of R+C+C_C extracted results with the schematic results are given in section 4.3.

4.1 Circuit Topology and Modeling

The circuit shown in Fig 4.1 shows only I-channel LO buffer. One more LO buffer is there in Q-channel also. The topology is similar to a differential common source amplifier with an additional inductance in shunt peaking fashion to obtain higher bandwidth. The maximum frequency of operation will be 12GHz and the parasitic capacitance at the drain node of NMOS in each side will contribute to reduced gain of the circuit at higher frequencies. This can be overcome with the insertion of bandwidth extension inductors on each differential branch.

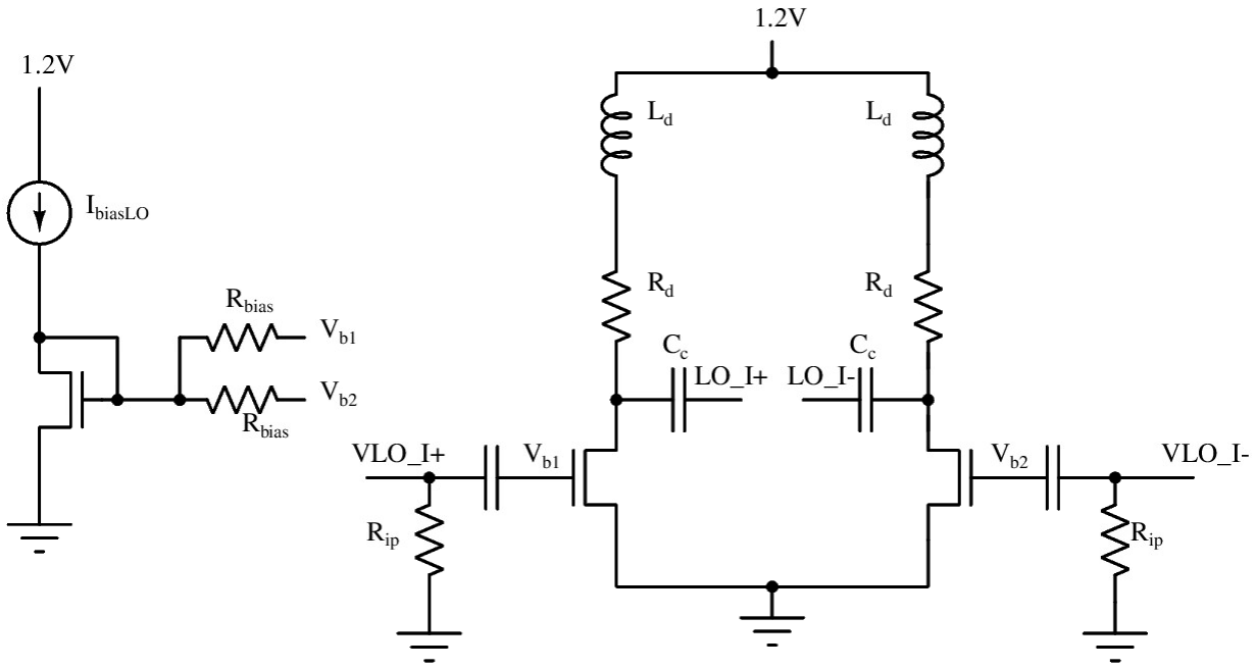

Fig 4.1: Circuit Diagram of I-Channel LO Buffer

The small signal diagram of one differential branch of the circuit is given in Fig 4.2 for better understanding of its operation.

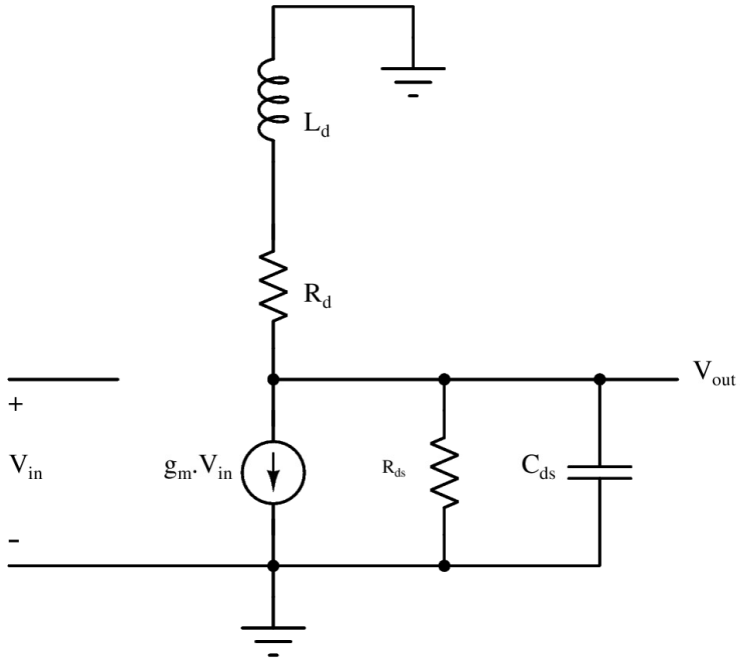

Fig 4.2: Small Signal Diagram of LO Buffer

The voltage gain (Av) and the 3dB bandwidth with and without the drain inductors are given in expressions from 4.1 to 4.3.

$$Av = -g_m[(R_d+j\omega L_d)\|(R_{on}+(1/j\omega C_{dd}))] \approx -g_m[(R_d+j\omega L_d)\|(1/j\omega C_{dd})] \quad (4.1)$$

If Drain inductor is not there; 3dB Band Width $= \frac{1}{2\pi R_d C_{dd}}$ (4.2)

The shunt peaking drain inductor can increase the bandwidth up to 1.4 times the original value.

$$\text{3dB Band Width after Band width extension} = \frac{1.4}{2\pi R_d C_{dd}} \quad (4.3)$$

4.2 Design Procedure and Simulated Results

The designed circuit parameters and some of the important simulation results of the LO buffer schematic are given in Table-4.1.

Parameter	**Value**
Transistor Width (W)	33.6µm
Drain Resistance (R_d)	39Ω
BW Extn. Inductor (L_d)	1.2nH
C_C	2.2pF
V_G	487.1mV
V_D	629.6mV
I_d per Half	19.6mA
G_m	134.6mS
C_{dd}	32fF
Simulated 3dB BW	32.9GHz

Table-4.1: Designed Parameters of LO Buffer in Schematic

The voltage gain v/s frequency plot of the LO buffer in schematic without the bandwidth extension inductor is given in Fig 4.3. The voltage gain at 100MHz is around 7.6dB and the 3dB bandwidth is around 28.4GHz.

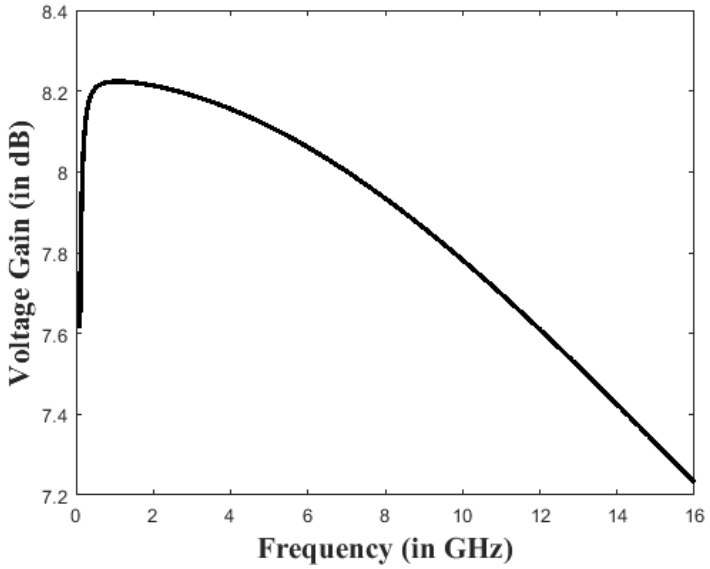

Fig 4.3: Voltage Gain v/s Freq plot of LO Buffer without BW Extension

The 3dB bandwidth of the LO buffer is already higher than 12GHz but it will be good if there is additional bandwidth extension in the LO buffer such that the degradation in mixer performance at higher frequencies be reduced drastically. The additional jump in the voltage gain of LO buffer in schematic at higher frequencies is shown below in the Fig 4.4.

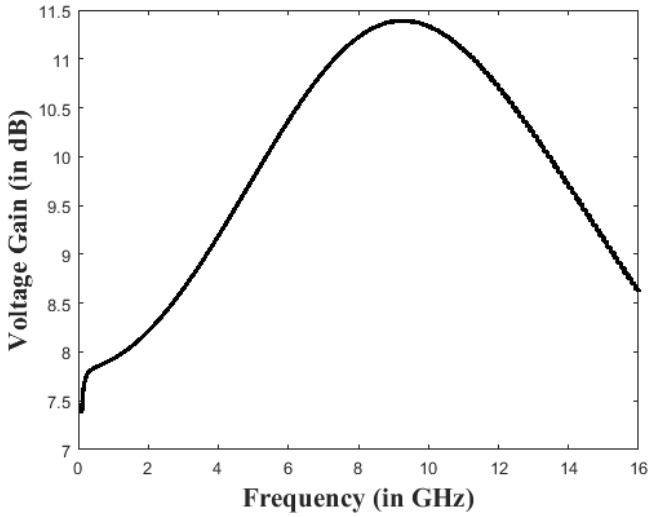

Fig 4.4: Voltage Gain v/s Freq plot of LO Buffer with BW Extension

4.3 Layout and Extracted Results

The layout of the differential LO buffer is shown in Fig 4.5.The layout has to be symmetrical similar to the mixer.

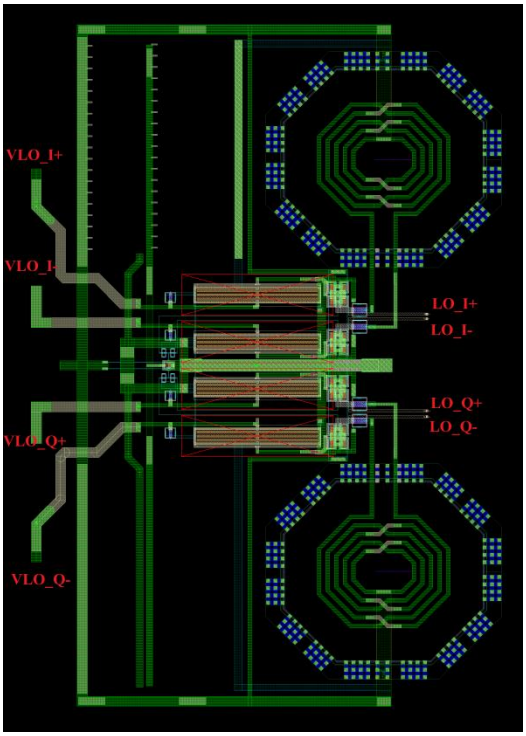

Fig 4.5: Layout of Differential I and Q-Channel LO Buffer

The R+C+C_C extracted voltage gain of the same LO buffer is shown in Fig 4.6. There is degradation in the bandwidth of the R+C+C_C extracted simulation results compared to that in the schematic simulation result.

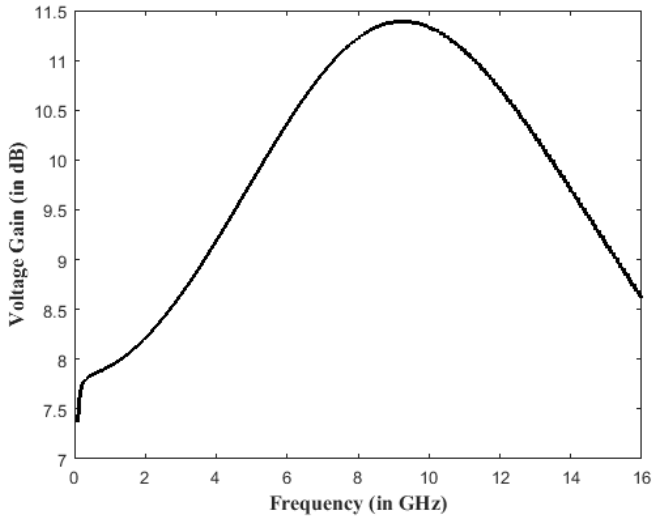

Fig 4.6: Voltage Gain v/s Freq plot of R+C+C_C extracted block of LO Buffer Layout

The comparison of some important results including the DC voltage gain, 3dB bandwidth and significant parasitic component values are given in Table-4.2.

Parameter	Value in Schematic without BW extension	Value in Schematic with BW extension	Value in R+C+Cc Extracted block
Voltage Gain at 100MHz	7.6dB	7.7dB	7.4dB
Drain Capacitance of Buffer NMOS	32fF	32fF	160.5fF
Gate Capacitance of Mixer Switch	70.5fF	70.5fF	179.2fF
Theoretical 3dB Bandwidth	28.8GHz	33.1GHz	16.8GHz
Simulated 3dB Bandwidth	28.4GHz	32.9GHz	16.7GHz

Table-4.2: Comparison of results in Schematic and Layout

Chapter 5

Self-Biased CMOS Inverter as Pre-PA Stage

This chapter explains the significance of a low gain Pre-PA stage, its circuit topology and its performance. This chapter includes two subsections. Section 5.1 describes about the circuit topology of the Pre-PA stage and its performance in the schematic simulations. The same section includes the theoretical calculation of voltage gain and 3dB bandwidth expressions and their estimated values.

Section 5.2 deals with the schematic simulation results of the Pre-PA stage and the difference in the mixer performance before and after the insertion of Pre-PA stage. The significance of Pre-PA stage in this transmitter design is described in the same section.

Section 5.3 is included with the floor plan of Pre-PA stage layout, information about the parasitic components at significant nodes along with the comparison of the schematic simulation results and the R+C+C_C extracted simulation results of the layout.

5.1 Circuit Topology and Modeling

The circuit diagram of the self-biased inverter used as Pre-PA block is shown with all the components in Fig 5.1. A resistor of large value is connected between the drain and gate terminals of both the NMOS and PMOS to bias the output node of the inverter. The parasitic capacitances at the drain node cum the input node of the subsequent stage (PA stage) are the main contributors to the band width degradation of the Pre-PA stage. The introduction of Pre-PA stage into the transmitter block is to relax the mixer design via replacing input capacitance of PA by the input capacitance of Pre-PA stage as the load capacitance of the mixer. So there is strict requirement of limiting the input

capacitance of self-biased inverter to at least half the value of the input capacitance of the Pre-PA stage.

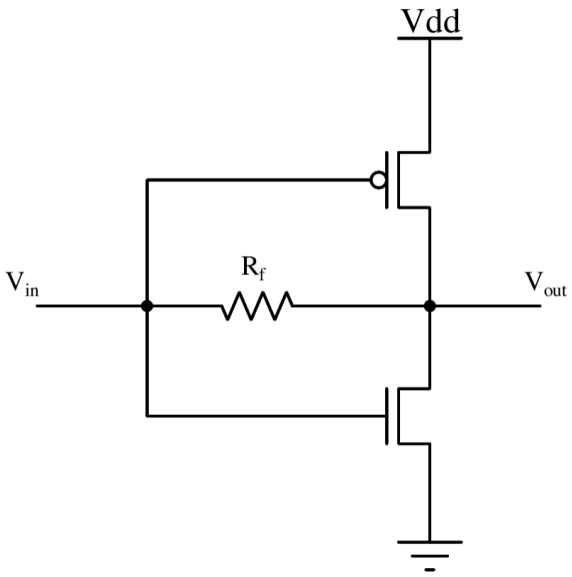

Fig 5.1: Circuit Diagram of Self-Biased Inverter

The small signal circuit diagram of the above self-biased inverter included with the significant parasitic components is given in Fig 5.2.

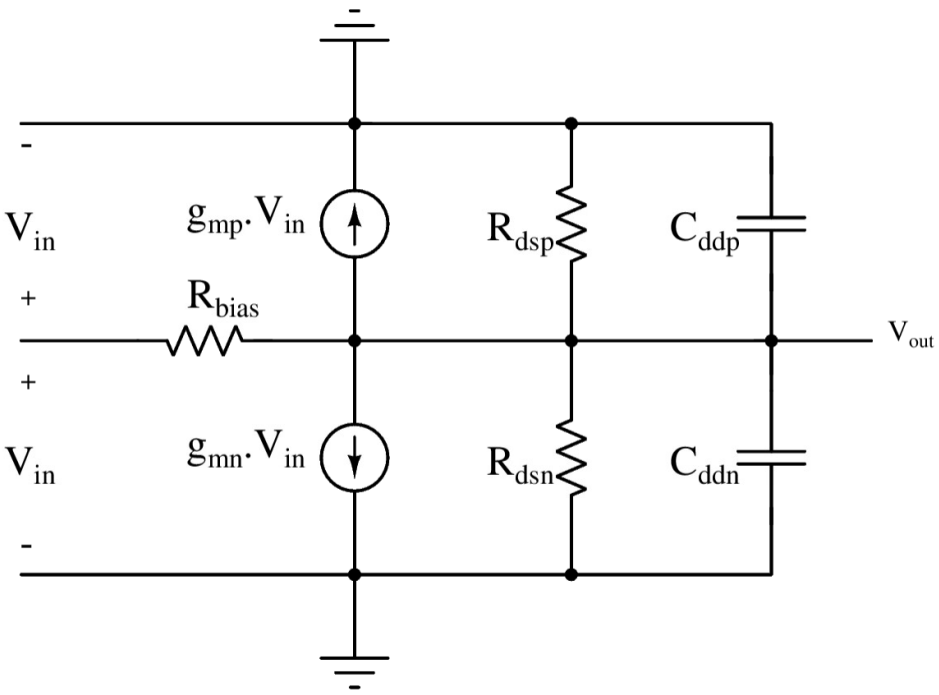

Fig 5.2: Small Signal Diagram of Self-Biased Inverter

There is an additional capacitance at the output node of the self-biased inverter other than those shown in the above figure. It is due to the gate capacitance of subsequent PA stage, which will be large enough to degrade the Pre-PA performance at higher frequencies.

Let the input capacitance of PA be C_{inPA} and the bias resistance connected between drain and gate are larger, then the voltage gain expression will be as given below in expression 5.1 and 5.2.

$$Av = -(g_{mp} + g_{mn}) [(r_{dn}||(1/j\omega C_{ddn}))||(r_{dp}||(1/j\omega C_{ddp}))||((1/j\omega C_{inPA}))] \quad (5.1)$$

$$Av \approx -(g_{mp} + g_{mn}) [(r_{dn}||r_{dp})||((1/j\omega C_{inPA}))] \quad (5.2)$$

The 3dB bandwidth is determined by the effective capacitance at the output node along with the effective drain resistance of both NMOS and PMOS. The 3dB bandwidth is given in expression 5.3.

$$\text{3dB Band Width} = \frac{1}{2\pi(r_{dn||}r_{dp})C_{inPA}} \quad (5.3)$$

5.2 Design Procedure and Simulation Results

The output node has to be biased exactly at half the supply voltage i.e. 600mV to get symmetrical output swing for symmetrical input signals. The NMOS and PMOS widths are designed such that the transconductance of both should be equal and the designed ratio of PMOS width to NMOS width came out to be 2.45:1.

The designed circuit parameters and some of the important simulation results of the self-biased inverter schematic are given in Table-5.1. All the values in the Table-5.1 are evaluated in the schematic of the full test bench, even the load capacitance is the input capacitance of the PA in its schematic.

Parameter	Value
NMOS Width	19.2µm
PMOS Width	47µm
R_{bias}	9.4kΩ
I_{bias}	4.1mA
C_{dd} of NMOS	4.5fF
C_{dd} of PMOS	11.6fF
r_{ds} of NMOS	285.3Ω
r_{ds} of PMOS	206.9Ω
Load Capacitance	166.7fF
Theoretical 3dB BW	7.26GHz
Simulated 3dB BW	5.65GHz
Low Frequency Voltage Gain	5.3dB
Theoretical 0dB Frequency	37.2GHz
Simulated 0dB Frequency	30.6GHz

Table-5.1: Designed Parameters of Self-Biased Inverter

The voltage gain versus frequency plot of the self-biased inverter is shown in Fig 5.3.

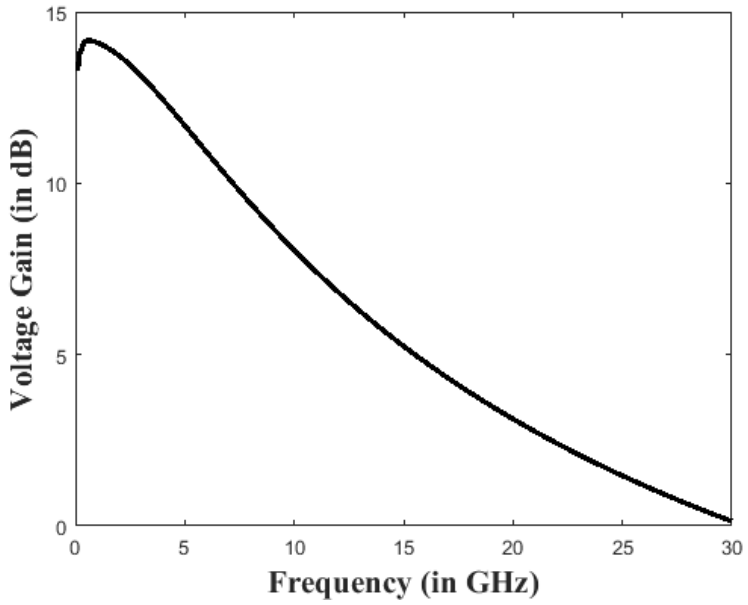

Fig 5.3: Voltage Gain v/s Freq Plot of Self Biased Inverter schematic

5.3 Layout and Extracted Results

The layout of the self-biased inverter is shown in Fig 5.4 below.

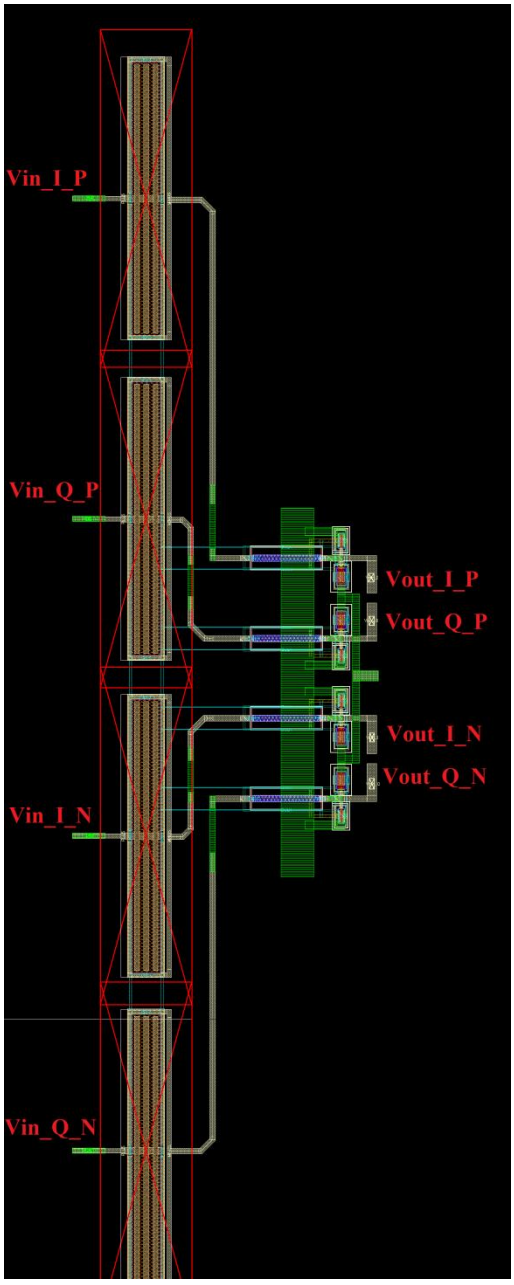

Fig 5.4: Layout of Pre-PA Stage including Self-Biased Inverters

The R+C+Cc extracted data of the self-biased inverter gives a Voltage gain versus frequency plot as shown in the Fig 5.5.

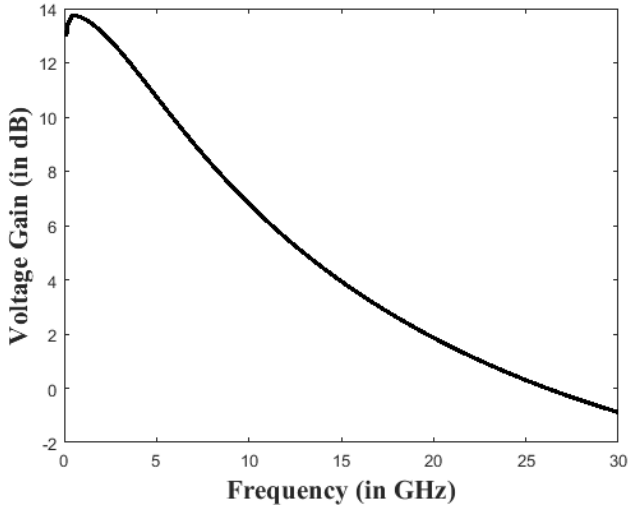

Fig 5.5: Voltage Gain v/s Freq plot of the Layout extracted block

The voltage gain of the self-biased inverter changed in such a way that the low frequency voltage gain remains almost same but the high frequency voltage gain reduced drastically from the schematic to the layout. The 3dB bandwidth is reduced from 5.65GHz to 4.98GHz and the 0dB frequency is also reduced from 30.6GHz to 26.2GHz in the layout compared to the schematic. These changes are enough to promise the required performance of the Pre-PA stage.

The comparison of some of the significant parasitic components between schematic and layout is given in Table-5.2.

Node	**C**	**C_C**	**$C+C_C$**	**Net**
MixP_I	19.7fF	54.8fF	74.5fF	94.2fF
Mixn_I	17.7fF	63.3fF	81fF	98.7fF
MixP_Q	18.4fF	60.3fF	78.7fF	97.1fF
Mixn_Q	19.8fF	54.8fF	74.6fF	94.4fF

Table-5.2: Input node parasitic components of Self-biased Inverter

Chapter 6

IQ-Adder + PA

This chapter is included with the detailed description about the final stage of the transmitter chain. The circuit topology, small signal diagram, bandwidth and voltage gain expressions and its derivations are explained in section 6.1. The section 6.2 deals with the important schematic simulation results of IQ-Adder+PA stage along with significant design criterion to be concerned with. Section 6.3 is included with the floor plan of layout; R+C+C_C extracted results and its comparison with schematic simulation results.

6.1 Circuit Topology and Modeling

The circuit diagram of the IQ-Adder+PA is shown in Fig 6.1. The bottom MOSFETs are used as a high gain device of the PA and the transconductance device for converting the voltage signal coming from the IQ-mixer through differential I and Q channels into corresponding current signals. The positive I channel and positive Q channel current signals are added together by shorting the corresponding NMOS drain terminals together.

The PA performance depends significantly upon the off chip bias-tee and balun used and the off-chip matching networks used. The output impedance of the PA depends largely on the drain capacitance of the cascoded NMOS and the matching network design will be difficult if the parasitic capacitance value is increased [4]. Hence it is very important to consider the additional parasitic effects coming from the layout into the schematic design.

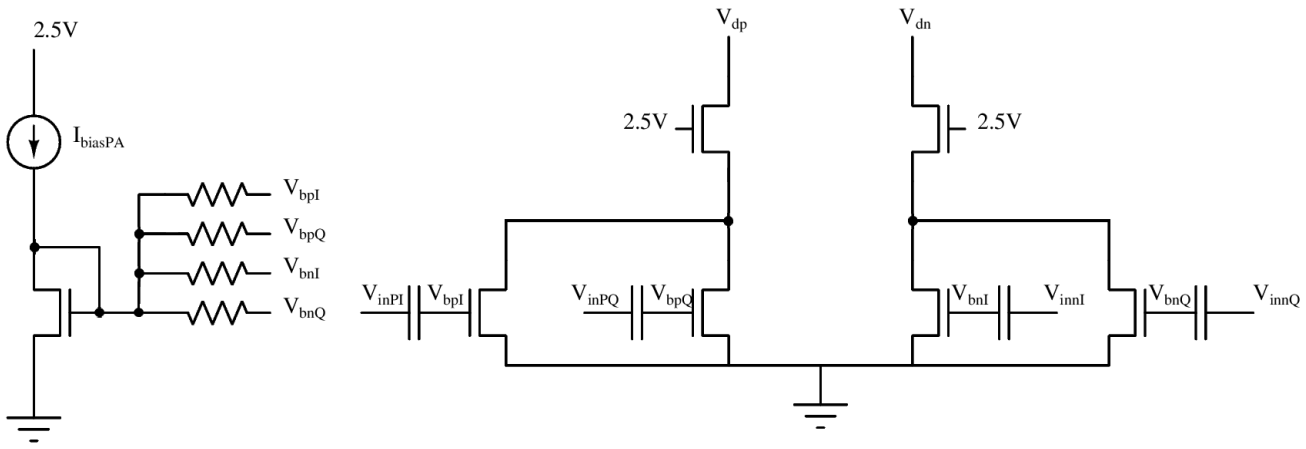

Fig 6.1: Circuit Topology of IQ-Adder+PA stage

The small signal diagram of one differential half is shown in Fig 6.2 below.

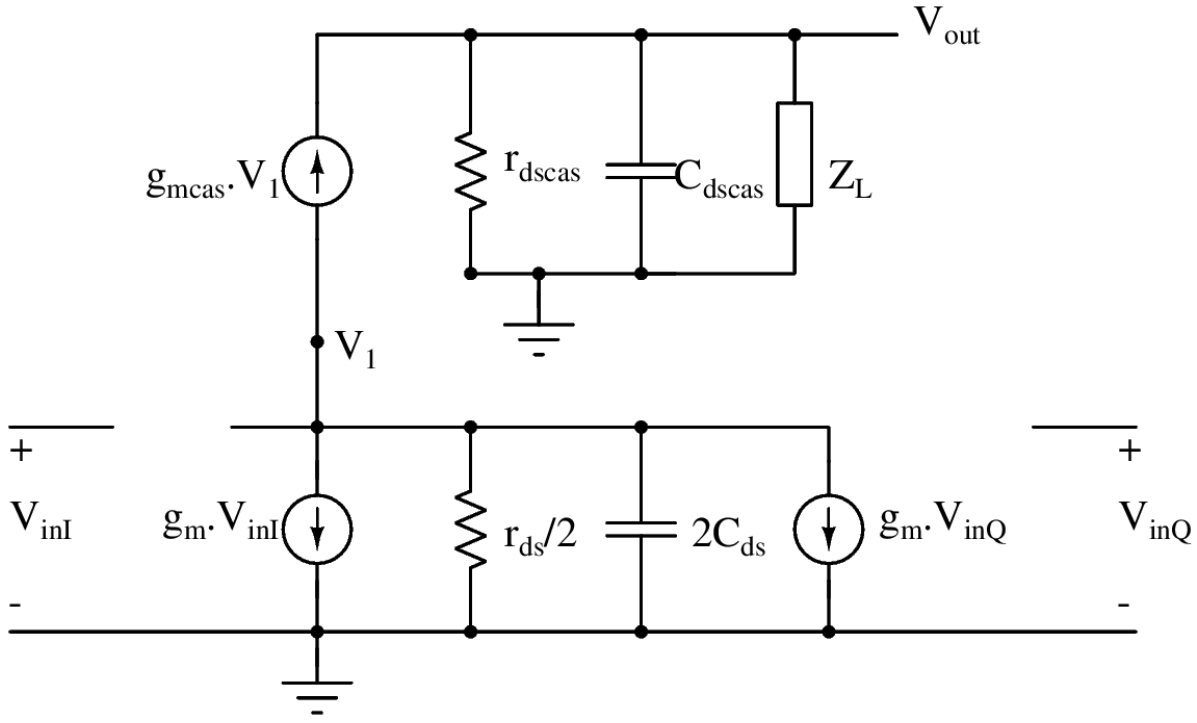

Fig 6.2: Small Signal Diagram of IQ-Adder+PA Stage

Z_L is the load impedance of the PA, which is nothing but the input impedance of the package model used looking from the PA output node. r_{ds} and C_{ds} are the parasitic components of the bottom NMOSs and r_{dscas} and C_{dscas} are that the cascoded NMOS.

$$\text{Output Impedance of PA, } Z_{out} = \frac{g_m \times g_{mcas}}{j\omega C_{dscas}} \quad (6.1)$$

$$\text{Voltage Gain, } Av = -g_m \times (Z_L \parallel Z_{out}) \quad (6.2)$$

Perfect matching between PA output and the antenna will make the load impedance (Z_L) of PA equal to 50Ω. Then, the 3dB bandwidth under this case will be as given in expression 6.3.

$$\text{3dB Band Width after Band width extension} = \frac{g_m \times g_{mcas}}{100\pi C_{dscas}} \quad (6.3)$$

6.2 Design Procedure and Simulation Results

The transistor widths are designed based on the required transconductance value and the gate bias voltages are taken in such a way that the 1dB compression point of the circuit is higher. The voltage gain and maximum deliverable output power are dependent upon the off-chip matching network design. The designed matching network components for different frequency of operation are given in Table-6.1. These values including the matching network component values will be different after the layout R+C+C_C extraction since these results are extremely dependent upon the drain parasitic capacitance of the cascoded NMOS.

Freq	Type	Component Values			O/P Refl Coeff (dB)	
		C_{mat1}	L_{mat}	C_{mat2}	Worst	Best
10.5GHz to 12GHz	3	679.2fF	407pH	---	-9dB	-20.9dB
9.2GHz to 10.5GHz	3	1.5pF	507pH	---	-9dB	-20.9dB
7.65GHz to 9.2GHz	3	20pF	637pH	---	-9dB	-12.5dB
6.5GHz to 7.85GHz	1	100pF	636pH	540fF	-9dB	-16.5dB
5.74GHz to 6.63GHz	1	200pF	853pH	342fF	-9dB	-30.4dB
4.92GHz to 5.74GHz	1	200pF	1.2nH	400fF	-9dB	-18.1dB
4.2GHz to 4.92GHz	2	---	1.6nH	402fF	-8.4dB	-19.3dB
3.55GHz to 4.2GHz	2	---	2nH	490fF	-8.3dB	-14.3dB
2.93GHz to 3.55GHz	2	---	2.9nH	412fF	-8.2dB	-26.2dB
2.44GHz to 2.95GHz	2	---	3.5nH	691fF	-8dB	-12.4dB
1.94GHz to 2.44GHz	2	---	5nH	741fF	-8.4dB	-16.4dB
1.54GHz to 1.94GHz	2	---	6.7nH	1pF	-8.6dB	-12.8dB
1.2GHz to 1.54GHz	2	---	9.7nH	1.2pF	-8.5dB	-15.3dB
930MHz to 1.2GHz	2	---	13nH	1.6pF	-8.5dB	-12.7dB
140MHz to 220MHz	1	12.3pF	90nH	11.9pF	-8.2dB	-9.5dB

Table-6.1: Output Matching network Component Values of PA

The output matching network design is extremely important in determining the voltage gain of the overall transmitter. The matching network types are chosen based upon the requirement of increased Q-factor in the design. The usual L-matching networks cannot vary its Q-factor at a particular frequency and hence some of the frequency ranges are satisfied with T-Matching networks.

Similarly the voltage gain and maximum deliverable output power values at room temperature and at typical process corner are given in Table-6.2.

f_{LO}	f_{msg}	Voltage Gain	P_{out_1dB}	Change in PM
200MHz	20MHz	23.1dB	10.7dBm	26.7º
600MHz	20MHz	21.2dB	10.5dBm	4.8º
900MHz	20MHz	19.9dB	13.6dBm	0.4º
2GHz	200MHz	18.4dB	13.2dBm	4.4º
4GHz	200MHz	16.7dB	14.2dBm	0.5º
7GHz	200MHz	15.4dB	13.9dBm	2.1º
10GHz	200MHz	14.3dB	10.9dBm	5.5º
12GHz	200MHz	13.5dB	13.2dBm	4.7º

Table-6.2: Performance of PA at different frequency of operation

6.3 Layout and Extracted Results

The floor plan of the PA without the decoupling capacitors is shown in Fig 6.3. The layout has been done in a symmetrical fashion.

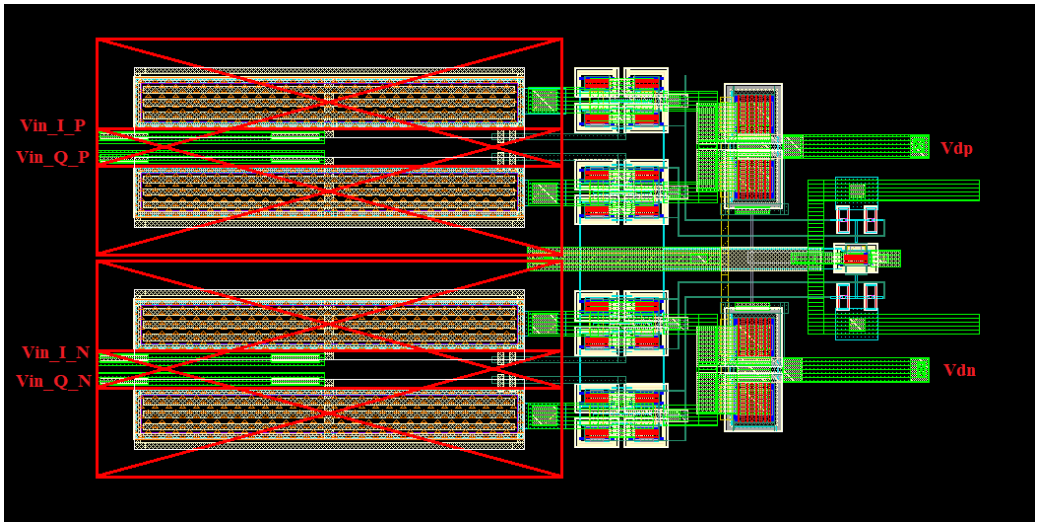

Fig 6.3: Full Layout of PA

The R+C+Cc extracted simulation results of the PA layout are given in Table-6.3.

f_{LO}	f_{msg}	Voltage Gain	P_{out_1dB}	Change in PM
200MHz	20MHz	21.1dB	12.36dBm	13.4º
600MHz	20MHz	19.6dB	11.72dBm	5.5º
2GHz	200MHz	17.1dB	12.47dBm	4.8º
7GHz	200MHz	15.2dB	12.77dBm	1.3º
10GHz	200MHz	12.3dB	11.88dBm	3.6º
12GHz	200MHz	11.7dB	12.04dBm	7.1º

Table-6.3: Simulation results of PA Calibre block

6.4 Full Transmitter Simulation Results

The 1dB output power compression point and net voltage gain were the circuit performance parameters concerned with. Refer Table-6.4 to understand the full transmitter simulation results after the R+C+C_C extraction of the full layout.

f_{LO}	f_{msg}	Change in PM	A_V at Low Pin	P_{in_1dB}	P_{out_1dB}
100MHz	20MHz	4.2º	25.6dB	-18.5dBm	6.1dBm
500MHz	20MHz	5.1º	25.5dB	-18.4dBm	6.1dBm
1GHz	200MHz	4.9º	24.4dB	-17.6dBm	5.8dBm
5GHz	200MHz	3.3º	16.5dB	-8.3dBm	5.1dBm
10GHz	200MHz	2.9º	16.6dB	-8.7dBm	4.9dBm
12GHz	200MHz	2.2º	8.9dB	-3.4dBm	4.5dBm

Table-6.4: Full Transmitter Calibre block Simulation Results

The overall power dissipation from each stage of the full transmitter is shown in Table-6.5.

Stage	Current per Branch	Supply Voltage	Net Power Dissipation
LO Buffer	18.6mA	1.2V	89.3mW
Pre-PA	8.3mA	1.2V	39.9mW
PA	123.5mA	2.5V	617.5mW
Overall	---	---	746.7mW

Table 6.5: Power dissipation in each stage of transmitter

The AM-AM plot and AM-PM plot of the full chain transmitter at different LO frequencies are shown from Fig 6.4 to Fig 6.15.

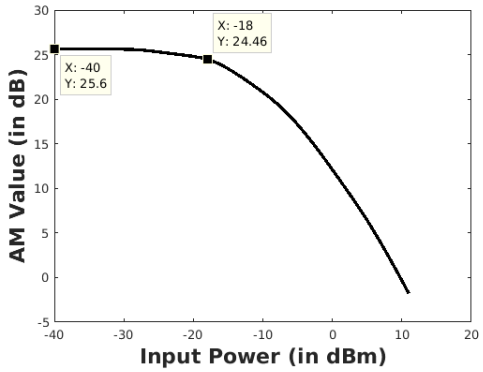

Fig 6.4: AM-AM Plot at f_{LO} = 100MHz

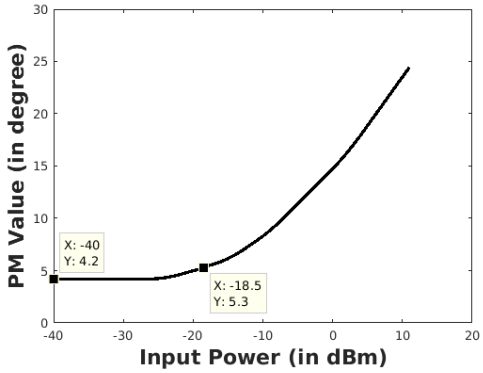

Fig 6.5: AM-PM Plot at f_{LO} = 100MHz

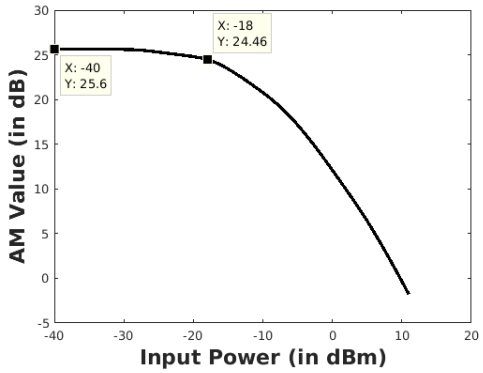

Fig 6.6: AM-AM Plot at f_{LO} = 500MHz

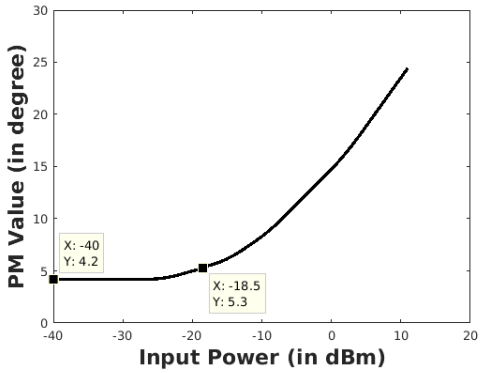

Fig 6.7: AM-PM Plot at f_{LO} = 500MHz

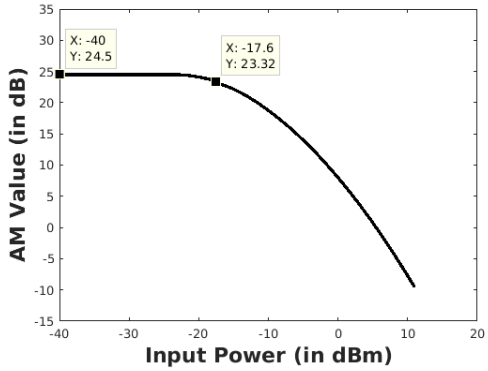

Fig 6.8: AM-AM Plot at f_{LO} = 1GHz

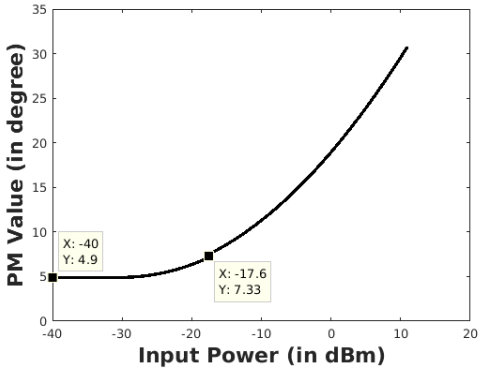

Fig 6.9: AM-PM Plot at f_{LO} = 1GHz

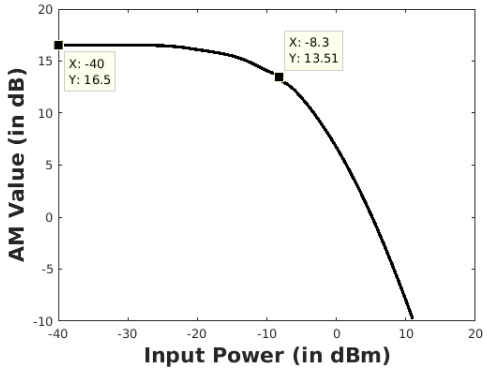

Fig 6.10: AM-AM Plot at f_{LO} = 5GHz

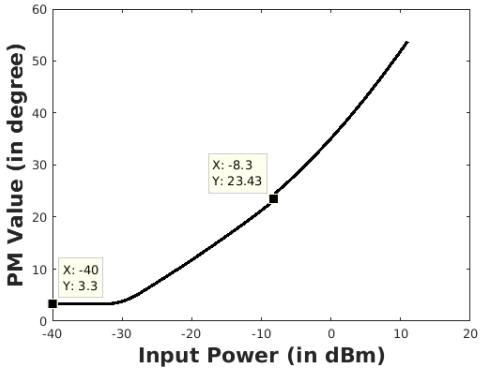

Fig 6.11: AM-PM Plot at f_{LO} = 5GHz

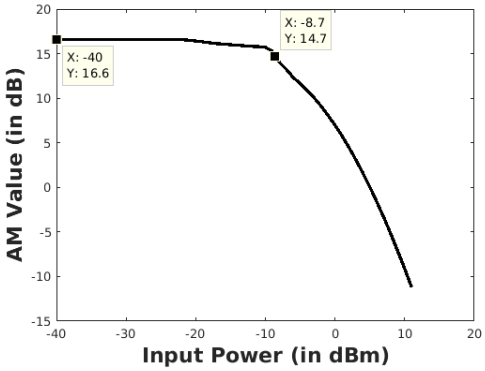

Fig 6.12: AM-AM Plot at f_{LO} = 10GHz

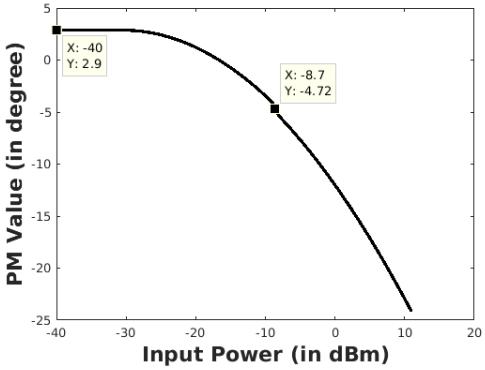

Fig 6.13: AM-PM Plot at f_{LO} = 10GHz

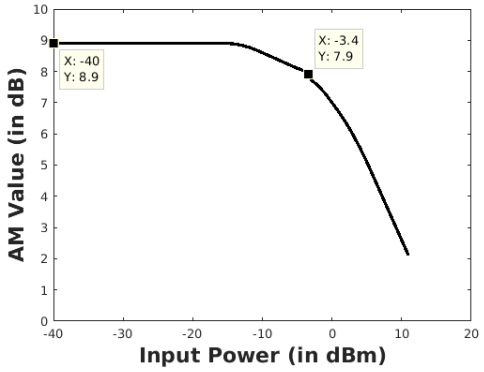

Fig 6.14: AM-AM Plot at f_{LO} = 12GHz

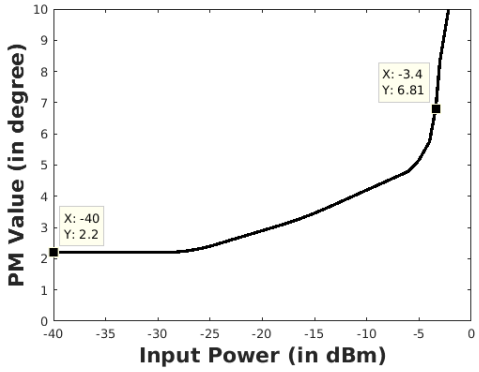

Fig 6.15: AM-PM Plot at f_{LO} = 12GHz

Chapter 7

Conclusion and Future Improvements

7.1 Concluding Remarks

Our work has been an effort developing a wideband RF transmitter so that the consumer can use it independent of the frequency band of their operation. We could overcome the issue of parasitic components which limits the wideband operation of several RF circuits. There has been availability of wideband off-chip components in the market for the consumer use but the RF on-chip components were always narrowband.

The bandwidth extension scheme [introduced in *Bandwidth Extension Techniques of CMOS Amplifiers* by *Sudip Shekhar, Jeffrey S. Walling, David J. Allstot* in 2006] using either shunt or series peaking inductors were useful in majority of the blocks in the transmitter. This scheme made us to improve the bandwidth by about 1.4 to 1.5 times in each block other than the Pre-PA stage.

7.2 Future Improvements

The I and Q components' addition is being done at the drain terminals of bottom transistors in the PA stage as of now. This can be shifted to the output terminal of the Pre-PA stage and thus the PA design will become more relaxed. This improvement will result in the removal of one of the bottom transistor in each differential half of the PA, so higher transconductance of bottom transistor and hence larger voltage gain can be obtained.

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