DYNAMIC VOLTAGE BALANCING OF SERIES CONNECTED SIC MOSFET'S

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THESIS CERTIFICATE

This is to certify that the thesis titled **DYNAMIC VOLTAGE BALANCING OF SERIES CONNECTED SIC MOSFET'S**, submitted by **Subin T (EE17M034)**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

There is no doubt regarding the advantages of SiC MOSFET over Si IGBTs. SiC MOSFETs can switch at high frequencies leading to compact power converters with very high power density. Faster switching results into overshoot and oscillations in the device voltage and current.This overshoot and oscillations deteriorate the EMI performance of the power converter, which requires large mitigation and control circuits for high voltage converters. So, in order to make smaller, compatible and efficient converter, high voltage rating devices are preferred. Since higher voltages SiC MOSFETs are at early stage of development and are not yet commercialised. Stacking the individual semiconductor devices is an effective way of reaching higher voltages. Due to restriction in availability of medium voltage SiC devices, stacking the individual semiconductor devices in series can be the possible solution towards taking advantages of the superior properties of SiC MOSFETs at higher voltages. With this topology, size and efficiency of the converters will improve significantly as compared to Si based high voltage converters.

In this thesis, the main issues and challenges of operating SiC power devices in series will be explored and common mitigation techniques will be discussed. In the topology, with passive external gate drives, two series connected SiC MOSFETs are synchronously driven. The v-i characteristics and switching characteristics were also studied. To Balance the dynamic or transient voltages, RC based Snubber circuits were introduced. Effect of external gate Resistance on transients voltage balance were also studied. Simulation for the same has been done in Pspice. Designed Passive gate drivers and Proposed voltage deviation mitigation circuits were tested in a Double Pulse (DP) test set-up with new SiC MOSFETs.

The device Drain voltage and current sensing circuits were also made and tested in hardware set-up and compared with actual voltage and simulated waveforms. Results for the same is also presented in work. Studies on mitigating the measurement error introduced in probes were also done and results were taken for the same.

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ABBREVIATIONS

CM	Common Mode
DP	Double Pulse
DUT	Device under Test
DSP	Digital Signal Processing
EMI	Electro Magnetic Interference
ESL	Equivalent series Inductances
ESR	Equivalent Series Resistance
FPGA	Field Programmable Gate Arrays
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PGD	Passive Gate Driver
RPS	Regulated Power Supply
SiC	Silicon Carbide
SOA	Safe Operating Area/Region
WBG	Wide Band Gap

NOTATION

C_{DS}	Drain to source capacitance, nF
C_{GD}	Gate to drain capacitance, nF
C_{GS}	Gate to source capacitance, nF
C_{iss}	Input capacitance, nF
C_{oss}	Output capacitance, nF
dv/dt	Device voltage slew rate, kV/μs
di/dt	Device current slew rate, kS/μs
D_f	Freewheeling Diode
E_{on}	Turn on switching loss, μJ
E_{off}	Turn off switching loss, μJ
g_{fs}	SiCFET transconductance, S
i_d	Drain current
i_l	Load current
i_{ch}	Channel current
i_g	Gate current
L_p	Power loop parasitic inductances, nH
L_{load}	Load inductance, nH
L_d	Drain side parasitic inductance, nH
L_s	Source side parasitic inductance, nH
L_g	Gate loop parasitic inductance, nH
L_{DC}	DC bus parasitic inductance, nH
$\mathbf{\Delta t}$	Time delay at gate driving pulse, ns
T_{on}	Total turn on time, s
T_{off}	Total turn off time, s
R_G	Gate resistance, Ω
V_d	Drain voltage, V
V_{gs}	gate to source voltage, V
V_{DC}	DC bus voltage, V
v_k	Kelvin voltage, V
v_{th}	Threshold voltage, V
v_{pl}	Plateau voltage, V
ζ	Damping factor

CHAPTER 1

INTRODUCTION

In laast ten years, WBG materials have been widely adopted in many power electronic devices. They have significant advantages over traditional Si device due to larger band gap and breakdown field. With the WBG material property, it is expected that WBG device will provide even higher breakdown voltage while maintaining the same size and on resistance in comparison to Si devices. This will significantly shrink the size of power devices and reduce the power loss resulting in higher efficiency of the converter. The new generation SiC MOSFETs comes with kelvin source, i.e, device has 4 terminals. These kelvin source and gate terminal will ensure the reduction in parasitic inductances in the gate loop of the device. The new SiC MOSFET has much lower on resistance, higher voltage-blocking capability, lower switching loss, lower gate ringing and higher temperature operation capability than both the Si MOSFET and the Si insulated gate bipolar transistor (IGBT). This makes SiC MOSFETs a promising alternatives for Si power devices for high voltage applications. It is also interesting to note that switching time of a SiC MOSFET has been shrunken at least five times compared to a Si IGBT of similar rating. It allows SiC MOSFET based converter to operate at switching frequency more than 20 kHz with good efficiency figures.

Despite of huge development in WBG materials, maximum voltage rating of commercially available SiC devices till now are 1.7 KV. Stacking the semiconductor devices in series/parallel combination would be better solution for compact, efficient high voltage power converters. Although parallel connection of MOSFET has been studied and used, series connection of multiple lower voltage device will increase the overall blocking voltage of SiC devices. The series connection is much more challenging due to static and dynamic voltage sharing. However key obstacles to the benefits of SiCFETs are high frequency oscillations and overshoot in the device voltage and current. This ringing and overshoot are caused by the L-C network formed between parasitic inductances contributed by the bus bar, PCB layout and device capacitances. These undesired oscillations in voltage and current generate stress in device at every switching instant. They also degrades EMI performance and efficiency of switching device and converter.

So it is necessary to provide voltage balancing circuits and controller to ensure the safe operation of device.

In this scenario, exploiting the benefits of SiC MOSFETs without sacrificing its switching speed (typically 50 to 60 ns) is a challenge. One of the solutions to this is active control of gate signal. A pulse shift delay logic and gate resistance based passive gate driving technique for a SiC MOSFET is designed.

1.1 Literature Review

Many studies on switching characteristics of SiC Devices, and effect of parasitics, common mode injection on driving SiC Devices have already been carried out. Several studies on these cases in series connection is still going on.

High voltage power converters need high voltage rated semiconductors. But we know the advantages of Silicon carbide semiconductors compared to Silicon semiconductors. Even though SiC MOSFETs development started long back in 1990's, availability of High voltage SiC MOSFETs are still unknown. [1-2]Some high voltage, low current SiC devices are available in research laboratories. They have the potential to significantly impact the system performance, size, weight, high-temperature reliability, and cost of next-generation energy conversion and transmission systems. Experimentally, these developed devices exhibits low switching losses at higher voltages when compared to commercially available 6.5kV Si MOSFET.

Literature [3-4] deals with the zero voltage switching (ZVS) characteristics of SiC N-IGBTs to reduce the dv/dt at switching pole along with reduction in the switching losses and increase in the switching frequency limits with external snubber capacitor. Experimental study proves that turn on and turn off dv/dt with external snubber reduced very much compared to without snubber.

A new topology power module with series and parallel connection of low voltage SiC MOSFET's has been reported in [5]. It uses a single gate driver which has capacitive coupling circuit to both devices gate terminal ensuring equal voltages at gate-source terminal. This results in an undesired sequential turn on/off process, i.e., device closer to gate driver will respond or commute first and furthest one in series connection will commute last. there fore the switching losses in devices will be unequal.

Literature [6] is continuation of reference [5] which also talks about speeding capacitors

in gate driver to reduce switching delays between devices, it does not improve the turn off process compared to turn on.

Active Voltage control(AVC) technique is introduced in [7] to ensure the dynamic and static voltage balancing of series connected IGBTs. Mismatched tail currents results in the device with the lower tail current charge supporting a higher voltage and incurring a higher switching loss. AVC is not effective in the tail current region since the device is no longer in the active region.

Article [8] deals with experimental study on RCD based snubber circuit and its effect on device loss. Inductance were added to make resonance and to avoid the effect of transformers in load side. Different drain side techniques or circuits were discussed in [10]-[12].

In series connection of IGBTs[13], the gate control circuits ensure better voltage balancing compared to active clamping and passive snubbers in terms of switching losses and commutation time. The number of IGBTs in a series string was optimized in terms of power losses. Significant power savings can be achieved by using lower rated IGBTs at higher frequencies and higher rated IGBTs at low frequencies.

Literature [14] proves gate resistance has little effect on switching loss and it is important to select snubber capacitor appropriately ensuring that both switching loss and voltage inequality minimizes or should be compromised.

Miller current injection to gate driving side is proposed in [15], which slow downs top device. BJT based miller circuit is used, this circuit needs to be tuned appropriately for achieving desired results, which is cumbersome.

Article[16] discuss about Gate driver design for device with fast switching rates considering the switching noise and common mode problems. dv/dt and di/dt based Protections circuits were designed.

A closed loop active delay control method with silicon delay line IC for series connected SiC MOSFET is proposed in [17].

Effect of common mode current in SiC MOSFETs were discussed in [18]. It proposes a predictive model to estimate these common mode currents. Furthermore,common mode current effect is studied by adding the common mode choke in AGD.

1.2 Organisation of Thesis

The Thesis is organised as follows:
Chapter 2 discuss the problems associated with SiC MOSFET implementation and solution to mitigate those problems.

Chapter 3 discusses the performance of various mitigation techniques to reduce the voltage deviation seen during series connection. The developed Passive gate driver(PGD) is tested in the Double Pulse(DP) test setup. Proposed sensing techniques were also tested in Simulation and results for the same are presented.

Chapter 4 briefs about hardware implementation and problems faced in hardware setup.

Chapter 5 reports the results obtained from simulation and hardware implementation of double pulse test setup. Reason for difference in sensed voltage and actual voltage were also discussed in this section.

Chapter 6 summarizes the thesis.

CHAPTER 2

CHALLENGES OF IMPLEMENTING SIC MOSFETS

2.1 Introduction

The SiC MOSFETs possess a variety of benefits compared to Si-IGBT's that make them ideal for applications which operates at high voltages, temperatures, and switching frequencies. However, many challenges present themselves due to circuit and device parasitic elements, and variations in the operating characteristics of the device. Even though there are some parasitic capacitance in PCB due to positioning of components, signal trace and ground trace. Parasitic inductances present in the converter layout are contributed by device packaging, board layout and ESL of DC bus capacitor. These parasitic inductances/ loop inductances form L-C networks with device capacitances during every switching transients. These L-C network can cause overshoots and ringing in the device characteristics at every switching instants These responses generate voltage and current stress in the device, cause additional switching loss and degrade electromagnetic interference(EMI) performance of power converters. An IGBT based two level converter layout contains parasitic inductance in range of 300nH[19-20]. Due to its slower switching speed, IGBTs doesn't show considerable amount of voltage and current overshoot for this value of parasitic inductances. Whereas due to faster switching speed of SiC MOSFETs, device performance deteriotes considerably for this range of parasitic inductances. The typical switching duration of SiCFET is 20-30ns for a applied gate voltage (V_{gs}) of +20/-5V with gate resistance of 2.5Ω. Typical range of dv/dt, di/dt slewrates that SiC MOSFET experiences, is around 10 to 15kV/μs and 1 to 1.5kA/μs respectively. These slewrates are almost four times higher than that of a Si IGBTs. So it is necessary to analyze the effect of parasitic inductances on switching performance of SiC MOSFETs in order to design an efficient and feasible high voltage converter.

There have been studies to explain these switching dynamics by mathematical modeling for a Silicon MOSFET[21]-[27]. This gives many possible solutions, and some of those

solutions plays important role in describing the switching dynamics of silicon carbide devices in the presence of parasitic or loop inductances.

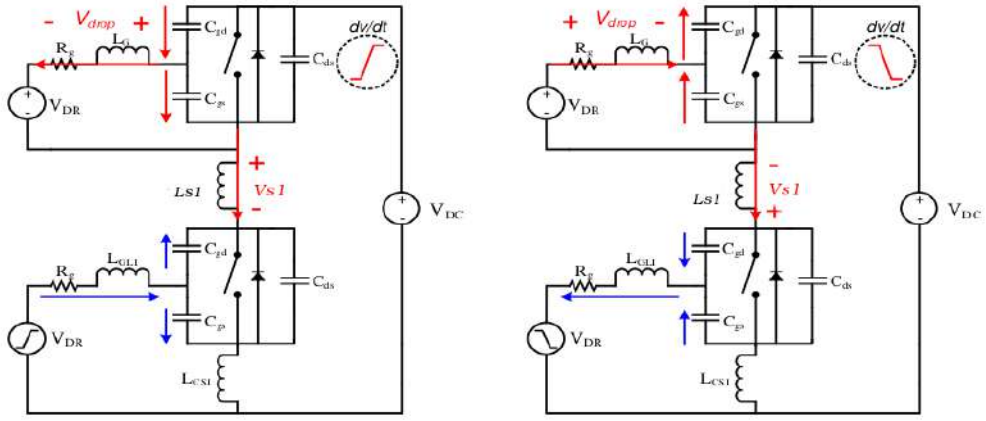
2.2 Crosstalk and Self Turn-on

Silicon carbide devices are known for their ability to switch at very fast speeds with high dv/dt and di/dt, resulting in smaller switching power losses and the ability to operate at higher frequencies. Unfortunately, there are some unintentional effects that manifest themselves when these devices switch at high dv/dt rates. One side-effect of high dv/dt is crosstalk, meaning the interaction between complementary devices in a phase-leg, when the switching transient of one device causes the unintentional turning-on of the opposite device. This effect is referred to as false-turn-on, implying that the event occurred due to circuit parasitics and not as a result of a faulty control signal.

The main result of a false-turn-on is that both devices will be conducting at the same time, allowing high current to flow and a short-circuit to occur. Even if the short-circuit does not result in a catastrophic event, there are still reliability concerns due to high thermal losses. Additionally, the likelihood of a false-turn-on is greater with higher temperature because the threshold voltage has a negative temperature coefficient, making it easier to turn on the device. The shoot-through current also has a positive temperature coefficient, resulting in higher stress on the device at higher temperatures[30]. The potential for failure is greater for SiC devices compared to Si IGBTs because the SiC MOSFET has a lower short circuit withstand time (SCWT).

False turn-on can be caused by the interaction with a complementary device or by a device′s own high-speed transient and interaction with the C_{GD}. Therefore, in both cases, The miller Capacitance, C_{GD}, serves the main pathway for current to flow to the gate(uncontrollable variable). Some of the other variables affecting the possibility of a false turn on are the threshold voltage, V_{th}, internal gate resistance $R_{G,int}$ and packaging inductances at the gate and source, L_G and L_S respectively, in the path of gate current.

In Series connection, crosstalk between two devices can occur during either the turn on or turn off transition of either device in a half-bridge due to the rapidly changing voltage and current sharing at the midpoint. Consider the two devices in a phase leg as shown in FIG.2.1, during the turn on of the lower device, a negative slope dv/dt transition occurs across the C_{GD} of the upper device. This dv/dt results in current that flow through gate



(a) Lower device turns on. (b) Lower device turns off.

Figure 2.1: Crosstalk of two devices in a phase leg

of upper device, causing a voltage drop across the gate resistance as well as the gate loop inductance, which increase the voltage, V_{GS}. If this voltage exceeds the threshold, the device will turn on. Similarly, during turning off of lower device, there is a positive slope dv/dt that causes current through C_{GD} of the upper device in the opposite direction, as shown in *Fig.2.1(b)*. This current flows through the R_G, L_G and L_{s1} causing a negative voltage that further pulls-down the device.

One commonly adopted solution is the use of a negative bias, -5 V, to hold the device in the off-state and cancel any positive voltage spikes. However, the magnitude of the voltage spikes may be large enough to still reach the threshold voltage, especially at higher temperatures when the threshold voltage is lower. The magnitude of the voltage spikes will be affected by the impedance in the gate loop. Thus, it is necessary to make the impedance as small as possible, which is achieved by changing the gate resistor. A higher R_G is typically used to reduce dv/dt, thus there is a tradeoff between the size of the resistor and the amount of impedance in the path. Another accepted solution is Active Miller Clamp and use of bipolar drive with -5V, seperate turn on and turn off paths.

2.3 Parasitic Inductance

Another critical challenge in the implementation of SiC devices are the parasitic inductances in the device and circuit. The package of the SiC device, whether discrete or in

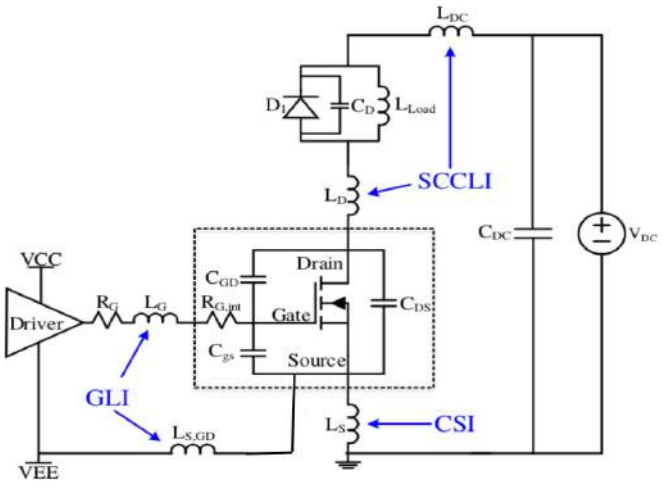


Figure 2.2: Parasitic components in and around SiC device

a power module, and the circuit board layout affect the amount of parasitic inductances present in certain regions of the circuit. Each of these inductances can be lumped into the critical areas of the circuit. The interactions of di/dt during the turn-on and turn-off transitions result in ringing, voltage overshoot, or reduced driving speed.

The parasitic inductances can be split into three categories: the common source inductance(CSI), the gate loop inductance(GLI), and the switched current commutation loop inductance(SCCLI). The Common source inductance includes the inductance at the source inside the package of the SiC MOSFET, the PCB source trace inductance. The Gate loop inductance are enclosed by the gate drive current path, Presence of kelvin terminal eliminates the presence of source inductance in gate loop. Finally, the SCCLI includes the connections between the upper and lower devices in a phase-leg configuration, and results in the main voltage and current ringing of the power loop. in series connection, this inductance will be rised by n times as if n number of device is added in series.

The drain inductance acts as a turn on snubber for the MOSFET by limiting the di/dt of the drain current and reducing the V_{DS} across the device ($L\frac{di}{dt}$), thus reducing turn on losses. However, at turn off, the voltage induced across the inductor is added to V_{DS}, producing an overshoot and increases the turn-off switching losses. When the device is subjected to these voltage overshoots at every switching cycle, the stress over time may decrease the life of the device.

Presence of kelvin terminal eliminates the effect of source lead inductances in gate loop, which improves the switching times compared to previous version of CREE SiC device.

When three terminal SiC devices are used, gate loop includes source lead inductance which also depends on length of return path, which reduces the injected gate current(i_g) and slows down the charging rate of C_{iss}. Slow charging of C_{iss} increases the switching time.

2.4 Protection

SiC MOSFETs can operate very efficiently at high temperatures, and can actually switch faster as temperature increases. The speed at which they switch, however, also affects how fast they will reach a damaging level of current during short circuit event. The ability to prevent, protect such an event is a critical part of the gate driver design. Short circuits will not only cause damage to device over time, but can cause catastrophic failure of the device. Since the short circuit withstand time of device is much smaller than Si device, gate driver has to able to detect a short circuit event faster than the gate driver for a silicon device. Additionally, because SiC devices can switch so fast, the action of turning off device when a SC is detected must be handled carefully so that a very large voltage spike is not caused due to the high di/dt. And these excessive overshoot can result in fast degradation of the device.

Typically, a short circuit event is detected using desaturation method, or DESAT pro-

Figure 2.3: Photograph of failed SiC MOSFET

tection, which is used to determine when the device moves from saturation region to the active region. The transition from saturation to active is not clear for SiC device compared to Si device. The DESAT method can still be utilized for a SiC MOSFET,

but the design must be more precise than that of a si device, or else false detections and unnecessary shutdown can occur. The DESAT method utilizes the on-resistance and the maximum current rating of the device to determine a normal on-voltage across the device. Usually a high-voltage desaturation diode in series with a zener diode is used to block the current signal to the DESAT pin of a gate driver IC until the reference voltage is surpassed, and DESAT is triggered. This means V_{DS} is being monitored at all times. Other than the difficulty in detecting the transition, this method also has the downfall of having to connect sensing circuitry to the high-voltage V_{DS} of the MOSFET. The isolation barrier needs to be sufficient to protect the control circuitry and the delay between the sensed signal and the controller′s response needs to be very short. Additionally, the actual reference voltage for the DESAT protection should be adjustable based on the operating condition, such that a short circuit is not falsely detected.

The speed of the detection must be very fast. When utilizing an IC gate driver with DESAT detection, the propagation delays and detection times from the datasheet should be considered. The propagation delay, which applies to both turn-on and turn-off, will indicate how fast the driver will respond to a control signal telling it to turn-off the device. This is added to the time it takes for the control circuitry to detect the fault, which may also be given in the IC′s datasheet if it has DESAT protection as a functionality. Additionally, the physical location of the gate driver will affect the speed at which it detects the fault because parasitic inductance increases with length of traces, and thus increases the propagation delay between the device and the driver.

Another aspect of the DESAT design is what action the gate driver takes to shut down the device in a controlled manner. If the device is turned off as usual, the current will fall at a very fast di/dt transition, causing large voltage overshoot due to parasitic inductances. Thus, the device should be shut down slowly to avoid over-voltages. This can be achieved through the use of large gate resistors in turn off path to decrease the gate current during the transition.

CHAPTER 3

DYNAMIC VOLTAGE BALANCING IN SERIES CONNECTION

The commercial purpose medium and high voltage SiC devices are under development. Some high-voltage low-current SiC devices (10 kV to 15 kV, 10A to 20A) are available but only in research laboratories [1-2]. They are in limited number due to the low current handling capability in addition to the known issues associated with high dv/dt and requirements of custom design of inductive interfacing components (to reduce the coupling capacitive currents) [3-4]. This makes Si device dominant in medium and high voltage applications. Therefore, to explore the capability of SiC MOSFETs in medium and high voltage applications, the series connection of 1kV/35A SiC MOSFET (third generation CREE device) has been investigated. Stacking of multiple devices in series has following design constraints:

- Unequal static voltage sharing of series connected devices due to mismatch in device leakage currents.
- Unequal dynamic voltage sharing due to mismatch in device parameters and mismatches in the total delay time.
- Parasitic inductance(due to PCB packaging, board inductance) forms L-C networks with device capacitor and causes oscillations and overshoot in device voltage and device current, resulting stress in device and addition switching loss.

Considering the above constraints, several basic mitigation circuits were designed and will be explained in upcoming sections. To begin the proper study of new four terminal devices,isolated passive gate driving(PGD) technique were chosen. Reference [5] uses single gate driver to turn on and turn off the devices in series, which results in undesired switching processes due to delays and other factors like gate capacitances and loop parasitic inductances. When switching happens, device closer to gate driver will commute first, furthest one will commute last depending on transmission length. This switching delay will reduce the switching frequency capability due to effective dead band requirement [6]. Therefore, multiple gate drivers were designed and drives

each devices at the same time (same length of optical cables were used for gate pulse transmission). This method contributes to the gate signal control and provides more flexibility for the gate-side control and device protection in high-power application.

Substantial study have been done to analyze the causes of the uneven voltage sharing, and various techniques have also been proposed to improve the voltage sharing among devices. These techniques can be divided into two categories, namely the drain-source side techniques and the gate-side techniques [7]-[9]. Drain-source side technique category has three different types, namely, the passive snubber circuits, resonant snubber circuits, and clamping circuits.[10]-[12] Gate side control category includes active control circuits and synchronous control circuit.

3.1 Passive Snubber Circuit

The use of a passive snubber is a widely used technique in series operation of power devices. RC based snubber circuit is one of those drain-source side techniques for mitigating inequality in voltage sharing[13]. A resistor-capacitor (RC) or resistor-capacitor-diode (RCD) circuit is used in parallel with the series element for transient sharing. Passive snubbers are simple to implement; they reduce the switching losses and can be used in robust applications. The use of large snubber capacitors minimizes the voltage unbalance but also increases both snubber power loss and commutation time of the device. Therefore, snubber capacitors are designed with an objective of eliminating the voltage transient and ringing caused by providing an alternate path for the current to flow through circuit′s intrinsic leakage inductance. Proposed snubber circuit consist of series connected resistance and capacitances paralleled with balancing resistance, R_b as shown in *Fig. 3.1*.

Fig. 3.2 shows the deviations in device voltages when connected in series without any voltage balancing circuits.To reduce the static voltage sharing inequality, a balancing resistance of few hundred kilo ohms were chosen. One can choose higher value of balancing resistance as long as its sufficiently larger than the leakage current of the SiC MOSFET. But, on the other hand higher value of balancing resistance leads to higher time constant and therefore it will take more time to settle in static condition, If this

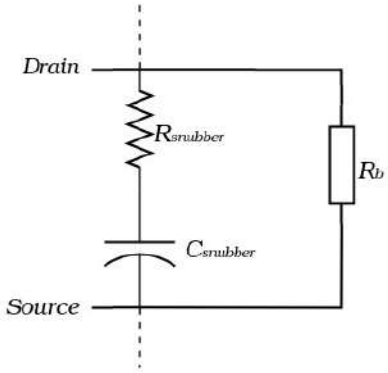


Figure 3.1: Passive snubber circuit

time constant is greater than the switching frequency.

Figure 3.2: Individual device voltage in series connection without snubber circuit

The value of snubber capacitor has been selected at least 5-10 times the devices output capacitance as starting value to nullify the mismatch in the device output capacitances[14]. The snubber capacitance could reduce the unbalance in dynamic voltage sharing between the devices and the rate of rise of drain-source voltage across series connected devices. During turn-off, V_{DS} will be nearly equal between the devices as the snubber capacitance is much larger than device′s output capacitance. It also makes the turn-off process in the devices partially zero-voltage switching and hence reducing the turn off losses in the process. The starting value of resistance ($R_{snubber}$) is selected such that the time constant of snubber is low enough to discharge capacitor during ON time.

Values of snubber capacitance and resistance are selected in such a way that total switching losses in the device and difference in dynamic voltage sharing is minimised. Simulation for the same has been done considering the worst case delays. For Different R and C values Ltspice simulation result is shown below.

case: 1	Snubber Capacitance(nF)	snubber resistance (mΩ)	DC Bus Voltage (V)	Switching frequency (kHz)	Max. Switching Loss across a single device (W)	voltage Deviation (V)
i	10	400	1500	10	78.85	259
ii	10	400	1500	50	394.27	259
iii	10	400	1500	100	788.54	259

Table 3.1: Simulation result for R = 0.4mΩ and C= 10nF

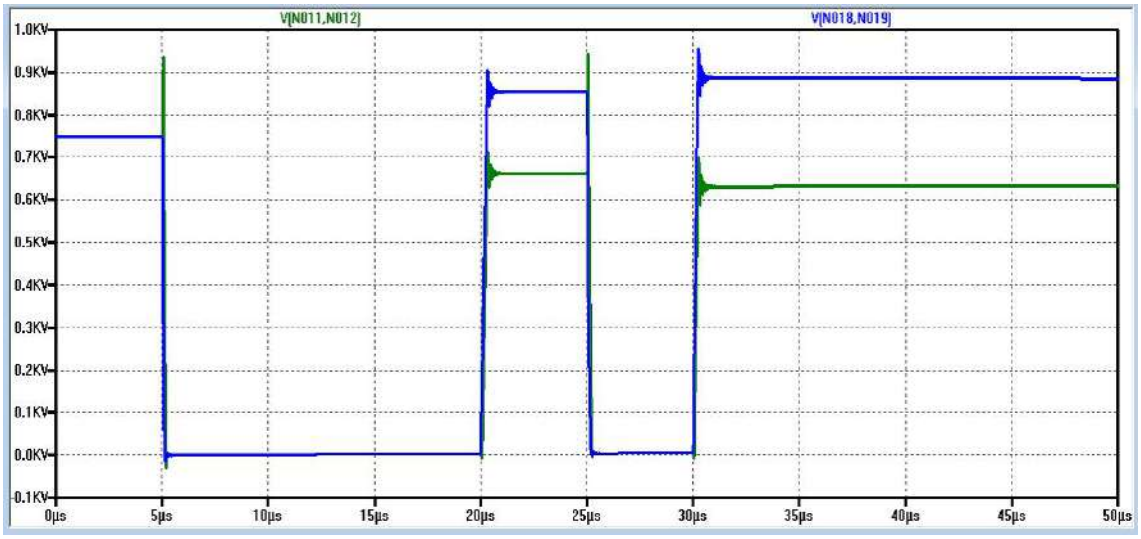


Figure 3.3: Ltspice simulation result for R =0.4mΩ and C= 10nF
Scale; Voltage: 0.1kV/div, time: 5us/div

Figure 3.3 shows the simulation result for RC connected series circuit. Voltage deviation for this case is 259V. Device that get commutated first will share maximum voltage for duration until the next device commutated. The simulation were done considering the worst case delay of 50ns. Therefore, as aforementioned device 1 (represented as blue line) get turned on first and then device 2 (represented as green line) get turned on after 50ns. Switching loss at different frequencies were calculated and is tabulated in *Table 3.1*.

Figure 3.4 shows the simulation result for RC connected series circuit. Voltage deviation for this case is 142V. As mentioned above, for same delay in second gate driver

case: 2	Snubber Capaci-tance(nF)	snubber resis-tance (mΩ)	DC Bus Voltage (V)	Switching frequency (kHz)	Max. Switch-ing Loss across a single device (W)	voltage Deviation (V)
i	22	180	1500	10	151.92	142
ii	22	180	1500	50	759.61	142
iii	22	180	1500	100	1519.23	142

Table 3.2: Simulation result for R = 0.18mΩ and C= 22nF

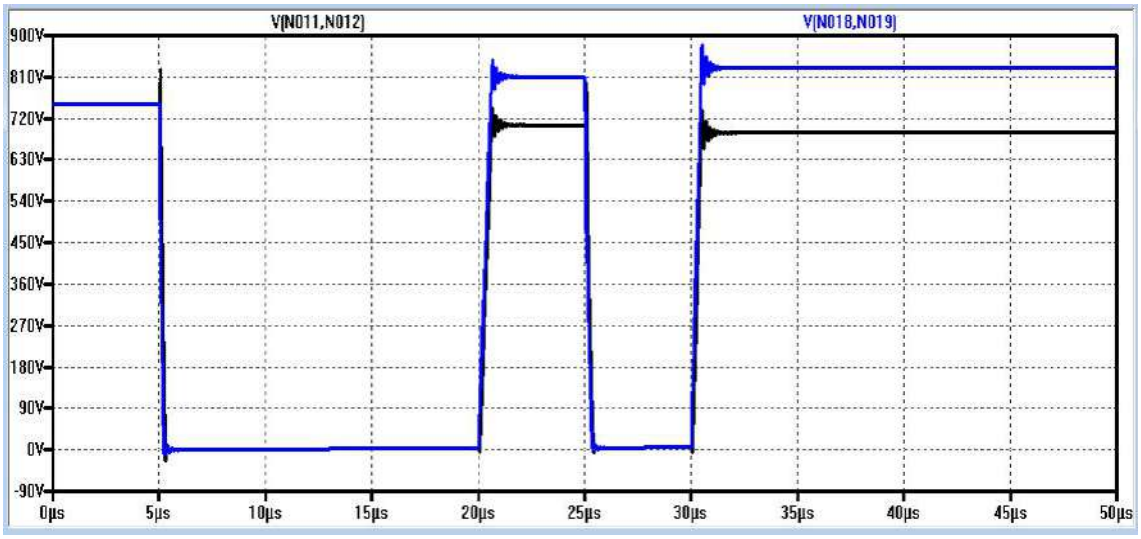


Figure 3.4: Ltspice simulation result for R =0.18mΩ and C= 22nF
Scale; Voltage: 0.1kV/div, time: 5us/div

device 1 (represented as blue line) get turned on first and then device 2 (represented as green line) get turned ON. Switching loss at different frequencies were calculated and is tabulated in *Table 3.2*.

Similarly, for the 33nF and 56nF capacitors, simulation studies were done.(Refer

case: 3	Snubber Capaci-tance(nF)	snubber resis-tance (mΩ)	DC Bus Voltage (V)	Switching frequency (kHz)	Max. Switch-ing Loss across a single device (W)	voltage Deviation (V)
i	33	120	1500	10	216	102
ii	33	120	1500	50	1079.9	102
iii	33	120	1500	100	2159.78	102

Table 3.3: Simulation result for R = 0.12mΩ and C= 33nF

Fig.3.5 and Fig.3.6.) Switching Loss for both were calculated and tabulated in *Table 3.3* and *Table 3.4*.

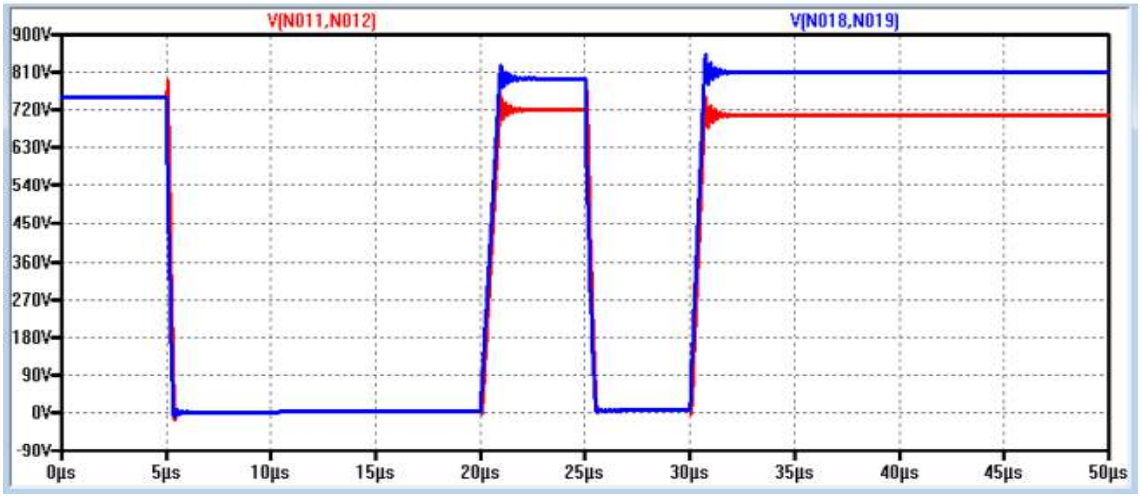


Figure 3.5: Ltspice simulation result for R =0.12mΩ and C= 33nF
Scale; Voltage: 0.09kV/div, time: 5us/div

The maximum peak overshoot voltage in case 3 is 857V and deviation is 102V.

case: 4	Snubber Capacitance(nF)	snubber resistance (mΩ)	DC Bus Voltage (V)	Switching frequency (kHz)	Max. Switching Loss across a single device (W)	voltage Deviation (V)
i	56	71	1500	10	350.38	64
ii	56	71	1500	50	1751.91	64
iii	56	71	1500	100	3503.80	64

Table 3.4: Simulation result for R = 0.07mΩ and C= 56nF

The maximum overshoot in case 4 is 824V. and deviation is 64V.

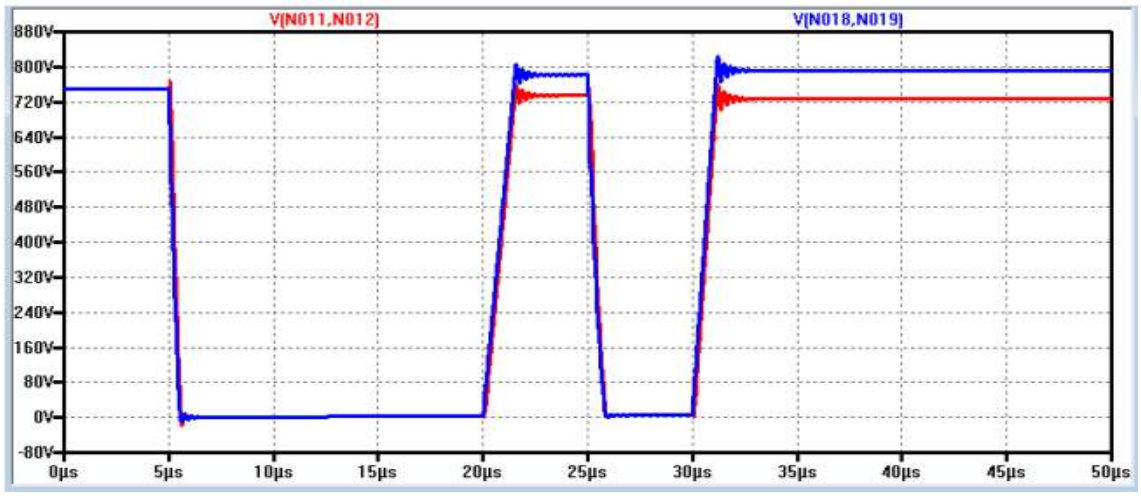


Figure 3.6: Ltspice simulation result for R =0.071mΩ and C= 56nF
Scale; Voltage: 0.08kV/div, time: 5us/div

From simulation studies, reduction in deviation can be seen as capacitance increases but it also increases the switching loss of individual device for a given switching fre-

quency. Therefore, it is desired to select the appropriate R and C values for required switching frequency and voltage levels. At lower value of gate resistances, there is no substantial change in switching loss per device with snubber and without snubber case for same DC bus voltage[14].

3.2 Gate-Side Voltage Balancing Technique

A common characteristic of the gate side techniques is to correct the voltage imbalance of the series-connected semiconductor device by adjusting its gate voltage. However, regardless of the quantity of devices connected in series, all techniques require a corresponding number of isolated gate driving signal for each series connected device. Since gate voltage will be fixed in passive gate driving technique, transient voltage can be balanced by adjusting the rate in rise of gate voltage either by changing gate resistance of any one of driver or by introducing the delay in the pulse so that $\frac{dV_{GS}}{dt}$ of all gate driver matches well.

3.2.1 Pulse Delay Shift Logic

It is very important to note the Gate voltage level as if Gate voltage to any of the device connected in series is not equal, then gate charging to corresponding device also differs which also causes deviations in device voltages. Another reason for cause of deviation is time delay in switching actions. This will also cause difference in gate charge in devices in series connection. Gate pulse given to the gate driver can be varied using Delay logic circuit. Intention of providing this circuit is to study the device performance under mismatch conditions by changing the turn on or turn off propagation delay times of individual switching devices.

By analysing the actual waveform and the required output waveform as shown in *Fig: 3.7*, digital data can be extracted and tabulated (*Table: 3.5*) to define the equation and identify the number of logic gates required to implement this idealogy. The Sum of Product combination for above mentioned karnaugh map is

$$Y_{requiredpulse} = F * (\overline{G} + R) \tag{3.1}$$

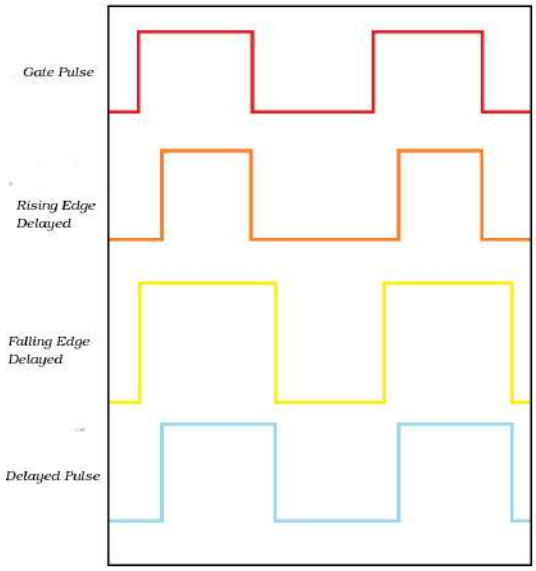


Figure 3.7: introducing delay in actual pulse

Actual Gate Pulse	Rising Edge Delayed Pulse	Falling Edge Delayed Pulse	Output or Required Delayed Pulse
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0*	0
1	1	1	1

Table 3.5: Design of Pulse delay shift logic

**practically falling edge delay cannot be low when there is actual pulse coming in, so this row is not considered while designing k-map.*

	$\overline{R}\,\overline{F}$	$\overline{R}$F	RF	R.$\overline{F}$
$\overline{G}$	0	1	1	0
G	0	0	1	0

Table 3.6: Karnaugh map for required Pulse

From the *Eqn:3.1* number of logic gate required to implement delay circuit is three, i.e., combination of NOT, OR and AND gate.Refer *Fig: 3.8.*

To create the delay in Rising and falling edge as desired, RC- Diode combination is chosen and this combination output is compared with certain reference to give required delay at rising edge or falling edge. *Fig: 3.9* shows the mentioned circuit having RC-Diode and comparator followed by digital logic circuit. TLV3502 is used as comparator,

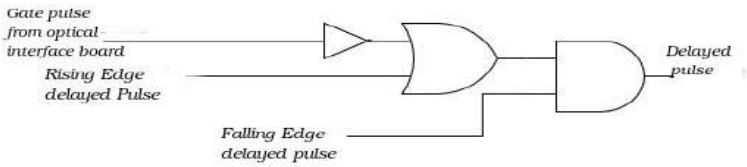


Figure 3.8: simplified delay introducing circuit

which has pretty good CMRR and slew rate.

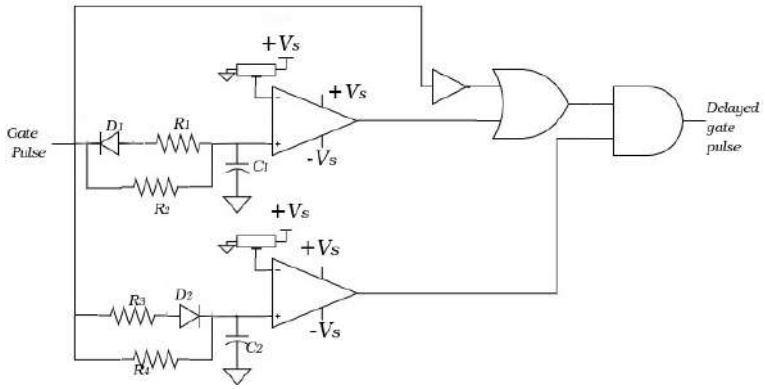


Figure 3.9: implemented delay circuit

Simulation for the above circuit is done and verified with hardware result.

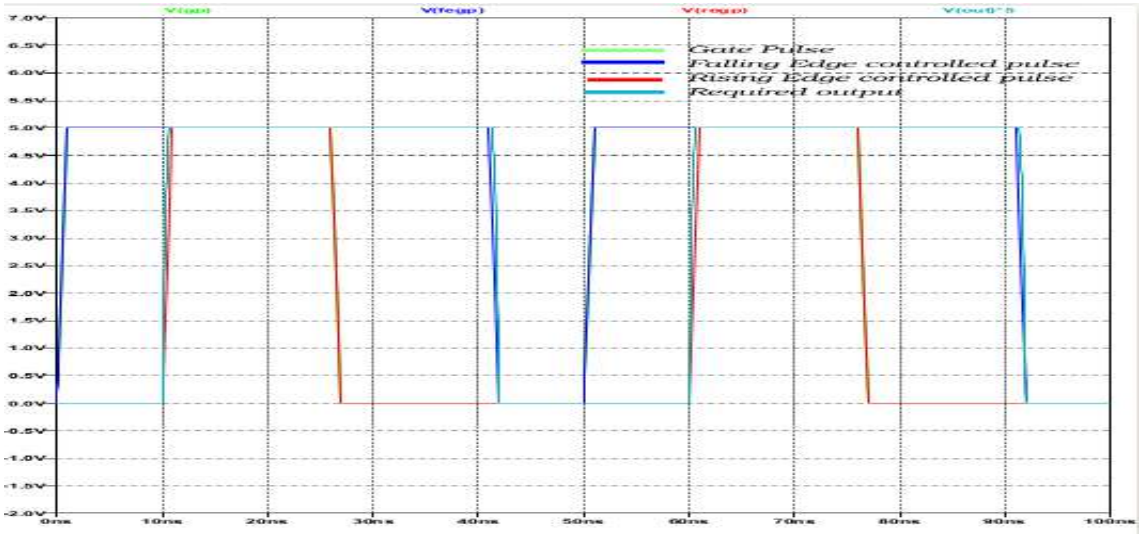


Figure 3.10: Simulation result for pulse delay circuit. Scale; Voltage: 0.5V/div, time: 10ns/div

3.2.2 Gate Resistance Control

Another method of dynamic voltage balancing is adjusting the rate of rise of gate voltage of any one device so that it reaches desired voltage at the same time as other device reaches its voltage level. Even though devices from same company and of same rating is believed to have same internal capacitance and resistance value. But it has some difference in terms of intrinsic characteristics i.e., gate to drain capacitance, C_{GD} and gate to source capacitance, C_{GS}.

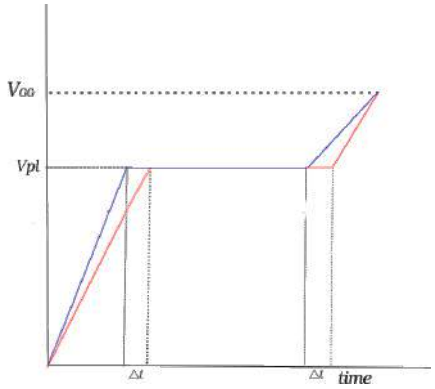


Figure 3.11: Different Gate voltages of two series connected devices

Difference in gate voltage dv/dt shown in *Fig.3.11* will also give deviation in drain voltages. Assuming that there is some delay Δt introduced as shown in *Fig.3.12* even though gate side dv/dt are same, which cause certain deviation in drain voltage, $\Delta \mathrm{V}_{DS}$.

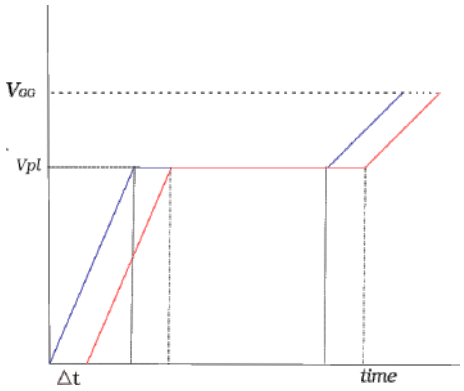


Figure 3.12: Gate voltages of two series connected devices with Δ t delay in driving circuit

$$\Delta V_{DS} = \frac{d(V_{DS1}}{dt} * t_{r1} - \frac{dV_{DS2}}{dt} * t_{r2} \tag{3.2}$$

$$\Delta V_{DS} = \frac{d(V_{DS1}}{dt} * t_{r1} - \frac{dV_{DS2}}{dt} * (t_{r1} - \Delta t) \tag{3.3}$$

$$\Delta V_{DS} = t_{r1} * [\frac{d(V_{DS1}}{dt} - \frac{dV_{DS2}}{dt}] + \Delta t * \frac{dV_{DS2}}{dt} \tag{3.4}$$

$$\frac{\Delta V_{DS}}{dV_{DS2}/dt} = t_{r1}.[\frac{dV_{DS1}/dt}{dV_{DS2}/dt} - 1] + \Delta t \tag{3.5}$$

$$\Delta t = \frac{\Delta V_{DS}}{dV_{DS2}/dt} - t_{r1}.[\frac{dV_{DS1}/dt}{dV_{DS2}/dt} - 1] \tag{3.6}$$

for dynamic voltage to be balanced, Δ V$_{DS} = 0\ then,$

$\Delta t = t_{r1}.(1 - \frac{d(V_{DS1}/dt}{dV_{DS2}/dt})$(3.7)

we also know that,

$$\frac{dV_{DS}}{dt} = \frac{I_G}{C_{GD}} \tag{3.8}$$

where

$$I_G = \frac{V_{GS}}{R_G} \tag{3.9}$$

then *Eqn.3.8* becomes,

$$\frac{dV_{DS}}{dt} = \frac{V_{GS}}{R_G.C_{GD}} \tag{3.10}$$

substituting *Eqn.3.10.* in *Eqn.3.6.*

$$\Delta t = t_{r1}.(1 - \frac{V_{GS}/R_{G1}.C_{GD1}}{V_{GS}/R_{G2}.C_{GD2}}) \tag{3.11}$$

Assuming that Gate voltage, V_{GS} is same for all devices, then Δt becomes,

$$\Delta t = t_{r1}.(1 - \frac{R_{G1}.C_{GD1}}{R_{G2}.C_{GD2}}) \tag{3.12}$$

Selecting appropriate gate resistance R_{G1} and R_{G2}, both delay in rise time, fall time and deviation in Drain-Source voltage can be reduced or brought to zero.

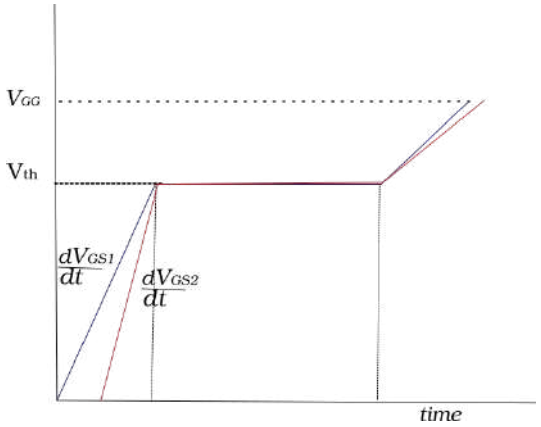


Figure 3.13: Gate voltages of two series connected devices when gate resistance of one device is changed

Simulation for above idealogy is done in Ltspice for different cases.
Case 1: Equal gate resistance for two devices connected in series assuming no delay in driving section.

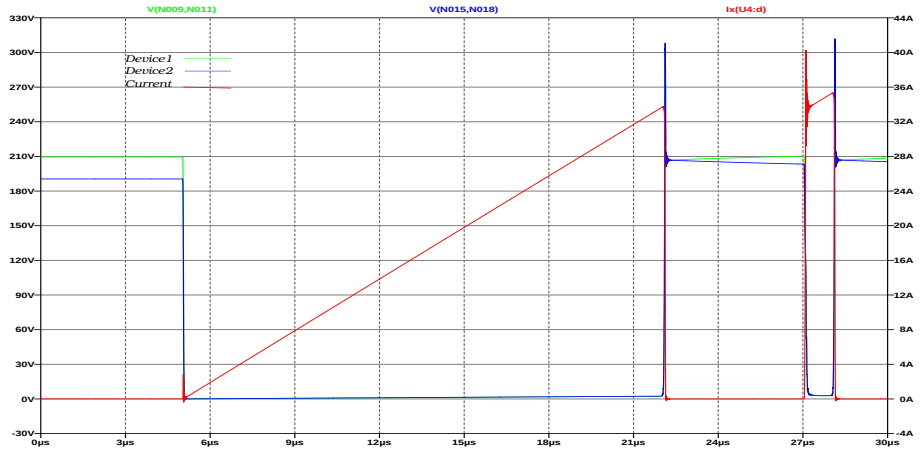
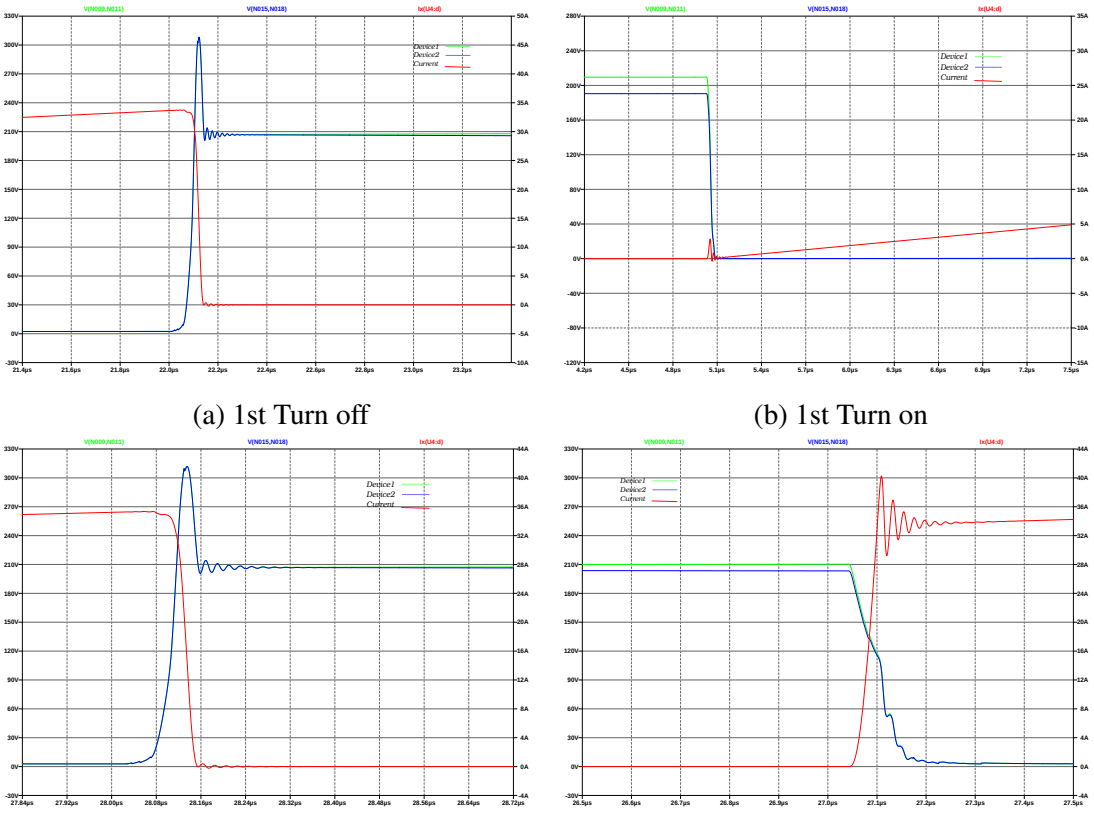


Figure 3.14: Simulation waveform for Case 1: R=100Ω, Δt=0ns. Scale; voltage: 30V/div, current: 5A/div, time: 3us/div



(a) 1st Turn off

(b) 1st Turn on

(c) 2nd Turn off

(d) 2nd Turn on

Figure 3.15: Second Pulse waveform for Case 2. Scale; voltage(a,c,d): 30V/div, voltage(b): 40V/div, current(a,b): 5A/div, current(c,d): 4A/div, time(a,b): 0.3us/div, time(c): 80ns/div, time(d): 100ns/div

Red colour plot in simulation represents device current and Green and blue colour waveform represents top and bottom device voltages respectively.

Case 2: Equal gate resistance for two devices connected in series assuming worst case delay of 50ns.

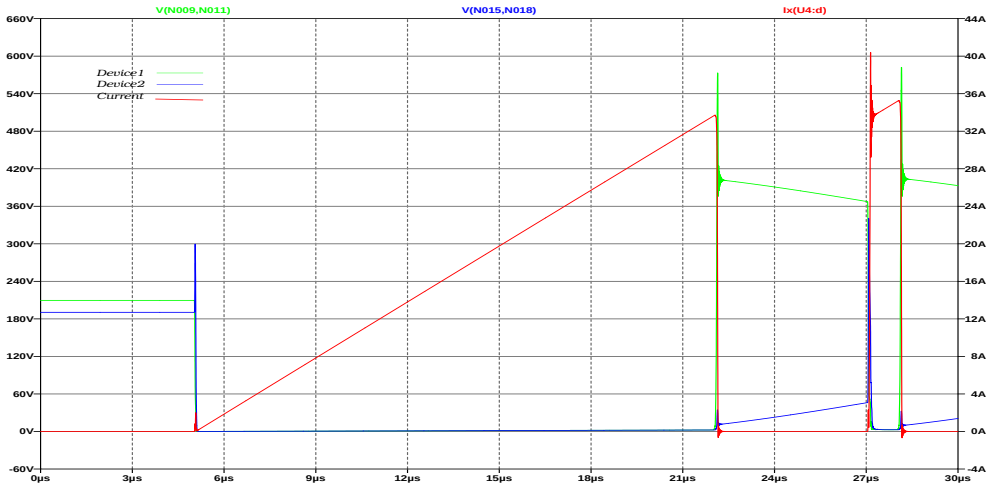
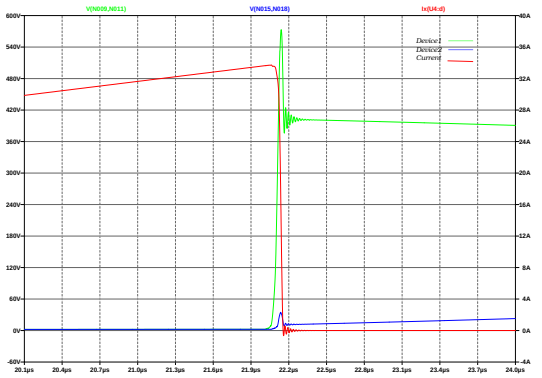
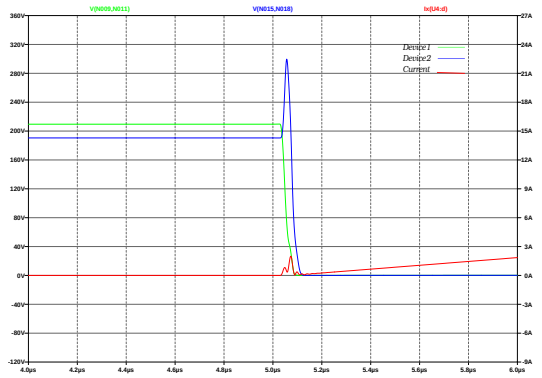


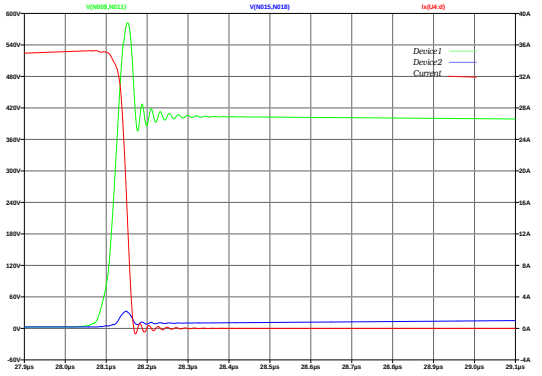
Figure 3.16: Simulation waveform for Case 2: R=100Ω, Δt=50ns. Scale; voltage: 60V/div, current: 4A/div, time: 3us/div



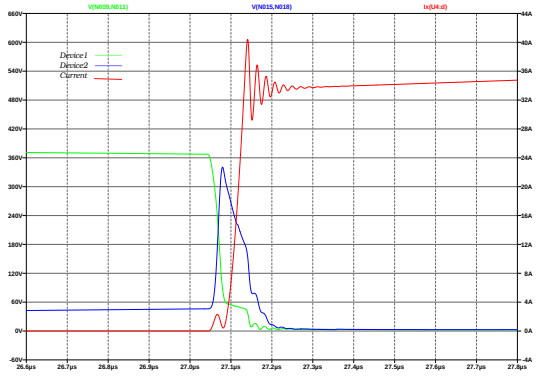
(a) 1st Turn off



(b) 1st Turn on



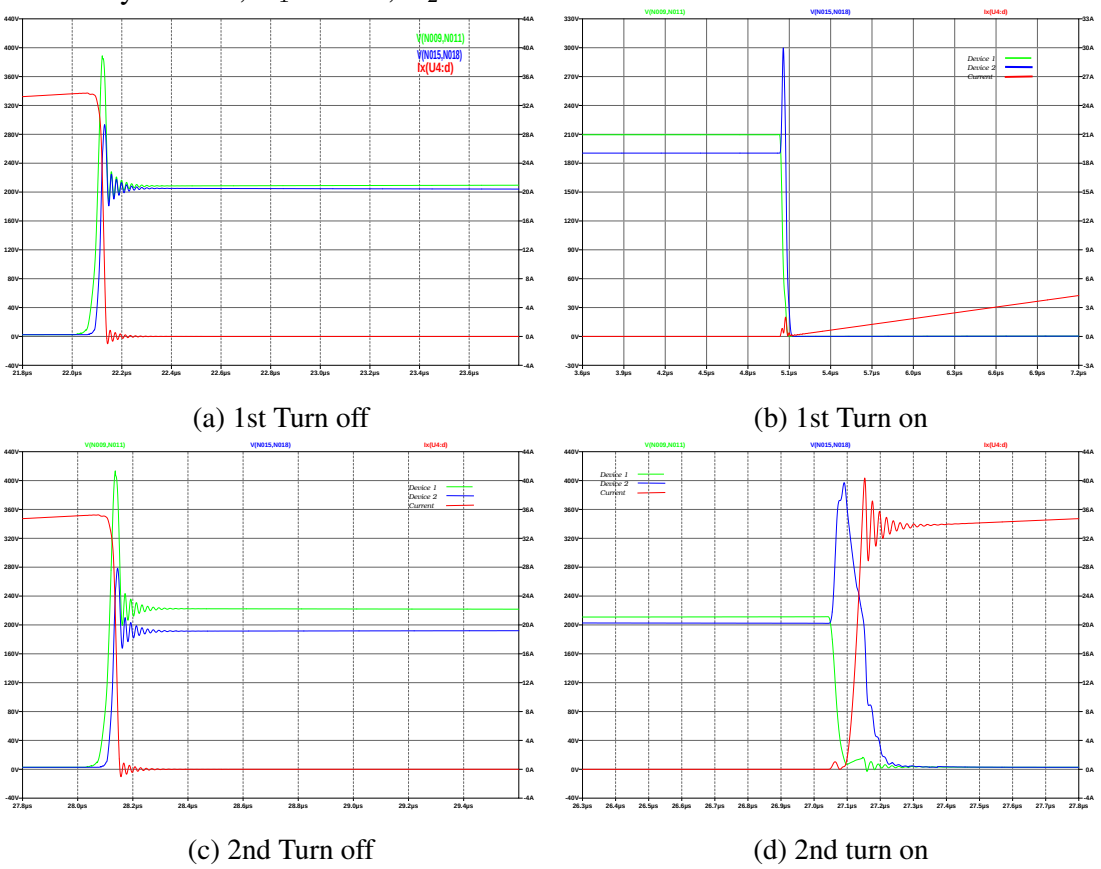
(c) 2nd Turn off



(d) 2nd Turn on

Figure 3.17: First and second Pulse waveform for Case 2. Scale; voltage: 60V/div, current: 4A/div, time(a): 0.3us/div, time(b): 0.2us/div, time(c d): 0.1us/div

Case 3: Different gate resistance for two devices connected in series assuming worst case delay of 50ns, R_1=100Ω , R_2=57.5Ω.



(a) 1st Turn off

(b) 1st Turn on

(c) 2nd Turn off

(d) 2nd turn on

Figure 3.18: Double Pulse waveform for Case 3. Scale; voltage(a): 40V/div, current(a): 4A/div, time(a): 0.2us/div, voltage(b): 30V/div, current(b): 3A/div, time(b): 0.3us/div, voltage(c, d): 40V/div, current(c,d): 4A/div, time(c): 0.2us/div, time(d): 0.1us/div

Case 4: Different gate resistance for two devices connected in series assuming worst case delay of 50ns, R_1=68Ω, R_2=27Ω.

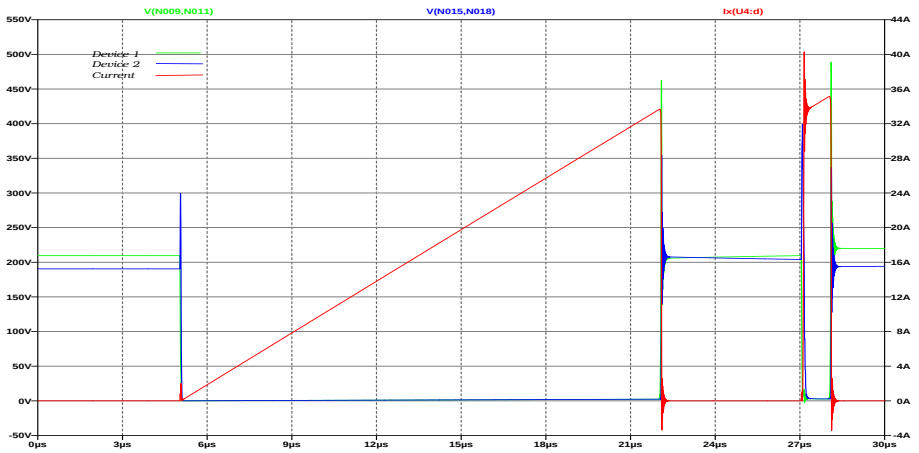
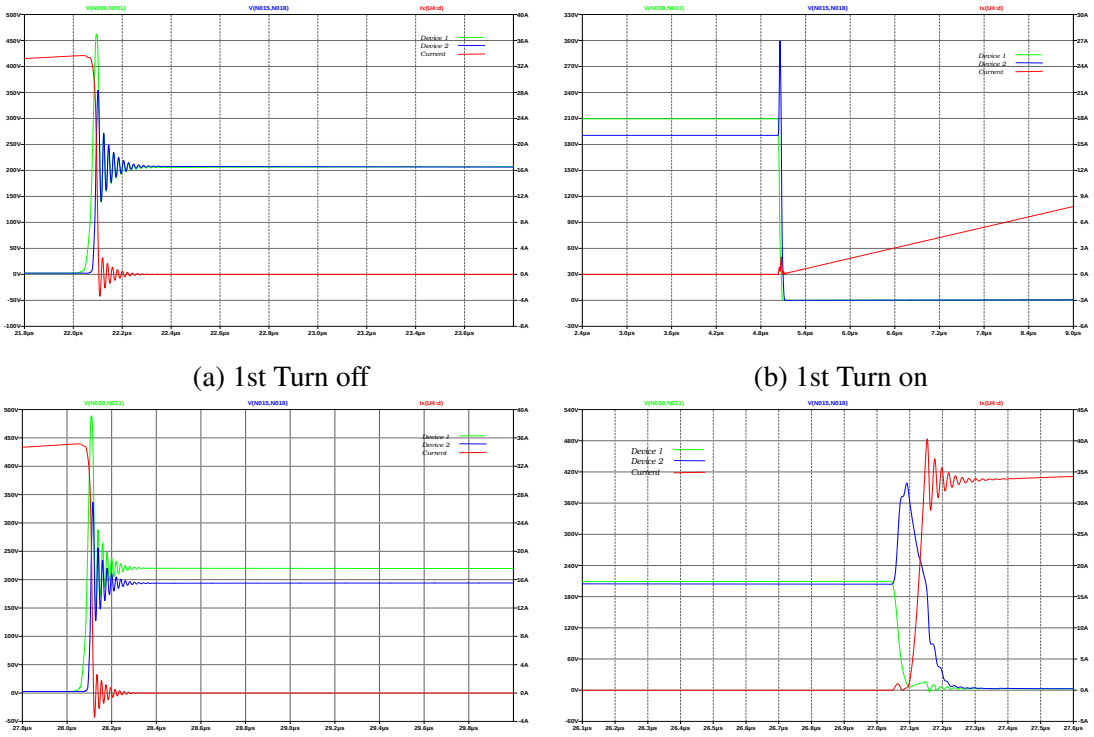


Figure 3.19: Simulation waveform for Case 4: R_1=68Ω, R_2=27Ω, Δt=50ns. Scale; voltage: 50V/div, current: 4A/div, time: 3us/div



(a) 1st Turn off

(b) 1st Turn on

(c) 2nd Turn off

(d) 2nd turn on

Figure 3.20: Double Pulse waveform for Case 4. Scale; voltage(a): 50V/div, current(a,c): 4A/div, time(a): 0.2us/div, voltage(b): 30V/div, current(b): 3A/div, time(b): 0.6us/div, voltage(c,d):50V/div, current(d): 5A/div, time(c): 0.2us/div, time(d): 0.1us/div

3.3 Sensing of Device parameters

Sensing of device voltage is the very important for active gate control of series connection of SiC MOSFET's. To Design active gate driver with FPGA or DSP control on board, it is necessary to sense or capture entire transient region of voltage and current for perfect design of closed loop feedback control.

3.3.1 Drain Voltage Sensing

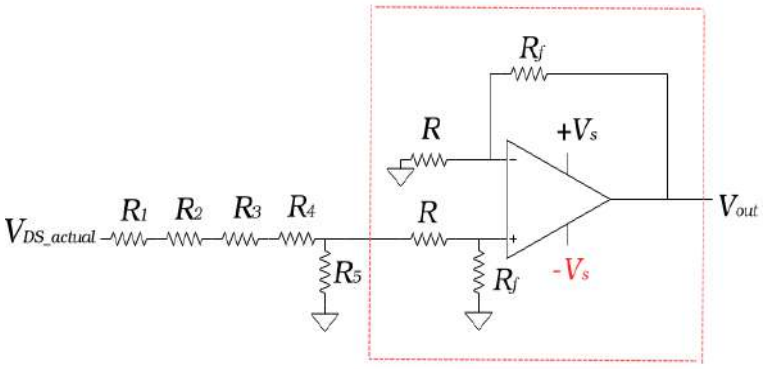


Figure 3.21: Voltage sensing circuit

For series connection application, individual device voltage can go upto 70-80 % of rated voltage. Device might detoriate or fail if transient voltage rises beyond rated voltage for few nanoseconds.

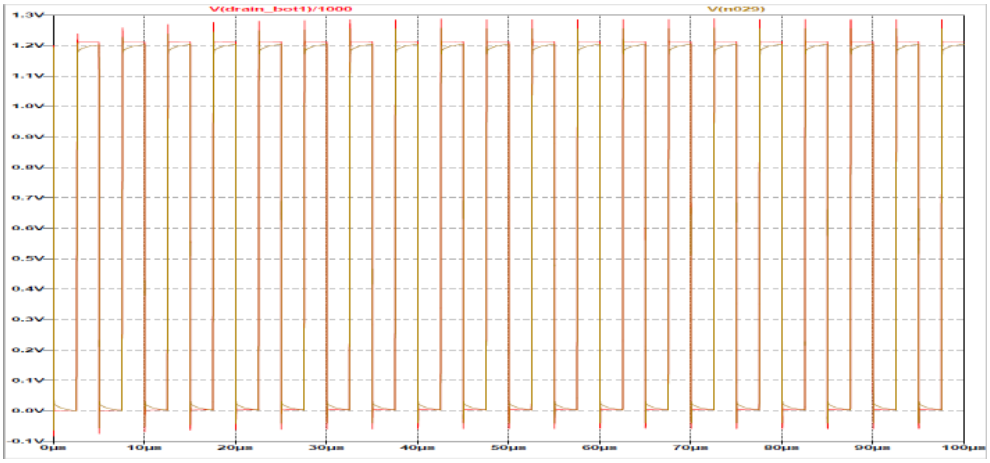


Figure 3.22: Simulation result for Voltage sensing; scale x-axis: 10us/div, V_{DS}: 0.1V/div

To feed the actual voltage shape to digital controller, voltage level should be scaled down to signal level, $\pm$ 5V. The switching of SiC MOSFET happens within few nanoseconds and thus V_{DS} exhibits a very high dv/dt for very short interval of time (high frequency component).Therefore to track/capture exact voltage, resistor bridge connected with high CMRR, Slew rate differential Opamp, **AD8045** were selected.(Refer *Fig.3.21*).

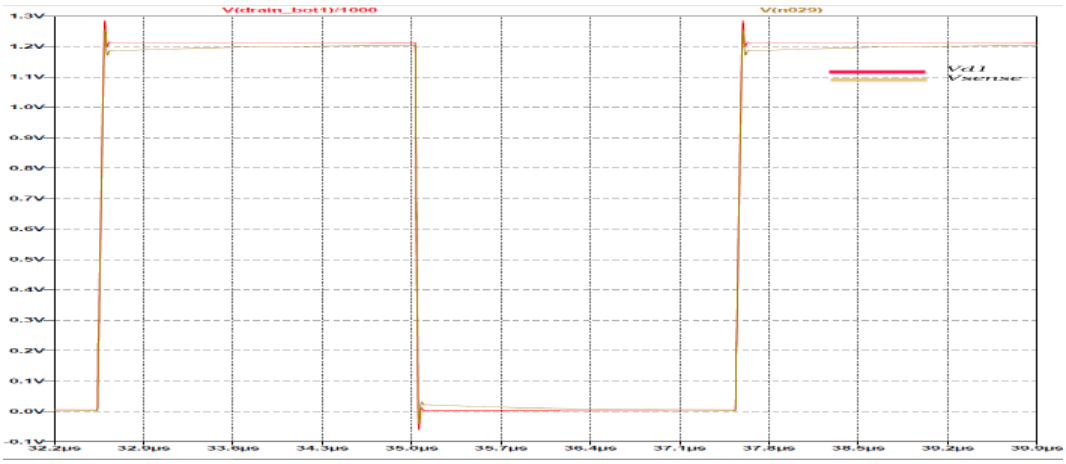


Figure 3.23: Voltage sensing simulation waveform, zoomed version ; scale x-axis: 0.7us/div, V_{DS}: 0.1V/div

Problems associated with this circuit will be discussed in *Chapter 5*. Simulation for the following circuit were done in Ltspice software and result turns out to be matching with actual voltage. Refer *Fig.3.22* and *Fig.3.23*.

3.3.2 Drain current Sensing

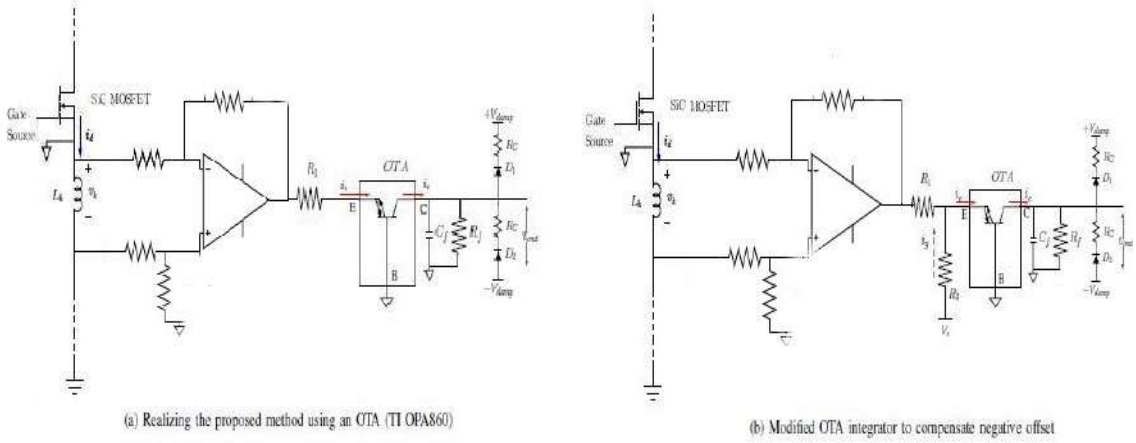


Figure 3.24: widebandgap integrator

This section proposes a Kelvin voltage based drain current sensing method. Though, Kelvin voltage based current sensing method is common in IGBT application, but its application for SiC MOSFETs is rarely reported. The Kelvin voltage (v_k is the voltage that appears across the kelvin terminal and actual source of a SiC MOSFET due to small parasitic inductance contributed by device packaging. The magnitude of Kelvin voltage is given by *Eq.3.13*.

$$v_k(t) = Lp.\frac{di_d}{dt} \tag{3.13}$$

Current sensing circuitry has been designed by monitoring voltage across the parasitic inductance (additional inductance of 10nH has been added), i.e., Kelvin voltage. The switching of SiC MOSFET happens within few nano seconds and thus I_D exhibits a very high di/dt for very short interval of time (high frequency component).

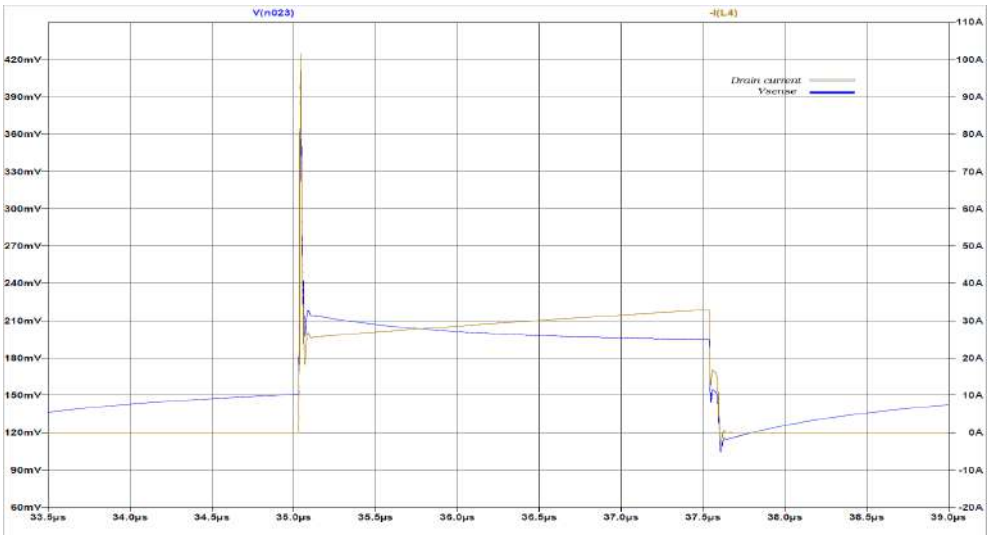


Figure 3.25: current sensing simulation; scale; x-axis: 0.5us/div, I_D = 10A/div, Vout = 30mV/div

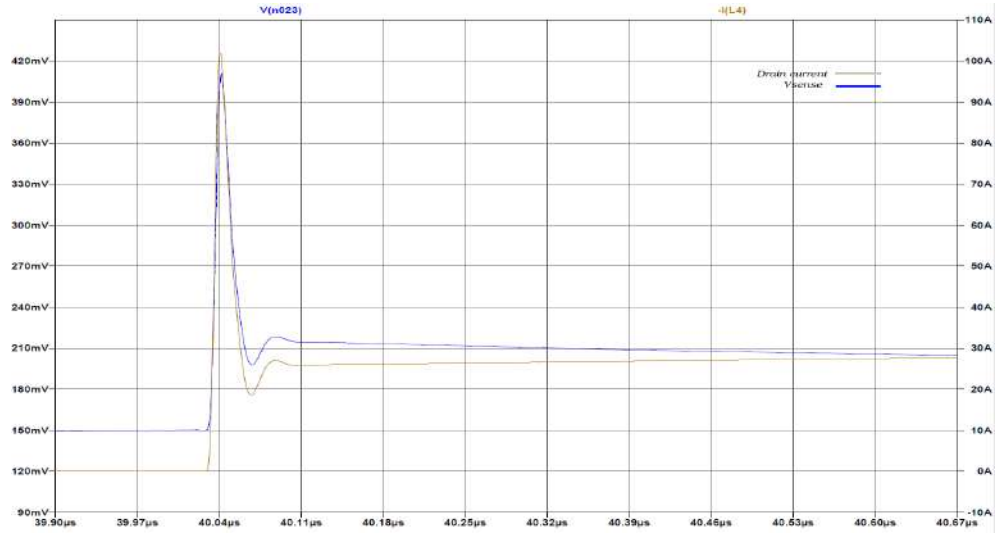


Figure 3.26: current sensing simulation; scale; x-axis: 70ns/div, I_D = 10A/div, Vout = 30mV/div

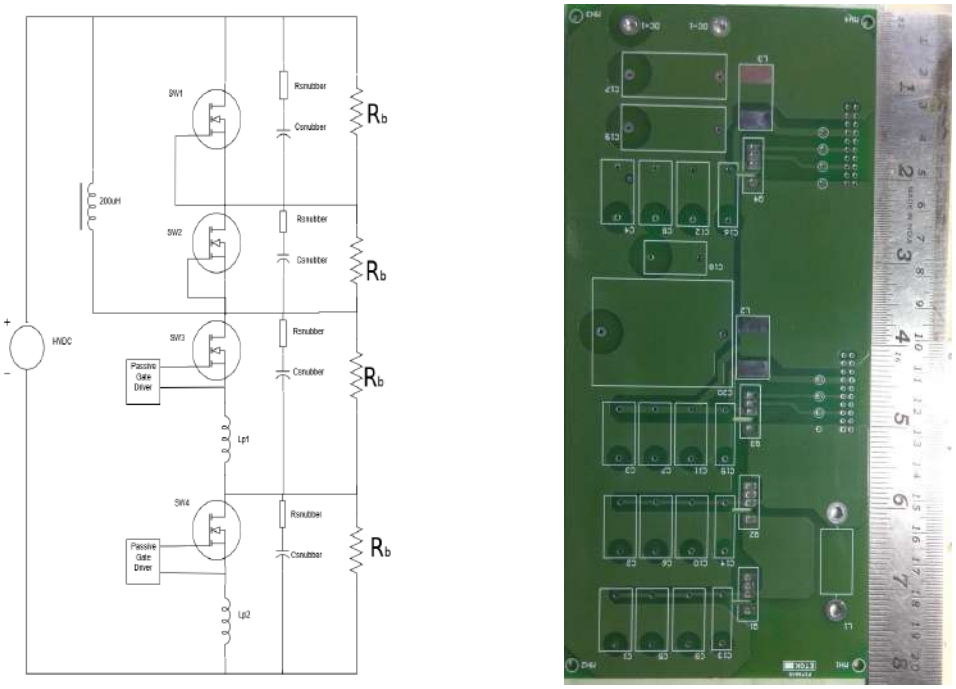
Whereas, the di/dt during the steady state conduction is much lower than that during the switching interval as it is primarily governed by the load inductance (low frequency component). To reconstruct the drain current id from the kelvin voltage a wideband integrator is required. A wideband high CMRR Operational Transconductance Amplifier (OTA) based integrator is used which replicates current I_D. However, due to the faster switching of the SiC device, higher slew rate operational amplifier is required and higher bandwidth is required to faithfully replicate the overshoots and oscillation in drain current. Therefore, commercially available OTA; Texas instruments' OPA860 and Analog Device's AD8045C opamp is used for this application. From the Datasheets of OPA860 and AD8045 it is observed that it has a flat frequency response upto 100MHz and hence both can integrate wideband signals therefore both the ICs were chosen for this application.

In the case of OTA, base of OTA transistor is ground so that current i_b= 0, and i_c = i_e. So, emitter current, i_e is basically current through R_1 connected to kelvin source terminal. Integral of i_e results in in a voltage proportional to I_d. A capacitor C_f can be used to integrate the collector current, i_c and thus produce a voltage v_{out} proportional to the drain current. However placing capacitor alone for integration creates a DC offset problem at output of integrator as low frequency signals can saturate OPamp IC's. To overcome this, a resistor R_f is placed across C_f. (*Fig.3.24.*) to ensure proper DC biasing of the integrator circuitry. Selection of R_f and C_f has done in such a way that entire device current can be reproduced by the wideband integrator. simulation results for same have been shown in *Fig.3.25* and *Fig.3.26*.

CHAPTER 4

HARDWARE ORGANISATION

This chapter deals with design and development of proposed gate driver, isolated power supply for the CGD, double pulse test setup.

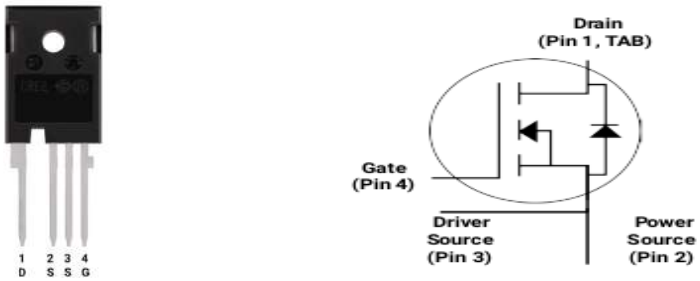


(a) circuit diagram (b) Printed circuit diagram

Figure 4.1: Double Pulse Test setup

SiC MOSFET is tested in a double pulse test setup as shown in *Fig.4.1*. PCB of test bed is made up of two layer flame retardant(FR4) material with a thickness of 3mm. Board can accomodate four SiC devices, two gate drivers with power supply and load inductor. The DC bus is sandwiched to have minimum parasitic/loop inductance in the layout, as one can see in the *Fig.4.1(b)* the components are placed in a straight line on top and bottom of board so that only one loop is formed in whole board, this in turn reduces the loop incuctances. A 20.5 μF polypropylene film capacitors combinations are connected across the DC bus(in DP board) to nullify the effect of layout parasitic inductances. Also a set of four, 16 μF metalized polypropylene capacitors are connected across DC bus to nullify effect due to paraasitic inductances. Metalized polypropylene capacitors are selected due to its very low equivalent series inductance(ESL).

The Device Under Test (DUT) for the DP test was a third generation SiC MOSFET module from CREE (Refer. *Fig.4.2*). This SiC MOSFET has four terminals, kelvin voltage is additional fourth terminal added among other three terminals. The key parameters of the device are presented in *Table.4.1*.



(a) photograph of device (b) Pin diagram

Figure 4.2: CREE SiC MOSFET

Parameters	Value
Part No	C3M0065100K
V_{DSmax}	1000V
$I_{Dcontinuous}$	35A
R_{DSon}	65mΩ
C_{iss}	660pF
C_{oss}	60pF
C_{rss}	4pF
$V_{GS(th)}$	2.1V
R_{Gint}	4.7Ω

Table 4.1: SiC MOSFET Details

The DPT setup is designed handle pulsed current upto 300A. Therefore, a load inductor which can with stand 300A without saturating is required.

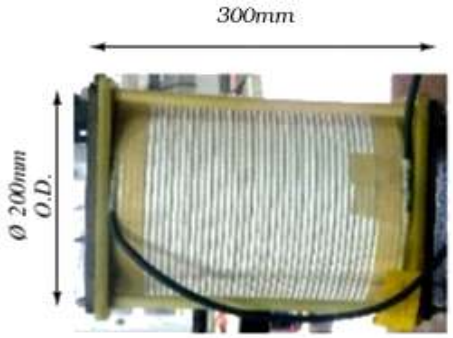


Figure 4.3: 200μH Air core inductor

A 200μH air core inductor was designed as shown in *Fig.4.3*. The designed inductor

consists of single layer winding which reduces the effect of stray capacitcances thereby improving the performance of inductor.

4.1 Passive Gate Driver

Passive Gate Driver incorporate all sensing and mitigation circuitry mentioned in chapter 3. To Drive the fast switching SiC MOSFETs, gate driving IC designed by Texas Instruments, ISO5852Q were chosen. For SiC MOSFETs, the driving voltage are +15V in the ON state and -2.5V in the OFF state.

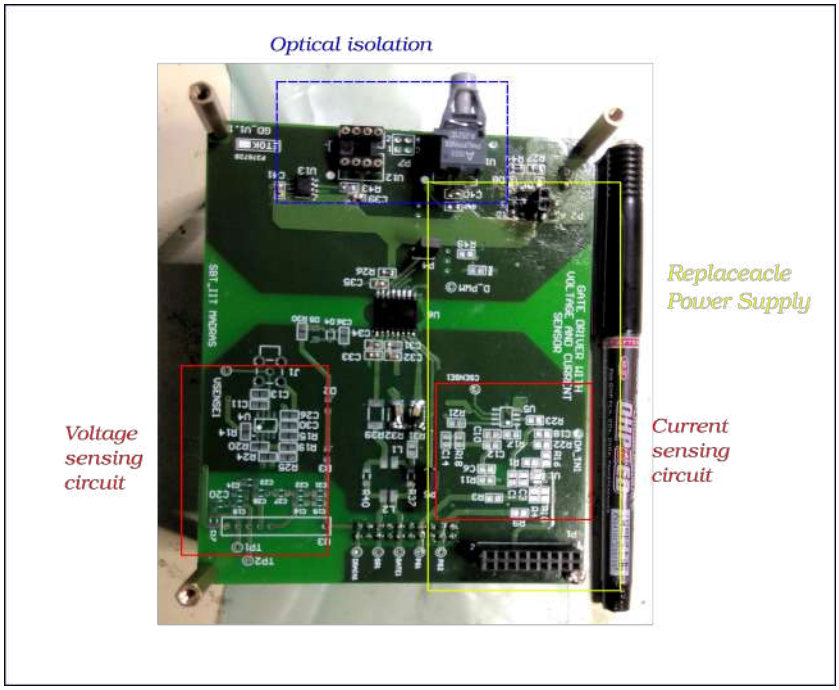
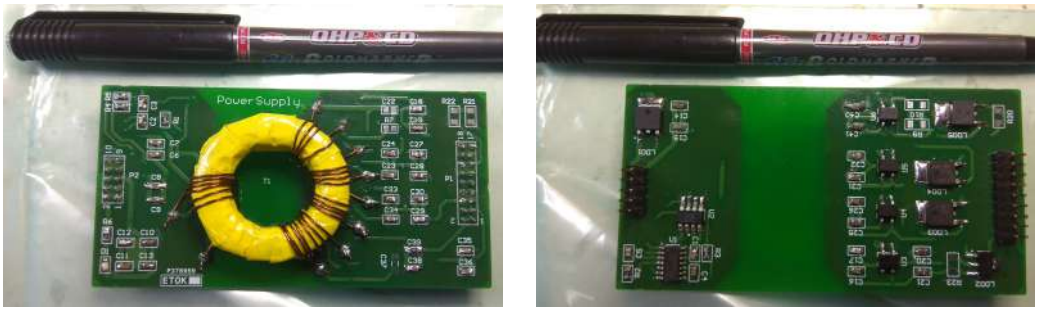


Figure 4.4: Top view of Gate Driver

The gate driver IC ISO5852 has advanced feature like Desat protection, soft turn off, undervoltage protection, minimum common mode transient immunity (100V/ns) etc. It has high isolation surge withstand voltage, 12800 V_{pk}. This could help in reduction of the overall size of gate driver section. *Fig.4.4* shows the designed gate driver PCB. sensing and other circuitry sections are marked in Figure. PCB is designed in such a way that it ensures smaller size board with 2.7mm thickness and four layer FR4 material.

An isolated power supply consisting of high isolation voltage rating is specifically de-



(a) Top view (b) Bottom View

Figure 4.5: Power Supply

signed for the gate driver. This supply Is designed such that it can with stand large dv/dt and isolation voltage requirements. In this design, power supply of the gate driver is isolated using galvanic isolation of transformer as shown in *Fig.4.5*. Isolated power supply boards are mounted at the back of the gate driver board (yellow coloure border shown in *Fig.4.4*) generating +15 /-2.5V gate supplies. +5 /-5V supplies are for powering up sensing ICs. Since, the gate driver supply and signal input supply are separate; the overall system has two grounds excluding the driver isolation side. This separation will provide two paths for common mode current to flow through ground potential.

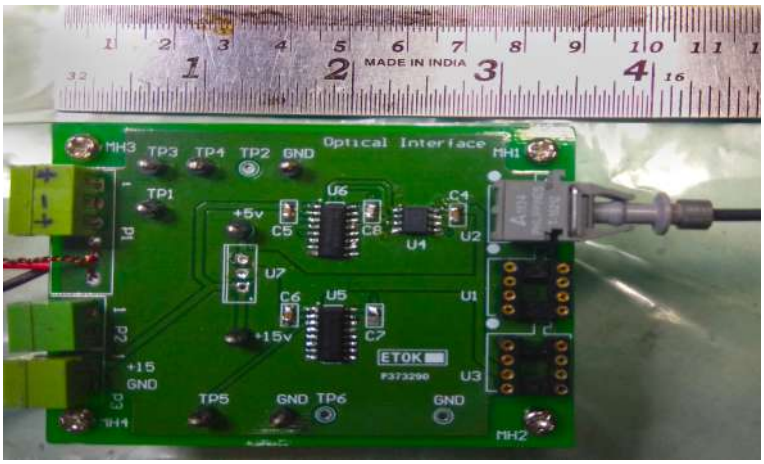


Figure 4.6: Optical Interface Card

To mitigate gate pulse signal contamination due to common mode noise, gate signal is transmitted using an optical interface card, which completely isolates the gate drivers from control board. *Fig.4.6* shows the optical interface card used for transmitting the PWM to gate driver via optical cables. Optical interface card consists of pull up circuit for fault reciever and level shifter circuit for PWM Transmission.

The individual components of the setup are assembled together to perform the DPT. The entire DPT setup is shown in *Fig.4.7*. The DC bus voltage to the DPT setup is adjusted

by using an autotransformer as shown in *Fig.4.7*.

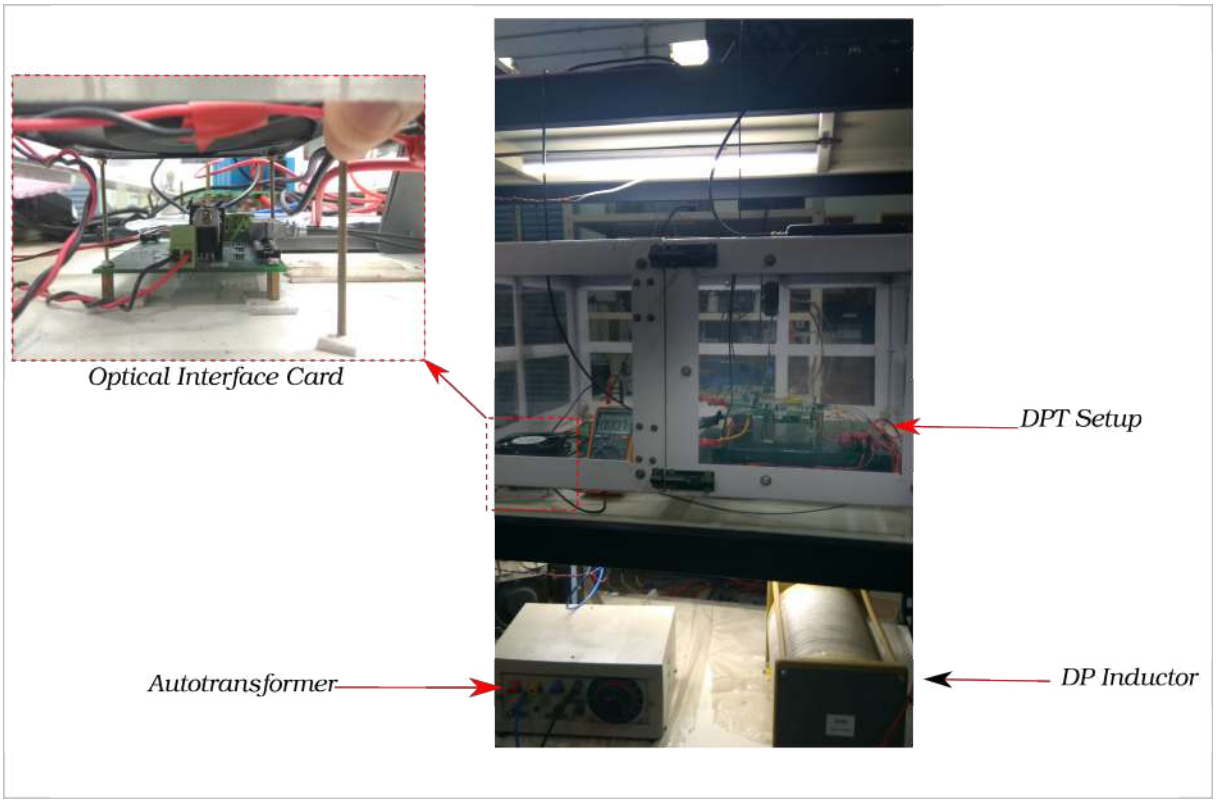


Figure 4.7: Double Pulse Test Setup

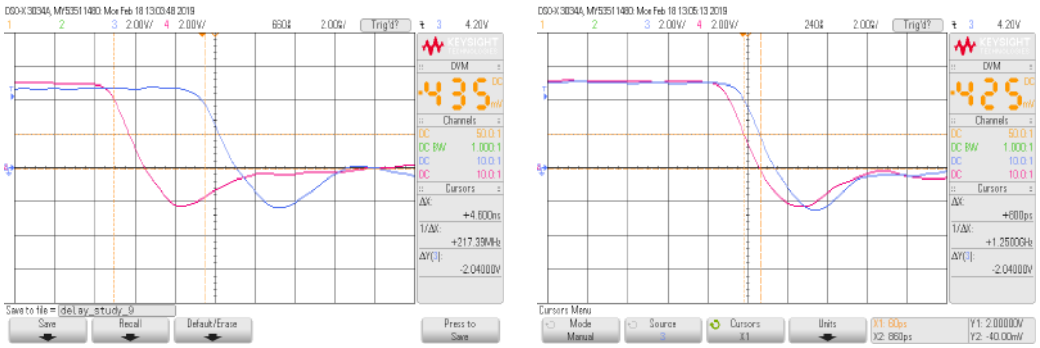
CHAPTER 5

HARDWARE RESULTS

Hardware implementation of designed circuit were discussed in previous chapter, designed gate driver and CREEs latest silicon carbide device were tested in Double Pulse test at 400 to 800V DC Bus. Experimental results for all studies were presented in this chapter.

5.1 Gate Pulse Comparison

At smaller DC voltages, Devices connected in series shows different rise time and fall time. This led to primary investigation on Gate voltages, driving circuits in pulse generator etc. It is found that the length of optical cable connected to gate drivers from optical interface card is different. Length of two cables differ by 6cm also each cable has propogation delay of 110ns(for 1meter length). The hardware results reveals that the input gate pulses given to gate driver IC differs by 0.3 to 3.5ns in rise time and 0.8 to 5.5ns in fall time.



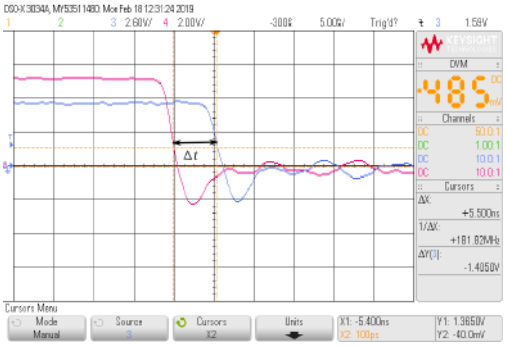
(a) Maximum observed delay Scale; time: 2ns/div, voltage: 2V/div

(b) Minimum observed delay Scale; time: 2ns/div, voltage: 2V/div

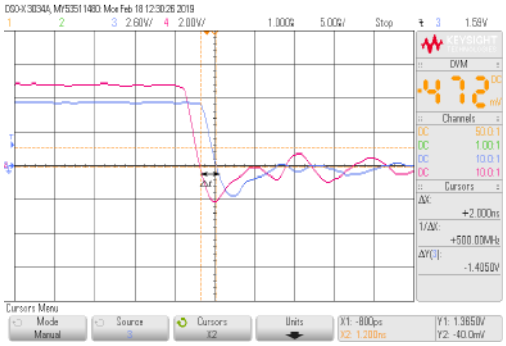
Figure 5.1: DPT 2^{nd} pulse fall time

The time delay observed in second pulse is 0.7ns(minimum) and 4.6ns(maximum) as shown in *Fig.5.1*. This difference in delay is observed due to variation in pulse feeded to optical interface card, i.e., for every press on switch in analog pulse generator, position of pulse changes and also time taken for this pulse to reach level shifter and optical

transmitter is different due to track length difference in OIC.



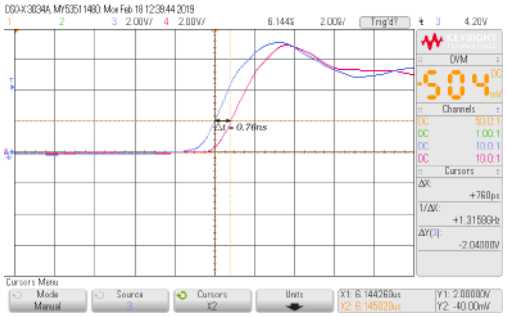
(a) Maximum observed delay Scale; time: 5ns/div, voltage: 2V/div



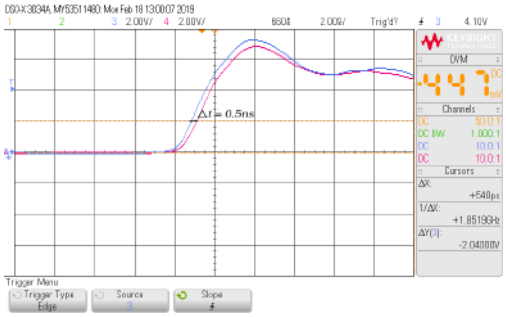
(b) Minimum observed delay Scale; time: 5ns/div, voltage: 2V/div

Figure 5.2: DPT 1^{st} pulse fall time

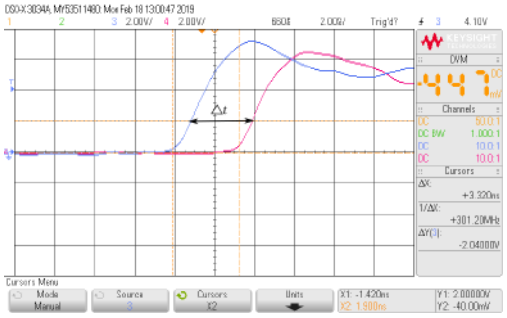
From *Fig.5.2* minimum fall time delay occured is 2ns and maximum fall time delay is 5.5ns.



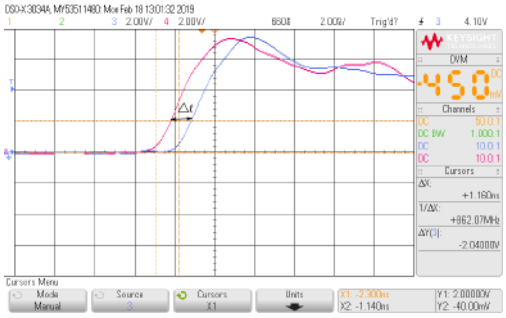
(a) Maximum observed delay Scale; time: 2ns/div, voltage: 2V/div



(b) Minimum observed delay. Scale; time: 2ns/div, voltage: 2V/div



(c) Maximum observed delay. Scale; time: 2ns/div, voltage: 2V/div



(d) Minimum observed delay. Scale; time: 2ns/div, voltage: 2V/div

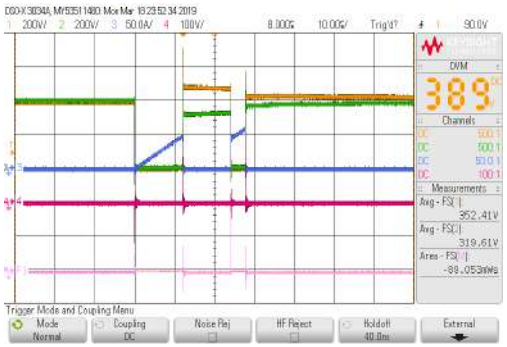
Figure 5.3: DPT rise time

Absolute maximum rise time delay is 5.5ns and minimum delay is 0.5ns.

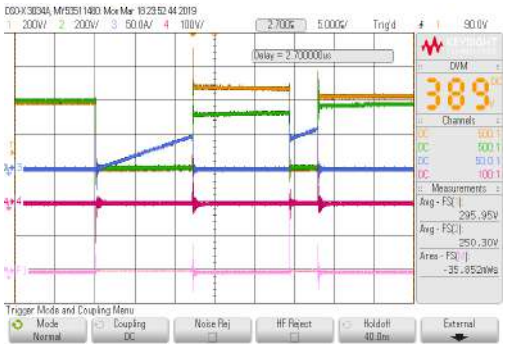
5.2 Snubber Circuit

In chapter 3, we have seen the simulation for different capacitors that are available in market. Considering the voltage deviation and losses, the 22nF capacitor were chosen for hardware implementation. But to make sure that there is no huge difference in simulation and hardware results, selection of snubber capacitor were done experimentally by changing the capacitors that are readily available. Small resistance in the range of mΩs are not readily available and are not recommended because of its smaller ratings. In hardware implementation, 2.5Ω resistance were chosen for snubber study. As the snubber resistance increases, losses will also increase accordingly which affects overall efficiency of converter. Studies were done with two different external gate resistances. Since the leakage current of device is so small(in nanoAmperes), a 100kΩ Resistors were chosen as balancing resistance (R_b) for static voltage balancing.

Case 1.a: 1nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 14.7Ω.



(a) Double Pulse 1 Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div



(b) Double Pulse 2 Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

(c) Double Pulse 3 Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

(d) Double Pulse 4 Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

Figure 5.4: DP Waveforms for 1nF snubber capacitor

Due to pulse contamination, 4 sets of Double pulse waveform were obtained as shown in *Fig.5.4*. Studies were done selecting one such set. *Fig.5.5*. shows the selected set and *Fig.5.6* shows the falling and rising edge of second pulse.

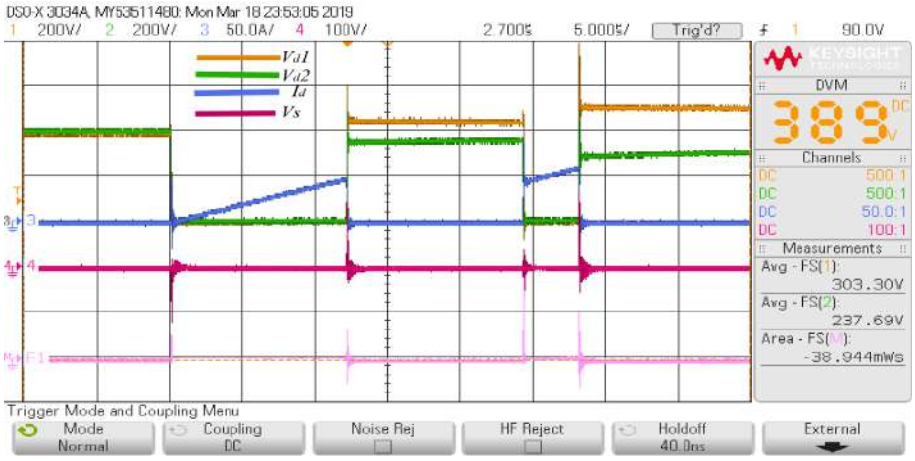
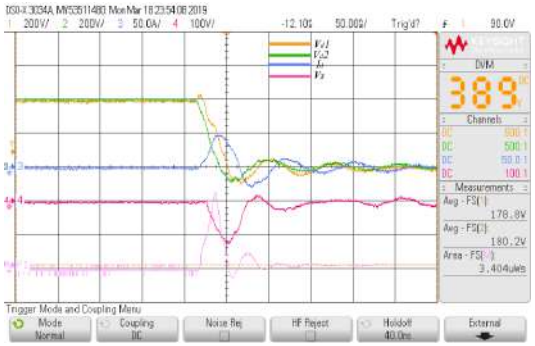
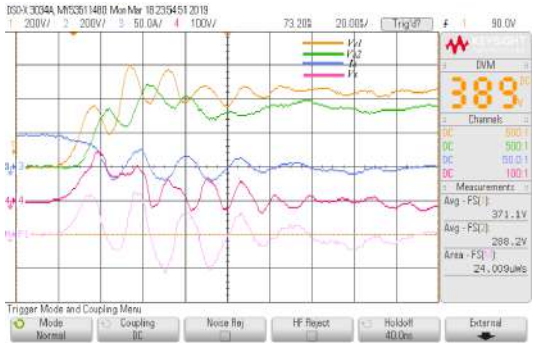


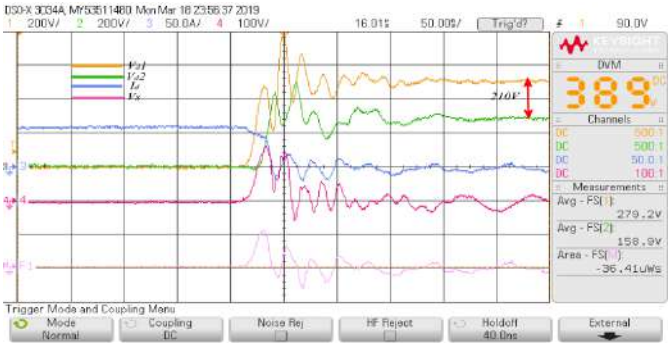
Figure 5.5: DP waveform for Snubber capacitor, C_s=1nF, Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div



(a) Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div



(b) Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div



(c) Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

Figure 5.6: DP Waveform for 1nF snubber capacitor: Rising and falling edge capturing.

At 800V DC voltage, top device voltage(Yellow) differ from bottom device voltage(green) by approximately 210V. Light pink coloured waveform reveals switching energy loss at that instant of capturing. Therefore 1nF snubber capacitor is not suitable or sufficient for high voltage application.

Case 1.b: 1nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 184.7Ω.

(a) Double Pulse 1. Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

(b) Double Pulse 2 Scale; time: 5μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

(c) Double Pulse 3 Scale; time: 10μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

Figure 5.7: DP Waveforms for 1nF snubber capacitor, R_g=184.7Ω

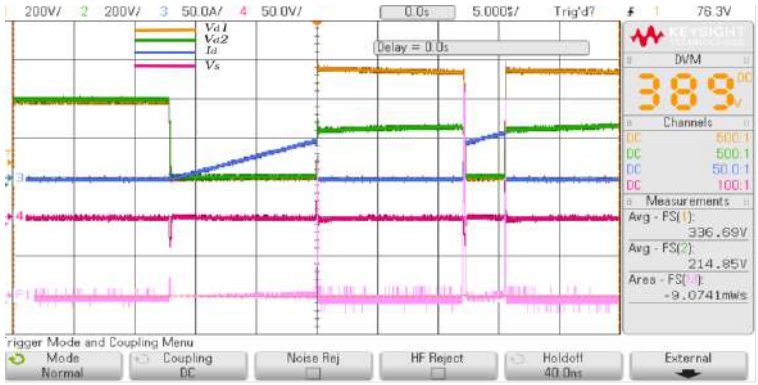


Figure 5.8: DP waveform for Snubber capacitor, C_s=1nF, R_g=184.7Ω Scale; time: 5μs/div, device voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

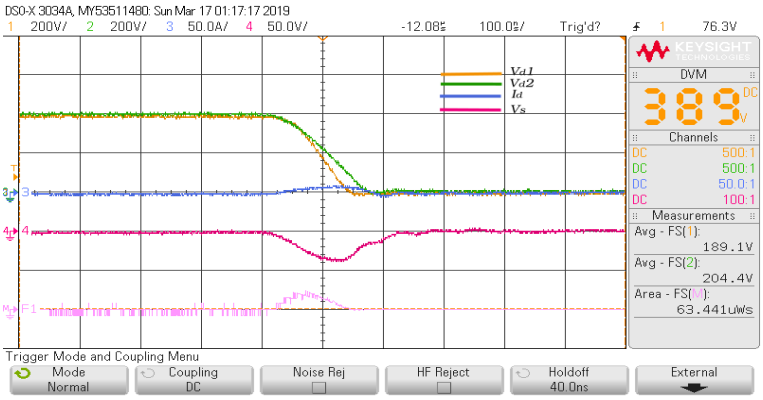


Figure 5.9: Turn on time capturing, C_s=1nF, R_g=184.7Ω Scale; time: 100ns/div, device voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

Fig.5.7. depicts three different waveforms obtained due to pulse contamination from optical interface card.
The device voltages (yellow and green waveform) differences can be noticed in above oscilloscope output. As you can observe in *Fig.5.9*, Snubber circuit has least effect during turn on time.

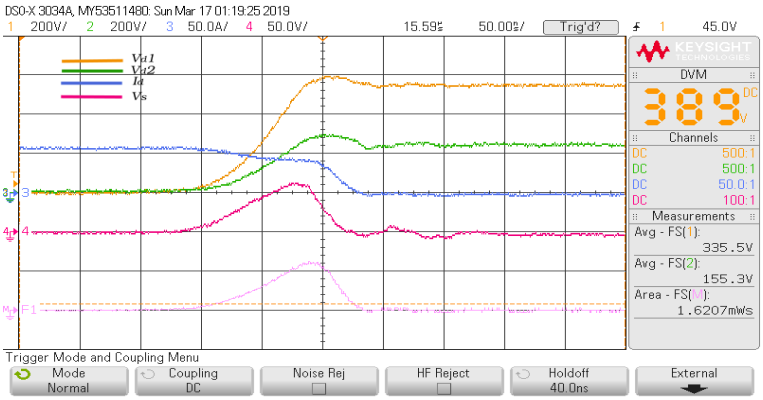
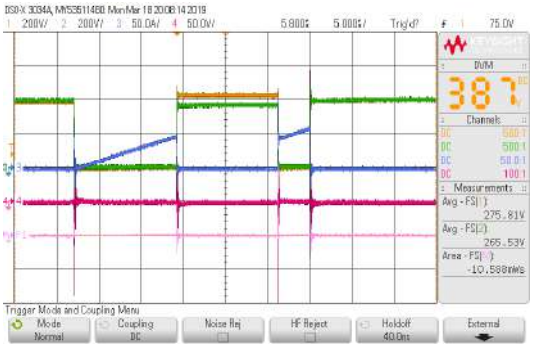


Figure 5.10: Turn Off time capturing, C_s=1nF, R_g=184.7Ω Scale; time: 50ns/div, device voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

Here, R_{gext}=180Ω is used only to check the feasibility of series connection. Turn off Voltage deviation in devices with 1nF snubber capacitor is shown in *Fig.5.10*. A deviation of 300V (Between yellow and green voltage waveform) is seen when 800V DC voltage applied. The switching loss(pink colour) is also shown in *Fig.5.9* and *Fig.5.10*.

- Turn on energy loss(E_{on}) per device = 0.063mJ.
- Turn off energy loss(E_{off})per device = 1.6203mJ.

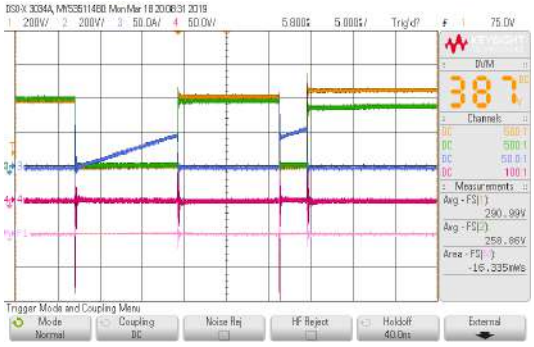
Case 2.a: 2.2nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 14.7Ω.



(a) Double Pulse 1 Scale; time: 5μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

(b) Double Pulse 2 Scale; time: 5μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

(c) Double Pulse 3 Scale; time: 5μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div



(d) Double Pulse 4 Scale; time: 5μs/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

Figure 5.11: DP Waveforms for 2.2nF snubber capacitor

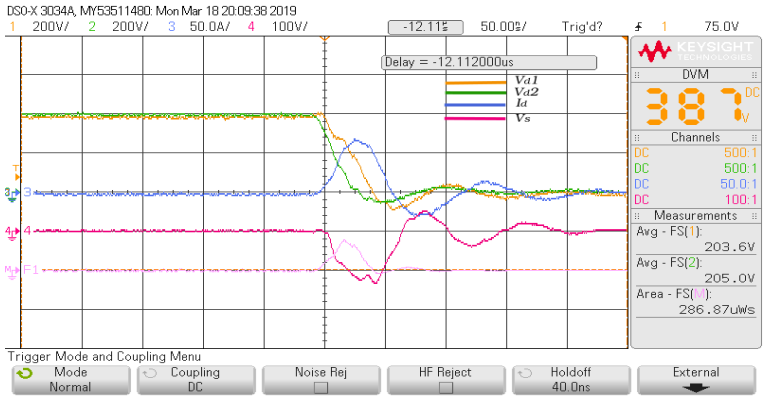


Figure 5.12: First Turn on Edge capturing, C_s=2.2nF, R_g=14.7Ω Scale; time: 50ns/div, device voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

The turn on edge for first pulse of double pulse (*Fig.5.11(d)*) is shown in *Fig.5.12*. The switching loss of top device for this case is 0.286mJ. Similarly first pulse turn off switching loss is 0.065mJ shown in *Fig.5.13*.

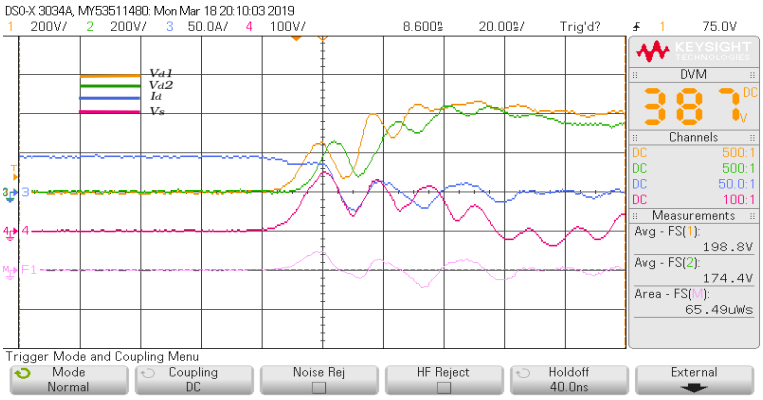
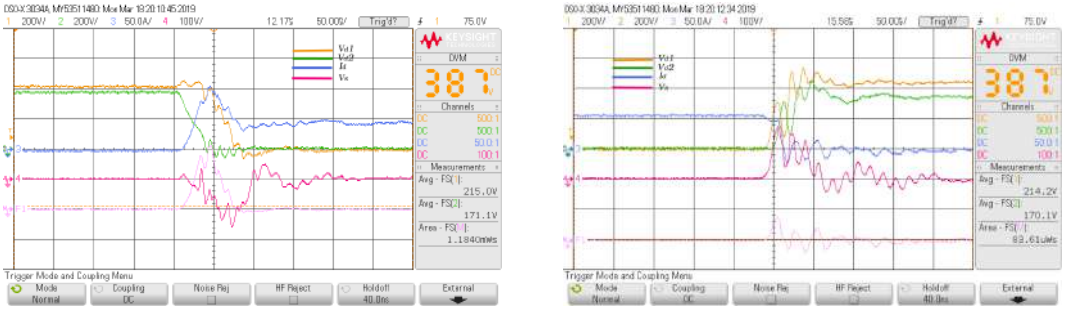


Figure 5.13: First Turn off Edge capturing, C_s=2.2nF, R_g=14.7Ω Scale; time: 20ns/div, device voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

Similarly, the waveforms for second pulse turn on and turn off edges are shown in *Fig.5.14*. The turn on energy loss is 1.18mJ and turn off loss is 0.083mJ. Therefore total switching loss is 1.614mJ.



(a) Turn on Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

(b) Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

Figure 5.14: Second pulse Waveforms for 2.2nF snubber capacitor

Case 2.b: 2.2nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 184.7Ω.

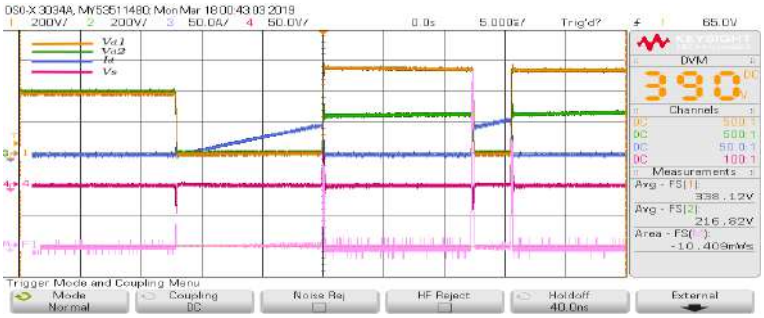
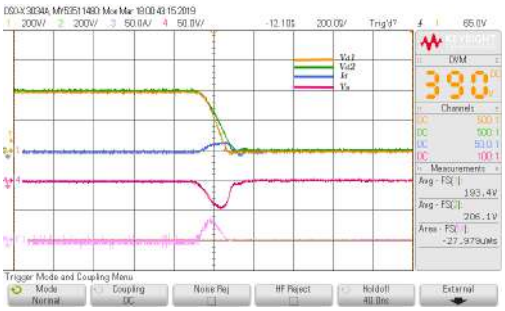
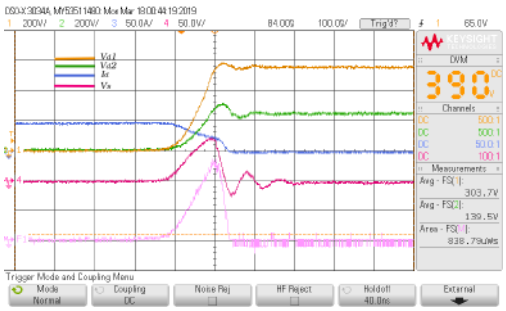


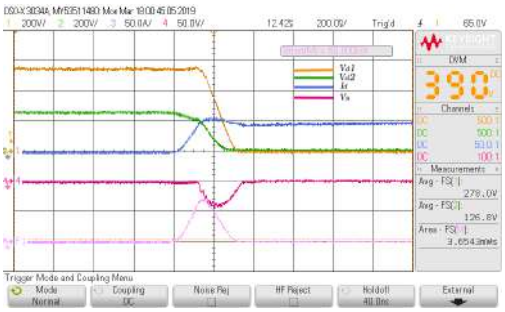
Figure 5.15: Double Pulse waveform, C_s=2.2nF, R_g=184.7Ω Scale; time: 5μs/div, device voltage: 200V/div, current: 50A/div, snubber voltage:50V/div



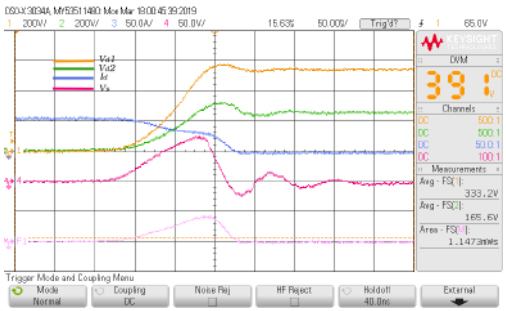
(a) First Turn on Scale; time: 200ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div



(b) First Turn off Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div



(c) Second Turn on, Scale; time: 200ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

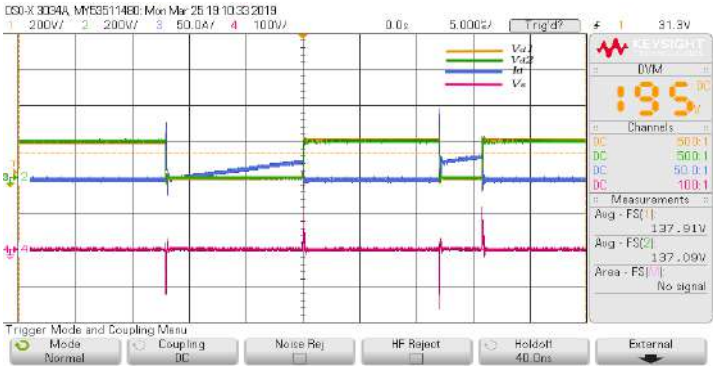


(d) Second Turn off, Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

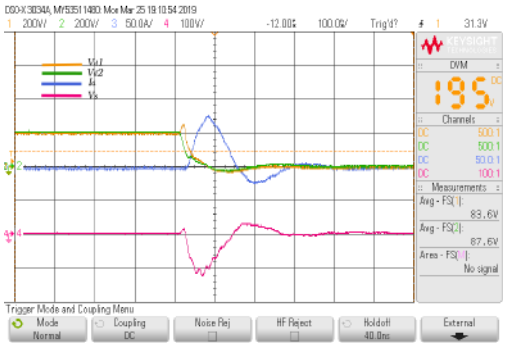
Figure 5.16: Turn on and turn off switching Waveforms for 2.2nF snubber capacitor, $R_g = 184.7\Omega$.

Therefore, from these waveforms Total switching loss of device is found to be 5.612mJ. So overall switching loss if two devices connected in series will be 11.224mJ assuming that device parameters are approximately same. Total losses were calculated by collecting waveform details in excel datasheet and analysing the waveform completely. It is also found that overall losses increases with increase in snubber capacitance and difference in pulse contamination observed before.

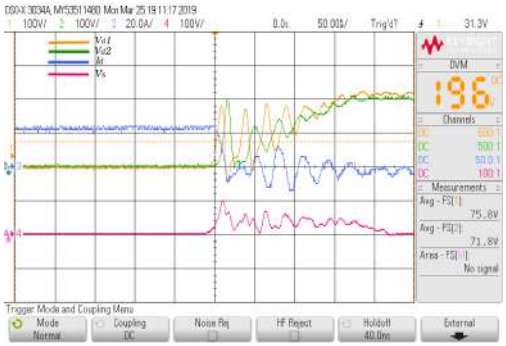
Case 3.a: 11nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 14.7Ω.



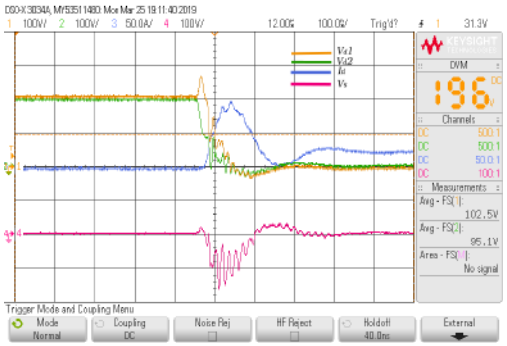
(a) Double Pulse waveform, C_s=11nF, R_g=14.7Ω Scale; time: 5μs/div, device voltage: 200V/div, current: 50A/div, snubber voltage:100V/div



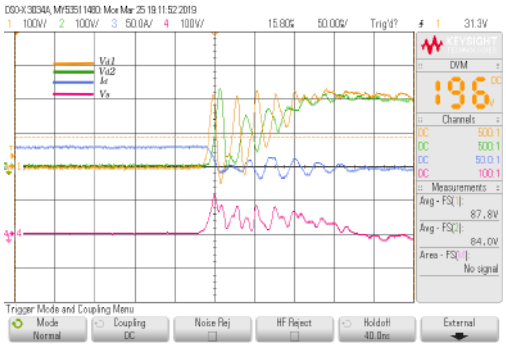
(b) First Turn on *Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div*



(c) First Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div, snubber voltage:100V/div



(d) Second Turn on Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

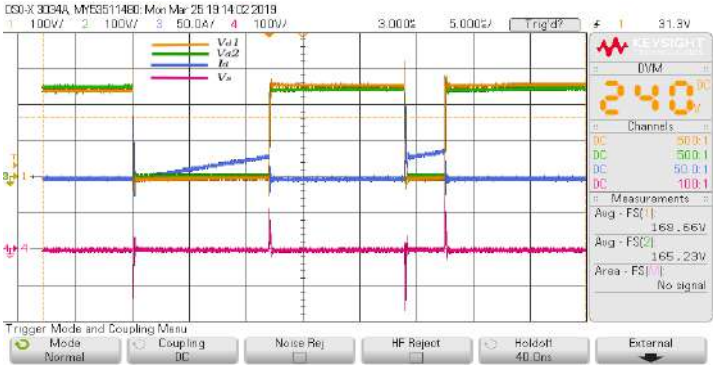


(e) Second Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:100V/div

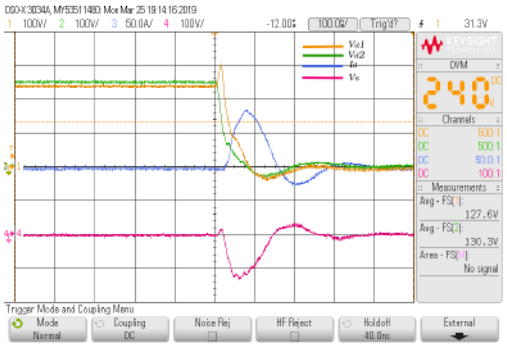
Figure 5.17: Double pulse switching Waveforms for 11nF snubber capacitor, R_g = 14.7Ω, V_{DC}=400V

Fig.5.17 shows DP waveform and all four switching edges of DP waveform when tested the setup at 400V DC Bus. Figure clearly shows that 400V DC bus, the voltage deviation is less than 10V(Difference in device 1 voltage*(yellow)* and bottom device voltage*(green)*).

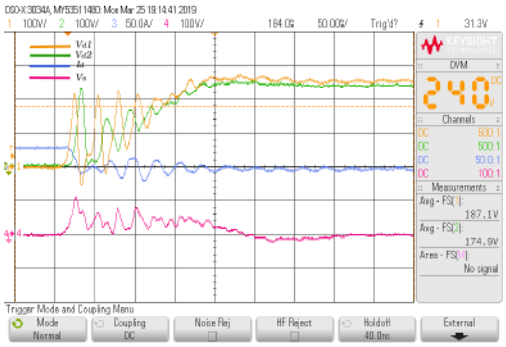
Fig.5.18 shows DP waveform and all four switching edges of DP waveform when tested the setup at 500V DC Bus.



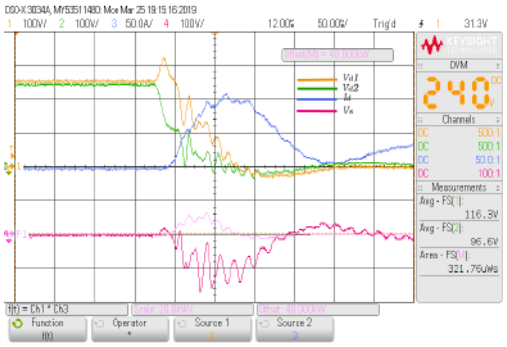
(a) Double Pulse waveform, C_s=11nF, R_g=14.7Ω Scale; time: 5μs/div, device voltage: 100V/div, current: 50A/div, snubber voltage:100V/div



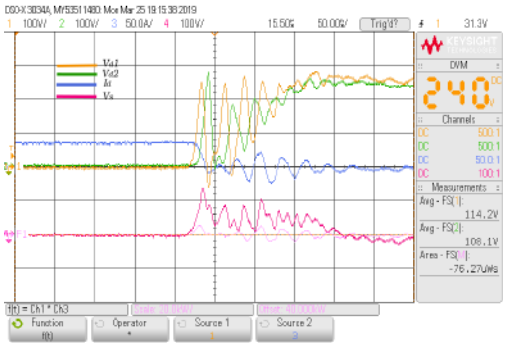
(b) First Turn on Scale; time: 100ns/div, voltage: 100V/div, current: 50A/div, snubber voltage:100V/div



(c) First Turn off, Scale; time: 50ns/div, voltage: 100V/div, current: 20A/div, snubber voltage:100V/div



(d) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, current: 50A/div, snubber voltage:100V/div

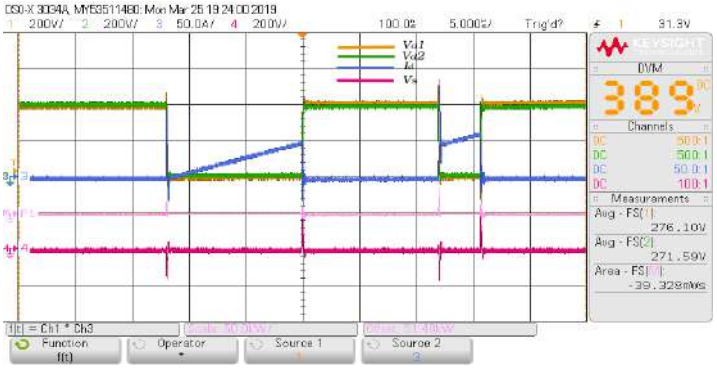


(e) Second Turn off, Scale; time: 50ns/div, voltage: 100V/div, current: 50A/div, snubber voltage:100V/div

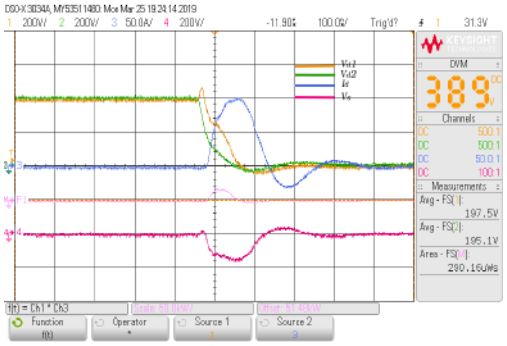
Figure 5.18: Double pulse switching Waveforms for 11nF snubber capacitor, R_g = 14.7Ω, V_{DC}=500V

Analysing the waveforms of switching edges, Voltage deviation in this case is found to be 28V. Because of higher di/dt, device has higher overshoot in current at the beginning of turn on edge.

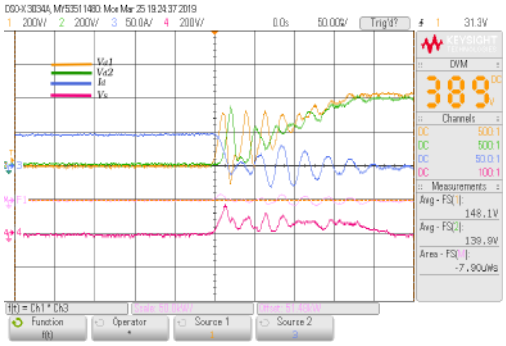
DP waveform and all four edges of DP waveform when tested the setup at 800V DC Bus is shown in *Fig.5.19*.



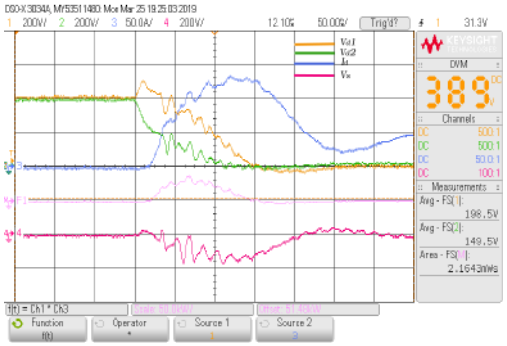
(a) Double Pulse waveform, C_s=11nF, R_g=14.7Ω Scale; time: 5μs/div, device voltage: 200V/div, current: 50A/div, snubber voltage:200V/div



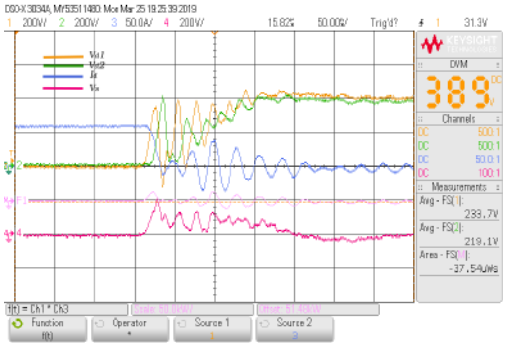
(b) First Turn on Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div



(c) First Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div



(d) Second Turn on Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div

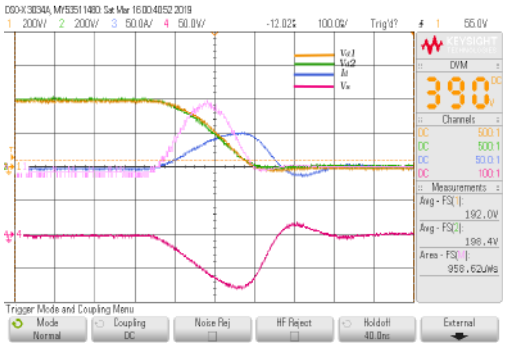


(e) Second Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div

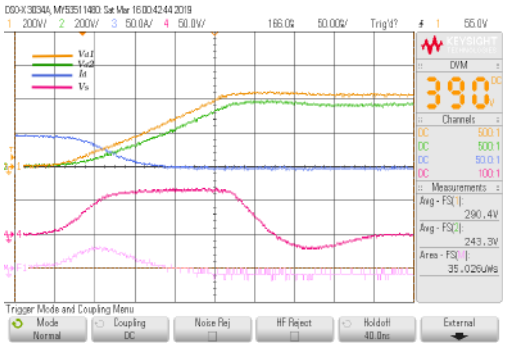
Figure 5.19: Double pulse switching Waveforms for 11nF snubber capacitor, R_g = 14.7Ω, V_{DC}=800V

Voltage deviation in this case is 48V. Device switching loss is calculated by analysing the excel data of above waveform and found to be 2.409mJ.

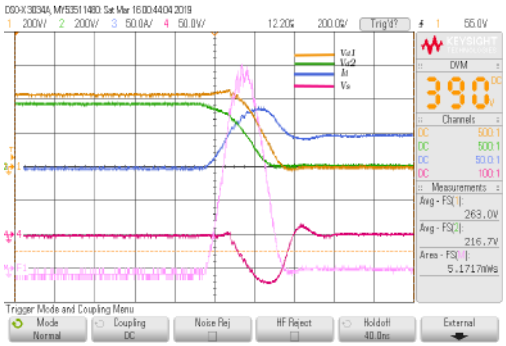
Case 3.b: 11nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 184.7Ω.



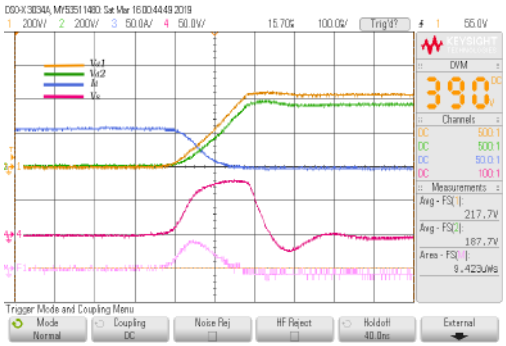
(a) First Turn on Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div



(b) First Turn off Scale; time: 100ns/div, voltage: 200V/div, current: 20A/div, snubber voltage: 50V/div



(c) Second Turn on Scale; time: 200ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

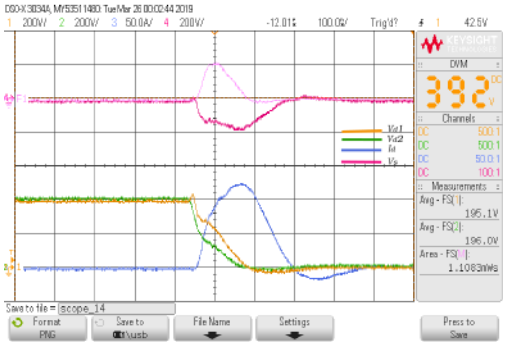


(d) Second Turn off Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

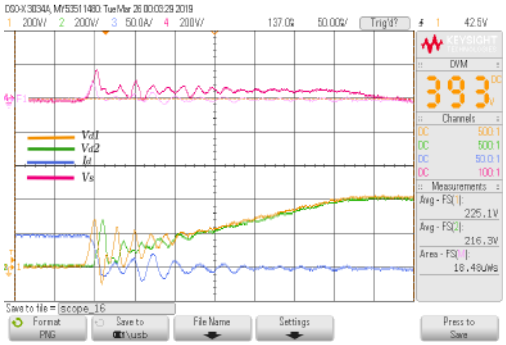
Figure 5.20: Double pulse switching Waveforms for 11nF snubber capacitor, R_g = 184.7Ω, V_{DC}=800V

Fig.5.20 reveals all four edges of DP waveform when tested the setup at 800V DC Bus. Dynamic voltage difference is 54V. The switching loss of one device is found to be 1.905mJ.

Case 4.a: 22nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 14.7Ω.

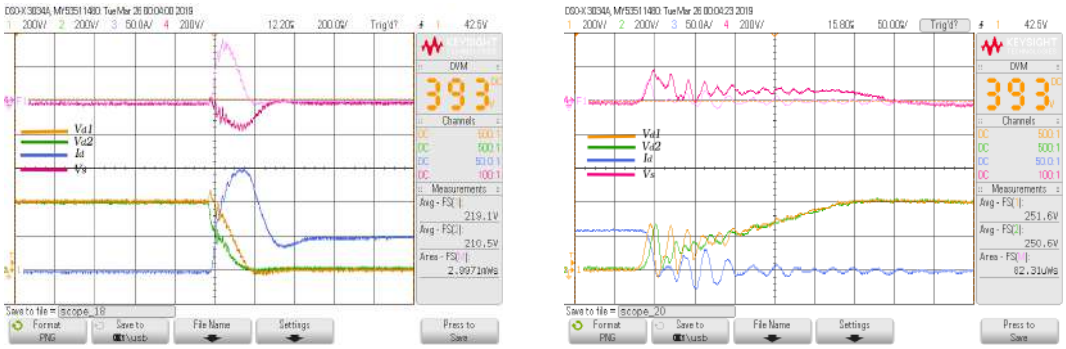


(a) First Turn on Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div, snubber voltage: 200V/div

Figure 5.21: First pulse switching Waveforms for 22nF snubber capacitor, R_g = 14.7Ω, V_{DC}=800V



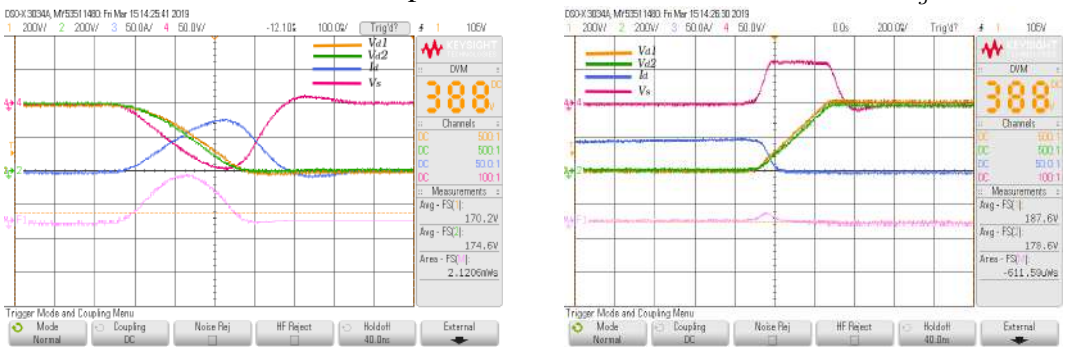
(a) Second Turn on Scale; time: 200ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:200V/div

(b) Second Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div, snubber voltage: 200V/div

Figure 5.22: Second pulse switching Waveforms for 22nF snubber capacitor, R_g = 14.7Ω, V_{DC}=800V

Fig.5.21 and *Fig.5.22* depicts first and second turn on and turn off edges of Double pulse at 800V DC Bus, dynamic voltage difference at 800V DC Bus is less than 20V. Switching energy loss per device in this case is calculated and found to be 4.20619mJ.

Case 4.b: 22nF WIMA Film capacitor and 2.5Ω Resistance in series, R_g= 184.7Ω.



(a) First Turn on Scale; time: 100ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

(b) First Turn off Scale; time: 200ns/div, voltage: 200V/div, current: 20A/div, snubber voltage: 50V/div

(c) Second Turn on Scale; time: 200ns/div, voltage: 200V/div, current: 50A/div, snubber voltage:50V/div

(d) Second Turn off Scale; time: 100ns/div, voltage: 200V/div, current: 20A/div, snubber voltage: 50V/div

Figure 5.23: Double pulse switching Waveforms for 22nF snubber capacitor, R_g = 184.7Ω, V_{DC}=800V

The switching energy loss for Case.4.b is 8.046548mJ/device.

5.3 Effect of R_G on Dynamic Voltage

This section showcase the hardware results of Double Pulse Test conducted for different gate resistances connected in gate driver. At minimal gate resistance, the peak overshoot is almost 300%. So device is not tested above 100V DC Bus for gate resistance below 10Ω (Excludes internal resistance of 4.7Ω). Therefore, hardware test were done for 10-200Ω gate resistance at 400V DC bus voltage.
Case 1: R_g= 14.7Ω.

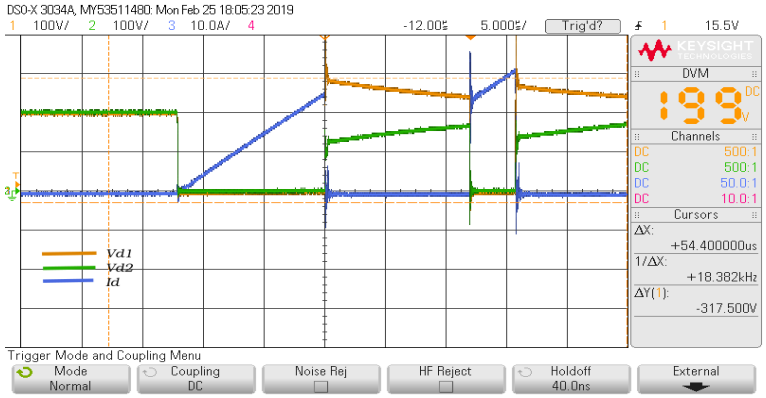
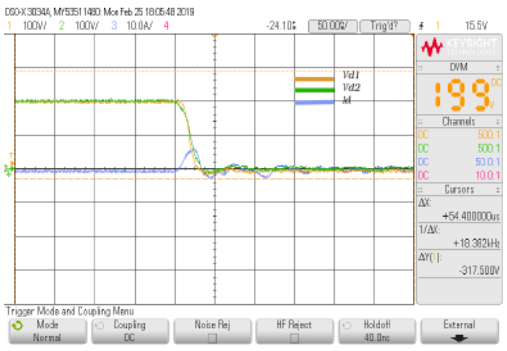
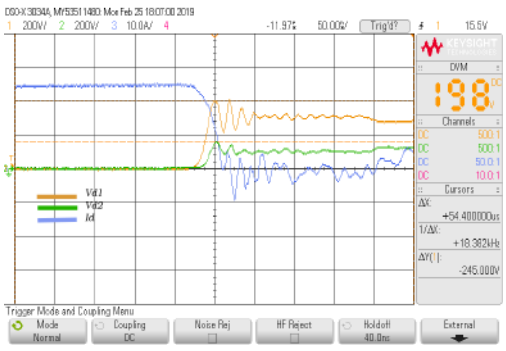


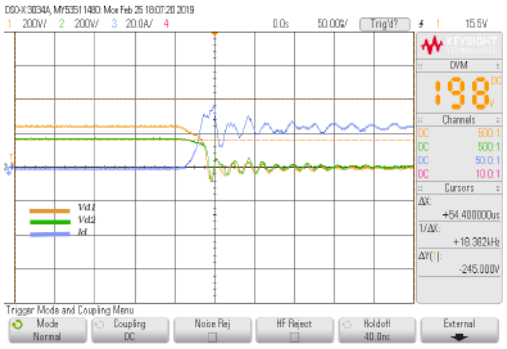
Figure 5.24: Double Pulse waveform, R_g=14.7Ω Scale; time: 5μs/div, device voltage: 100V/div, current: 10A/div



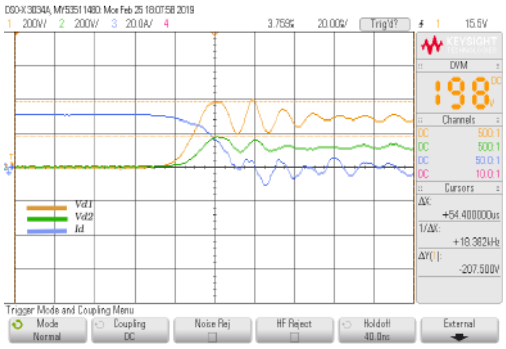
(a) First Turn on Scale; time: 50ns/div, voltage: 100V/div, current: 10A/div



(b) First Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 200V/div, current: 20A/div

Figure 5.25: Double Pulse test waveform, R_G=14.7Ω

Switching Transients in device is shown in *Fig.5.25.*, dynamic difference between top device (yellow) and bottom device (green) also varies slightly with change in gate resistance. Voltage slew rate and amount of overshoot also dependent on gate resistances, which we will see in upcoming cases.

Case 2: R_g= 51.7Ω, V_{DC}=400V.

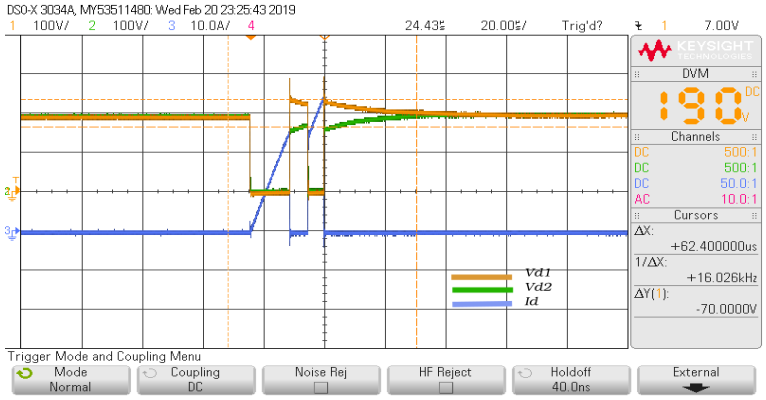
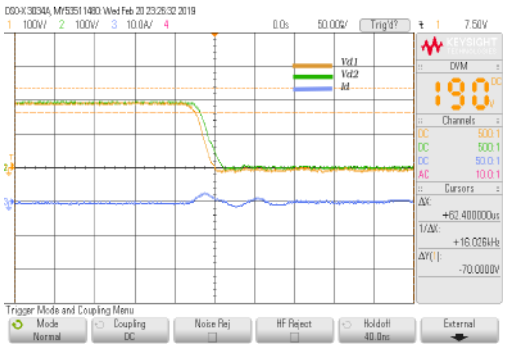
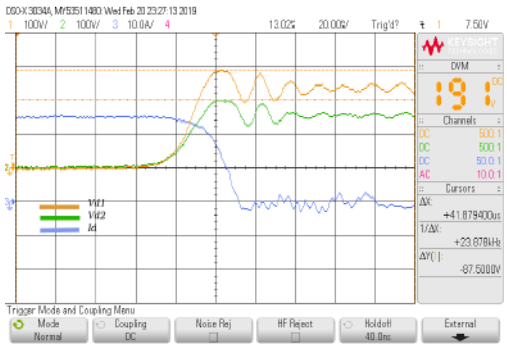


Figure 5.26: Double Pulse waveform, R_g=14.7Ω Scale; time: 20μs/div, device voltage: 100V/div, current: 10A/div

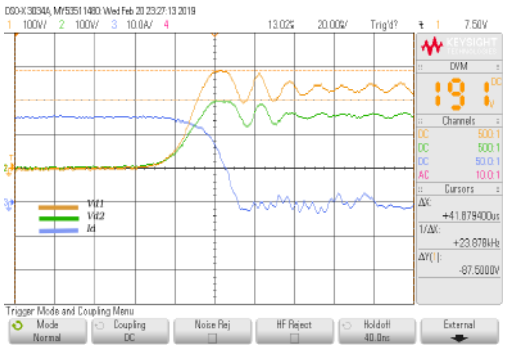
Multiple waveforms were taken due to pulse contamination and Waveform that repeats again after a series of sets were taken into consideration, is shown in *Fig.5.26* and corresponding turn on and off edges were shown below in *Fig.5.27.*



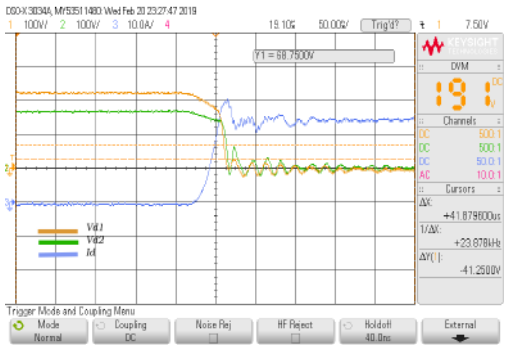
(a) First Turn on Scale; time: 50ns/div, voltage: 100V/div, current: 10A/div



(b) First Turn off Scale; time: 20ns/div, voltage: 100V/div, current: 10A/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, current: 10A/div



(d) Second Turn off Scale; time: 100ns/div, voltage: 100V/div, current: 10A/div

Figure 5.27: Double Pulse test waveform, R_G=51.7Ω, V_{DC}=400V

Case :3 R_g= 72.7Ω, V_{DC}=400V.

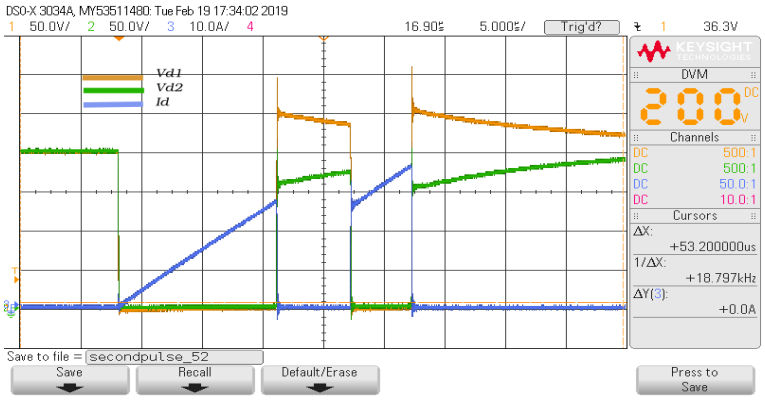
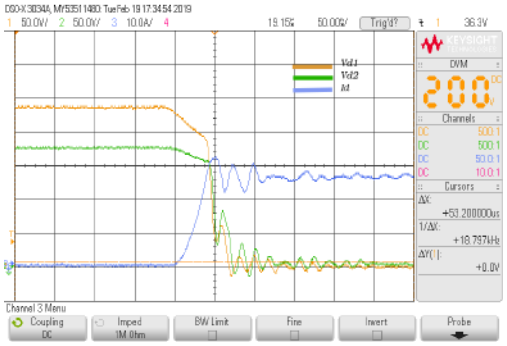
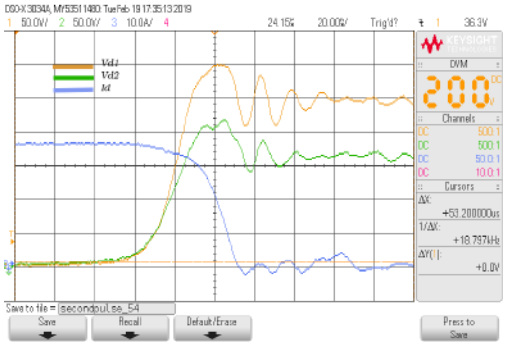


Figure 5.28: Double Pulse waveform, R_g=72.7Ω Scale; time: 5μs/div, device voltage: 50V/div, current: 10A/div

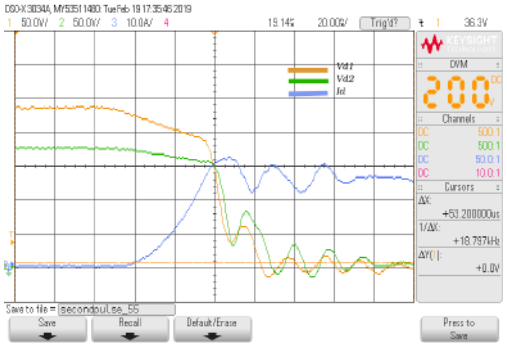
Multiple waveforms were taken into account due to pulse contamination and one set of result is shown in *Fig.5.28* and *Fig.5.29*.



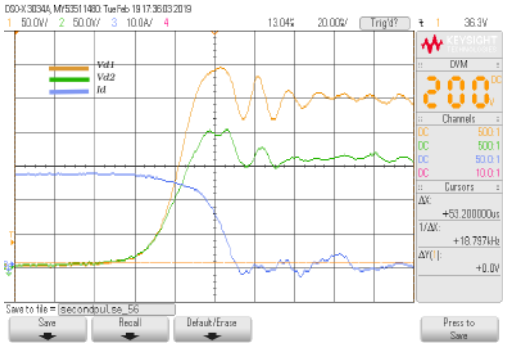
(a) First Turn on Scale; time: 50ns/div, voltage: 50V/div, current: 10A/div



(b) First Turn off Scale; time: 20ns/div, voltage: 50V/div, current: 10A/div



(c) Second Turn on Scale; time: 20ns/div, voltage: 50V/div, current: 10A/div



(d) Second Turn off Scale; time: 20ns/div, voltage: 50V/div, current: 10A/div

Figure 5.29: Double Pulse test waveform, R_G=72.7Ω, V_{DC}=400V

Amount of overshoot in voltage and current reduces with increase in gate resitances, but it also increases the switching times parallely.
Case :4 R_g= 104.7Ω, V_{DC}=400V.

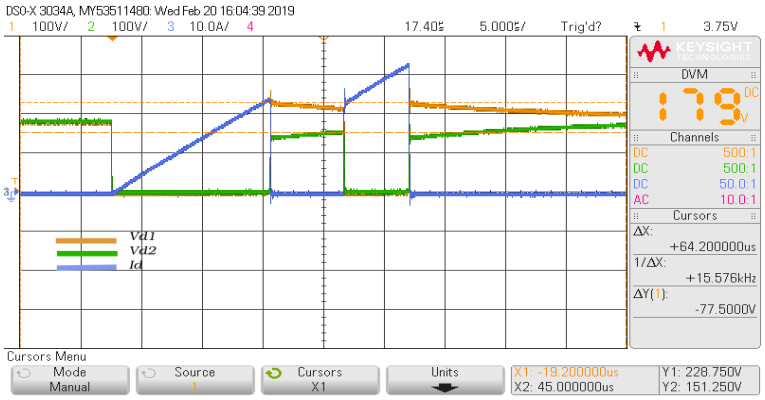
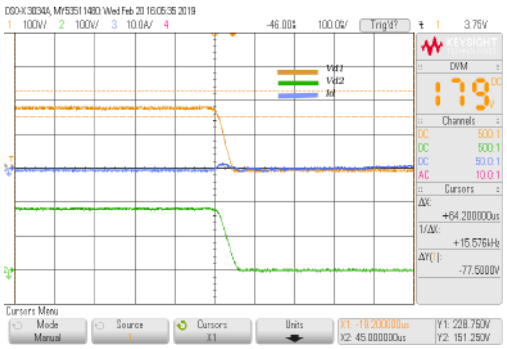
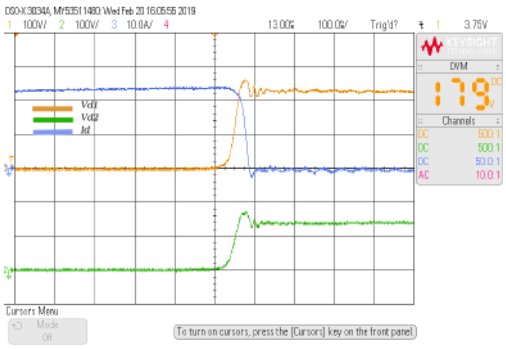


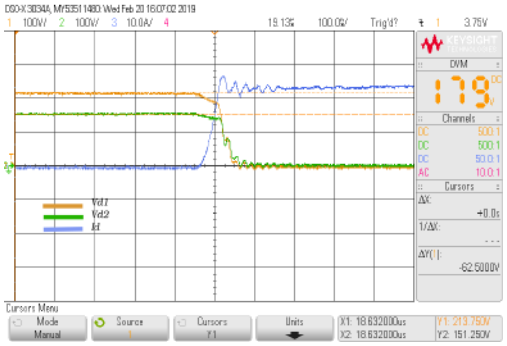
Figure 5.30: Double Pulse waveform, R_g=104.7Ω Scale; time: 5μs/div, device voltage: 100V/div, current: 10A/div



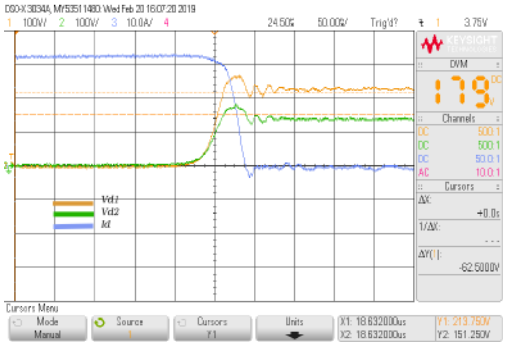
(a) First Turn on Scale; time: 100ns/div, voltage: 100V/div, current: 10A/div



(b) First Turn off Scale; time: 100ns/div, voltage: 100V/div, current: 10A/div



(c) Second Turn on Scale; time: 100ns/div, voltage: 100V/div, current: 10A/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, current: 10A/div

Figure 5.31: Double Pulse test waveform, R_G=104.7Ω, V_{DC}=400V

While analysing all cases,top devices is found to clamps at very high voltage always. But the intensity or magnitude of peak voltage overshoot reduces with rise in gate resistances.

Case :5 R_g= 184.7Ω, V_{DC}=400V.

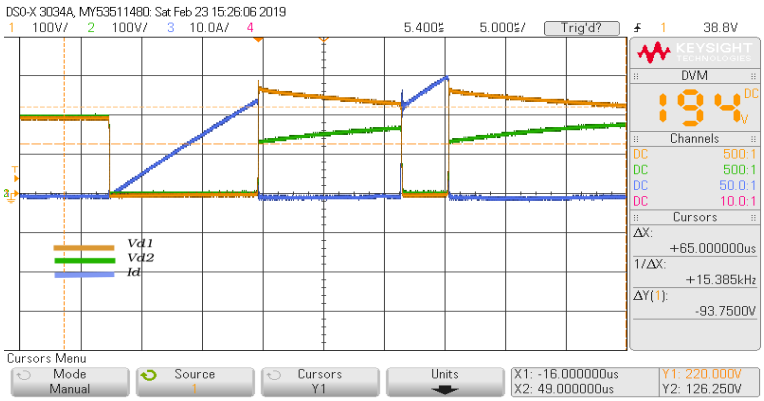
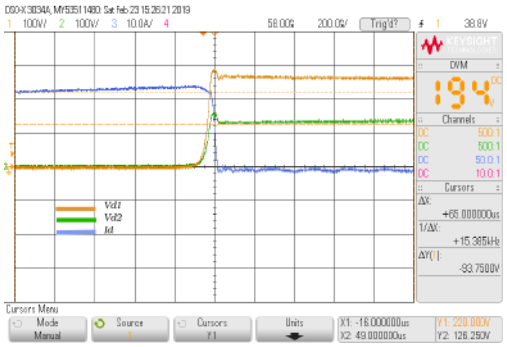
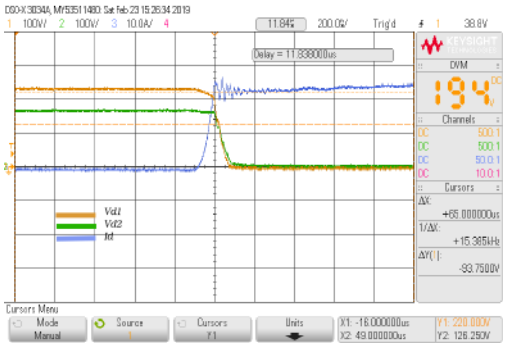


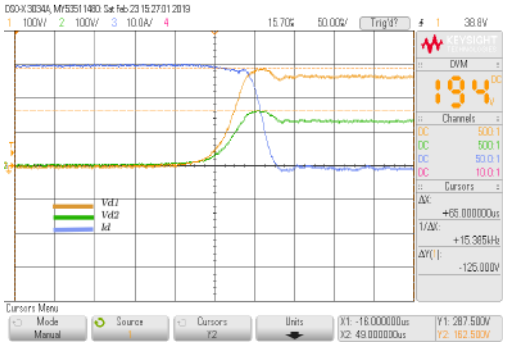
Figure 5.32: Double Pulse waveform, R_g=184.7Ω *Scale; time: 5µs/div, device voltage: 100V/div, current: 10A/div*



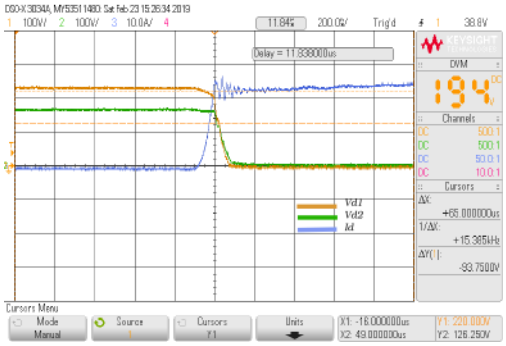
(a) First Turn on Scale; time: 200ns/div, voltage: 100V/div, current: 10A/div



(b) First Turn off Scale; time: 200ns/div, voltage: 100V/div, current: 10A/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, current: 10A/div



(d) Second Turn off, Scale; time: 200ns/div, voltage: 100V/div, current: 10A/div

Figure 5.33: Double Pulse test waveform, R_G=184.7Ω, V_{DC}=400V

In all the five or more cases, top device close to diode clamp or + DC always take maximum voltage compared to bottom device(s). To identify the reason for taking maximum voltage, incremental tests were done by interchanging the devices alone, and by interchanging the gate driver alone etc.
Interchanging device doesn't have much effect in the voltage clamping or dynamic response but these slight difference in transient response is due to internal capacitance (C_{oss}) of device which varies with device voltage, V_{Drain}.

Similarly, interchanging gate driver has no effect on transients at high voltage, but at lower voltage (say 50-100V DC) the gate side parameters like C_{gd} and C_{gs} has impact on voltage sharing and maximum voltage device clamps. It was found that at one particular case, the bottom device rise first than top device due to device parameters.
So from simulation and hardware studies, it is clear that non simultaneous switching will results in unequal voltage sharing among series connected semiconductor devices. The most important factor contributing to dynamic voltage mismatch is the parasitic capacitances from gate to ground. According to *Fig.5.34* where a higher voltage SiC MOSFET is realized by series connecting two SiC MOSFET in series, there is a parasitic capacitance from gate of each device to ground.

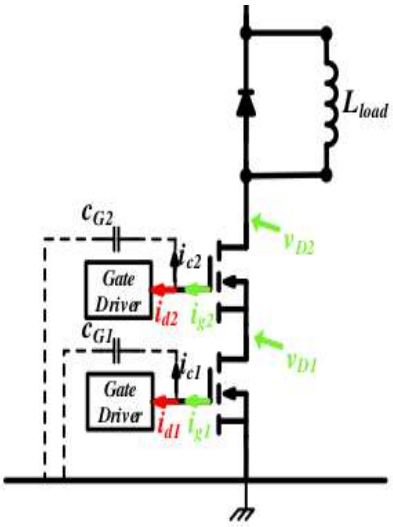


Figure 5.34: Series connected devices in Double Pulse setup

This capacitance is composed of the parasitic capacitance of the power supplies used for passive gate driver, as well as the parasitic capacitance inside the device package from gate to baseplate, where the baseplate is usually grounded. Even if well matched devices and gate drivers are used, during the turn-off process equal currents will flow to the gate drivers (i_{d1}=i_{d2}). Eventhough the gates are well coupled to sources, due to dv/dt at the gate, a secondary gate current will flow from each gate to ground which can be calculated as

$$i_{cn} = c_{Gn}\frac{dV_{Gn}}{dt} \tag{5.1}$$

where dV_G/dt is the rate of voltage change at the gate of the nth MOSFET. The total gate current during turn off is equal to the sum of the gate driver current component and the current through the parasitic capacitor(*Eqn.5.2*). On the other hand, dv/dt at the gate of top MOSFET is equal to dv/dt at the drain of the bottom MOSFET, while the gate of the bottom MOSFET is almost on ground potential which means that even with perfectly matching gate drivers, the total gate current for the top MOSFET will be larger than the bottom one, resulting in faster turn off for it. Faster turn off will results in a higher share of the total dc voltage for the top device

$$i_{gn} = i_{dn} + i_{cn} \tag{5.2}$$

5.4 Voltage Sensing

For voltage sensing, Caddock resistance bridge and normal resistance bridge based opamp circuit were implemented and tested. For measuring the voltages; Lecroy Teledyne oscilloscope, 100MHz 6kV high voltage differential probe(**HVD3605A**) is used to measure drain voltage and a high voltage fiber optical isolated probe (**HVFO103**) is used to measure the sensed voltage. The high voltage isolated probe far surpasses the measurement capabilities and signal fidelity of conventional high attenuation, high voltage differential probes and acquisition systems that rely on galvanic channel-channel and channel-ground HV isolation. This probe setup consists of seperable mini tips, amplifier, optical cable. The amplifier/modulating transmitter is a frequency modulating optical transmitter integrated with a high performance electrical amplifier. The transmitter is battery powered, so there is no direct connection from the floating DUT, providing HV isolation between the Device under test(DUT) and the grounded oscilloscope. Advantage of this probe other than isolation is common mode injection is reduced to greater extent and probe capacitance is very small (25pF) compared to other differential probes.
Fig.5.36 shows the common mode voltage(yellow) of isolation probe when setup is run at 200V DC. it is to be noted that probe tip was hung or vertically positioned in test setup as shown in *Fig.5.35*

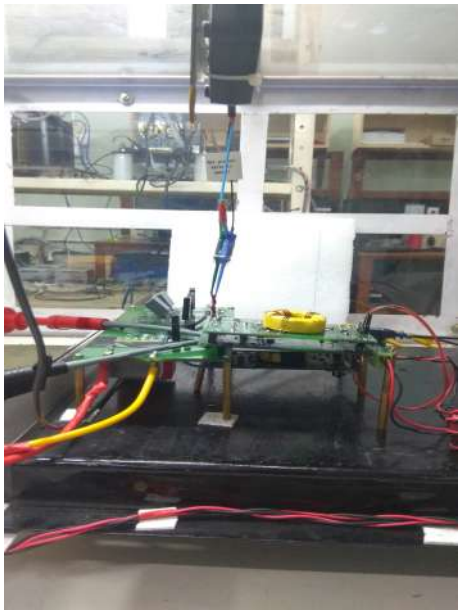
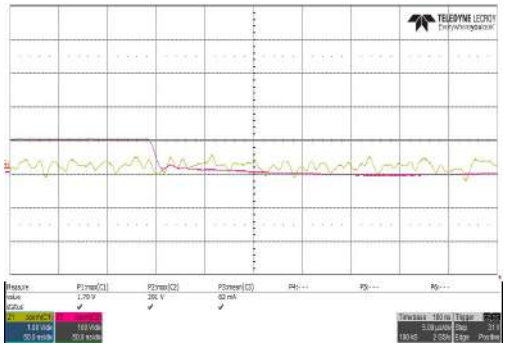
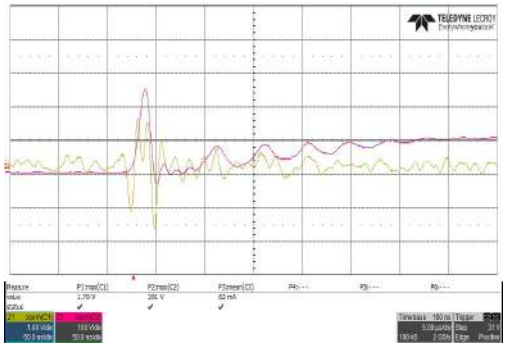


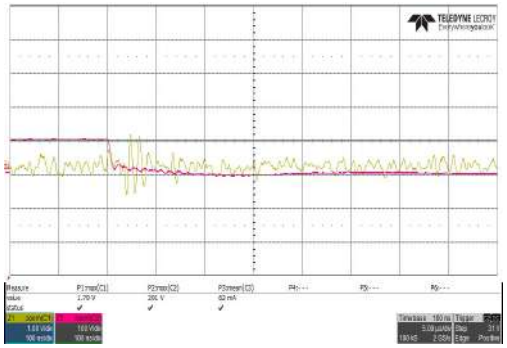
Figure 5.35: Voltage Sensing with optically isolated probe/tip



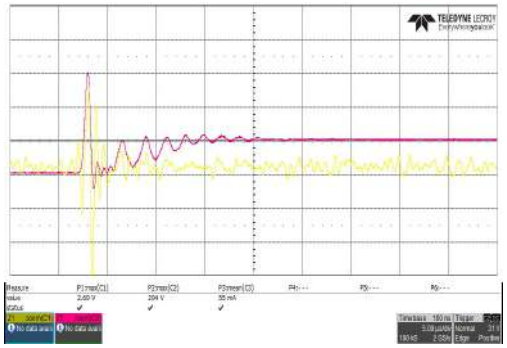
(a) First Turn on Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div

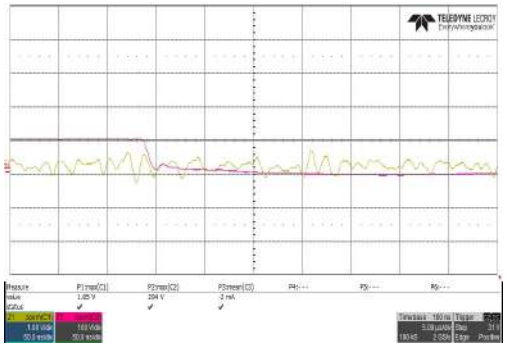


(c) Second Turn on Scale; time: 100ns/div, voltage: 100V/div, common mode volage: 1V/div

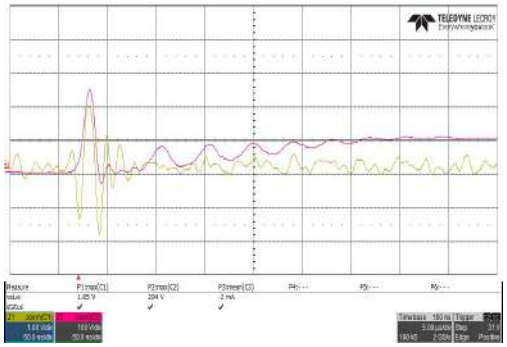


(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div

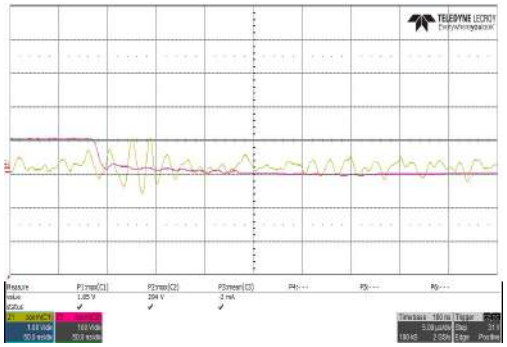
Figure 5.36: Probe Common mode pickup- Double Pulse waveforms set1



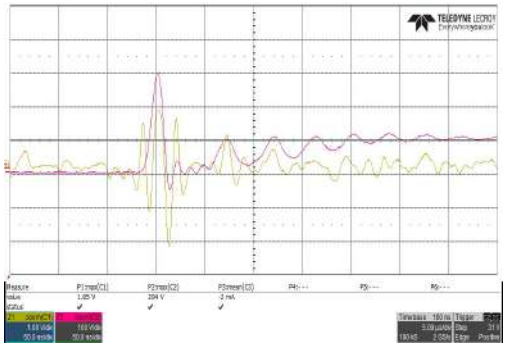
(a) First Turn on Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div



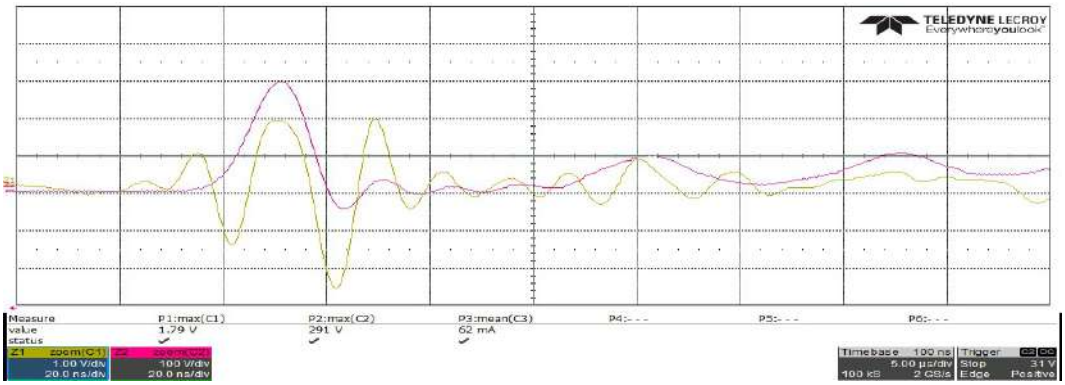
(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div



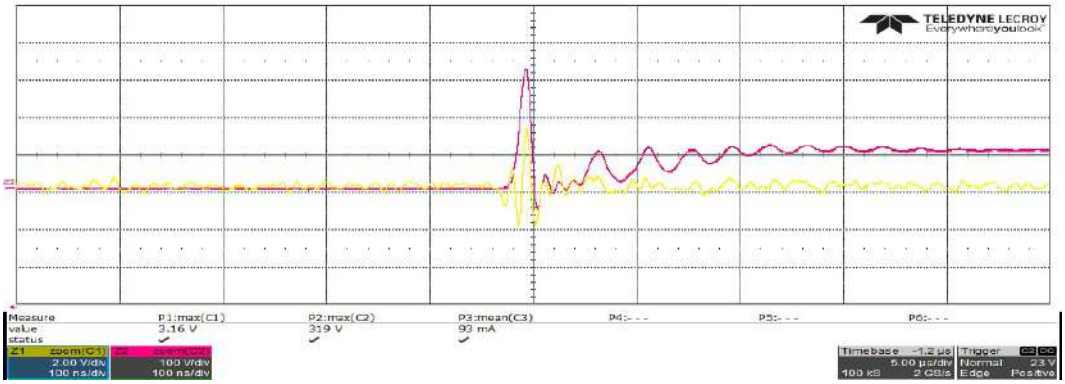
(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, common mode volage: 1V/div

Figure 5.37: Probe Common mode pickup- Double Pulse waveforms set 2

Fig. 5.36. and Fig. 5.37. shows the two different sets of common mode voltage(Yellow waveform) when run at 400V DC Bus, device voltage measured with Teledyne Lecroy's High voltage differential probe is also shown, pink colour plot.
There is a chance for presence of parasitic capacitor build between adapter attached to the metal body as shown in *Fig.5.35*, contributing the common mode injection. So probe position is changed such a way that adapter is far away from metal bodies of test setup. Then again common mode voltage were observed at same voltage level as before. however, this time the common mode voltage is much less than previous case.



(a) Second Turn on Scale; time: 20ns/div, voltage: 100V/div, common mode volage: 1V/div



(b) Second Turn off Scale; time: 100ns/div, voltage: 100V/div, common mode voltage: 1V/div

Figure 5.38: Probe Common mode pickup- Double Pulse waveforms set 3

Fig.5.38 shows new common mode voltages when optical isolated probe tips were connected at ground terminal as before and adapter were placed using plastic mobile holder.

Therefore, the sensed voltage will definitely have this common mode signal. *Fig.5.39* shows waveforms for potential divider output connected to drain terminal of top device.

Case: 1 Voltage sensing at Resistance bridge output.

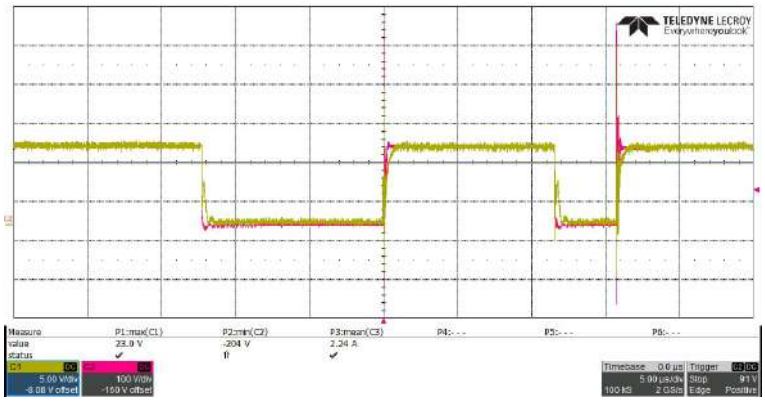
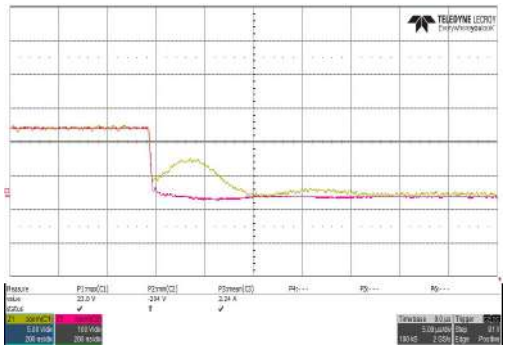
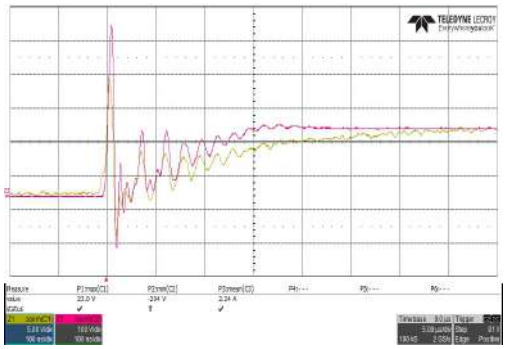


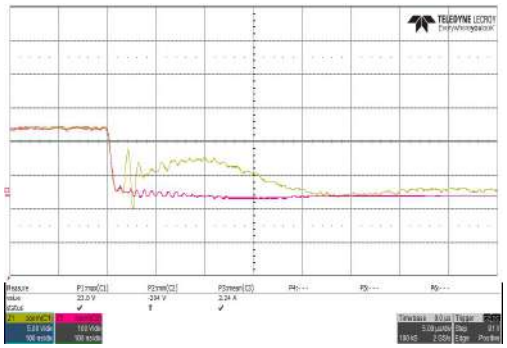
Figure 5.39: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage: 5V/div



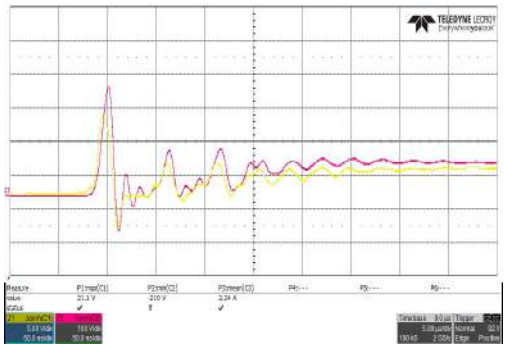
(a) First Turn on Scale; time: 200ns/div, voltage: 100V/div, vsense: 5V/div



(b) First Turn off Scale; time: 100ns/div, voltage: 100V/div, vsense: 5V/div



(c) Second Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense: 5V/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense: 5V/div

Figure 5.40: Double Pulse sensed voltage waveform, V_{DC}=400V

Transient response are not matching because of trace capacitance in board formed between sensed terminal and ground. To mitigate these, a set of capacitance were added in parallel to Resistance in bridge such that ac gain equals dc gain and effect of trace capacitance is negligible.

Case: 2 Voltage sensing with Capacitor bridge alone.

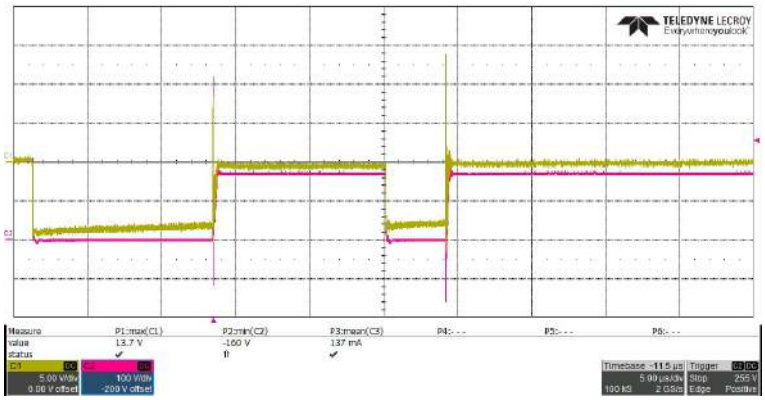
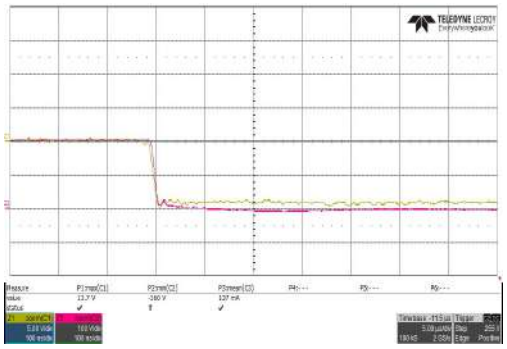
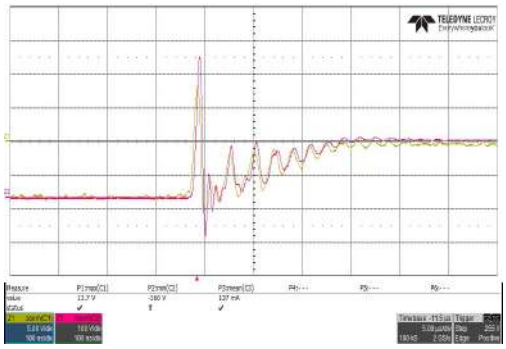


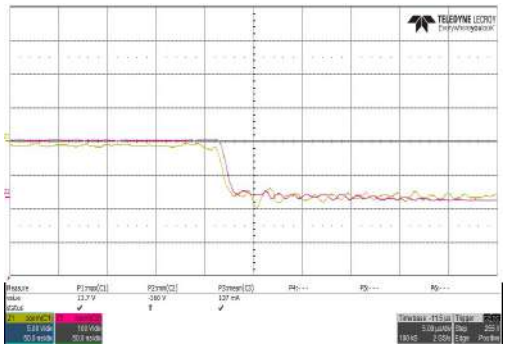
Figure 5.41: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage: 5V/div



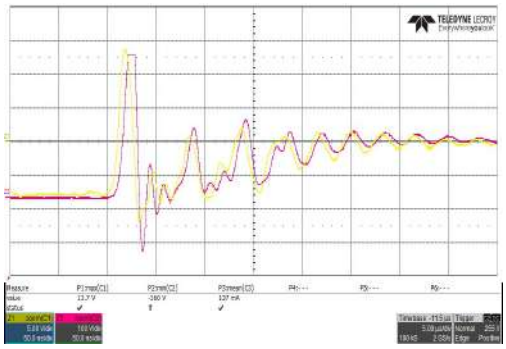
(a) First Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense: 5V/div



(b) First Turn off Scale; time: 100ns/div, voltage: 100V/div, vsense: 5V/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, vsense: 5V/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense: 5V/div

Figure 5.42: Capacitor bridge output voltage waveform, V_{DC}=400V

Capacitor bridge alone were connected just to check the transient response alone. With larger capacitances, most of board trace capacitance effect were neglected. Sensed Voltage(Yellow) and Device voltage(Maroon) transients matches very well with designed gain, but static voltages are not matched due to absence of resistance or in other words dc gain is different. As mentioned before, common mode voltage is present in sensed voltage, To get proper sensed voltages, compensation is required.

Case: 3 Voltage sensing with RC compensation.

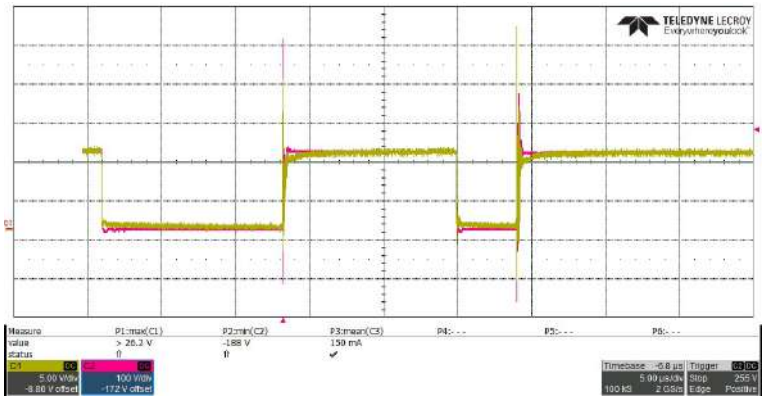
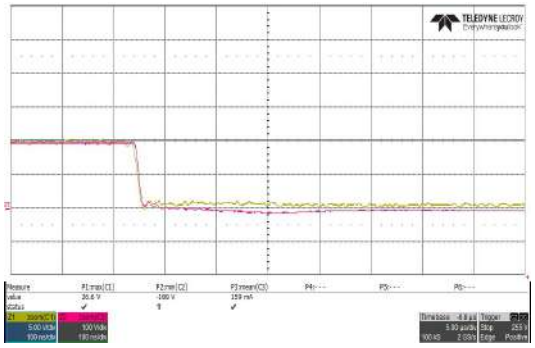
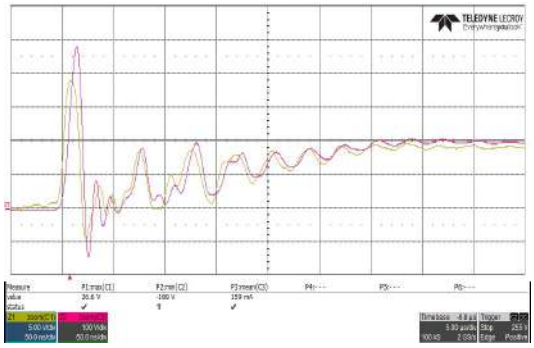


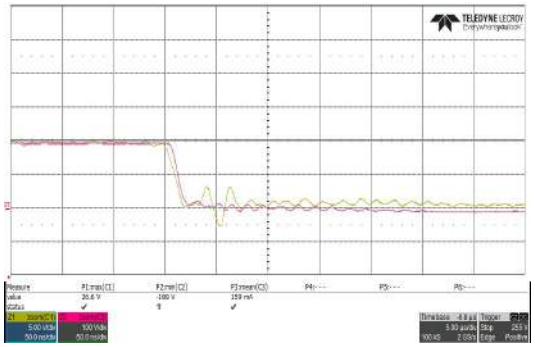
Figure 5.43: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage(yellow): 5V/div



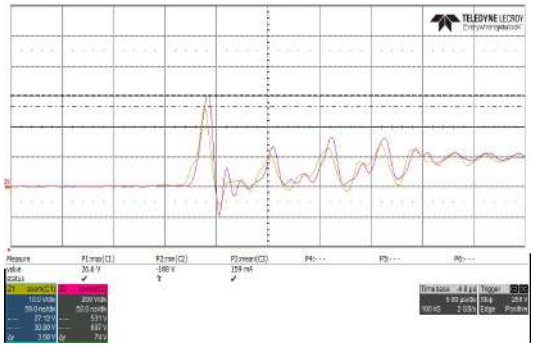
(a) First Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 200V/div, vsense(yellow): 10V/div

Figure 5.44: RC compensated sensed voltage waveform, V_{DC}=400V

With the selected resistances and capacitances, ac gain and dc gain are equal, but the sensed waveform is 95% matching with actual waveform. The presence of common mode in sensing voltage is the reason for mismatch in transient voltage.

To understand till what range of tolerance level, the sensed voltage matches 100% with actual measured voltage. Following cases were studied:

Case: 4 Voltage sensing with 120% RC compensation.

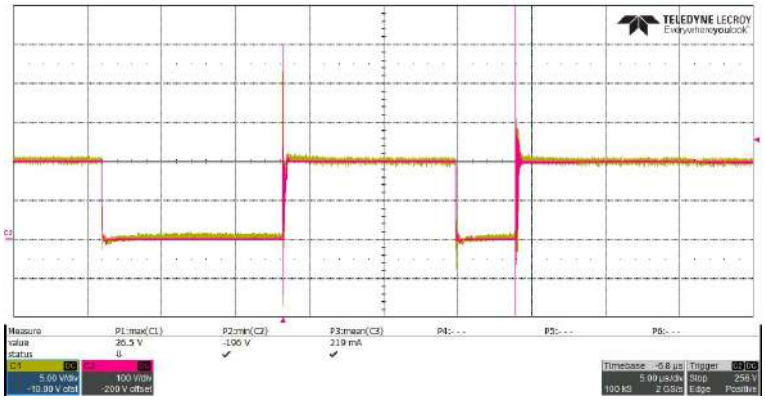
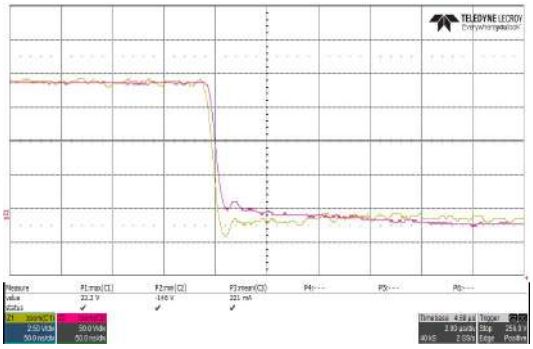
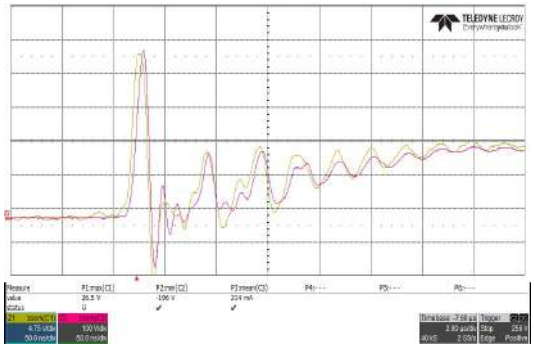


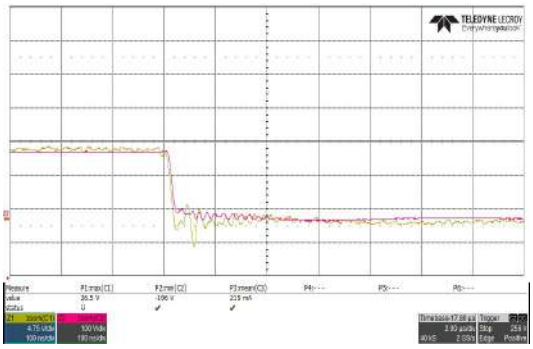
Figure 5.45: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage(yellow): 5V/div



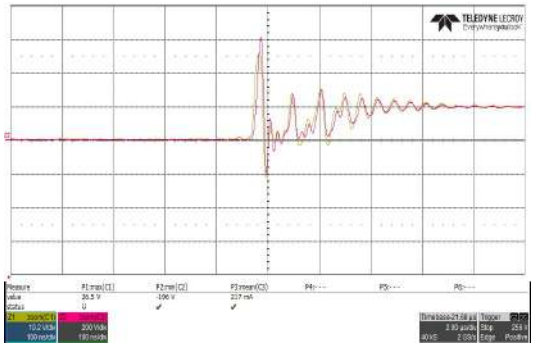
(a) First Turn on, Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 2.5V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 4.75V/div



(c) Second Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense(yellow): 4.75V/div



(d) Second Turn off Scale; time: 100ns/div, voltage: 200V/div, vsense(yellow): 10.2V/div

Figure 5.46: RC 120% compensated sensed voltage waveform, V_{DC}=400V

Sensed voltage(yellow) is somehow matching with actual voltage during turn off instant, but in turn on condition, voltage is found to drop below zero level. So to eliminate this further compensation is added and analysed.

Case: 5 Voltage sensing with 150% RC compensation.

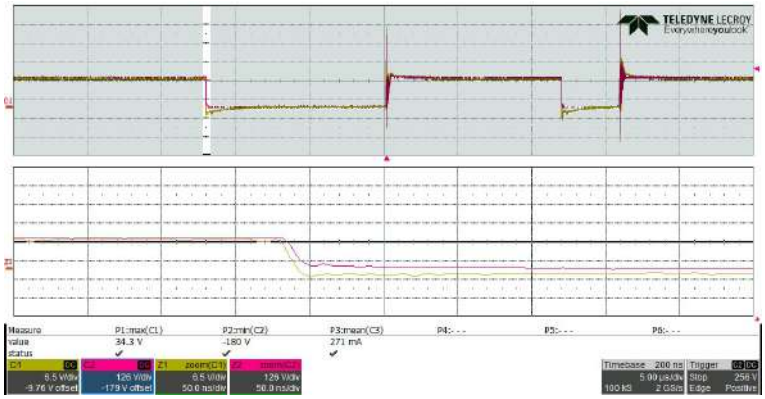
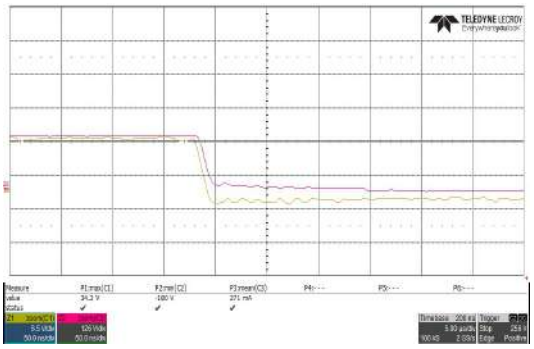
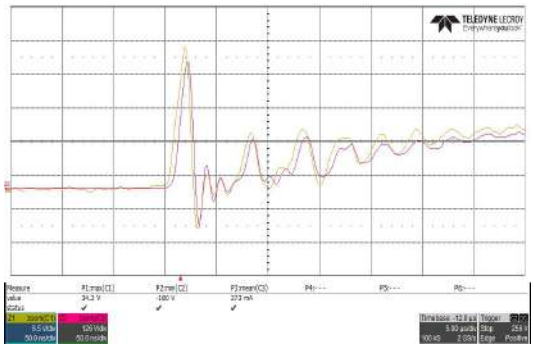


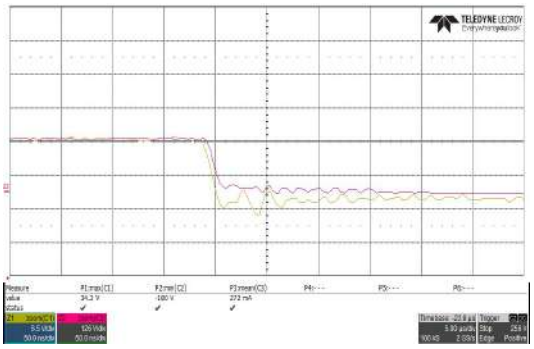
Figure 5.47: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 126V/div, sensed voltage(yellow): 6.5V/div



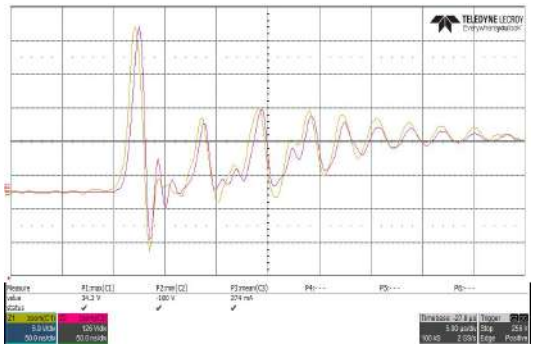
(a) First Turn on, Scale; time: 50ns/div, voltage: 126V/div, vsense(yellow): 6.5V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 126V/div, vsense(yellow): 6.5V/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 126V/div, vsense(yellow): 6.5V/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 126V/div, vsense(yellow): 6.9V/div

Figure 5.48: RC 150% compensated sensed voltage waveform, V_{DC}=400V

At 150% compensation, turn on voltage is not matched properly at some instant. However, with proper tuning between 120% and 150%, the voltage can be matched completely as the device voltage sensing is an important aspect when it comes to series connection of devices.

Case: 6 Voltage sensing with 80% RC compensation.

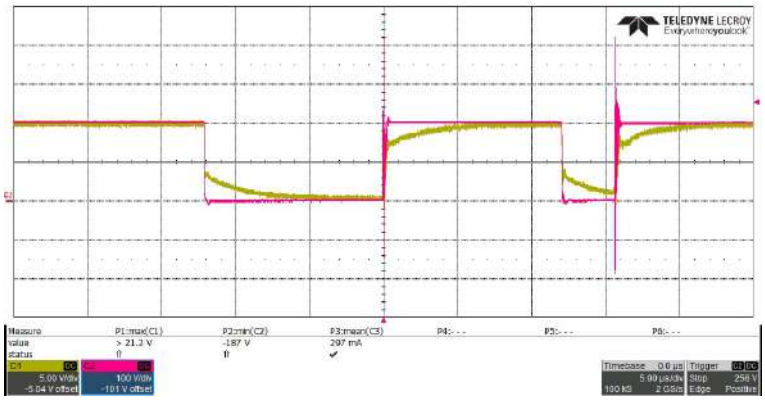
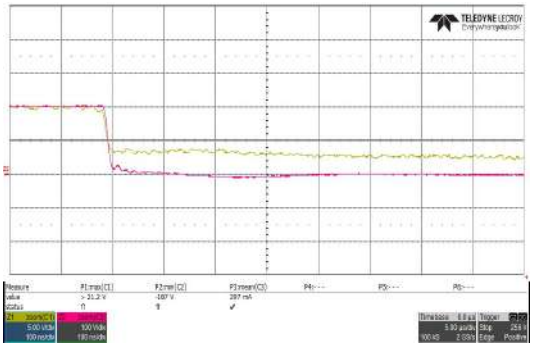
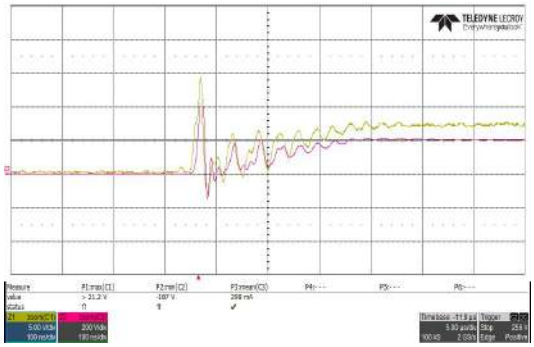


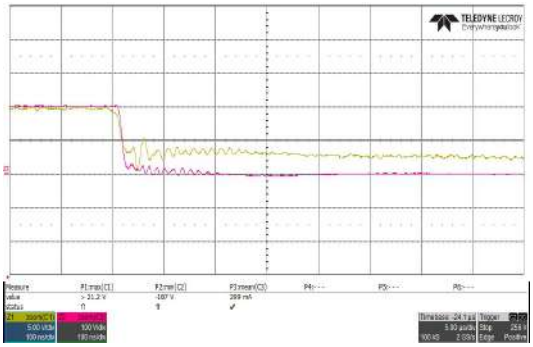
Figure 5.49: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage(yellow): 5V/div



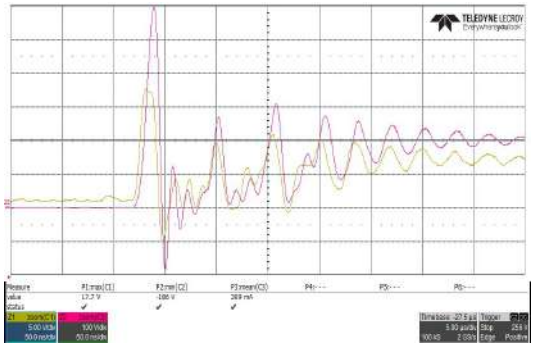
(a) First Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(b) First Turn off Scale; time: 100ns/div, voltage: 200V/div, vsense(yellow): 5V/div



(c) Second Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div

Figure 5.50: RC 80% compensated sensed voltage waveform, V_{DC}=400V

Case: 7 Voltage sensing with 50% RC compensation.

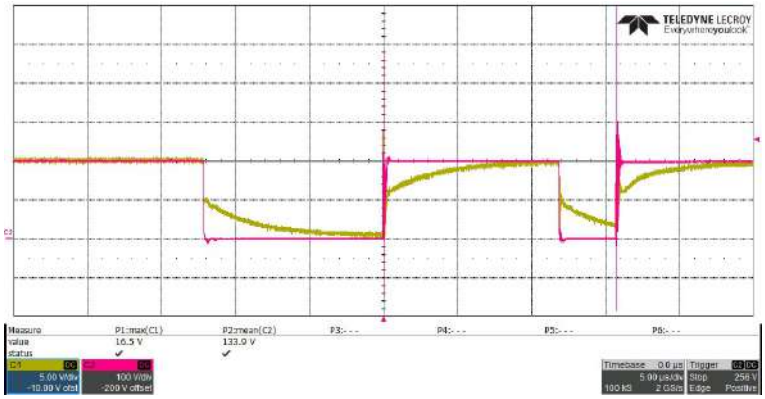
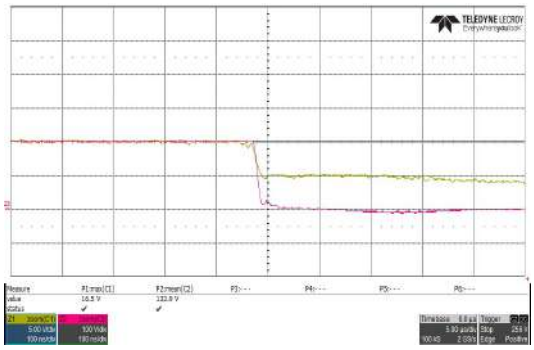
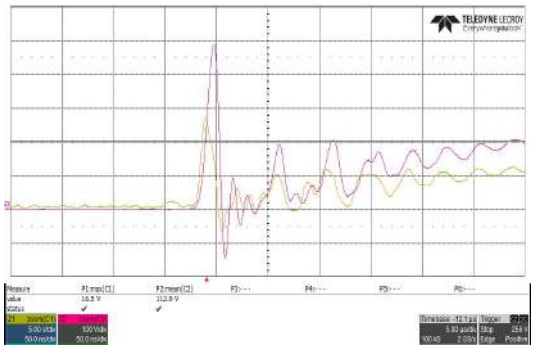


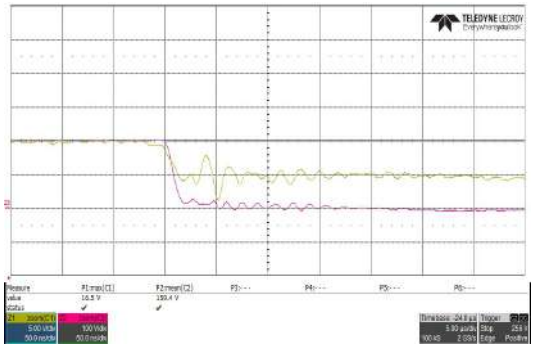
Figure 5.51: Double Pulse waveform, Scale; time: 5μs/div, device voltage: 100V/div, sensed voltage(yellow): 5V/div



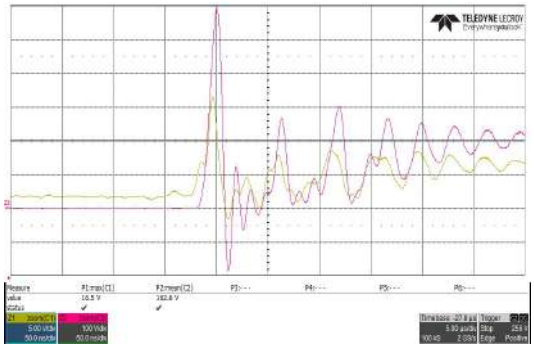
(a) First Turn on Scale; time: 100ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(b) First Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div



(c) Second Turn on Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div

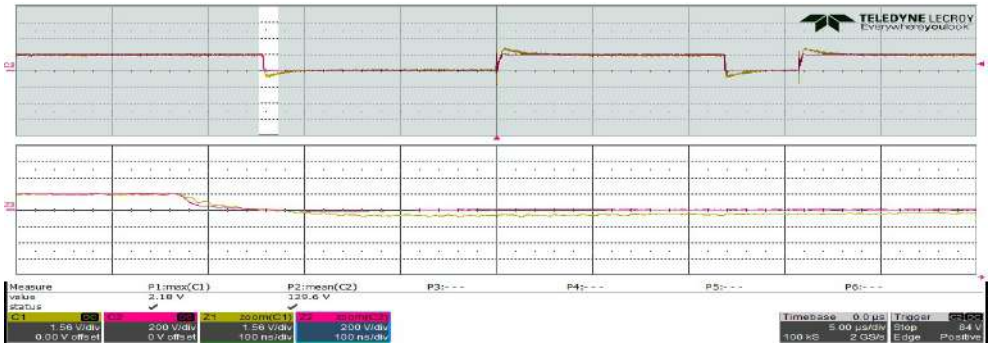


(d) Second Turn off Scale; time: 50ns/div, voltage: 100V/div, vsense(yellow): 5V/div

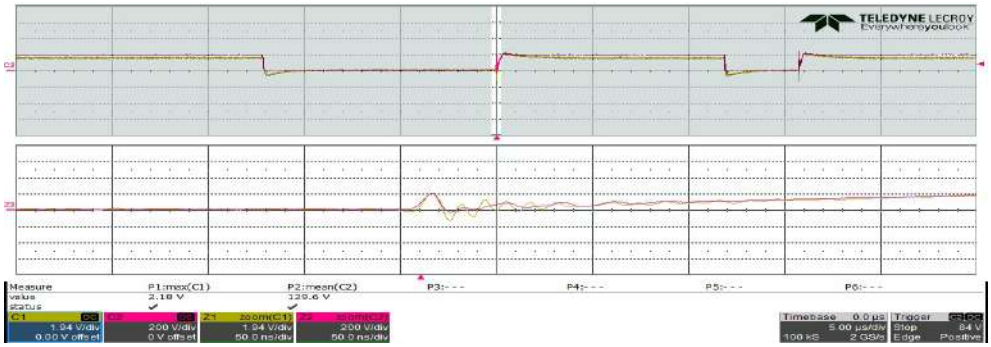
Figure 5.52: RC 50% compensated sensed voltage waveform, V_{DC}=400V

From above studies, the capacitance or ac gain tolerance range is -20% to +50% of theoretical compensation value, i.e., RC compensation with 80% to 150% capacitance tolerance range gives almost matching waveforms. However comparing all the case studies, RC compensation done at 120% has given the best sensing results .

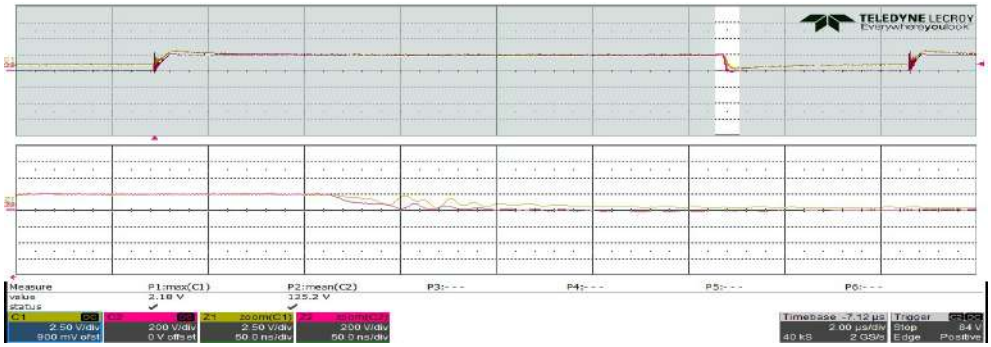
Fig.5.53 represents the output waveform of **AD8045** IC connected to drain terminal via compensated RC bridge.



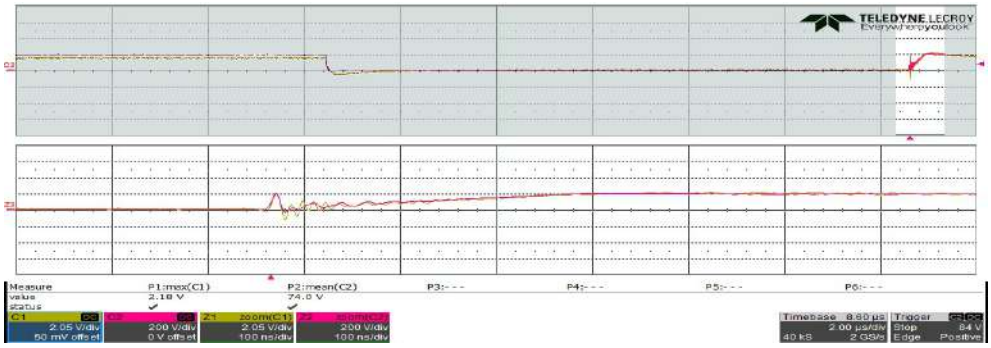
(a) First turn on, Scale; time: 100ns/div, voltage: 200V/div, vsense: 1.56V/div



(b) First turn off, Scale; time: 50ns/div, voltage: 200V/div, vsense: 1.94V/div



(c) Second turn on, Scale; time: 50ns/div, voltage: 200V/div, vsense: 2.5V/div

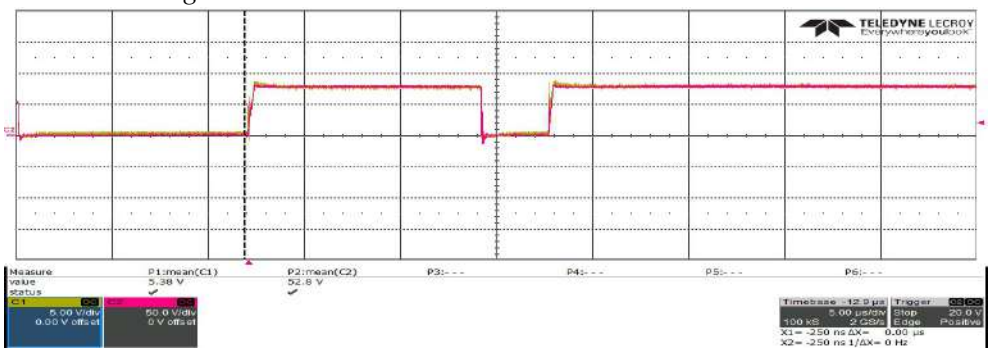


(d) Second turn off, Scale; time: 100ns/div, voltage: 200V/div, vsense: 2.05V/div

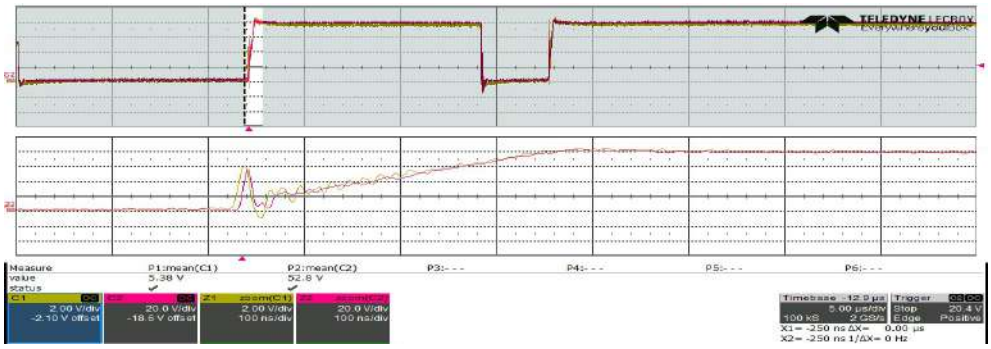
Figure 5.53: AD8045 output-Voltage sensing

Even though the AD8045 has very good CMRR and slew rate, delay might happen due to opamps deadtime. Luckily, due to compensation, waveforms were matched properly.

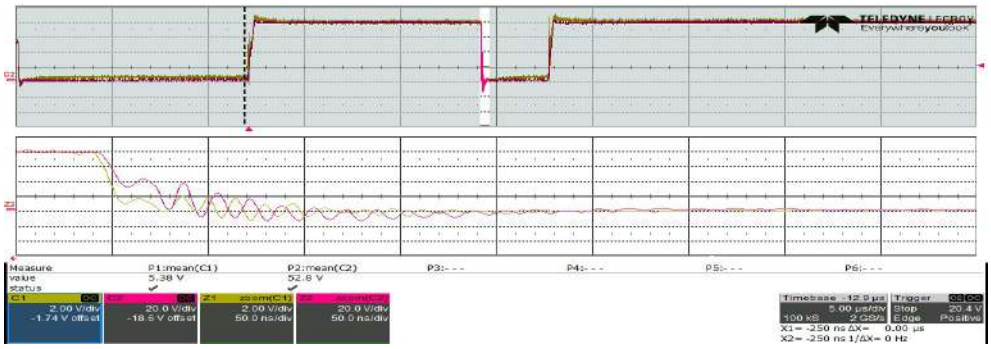
Caddock 1776 C68 is simple resistance bridge divided in the ratios $1/10^4$, $1/10^3$,..,1/10. It can be used fo high voltage sensing applications. Output of AD8045 via caddock IC is shown in *Fig.5.54*.



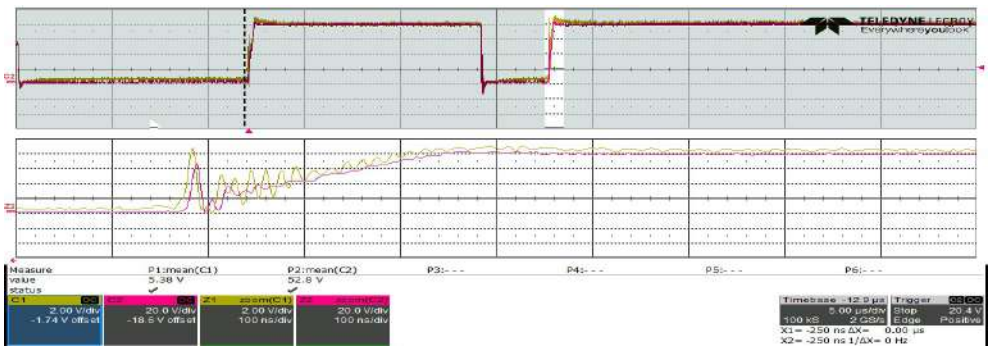
(a) Double pulse, Scale; time: 5μs/div, voltage: 50V/div, vsense: 5V/div



(b) First turn off, Scale; time: 100ns/div, voltage: 20V/div, vsense: 2V/div



(c) Second turn on, Scale; time: 50ns/div, voltage: 20V/div, vsense: 2V/div



(d) Second turn off, Scale; time: 100ns/div, voltage: 20V/div, vsense: 2V/div

Figure 5.54: Voltage sensing: Caddock-AD8045 output, V_{DC}=400V, gain= 1/10

5.5 Pulse Shift Delay Logic

After making certain adjustments like changing the optical reciever, fibre cable etc., new delay is introduced, i.e., 20ns delay in turn on edge and turn off edge. Refer *Fig.5.55*

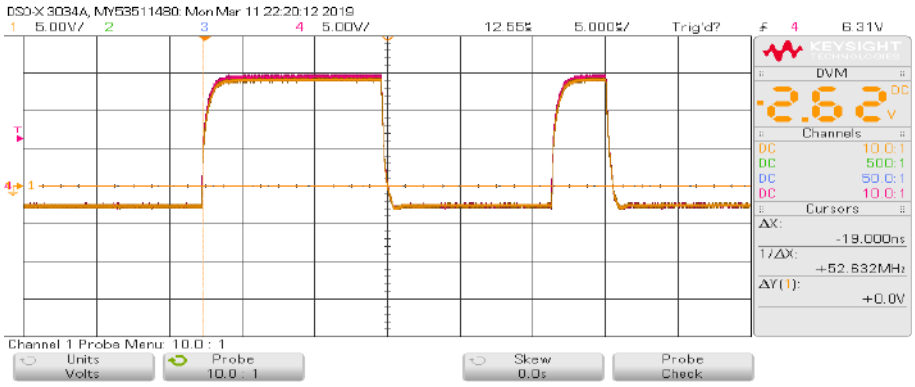
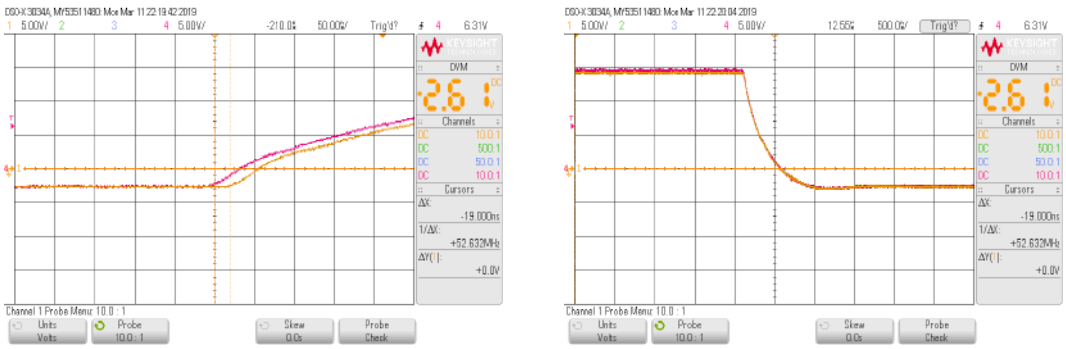


Figure 5.55: Gate voltage Double Pulse waveform. Scale; time: 5μsec/div, voltage: 5V/div



(a) Turn On edge delay, Δt = 20ns, Scale; time: 50ns/div, voltage: 5V/div

(b) Turn Off edge delay, Δt = 20ns, Scale; time: 500ns/div, voltage: 5V/div

Figure 5.56: Rising and falling edge of Gate Voltage Pulse shown in Fig.5.55

Fig.5.56. shows the turn on and turn off edges of gate voltages as shown in *Fig.5.55*. Top device gate voltage is shown by maroon waveform and yellow waveform depicts bottom device gate voltage. Therefore, to mitigate the delay in gate voltage, a 20ns delay is introduced in device 1 gate voltage using pulse logic shift delay circuit. *Fig. 5.57* shows the device parameters after mitigating the delay

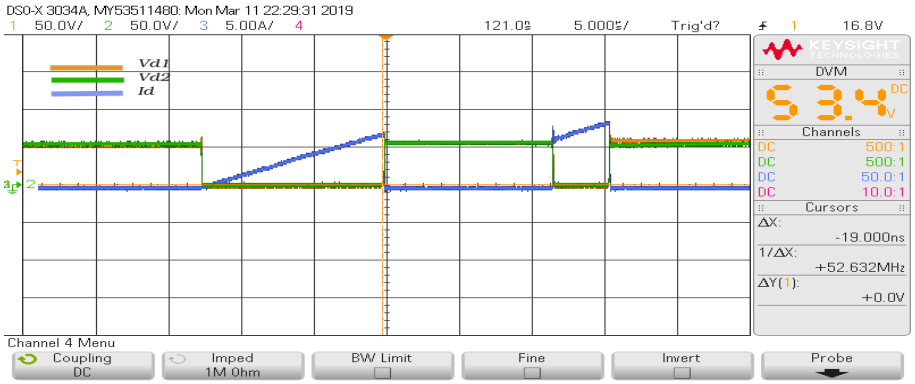
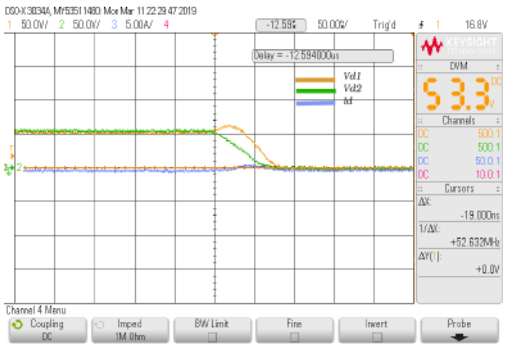
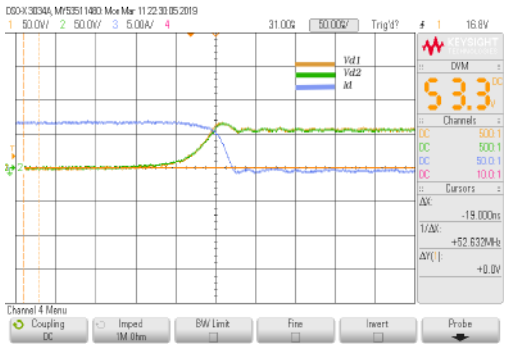


Figure 5.57: Double Pulse waveform. Scale; time: 5μsec/div, device voltage: 50V/div, current: 5A/div

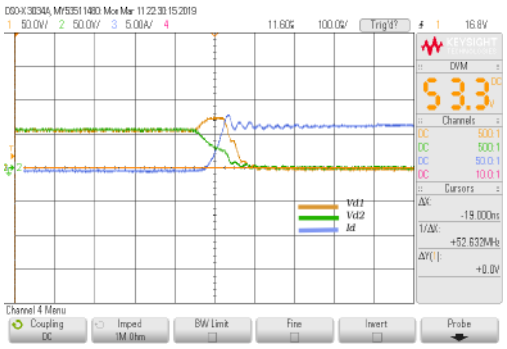
At 100V DC bus voltage, switching characteristics were analysed after introducing delay of 20ns in top device gate driver.



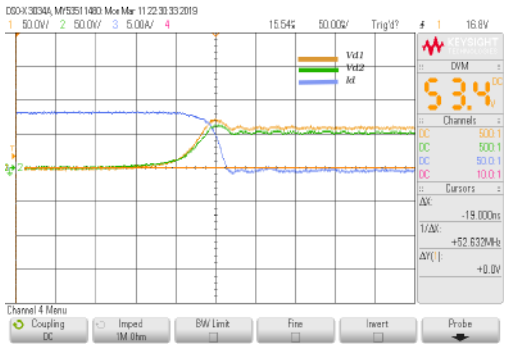
(a) First Turn On, Scale; time: 50ns/div, voltage: 50V/div, current: 5A/div



(b) First Turn Off Scale; time: 50ns/div, voltage: 50V/div, 5A/div



(c) Second Turn On Scale; time: 100ns/div, voltage: 50V/div, current: 5A/div



(d) Second Turn Off Scale; time: 50ns/div, voltage: 50V/div, current: 5A/div

Figure 5.58: Device parameters after the application of PSDL

Fig.5.58. is one example for PSDL application, assuming that internal and external capacitance of devices connected in series are same. However as you can see in *Fig.5.58(b,d)* the dv/dt rates are same, but due to device's internal capacitor variation, the dynamic voltage of both device are not fully matched.
With appropriate tuning of PSDL circuit, we can ensure that there is no problem in gate side to create a problem on voltage balancing in series connection. It will be good if this idealogy is included in design of active gate driver with feedback sensing system.

CHAPTER 6

CONCLUSION

6.1 Summary and Conclusion

The superior properties of SiC MOSFET is well known. The faster switching coupled with lower conduction losses make SiCFET ideal for high power density converters. SiC MOSFET modules can further reduce the size of the converters leading to more dense and compact power converter which can open up a new realm of applications of power electronics and drives. However, the layout parasitic inductance deteriotes the performance by introducing overshoot and oscillations on device parameters, leading to a poor EMI performance. This is verified in both simulation and hardware results. Therefore in the presence of the layout parasitic inductances, utilizing the SiC MOSFET to its full potential without increasing the switching times is a challenge.

In this thesis, challenges in implementing SiC MOSFET in series connection is studied in detail. The effect of parasitic inductances on the switching performance of a SiC MOSFET are analysed in detail The presence of kelvin source in device reduces the gate loop inductances, which reduces the overshoot and oscillations compared to previous version of Silicon carbide MOSFET. In order to study the new SiC MOSFET in series connection, a passive gate driver was designed. The optimum range of gate resistance were identified through simulation and verified by experimental results. Due to difference in optical cable length and other factors like difference in device capacitances, Gate pulse of two device were delayed by 10-20ns. Therefore, assuming that such problem will happen in future, Pulse delay shift logic and other methods were proposed in the thesis. These methods were verified in both simulation and hardware results.

Performance of designed sensing circuits were studied and problems assosciated with measurements were discussed in thesis. Presence of commonmode noise pickup affected measurement of sensed voltage. The use of High voltage optically Isolated Probe

designed by Teledyne Lecroy.Ltd really helped in understanding the amount of common mode pickup and actual sensed voltage.

6.2 Future Scope and Work

There remains a good scope of extending this project by adding additional features to gate driver. To make sure that SiC MOSFET is used at its full potential, noise immune active gate driver should be designed to drive device in series connection. Once device is fully utilised, it can be used in following application as series connection of device will have very good impact:

- Solid state Transformer(SST)
- Solid state Circuit Breaker(SSCB)
- MV Drives
- Light HVDC.
- Distribution and transmission level appartus

APPENDIX A

Key Datasheet parameters

Silicon Carbide MOSFET

Parameters	Value
Part No	C3M0065100K
V_{DSmax}	1000V
$I_{Dcontinuous}$	35A
R_{DSon}	65mΩ
C_{iss}	660pF
C_{oss}	60pF
C_{rss}	4pF
$V_{GS(th)}$	2.1V
R_{Gint}	4.7Ω

Table A.1: Key datasheet parameters of CREE SiC MOSFET(C3M0065100K)

Texas Instruments Gate Driver IC

Parameters	Value
Part No	ISO5852
V_{CC1}	5.5V(max)
V_{CC2}	15V(min), 30V(max)
V_{EE2}	-15V(min)
$I_{(OUTH)}$	2.7A
$I_{(OUTL)}$	5.5A
Withstand isolation voltage	5700V_{RMS}
Propogation Delay	110ns(Max)
CMTI at 1500V	100V/ns

Table A.2: Key datasheet parameters of gate driver IC(ISO5852)

Details of equipments used for hardware experiments

Equipment	Manufacturer	Part Number	Key parameter
Oscilloscope	Agilent Technologies	DSO-X 3034A	350MHz
Oscilloscope	Teledyne Lecroy	wavesurfer 3034Z	350MHz
Differential Probe	Agilent Technologies	N2790A	100MHz
Differential Probe	Tektronix	P5205A	100MHz
High voltage Differential Probe	Teledyne Lecroy	HVD3605A	6000V/100MHz
High Voltage optical isolation Probe	Teledyne Lecroy	HVFO103A	60MHz
Current Probe	Agilent Technologies	N2781B	150A/10MHz

Table A.3: Equipment details

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