DESIGN AND DEVELOPMENT OF AUXILIARY POWER SUPPLY FOR INVERTER APPLICATIONS

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **DESIGN AND DEVELOPMENT OF AUXILIARY POWER SUPPLY FOR INVERTER APPLICATIONS**, submitted by **MANIGILLA PRADEEP KUMAR REDDY (EE17M031)**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS : Auxiliary Power Supply ; Isolated Converter ; Cross Regulation ; Current Mode Control IC UCx84x.

Auxiliary Power Supply is a vital part in an Inverter. It powers the control, signal acquisition and conditioning units of an Inverter. A Digital Signal Processor acts as the brain of an Inverter. It requires 3.3V and 1.8V for its functioning, often these voltages are derived from a 5V d.c supply. The circuits in control and signal conditioning units require Isolated 5V, 15V and -15V d.c power supplies. Available input source for the auxiliary power supply are, dc bus voltage of the inverter and rectified ac voltage of the grid. Isolation is achieved using a transformer. Other advantages of using transformer are,

- Two step voltage reduction,
- Less voltage stress on devices and
- Multiple outputs can be obtained effortlessly by adding additional windings on secondary side.

Three isolated converter topologies, Full bridge, Forward and Flyback topologies are simulated in MATLAB to study working principles, advantages and disadvantages of each converter. Among these Isolated converter topologies the Flyback Converter topology is best suited for low power applications because of its low part count and ease of implementation. In simulation studies it is observed that a Flyback converter operating in Discontinuous conduction Mode **(DCM)** has least losses. A closed loop current mode control of Flyback Converter is achieved using an **IC UC3844.** An additional auxiliary winding is used to power the IC and it also acts as feedback for the control circuit. The duty cycle of the gate signal is controlled to regulate this auxiliary output and the other outputs are cross regulated by the output filter diodes.

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ABBREVIATIONS

CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
GCF	Gain Cross over Frequency
RMS	Root Mean Square

NOTATION

L_m	Magnetizing inductance
$i_m(t)$	Magnetizing current
V_g	Input voltage
V_p	Voltage on primary winding
V_o	Voltage on secondary winding
V_1	Main output voltage
V_2	First auxiliary output voltage
V_3	Second auxiliary output voltage
I_g	Net primary current
I_1	Main output load current
I_2	First auxiliary output load current
I_2	Second auxiliary output load current
$n_1 : n_n$	Primary to n^{th} winding turns ratio

CHAPTER 1

INTRODUCTION

1.1 Objective

The aim of the project is to design an auxiliary Power Supply which has half the dc bus voltages of an Inverter and rectified single phase ac voltage of grid as inputs and isolated 15V, -15V and 5V d.c as outputs. These voltages can be used to power Digital Signal Processor and its peripheral circuits as shown in the Fig.1.1.

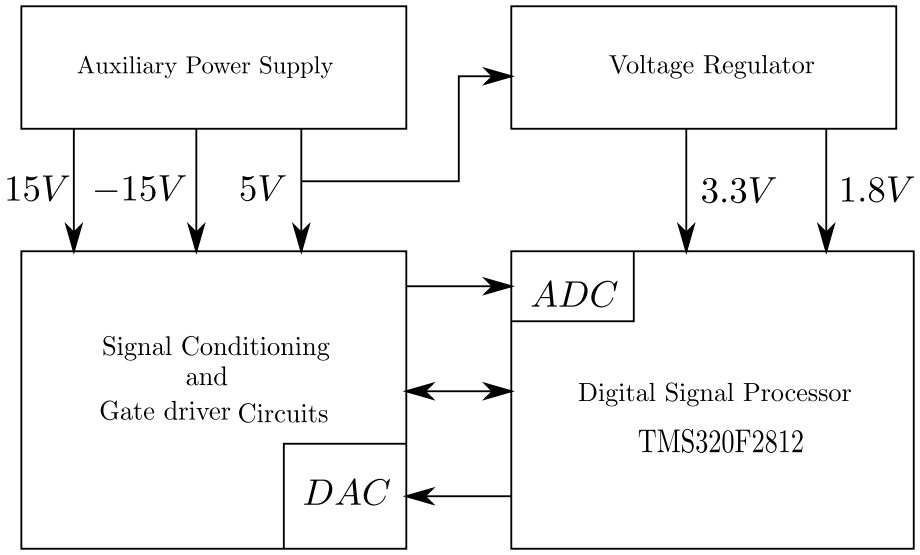


Figure 1.1: Auxiliary Power Supply Block Diagram

Many circuits require isolated supply, isolation can achieved by using a transformer. Transformer provides galvanic isolation between input and the output. In case of multi output converter an added advantage of incorporating transformer is that multiple outputs can be obtained effortlessly by adding additional windings on the secondary side of the same transformer core.

The rectified A.C. will have approximately $325V$ on the d.c side and half the d.c bus voltage can be as high as $400V$. When loaded the input voltage will have a range of $(300, 400)V$. This input voltage should be stepped down and isolated using an isolated dc to dc converter.

1.2 Transformer Isolation

In many applications it is desired to have isolation between input and output. Isolation can be obtained by connecting a 50 or 60 Hz transformer at the input ac source. However, since the size and weight of a transformer vary inversely with the frequency, significant reduction in size can be achieved by incorporating transformer into the converter circuit such that the transformer operates at the converter switching frequency i.e. tens or hundreds of kilohertz. When a transformer is in a circuit few things should be taken care such as effect of magnetizing inductance.

1.2.1 Effect of Magnetizing Inductance

Physical transformers contain a magnetizing inductance L_m as illustrated in Fig.1.2.

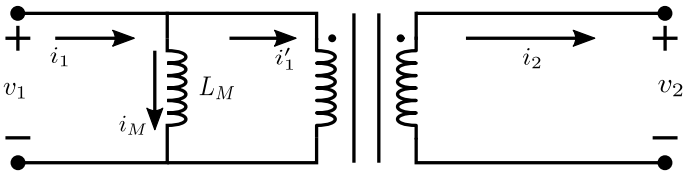


Figure 1.2: Equivalent circuit of a transformer

The magnetizing current $i_M(t)$ is proportional to the magnetic field $H(t)$ inside the core. The B-H characteristics of the transformer core are illustrated in the Fig.1.3

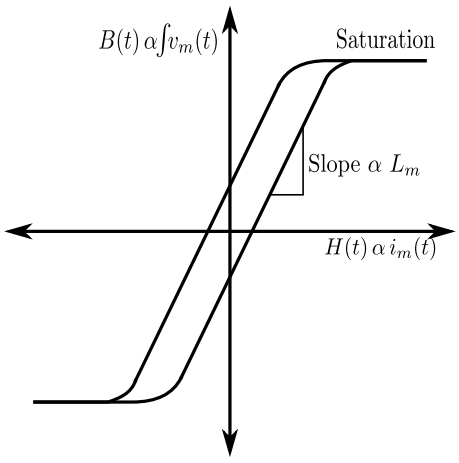


Figure 1.3: B-H characteristics of magnetic core

If the magnetizing current becomes too large, then the magnetic field increases and causes the core to saturate. The magnetizing inductance then becomes very small in

magnitude, effectively shorting the transformer. In a well designed transformer, the magnetizing inductance will be large in magnitude over the intended range of frequencies, such that the magnetizing current $i_m(t)$ is much smaller in magnitude than $i_1(t)$. Then $i_1^{'}(t) = i_1(t)$ and the transformer behaves nearly as ideal transformer. It should be noted that magnetizing current $i_m(t)$ and $i_1^{'}(t)$ are independent quantities.

1.2.2 Volt-Sec Balance of Magnetizing Inductance

Magnetizing inductance should obey all the usual laws of inductance. In the Fig.1.2 primary voltage $V_1(t)$ is applied across L_m, hence

$$v_1(t) = L_m \frac{di_m(t)}{dt} \tag{1.1}$$

Integration leads to,

$$i_M(t) - i_M(0) = \frac{1}{L_m} \int V_1(t) dt \tag{1.2}$$

since the magnetizing current is proportional to the integral of applied voltage, it is important that the dc component of this voltage is zero. Otherwise, during each switching period there will be net increase in magnetizing current, eventually leading to excessive $i_M(t)$ and transformer saturation.

1.3 Power Rating

Rating of Power Supply = 15V*3A + -15V*-1A + 5V*5A = 85W.

High efficiency is essential in any power processing application. If the power loss is substantial then large heat sinks and expensive cooling systems are required. In an efficient converter since little power is lost, the converter elements can be packed with high density, leading to a converter of small size and weight. Losses in the converter is the deciding factor to select an appropriate converter topology for an application.

1.4 Organisation of the Thesis

The thesis is organised into seven chapters.

Chapter 2 gives an insight into working principle of a full bridge, forward and flyback isolated converters and briefly discusses about advantages and disadvantages of each topology.

Chapter 3 presents the simulation results depicting the differences between a single output and a multi-output forward and flyback converters. It also discusses about feasibility of operating multi-output forward and flyback converters in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

Chapter 4 gives various loss formulae and loss calculations in a multi-output forward converter operating in CCM and a multi-output flyback converter operating in CCM and DCM.

Chapter 5 discusses about the hardware implementation aspects of designing a closed loop current mode control for a flyback converter operating in DCM.

Chapter 6 analyses the results obtained while testing the hardware set up.

Chapter 7 concludes the thesis.

CHAPTER 2

ISOLATED CONVERTER TOPOLOGIES

2.1 Full Bridge Isolated Converter

The full-bridge isolated buck converter is illustrated in Fig.2.1. A version containing center-tapped secondary winding is shown. The two halves of the center-tapped secondary winding may be viewed as separate windings and hence can consider as a three winding transformer having turns ratio $1 : n : n$. The conducting devices for various time intervals are listed in Table.2.1 and the waveforms are shown in Fig.2.2.

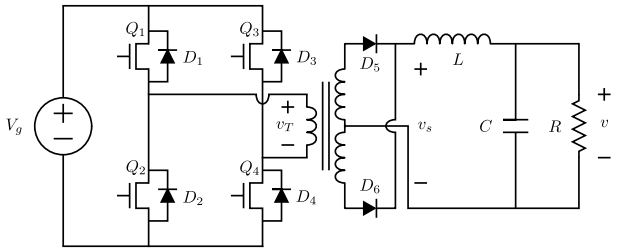


Figure 2.1: Full bridge isolated DC-DC converter

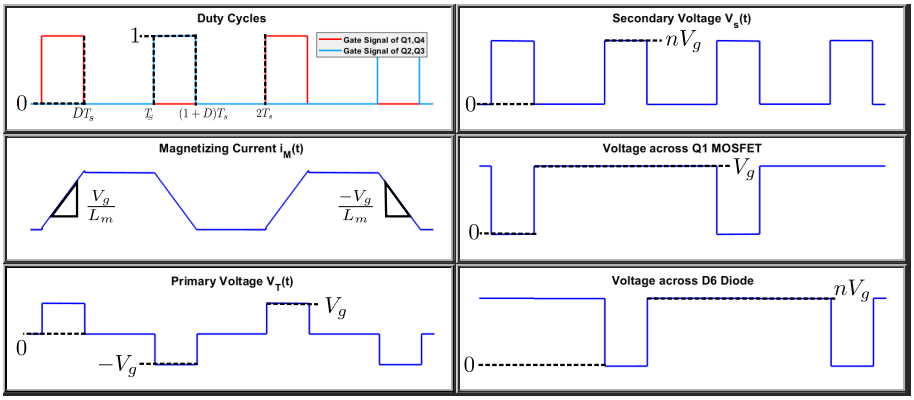


Figure 2.2: Full bridge converter waveforms

Table 2.1: Time vs conducting devices in Full bridge converter

Time interval	$0\,to\,DT_s$	$DT_s\,to\,T_S$	$T_s\,to\,(1+D)T_S$	$(1+D)T_s\,to\,2T_S$
Devices Conducting	Q_1 , Q_4 , D_5	Q_1 , Q_3 , D_5 , D_6	Q_2 , Q_3 , D_6	Q_1 , Q_3 , D_5 , D_6

The working principle of the converter as explained in [1] is during the first subinterval $0 < t < DT_s$ (when red pulse in high in Fig.2.2), transistors Q_1 and Q_4 conduct and the voltage V_g is applied across primary winding. This positive voltage causes the magnetizing current $i_M(t)$ to increase with a slope $\frac{V_g}{L_M}$ as shown in Fig.2.2. A voltage of nV_g appears at each half of secondary winding causing the diode D_5 to forward bias and D_6 is reverse biased. The voltage $V_s(t)$ is equal to $nV_g(t)$.

During the second subinterval $DT_s < t < T_s$, transistors Q_1 and Q_3 conduct and hence $v_T = 0$. The magnetizing current will remain constant as illustrated in Fig.2.2. Diodes D_5 and D_6 are forward biased. The voltage $V_s(t)$ is equal to zero.

During the third subinterval $T_s < t < (1 + D)T_s$ (when blue pulse is on as shown in Fig.2.2), transistors Q_2 and Q_3 conduct. The applied transformer primary voltage is $v_T = -V_g$ which causes the magnetizing current $i_M(t)$ to decrease with a slope $\frac{-V_g}{L_M}$ as shown in Fig.2.2. The voltage $-nV_g$ appears at each half of secondary winding. Diode D_5 is reverse biased and D_6 is forward biased. The voltage $V_s(t)$ is equal to $nV_g(t)$.

During the last subinterval $(1 + D)T_s < t < 2T_s$, transistors Q_1 and Q_3 conduct same as in second interval. The magnetizing current will remain constant as $v_T = 0$. Diodes D_5 and D_6 both are forward biased. The voltage $V_s(t)$ is equal to zero.

2.1.1 Advantages

1. Transformer is utilized efficiently. The magnetic flux swings in both positive and negative sides of B-H curve as a result required core area is smaller.
2. Voltage stress and power rating of the transistors is minimum thus this converter is suitable for high power applications.

2.1.2 Disadvantages

1. Too many switches and each switch requires its corresponding driving circuit. Isolated voltages are required to power gate drivers.
2. Each output requires a pair of secondary windings, thus making the total number of secondary windings twice that of the other converters.
3. Space required is high because of too many magnetic components and a bulky transformer.
4. Cross regulation is poor in Discontinuous Conduction Mode.

2.2 Forward Converter

The forward converter is illustrated in Fig.2.3. This isolated converter is based on the buck converter. It has a single transistor and hence finds application at power levels lower than those of full bridge converters. The duty cycle in a forward converter has a limitation, for the transformer ratio $n_1 : n_2$ the duty cycle is limited to the range,

$$0 < D < \frac{1}{1 + \frac{n_2}{n_1}} \tag{2.1}$$

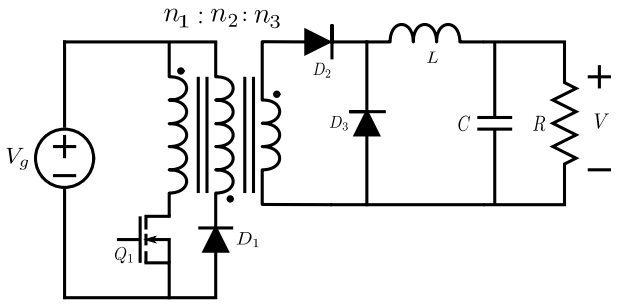


Figure 2.3: Forward converter

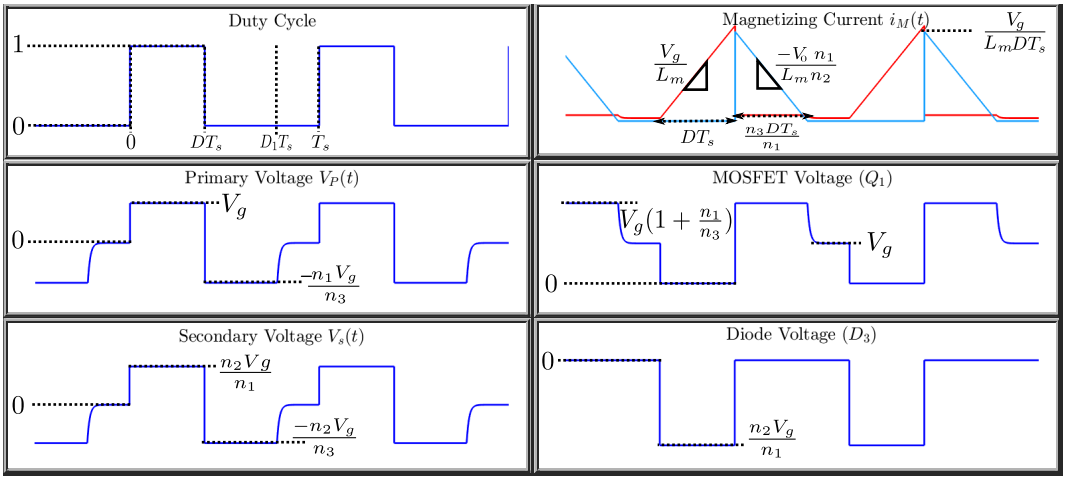


Figure 2.4: Forward converter waveforms

Table 2.2: Time vs conducting devices in a Forward converter

Time interval	$0\,to\,DT_s$	$DT_s\,to\,D_1T_S$	$D_1T_s\,to\,T_S$
Devices Conducting	Q_1 , D_2	D_1 , D_3	D_3

The working principle of the converter as explained in [1] is during the first subinterval $0 < t < DT_s$, transistor Q_1 conducts and diode D_2 becomes forward biased. The diodes D_1 and D_3 are reverse biased. Voltage V_g is applied to the transformer primary winding and hence the transformer magnetizing current $i_M(t)$ increases with a slope of $\frac{V_g}{L_M}$ as shown in Fig.2.4.

During the second subinterval $DT_s < t < T_s$, the transistor Q_1 is switched off. The transformer magnetizing current $i_M(t)$ should continue to flow. Since transistor Q_1 is off, it should flow through primary winding (coming out of the polarity mark). Diode D_1 becomes forward biased and the current $i_M(t)\frac{n_1}{n_2}$ flows into the polarity mark of second winding.

Voltage V_g is applied across second winding and hence the voltage across magnetizing inductance is $-V_g\frac{n_1}{n_2}$. This negative voltage causes the magnetizing current to decrease with a slope of $-V_g\frac{n_1}{(n_2 * L_M)}$ as shown in Fig.2.4. The time taken for the magnetizing current to become zero is equal to $\frac{n_2}{n_1}DT_s$, it depends on the turns ratio $\frac{n_1}{n_2}$. Magnetizing current reset time should be less than $(1-D)T_s$.

$$\frac{n_2}{n_1}DT_s \; < \; (1-D)T_s \; => \; D \; < \; \frac{1}{1+\frac{n_2}{n_1}}.$$

2.2.1 Advantages

- Good for medium power multi output converters.
- Less stress on reactive elements.
- Requires less space when compared to a Full Bridge Converter.

2.2.2 Disadvantages

- High stress on MOSFET and Secondary diode.
- Higher switching losses.
- Poor cross regulation especially in discontinuous conduction mode
- Too many magnetic components.

2.3 Flyback converter

The flyback converter is based on a buck-boost converter. The configuration of a flyback converter is illustrated in Fig.2.5. The transformer in a flyback converter is called flyback transformer (a coupled inductor). Unlike the ideal transformer, current does not flow simultaneously in both windings of the flyback transformer. The magnetizing inductance L_M functions in the same manner as inductor L of the original buck boost converter.

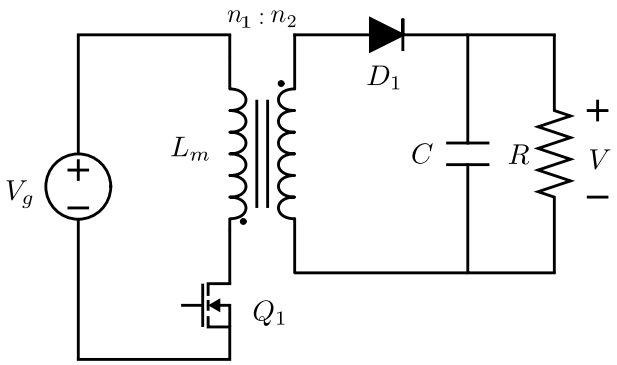


Figure 2.5: Flyback converter

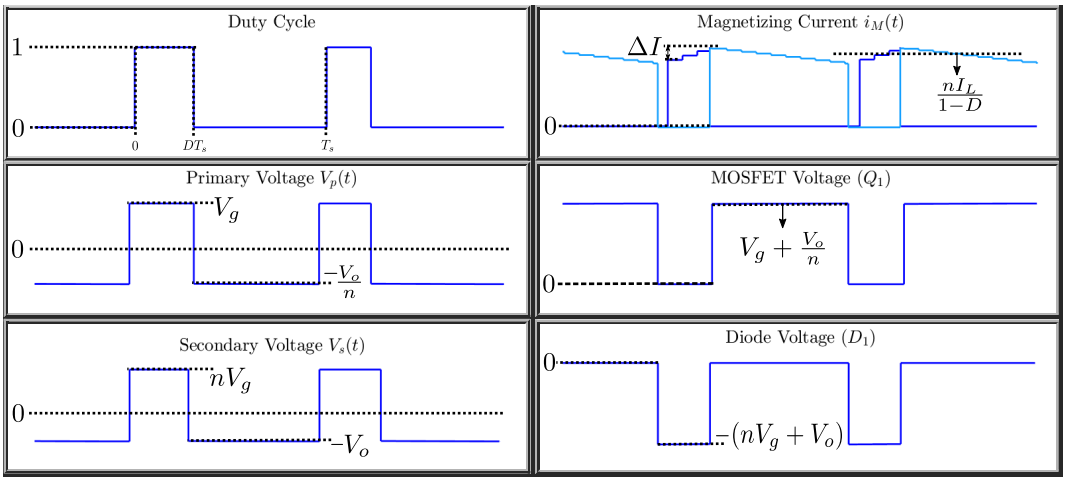


Figure 2.6: Flyback converter waveforms

Table 2.3: Time vs conducting devices in a Flyback converter

Time interval	$0\,to\,DT_s$	$DT_s\,to\,T_S$
Devices Conducting	Q_1	D_1

The working principle of the converter as explained in [1] is during the first subinterval $0 < t < DT_s$, transistor Q_1 conducts and voltage V_g is applied across the magnetizing inductor L_m. AS a result the magnetizing current i_M increases with a slope of $\frac{V_g}{L_m}$ as shown in the Fig.2.6. The diode D_1 is reverse biased and the capacitor current $i_c(t) = \frac{V}{R}$.

During the second subinterval, the transistor Q_1 is off and the diode D_1 conducts. The voltage across magnetizing inductance L_m during this subinterval is $-V\frac{n_1}{n_2}$. The magnetizing current will decrease with a slope of $-V\frac{n_1}{n_2 L_m}$ as shown in Fig.2.6. The capacitor current during this subinterval $i(t)_c = i_L\frac{n_1}{n_2} - \frac{V}{R}$.

2.3.1 Advantages

- Least part count, only one magnetic component and only one switch.
- Simple and Economical.
- Can be operated in Discontinuous Conduction Mode.

2.3.2 Disadvantages

- High stress on energy storage capacitors.
- High current stress on switch.

2.4 Comparison of Voltage and Current Stress on Diodes and MOSFET

Specifications

Table 2.4: Converter Specifications

Input Voltage	V_g	400V
Output Voltages	V_1, V_2, V_3	$15V$, $-15V$, $5V$.
Load Current (secondary)	I_1, I_2, I_3	$3A$, $1A$, $5A$.
Load Current (referred to primary)	$I_o = \frac{n_2 I_1 + n_3 I_2 + n_4 I_3}{n_1}$	$1.7A$
Transformer turns ratio	$n_1 : n_2$	
Full Bridge Converter	$n_1 : n_2 : n_3 : n_4 : n_5 : n_6 : n_7$	$1 : 0.3 : 0.3 : 0.3 : 0.3 : 0.1 : 0.1$
Forward Converter	$n_1 : n_2 : n_3 : n_4 : n_5$	$1 : 1 : 0.3 : 0.3 : 0.1$
Flyback Converter	$n_1 : n_2 : n_3 : n_4$	$1 : 0.3 : 0.3 : 0.1$
Magnetizing Inductance		
Flyback converter	L_m	$40\mu H$
Other converters	L_m	$344\mu H$

Table 2.5: Voltage and Current Stress on Diodes

Converter	Peak Voltage		Peak Current	
	Expression	Value	Expression	Value
Full Bridge Converter (Secondary Diodes)				
D_5	$\frac{2V_g n_2}{n_1}$	$240V$	$(I_o + \frac{\Delta I}{2})$	$1.7425A$
D_6	$\frac{2V_g n_2}{n_1}$	$240V$	$(I_o + \frac{\Delta I}{2})$	$1.7425A$
Forward converter (Output Tertiary Diodes)				
D_2	$\frac{V_g n_2}{n_1}$	$120V$	$(I_o + \frac{\Delta I}{2})$	$1.7425A$
D_3	$\frac{V_g n_2}{n_1} + V$	$135V$	$(I_o + \frac{\Delta I}{2})$	$1.7425A$
Forward converter (Reset Secondary Diode)				
D_1	$V_g \frac{n_3}{n_1}$	$400V$	$\frac{V_g * D * T_s}{L_m}$	$1.07527mA$
Flyback converter (Secondary Diode)				
D_1	$V_g(\frac{n2}{n1} + \frac{D}{1-D})$	$135V$	$\frac{V_g D T_s n_1}{2 L_m n_2} + \frac{I_o}{(1-D)}$	$6.376593A$

Table 2.6: Voltage and Current Stress on MOSFET

Converter	Peak Voltage		Peak Current	
	Expression	Value	Expression	value
Full bridge converter	V_g	$400V$	$\frac{V_g DT_s}{L_m} + \frac{n_2}{n_1}(I_o + \frac{\Delta I}{2})$	$1.7436A$
Forward converter	$V_g(1 + \frac{n_1}{n_2})$	$800V$	$\frac{V_g DT_s}{L_m} + \frac{n_3}{n_1}(I_o + \frac{\Delta I}{2})$	$1.7436A$
Flyback converter (in CCM)	$V_g + \frac{n_1 V_1}{n_2}$	$450V$	$\frac{V_g DT_s}{2*L_m} + \frac{n_2 I_o}{n_1(1-D)}$	$1.913A$
Flyback converter (in DCM)	$V_g + \frac{n_1 V_1}{n_2}$	$450V$	$\frac{V_g DT_s}{L_m}$	$4.254A$

Full bridge Isolated converters are typically used at power levels greater than **1kW**. It may not be suitable for lower power applications because of its high part count. Forward and Flyback converters are more suited and for this application as the power rating is less. The Multi-output topologies of these two converters are analysed in detail in the next chapter. The feasibility of operating these two converters in Continuous Conduction Mode **(CCM)** and Discontinuous Conduction Mode **DCM** is also discussed.

CHAPTER 3

MODE OF OPERATION

This chapter discusses about differences in a single output and multi output Forward and Flyback converters and also feasibility of operating these converters in CCM and DCM. In Multi output converters all the secondary outputs are to be regulated. In most of the cases while designing a closed loop control feed back is taken from a single output and all other outputs are cross regulated. Cross regulation in Forward and Flyback Converters operating in CCM and DCM modes is also discussed in this chapter.

3.1 Forward Converter

Single Output Forward Converter

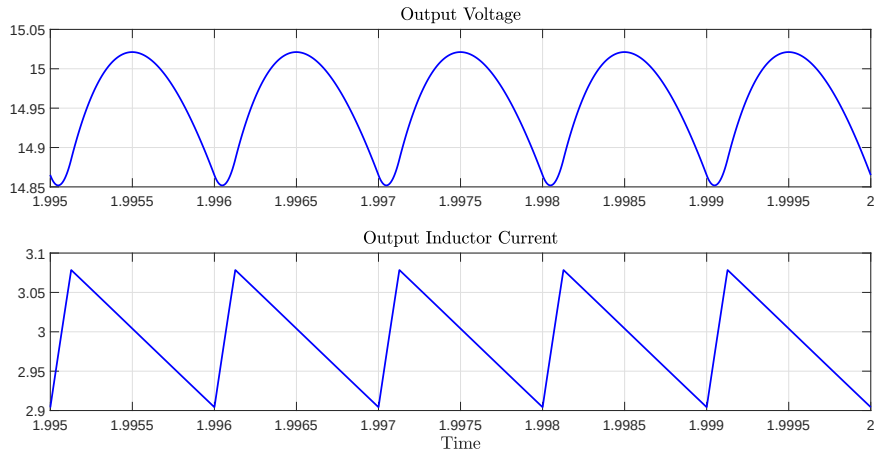


Figure 3.1: Output voltage and current in a single output Forward converter

In Fig.3.2 both the main and auxiliary output currents are continuous and the main output current and voltage are same as in Fig.3.1. The only difference between a single output and a dual output converter is in input current as shown in Fig.3.3. The problem arises when one of the output is lightly loaded as shown in Fig.3.4. Auxiliary output voltage is unregulated because the auxiliary output inductor current is discontinuous.

Dual Output Forward Converter

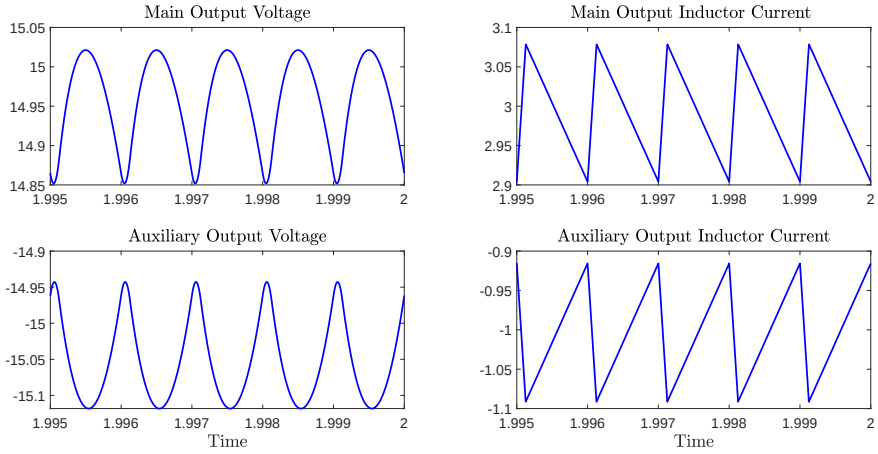


Figure 3.2: Output voltages and currents in a dual output Forward converter

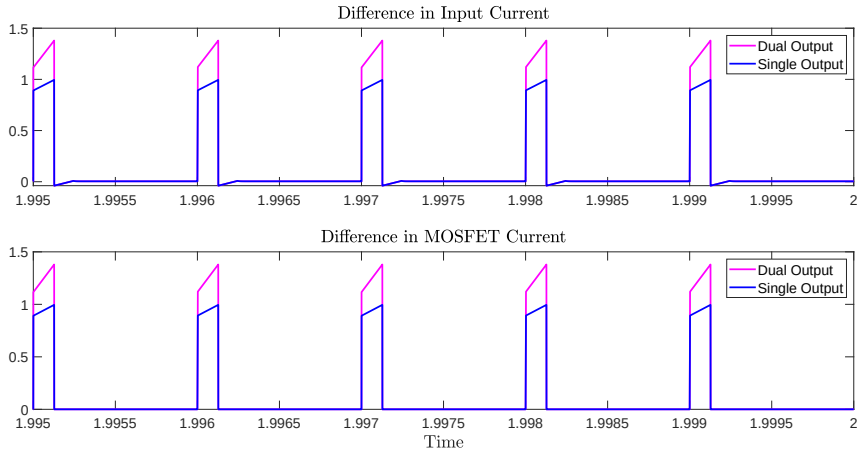


Figure 3.3: Input current in dual output and a single output converter

Lightly loaded Forward Converter

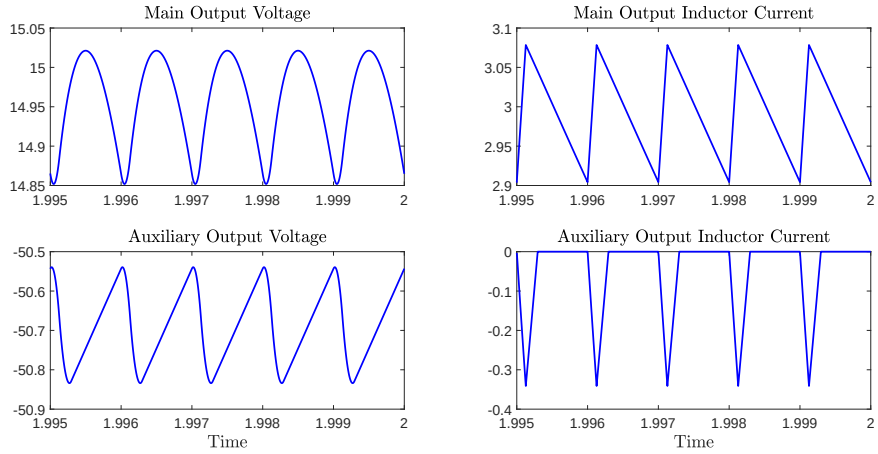
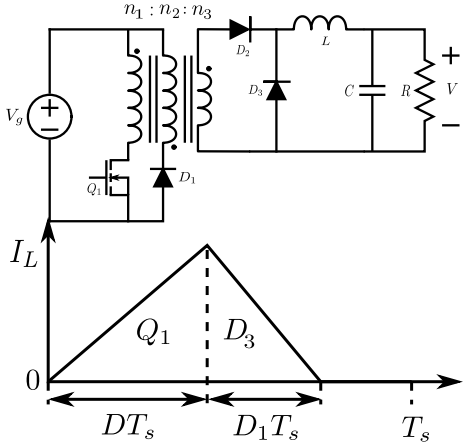


Figure 3.4: Lightly loaded dual output Forward converter

In Fig.3.2 both the main and Auxiliary outputs are regulated because the output inductor currents are continuous at both the outputs. In that scenario the output voltages depend only on the input voltage and duty cycle but when output inductor current is discontinuous as in Fig.3.4 output voltage not only depend on input voltage and duty cycle but also on load. A detailed derivation is given in the next section.

3.1.1 Forward Converter in DCM



We know that in a forward converter average inductor current is equal to load current.

$$\frac{1}{2} * I_{peak} * (D + D_1) = I_{load} = \frac{V}{R} \tag{3.1}$$

from inductor volt second balance equation,

$$(n_2 V_g - V) * D = V * D_1 \tag{3.2}$$

we can rewrite the above equation as,

$$D + D_1 = \frac{n_2 V_g * D_1}{V} \tag{3.3}$$

I_{peak} can be found from inductor equation during MOSFET turn on,

$$I_{peak} = \frac{(n_2 V_g - V) * D * T_s}{L} \tag{3.4}$$

Duty cycle D_1 is,

$$D = \sqrt[2]{\frac{V^2}{n_2 V_g * (n_2 V_g - V)} (\frac{2L}{RT_s})} \tag{3.5}$$

The equation(3.5) says that when the inductor current is discontinuous the required duty cycle to regulate an output depends on the load connected to that output. If multi output forward converter is operated in DCM each output may require different duty cycle. As the loads connected at different outputs may be different it is not possible to operate a Multi Output forward converter in DCM. **The cross regulation of auxiliary outputs of a Forward converter operating in DCM is not feasible.**

3.2 Flyback Converter

Single Output Flyback Converter

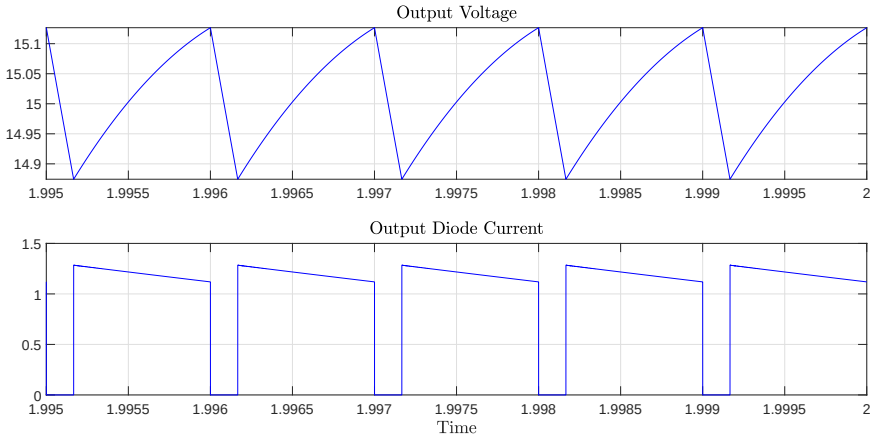


Figure 3.5: Output voltage and vurrent in a single output Flyback converter

Dual output Flyback Converter

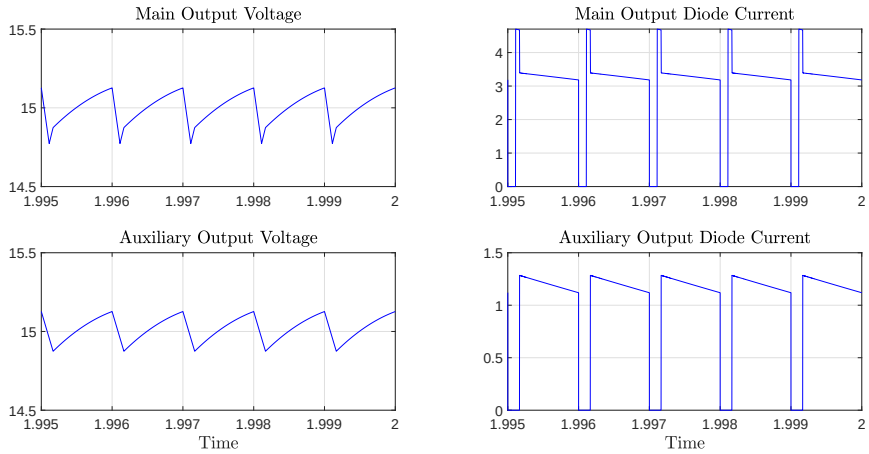


Figure 3.6: Output voltages and vurrents in a dual output Flyback converter

Lightly loaded Flyback Converter

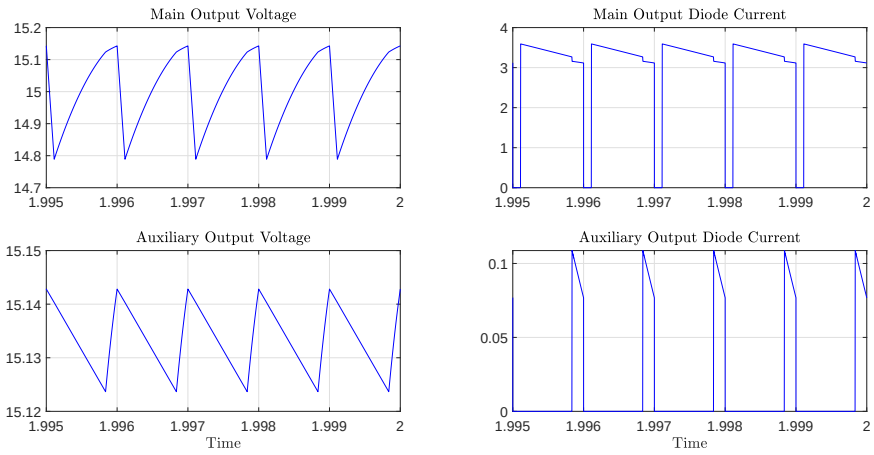


Figure 3.7: Lightly loaded dual output Flyback converter

In a Flyback converter the output voltages in single and dual output converters are regulated as shown in Fig.3.5 and Fig.3.6 respectively but it can be observed in Fig.3.6 that the output diodes doesn't start conducting simultaneously. Unlike Forward converter both main and auxiliary outputs are regulated even under lightly loaded conditions as shown in Fig.3.7. This is because the magnetizing current is still continuous as shown in Fig.3.8. In Fig.3.7 it can observed that the lightly loaded auxiliary output diode conducts for a very short duration of time. In a Flyback converter as magnetizing inductance is common for all the outputs, secondary diodes will make sure that heavily loaded converter gets more current and lightly loaded converter gets less current.

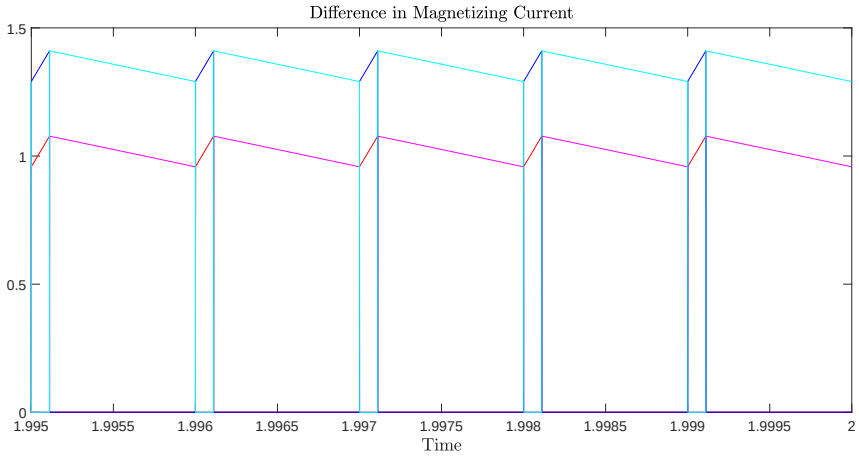


Figure 3.8: Difference in magnetizing currents of Flyback inductor

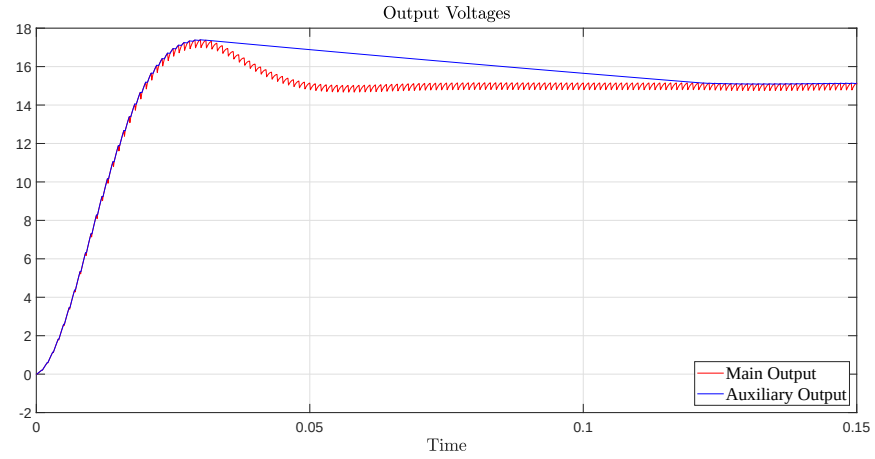


Figure 3.9: Lightly loaded dual output Flyback converter

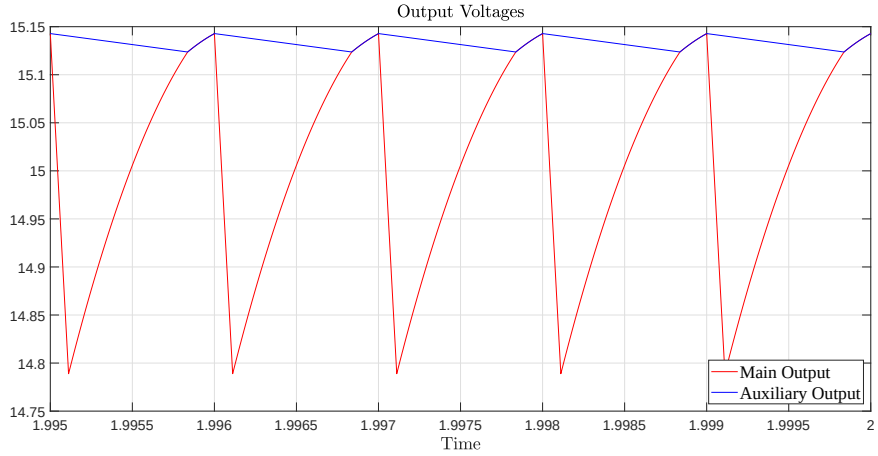
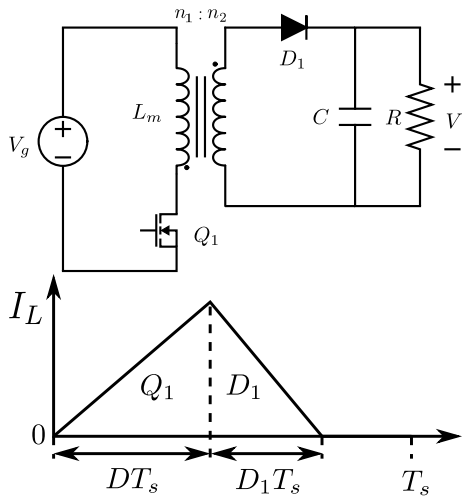


Figure 3.10: Lightly loaded dual output Flyback converter when settled

Under lightly loaded conditions it is observed that auxiliary output voltage of forward converter is higher than the required value because the auxiliary output inductor current was in discontinuous conduction mode as shown in Fig.3.4, where as for same load conditions in a flyback converter the main and auxiliary voltages had been maintained at the specified value. This is because the magnetizing inductor current in flyback converter is still in continuous conduction mode. What happens when this magnetizing current is discontinuous is discussed in next section.

3.2.1 Flyback in DCM



In Flyback converter average load current is equal to average diode current,

$$I_{load} = \frac{1}{2} * I_{Diode,peak} * D_1 \tag{3.6}$$

Peak of the inductor current is equal to sum of diode peak currents referred to primary side,

$$I_{peak} = \frac{2 * n_2 I_1}{D_1} + \frac{2 * n_3 I_2}{D_1} + \frac{2 * n_4 I_3}{D_1} \tag{3.7}$$

from the inductor equation peak current can also be written as,

$$I_{peak} = \frac{V_g * D * T_s}{L_m} \tag{3.8}$$

from Inductor Volt-Second balance equation,

$$D_1 = \frac{n_2 * V_g D}{V} \tag{3.9}$$

Duty Cycle is given by

$$D = \frac{1}{V_g} \sqrt{\frac{2 * (n_2 I_1 + n_3 I_2 + n_3 I_3) * L_m * V}{n_2 * T_s}} \tag{3.10}$$

In a Flyback converter the duty cycle in discontinuous conduction mode depends on the equivalent resistance, making multi-output converter operation in discontinuous conduction mode feasible.

3.2.2 Components Comparison among Forward Converter in CCM, Flyback Converter in CCM and Flyback Converter in DCM

In the previous sections, it is proved that a multi output Forward converter can't be operated in DCM where as a multi output Flyback converter can be operated in both CCM and DCM. The primary comparison which can be carried to decide among them is components comparison. Voltage and current stress across each switching device is presented in chapter 2. In this section the reactive elements like inductors, capacitors and transformer are compared. The expression and value of each component are listed in Table.3.1. The Forward converter has more number of magnetic components but the capacitance required is low. Flyback converter has least component count but the capacitance required is high. Among Flyback converters operating in CCM and DCM the capacitor values required in DCM mode of operation is higher.

Table 3.1: Required Components

Name of component	Type of Converter					
	Forward in CCM		Flyback In CCM		Flyback in DCM	
	Expression	Value	Expression	Value	Expression	Value
+15V Output Capacitance(μF)	$\frac{(0.1I_1)T_s}{8(0.01V_1)}$	2.50	$\frac{I_1DT_s}{0.01V_1}$	22.22	$\frac{I_1(1-D_1)T_s}{0.01V_1}$	95.69
-15V Output Capacitance(μF)	$\frac{(0.1I_2)T_s}{8(0.01V_2)}$	0.83	$\frac{I_2DT_s}{0.01V_2}$	7.41	$\frac{I_2(1-D_1)T_s}{0.01V_1}$	31.89
+5V Output Capacitance(μF)	$\frac{(0.1I_3)T_s}{8(0.01V_3)}$	12.5	$\frac{I_3DT_s}{0.01V_3}$	111.11	$\frac{I_3(1-D_1)T_s}{0.01V_1}$	478.46
+15V Output Inductor(μH)	$\frac{n_2V_gDT_s}{0.1I_1}$	200	nil	-	nil	-
-15V Output Inductor(μH)	$\frac{n_3V_gDT_s}{0.1I_2}$	600	nil	-	nil	-
+5V Output Inductor (μH)	$\frac{n_4V_gDT_s}{0.1I_3}$	40	nil	-	nil	-
Magnetizing Inductance(μH)	$\frac{n_1^2\mu_oA_c}{l_c}$	344	$\frac{n_1^2\mu_oA_c}{l_c}$	344	$\frac{n_1^2\mu_oA_c}{l_g}$	40

CHAPTER 4

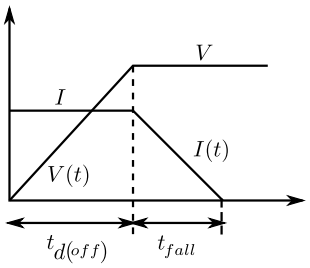
LOSSES IN A CONVERTER

4.1 MOSFET Losses

Conduction losses

$$P_{conduction} = I_{rms}^2 * R_{ds_{on}} \tag{4.1}$$

Switching Losses



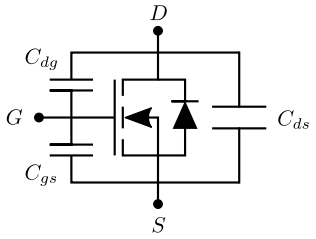
Switching Losses,

$$P_{switching} = (\frac{1}{2} * V_{peak} * I_{peak} * (t_{on} + t_{off})) * f_s \tag{4.2}$$

Table 4.1: Expressions for Switching Losses

Converter	Expression
Forward in CCM	$\frac{f_s}{2}(t_{on} + t_{off})V_{peak}(\frac{V_g DT_s}{L_m} + (I_o + \frac{\Delta I_o}{2}))$
Flyback in CCM	$\frac{f_s}{2}(t_{on} + t_{off})V_{peak}(\frac{V_g DT_s}{2*L_m} + \frac{I_o}{(1-D)})$
Flyback in DCM	$\frac{1}{2}(t_{off})V_{peak}(\sqrt{\frac{2V_1 f_s(n_2 I_1 + n_3 I_2 + n_4 I_3)}{n_2 L_m}})$

Output Capacitor losses,



$$P_{capacitor} = (\frac{1}{2} * C_{ds} * V_B^2) * f_s \tag{4.3}$$

MOSFET Specifications

Table 4.2: MOSFET Specifications

Parameter	Symbol	Value
Rated voltage	V_{DS}	800V
Continuous drain current	I_{DS}	11A
Output Capacitance	C_{oss}	15pF
Turn-on delay time	$t_{d(on)}$	10ns
Rise time	t_r	6ns
Turn-off delay time	$t_{d(off)}$	40ns
Fall time	t_f	10ns

Test conditions:$V_{DD} = 400V, V_{GS} = 13V, I_D = 4.5A, R_g = 7.5\Omega$.

Mosfet Losses vs Frequency

Table 4.3: MOSFET Losses

Switching frequency (kHz)	Forward in CCM		Flyback in CCM		Flyback in DCM	
	Conduction losses (W)	Switching losses (W)	Conduction losses (W)	Switching losses (W)	Conduction losses (W)	Switching losses (W)
50	0.32691	5.6827	0.473957	2.4553	0.587746	5.2619
100	0.24463	7.9933	0.309228	3.9512	0.415599	7.4860
150	0.21726	10.3039	0.25432	5.4472	0.339335	9.2102
200	0.20349	12.6145	0.22686	6.9432	0.293872	10.6757
250	0.19533	14.9251	0.21039	8.4391	0.262848	11.9759

4.2 Diode Losses

Conduction Losses

$$P_{Diode,Conduction} = V_f * I_{avg} \tag{4.4}$$

Forward voltage drop of selected schottky diode is $V_F = 0.16V$. As the average load current is same in all the converters, cumulative diode conduction losses in all the converters is equal to $1.44W$.

Reverse Recovery Losses
Diode recovery Losses are given by,

$$P_{Diode,recovery} = V_B I_{reverse} t_{recovery} f_s \tag{4.5}$$

Diode Losses vs Frequency

Table 4.4: Diode Losses

Switching frequency (kHz)	Forward in CCM		Flyback in CCM		Flyback in DCM	
	Conduction losses (W)	Rev.Rec losses (mW)	Conduction losses (W)	Rev.Rec losses (m)W	Conduction losses (W)	Rev.Rec losses (mW)
50	1.44	0.2567	1.44	0.05615	1.44	0.05615
100	1.44	0.5133	1.44	0.1123	1.44	0.1123
150	1.44	0.77	1.44	0.1684	1.44	0.1684
200	1.44	1.027	1.44	0.2246	1.44	0.2246
250	1.44	1.283	1.44	0.2807	1.44	0.2807

4.3 Resistor Losses

Resistance losses in Forward converter in CCM = $4.25W$

$(R_{+15} = 100k\Omega,\ R_{-15} = 300k\Omega\, and\, R_{+5} = 40k\Omega,)$

Resistance losses in Flyback converter in CCM = $11.5W$

$(R_{+15} = 19.592\Omega\, or\, R_{+5} = 2.176k\Omega)$

Resistance losses in Flyback converter in DCM = $0W$

4.4 Total Losses

Table 4.5: Total Losses

Switching frequency (kHz)	Forward in CCM (W)	Flyback in CCM (W)	Flyback in DCM (W)
50	11.9563	15.9254	7.3458
100	14.4412	17.3127	9.4539
150	16.9812	18.8099	11.1579
200	19.5350	20.3347	12.6390
250	22.0934	21.8702	13.9594

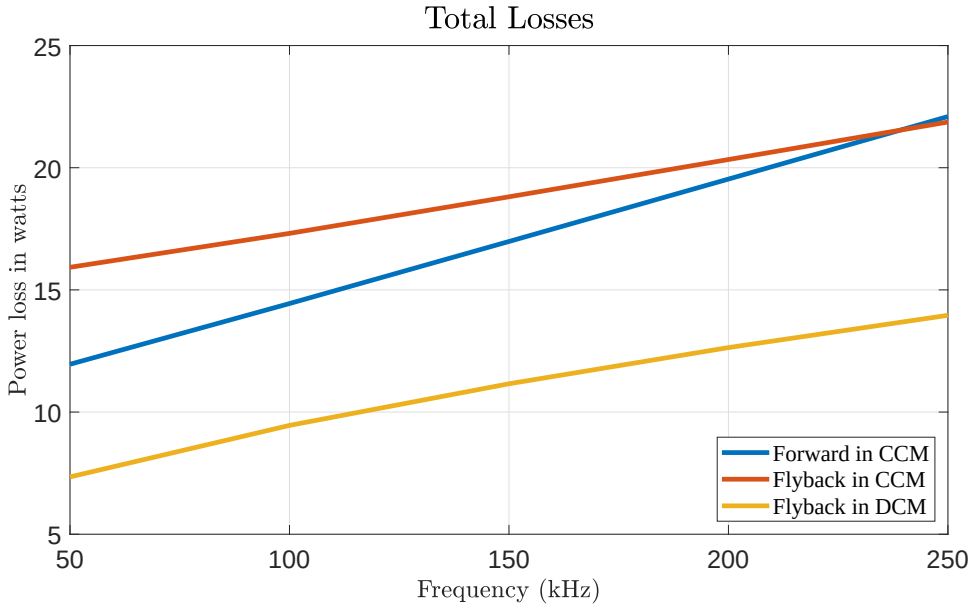


Figure 4.1: Total losses comparison

Selected Topology and Mode of Operation

Among Forward and Flyback converters, the Flyback converter has the least component count. It is understood that a Forward converter can not operate in DCM and connecting a resistor at each out of a forward converter is lossy proposition. After comparing losses in all the suitable converter typologies it is concluded that a Flyback converter operating in DCM is best suited for this application.

CHAPTER 5

HARDWARE IMPLEMENTATION

5.1 Transformer Design

Core is the vital element in a transformer as the frequency of operation and rating of the converter depends on it. Iron cores have higher saturation flux limit but they can not operate at high frequencies. In a Flyback converter, since the transformer is included in the switching converter it must operate at very high frequencies. "Ferrite" is usually used as core material in high frequency transformers. These ferrite cores are available in various shapes and sizes, **Area product** is the parameter used for core selection.

5.1.1 Area Product

Area product is the product of two areas known as the **Core area** and the **Window area**.

Core Area

Every magnetic core material will have a saturation limit. The saturating flux density of the ferrite cores in $B_{max} = 0.2T$. Magnetic flux density is related to magnetic field intensity H as

$$B = \mu_o H \tag{5.1}$$

Ampere's law states that the magnetic field intensity and the current passing through the conductor are related as

$$H = \frac{NI}{l_c} \tag{5.2}$$

where N is number of turns and l_c is mean magnetic length. The magnetizing inductance of a transformer with "N_p" primary turns is

$$L_m = \frac{N_p^2 \mu_o A_c}{l_c} \tag{5.3}$$

From equations (5.1), (5.2)and (5.3) we can derive an expression for core area A_c as

$$A_c = \frac{L_m I_{peak}}{N_p B_{max}} \tag{5.4}$$

The only unknown parameter in this expression is N_p and the above expression describes the the core area required for magnetic flux density to be less than the saturation limit when peak current flows in the winding.

Window area

A window in a transformer is the space between two adjacent limbs of the core. All the primary and secondary windings are wound on the central limb of the transformer. The window area should be sufficient to accommodate all these windings. The area occupied by one set of winding (primary/secondary) will depend upon number of turns and wire gauge of the winding. Every conducting material has a maximum allowable current density such that the wire doesn't melt due to conduction losses. Maximum current density for an enamelled copper wire $J_{max} = 3\frac{A}{mm^2}$.

$$A_{wire} > \frac{I_{RMS}}{J_{max}} \tag{5.5}$$

window area occupied by one set of winding (primary) is $N_p A_{wire} = N_p \frac{I_{P_{rms}}}{J_{max}}$.
window area required to accommodate all the set of windings is given by

$$A_w = \frac{N_p(I_{P_{rms}} + \frac{N_S}{N_P} I_{S_{rms}} + \frac{N_T}{N_P} I_{T_{rms}} + ...)}{K_w J_{max}} \tag{5.6}$$

Where K_w is a window constant, it is a safety factor given by $K_w = 0.35$. The ratios $\frac{N_s}{N_p}$ and $\frac{N_s}{N_p}$ are known values. The equations (5.4) and (5.6) have N_p but the primary number of turns is still unknown. If the equations (5.4) and (5.6) are multiplied one can observe that N_p gets cancelled and the resultant is a constant which is popularly known as **Area Product**.

$$A_c A_w = \frac{L_m I_{peak} I_{eq_{rms}}}{K_w B_{max} J_{max}} \tag{5.7}$$

Selected Transformer core

In this application area product is $A_C A_W = 2461mm^4$. An ETD core with the following dimensions has been selected for this application $ETD\ 39/20/13$ whose area product is $A_C A_W = 31701.6mm^2$.

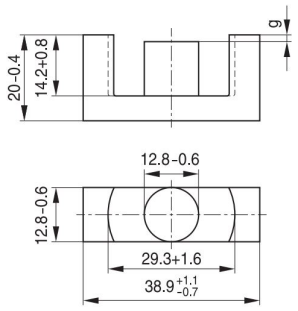


Figure 5.1: Core Dimensions

5.1.2 Number of turns and Air gap

Frequency	$100kHz$	$150kHz$	$200kHz$	$250kHz$
Number of Turns N_p	10.16	8.30	7.19	6.43
Air gap l_g in mm	0.418	0.279	0.209	0.167

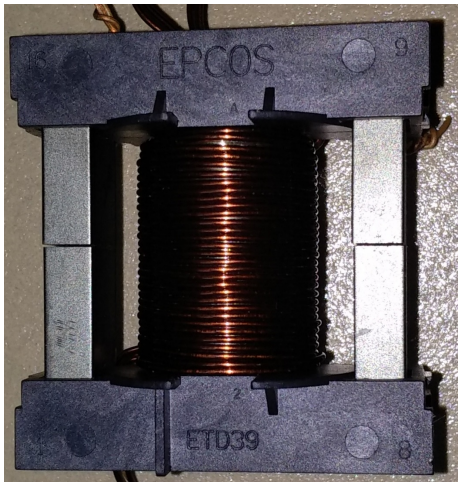


Figure 5.2: Transformer designed

5.2 Closed Loop Current Mode Control Using an IC UC3844

Current Mode control for closed loop output regulation can be implemented cost effectively and with minimum components using current mode control IC UCx84x series. IC UC3844 is specifically designed for off-line application. Fig.5.3 illustrates the internal functioning blocks of the IC.

5.2.1 Current mode control IC

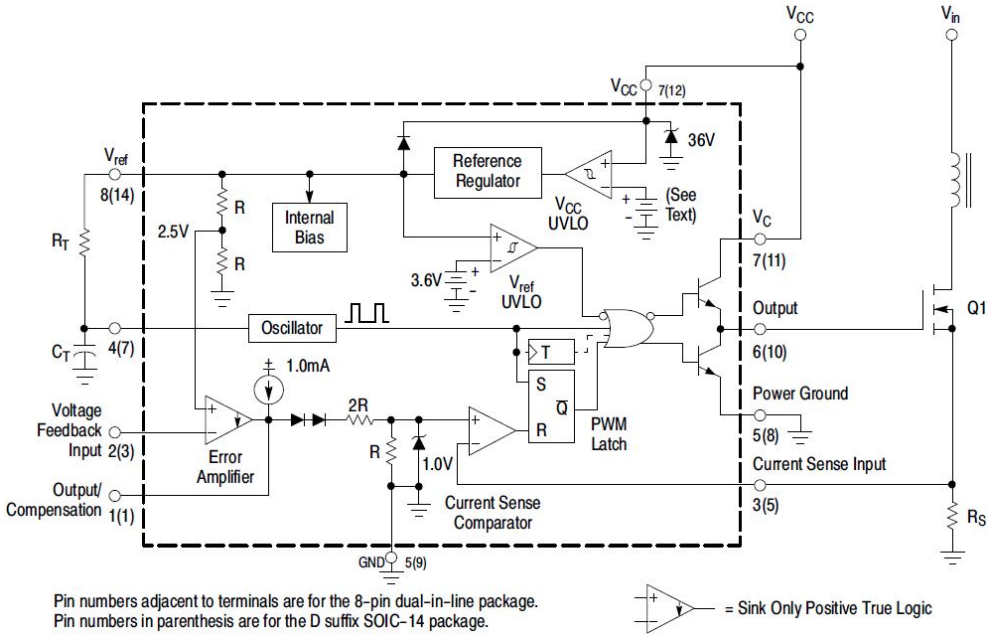


Figure 5.3: Internal blocks of IC, courtesy: UCx84x datasheet [8]

5.2.2 Advantages of using Current Mode Control IC

1. Current mode operation upto $500kHz$ switching frequency.
2. Latching PWM for cycle by cycle current Limiting
3. Under voltage lockout with hysteresis, $16V$ on and $10V$ off.
4. High Current Totem pole output.
5. Automatic feed forward compensation
6. Low start-up and operating current.

5.2.3 Closed Loop Current Mode Control

The duty cycle of the gate signal is generated by comparing the current passing through the switch with a reference value generated by voltage error as shown in Fig.5.4. The output voltage to current reference transfer function $G_{vi_c}(s)$ derivation is given in Appendix A. The bode plot of $H*G_{vi_c}(s)$ is shown in Fig.5.6. The bode plot error amplifier is given in the data sheet of the IC.

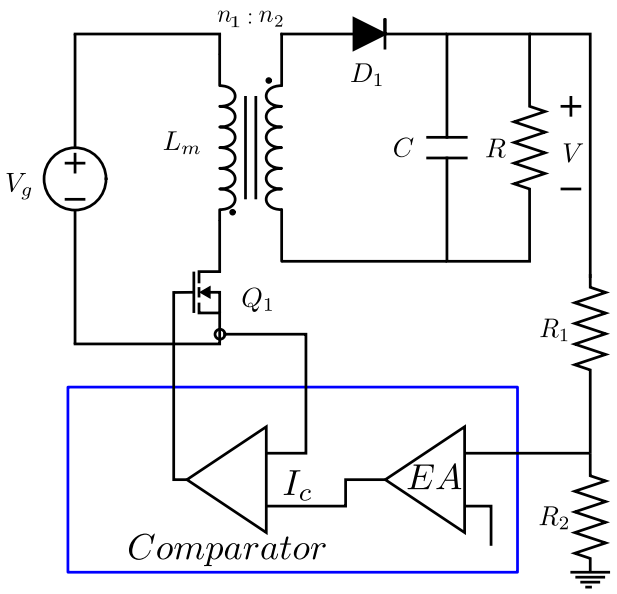


Figure 5.4: Closed loop control of Flyback Converter

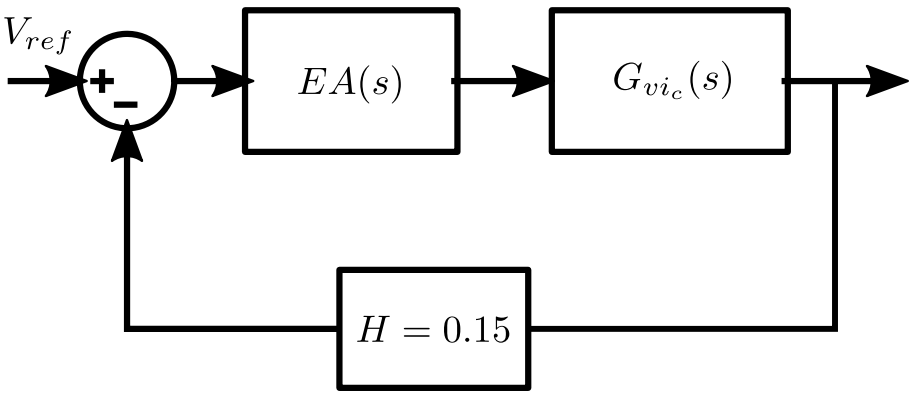


Figure 5.5: Block diagram of Closed loop control

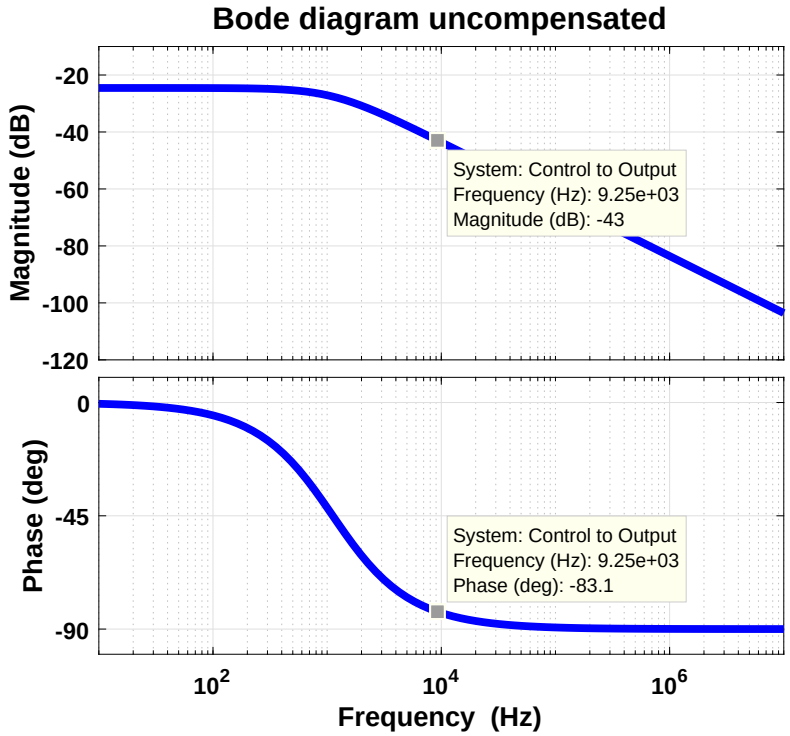


Figure 5.6: Bode plot of $G_{vi_c(s)}$

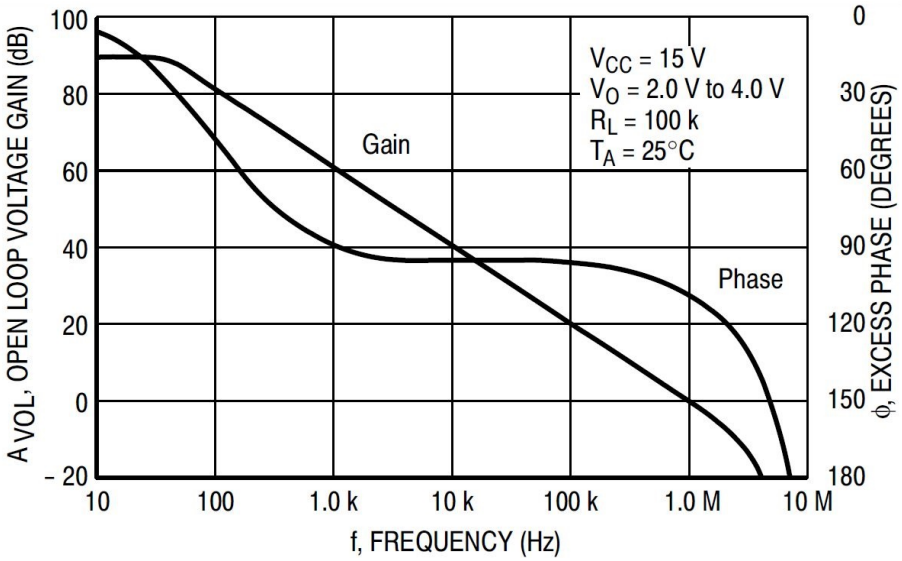


Figure 5.7: Bode plot of error amplifier, courtesy:UCx84x datasheet [8]

The estimated gain cross over frequency and phase margin of over all closed loop transfer function from Fig.5.6 and Fig.5.7 are

Gain Cross over Frequency (GCF) = 9.25kHz.

Phase Margin = 71^o

The attenuation near the switching frequency $f_s = 125kHz$ is approximately $-70db$. The closed loop system will be stable as the phase margin is positive and GCF is less than one tenth of switching frequency.

5.3 Schematic

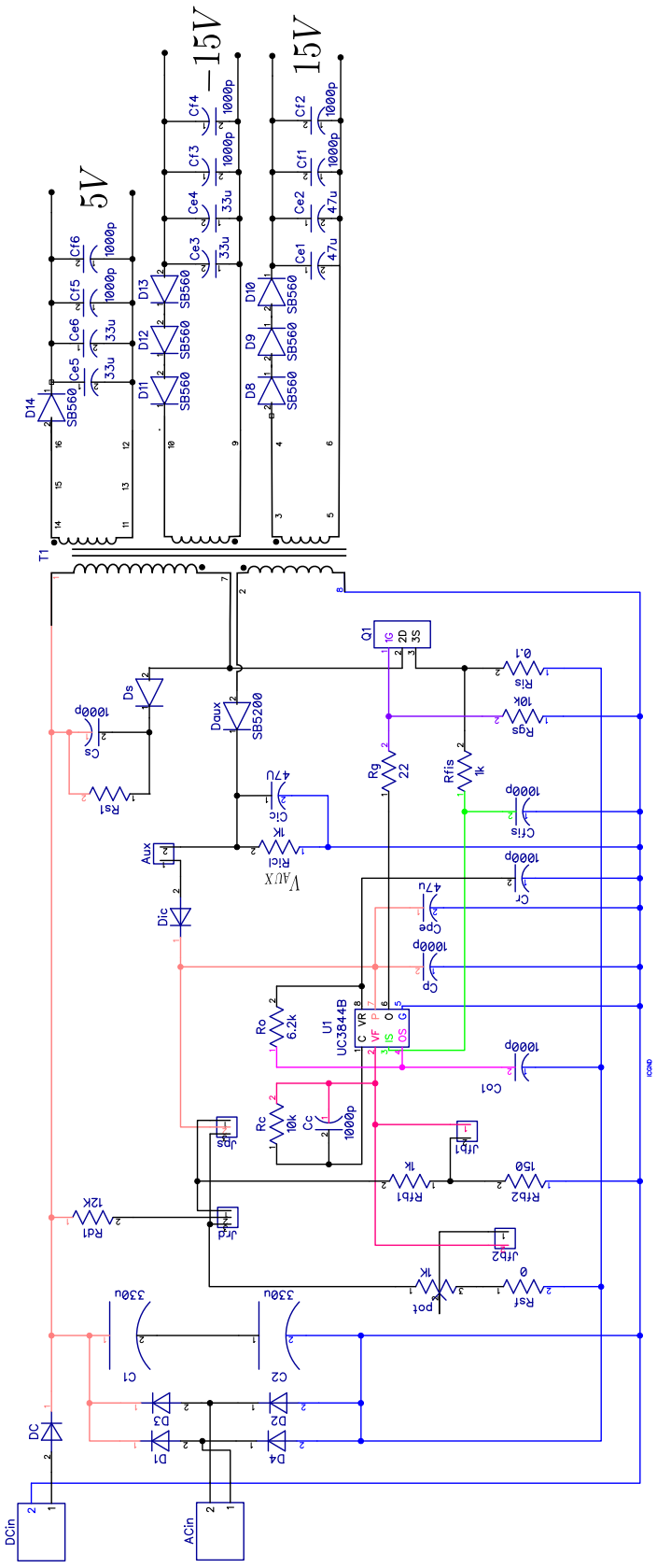


Figure 5.8: Schematic of converter designed

5.4 Layout

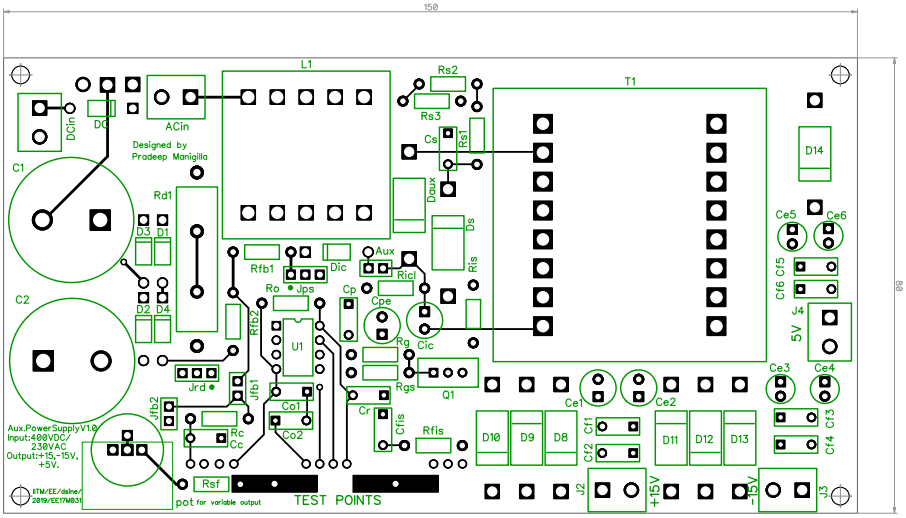


Figure 5.9: PCB Layout

5.4.1 Board

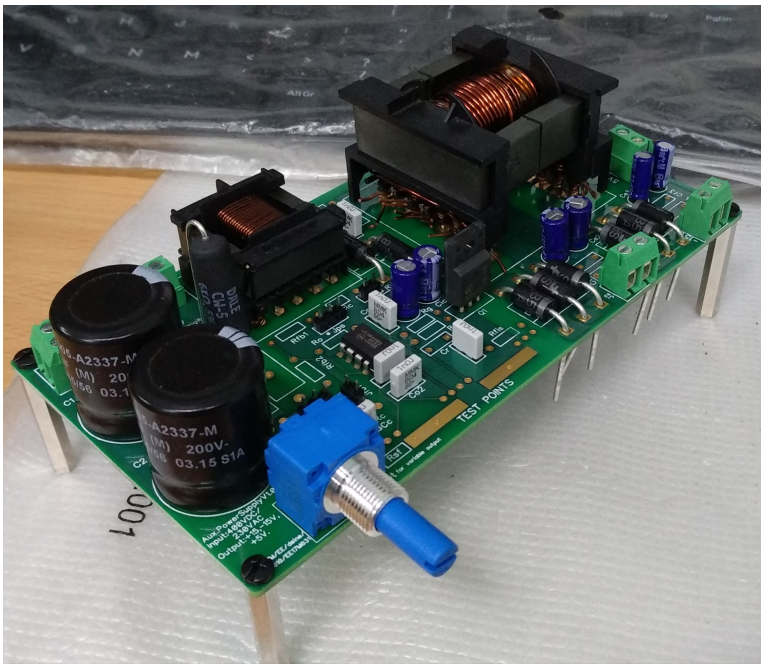


Figure 5.10: Assembled board

5.5 Components Selection

IC Startup Circuit

The IC turns-on when a voltage above $16V$ is applied. Once the IC is powered on the voltage can go as low as $10V$. When the converter is off the only available supply voltage is at input dc Bus capacitor. A resistor divider circuit is used to step down the input dc voltage and power the IC. The IC can draw current upto $17mA$. This lowers the voltage that is being applied to the IC. Care should be taken such that IC voltage doesn't go below $10V$ even when the IC draws current.The chosen Resistors are

$$R_1 = 12K\Omega$$

$$R_2 = 1K\Omega$$

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the $5.0V$ reference (pin 8) through the resistor R_T to approximately $2.8V$ and discharged to $1.2V$ by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the output to be in a low state, thus producing a controlled amount of output dead time. An internal flip-flop has been incorporated which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output dead time at a given frequency.
The chosen R_T and C_T are

$$R_T = 6.2k\Omega$$

$$C_T = 1000pF$$

Current Sensing

The UC3844B functions as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle by cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q_1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak MOSFET current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} = \frac{V_{Pin_1} - 1.4}{3} \tag{5.8}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input(Pin 2) and output (Pin 1) is provided. It features a typical dc voltage gain of $90dB$. The non inverting input is internally biased at $2.5V$. The converter output voltage is typically divided down and monitored by the inverting input. The Error Amp Output (Pin 1) is provided for external loop compensation. The output voltage is offset by two diode drops $(1.4V)$ and divided by three using resistor divider circuit before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the output (Pin 6) during soft start interval. The Error Amp minimum feedback resistance is limited by the amplifier's source current $(0.5mA)$ and the required output voltage to

reach the comparator's 1.0 V clamp level:

$$R_c = \frac{3.0 + 1.4}{0.5mA} = 8.8k\Omega \tag{5.9}$$

The Chosen values for compensation circuit are

$$R_c = 10k\Omega$$

$$C_c = 1000pF$$

Gate Circuit

The IC has a totem pole circuit for driving the gate of MOSFET as shown in Fig.5.3. The power supplied to the totem pole circuitry is same as IC power supply, this can be observed in Fig.5.3. Thus the gate voltage switches between Vcc and ground. The gate pin (pin 6) of the IC can give a maximum of 1A current, so gate resistance should be chosen such that the maximum current through this pin doesn't exceed 1A. It should also be noted that higher value of R_g increases the turn-on and turn-off times.

$$R_g > \frac{V_{cc}}{1A} \tag{5.10}$$

The chosen value of gate resistance for IC supply voltage V_{cc} of $18V$ is

$$R_g = 22\Omega$$

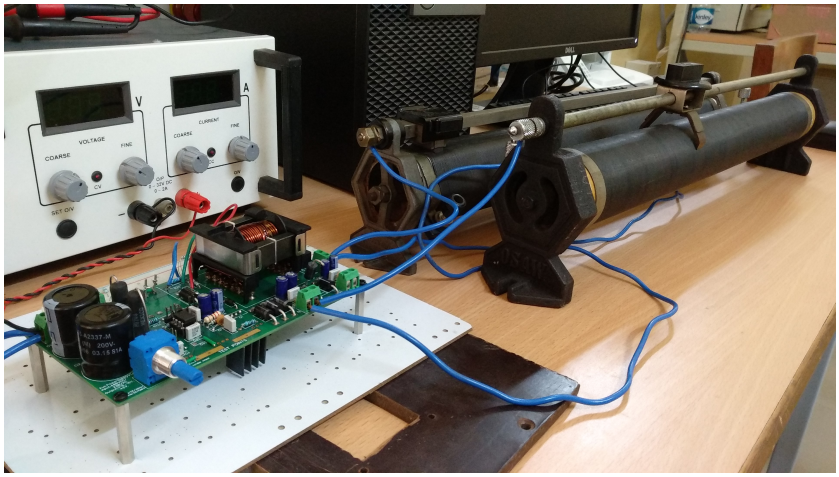


Figure 5.11: Designed Flyback converter hardware setup

5.6 Bill of Materials

Table 5.1: Bill of Materials

Name of Component	Manufacturer	Specification	Quantity	Cost
Diodes $D_1 \, to \, D_4, DC, D_{Aux}$	On Semiconductor	1N4007	6	30.00
Line Inductor				
(i)Transformer Core	EPCOS	E 25/13/7	2	84.96
(ii)Transformer Bobbin	EPCOS	10 Pin Bobbin	2	90.72
D.C.Bus Capacitor	EPCOS	$330\mu F$	2	424.80
Resistor	Vishay DALE	6K	2	227.02
Resistor	Ohmite	0.1	1	80.37
Potentiometer	Bourns	$1K$	1	397.62
Current Mode IC	On Semiconductor	UC3844	1	37.87
MOSFET	Infineon	$800V$, $11A$	1	123.12
Flyback Transformer				
(i)Transformer Core	EPCOS	ETD 39/20/13	2	184.20
(ii)Transformer Bobbin	EPCOS	16 Pin Bobbin	1	137.52
Electrolytic Capacitor	Panasonic	$33\mu F$	2	11.80
Electrolytic Capacitor	Panasonic	$47\mu F$	2	15.40
Electrolytic Capacitor	Panasonic	$100\mu F$	2	11.80
Film Capacitor	KEMET	$1000pF$	10	165.60
PCB			1	3275.00
			Total	5297.8

CHAPTER 6

HARDWARE TESTING AND RESULTS

The Flyback transformer is designed such that the converter can operate at any switching frequency greater than 100kHz. In chapter 4 we observed that losses in a converter increases with switching frequency. The oscillator section of the IC is designed such that the converter operates at a switching frequency of $125kHz$. The obtained frequency is $124.1kHz$ as shown in the Fig.6.1. The difference in the desired and achieved switching frequency is due to slight deviation in the resistance from actual specified value. Gate signal characteristics can be seen in Fig.6.2.

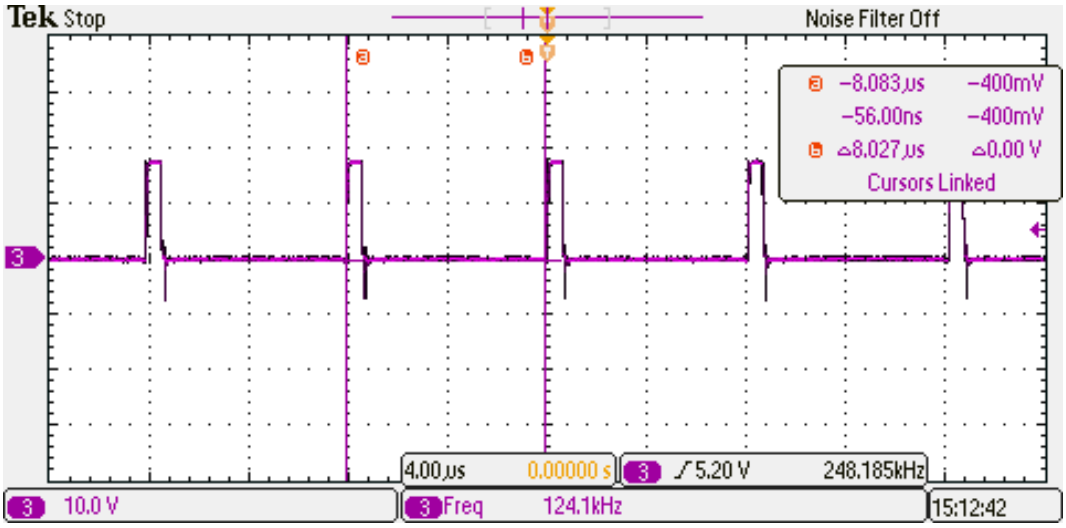


Figure 6.1: Switching frequency

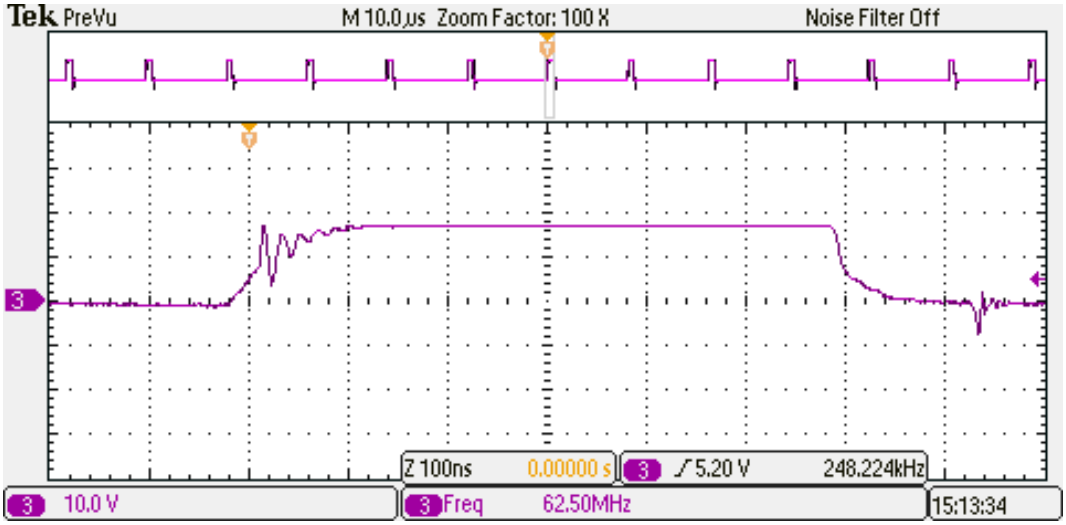


Figure 6.2: Gate signal characteristics

The converter can be powered either with dc or single phase ac voltage. The A.C. voltage is rectified before it is taken as input. The maximum input voltage rating of the converter is $400V$ dc. As mentioned in chapter 1 the input voltage range in this application is $(300, 400)V$ so the IC start up circuit is designed such that IC turns on when the input dc voltage is greater than $290V$. The converter input dc voltage should be higher than $290V$ for proper functioning of the circuit. A single phase A.C voltage is rectified and corresponding dc voltage is $328V$ as shown in the Fig.6.3. When loaded the average input voltage got reduced by a couple of volts and settled at $326V$ as shown in the Fig.6.4.

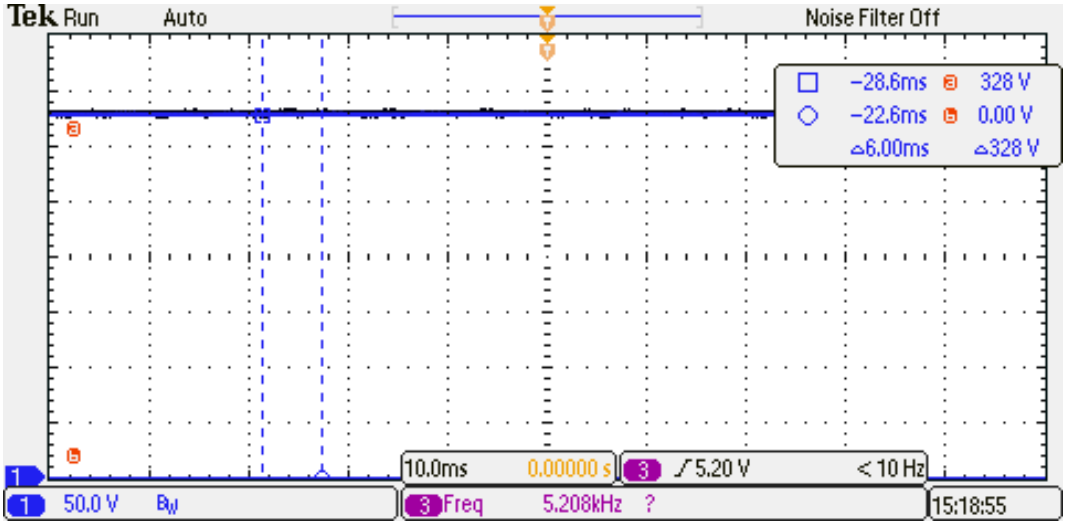


Figure 6.3: D.C. Voltage (Unloaded)

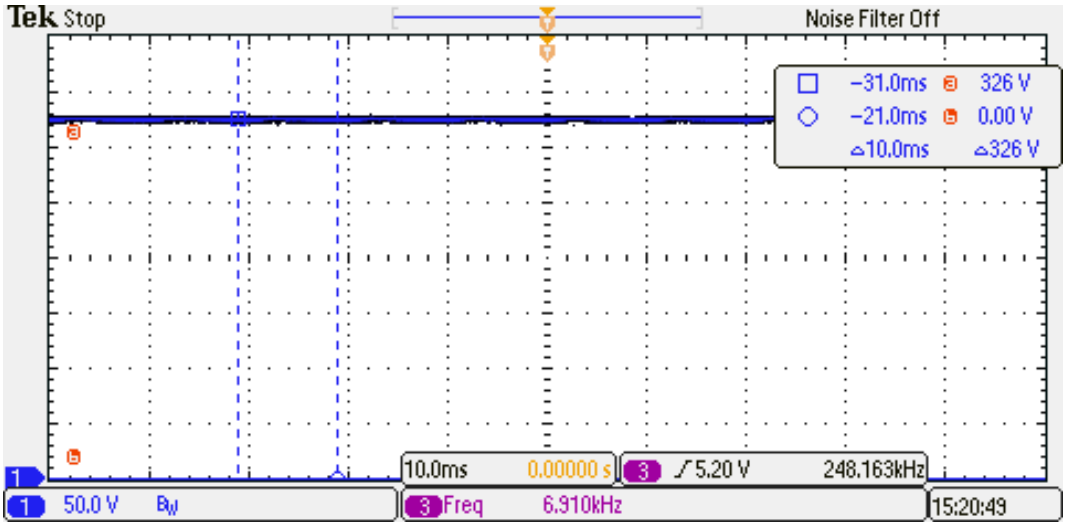


Figure 6.4: D.C. Voltage (Loaded)

A Flyback converter operating in DCM has three intervals of operation in one switching cycle they are,

Interval-1	$0\,to\,DT_s$	MOSFET is conducting
Interval-2	$DT_s\,to\,D_1T_s$	Diode is conducting
Interval-3	$D_1T_s\,to\,T_s$	Neither MOSFET nor Diode conducts

During the first sub interval $0\,to\,DT_s$ gate signal is high and the MOSFET is turned on. During this interval the voltage V_{ds} goes to zero which can be observed in the Fig.6.5, at DT_s a voltage spike appears across MOSFET drain and source due to leakage inductance of primary winding. A RCD snubber is connected across the primary winding to limit the overshoot in voltage, the observed voltage overshoot was $428V$ as shown in the Fig.6.5, During second sub interval $DT_s\,to\,D_1T_s$ the output diode conducts and the output voltage gets reflected on the primary side. During this interval the voltage across MOSFET V_{ds} is given by $V_g + V\frac{n_1}{n_2}$, in this application this voltage corresponds to $(328 + 15\frac{1}{0.3}) = 378V$ this can be observed in the Fig.6.6. During third sub interval neither MOSFET nor Diode conducts and voltage across primary winding is zero. The voltage across the MOSFET V_{ds} is equal to the input voltage i.e. $328V$ as shown in the Fig.6.7. The Gate signal, voltage across the MOSFET V_{ds} and the MOSFET current can be observed in the Fig6.8. It can be seen that the MOSFET current starts from zero while device is turning on. As a result the turn on losses in the MOSFET (expect for output capacitor losses) are zero for every switching cycle. This is one of the reason why the losses in a Flyback converter operating DCM are minimum.

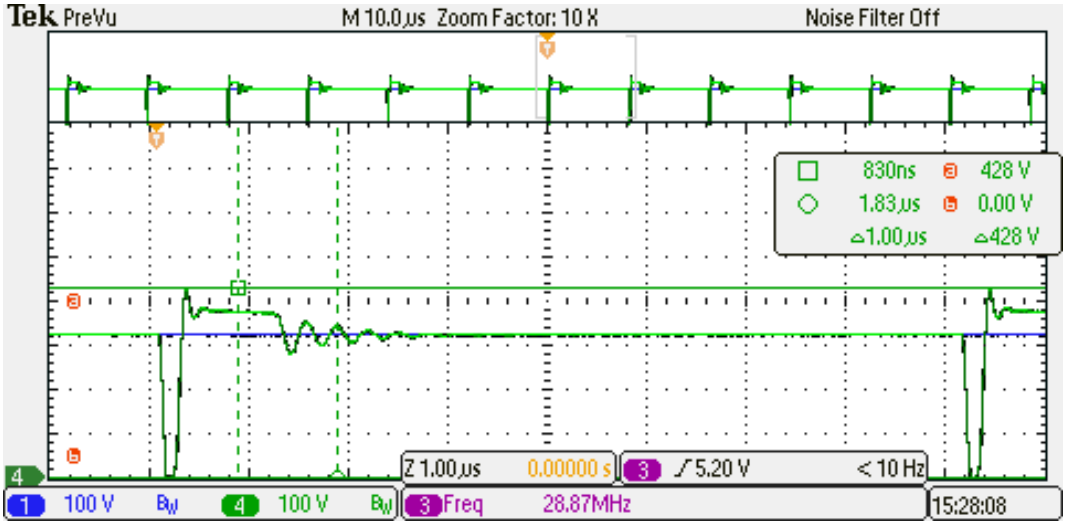


Figure 6.5: V_{ds} Overshoot

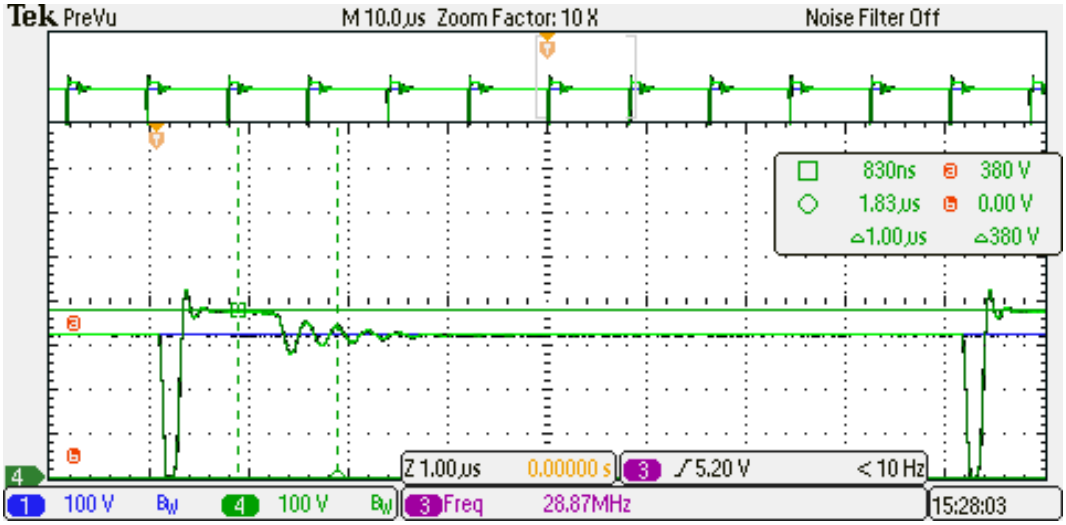


Figure 6.6: V_{ds} During diode conduction

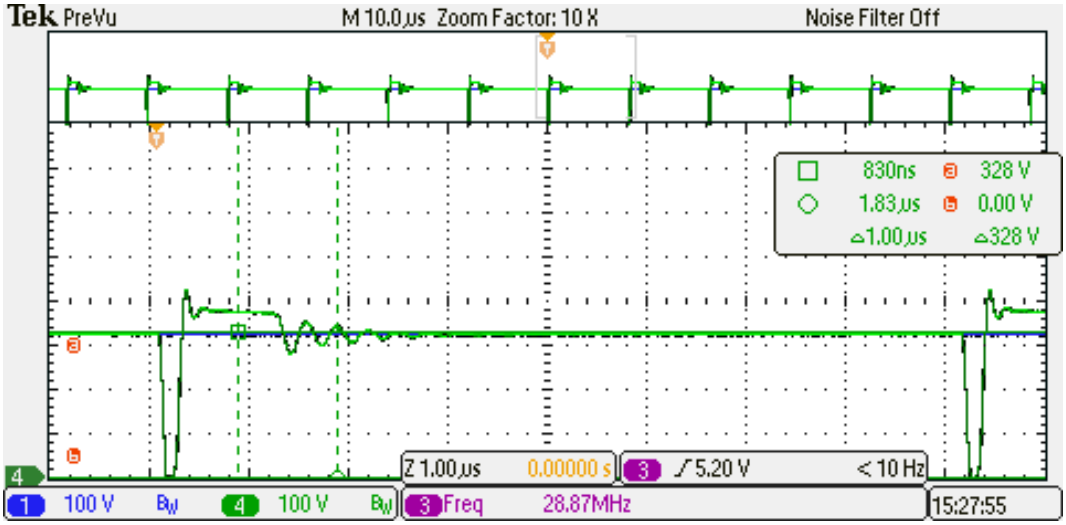


Figure 6.7: V_{ds} when flyback inductor current is zero

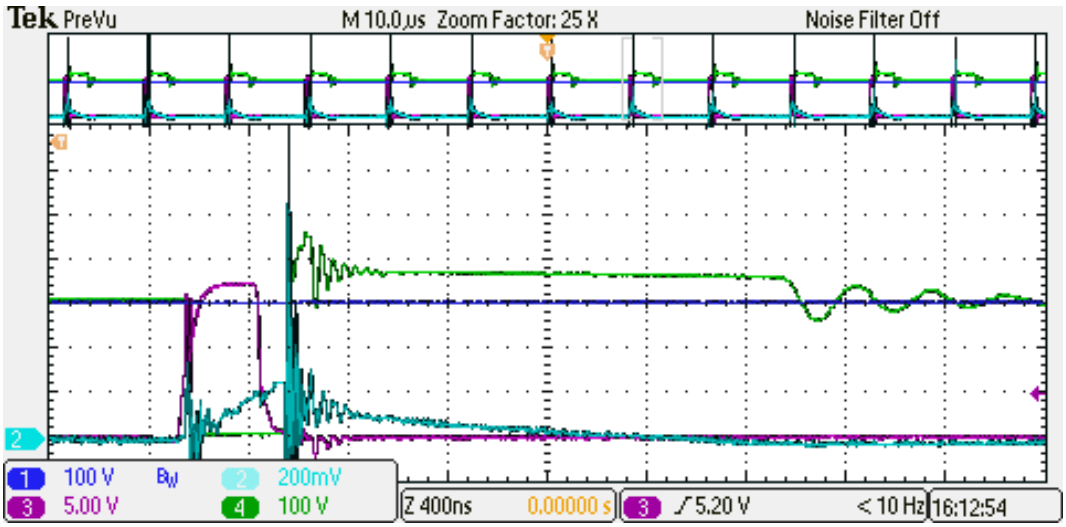


Figure 6.8: MOSFET current during conduction

The regulated output voltages at $+15V$ and $+5V$ can be seen in the Fig.6.9 and Fig.6.10 respectively.

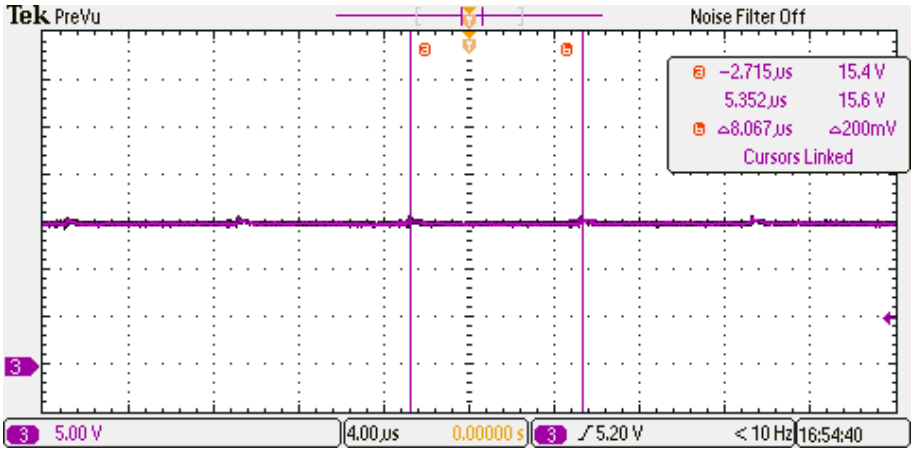


Figure 6.9: +15 output voltage

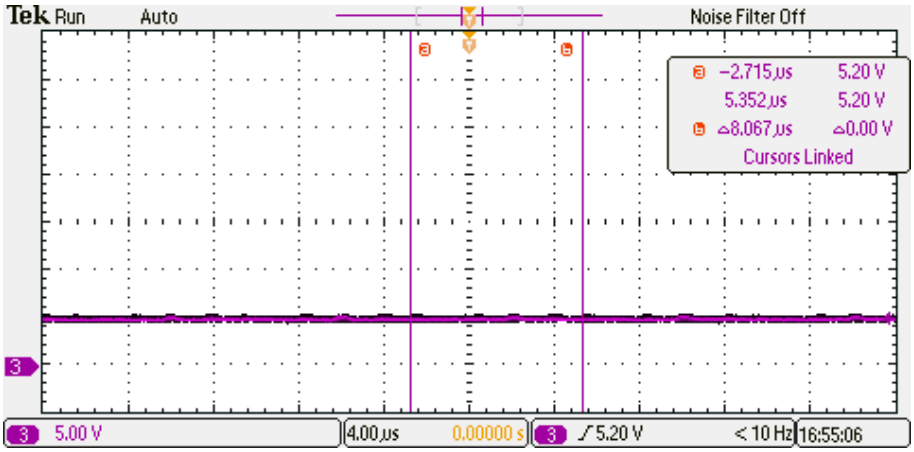


Figure 6.10: +5 output voltage

When there is a sudden change in load, it is observed that the current reference has settled to the new value with in $4ms$ (500 switching cycles) as shown in the Fig.6.11. The response was quick and it is acceptable in practical applications.

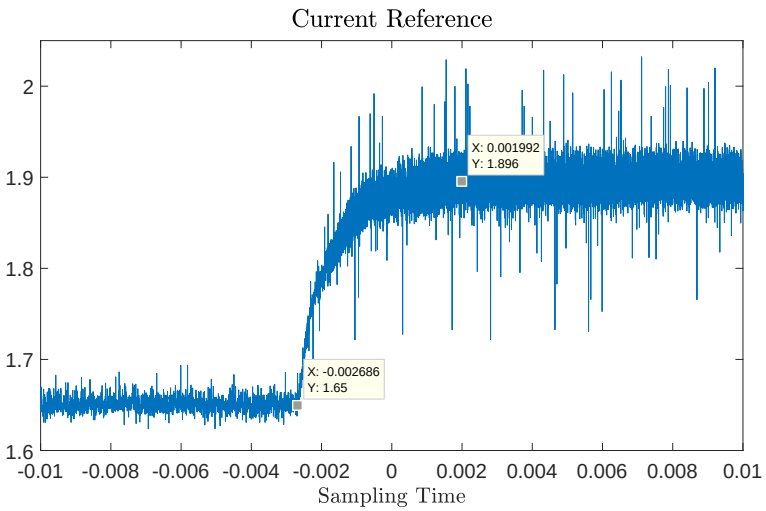


Figure 6.11: Current reference for a step change in load

CHAPTER 7

CONCLUSION

This work mainly emphasizes on selection of a suitable multi output isolated converter topology for low power applications. A detailed analysis is carried out to know the advantages and disadvantages in a few prominent isolated converter topologies in the literature. It is understood that Forward and Flyback converter topologies are most suitable for low power applications. A detailed analysis is carried out to know the feasibility of operating a multi output Forward and a multi output Flyback converter in CCM and DCM. It is understood that a multi output Forward converter can't be operated in DCM. After comparing losses in a multi output Forward converter operating in CCM and a multi output Flyback operating in CCM and DCM, it is found that a Flyback converter operating in DCM generates least losses. A Multi output Flyback converter is simple and economical to implement and as the losses are least in DCM operation a Flyback converter operating in DCM is finalized for hardware implementation.

Closed loop current mode control of a Flyback converter is achieved using a current mode control IC UC3844 as it is very cost effective and requires minimum components. The waveforms and results captured from hardware experimentation are as expected except for load regulation. The load regulation of output voltage is not as expected due to unavoidable leakage inductances.

APPENDIX A

Average Switch Waveform Model

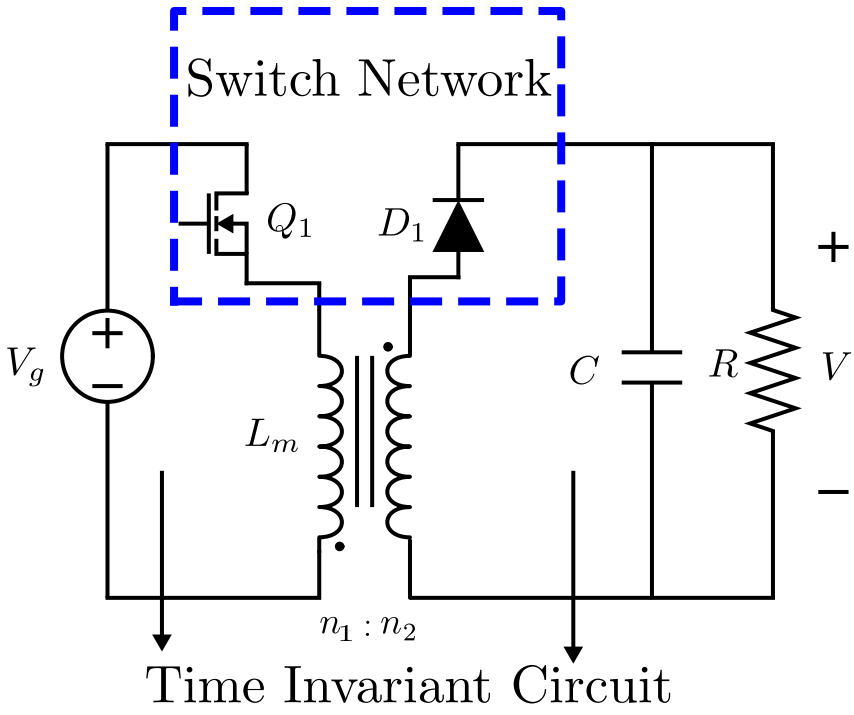


Figure A.1: Switch Network and time invariant network

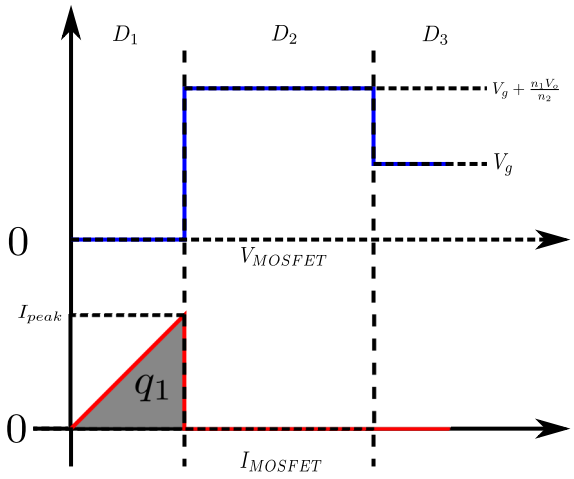


Figure A.2: MOSFET Switch waveforms

$$V_1 = (0D_1) + ((V_g + \frac{n_1 V_o}{n_2})D_2) + V_g(1 - D_1 - D_2) \tag{A.1}$$

we know that $\frac{n_1}{n_2} V_o D_2 = V_g D_1$

$$V_1 = V_g D_2 + V_g D_1 + V_g(1 - D_1 - D_2) = V_g \tag{A.2}$$

$$I_1 = \frac{q_1}{T_s} = \frac{D_1 T_s I_{peak}}{2T_s} = \frac{1}{2} I_{peak} D_1 \tag{A.3}$$

$$D_1 = \frac{I_{peak} L_m}{V_g T_s} \tag{A.4}$$

$$I_1 = \frac{1}{V_g} \frac{L_m I_{peak}^2 f_s}{2} \tag{A.5}$$

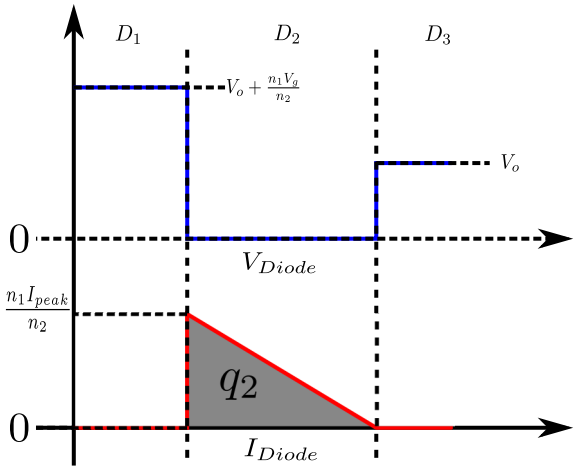


Figure A.3: DIODE Switch waveforms

$$V_2 = ((V_o + \frac{n_2 V_g}{n_1}) D_1) + (0 D_2) + (V_o(1 - D_1 - D_2)) \tag{A.6}$$

we know that $\frac{n_1}{n_2} V_o D_2 = V_g D_1$

$$V_2 = V_o \tag{A.7}$$

$$I_2 = \frac{q_2}{T_s} = \frac{n_1 D_2 I_{peak} T_s}{2 n_2 T_s} \tag{A.8}$$

$$I_2 = \frac{V_g}{V_o} I_{peak} D_1 \tag{A.9}$$

from equation (A.4)

$$I_2 = \frac{1}{V_o} \frac{L_m I_{peak}^2}{2} \tag{A.10}$$

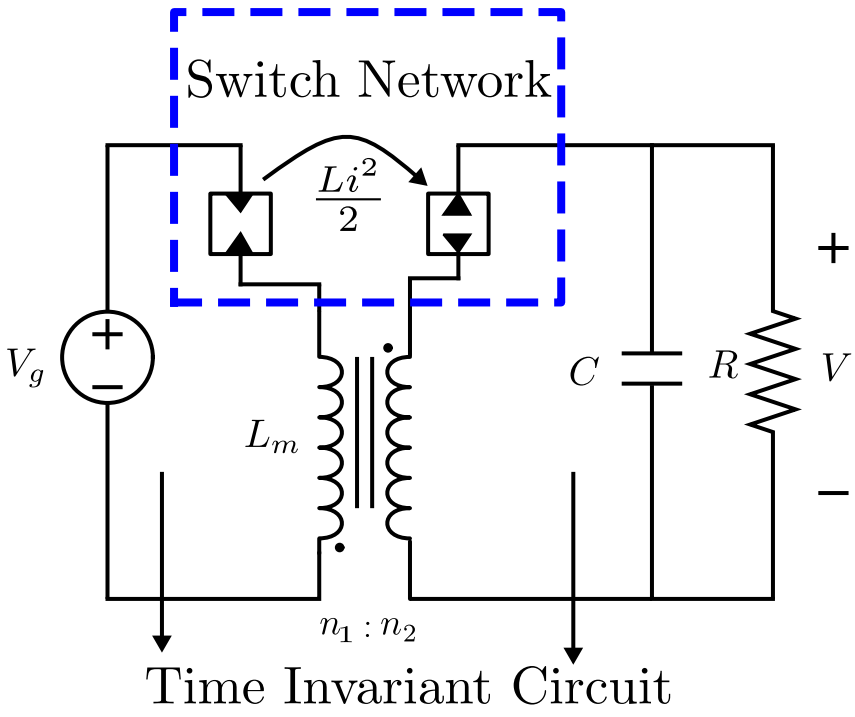


Figure A.4: Average switch model

Control to Output Transfer Function

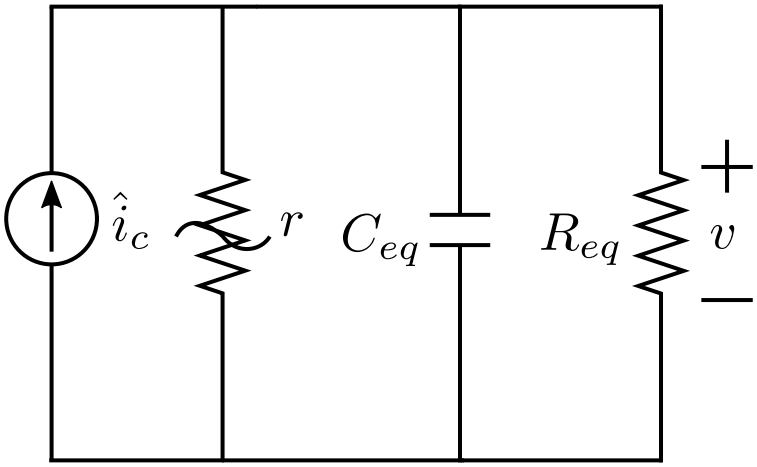


Figure A.5: Small signal model

$$G_{vi_c}(s) = \frac{R_{eq}}{2} \frac{1}{1 + \frac{s}{\frac{2}{R_{eq}C_{eq}}}} \tag{A.11}$$

The output voltage to reference current transfer function for this application is

$$G_{vi_c}(s) = \frac{0.3947}{0.0001421s + 1} \tag{A.12}$$

APPENDIX B

DC BUS CAPACITOR SELECTION

B.1 Voltage Ripple

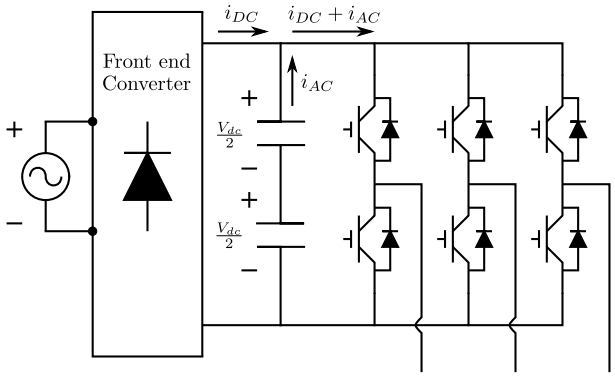


Figure B.1: DC Capacitor Currents

An inverter converts d.c power into a.c using power electronic switches. Usually in many applications electrical energy is first stored in batteries or capacitors which then act as dc bus of an inverter. In the present application the dc capacitors are charged using a front end converter. It is assumed that the front end converter maintains the dc bus voltage at $800V$ by supplying dc component of the load current. All other oscillating components of load current flows through d.c capacitors, as a result ripple is observed in dc bus voltage. This voltage ripple depends on the charge transferred from dc capacitors in one switching cycle which intern depends on load current. In a 10KVA inverter under balanced conditions, peak value of the load current is

$$I_{max} = \frac{10 * 10^3 * \sqrt{2}}{0.9 * 240} = 21.824A \tag{B.1}$$

B.1.1 Design objective

The aim of the inverter d.c bus design is to limit dc bus voltage ripple to less than 1% of V_{DC}, $V_{DC} = 800V$, 1% of V_{DC} is equal to $8V$. An inverter operating with SPWM technique is designed in MATLAB to compute dc component of load current and to

measure current flowing through the capacitors. The data of charge transferred from the capacitors for various load conditions is collected from simulation studies. It is observed that maximum charge transfer takes place when the inverter is operated in 180^o mode of operation and minimum value of net dc bus capacitance required to limit voltage ripple to less than $8V$ is $C = 1174\mu F$.

B.2 Capacitor RMS Current

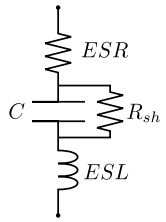


Figure B.2: Capacitor equivalent circuit

Physical capacitors are non ideal and have Equivalent Series Resistance (ESR), Equivalent Series Inductance (ESL) and a shunt resistance (R_{sh}) as shown in the Fig.B.2. Every capacitor will have a range of safe operating temperatures and thus have a limit on RMS current that it can supply. If the RMS current drawn from a capacitor exceed its limit then it leads to early capacitor failure. Thus RMS value of current flowing trough a capacitor is an important parameter for capacitor selection. Analytic expression of RMS current flowing through dc bus capacitors is given in [7] but only for balanced loads not for non linear loads. The expression for dc capacitor's rms currents under balanced load conditions is

$$I_{rms} = I_{peak}\sqrt{\frac{\sqrt{3}m}{4\pi} + (\frac{\sqrt{3}m}{\pi} - \frac{9m^2}{16}) * cos^2(\phi)} \tag{B.2}$$

The data of RMS current through the dc capacitors for various load conditions is collected from MATLAB simulation studies. It is observed that RMS current through the capacitors is highest when load current has 20% of 5^{th} harmonic and the value is 10.05A.

B.3 Balancing Resistor Selection

In dc bus design, capacitors are connected in series as shown in Fig.B.1. In the capacitor equivalent circuit of Fig.B.2 under steady state when capacitor is charged, capacitor 'C' acts as an open circuit and inductor 'ESL' acts as short circuit. The equivalent circuit then reduces to two resistors, 'ESR' and 'R_{sh}' connected in series where $R_{sh} \ >>> \ ESR$. Thus equivalent circuit can be approximated to just a shunt resistance across capacitor terminals. Shunt resistance is calculated from rated voltage and leakage current $R_{sh} = \frac{V_{rated}}{I_{leak}}$. In capacitor data-sheets leakage current is usually specified as a function of capacitance so the possible range of shunt resistance values depends on capacitor tolerance. The d.c. bus voltage distribution among the top and bottom capacitors depends on shunt resistances but no two capacitors have equal shunt resistance as a result d.c bus voltage is unequally distributed. External resistors can be connected in parallel to the capacitors such the net shunt resistance comes down and nearly becomes equal then the d.c bus voltage is almost distributed equally. In worst case condition it is assumed that shunt resistance in Fig.B.2 of top and bottom capacitors are at extremes and external resistors are selected such that deviation in top and bottom capacitor voltage is less than $8V$.

Table B.1: Components for DC bus design

Component	Specification	Manufacturer	Part number
d.c bus capacitor	$820\mu F$, Electrolyte capacitor	United Chemi-com	EKMZ451VSN821MR60S
Balancing resistor	$51.5\Omega,\ 6.5W$ Wire-wound resistor	Vishay	CW00551K50JB12

Datasheets

1. DC bus capacitor: $https://www.mouser.in/datasheet/2/420/ucc_KMZ-1210940.pdf$
2. Balancing resistor: $https://www.mouser.in/datasheet/2/427/cw-110764.pdf$

APPENDIX C

SNUBBER CAPACITOR SELECTION

C.1 Introduction

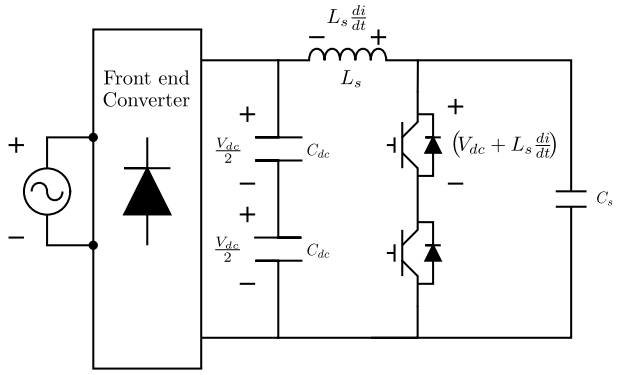


Figure C.1: DC Capacitor Currents

When a power device is turned off abruptly, trapped energy in the stray inductance causes a voltage overshoot across the device. The magnitude of these voltage transients depends on the switch current, turn-off time and stray inductance. Fast switching IGBTs have highly destructive transients as these devices switch large currents in short duration of time. A capacitor connected across one leg of an inverter as shown in Fig.C.1 will provide a path for stray inductor current and eliminates severe voltage transients across the switch. This capacitor is also called as **Snubber capacitor**. The Sunbber capacitor provides protection against voltage transients during turn-off operations thus allowing faster yet safer operation of switches.

The Snubber capacitor value for a permissible voltage shoot ΔV in a circuit with stray inductance of $_s$ is given by

$$C_s = \frac{L_s I_c^2}{\Delta V^2} \tag{C.1}$$

In this analysis stray inductance is taken as $1\mu H$ and ΔV is taken as $40V$. The computed value of snubber capacitor is approximately $0.4\mu F$. The RMS current through the snubber capacitor for various load conditions are listed in table.C.1.

Table C.1: Sunbber Capacitor RMS Currents

Condition	Peak Current	RMS Value
Balanced	22A	11.5A
$Fundamental\ +\ 10\%\, 5^{th}$	24.09A	12.12A
$Fundamental\ +\ 20\%\, 5^{th}$	25.96A	12.7A
$Fundamental\ +\ 10\%\, 7^{th}$	22.28A	11.07A
$Fundamental\ +\ 20\%\, 7^{th}$	24.01A	11.87A
$Fundamental\ +\ 10\%\, 5^{th}\ +\ 10\%\, 7^{th}$	22.19A	11.6A

Film capacitors have very low ESR values hence they can give high rms currents. A metallized polypropylene film capacitor is chosen as snubber capacitor.

Table C.2: Snubber Capacitor

Component	Specification	Manufacturer	Part number
Snubber capacitor	$4.7\mu F$, Polypropylene capacitor	EPCOS	B32774H0475K000

Datasheet

1.Snubber capacitor: $https://www.mouser.in/datasheet/2/400/MKP_B32774H_778H-1527434.pdf$

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