Hardware Implementation of Layermapping and Precoder for 5G NR Transmitter Chain

A Project Report

submitted by

MONILAL KOLEY

in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS

MAY 2019

THESIS CERTIFICATE

This is to certify that the thesis titled **Hardware Implementation of Layermapping and Precoder for 5G NR Transmitter Chain**, submitted by **MONILAL KOLEY**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nitin Chandrachoodan
Project Guide
Associate Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Dr. Radha Krishna Ganti
Project Co-Guide
Associate Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date: 09.05.2019

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude towards several people who enabled me to reach this far with their timely guidance, support and motivation. First and foremost, I offer my earnest gratitude to my guide, **Dr. Nitin Chandrachoodan** whose knowledge and dedication has inspired me to work efficiently on the project and I thank him for motivating me, allowing me freedom and flexibility while working on the project. I would like to thank my co-guide **Dr. Radha Krishna Ganti** who have guided me throughout the project.

REFERENCES

[1] 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; Physical channels and modulation (Release 15) (3GPP TS 38.211 V15.1.0 (2018-03)).

[2] Xilinx, Vivado Design Suite User Guide High-Level Synthesis (UG902). Xilinx (v2018.1) User Guide, 2018.

[3] Xilinx, Vivado Design Suite User Guide Implementation (UG904). Xilinx (v2018.1) User Guide, 2018.

[4] LogiCORE IP Fast Fourier Transform Product Guide (PG109).