Single Stage mmWave Beamformer Receiver for 5G Networks

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Single Stage mmWave Beamformer Receiver**, submitted by **Denish Dhanji Vaid**, to the Indian Institute of Technology, Madras, for the award of the degree of **DUAL DEGREE (BACHELOR OF TECHNOLOGY & MASTER OF TECHNOLOGY)**, is a bonafide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: 5G mobile communication, current-reuse, low-noise amplifiers, millimeter wave circuits, mixers, phase-shifters, phased-arrays, receivers.

The next generation of mobile communication standards, 5G networks, are expected to satisfy the exponentially growing demand for wireless capacity and data-rates. 5G networks are also set to open up new possibilities and spur innovations in various domains. However, multiple technologies and paradigms need to be materialized to tap the full potential of 5G networks.

On the circuits side, the critical challenge is the implementation of phased-array architectures with multiple antennas and channels on the RF front-end to support beamforming and massive-MIMO. Area and power-efficiency are also crucial to be able to accommodate the entire array of transceivers.

This thesis presents a new phase-shifting architecture that simplifies the RF front-end implementation and reduces its area and power consumption. The proposed architecture achieves IQ down-conversion without the use of quadrature LO signals. The single-stage receiver topology, which has been used for lower carrier frequencies, also fits into the proposed phase-shifting scheme. The analysis and optimization of this topology to work at mmWave frequencies are also presented here.

A 26GHz receiver implementing the proposed optimized single-stage topology was designed to validate its performance. The simulated results are also presented in this thesis.

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ABBREVIATIONS

ADC	Analog-to-Digital Converter
BB	Baseband
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DNW	Deep-Nwell
EM	Electro-Magnetic
ESD	Electrostatic Discharge
IC	Integrated Circuit
IF	Intermediate Frequency
IQ	In-Phase Quadrature-Phase
ISS	Impedance Standard Substrate
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MIMO	Multiple-Input Multiple-Output
mmWave	Millimeter Wave
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PA	Power Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PPF	Poly-Phase Filter
RF	Radio Frequency
RTPS	Reflection-Type Phase-Shifter
SoC	System-on-Chip
TIA	Trans-Impedance Amplifier
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier

NOTATION

$\mathbf{F_{LO}}/\omega_{\mathbf{LO}}$	Local-Oscillator Frequency
$\mathbf{F_T}/\omega_{\mathbf{T}}$	MOSFET Transit Frequency
γ	MOSFET Noise Coefficient
$\mathbf{g_M}$	MOSFET Trans-conductance
$\mathbf{k_B}$	Boltzmann Constant
$\mathbf{r_o}$	MOSFET Output-Resistance
$\mathbf{R_s}$	Standard Characteristic Impedance (50Ω)
$\mathbf{T}$	Absolute Temperature

CHAPTER 1

INTRODUCTION

The increased demand for higher data rates, better quality of service, lower latency, and larger wireless capacity has led to a rapid race to the establishment and deployment of the next generation of mobile communication standards, 5G networks. This new standard is envisioned to open up new possibilities in domains such as communication, security, healthcare, transportation, and consumer electronics. To make 5G networks a feasible solution to the increased demand, several technological innovations and advancements are being pursued both in academia and in the industry [5; 7].

1.1 Key Technologies and Challenges in 5G Networks

A variety of potential paradigms and technologies are expected to go into the realization of 5G networks [1]. The previous generations of mobile communications have all used lower carrier frequencies (up to 6GHz), which has led to spectrum congestion and lower quality of connections. Low-frequency carriers also limit the bandwidth of operation and the maximum capacity. 5G networks will tap the unused spectrum in the millimeter-wave (mmWave) frequency range to meet the projected data rate and capacity requirements.

However, mmWave transmissions suffer from more significant path loss and shadowing. This poses severe constrains on the traditional base station-mobile station link budget. The small cell paradigm combats this issue by using an extensive network of

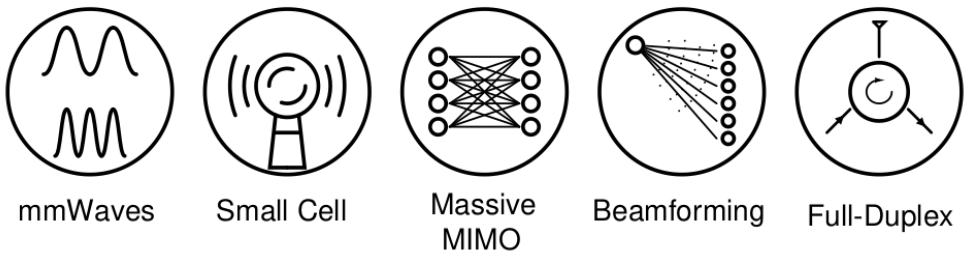


Figure 1.1: Potential enabling technologies for 5G

closely spaced miniature base stations instead of one large base station. This reduced size base station is made feasible by the smaller antenna size required for mmWave signal transmission. Smaller antenna sizes also allow the placement of multiple antennas on the base station and mobile station, paving the way for paradigms such as massive MIMO (multiple-input multiple-output) and beamforming. Massive-MIMO enables the operation of multiple data-links simultaneously, and can significantly improve the spectrum efficiency. However, the co-existence of multiple broadcast links can pose severe interference problems. This is resolved by beamforming, which uses phased-arrays to create highly directional and power-efficient links. Beamforming also helps mitigate the difficulties in closing the link budget in mmWave channels. Paradigms like full-duplex, which can enable simultaneous transmission and reception over the same frequency to further improve spectrum efficiency, are also being considered for the 5G standard.

1.2 IC Design and 5G Networks

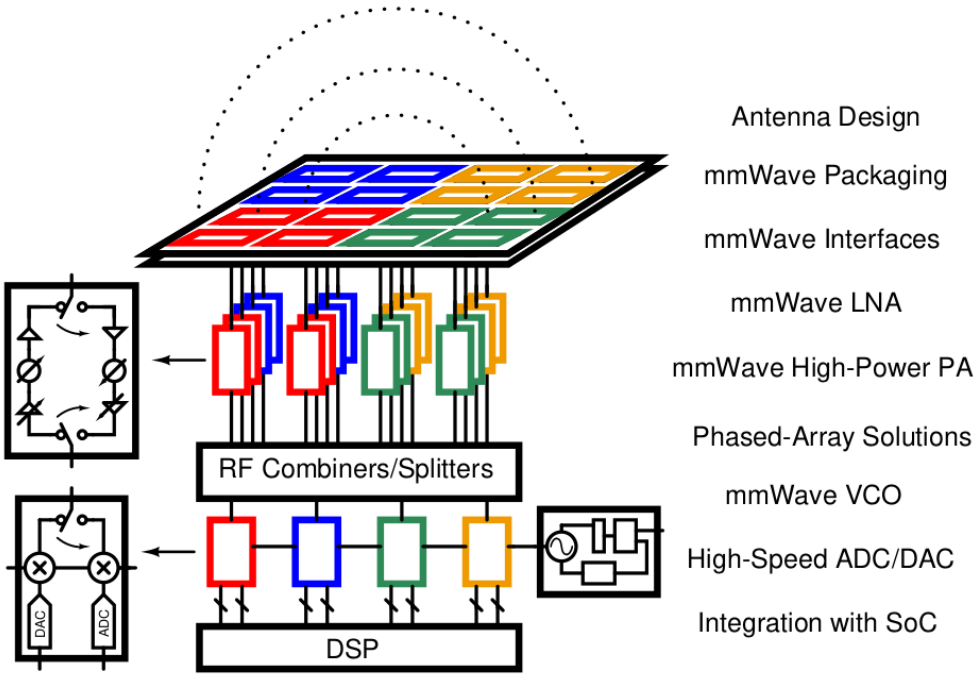


Figure 1.2: Typical 5G front-end architecture for supporting 4×4 MIMO with 4 antenna beamforming

IC design for mmWave circuits presents a variety of challenges that need to be overcome. These include pushing transistors to operate while approaching their transit fre-

quencies, ensuring efficient signal transmission on top of lossy silicon substrates, and running additional EM simulations for design verification and validation.

In the context of mmWave 5G networks, the design and integration of multiple RF channels required to meet the link budget is a major challenge. This involves low-power mmWave phased-array SoC, low-power low-noise amplifiers, mmWave EM interfaces and packages, mmWave VCOs with wide tuning range, and high-power high-efficiency mmWave power amplifiers.

The phased-array RF front-end, which allows beamforming, requires an array of transceivers and antennas with independent phase control. We address the primary circuit and system-level challenges involved in designing the receiver segment of the phased-array. Considering the requirements of a mobile station, we present a new phase-shifting architecture that results in a more compact and low-power design. A receiver that implements a single-stage topology with current reuse fits naturally into the proposed phase-shifting scheme. A new optimized single-stage topology is pre- sented here, along with the analysis and comparison of this topology with variants from past literature. A 26GHz receiver implementing this proposed single-stage topology with LO path Beamforming has been designed to validate its performance. The simulated results are also presented here.

Chapter 2 presents the proposed integrated phase-shifting scheme in the context of phased-array receivers. Chapter 3 discusses the conventional single-stage receiver and its working principle. Chapter 4 presents the design and analysis of the proposed optimized single-stage receiver topology, while Chapter 5 contains its implementation details and Chapter 6 presents the measurement results. Chapter 7 concludes this thesis

CHAPTER 2

THE PHASED-ARRAY

One of the key aspects of the mmWave 5G architecture is the use of phased-array RF front-ends with multiple antennas to support beamforming, which helps combat fading, shadowing, and path loss at mmWave frequencies. Several circuit architectures have been proposed in literature to integrate phase-shifters into a regular transceiver chain to make it a phased-array transceiver.

We consider the major phased-array receiver architectures and then illustrate a new phase-shifting architecture that results in a compact and low-power implementation.

2.1 Conventional Receiver Chain Implementations

We consider the conventional receiver chain consisting of an LNA, mixer, and ADC. A phased-array receiver can be realized using different phase-shifting architectures, such as LO-path phase-shifting [9],[21] RF-path phase-shifting [12; 8; 18], digital phase-shifting and hybrid phase-shifting [14].

The phase-shifting architecture employed changes the linearity, gain, noise, power, and area requirements of each block in the receiver chain. Phase-shifting in the RF path results in a low-power and area-optimized design (Figure 2.1). While this relaxes the linearity constraints on the mixer, the phase-shifter loss and noise figure become critical and need to be optimized. Phase-shifting in the LO-path increases the power and area overhead due to the presence of multiple mixers (Fig. 2.2). However, this scheme allows gain-invariant phase-shifting across the RF frequency range. Digital and hybrid phase-shifting results in a more flexible and reconfigurable architecture at the cost of much higher power and area overhead (Figure 2.2), as multiple RF channels have to be independently processed at baseband.

All of the above architectures require a phase-shifting circuit that has variable phase control [2]. Phase-shifting can be achieved by using passive techniques like switched

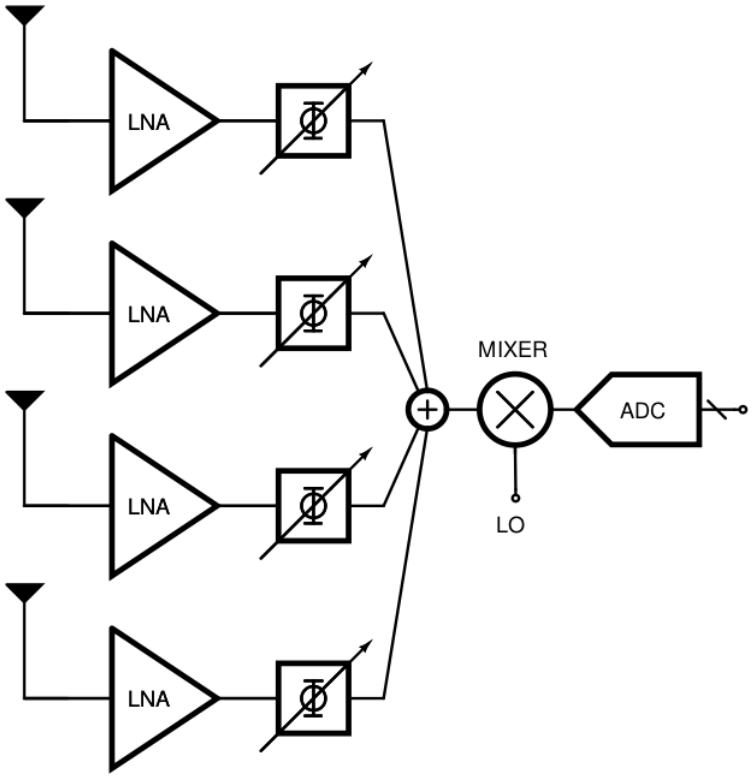


Figure 2.1: RF-path phase-shifting

LC sections [11; 8; 18] and RTPS [12], or by using active techniques, involving IQ signal generation and interpolation [21]. IQ signal generation can be achieved by using poly-phase filters (PPF) [17] or quadrature-hybrids [19].

Another critical implementation aspect is the choice of the IF frequency, leading to architectures such as direct-conversion, low-IF, sliding-IF, dual-conversion receivers, and direct-sampling. Direct-conversion receivers avoid the burden of image filtering and associated circuit power and area overheads, while the other IF architectures allow for easier signal processing and lower sensitivity to mismatch as they operate at a lower IF frequency [8].

Different schemes can be optimized for different requirements. We consider the requirements for a mobile station, which needs a low-power and area-efficient implementation. A direct-conversion RF-path phase-shifting scheme is chosen for this. We note that this scheme can be implemented for a variety of LNA and mixer topologies. We present an integrated phase-shifting scheme and single-stage receiver topology that complements each other to realize area and power optimization goals.

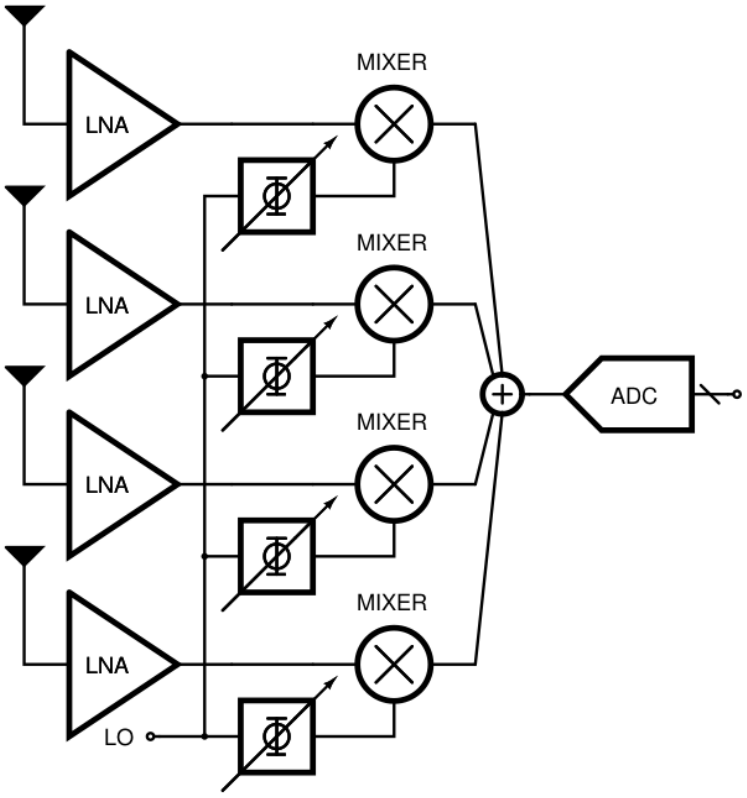


Figure 2.2: LO-path phase-shifting

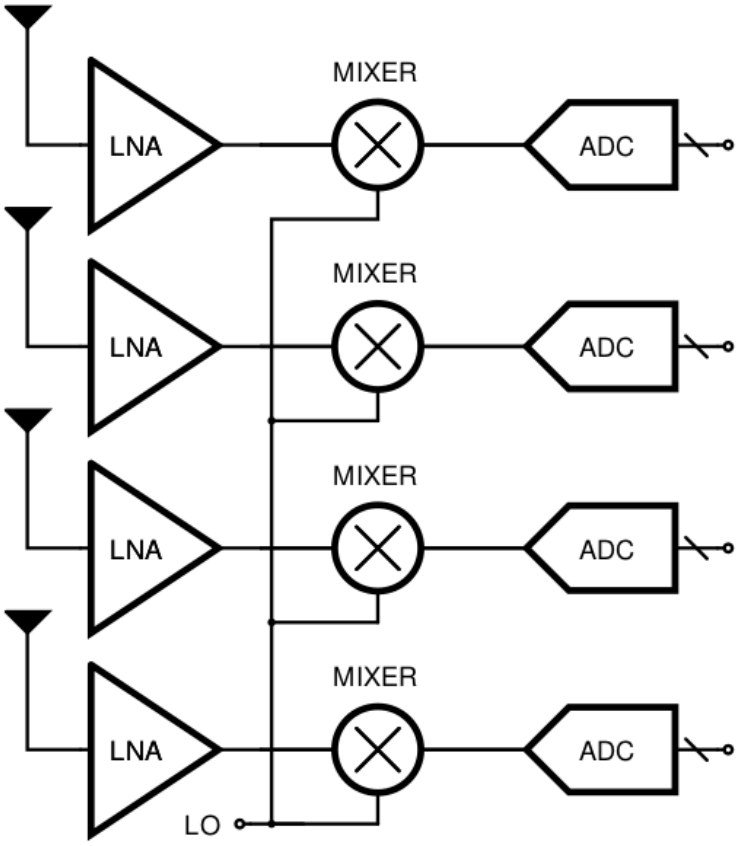


Figure 2.3: Digital phase-shifting

2.2 Proposed Integrated Phase-Shifting Scheme

We first consider a conventional direct-conversion 2-channel phased-array receiver (Figure 2.4), with phase shifting in the RF path describes a potential implementation of this architecture. We note that we are generating multiple phase-shifted versions of the input in the RF path. We are also generating quadrature-phase LO signals to implement an IQ Receiver.

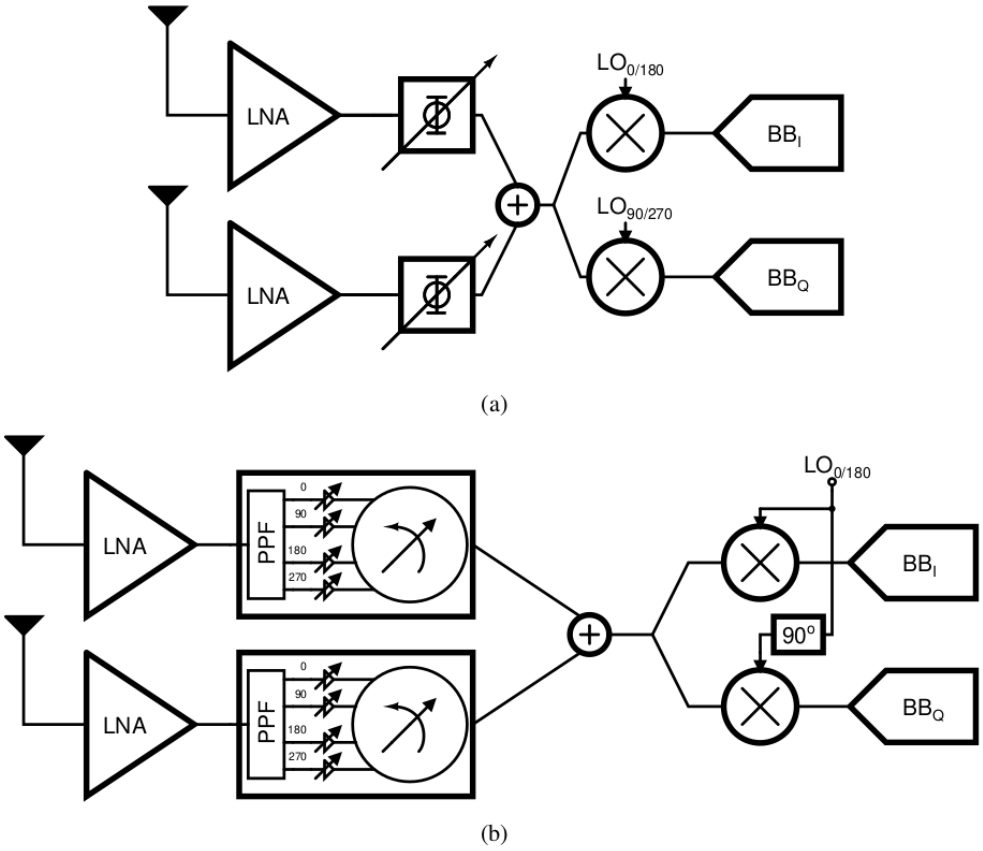


Figure 2.4: Conventional 2-channel phased-array direct-conversion receiver: (a) Top level block diagram; (b) Typical PPF-based implementation

The phase-shifter on the RF-path is essential for the phased-array to facilitate beamforming. The phase-shift on the LO-path is a constant 90° shift, as opposed to the variable phase-shifter on the RF-path. The LO-path phase-shift can be generated using a quadrature-hybrid, but it will lead to increased area overhead. A PPF-based implementation can be used, but it will require additional tuning and digital control for accurate quadrature generation. A QVCO is a viable solution for direct-conversion receivers

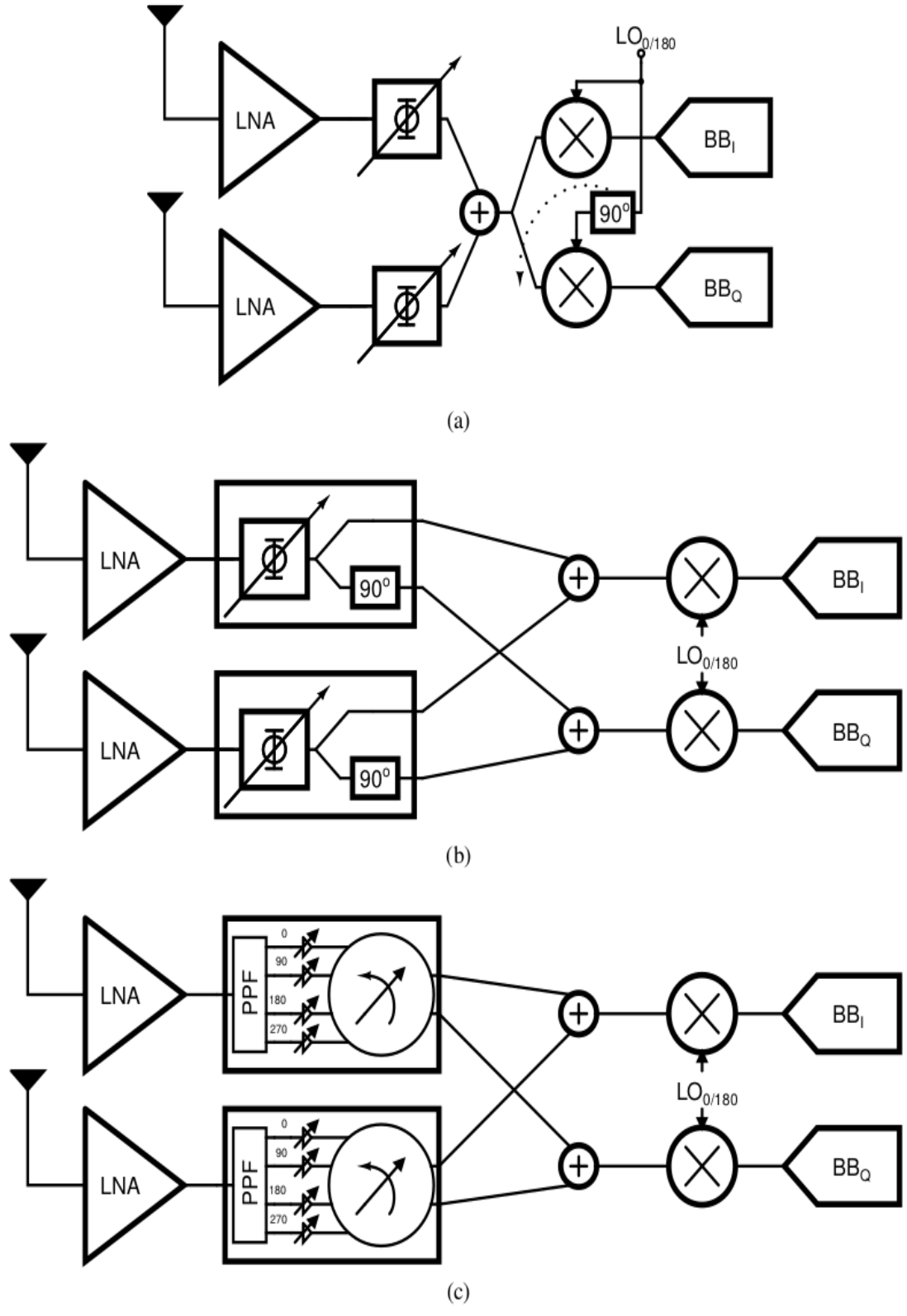


Figure 2.5: Proposed 2-channel phased-array receiver: (a) Development from conventional implementation; (b) Top level block diagram; (c) Current-steering PPF-based implementation.

[4; 8], as it can directly generate the required LO phases, but at the cost of tuning- range, phase-noise, power consumption, and area when compared to a regular VCO.

The proposed integrated phase-shifting scheme completely removes the need for quadrature LO signals, greatly simplifying the receiver architecture. This proposed architecture depicted in Figure 2.5 can be understood as moving the 90° phase-shift from the LO-path onto the RF-path. Now, instead of the phase-shifter giving a single phase-shifted output, it must also give a 90° phase-shifted output as well.

To motivate the realization of this scheme, we consider an active PPF-based phase-shifting scheme on the RF-path. The PPF will generate quadrature phase-shifted versions of the RF signal, which will then be appropriately summed to get the required phase-shifts. Assuming a current-mode implementation, this is equivalent to a form of current-steering, where a part of the current is used and summed at the output of the phase-shifter. The proposed implementation scheme shows how the part of the current not used to generate the output phase can be utilized to generate a quadrature phase-shifted output as well. For this scheme to work, we need to show that for any given phase-shift on the RF-path, we can also generate quadrature phase-shifted outputs that can be down-converted by mixers without the need for quadrature LO signals.

2.3 Working of the Integrated Phase-Shifting Scheme

We assume that we have quadrature phases of the input signal, with a fixed amplitude. A PPF or a quadrature-hybrid can generate this. We also assume that if a part of the signal is used to generate one phase, the remaining part of the signal can be used to generate another phase. A current-mode implementation naturally gives this flexibility.

Our objective is to show that given the input quadrature phases 0°, 90°, 180° and 270°, we can generate quadrature phase-shifted signals of any required phase-shift.

Let v_k represent one of the input quadrature phases (0°/90°/180°/270°), and v_{k+1} be the input phase 90° shifted from it. Hence, in this notation, $v_{k+2} = -v_k$.

Let the required output phase lie in the quadrant characterized by the input phases v_i and v_{i+1} such that

$$s_{I+} = \alpha v_i + \beta v_{i+1} \tag{2.1}$$

where α and β are the scaling coefficients. We can also generate its differential counterpart as follows:

$$s_{I-} = \alpha v_{i+2} + \beta v_{i+3} \tag{2.2}$$

This is the conventional implementation, where each input phase is used once to generate either the in-phase positive or in-phase negative signal. However, we note we can also generate the following signals using the part of the input signals not used in generating the in-phase output.

$$\begin{aligned} s_{Q+} &= (1-\beta)v_{i+1} + (1-\alpha)v_{i+2} \\ s_{Q-} &= (1-\beta)v_{i+3} + (1-\alpha)v_i \end{aligned} \tag{2.3}$$

Orthogonality of s_{I+} and s_{Q+} can be satisfied by ensuring that their dot product evaluates to zero, giving the relation

$$\begin{aligned} s_{I+} \cdot s_{Q+} &= (\alpha v_i + \beta v_{i+1}) \cdot ((1-\beta)v^*_{i+1} + (1-\alpha)v^*_{i+2}) \\ 0 &= -\alpha(1-\alpha)|v|^2 + \beta(1-\beta)|v|^2 \\ \Rightarrow \quad \alpha(1-\alpha) &= \beta(1-\beta) \\ \Rightarrow \quad \alpha + \beta &= 1 \end{aligned} \tag{2.4}$$

It can also be shown that this relation for α and β also ensures that the magnitude of each of the output phases is equal for any given phase-shift. However, there is an amplitude dependence across phase-shifts, which can be corrected.

Hence, our integrated phase-shifting scheme is as follows:

1. Choose the quadrant in which the required output phase-shift is present. Let the input phases that form this quadrant be v_i and v_{i+1}
2. Choose the scaling factor α such that the required phase-shift is obtained with the combination $\alpha v_i + (1-\alpha)v_{i+1}$
3. The output phases will now be
   (a) $s_{I+} = \alpha v_i + (1-\alpha)v_{i+1}$
   (b) $s_{I-} = \alpha v_{i+2} + (1-\alpha)v_{i+3}$
   (c) $s_{Q+} = \alpha v_{i+1} + (1-\alpha)v_{i+2}$
   (d) $s_{Q-} = \alpha v_{i+3} + (1-\alpha)v_i$

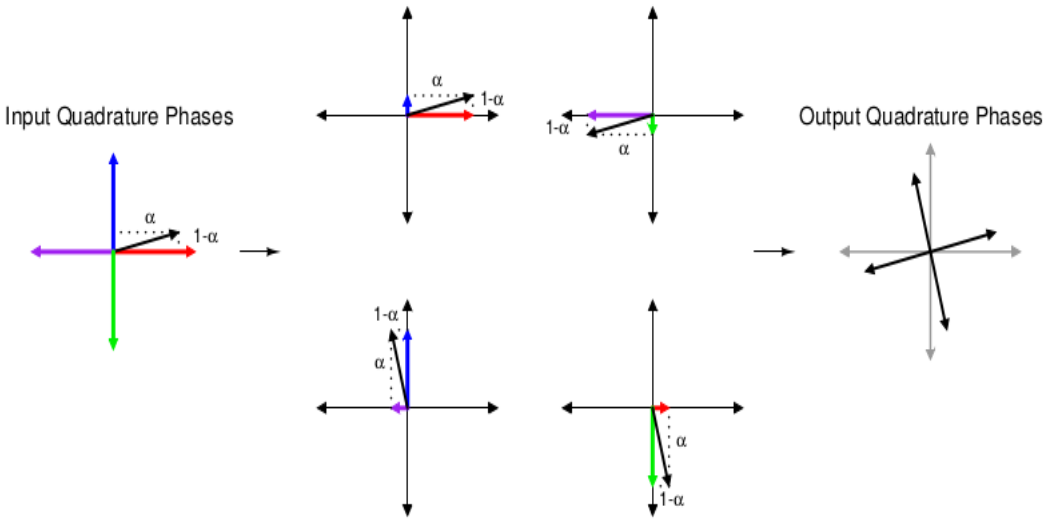


Figure 2.6: Illustration of the working of the integrated phase-shifting scheme.

It can be shown that the maximum to minimum amplitude variation for this phase-shifting scheme is 3dB (or a 1.5dB variation about the average). This scheme is illustrated in Fig. 3.3, where each of the input quadrature phases is split into two parts to generate the required output quadrature phases.

The key aspect of this scheme is the full use of the generated quadrature phases of the RF signal, which is used to achieve IQ down-conversion without the need for quadrature LO signals, significantly reducing the area and power requirements of the receiver. This is different from using a phase-shifter that can give quadrature phase-shifted outputs by using two independent paths for the I and Q outputs, and thereby incurring larger area and power overheads.

While we have eliminated the 90° phase-shift on the LO-path, we could have chosen to eliminate the phase-shifting in the RF-path instead. However, the resulting topology would require multiple mixers to achieve IQ down-conversion, adding area and power penalties. We have emphasized a current-steering PPF-based RF-path phase- shifting for a more power-efficient architecture and compatibility with the single-stage topology that further brings down power and area. A quadrature-hybrid based approach has been proposed in [19], but instead of using the quadrature RF signals to eliminate quadrature LO signals, it attempts to use both the signals to down-convert two conjugate beams simultaneously, at the cost of additional mixers and baseband channels.

CHAPTER 3

IMPLEMENTATION OF PHASE SHIFTER

This brief implements LO path Phase Shifting scheme. An advantage of this technique is that the Phase Shifter non-idealities are not in the RF path. The signal combining is done at the IF frequency band which makes the realization of the combiner easier than the RF combining technique due to much lower operating frequency. Linearity requirements of the IF and baseband building blocks will be relaxed as a result of the attenuation of unwanted signals through spatial filtering of the phased array. The other advantage is that since phase shifters are inserted in LO paths of mixers, their noise and non-linearity will have minimal effects on the overall performance of the chain. But there are still N mixers that should be designed for a good dynamic range to cope with large blockers. The distribution of the LO signal is another challenge because a symmetric LO distribution network is necessary to provide identical phases for all mixers. Due to the loss of transmission lines in the LO distribution network, additional amplifiers might be needed to restore the signal level which adds to the power dissipation of the entire system

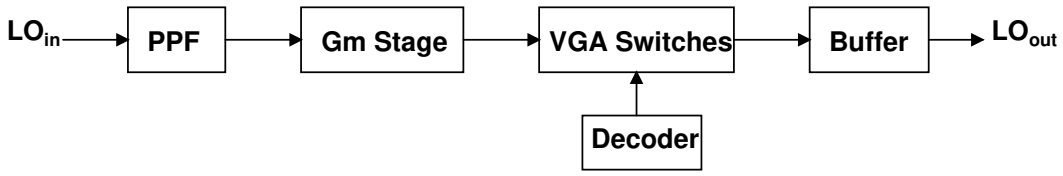


Figure 3.1: Block Diagram of Phase Shifter Architecture.

The architecture of 5 bit Phase Shifter is shown in Figure 3.1. At the beginning, it uses PPF to generate quadrature LO signals from single Local Oscillator. However, the large insertion loss introduced by the PPF makes the phase shifter presented a low gain. These quadrature voltage signal are then converted to current signal by Gm MOSFET's. The phase shifter is designed to achieve a full-360° phase shift and the VGA/Switches are controlled by the Digital Decoder to achieve the same. The VGA switches takes the quadrature current signal as input and combines them in an appropriate manner to

achieve the desired phase shift. An additional benefit that comes with the switch is that as an amplifier, it also compensates part of the loss caused by the PPF. These quadrature signals are then passed through the output buffer (differential common source amplifier) to drive the mixer switches and also provides an appropriate gain to achieve the full swing of LO signals.

3.1 Polyphase Filter (PPF)

As bandwidth is an expensive resource, most of the millimeter- wave transceivers make use of quadrature radio architectures so that both sides of the spectra can be used for information. The most common tehcnique to generate quadrature signals is to use Polyphase Filter (PPF). A PPF consists of a passive RC structure, which is used for differential quadrature generation. It can easily be cascaded to generate broadband quadrature signals. It can also be used as a complex filter, but the focus in this brief is on quadrature generation. We will use single LO Oscillator followed by PPF to generate quadrature LO signals.

Signal loss and influence of parasitics are two important aspects concerning PPF's at millimeter-wave frequencies [20].

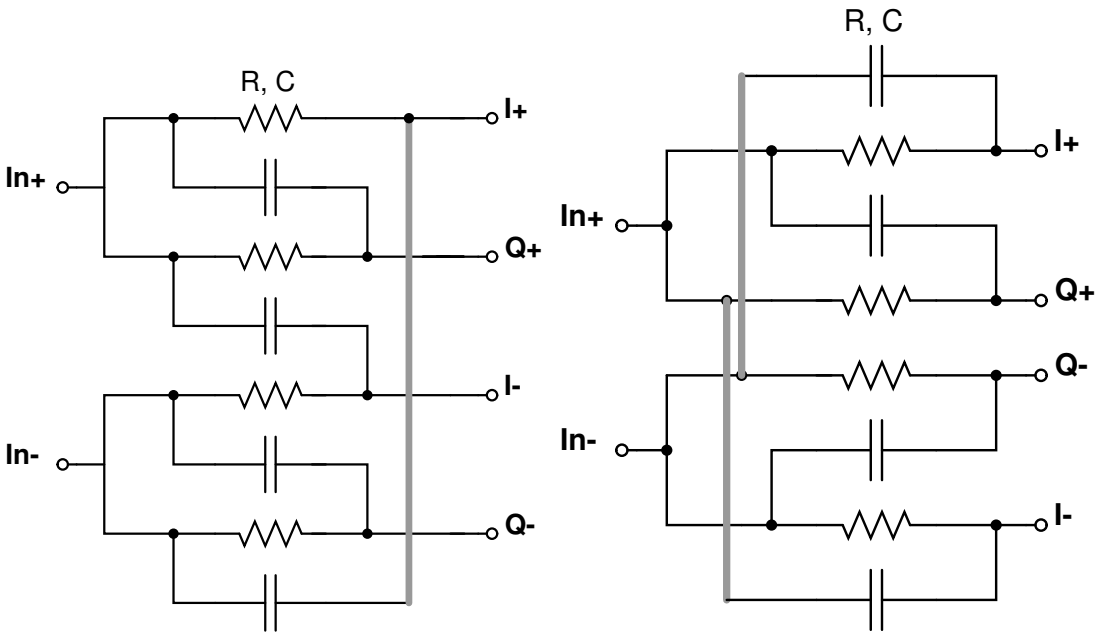
3.1.1 Signal Loss:

Signal loss in the millimeter-wave PPF can go relatively high compared with low-gigahertz applications. It can be relaxed by selecting an optimal input feeding structure and making a compact floor plan to minimize the interconnect length. For an unloaded PPF (as shown in Figure 3.2(b)), the signal loss is $3dB$.

3.1.2 Interconnect Parasitics:

In conventional designs, the layout style followed is shown in Figure 3.2(a), which has the highlighted assymetric long interconnect. At millimeter-wave frequencies (such as 60 GHz), long interconnects can have significant inductance. In a conventional layout, the length of the long interconnect is 40μm [see Figure 3.2(a)]. The desired pole is

shifted due to the dominant inductive interconnect along with other parasitic capacitance. To lessen this effect, the proposed implementation is to distribute it on the differential Q inputs, as shown in Figure 3.2(b). By doing so, the length is reduced by 40% and the structure is more symmetrical. In this brief, it will be referred to as form-II. In addition, this structure is more robust than form-I against capacitive parasitics.



((a)) Long Interconnect ((b)) Short Interconnect

Figure 3.2: (a) Conventional and (b) symmetric layouts of the PPF. The long interconnect is highlighted in bold gray.

3.1.3 Implementation and Simulated Results:

The optimal values of R and C are 208Ω and $33fF$ for the pole frequency to be at $26GHz$. Salicided p+ resistors and interdigitated metal–oxide–metal capacitors are used in the PPF. The size of the salicided resistors are optimized to reduce the impact of mismatch and the associated parasitic capacitance. There exists a tradeoff between matching and resistor cutoff frequency [11]. The size of the capacitors are also chosen to match the aspect ratio of resistors to minimize the routing overhead. Dummy capacitors are used in between two continuous resistors, and dummy resistors are used next to outer capacitors to provide same neighboring environment and to mitigate lithography edge effects. Simulated Voltage loss is $6.5dB$ for a tuned load of 50Ω.

3.2 Principle of Decoder and VGA Switches:

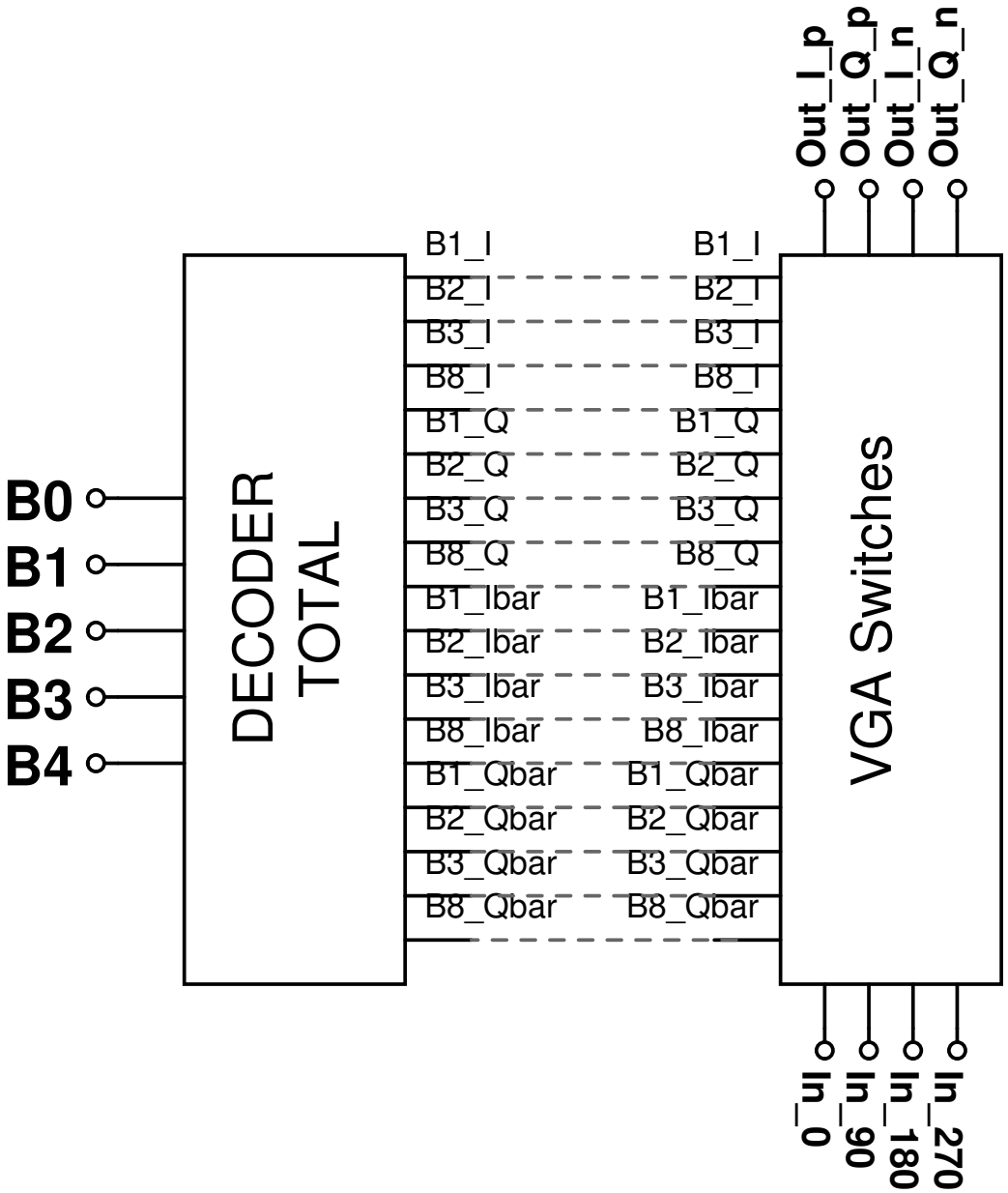


Figure 3.3: Illustration of the Phase Shifter Architecture

In this work, the phase shifter has a phase resolution of $11.25°$ (5-bit resolution) and a phase control range of 360°. The LSB bits (B2, B1, B0) are used to provide $8(2^3)$ discrete phase states within a single quadrant and the MSB bits (B4, B3) are used to select one out of the $4(2^2)$ quadrants. The single output signal is the combination of all four input quadrature signals weighted appropriately to achieve the desired phase shift. The weights A_I (assigned to inphase signal) and A_Q (assigned to Quadrature signal) are

calculated as per the equations below:

$$\tan\phi = \frac{A_Q}{A_I} \tag{3.1}$$

and

$$A = \sqrt{A_I^2 + A_Q^2} \tag{3.2}$$

where ϕ is the desired phase shift and A is the magnitude of the output signal. We can view it as the inphase signal being scaled by A_I and the quadrature signal by A_Q and both are combined to produce a signal of the desired phase shift. We have to make sure that for any given phase setting the equal number of VGA switches are in ON state so as to provide equal input and output impedance across all phase settings. This ensures that the entire circuit operation does not vary on the basis of phase settings.

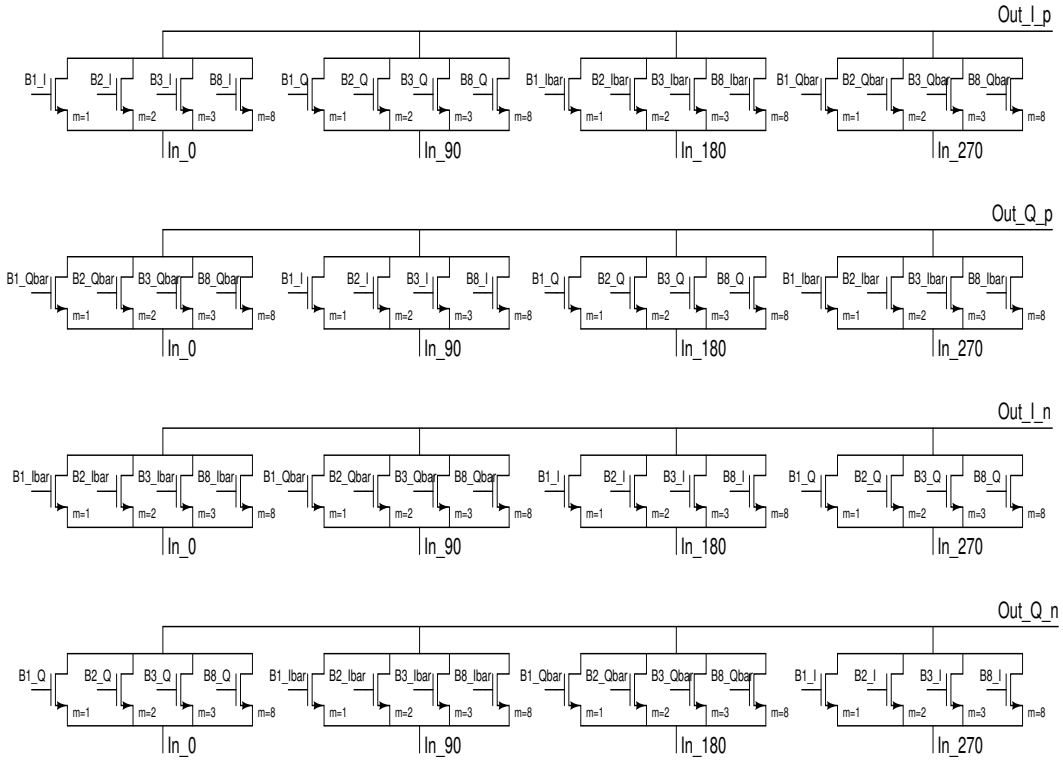


Figure 3.4: VGA Switches.

N_{I+}	N_{Q+}	N_{I-}	N_{Q-}	$Ratio(\frac{A_Q}{A_I})$	$AbsolutePhase(^\circ)$	$Stepwidth$	$Magnitude$
14	3	0	3	$\frac{0}{14}$	0	-	14
14	4	0	2	$\frac{2}{14}$	8.13	8.13	14.14
14	5	1	0	$\frac{5}{13}$	21.05	12.91	13.93
12	8	0	0	$\frac{8}{12}$	33.7	12.65	14.42
10	10	0	0	$\frac{10}{10}$	45.02	11.31	14.14
8	12	0	0	$\frac{12}{8}$	56.34	11.31	14.42
5	14	0	1	$\frac{13}{5}$	69	12.65	13.93
4	14	2	0	$\frac{14}{2}$	81.91	12.91	14.14

Table 3.1: A table showing the appropriate ratios of quadrature to inphase signal to achieve desired Phase shifts.

The Table 3.1 above shows the ratio of the quadrature signal to the inphase signal to generate the desired phase shift within a single quadrant. The same scheme could be extended to the rest of the quadrants as well. These are the best possible ratios to ensure two things: first being the phase shifts should be as close as possible to the ideal values and secondly for any given phase setting equal number of VGA switches are in ON state. Let's try to understand the concept used to arrive at the above table.

As discussed previously, each of the four quadrature output signals are the weighted combination of all four quadrature input signals (as shown in Figure 3.4). Given the above combination of ratios we would require four set of VGA switches with the multiplier in the ratio $1:2:3:8$ for each input signal. Let's try to understand the second row combination which generates the absolute phase shift of 8.13°. Here, $N_{I+} = 14$ implies that all the switches would be in ON state for the input signal In_0. Similarly $N_{Q+} = 4$ implies that the switch with multiplier $m = 3$ and $m = 1$ will be in ON state and rest will be in OFF state and similar conclusions can be made for $N_{I-} = 0$ and $N_{Q-} = 2$. Also note, that $A_Q = N_{Q+} - N_{Q-}$ because of the opposite phases of In_90

and In_270 input signals and similarly $A_I = N_{I+} - N_{I-}$. With these settings, we have

$$\begin{aligned} Out_{Ip} &= \frac{14}{20} * In_0 \quad + \frac{4}{20} * In_{90} + 0 * In_{180} \quad + \frac{2}{20} * In_{270} \\ Out_{Qp} &= \frac{2}{20} * In_0 \quad + \frac{14}{20} * In_{90} + \frac{4}{20} * In_{180} \quad + 0 * In_{270} \\ Out_{In} &= 0 * In_0 \quad + \frac{2}{20} * In_{90} + \frac{14}{20} * In_{180} \quad + \frac{4}{20} * In_{270} \\ Out_{Qn} &= \frac{4}{20} * In_0 \quad + 0 * In_{90} + \frac{2}{20} * In_{180} \quad + \frac{14}{20} * In_{270} \end{aligned} \tag{3.3}$$

From the above Equation 3.3 we can see that all the weights for In_0 adds to value 1 and similar phenomena for other input signals ($In_{90}, In_{180}, In_{270}$) as well. Thus, this method generates the quadrature output signals using unused part from the input signals. Hence, we are not discarding any part of the input signal. Also, notice the weights are rotating in the anticlockwise direction for the input signal combination to generate the respective output signals. Now, these switches are controlled by the Decoder as shown in Figure 3.3 which feeds the 16 controlling signals to the VGA switches block (Figure 3.4).

The Decoder block (Figure 3.5) consists of two main blocks:

A. **Actual Decoder:**

This block generates the controlling signal for the VGA switches using LSB 3 bits ($B0, B1, B2$) which provides 8 discrete phase shifts in a single quadrant. It realises the truth table as shown in the Table 3.2. The below truth table is for the case of first quadrant i.e the MSB bits are $B3 = 0$ and $B4 = 0$.

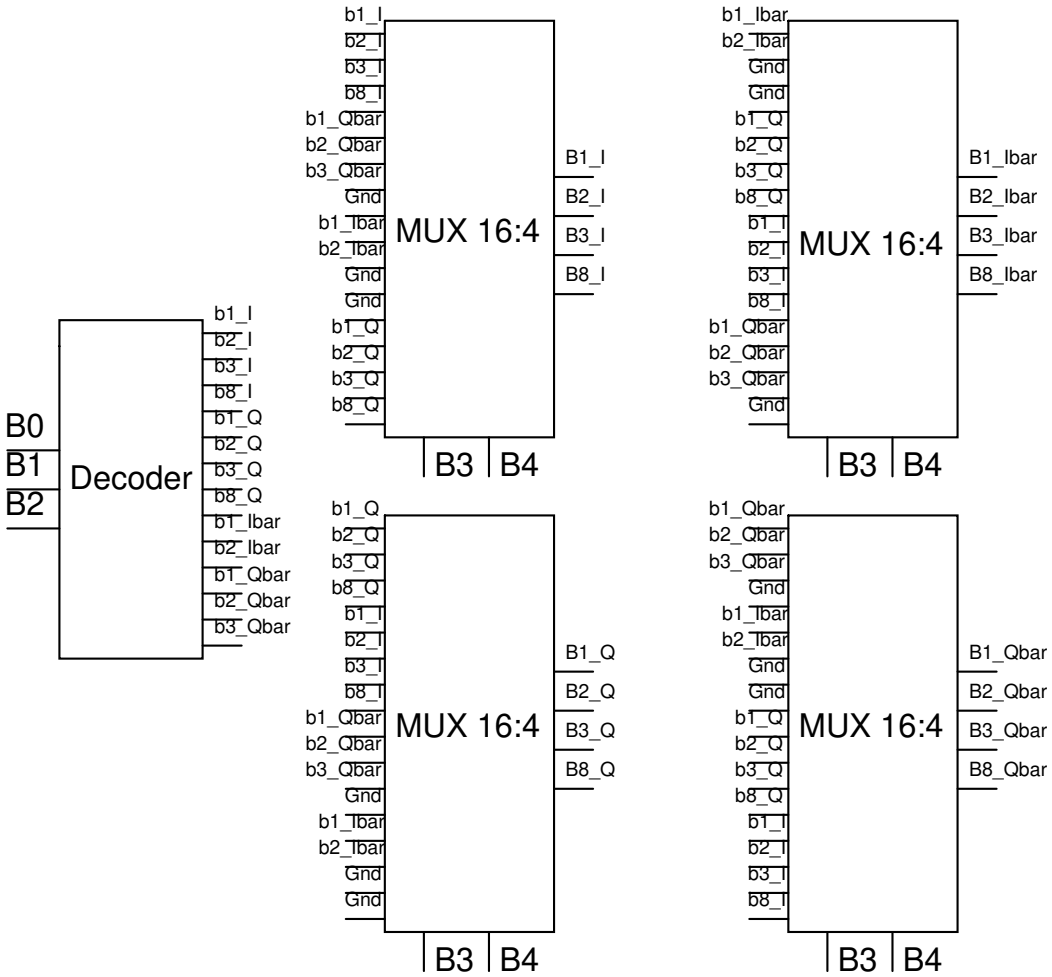


Figure 3.5: Decoder Block which takes five bits input and generates 16 controlling singnals.

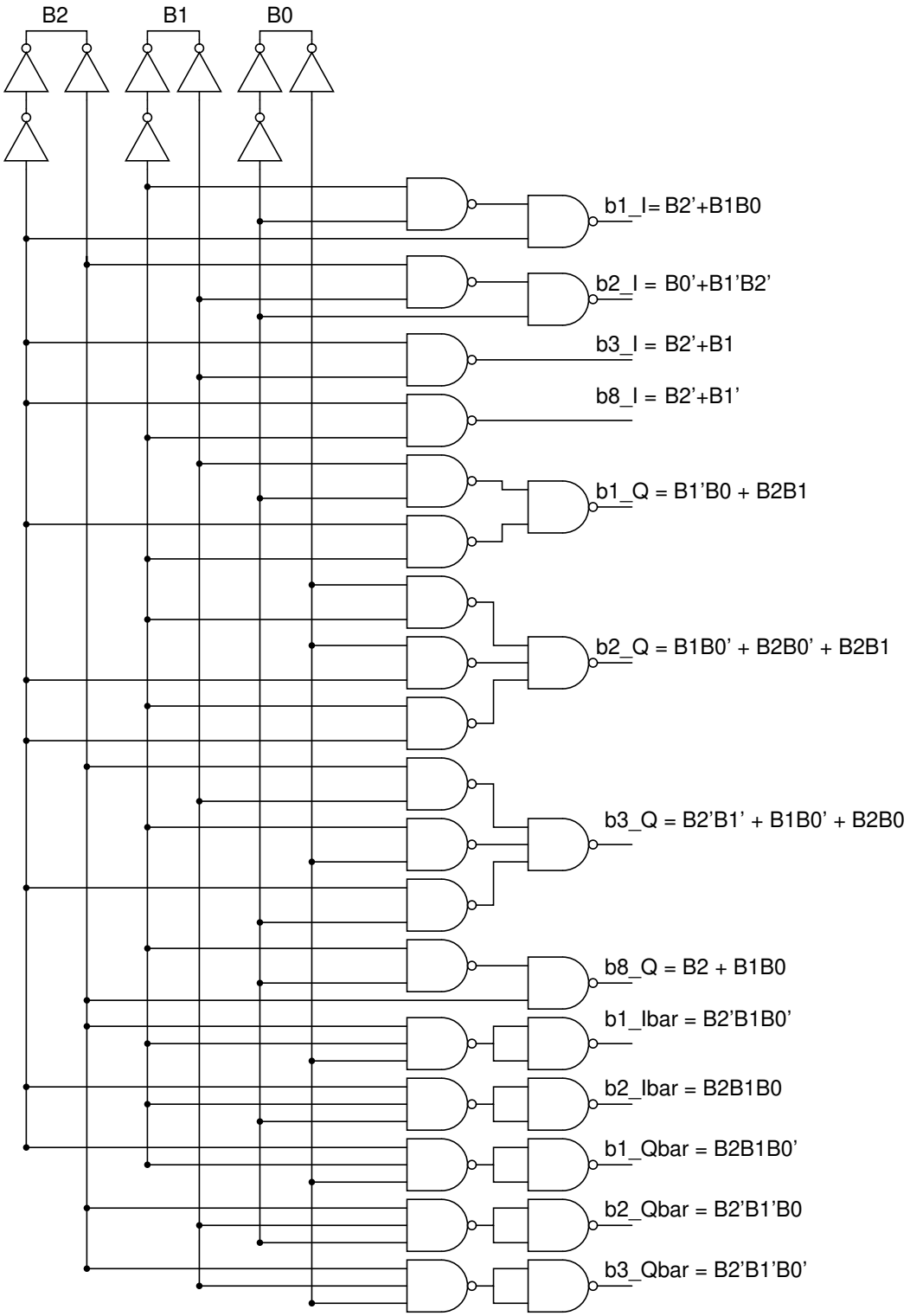


Figure 3.6: Actual Decoder.

		Bits								$Logic$
$B0$		0	1	0	1	0	1	0	1	
$B1$		0	0	1	1	0	0	1	1	
$B0$		0	0	0	0	1	1	1	1	
$Ratio$	$\frac{A_Q}{A_I}$	$\frac{0}{14}$	$\frac{2}{14}$	$\frac{5}{13}$	$\frac{8}{12}$	$\frac{10}{10}$	$\frac{12}{8}$	$\frac{13}{5}$	$\frac{14}{2}$	
$Phase(°)$		0	8.13	21.05	33.7	45.02	56.34	69	81.91	
I	$B1\_I$	1	1	1	1	0	0	0	1	$B2' + B1B0$
	$B2\_I$	1	1	1	0	1	0	1	0	$B0' + B1'B2'$
	$B3\_I$	1	1	1	1	0	0	1	1	$B2' + B1$
	$B8\_I$	1	1	1	1	1	1	0	0	$B2' + B1'$
Q	$B1\_Q$	0	1	0	0	0	1	1	1	$B1'B0 + B2B1$
	$B2\_Q$	0	0	1	0	1	0	1	1	$B1B0' + B2B0' + B1B2$
	$B3\_Q$	1	1	1	0	0	1	1	1	$B2'B1' + B1B0' + B2B0$
	$B8\_Q$	0	0	0	1	1	1	1	1	$B2 + B1B0$
Ibar	$B1\_Ibar$	0	0	1	0	0	0	0	0	$B2'B1B0'$
	$B2\_Ibar$	0	0	0	0	0	0	0	1	$B2B1B0$
	$B3\_Ibar$	0	0	0	0	0	0	0	0	0
	$B8\_Ibar$	0	0	0	0	0	0	0	0	0
Qbar	$B1\_Qbar$	0	0	0	0	0	0	1	0	$B2'B1B0'$
	$B2\_Qbar$	0	1	0	0	0	0	0	0	$B2'B1'B0$
	$B3\_Qbar$	1	0	0	0	0	0	0	0	$B2'B1'B0'$
	$B8\_Qbar$	0	0	0	0	0	0	0	0	0

Table 3.2: Truth Table to generate the controlling signals using LSB three bits for phase settings in first quadrant (B3 = 0, B4 = 0)

Now, for second quadrant (when $B3 = 1$ and $B4 = 0$) we have to rotate the controlling signals going into the VGA as shown in the table below (this is for the generation of the single inphase output Out_I_p (refer Figure 3.4)

$B4$	$B3$	$Quadrant$	In_0	In_90	In_180	In_270
0	0	1^{st}	I	Q	$Ibar$	$Qbar$
0	1	2^{nd}	$Qbar$	I	Q	$Ibar$
1	0	3^{rd}	$Ibar$	$Qbar$	I	Q
1	1	4^{th}	Q	$Ibar$	$Qbar$	I

Table 3.3: A table showing the controlling signals given to input signals in rotating manner to cover all four quadrants for the output signal

The above Table 3.3 is realised using the second block of the Decoder:

B. **MUX(16:4)** We are using four $16 : 4$ MUX in order to generate appropriate controlling signals for each of the input signals ($In\_0, In\_90, In\_180, In\_270$) of VGA Switches to cover entire $360°$ of phase shift range. Each block (as shown in Figure 3.5) takes the input as 16 (four combination) controlling signals from the actual decoder block and based on the values of $B3$ and $B4$ chooses one of the four combination as the output signal. The internal of the block (MUX 16:4) contains four $4 : 1$ MUXes (as shown in Figure 3.7).

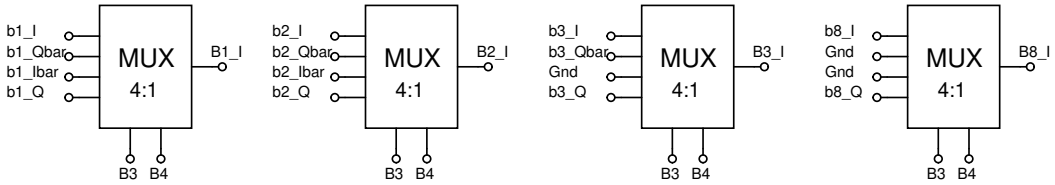


Figure 3.7: MUX 16:4

3.3 Understanding the Phase Shifter Scheme with an example:

Let's consider the generation of the output (Out_I_p) as shown in Figure 3.4 (refer to the first row of switches which are used in generation of the output Out_I_p) with a phase shift of $8.13°$. Now the ratio of quadrature signal to inphase signal required to generate this phase shift is ($\frac{2}{14}$) as shown in the Table 3.1. We have $N_{I+} = 14$ implying we want all the switches corresponding to the input signal (In_0) to be in ON state. For $N_{Q+} = 4$ we want the switches with weights $m = 3$ and $m = 1$ are in ON state and rest are in OFF state for input signal (In_90). For $N_{I-} = 0$ we want all the switches corresponding to input signal (In_180) to be in OFF state. For $N_{Q-} = 2$ we want the switch with weight $m = 2$ to be in ON state and rest in OFF state for input signal (In_270). Now to achieve this action decoder has to generate appropriate controlling signals ($B1\_I, B2\_I, B3\_I, B8\_I, B1\_Q, etc...$).

Let's now understand the decoder action. First thing is that the phase shift lies in the first quadrant so $B3 = 0$ and $B4 = 0$ and for the given phase shift value $B2 = 0, B1 = 0, B0 = 1$. Decoder takes this five bits as an input. The LSB three bits are taken by the actual decoder (shown in Figure 3.6) to generate the required controlling

signal as per table 3.2. The MSB two bits are taken by the MUX blocks to generate the final controlling signals (in this case it follows the row corresponding to 1^{st} quadrant in the table 3.3). These generated signals are then fed to the VGA block to achieve the required action.

Just as we discussed how the phase shifted output Out_I_p is generated, its differential and quadrature counterparts (Out_I_n, Out_Q_p, Out_Q_n) are generated in similar fashion with the controlling signals being rotated in an anticlockwise direction as going down in the Figure 3.4.

3.4 Generation of Phase Shifted LO Signals:

The LO signals are generated using two stage architecture:

1. Quadrature Phase shifted signal generation using single oscillator (LO Stage1)
2. Buffer to drive mixer switches and provide appropriate Gain (LO Stage2)

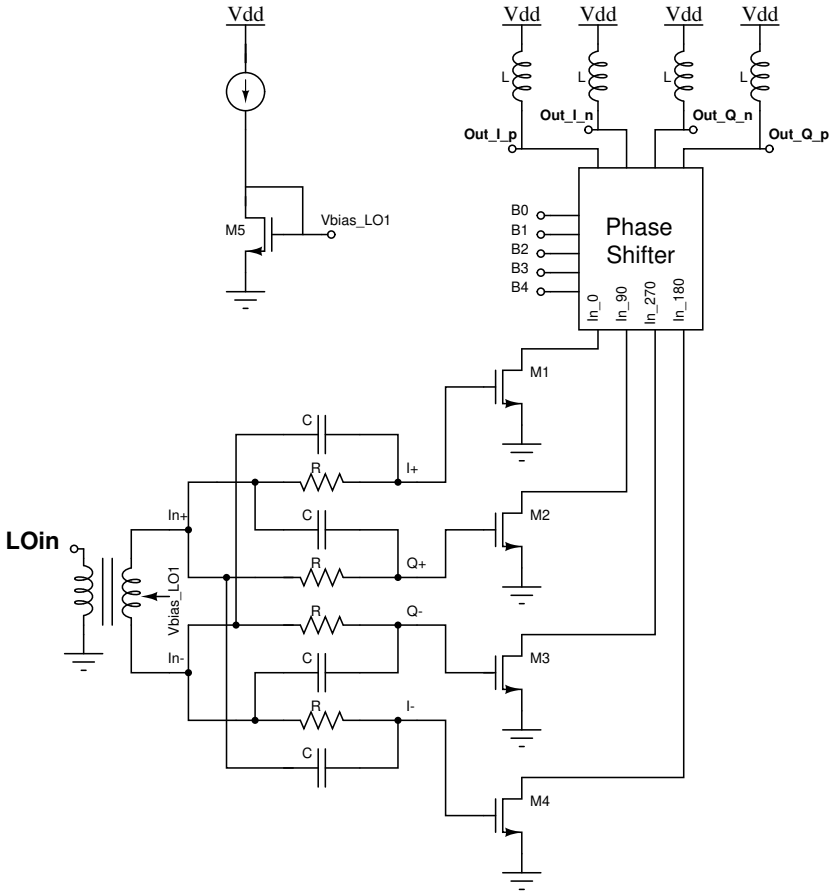


Figure 3.8: LO Stage1

As seen from Figure 3.8, a single sinusoidal input LO_{in} from the oscillator is fed into the Balun which generates the differential output voltages In_+ and In_-. These differential voltages are given as an input to PPF Block which generates the output as both differential inphase and differential Quadrature voltage signals. These four voltages are then given at the gate of the Gm-Mosfet to convert them into current signal and then pass it through the Phase Shifter. The current signals pass through the VGA switches (Figure3.4) where they are scaled appropriately and combined in a fashion to generate the required phase shift. These phase shifted current signals then pass through the inductor to produce phase shifted output voltages (Out_I_p, Out_I_n, Out_Q_p, Out_Q_n).

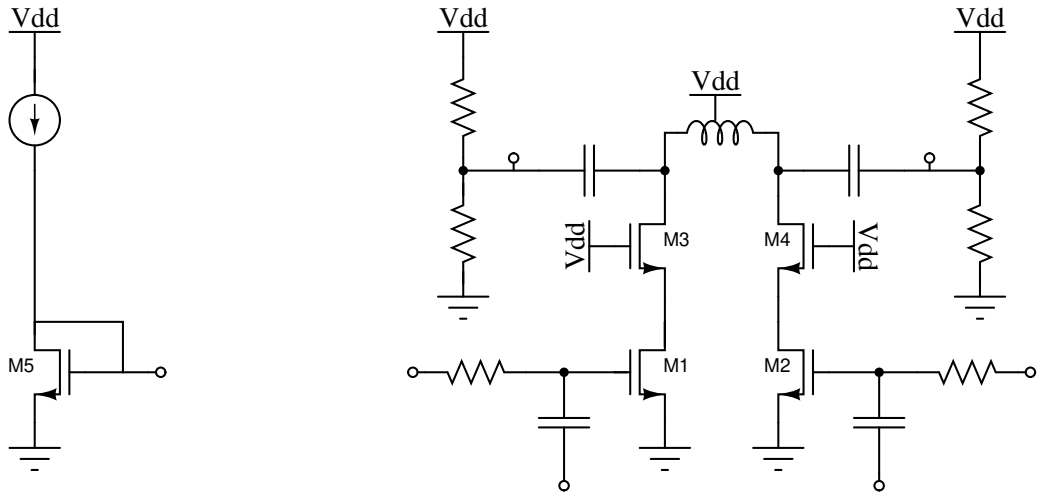


Figure 3.9: LO Stage2

The LO Stage2 block is basically a differential common source amplifier (cascoded structure) as seen from Figure 3.9. Two such amplifiers are used, one for inphase signals and other for quadrature signals. The output from the stage one is fed as an input to stage two.

3.5 Results and Plots:

In the plots below, k represents the total number of phase settings. In our case for 5-bit resolution we can have $32(2^5)$ total combinations, so $k \in [0, 32]$.

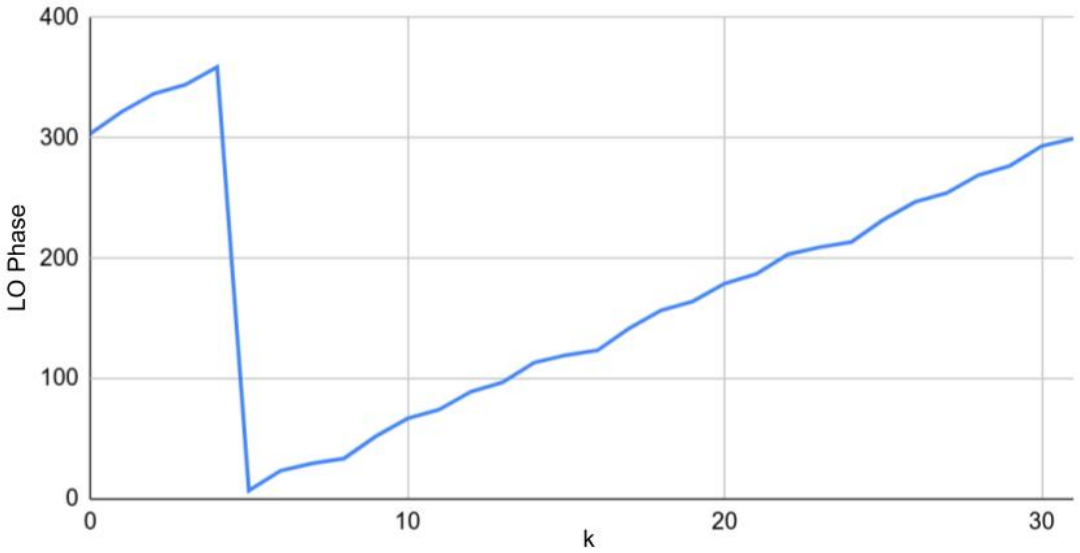


Figure 3.10: LO Phase Linearly changing with phase settings

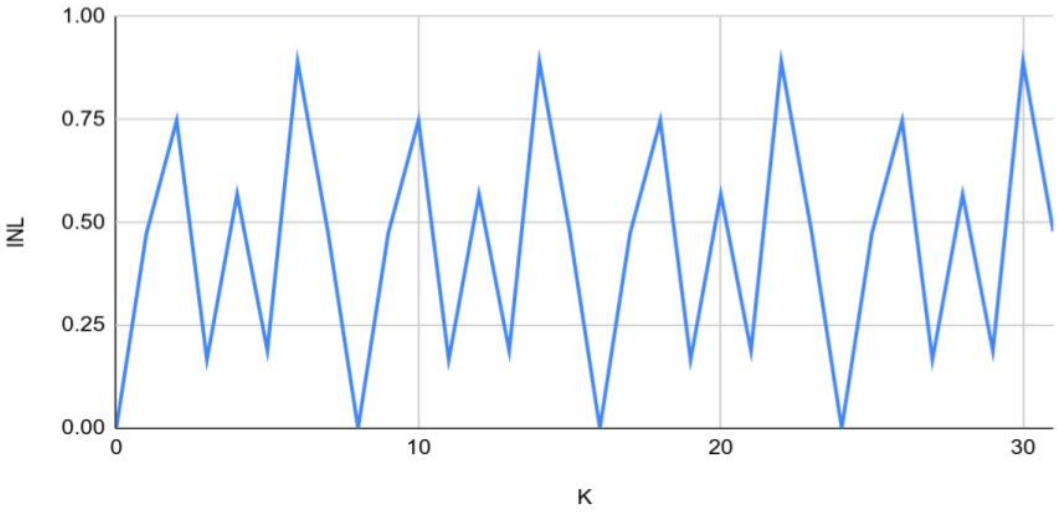


Figure 3.11: Integrated Non-Linearity

As seen form the Figure 3.11, the INL of the Phase Shifter is within $1LSB$.

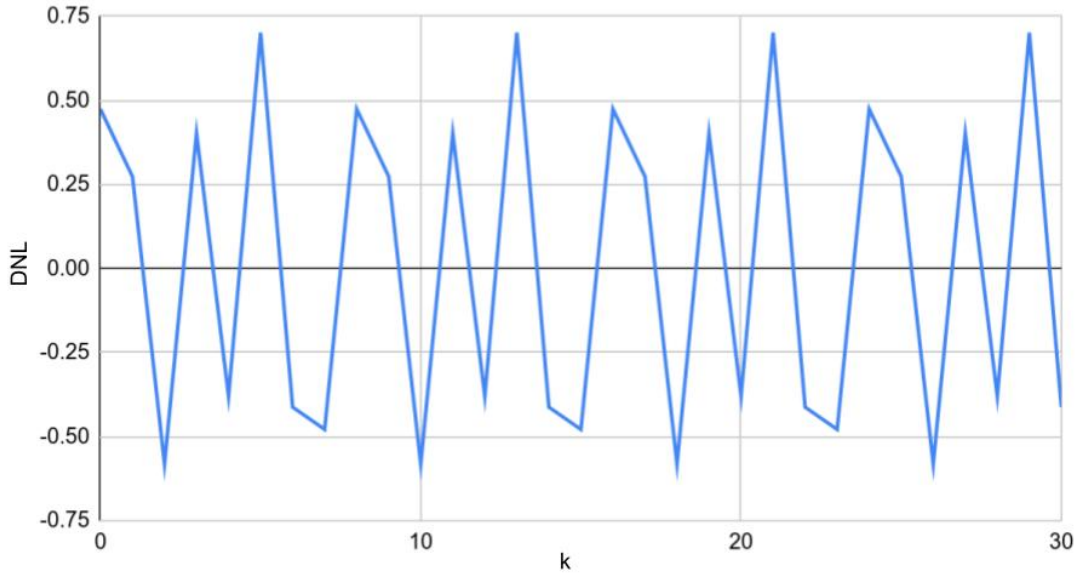


Figure 3.12: Differential Non-Linearity

CHAPTER 4

Proposed Single Stage Reciever

mmWave 5G architectures require multiple RF channels to meet the diversity and link budget requirements. Multi-antenna RF front-ends also allow for massive-MIMO and beamforming. We attempt a single-channel receiver block that can be easily integrated into such designs. We consider the requirements of a mobile station receiver, which has the added constrains of area and power so that the entire array of such receivers can be accommodated on the chip.

To accomplish this, we decide to adopt the single-stage topology, wherein low-noise amplification, down-conversion, and filtering are achieved in a single stage, reducing the area occupied. Such a topology can be realized using current-reuse techniques, which have the added benefit of lower power consumption. A receiver employing current-reuse between multiple stages would require a stacked implementation, which would result in voltage headroom issues. The single-stage receiver topology alleviates this issue by implementing the functionality of multiple stages onto a single stage by isolating these functions in the frequency domain.

The single-stage topology has since been substantially modified and improved upon for various specialized requirements such as multi-band cellular receivers [3], high dynamic-range and low-noise applications [6]. Since this topology uses the same devices for both baseband and RF functions, each stage's design is not independent of the other stages. There is an inherent trade-off between the performance specifications when the RF or baseband functions are optimized. We present a modified single-stage receiver topology that decouples some of these design aspects to allow for more straightforward optimization.

The proposed single stage receiver is as shown in Figure 4.1.

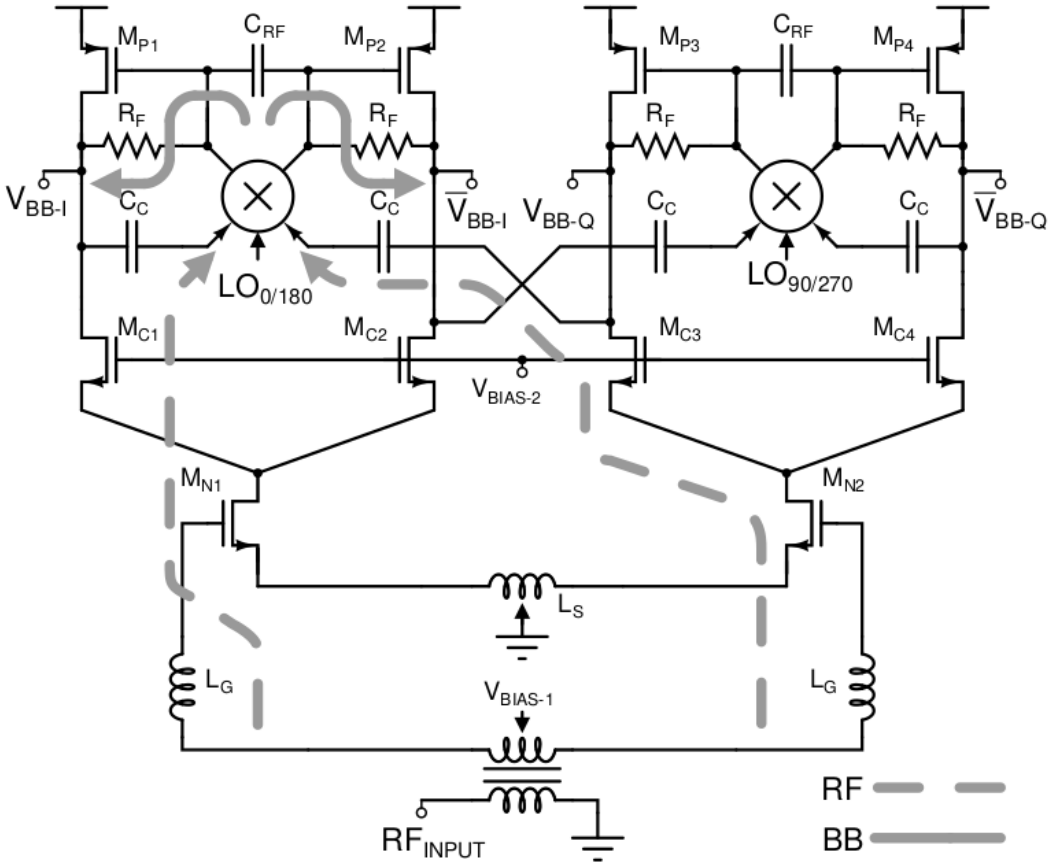


Figure 4.1: Proposed single-stage receiver implementation.

We note that the parasitic capacitances added by the MOSFETs significantly degrade the performance at mmWave frequencies. Due to the lower mobility of holes in PMOS devices, the trans-impedance amplifier devices will need to be sized larger than 20the NMOS cascode devices. This would result in the RF current at the baseband output node being shunted to ground through the parasitic capacitances instead of flowing into the passive current-mode mixer. This issue is alleviated by adding a series inductor to present a higher impedance at RF frequencies (Fig. 4.2).

4.1 Circuit Analysis:

Estimation of the gain and dominant noise contributions in the circuit are presented here. For the purpose of analysis, only the gate-source capacitance of $M_{N-1,2}$ and $M_{P-1,2,3,4}$ are considered. The input matching condition $R_S = \omega_T \times L_S$ is assumed to be satisfied. Analysis for the in-phase and quadrature-phases are identical, and hence

the subscripts I and Q are dropped.

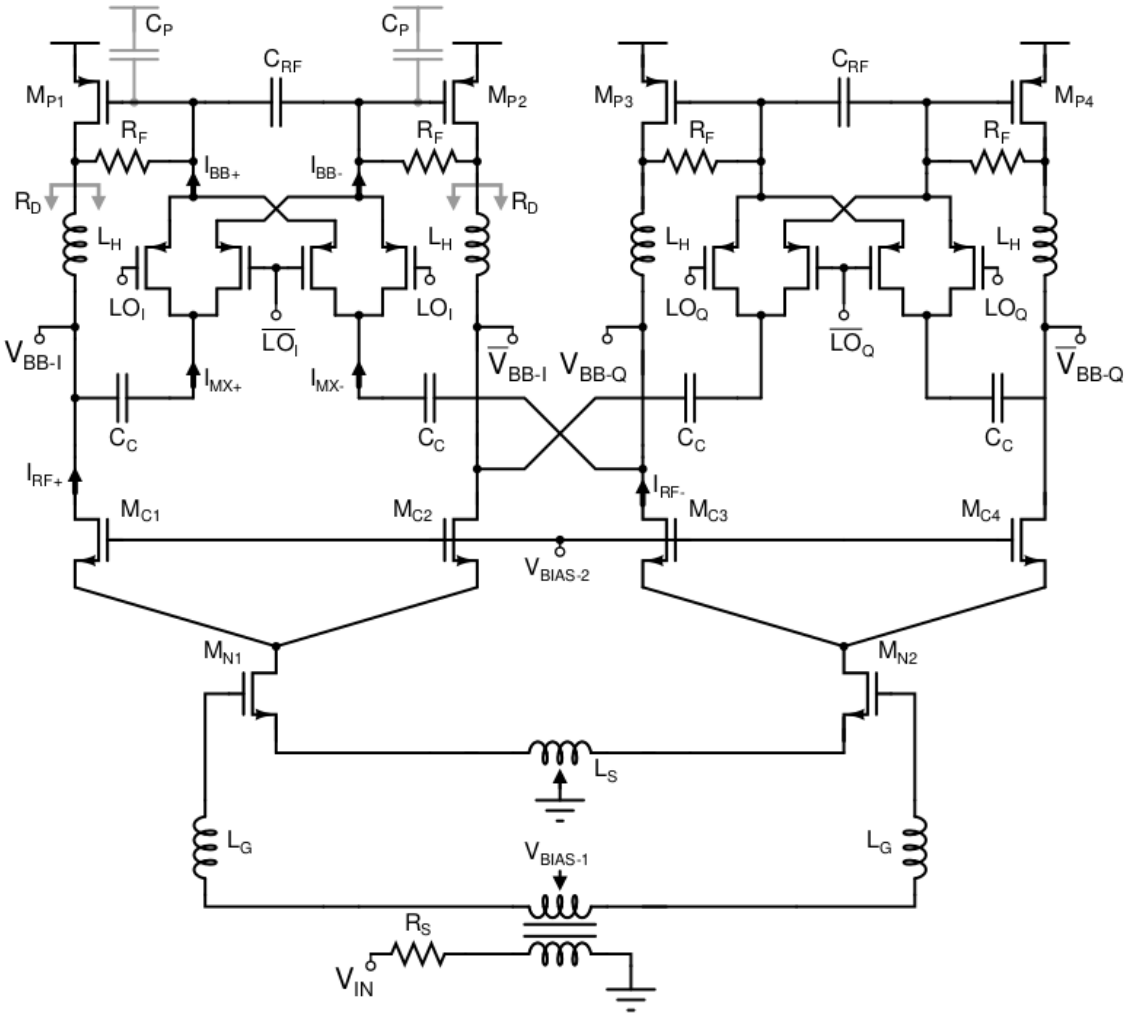


Figure 4.2: Schematic diagram of the proposed single-stage receiver.

4.1.1 Gain Analysis:

Traversing the signal flow path, the LNA first amplifies the input RF signal into an RF current. Its trans-conductance gain is

$$\frac{I_{RF}^{+} - I_{RF}^{-}}{V_{IN}} = \sqrt{2} \times Q \times (\frac{g_{MN}}{2}) \tag{4.1}$$

with terms corresponding to the balun, input matching and input trans-conductor respectively. This current then gets divided between the high impedance looking into the inductor L_H and the input impedance of the mixer. Assuming the capacitor C_{RF} to be a short circuit, the differential impedance looking into the inductor is

$$Z_{L,RF}(j\omega) = 2 \times (j\omega L_H + (R_F || r_{o-P})) \tag{4.2}$$

while the differential impedance looking into the mixer at frequency (ω + $k\omega_{LO}$) near $k\omega_{LO}$ is

$$Z_{IN,MZ}(\omega + k\omega_{LO}) = \left(\frac{8}{\pi^2 k^2}\right) \times Z_{TIA}(j\omega) \qquad \forall\, Odd\ k \tag{4.3}$$

which is proportional to the up-converted low baseband input impedance of the trans-impedance amplifier,

$$Z_{TIA}(j\omega) \approx \left(\frac{R_D + R_F}{1 + g_{MP} R_D}\right)\left(\frac{1}{1 + j\omega/\omega_{BW}}\right) \tag{4.4}$$

where the baseband bandwidth is

$$\omega_{BW} \approx \frac{1 + g_{MP} R_D}{(R_D + R_F) \times (C_P + 2C_{RF})} \approx \frac{g_{MP}}{C_P + 2C_{RF}} \tag{4.5}$$

This RF current that flows into the mixer is then down-converted, with a current transfer function from an input at frequency (ω + $k\omega_{LO}$) near $k\omega_{LO}$ to an output at frequency ω given by

$$\frac{(I^+_{BB} - I^-_{BB})|_{\omega}}{(I^+_{MX} - I^-_{MX})|_{\omega + k\omega}} = \frac{2}{\pi k} \qquad \forall\, Odd\ k \tag{4.6}$$

Now, this baseband current is converted to the output voltage by the trans-impedance amplifier with a trans-impedance gain of

$$R_{TIA} \approx \left(\frac{(g_{MP} R_F - 1) \times R_D}{1 + g_{MP} R_D}\right)\left(\frac{1}{1 + j\omega/\omega_{BW}}\right) \approx \frac{R_F}{1 + j\omega/\omega_{BW}} \tag{4.7}$$

The trans-impedance amplifier also embeds first-order filtering, which can be tuned by changing ω_{BW}

The total conversion gain of the receiver is

$$\frac{V^+_{BB} - V^-_{BB}}{V_{IN}} \approx \frac{\sqrt{2} \times Q}{\pi} \frac{g_{MN} R_F}{1 + j\omega/\omega_{BW}} \tag{4.8}$$

4.1.2 Noise Analysis:

Only the noise contribution of the active MOSFETs is considered here for analysis. There are multiple pathways in which device noise can interfere with the signal, and these are analyzed individually. We consider 3 different pathways: direct RF noise, folded RF noise, and baseband noise.

Direct Noise

We denote the noise added directly onto the RF signal at the frequency band of interest as direct RF noise. This is the in-band RF noise added by the input trans-conductor and cascode devices.

The noise of MOSFET M N-1,2 is from a single independent noise source, which then gets divided into two paths

$$\begin{aligned}(I_{RF}^{+} - I_{RF}^{-}) &= 2 \times 4k_BT\gamma g_{MN} \times \frac{1}{4} \times \frac{1}{4} \\ &= 4k_BT\gamma g_{MN} \times \frac{1}{8}\end{aligned} \tag{4.9}$$

the noise due to the cascode devices can be shown to be

$$\begin{aligned}(I_{RF}^{+} - I_{RF}^{-}) &= 4 \times 4k_BT\gamma g_{MC} \times \frac{1}{4} \\ &= 4k_BT\gamma g_{MC}\end{aligned} \tag{4.10}$$

Folded RF Noise

The mixer folds noise from higher harmonics into the signal band. However, the mixer gain from higher harmonics to the output baseband frequency decreases with an increase in the harmonic number, as described in (4.6). The degeneration by L_S , results in different noise densities for each harmonic.

$$\begin{aligned}(I_{RF}^{+} - I_{RF}^{-})|_{k\omega_{LO}} &= 2 \times 4k_BT\gamma g_{MN} \times \frac{1}{4} \\ &\times \frac{(1-k^2)^2 + k^2\beta^2}{(1-k^2)^2 + 4k^2\beta^2} \qquad \forall\, Odd\ k\end{aligned} \tag{4.11}$$

where

$$\beta = \left(\frac{\omega_T}{\omega_{LO}}\right)\left(\frac{L_S}{L_S + L_G}\right) \tag{4.12}$$

(4.9) is a special case of the above equation. The addition of the cascode noise at higher

frequencies is the same as (4.10)

Baseband Noise

The input signal after down-conversion flows through the trans-impedance amplifier, which is also a part of the single-stage receiver. Hence, the baseband noise of the devices also adds to the total output noise of the receiver. We note that $C_R F$ and C_C are designed to behave as an open circuit for baseband frequencies, presenting a low impedance looking into L_D and preventing baseband signal or noise from flowing into the mixer respectively.

The baseband noise from the input trans-conductor appears as common-mode noise for the proposed receiver, and hence does not appear at the differential baseband output. However, it suffer from the noise of the cascode devices.

$$\begin{aligned}(V_{BB}^{+} - V_{BB}^{-}) &= 2 \times 4k_B T\gamma g_{MC} \times \left(\frac{1}{g_{MP}}\right)^2 \\ &= 8k_B T\gamma g_{MC} \times \left(\frac{1}{g_{MP}}\right)^2\end{aligned} \tag{4.13}$$

4.1.3 Linearity Considerations:

The single-stage receiver topology implements current reuse without the stacking of stages, alleviating voltage headroom issues. However, the presence of 3 MOSFETs in the stack limits the topology's performance with scaling in the supply voltage.

Assuming a large gain, the linearity of this topology is limited by the biasing of the cascode MOSFETs. The drain of the cascode device, which is the baseband output node, is biased by the diode-connected PMOS of the trans-impedance amplifier. There is flexibility in choosing the gate voltage of the cascode device.

From the previous section, we note that a lower g M C improves noise performance. This can be achieved by increasing the overdrive of the cascode MOSFETs, resulting in a larger gate voltage of the cascode device. However, this will push the cascode device closer into the linear region, worsening the linearity performance.

This trade-off between noise and linearity can be optimized by changing the cascode gate bias voltage to get optimal performance for different receiver input signal levels.

4.2 Potential Adaptations of the Proposed Topology

4.2.1 Integration with the proposed Phase-Shifting scheme

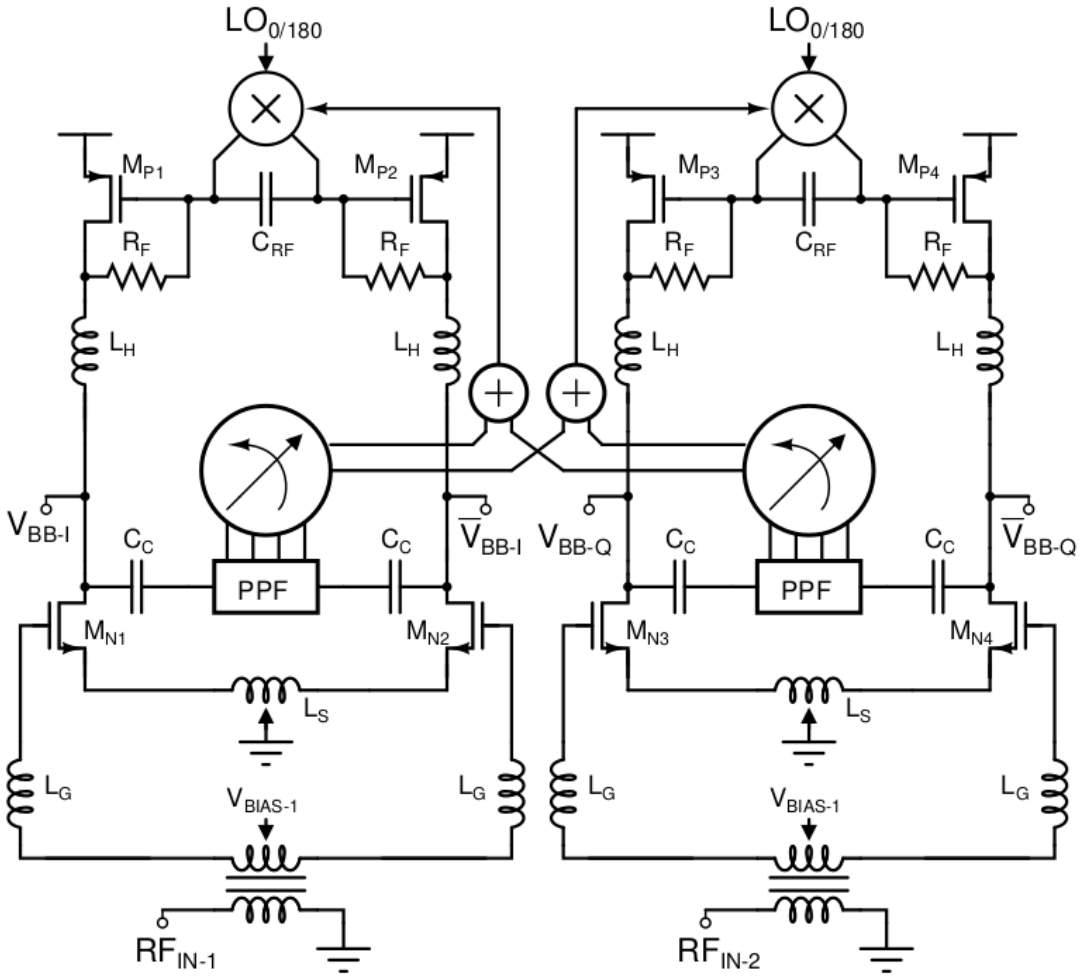


Figure 4.3: 2-Channel implementation of the proposed phase-shifting architecture using the single-stage receiver topology.

Fig. 4.3 depicts a 2-channel phased-array implementation using the proposed integrated phase-shifting scheme and the single-stage topology. We note that in the single-channel implementation, inductors L_H were the components that dominated the area. The 2-channel implementation, which still has the same number of L_H inductors, has only a moderate area increase compared to the single-channel implementation, substantiating the area-effectiveness of this implementation.

But the main issue with this design is that the PPF and the Phase Shifter is in the RF

Path. Since PPF has huge insertion loss in loaded condition, it creates a huge signal loss and hence affects the Noise Figure of the entire receiver chain. Hence, we implemented LO path Phase shifting in this brief.

CHAPTER 5

OPTIMIZED SINGLE-STAGE RECEIVER IMPLEMENTATION DETAILS

To validate the working of the optimized single-stage receiver topology, we have designed a 26GHz single-channel receiver on 65nm bulk CMOS process. The primary design considerations and details are presented in this chapter.

5.1 Technology Considerations

We have used commercially available GP flavor of the 65nm bulk CMOS process from TSMC for our design. It can support a supply voltage of 1.2V, has one poly layer, nine copper metal routing layers, and one aluminium redistribution layer. While the process design kit (PDK) has a separate set of RF components for active and passive devices, careful layout considerations were given for the actives, and EM simulations using EMX were run to validate the performance of passives at mmWave frequencies.

One of the challenges in mmWave designs is the rapid deterioration of performance in a poorly designed layout. For mmWave designs, the extracted layout simulation results can be potentially very different compared to the schematic results, adding to the complexity of the design. Several layout techniques suitable for mmWave designs have been documented in literature [13] to get the optimal performance from the process. The problem of discrepancy between layout and schematic is usually resolved through iterations, manual parameter modeling, or by using characterized cells.

To see the degradation from schematic to layout, the transit frequency is plotted from the schematic and extracted layout simulations for different MOSFETs from the PDK. Here, the base PDK layout without any additional routing is used for the extracted layout simulation. As seen in Fig. 5.1, the F T of the baseband device can vary by as much as 20% by just running an extracted layout simulation with the base layout. Wenote that in schematic simulations, the baseband MOSFETs have better F T than RF

MOSFETs, but this relation is reversed in the extracted layout simulation. However, the RF MOSFETS were well characterized in the process, as the schematic and extracted base layout simulations exactly match.

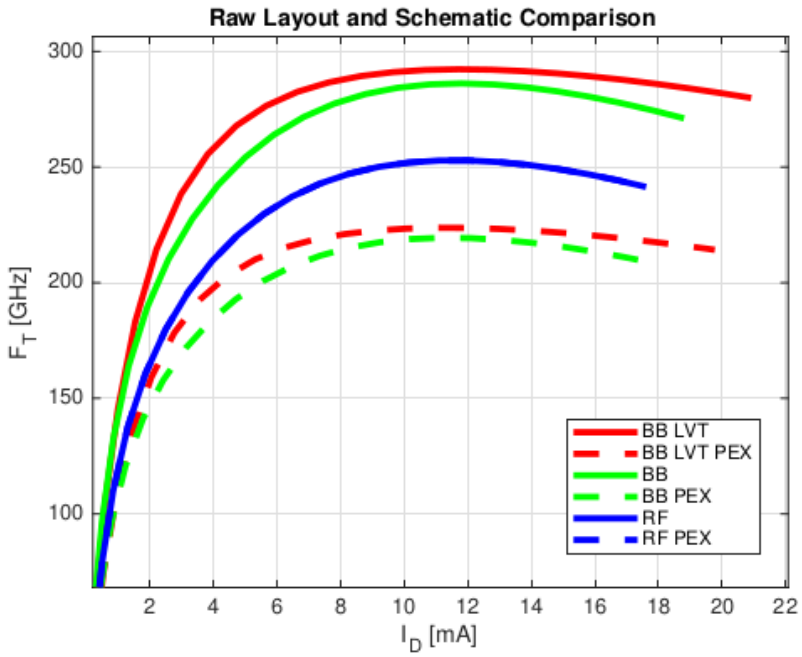


Figure 5.1: F_T comparison for the extracted base layout and schematic.

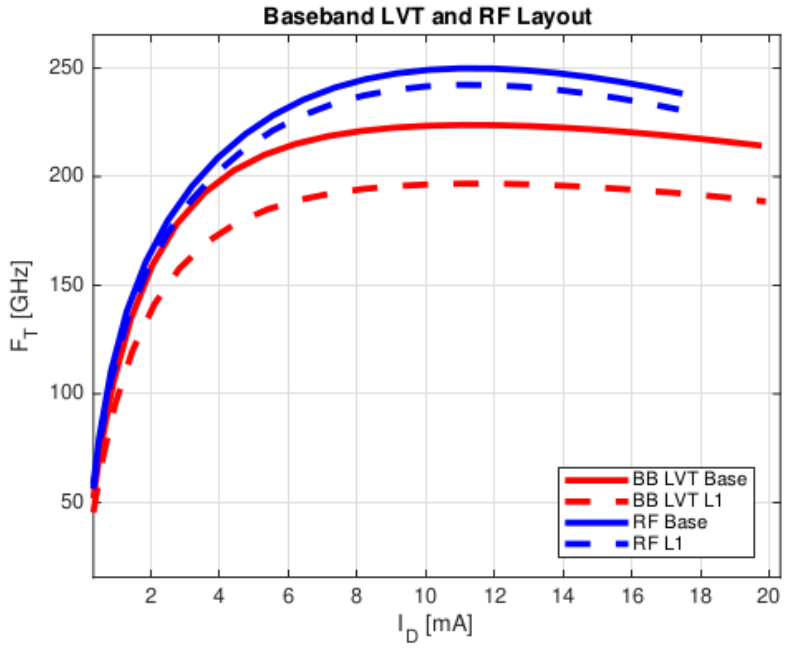


Figure 5.2: F_T comparison for the extracted base layout and layout routed to higher metal layers.

The extracted layout performance of different MOSFETs from the PDK was compared to get the optimal performance from the process. All of the layouts were routed to the same metal layer, with different layout styles optimizing between routing resistance and capacitance. Simulation results showed that the RF MOSFETs without the deep-nwell (DNW) had the highest transit frequency (Fig. 5.2). We note that the base layout of the RF MOSFETs in the PDK is routed to higher metal layers and characterized. Simulation results show only a nominal degradation in performance after further routing. Hence, the schematic of RF MOSFETs in the chosen process was directly used for mmWave designs without extra modeling or characterization.

5.2 Receiver Considerations

The single-stage receiver contains the LNA, mixer, and filter of a standard implementation all sharing the same bias current. Hence, the design and optimization of this receiver topology involved ensuring that each component of the receiver was properly biased and functioning according to specifications.

An inductively degenerated common-source stage with a balun and a center-tapped source inductor was used for the input matching circuit. The inductor to resonate out the gate capacitance was realized through the routing lines. To improve the gain and noise performance, a secondary-tapped balun was used to bias the input of the LNA, as opposed to using an AC coupling capacitor and biasing resistor.

The LNA and trans-impedance amplifier were designed to meet the gain and bandwidth specifications, as described in equation (4.8) and Section 4.1.2. The cascode devices were designed for a balance between linearity and noise, as discussed in Section 4.1.3. The passive current-mode mixer was biased close to the supply voltage, resulting in PMOS switching device performing better than an NMOS device.

The layout was designed so that there was symmetry between the differential sections of the circuit as well as the IQ sections to reduce the effects of mismatch.

5.3 Peripheral Circuitry

The output of the receiver was supplemented by an output buffer to drive the 50Ω load. This was implemented as a standard 2-stage opamp in a voltage follower configu- ration. The large-sized MOSFETs in the second-stage required for driving the resistive load led to a larger capacitance at the input of the second stage. This compensated the opamp without the need for any compensation technique.

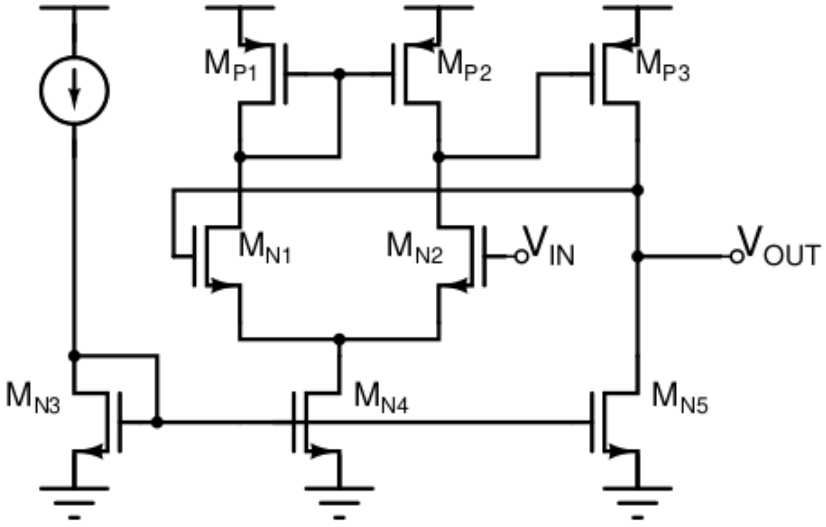


Figure 5.3: Output Driver implementation.

Three supply domains were created, one each for the receiver, LO buffer, and output driver. Each domain had its own decoupling capacitance to ensure a steady supply voltage. The bond-pads were chosen to isolate the three supply lines, but share the ground across the domains. The bond-pads in the PDK provided ESD protection.

5.4 mmWave Layout Considerations

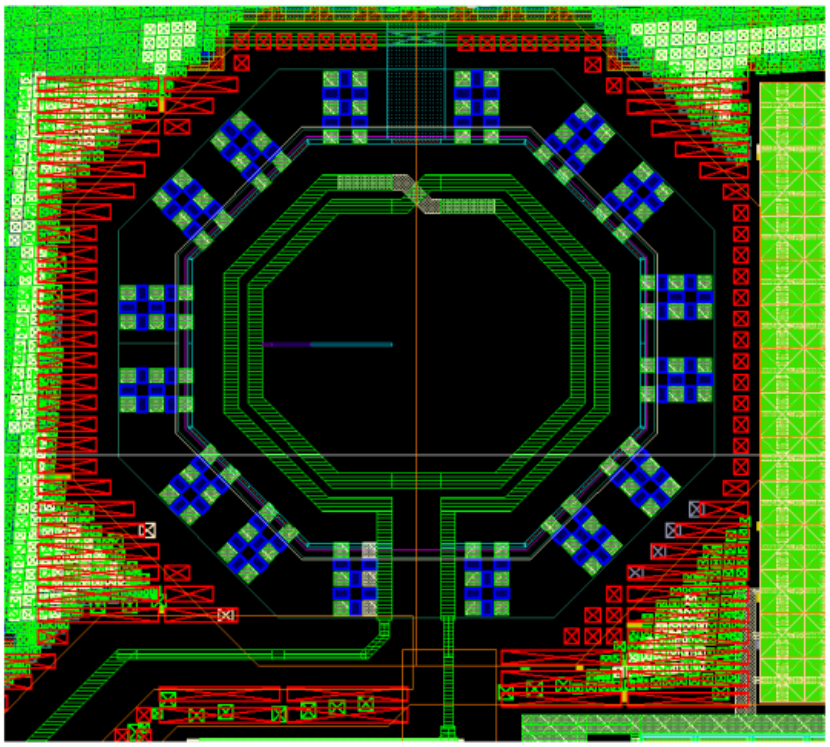


Figure 5.4: Inductor layout with ground ring and manual dummy placement.

mmWave layouts require careful floorplanning to ensure maximum isolation be- tween components and proper grounding. All RF elements were encased in ground boxes to improve isolation between them. The process supported 45°bends, and they were used for all RF lines.

Manual dummy placement was done for diffusion and poly layers near inductors to meet the density requirements. Dummy exclusion layers were drawn over RF components with sufficient clearance.

Care was taken to ensure minimal overlap between RF lines and proper segmentation between actives and passive for EM simulation and parasitic extraction. The supply and ground lines were carefully simulated to ensure that any line inductance does not deteriorate the performance.

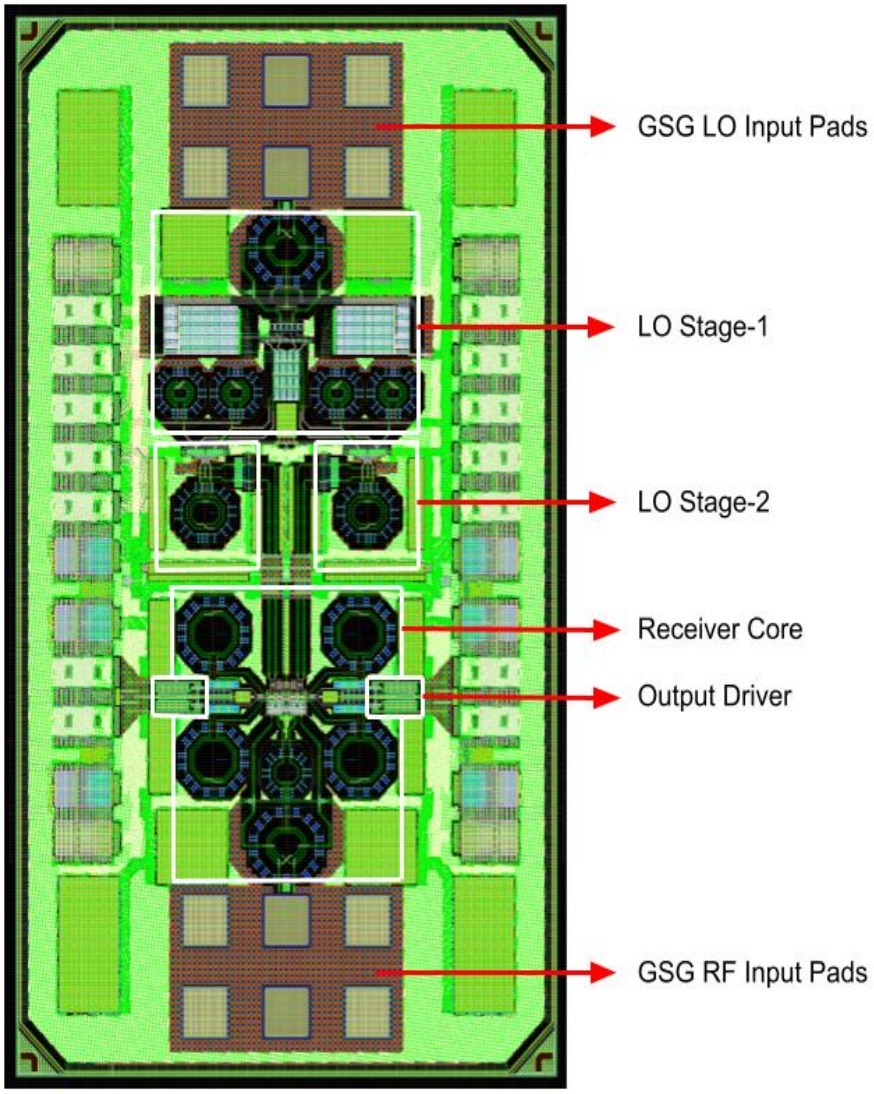


Figure 5.5: Designed layout of the chip.

CHAPTER 6

Simulated Results

A 26GHz Beamformer Receiver was implemented to validate the performance of the proposed single- stage topology at mmWave 5G frequencies. A 1.73mm×1mm die is made ready to be taped-out. This chapter presents simulated results of the implementation.

6.1 Simulated Results:

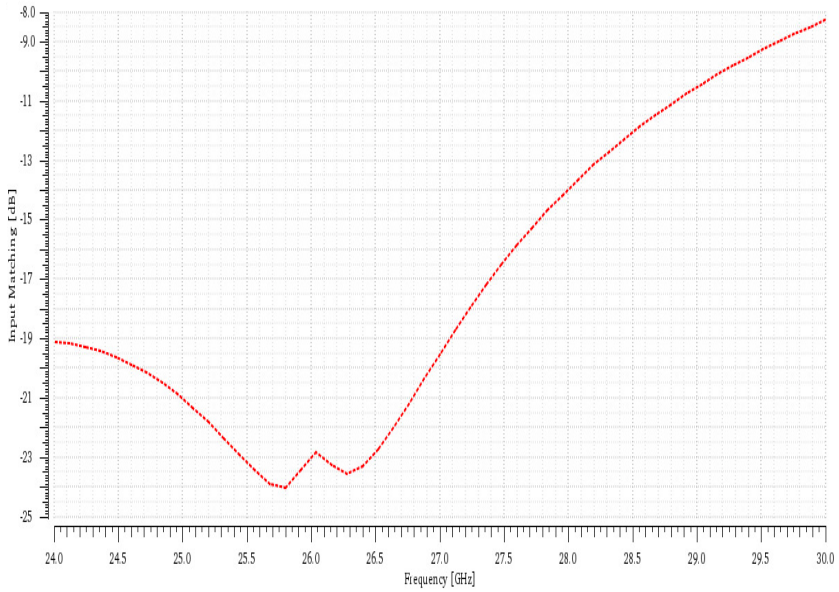


Figure 6.1: Simulated S_{11} for F_{LO} =26GHz

We note from the Figure 6.1 that S_{11} is better than $-10dB$ over the frequency range of interest.

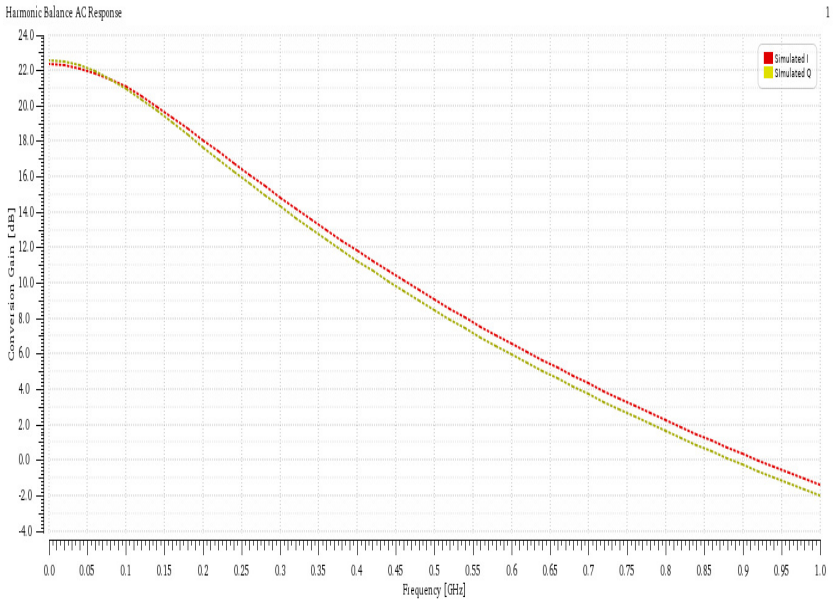


Figure 6.2: Simulated Gain for F_{LO} =26GHz

We note from Figure 6.3 that simulated gain at the Baseband Frequency of $200MHz$ is $18dB$. The gain difference between between I and Q at $200MHz$ is $0.27dB$. The gain difference between I and Q is attributed from the slight mismatch occurred between the two paths and the amplitude mismatch in the LO signals for both the paths.

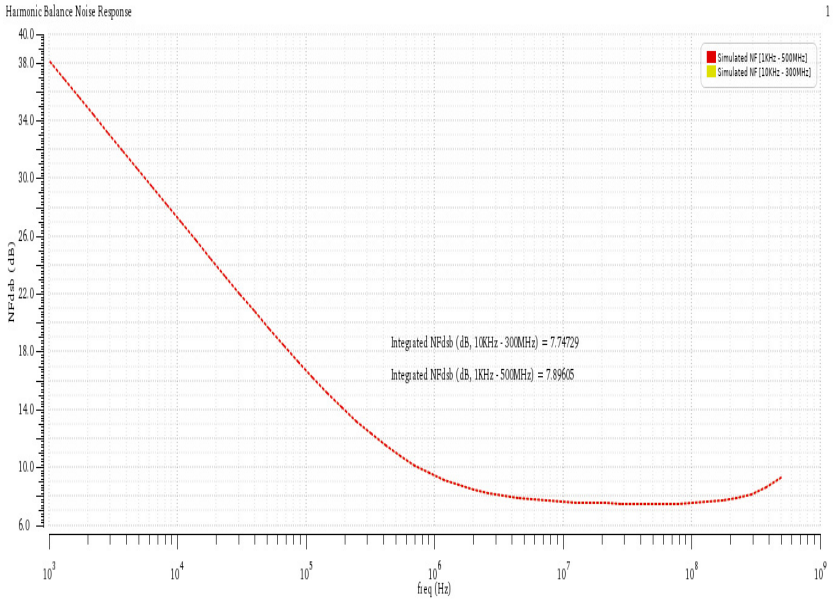


Figure 6.3: Simulated Noise Figure for F_{LO} =26GHz

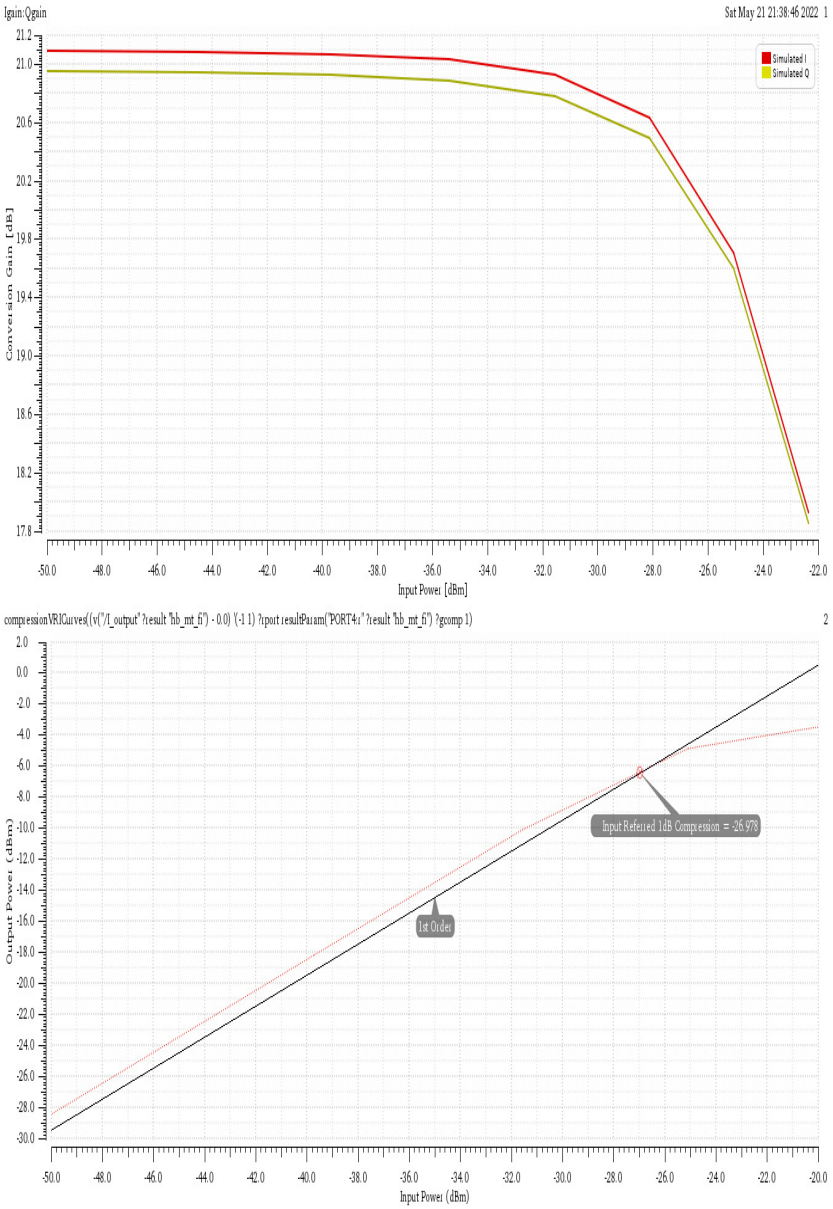


Figure 6.4: Simulated Gain compression for F_{LO} =28GHz at $100MHz$ offset.

The simulated input 1-dB compression point of the chip is $-27dB$ as seen from Figure 6.4.

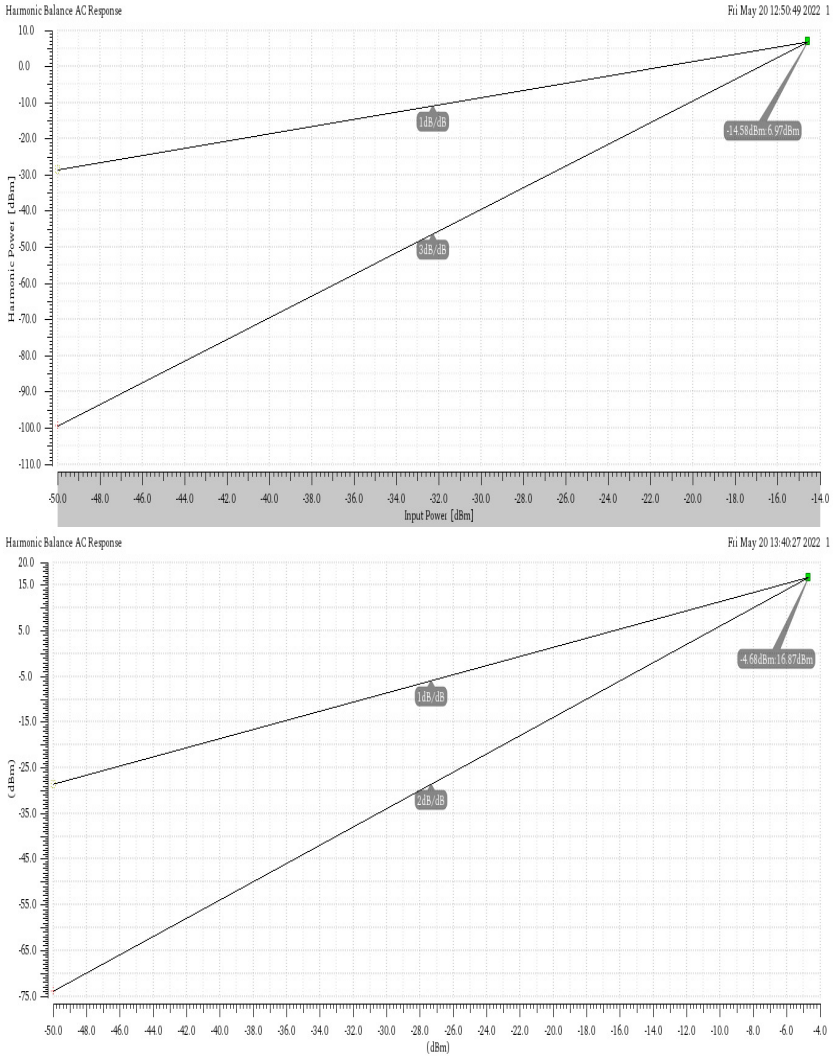


Figure 6.5: Simulated linearity performance for F_LO =26GHz: (a) IIP_2 at 100MHz and 110MHz offset; (b) IIP_3 at 100MHz and 110MHz offset.

As seen from the Figure 6.5, $IIP_3 = -14.6dBm$ and $IIP_2 = -4.7dBm$.

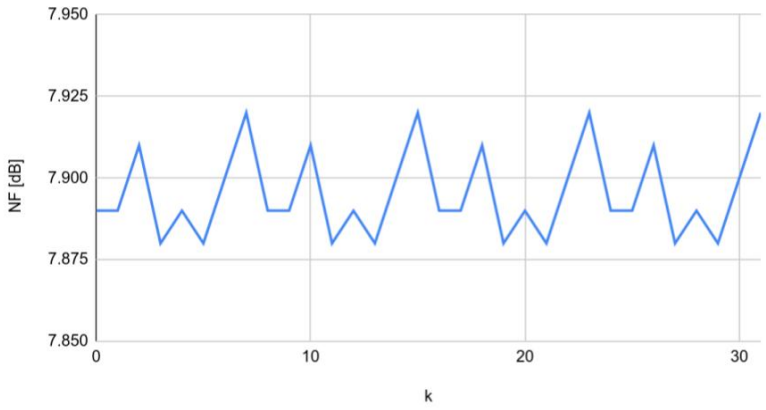


Figure 6.6: Simulated NF as a function of different phase settings

We note from Figure 6.6 that the Noise Figure of the chip is almost constant across all phase settings and hence we can conclude that the receiver performance is invariant of the different phase settings.

6.2 Comparison with other Receivers:

Metric	This work	[8] LG JSSC'18	[14] CMU JSSC'18
Architecture	Direct Conversion		Heterodyne (IQ Outputs)
Process	65nm CMOS	28nm CMOS	65nm CMOS
Phase-Shifter/VGA	Yes	Yes	Yes
Frequency [GHz]	24.0-28.0	25.8-28.0	25-30
Gain [dB]	18	30 to 69	34
Noise Figure [dB]	7.89	6.7 to 13.6	7.3
IP 1dB [dBm]	-27	-68.9 to -34.8	-29 to -21
IIP_2 [dBm]	-4.7	-	-
IIP_3 [dBm]	-14.6	-59.9 to -25.8	-
Power [mW]	30.3	33.8	37

Table 6.1: Performance comparison with other IQ Receivers

CHAPTER 7

CONCLUSION FUTURE WORK

An integrated phase-shifting scheme and optimized single-stage receiver topology that complements each other to realize area and power optimization goals was presented. The working and implementation of the integrated phase-shifting scheme was illustrated. A 26GHz receiver implementing the proposed Phase shifting scheme was designed to validate its performance.

While this work has shown the working of the single-stage topology incorporating LO path Phase Shifting mechanism to function at the mmWave 5G spectrum, a design incorporating a phase-shifter in RF path needs to be implemented and validated to create a single RF receive channel required in the 5G phased-array architecture. This needs to be followed with a multi-channel implementation, where the proposed integrated phase-shifting scheme can be validated. Similar designs need to be implemented on the transmitter side, after which the complete RF front-end of a 5G beamforming transceiver IC can be designed.

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