5G - MILLIMETRE-WAVE FREQUENCY DOUBLER

A THESIS

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THESIS CERTIFICATE

This is to certify that the thesis entitled **"5G - MILLIMETER-WAVE FREQUENCY DOUBLER"** submitted by **BHANU PRAKASH VELDANDI**, to the Indian Institute of Technology, Madras for the award of the degree of **DUAL DEGREE (BACHELOR OF TECHNOLOGY & MASTER OF TECHNOLOGY)** is a bonafide record of research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

Keywords: 5G communication, frequency doubler, passive mixer, DC offset, IQ imbalance, millimetre-wave circuits.

The fifth generation of wireless communication standards, 5G networks, are expected to meet the growing demand for wireless capacity and data rates such as high speed, low latency and bandwidth constraints. 5G networks also open up new possibilities and innovations in various domains. However, multiple technologies and challenging designs and paradigms need to be materialized to see the full potential of 5G networks and systems.

On the circuits side, one of the critical challenge is the implementation of an LO oscillator or an LO driver for the upconversion operation in the transmitter. Area and power efficiency also become quite crucial aspects in the design.

This thesis presents a way to generate higher frequencies from lower frequencies, especially doubling the frequency, without the use of an on-chip Phase-Locked Loop. The proposed architecture produces fully differential In-phase and Quadrature sinusoids, with frequency twice the input frequency, so is the name frequency doubler, which can drive an upconversion mixer. The analysis, optimization and challenges in the design, in general, and at mmWave frequencies in specific, are also presented here.

A frequency doubler, whose input frequency is 13 GHz and output frequency is 26 GHz is designed and taped out as a fully bonded IC.

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CHAPTER 1

INTRODUCTION

The increased demand for higher data rates, lower latency, better quality and larger wireless capacity has increased the demand for the advancement, development and establishment of the next generation of mobile communication standards, the 5G (fifth generation) communication networks. This new standard is envisioned to open up new possibilities in domains such as communication, security, healthcare, transportation, and consumer electronics. To make 5G networks a feasible solution, several technological innovations and research advancements are being pursued both in the industry and academia.

1.1 Objective and scope of this thesis

A transmitter processes the voice or data signal and sends it to the antenna, which transmits the signal. The transmitter must drive the antenna with a high power level so that the transmitted signal is strong enough to reach far distances. The signal that needs to be transmitted is first applied to a modulator or upconverter (upconversion mixer) which converts the signal at baseband frequency to the carrier frequency (f_C), which is typically a higher frequency, that's why the name upconversion (translation from low frequency to high frequency).

We use a high-frequency LO waveform (frequency f_{LO}), typically generated from a Local Oscillator (that's why the name LO) to translate the baseband frequency to a higher frequency.

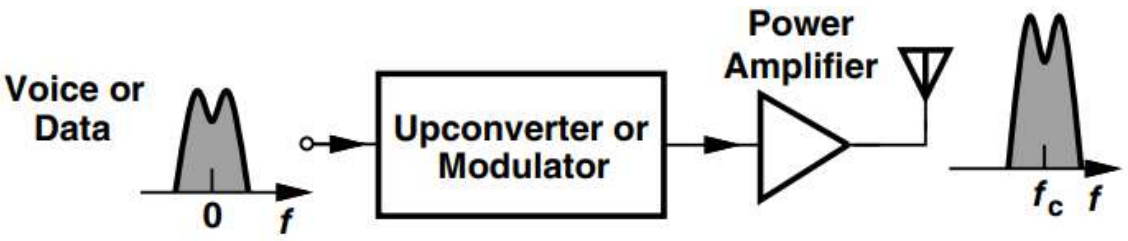


fig 1.1.1 Simple view of an RF transmitter

A variety of potential paradigms and technologies are expected to go into the realization of 5G networks. The previous generations of mobile communications have all used lower carrier frequencies (up to 6 GHz), which has led to spectrum congestion and lower quality of connections. Low-frequency carriers also limit the bandwidth of operation and the maximum capacity. 5G networks will tap the unused spectrum in the millimeter-wave (mmWave) frequency range to meet the projected data rate and capacity requirements.

The objective and scope of this thesis is to provide a LO waveform for the upconversion mixer so that the signal is transmitted in the desired 5G band, 26 GHz in this case. High-frequency Local Oscillators (typically PLLs, off the chip) can be costly or unavailable. The attempt here is to use an off-chip PLL at a lower frequency (13 GHz) and convert it (multiply it) to a higher frequency that can drive (provide the LO signal for) the up-conversion mixer.

1.2 Specifications of the frequency doubler

Since the input frequency is 13 GHz, the targeted output frequency is 26 GHz. The 13 GHz input tone is taken from outside the chip (off-chip PLL). Since it's an off-chip signal, there is a need for a 50 Ω matching network in the input path. The terminology used for this matching network in this thesis is *input matching* and the target specification is S_{11} < -10 dB.

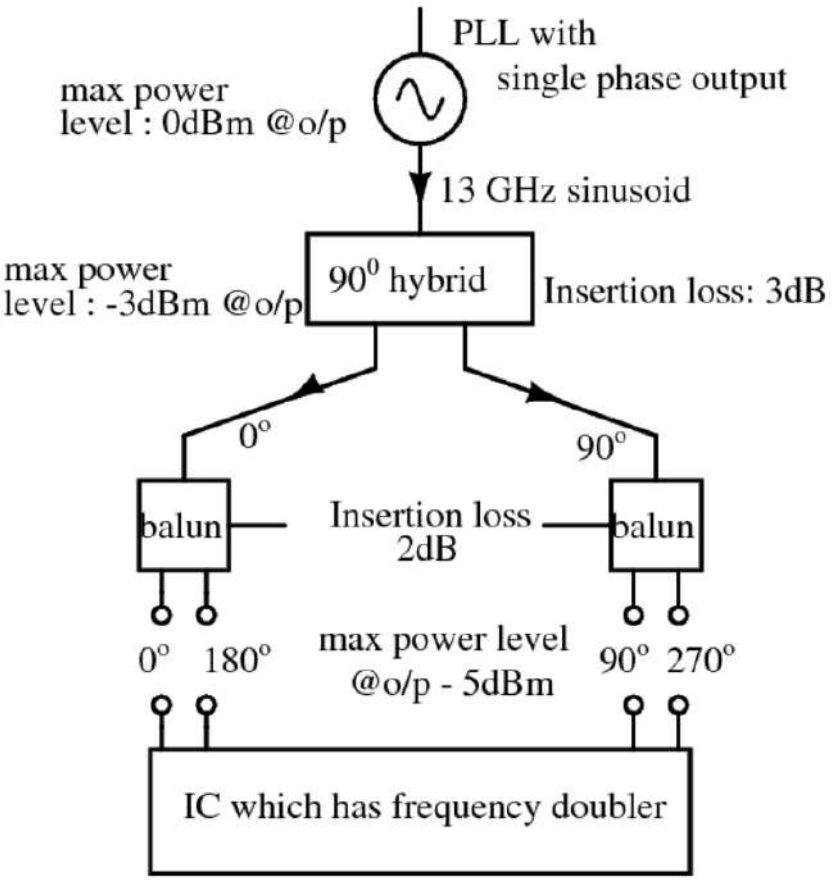


fig 1.2.1 block-level power levels of the 13 GHz input before IC.

The PLL's output at 13 GHz is a single-phase AC coupled signal with a power level tunable from -10 dBm to 0 dBm. The output from PLL is then applied to the 90° hybrid which provides Inphase and Quadrature signals from a single-phase signal. Each output of the 90° hybrid is then applied to a balun, which converts the single-ended signal to the differential. Hence we get differential I and Q signal i.e., the phases of the 13 GHz sinusoids at the outputs baluns are 0°, 90°, 180°, and 270° as shown in figure 1.2.1. The 90° hybrid, that is used, can have an insertion loss up to 3 dB and the balun can have insertion loss up to 2 dB. Hence the maximum power level of the 13 GHz sinusoid with differential I and Q phases is -5 dBm, which is used by the doubler inside the IC to multiply it by 2 and achieve LO sinusoid at 26 GHz.

Upconversion mixers also have their own specification on the minimum and maximum amplitude required for the LO signal that it needs. The amplitude and phases of the LO signal command the performance of the upconversion mixer to a very crucial extent, explained in the later chapters in detail. The specification provided is that the LO signal should have an amplitude ranging from 280 mV to 320 mV. The noise of the LO signal is not a concern as it is the LO for the upconverter in the transmitter, where the signal that we are transmitting is at much high power level compared to the typical noise level. The noise of LO becomes important in the receiver chain where the received message signal strength may be weak (low power level).

The specification of the phases of the LO signal provided to the upconverter is given in terms of the I-Q imbalance of the transmitter, which has to be lesser than -40 dBm. We need four phases (differential I-Q phases) for the 26GHz LO signal. The details of this specification are discussed in detail in the chapter 5: *The I-Q imbalance* .

The summary:

1. Input matching looking in from off-chip is S_{11} < -10 dB.
2. The maximum power level of the 13 GHz signal available from off-chip is -5 dBm.
3. The amplitude range of the 26 GHz LO signal provided to the upconversion mixer is 280mV to 320mV.
4. The I-Q imbalance of the transmitter is < -40 dBm.
5. We need 0^o, 90^o, 180^o, and 270^o phases for the LO signal.

CHAPTER 2

DIFFERENT WAYS OF IMPLEMENTING A FREQUENCY DOUBLER

A frequency doubler, as the name suggests, is a circuit that doubles the frequency i.e., the output frequency is twice the input frequency. This can be achieved by harnessing the second-order nonlinearity of the devices or by mixing operations or using a PLL with a divide by 2, represented as %2, frequency divider. The attempts to implement a frequency doubler with different topologies are discussed in this section in certain detail.

The resistive load and the parasitic capacitances from the device would make the Bandwidth at the load fall to a few GHz (<10GHz), which makes the load attenuating at the frequency of interest, 26GHz. So the parasitics are resonated with the inductor. Hence all these proposed circuits have LC tuned loads. Sometimes in the circuits, only a resistor is shown as the load, which can be understood as the total effective impedance, which is resistive at the resonance frequency.

2.1 Conventional Common Source Amplifier

Consider a Common Source Amplifier (CSA) as shown in the figure 2.1.1. Rather than using the straight amplifying property of the device, the attempt here is to use the nonlinearity of the device and harness the second harmonic content (the frequency twice the fundamental tone), given the fundamental tone is the input tone at 13GHz. The LC load is tuned at 26GHz to provide low impedance at 13GHz but high impedance at 26GHz. The output tone at the second harmonic turns out to be at a very low voltage level because the second-order nonlinearity is not a strong property of the device.

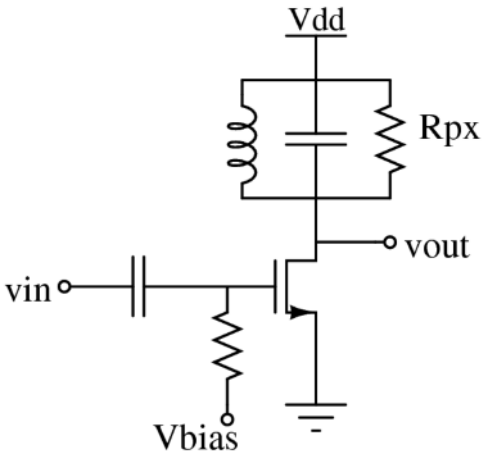


fig 2.1.1 Common Source Amplifier topology.

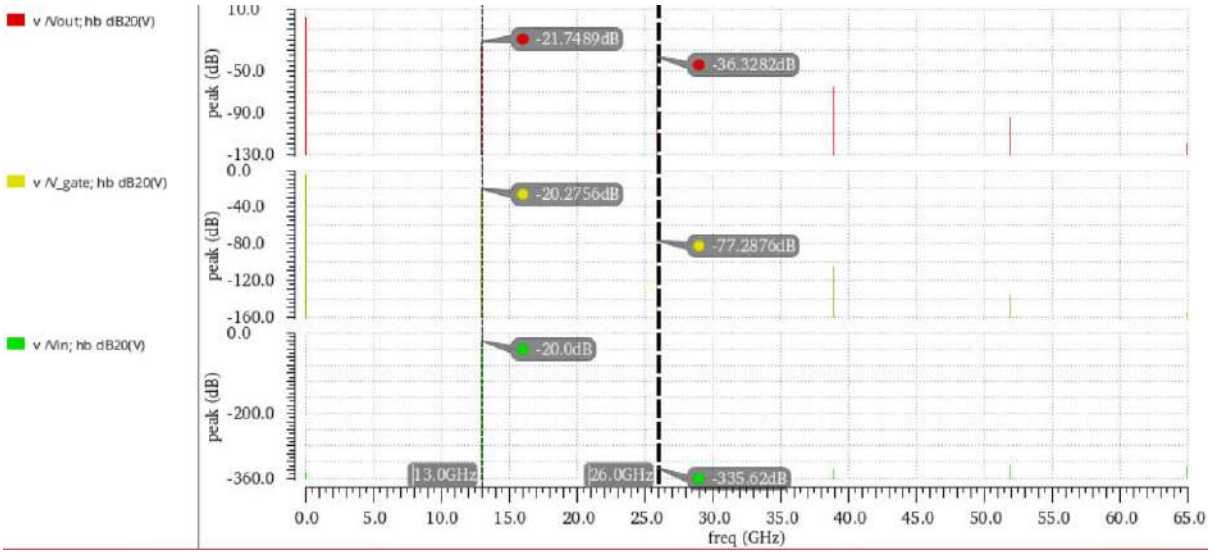


fig 2.1.2 Voltage spectrum at the output, gate of the transistor and the input applied to the circuit shown in the figure 2.1.1.

However, the second harmonic content is observed at the output of the CSA, its value is much lower than the applied 13 GHz tone. If we define the gain of this doubler as the ratio of the voltage level of the 26 GHz tone at the output to the applied input voltage level of the 13 GHz tone, the gain achieved from this circuit is -36.38dB - (-20)dB = -16.38dB. Another important note here is that this gain depends on the input signal level also.

The voltage level of the second harmonic can be increased by using amplifiers after this CSA stage to amplify the 26 GHz tone. This architecture demands heavy power consumption and amplification stages. This is a

possible way of implementation but not an efficient one. However, this architecture doesn't suit as a LO waveform provider for the receiver chain as noise is an important specification for the receivers and the amplifying devices further amplify the noise from the previous stages. This architecture may be used in the Transmitter chain, as the noise of LO is not a very crucial factor there.

When an input matching network is employed at the input of the CSA, the network can be similar to a typical LNA input matching, the signal level at the gate of the MOSFET in the CSA drops by half compared to the input signal applied. This makes the design more challenging (or more amplification demanding), as there is a 3dB attenuation in the signal path.

2.2 Switch - Common Gate amplifier topology

The attempt here, again, is to use the nonlinearity of the device but with a different topology, the Common Gate Amplifier as shown in the figure 2.2.1. The 50Ω input matching can be achieved by adjusting the load of the amplifier to the impedance required. The MOSFET just acts as a switch in the ON state, thereby offering a low resistance, Ron. The signal applied at the source of the NMOS sees an impedance which is the combination of Ron, parasitic capacitances and the load at the drain, which however is LC tuned at 26GHz. The input matching can be fairly achieved but the signal output at the second harmonic is very weak, because the load is only 50Ω at the resonant frequency. If we use a matching network and design the circuit for a good value of second harmonic, we get a decent gain similar to the CSA case, the result is shown in the figure 2.2.2.

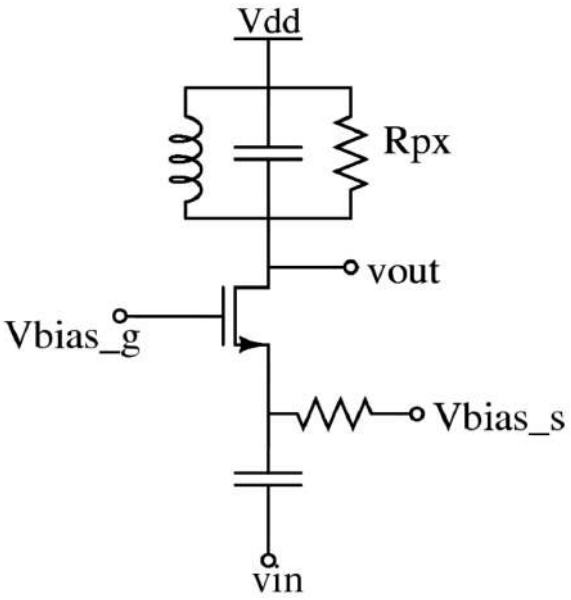


fig 2.2.1 Common Gate Amplifier Topology

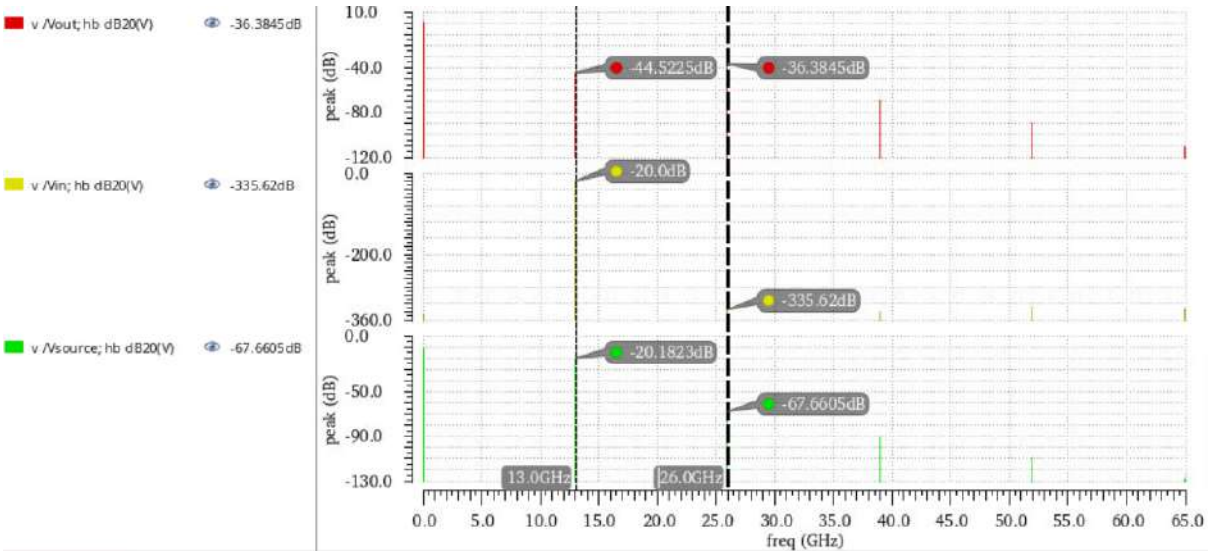


fig 2.2.2 Voltage spectrum at the output, input and the source of the transistor of the circuit shown in the figure 2.2.1.

The gain here is also the same as the one achieved with the CSA amplifier. This output needs amplification stages again to use it as a LO waveform for the mixer, making the situation similar to the CSA output stage.

2.3 Integer N synthesizer - PLL

Achieving frequency multiplication from an integer N synthesizer is quite possible as PLL is a closed-loop system which locks the phase of the output with respect to a reference clock (can be at a frequency lower than the output frequency). The output frequency is N times the input frequency (reference clock frequency, which can be considered as input frequency).

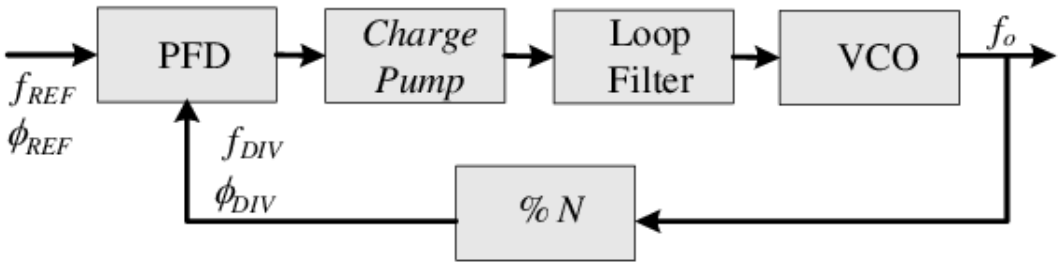


fig 2.3.1 Integer N PLL topology

The equation governing the behaviour of a PLL is

$$\Phi_{REF} = \Phi_{DIV} \qquad \text{(eqn 2.1)}$$

The phase detector detects the phase error between the Φ_{REF} and Φ_{DIV} and the phase detector and the charge pump circuit generates an error voltage corresponding to the phase error given by :

$$\Phi_{error} = \Phi_{REF} - \Phi_{DIV} \qquad \text{(eqn 2.2)}$$

The %N block divides the frequency of the output by N. Therefore it can be written that

$$\Phi_{out} = N \times \Phi_{DIV} \qquad \text{eqn(2.3)}$$

From the equations 2.1 and 2.3 we can write that

$$\Phi_{out} = N \times \Phi_{DIV} = N \times \Phi_{REF} \qquad \text{eqn(2.4)}$$

$$\frac{\partial}{\partial t}(\Phi) = \omega = 2\pi f \qquad \text{eqn(2.5)}$$

Differentiating equation 2.4 on both sides, we get

$$f_{out} = N \times f_{in} \qquad \text{eqn(2.6)}$$

For N = 2, we get $f_{out} = 2 \times f_{in}$.

Frequency doubling is achieved. The design and implementation are quite challenging at higher frequencies and are beyond the scope of this thesis.

2.4 Mixer

Mixers perform frequency translation by multiplying two signal waveforms. The mixer has three distinct ports, as shown in fig 2.4.1. The input signal gets multiplied by the Local Oscillator signal (LO signal) and hence the frequencies get translated. Mixers are typically used in the receiver or transmitter chain for the downconversion or upconversion respectively as shown in fig 2.4.2.

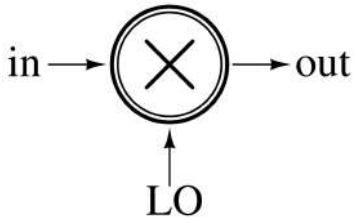


fig 2.4.1 Mixer shown as a three port system

When the input signal and LO signal both have the same frequency, let's say f_{in}, we get components at DC and twice the input frequency (and other harmonics, practically) as shown in eqn 2.9.

The equation governing the behavior of the mixer can be written as

$$\text{out} = \text{in} \times \text{LO} \qquad \text{eqn(2.7)}$$

which is similar to a simple analog multiplier which multiplies signals.

Let 'in' and 'LO' be sinusoidal signals: $\sin(\omega_{in}t)$ and $\sin(\omega_{LO}t)$, then the output is

$$\text{out} = \sin(\omega_{in}t) \times \sin(\omega_{LO}t) \qquad \text{eqn(2.8)}$$

In our case: the frequencies of 'in' and 'LO' are the same, say ω_{in}. This implies

$$\text{out} = \sin(\omega_{in}t) \times \sin(\omega_{in}t) = \sin^2(\omega_{in}t) = \frac{1}{2} \times [\ 1 - \cos(2\omega_{in}t)\ ] \qquad \text{eqn(2.9)}$$

The term 1 in '1 - $\cos(2\omega_{in}t)$' corresponds to the component at DC and the term $\cos(2\omega_{in}t)$ has frequency $2f_{in}$ i.e., there are components at zero frequency and frequency twice the input frequency.

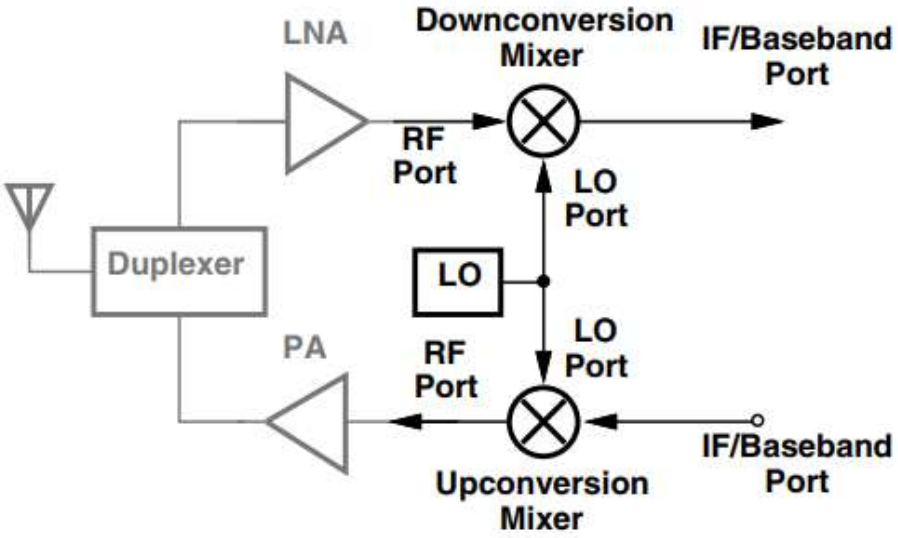


fig 2.4.2 Role of a mixer in a general transceiver.

CHAPTER 3

PASSIVE MIXER BASED FREQUENCY DOUBLER

3.1 Theoretical background - Basic mixer operation

Passive mixers do not provide any power gain, they have conversion loss. They may have current or voltage gain. Active mixers provide power gain using active devices. Voltage mode passive mixer translates the frequency by the switching action of a mosfet. The MOSFET is realized as a switch as shown in figure 3.1.1 (a), where V_{LO} turns the switch on and off which results in V_{IF} being V_{RF} or V_{IF} being equal to zero respectively. The abrupt switching action can be viewed as a multiplication of the RF input (V_{RF}) by a square wave toggling between 0 and 1. Thus, as illustrated in figure 3.1.1 (b), the circuit mixes the RF input with all of the LO harmonics, producing frequencies which can be viewed as RF frequency translated by the harmonics of LO.

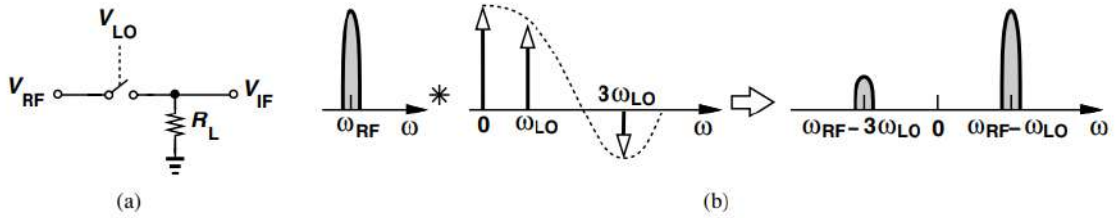


fig 3.1.1 (a) Mixer using an ideal switch, (b) input and output spectra

The output of this mixer can be written in the time domain as

$$V_{IF}(t) = V_{RF}(t) \cdot S(t) \qquad \text{eqn(3.1)}$$

where S(t) denotes a square wave toggling between 0 and 1 with a frequency of f_{LO}. The output spectrum is therefore given by the convolution of the spectra of $V_{RF}(t)$ and S(t). Since the spectrum of a square wave is equal to a train of impulses whose amplitudes follow a sinc envelope, we have

$$V_{IF}(f) = V_{RF}(f) * \sum_{n=-\infty}^{+\infty} \frac{\sin(n\pi/2)}{n\pi} \delta\left(f - \frac{n}{T1}\right) \qquad \text{eqn(3.2)}$$

$$= \sum_{n=-\infty}^{+\infty} \frac{\sin(n\pi/2)}{n\pi} V_{RF}\left(f - \frac{n}{T1}\right) \qquad \text{eqn(3.3)}$$

where T1 = 1 / f_{LO}.

Even if LO is a sinusoid instead of a square wave, the switching can be assumed to be maintained. Note that the spectrum that is shown in figure 3.1.1 (b) is not complete. Only two harmonics around the DC are shown.

Let us consider the case of a Down conversion mixer, where the received signal is at a high frequency (f_c) and the frequency is translated to a lower frequency. To lower the center frequency, the signal is multiplied by a sinusoid $A_o\cos(\omega_{LO}t)$, which is generated by a local oscillator (LO).

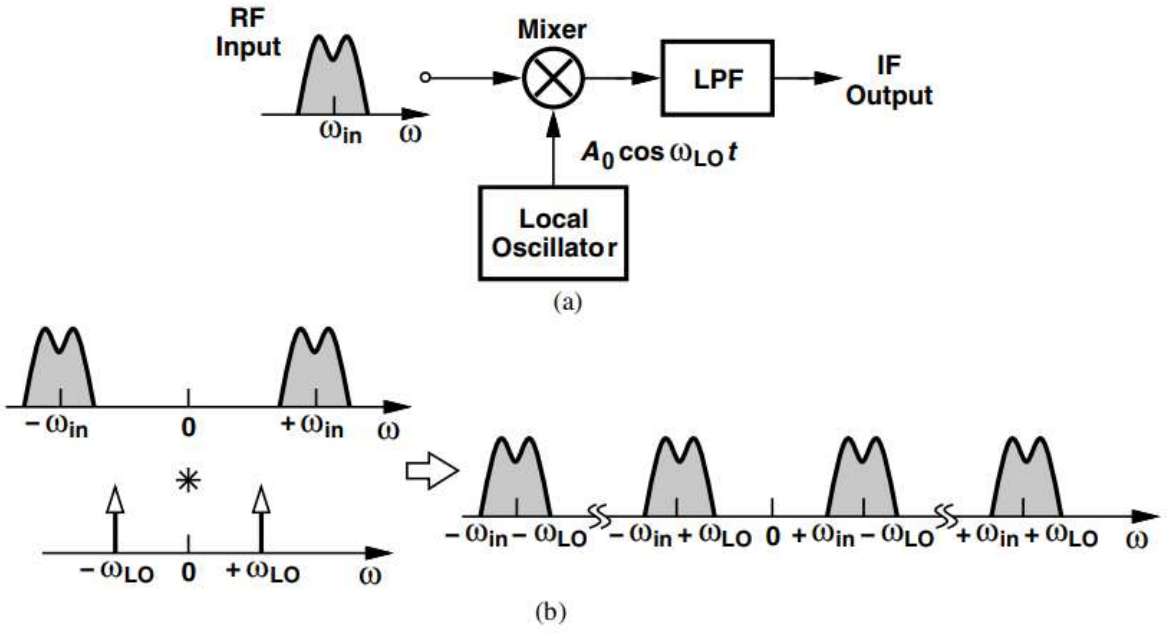


fig 3.1.2 (a) Downconversion by mixing, (b) resulting spectra.

Since multiplication in the time domain corresponds to convolution in the frequency domain, we observe from Fig. 3.1.2 (b), that the impulses at $\pm\omega_{LO}$ shift the desired channel to $\pm(\omega_{in} \pm \omega_{LO})$. The components at $\pm(\omega_{in} + \omega_{LO})$ are not of interest (since it is down conversion) and are removed by the low-pass filter (LPF) as shown in figure 3.1.2 (a), leaving the signal at a center frequency of $\omega_{in} - \omega_{LO}$ and $-(\omega_{in} - \omega_{LO})$. This entire operation is called "downconversion mixing" or simply "downconversion. If a band pass filter (BPF) tuned at frequency $\omega_{in} + \omega_{LO}$ is used in place of LPF, the components at $\pm(\omega_{in} - \omega_{LO})$ are filtered out leaving us with the components at a higher frequency. Now consider $\omega_{in} = \omega_{LO}$. The outputs now are at $\pm(2\omega_{LO})$ and at DC, which achieves frequency doubling.

3.2 Theoretical background - single-balanced vs double-balanced

The simple mixer of fig. 3.1.1(a) operates with a single-ended RF input and a single-ended LO. Discarding the RF signal for half of the LO period (when the switch is off), this topology is rarely used in modern RF design. Figure 3.2.1(a) depicts a more efficient approach whereby two switches are driven by differential LO phases, thus "commutating" the RF input to the two outputs.

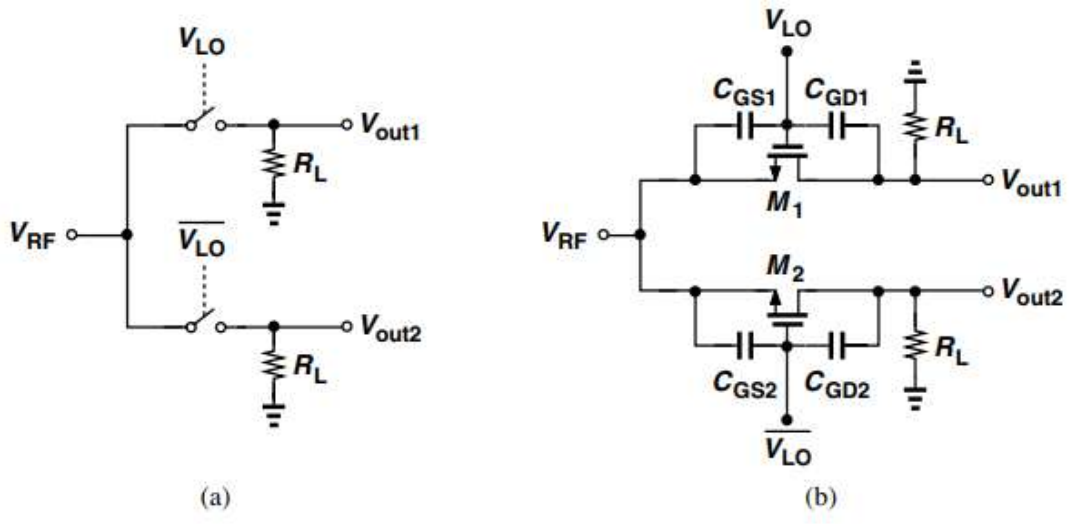


fig 3.2.1 (a) Single-balanced passive mixer, (b) implementation of (a).

This circuit is called a “single-balanced” mixer because of the balanced LO waveforms. Furthermore, the circuit naturally provides differential outputs even with a single-ended RF input, easing the design of subsequent stages. Also, as seen in fig. 3.2.1 (b), the LO-RF feedthrough at ω_{LO} vanishes if the circuit is symmetric. The single-balanced mixer of fig. 3.2.1 (b) nonetheless suffers from significant LO-IF feedthrough. In particular, denoting the coupling of V_{LO} to V_{out1} by $+kV_{LO}$ and that from V_{LO} to V_{out2} by $-kV_{LO}$, we observe that $V_{out1} - V_{out2}$ contains an LO leakage equal to $2kV_{LO}$. To eliminate this effect, we connect two single-balanced mixers such that their output LO feedthroughs cancel but their output signals do not. Shown in fig. 3.2.2, such a topology introduces two opposing feedthroughs at each output, one from V_{LO} and another from V^-_{LO}. The output signals remain intact because, when V_{LO} is high, $V_{out1} = V^+_{RF}$ and $V_{out2} = V^-_{RF}$, and when V^-_{LO} is high, $V_{out1} = V^-_{RF}$ and $V_{out2} = V^+_{RF}$. That is, $V_{out1} - V_{out2}$ is equal to $V^+_{RF} - V^-_{RF}$ for a high LO and $V^-_{RF} - V^+_{RF}$ for a low LO. Called a “double-balanced” mixer, the circuit of Fig. 3.2.2 operates with both balanced LO waveforms and balanced RF inputs.

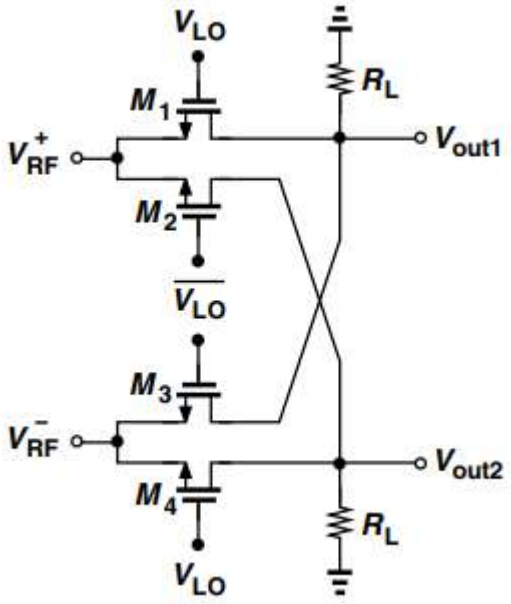


fig 3.2.2 Double balanced passive mixer

3.3 Frequency doubler implementation

Building from the above theoretical background, fig 3.3.1 shows a frequency doubler with a double-balanced mixer implementation which multiplies two waveforms of the same frequency.

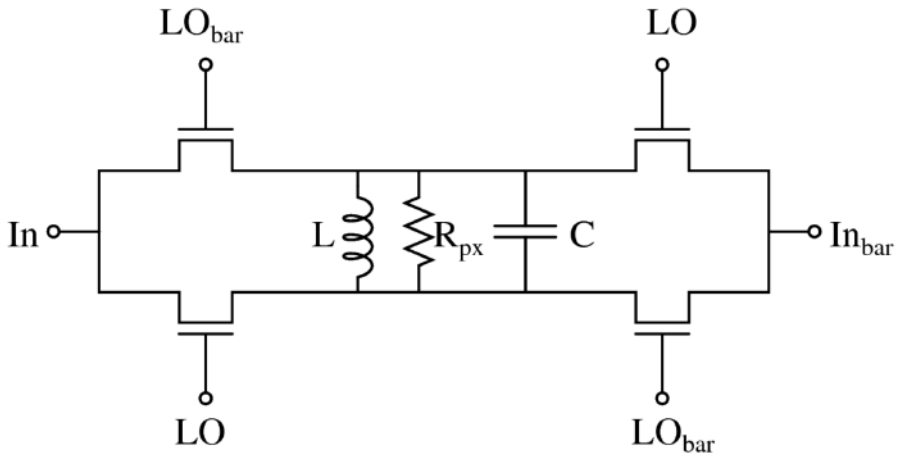


fig 3.3.1 LC tuned double balanced voltage mode passive mixer

As mentioned earlier in eqn(2.7), the equation governing the mixing operation can simply be written as out = in_1 x in_2, nothing but a simple analog multiplication. Mathematically we analyze the two inputs of the mixer in a similar way, as shown in figure 3.3.1, but in the circuit the implementation of mixer, one of the inputs governs the switching action and the other is the waveform whose frequency gets translated by the switching action.

There are four possible ways of multiplication of two waveforms of same frequency.

1. Multiplying Inphase with Inphase.
2. Multiplying Quadrature with Quadrature.
3. Multiplying Inphase with Quadrature.
4. Multiplying Quadrature with Inphase.

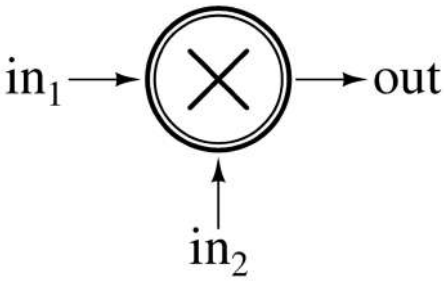


fig 3.3.2 mixer with inputs and output ports.

Let's understand them mathematically.

$$\sin(\omega_{in}t) \times \cos(\omega_{in}t) = 0.5 \times \sin(2\omega_{in}t) \qquad \text{eqn(3.4)}$$

$$\sin(\omega_{in}t) \times \sin(\omega_{in}t) = \sin^2(\omega_{in}t) = 0.5 \times (1 - \cos(2\omega_{in}t)) \qquad \text{eqn(3.5)}$$

$$\cos(\omega_{in}t) \times \cos(\omega_{in}t) = \cos^2(\omega_{in}t) = 0.5 \times (1 + \cos(2\omega_{in}t)) \qquad \text{eqn(3.6)}$$

In all these multiplications, doubling of frequency is achieved and we also get Inphase and Quadrature components. Let us make an assignment that the cosine component be called Quadrature and the sine component be called Inphase. With the above-mentioned four ways of multiplication and employing balanced topology, we achieve differential I-Q waveforms as outputs. Let us try to analyse these in detail.

3.4 The sin x cos multiplication

Multiplying Inphase with Quadrature and Quadrature with Inphase is mathematically the same: the sin gets multiplied with cosine. In the circuit level implementation, the difference comes in what is fed to the gates, the LO and LO_{bar} (which governs the switching action) and what is fed to the drains, the In and In_{bar} of the MOSFETs.

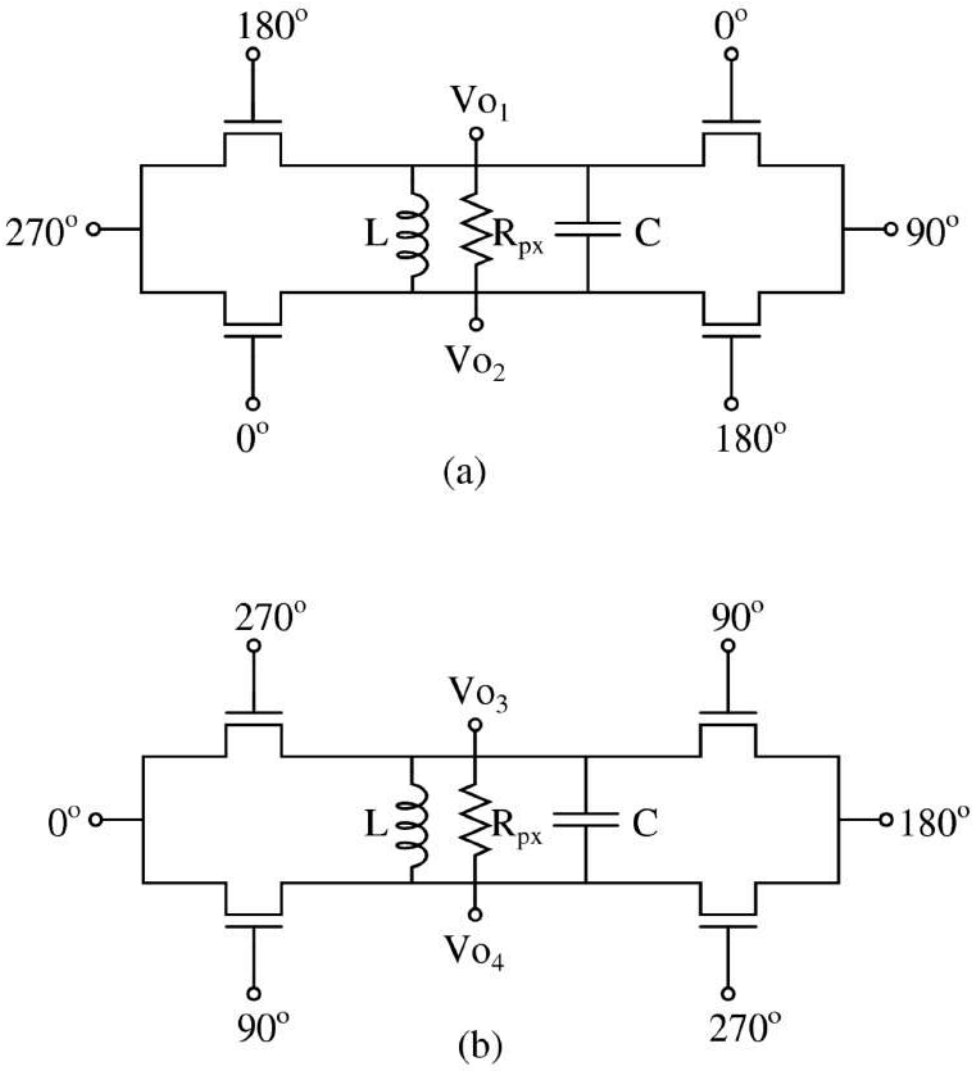


fig 3.4.1 Double balanced sin x cos multiplication as shown in fig 3.3.2

(a) sine is fed as In and cos as LO (b) cos is fed as In and sin as LO

Consider the circuits shown in figure 3.4.1, which shows the sin x cos multiplication based doubler implementations. The values of L and C are adjusted such that the load resonates at 26 GHz. R_{px} is the overall effective parasitic resistance of the load at the resonance frequency. The voltages applied at the inputs of the mixer are ideal sinusoids with frequency equal to 13 GHz. Mathematically represented by $V_o\cos(\omega_o t + \theta_i)$. Where ω_o is $2\pi f_o$ and f_o is 13 GHz. Only θ_i are marked at the respective nodes and θ_i can take only one of four values (0^o, 90^o, 180^o, and 270^o).

- 0^o is $Vocos(\omega_o t)$ which is cosine, the Quadrature.
- 180^o is $Vocos(\omega_o t + 180^o)$ which is equal to $-Vocos(\omega_o t)$.
- 270^o is $Vocos(\omega_o t + 270^o)$ which is equal to $Vosin(\omega_o t)$, the Inphase.
- 90^o is $Vocos(\omega_o t + 90^o)$ which is equal to $-Vosin(\omega_o t)$.

The resulting voltages at the output nodes Vo_1, Vo_2, Vo_3 and Vo_4 are shown in table 3.1. Note that only the magnitude and phases at 26 GHz are shown in the table and other harmonics are omitted as they are negligible or insignificant to the current discussion.

Node	Vo_1	Vo_2	Vo_3	Vo_4
Magnitude at 26GHz (in mV)	379	352	352	379
Phase at 26GHz (in deg)	58	291	-249	-122

Table 3.1 mag and phase at the output of the doubler shown in fig 3.4.1

- Vo_1 and Vo_2 are supposed to be differential tones but the phase difference actually is $291 - 58 = 233^o$.
- Vo_3 and Vo_4 are supposed to be differential tones but the phase difference actually is $-122 - (-249) = 127^o$.

The differential nodes should have a phase difference of 180^o.

With the same circuit topology, the frequency is lowered to test if it is a frequency and parasitic capacitance related phenomenon. The results are very similar to the ones shown above in Table 3.1, even when the input frequency is 10 kHz, which concludes that it's not a frequency and capacitance-dependent phenomenon. This may be explained by the phenomenon of DC offset generated from the mixing of sinusoids of the same frequency, which will be explained in a later section.

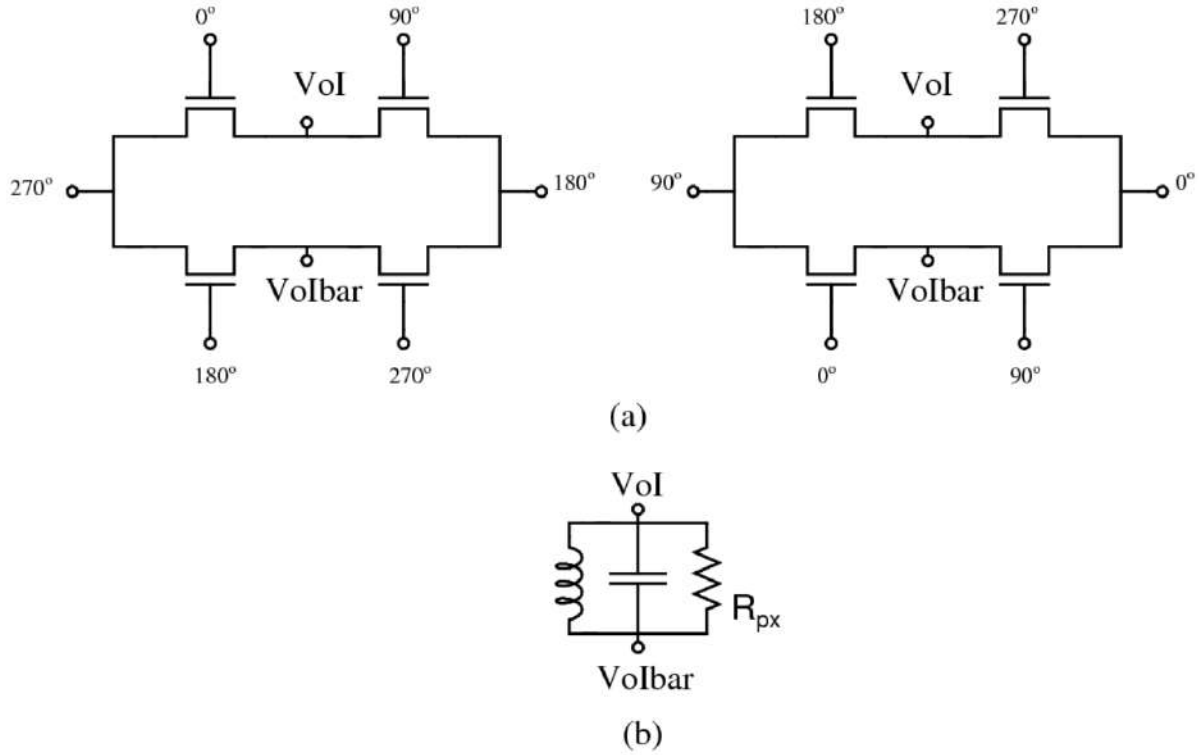


fig 3.4.2 (a) the sin x cos multiplication with nets shorted appropriately (b) shown is the load of the circuit.

An important observation from Table 3.1 is that the nodes Vo_1 and Vo_4 are exactly differential i.e., the magnitude of both the nodes are the same and the phase difference is 180°. Similarly the nodes Vo_2 and Vo_3 are exactly differential. This lets us join the nodes Vo_1 and Vo_3 together and Vo_2 and Vo_4 together. The nets resulting from the combination of Vo_1 + Vo_3 and Vo_2 + Vo_4 would still be differential in phase. The nets Vo_1 and Vo_3 are shorted and is named as VoI and the nets Vo_2 and Vo_4 are shorted and is named as VoIbar indicating the differential nature as shown in figure 3.4.2 (a). The circuit effectively needs only one LC tuned load as shown in figure 3.4.2 (b). The result of this circuit is presented along with the sin x sin and cos x cos multiplication in table 3.3, which is in section 3.5.

3.5 The sin x sin and cos x cos multiplication

In the previous section we have explored the circuit implementation of eqn(3.4). Here we will explore the implementation of eqn(3.5) and eqn(3.6) which is the multiplication of Inphase with Inphase and Quadrature with Quadrature. The circuits are shown in figure 3.5.1 (a) and (b).

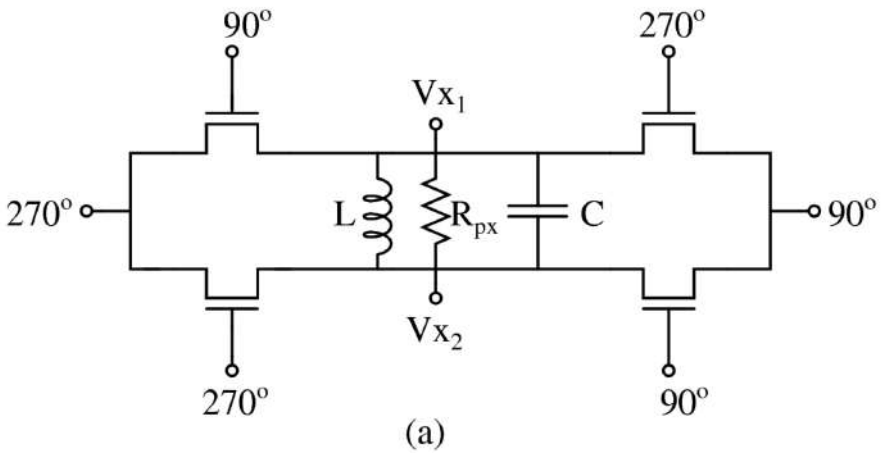


fig 3.5.1 (a) circuit implementation of multiplication of Inphase with Inphase

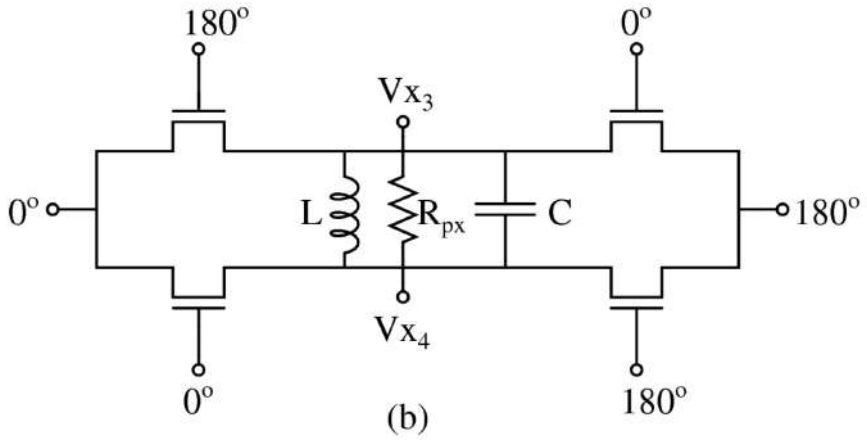


fig 3.5.1 (b) implementation of multiplication of Quadrature with Quadrature

The circuit diagram description is similar to the one discussed in the section 3.4. The resulting voltages at the output nodes Vx_1, Vx_2, Vx_3 and Vx_4 are shown in table 3.2. Here also, the magnitude and phases at 26 GHz are shown in the table and other harmonics are omitted.

Node	Vx_1	Vx_2	Vx_3	Vx_4
Magnitude at 26GHz (in mV)	380	75.8	380	75.8
Phase at 26GHz (in deg)	8.2	191.7	188.2	11.8

Table 3.2 mag and phase at the output of the doubler shown in fig 3.5.1

Comments from the above result:

- The supposed to be differential nodes Vx_1, and Vx_2 are 183.5 degrees apart.
- The supposed to be differential nodes Vx_3, and Vx_4 are 176.6 degrees apart.

Other observations:

- The phase difference between Vx_1 and Vx_3 is 180 degrees exactly and the magnitude is also the same.
- The phase difference between Vx_2 and Vx_4 is 180 degrees exactly and the magnitude is also the same.
- The magnitudes of Vx_1 and Vx_2 differ by a huge amount. The nets Vx_3 and Vx_4 also show similar behaviour. (This is explained in a later section)

The nets Vx_1 and Vx_4 can be shorted and the nets Vx_2 and Vx_3 can be shorted. This leaves us with the circuit as shown in figure 3.5.2 similar to the circuit in figure 3.4.2.

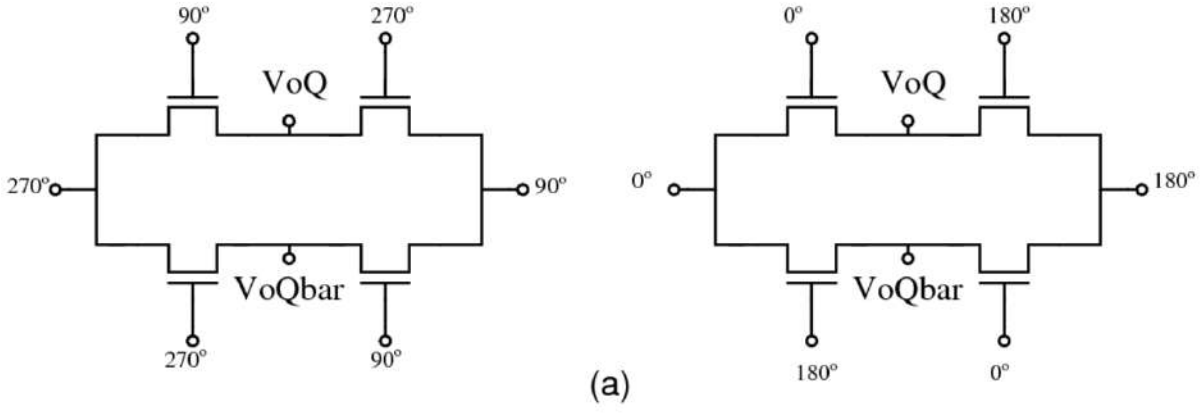
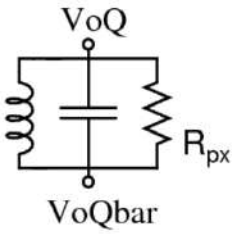


fig 3.5.2 (a) the sin x sin and cos x cos multiplication with the appropriate nets shorted together.



(b)

fig 3.5.2 (b) the load for the circuit shown in the figure 3.5.2 (a)

The final result at the output nodes of circuit (shown in figures 3.4.2 and 3.5.2) after shorting the appropriate nodes from all the four possible ways of implementing the multiplication operation is shown in table 3.3. The phase information of 26GHz is shown and the magnitudes of 26 GHz, 52 GHz and 104 GHz (the even harmonics of 26 GHz) are shown in the table. The magnitudes of other harmonics and harmonics of 13 GHz are not shown in the table as they were too small values, which can be considered as zero. Hence they are neglected.

nodes	Mag 26GHz (In Volts)	Phase 26GHz (In degrees)	Mag 2x26GHz (In Volts)	Mag 4x26GHz (In Volts)
VoI	292.2m	85	524u	143u
VoIbar	292.2m	-95	524u	143u
VoQ	311.7m	-4	2.5m	98u
VoQbar	311.7m	-184	2.5m	98u

Table 3.3 showing the result of circuits shown in figures 3.4.2 and 3.5.2

Comments from the above result:

- ➢ Only the 26 GHz content is the dominant one as the magnitude of other harmonics are quite lower compared to tone at 26 GHz.

- ➢ The phase difference between VoI and VoIbar: 85 - (-95) = 180°.
- ➢ The phase difference between VoQ and VoQbar: -4 - (-184) = 180°.
- ➢ VoI and VoIbar are exactly differential and the nets VoQ and VoQbar are exactly differential.

- ➢ The phase difference between VoI and VoQ: 85 - (-4) = 89°.
- ➢ Similarly the phase difference between VoIbar and VoQbar is 89°.
- ➢ The amplitudes of the VoI and VoIbar are exactly the same and the amplitudes of the VoQ and VoQbar are exactly the same but the amplitudes of I and Q outputs have a difference. This is explained in the next section.
- ➢ The I and Q outputs have a significant difference in phase and amplitudes.

3.6 DC offset in frequency doublers

DC offset is a standard problem in mixers when the frequencies of its two inputs are the same. As we have seen earlier, in section 3.1 and figure 3.1.2, when the input frequency is ω_{in} and LO frequency is ω_{LO} then the impulses at $\pm\omega_{LO}$ shift the desired input channel from ω_{in} to $(\omega_{in} \pm \omega_{LO})$, considering the single side band frequencies only. Now when ω_{in} and ω_{LO} are exactly the same one output spectrum contains frequencies $\omega_{in} \pm \omega_{in}$ which are at DC i.e., $(\omega_{in} - \omega_{in})$ and $2\omega_{in}$ i.e., $(\omega_{in} + \omega_{in})$. Ths additional component that is generated at DC interferes with the given circuit's DC conditions and creates a difference in the DC operating points and the characteristics of the components in the circuit. This creates a difference in the MOSFETs

behaviour and its operating points which is reflected in the magnitude and phases of the output of the doubler.

Eventhough the drain and source of the MOSFET are interchangeable terminals, for the simplicity of understanding, lets consider that the terminal that we are applying inputs are the drains and gates of the n-channel MOSFET. Theoretically, in an NMOS, among the drain and source terminals, the terminal which has the highest voltage acts as the drain and the other one is the source. The terminals G, D and S represent the gate, drain and the source as shown in fig 3.6.1.

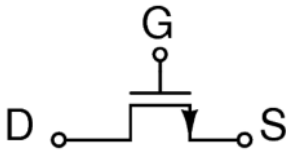


Fig 3.6.1 MOSFET with terminals fixed, for the simplicity of understanding.

The MOSFET and the phases shown at the gates and drains, in figure 3.6.2 represent the scenario of a mosfet in the double-balanced topology of cos x cos multiplication and cos x sin multiplication. Let's consider that the inputs we are applying are square waveforms, for the simplicity of understanding. Since the circuits have periodic waveforms as input it is sufficient and necessary that we analyse them for one time period.

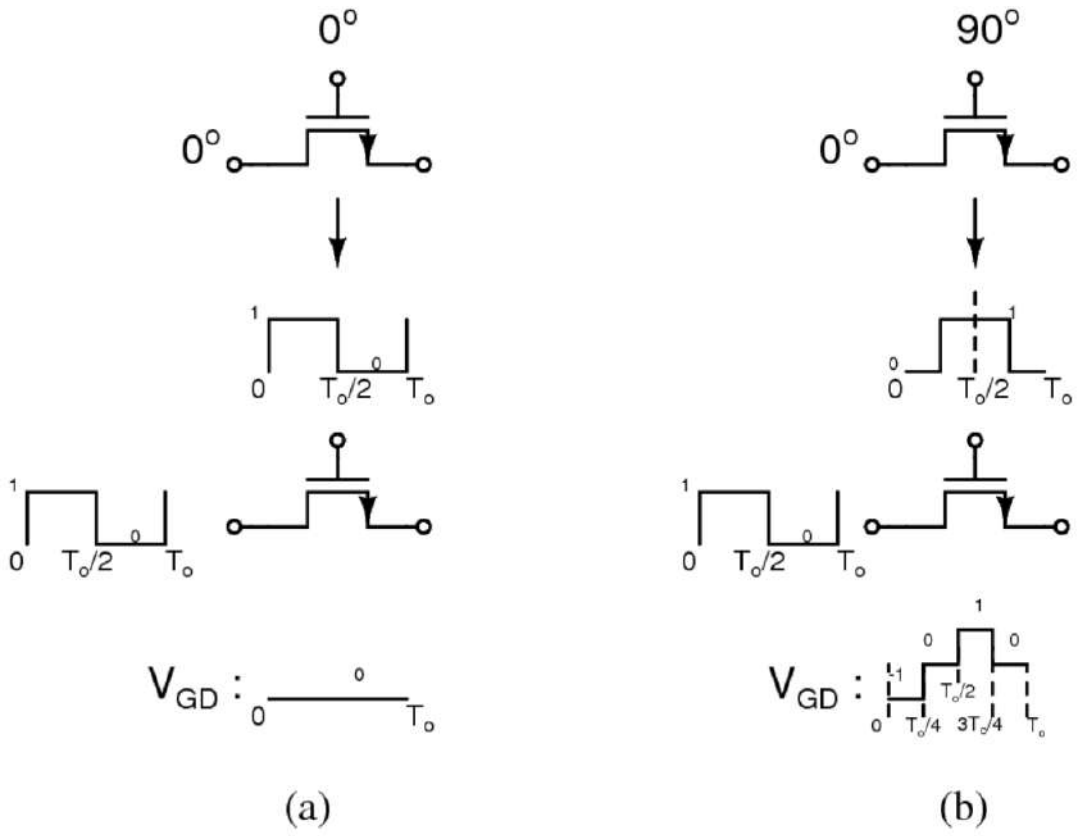


fig 3.6.2 gate and Drain voltage waveform of a MOSFET in (a) cos x cos multiplication (b) cos x sin.

As shown in figure 3.6.2 (a), in cos x cos multiplication, the voltage difference between the gate and the drain (V_{GD}) of the MOSFET M1 is zero in the whole period, as both the waveforms have same phase whereas in the cos x sin multiplication, the voltage V_{GD} of the MOSFET M2 changes from -1 to 0 to +1 and then back to 0 in one time period as shown in figure 3.6.2 (b). This shows that during the time:

- From t = To/4 to t = To/2 and from t = 3To/4 to t = To : the value of V_{GD} = 0 for both the fets M1 and M2.
- From t = 0 to t = To/4, V_{GD} = 0 for M1 but V_{GD} = -1 for M2.
- From t = To/2 to t = 3To/4, V_{GD} = 0 for M1 but V_{GD} = +1 for M2.

During the time interval from t = 0 to t = To/4 and t = To/2 to t = 3To/4 the MOSFETS M1 and M2 sees different V_{GD}, which creates a difference in the characteristics of the fets during that interval. This gives an intuitive explanation and justification on the difference in the I and Q

outputs of the doubler. The similar explanation can be extended for the other muliplications of sin x sin and sin x cos and viceversa.

The equations 3.4, 3.5 and 3.6 also gives a mathematical justification for the difference in the behaviour of the fets in the passive mixer which does the multiplications sin x cos and sin x sin or sin x cos and cos x cos.

- Equation 3.4: $\sin(\omega_{in}t) \times \cos(\omega_{in}t) = 0.5 \times \sin(2\omega_{in}t)$
- Equation 3.5: $\sin(\omega_{in}t) \times \sin(\omega_{in}t) = 0.5 \times (\mathbf{1} - \cos(2\omega_{in}t))$
- Equation 3.6: $\cos(\omega_{in}t) \times \cos(\omega_{in}t) = 0.5 \times (\mathbf{1} + \cos(2\omega_{in}t))$

The term **1** in $1 \pm \cos(2\omega_{in}t)$ corresponds to the DC term and the term $\cos(2\omega_{in}t)$ corresponds to the doubled frequency term. We don't see any DC term when sin and cos are multiplied. There is a presence of DC term at the output when sin and sin are multiplied or sin and cos are multiplied. This explains the difference in the DC characteristics of the fets in the mixers.

Another important note here is that the above-given explanations doesn't seem to provide a strong justification as to why the supposed to be differential outputs are not differential in the sin x cos multiplication in the circuit shown in figure 3.4.1. The reason is that the mosfet in the mixer doesn't behave as an ideal switch, they do not switch abruptly. MOSFETs have a certain threshold voltage V_{th} and at higher frequencies, the LO waveforms inevitably resemble sinusoids rather than square waveforms. There is a period of time ΔT where both the LO and LO_{bar} varies gradually and their value is approximately equal, as shown in fig 3.6.3. During this time, all the four transistors are ON or OFF (depending on the DC voltage at the gate) treating the signal applied at the drain as a common mode. All these non-idealities bring a difference in the DC characteristics in the sin x cos multiplication also, but the difference here is small compared to sin x sin multiplication or cos x cos multiplication; which can be understood from the values of magnitudes of the outputs from the tables 3.1 and 3.2. Vo_1 and Vo_2 show a small difference in the output compared to the difference between the outputs Vx_1 and Vx_2.

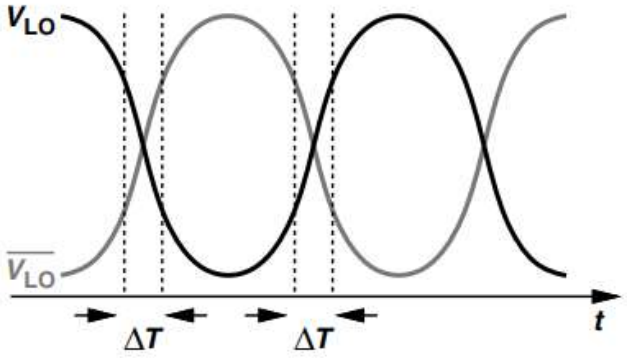


fig 3.6.3 LO waveforms showing when the switches are on or off simultaneously.

The difference in the supposed to be differential outputs, as seen in tables 3.1 and 3.2, vanishes i.e., the amplitudes are exactly the same and the phase difference is 180° when the frequencies of the input waveforms are different, which confirms the effect of the DC offset. Mathematically also the output frequencies are at $\omega_{in} \pm \omega_{LO}$ when ω_{in} and ω_{LO} are the input frequencies. When $\omega_{in} \neq \omega_{LO}$, we don't get any tone at DC.

3.7 DC biasing

For an n-channel MOSFET to conduct a significant amount of current, the condition is that it should be out of the cut-off mode of operation, which is the Gate-Source potential (V_{GS}) has to be greater than the threshold voltage (Vth) of the MOSFET i.e., $V_{GS} > Vth$. Hence the gate of the MOSFET is biased at a DC voltage such that the value of V_{GS} is close to Vth. Under this condition, when any sinusoidal input is applied at the gate, with the DC voltagebeing close to Vth, the value of V_{GS} will become greater than Vth during the positive half cycle of the sinusoid and the value of V_{GS} goes less than Vth during the negative half cycle of the sinusoid (with the assumption that the source voltage remains unchanged). Hence the transistor goes out of the cut-off region during the positive half cycle of the AC sinusoidal signal and it will be in the cut-off in the negative half cycle. For the MOSFET

biased in deep-triode, when V_{GS} > Vth: it conducts and it can be treated as a switch being on with very low on-resistance. When V_{GS} < Vth: it doesn't conduct (neglecting the sub-threshold conduction) which can be considered as a switch being off with very high off-resistance. Hence the gate of the transistor is biased at a particular DC voltage such that the value of V_{GS} is close to Vth. The drain can be biased at zero DC. Shown in figure 3.7.1 is the bias circuit used for the gate and drain terminals of the transistor in the passive mixer.

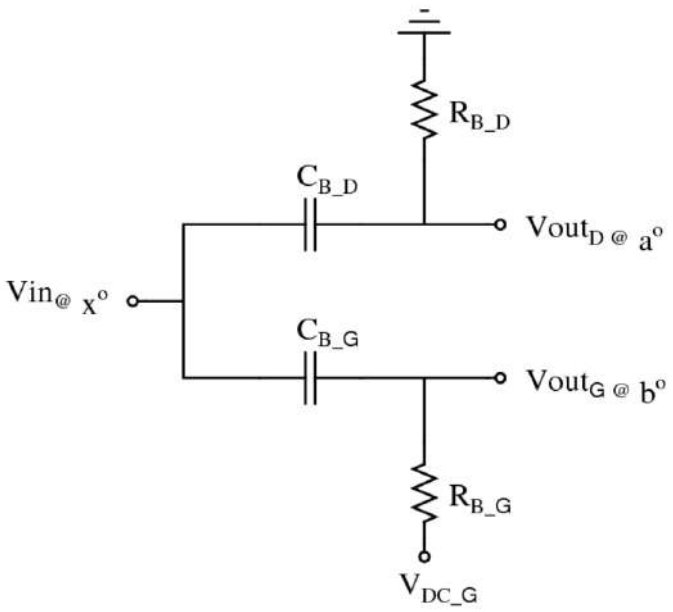


fig 3.7.1 Bias circuit for a particular phase of a LO signal is shown.

Note that in the figure 3.7.1, the phases at the nodes $Vout_D$ and $Vout_G$ are marked such that they have phases a^0 and b^0 respectively, which indicates that the phases at the nodes $Vout_D$ and $Vout_G$ need not be same eventhough the values of bias resistors and the AC coupling capacitors are exactly the same. It actually depends on the load at that particular node, shown in the figure 3.7.2. The analysis of phases and magnitudes can be obtained from writing the transfer function which will be dealt in the section 5.3.

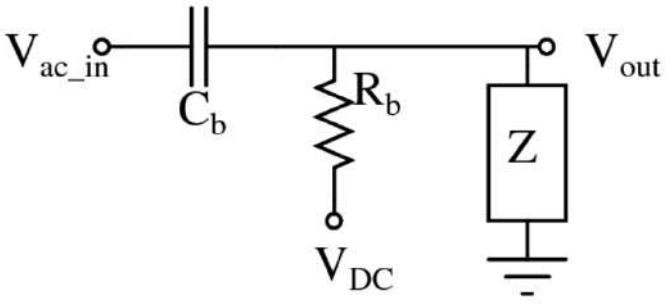


fig 3.7.2 Bias circuit and the load modelled as a block at the output of the bias circuit.

CHAPTER 4

ACTIVE MIXER BASED FREQUENCY DOUBLER

4.1 Theoretical Background

Active mixer, also popularly called a Gilbert Cell mixer, is a circuit that produces output voltage by multiplying the two input waveforms. For simplicity of understanding, let's say, V_{RF} and V_{LO} are the two input signals and V_{IF} is the output signal. Active mixers achieve conversion gain by performing three functions: they convert the RF voltage to a current, "commutate" (steer) the RF current by the LO, and convert the IF current to voltage. These operations are illustrated in Fig. 4.1.1.

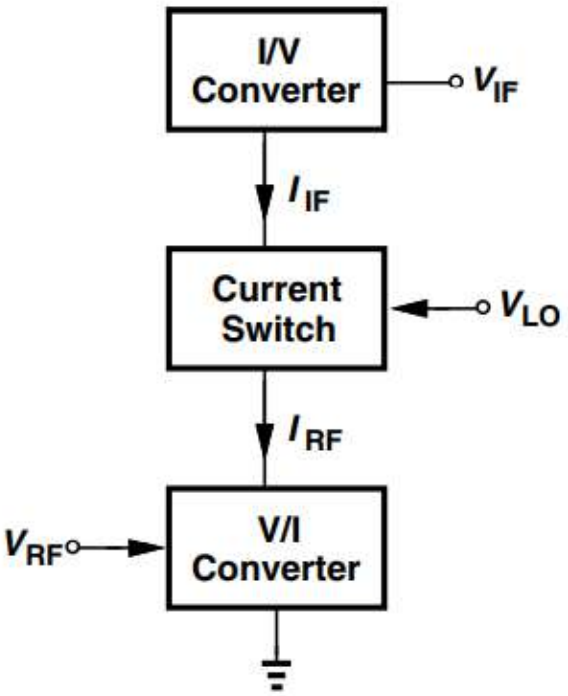


fig 4.1.1 Active mixer viewed as a V/I converter, a current switch, and an I/V converter.

Figure 4.1.2 depicts a typical single-balanced realisation of an active mixer. Here, M1 converts the input RF voltage to a current (and is hence called a “transconductor”), the differential pair M2–M3 commutates (steers) this current to the left and to the right, and R1 and R2 convert the output currents to voltage. We call M2 and M3 the “switching pair. We can observe that the input transconductance, I_{RF}/V_{RF}, and the output transresistance, V_{IF}/I_{IF}, can, in principle, assume arbitrarily large values, yielding a high gain. The LC load has only the real part as impedance at the resonance frequency, hence only a resistor is shown as the load in fig 4.1.2.

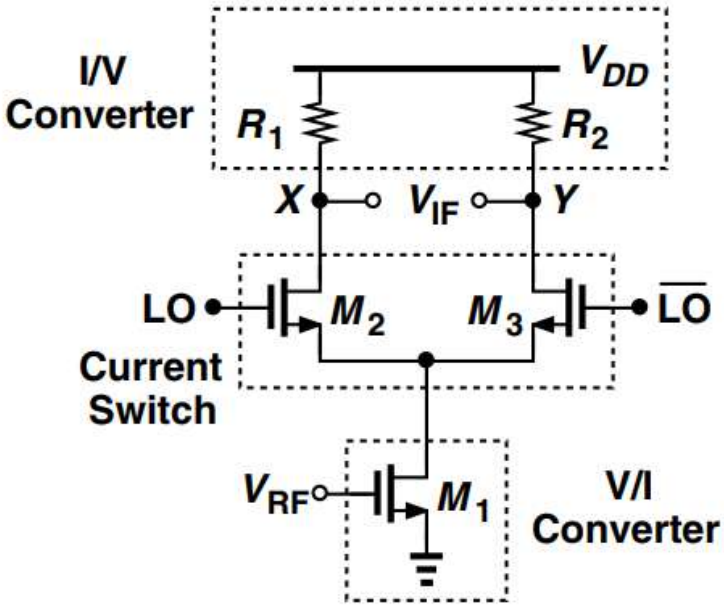


fig 4.1.2 Single balanced active mixer topology.

The current steering action in the LO current switch does the frequency translation. When V_{LO} is high value, all the current from the transconductance stage, I_{RF} flows through mosfet M2, as M3 is in the cutoff region (V_{LObar} is low, when V_{LO} is high, keeping the mosfet M3 in the cutoff region). During the period V_{LObar} being high, all the current flows through mosfet M3 and no current (almost no current, for a properly designed mixer) flows through mosfet M2. The frequency at which I_{RF} flows to the load is now translated by the frequency of V_{LO}. The entire mathematical analysis is

similar to the passive mixer case, the only difference is that in active mixer, the current is steered by the LO stage transistors where as in voltage mode passive mixer, the voltage gets sampled by the transistors.

4.2 The DC offset problem

The DC offset issue exists in both the active and passive mixer, when the frequencies of the input and the LO stages are same. In active mixer there are two stages where the DC offset can create problems; the transconductance stage and the LO stage. The DC characteristics of the transistors in these two stages will be different. Let us consider the AC input V_{RF} as a small signal AC. Therefore I_{RF} can be written as product of gm and the small signal input V_{RF}. The gm of a MOSFET is a function of the DC operating points.

$$I_{RF} = gm \, . \, V_{RF} \qquad \text{eqn (4.1)}$$

The LO stage fets steer the current into one direction when

$$V_{LO} > \sqrt{2} \, (V_{GS} - V_{th}) \text{ of the LO stage fets.}$$

Hence the effect of DC offset is much dominant in the active mixer case than the voltage mode passive mixer, where there is only one stage of MOSFETS involved. It becomes extremely challenging to correct the DC offset effect in case of active mixers eventhough it provides conversion gain. Hence the voltage mode passive mixer topology is implemented to doubler the frequency and the methods to reduce effect of DC offset are explained in the next chapter.

CHAPTER 5

THE I - Q IMBALANCE

5.1 What is I-Q imbalance?

In mixer operation, we get two frequencies $f_{LO} + f_{BB}$ and $f_{LO} - f_{BB}$ when baseband (frequency f_{BB}) and LO waveforms (frequency f_{LO}) are multiplied as shown in the equations 5.1, 5.2 and 5.3 or as explained in section 3.1.

$$\sin(\omega_{LO}t) \times \sin(\omega_{BB}t) = 0.5 [\cos((\omega_{LO}-\omega_{BB})t) - \cos((\omega_{LO}+\omega_{BB})t)] \quad \text{eqn(5.1)}$$

$$\cos(\omega_{LO}t) \times \cos(\omega_{BB}t) = 0.5 [\cos((\omega_{LO}+\omega_{BB})t) + \cos((\omega_{LO}-\omega_{BB})t)] \quad \text{eqn(5.2)}$$

$$\cos(\omega_{LO}t) \times \cos(\omega_{BB}t) = 0.5 [\sin((\omega_{LO}+\omega_{BB})t) + \sin((\omega_{LO}-\omega_{BB})t)] \quad \text{eqn(5.3)}$$

The frequencies $f_{LO} + f_{BB}$ and $f_{LO} - f_{BB}$ are very close enough and would fall within the bandwidth of any practically implementable filter with center frequency around f_{LO}. The frequencies $f_{LO} + f_{BB}$ and $f_{LO} - f_{BB}$ are separated by frequency $2f_{BB}$, whose value is very small compared to the LO frequency. The bandwidth (BW) of the filter would allow both the sidebands around LO to pass. When both these frequencies, $f_{LO} + f_{BB}$ and $f_{LO} - f_{BB}$, are transmitted; the receiver receives these two frequencies, which are very closeby. This leads to unwanted Intermodulation products and spurious tones, which can lead to signal desensitization and (or) signal blocking.

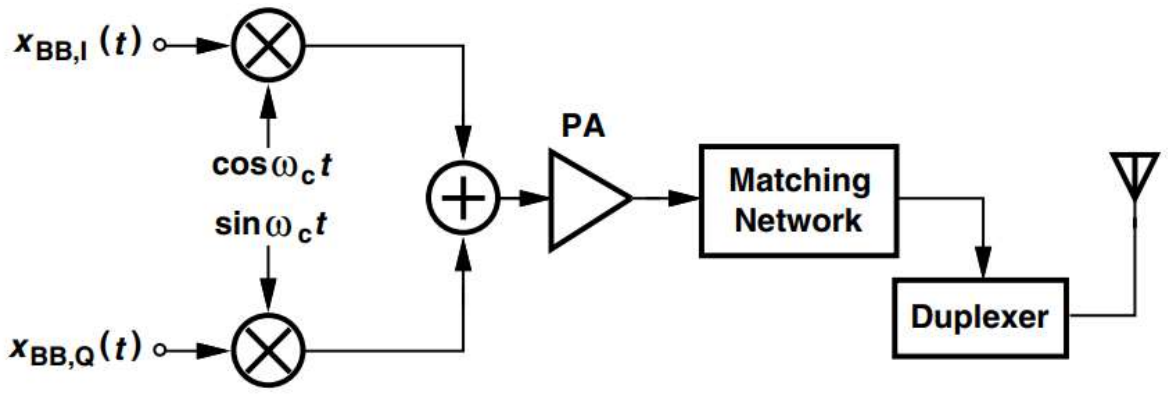


fig 5.1.1 Upconversion mixer architecture in a transmitter.

In order to transmit only one frequency, let's say we are targeting to transmit f_{LO} + f_{BB}, then we need to suppress the other sideband frequency f_{LO} - f_{BB}. The role of In-phase and Quadrature (I & Q) in the upconverter in the transmitter chain is to transmit the frequency of interest, in our case f_{LO} + f_{BB}, and to eliminate (or suppress) the other sideband frequency, which is f_{LO} - f_{BB}, generated in the mixing operation. Consider the architecture shown in figure 5.1.1. The signals $X_{BB,I}(t)$ and $X_{BB,Q}(t)$ are modulated (multiplied) with the I & Q LO signals and are summed up. This allows the transmitter to transmit only one frequency, as shown in equations 5.4 and 5.5. Either of these can be used depending on what frequency we want to transmit.

From equations 5.1 and 5.2, we can write

$$\sin(\omega_{LO}t) \times \sin(\omega_{BB}t) + \cos(\omega_{LO}t) \times \cos(\omega_{BB}t) = \cos((\omega_{LO}-\omega_{BB})t) \qquad \text{eqn(5.4)}$$

$$\cos(\omega_{LO}t) \times \cos(\omega_{BB}t) - \sin(\omega_{LO}t) \times \sin(\omega_{BB}t) = \cos((\omega_{LO}+\omega_{BB})t) \qquad \text{eqn(5.5)}$$

Now suppose, there is a small I-Q mismatch, which means I & Q phases in LO have a small phase imbalance of $\Delta\theta$ and gain mismatch of ε , this now translates to the output as shown in the equations below.

In ideal case, we have:

$$\text{Vout}(t) = \cos(\omega_{LO}t)\cos(\omega_{BB}t) - \sin(\omega_{LO}t)\sin(\omega_{BB}t) = \cos((\omega_{LO}+\omega_{BB})t)$$

Under phase and gain mismatch:

$$\text{Vout}(t) = (1+\varepsilon)\cos(\omega_{LO}t+\Delta\theta)\cos(\omega_{BB}t) - \sin(\omega_{LO}t)\sin(\omega_{BB}t) \qquad \text{eqn(5.6)}$$

$$= 0.5\,((1+\varepsilon)\cos(\Delta\theta) + 1)\cos((\omega_{LO}+\omega_{BB})t)$$

$$- 0.5\,(1+\varepsilon)\sin(\Delta\theta)\sin((\omega_{LO}+\omega_{BB})t)$$

$$+ 0.5\,((1+\varepsilon)\cos(\Delta\theta) - 1)\cos((\omega_{LO}-\omega_{BB})t)$$

$$- 0.5\,(1+\varepsilon)\sin(\Delta\theta)\sin((\omega_{LO}-\omega_{BB})t) \qquad \text{eqn(5.7)}$$

It follows that the power of the unwanted sideband at $\omega_{LO} - \omega_{BB}$ divided by that of the wanted sideband at $\omega_{LO} + \omega_{BB}$ is given by

$$P_{LO-BB} / P_{LO+BB} = [\{(1+\varepsilon)\cos(\Delta\theta)-1\}^2 + \{(1+\varepsilon)\sin(\Delta\theta)\}^2] / [\{(1+\varepsilon)\cos(\Delta\theta)-1\}^2 + \{(1+\varepsilon)\sin(\Delta\theta)\}^2]$$

$$= [(1+\varepsilon)^2 - 2(1+\varepsilon)\cos(\Delta\theta) + 1] / [(1+\varepsilon)^2 + 2(1+\varepsilon)\cos(\Delta\theta) + 1] \quad \text{eqn(5.8)}$$

When ε is zero:

$$P_{LO-BB} / P_{LO+BB} = (1 - \cos\Delta\theta) / (1 + \cos\Delta\theta) \quad \text{eqn(5.9)}$$

$$= \sin^2(\tfrac{\Delta\theta}{2}) / \cos^2(\tfrac{\Delta\theta}{2})$$

$$= \tan^2(\tfrac{\Delta\theta}{2}) \quad \text{eqn(5.10)}$$

The phase difference between the I and Q of LO waveform reflects in the difference in the power levels of the frequencies generated in the upconversion mixer. This difference, when mentioned in dB scale is quoted as a metric or measure of I-Q imbalance in the transmitter. The specification is that the I-Q imbalance to be lower than -40 dB.

5.2 I-Q imbalance in an ideal system

Consider the schematic shown in figure 5.2.1, where only ideal components are used and the I-Q imbalance is analysed. The parameters of the ideal components are adjusted such that it mimics the pre-designed up converter mixer of the transmitter chain. The plot in figure 5.2.2 shows the simulated I-Q imbalance with the ideal components in place of transistors with all the four phases of LO inputs having same amplitude and the phases being 0^0, 180^0, $(90+x)^0$, $(270+x)^0$ and x is varied from -2 to +2. Here differential nature is maintained but the phase difference between the I and Q vary from 88^0 to 92^0. The results says that a difference in 2^0 phase difference between the I and Q phases would drop the I - Q imbalance of the system to -36 dB.

The simulation result shown in figure 5.2.3 corresponds to the case where the phases are 0^0, 180^0, $(90+x)^0$, 270^0 and the amplitudes being same

for all the four phases. Here the phase of only one of the LO is swept where as in previous case, the phases of one of the differential sets is swept together without any disturbance to the differential behaviour.

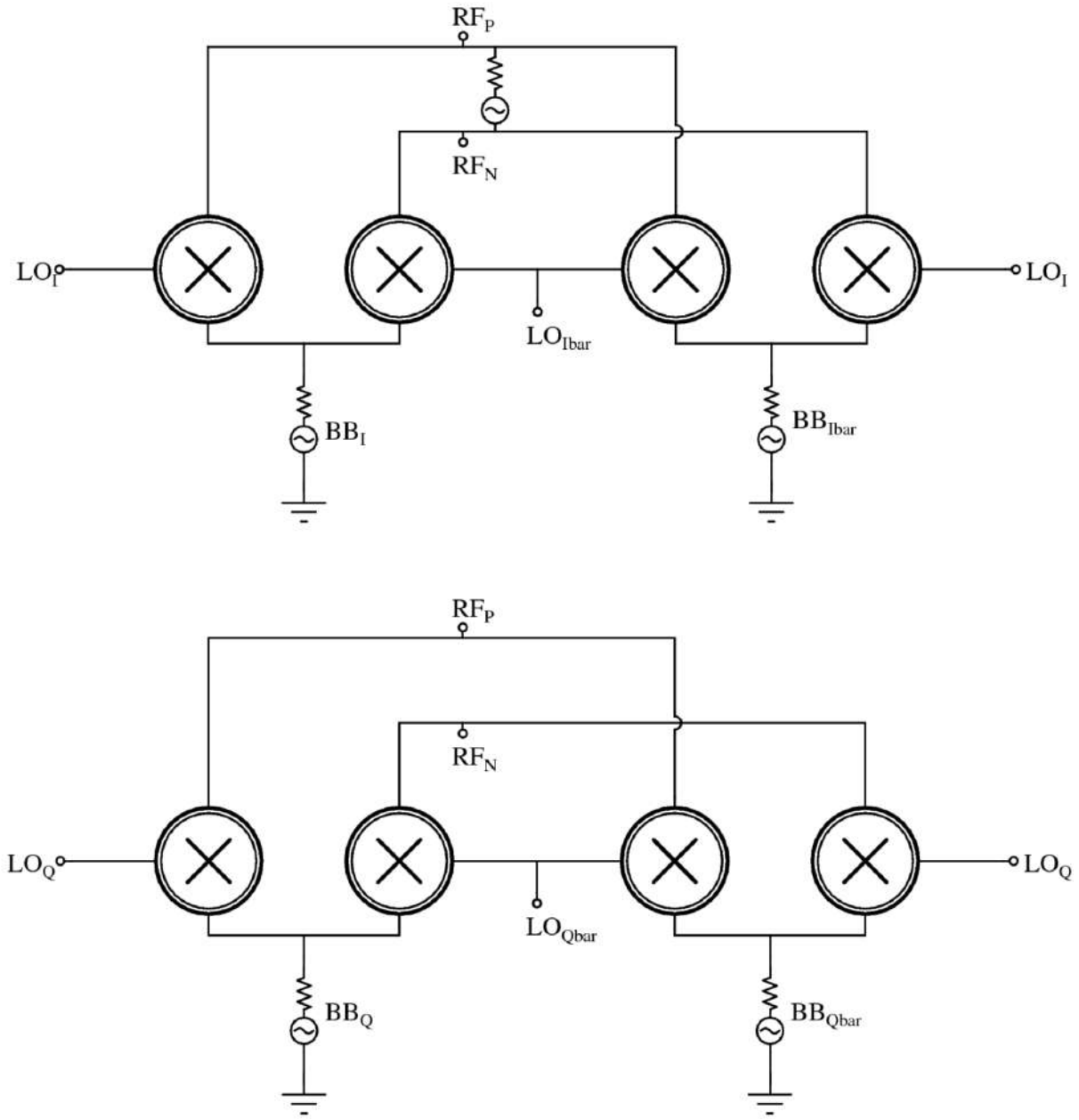
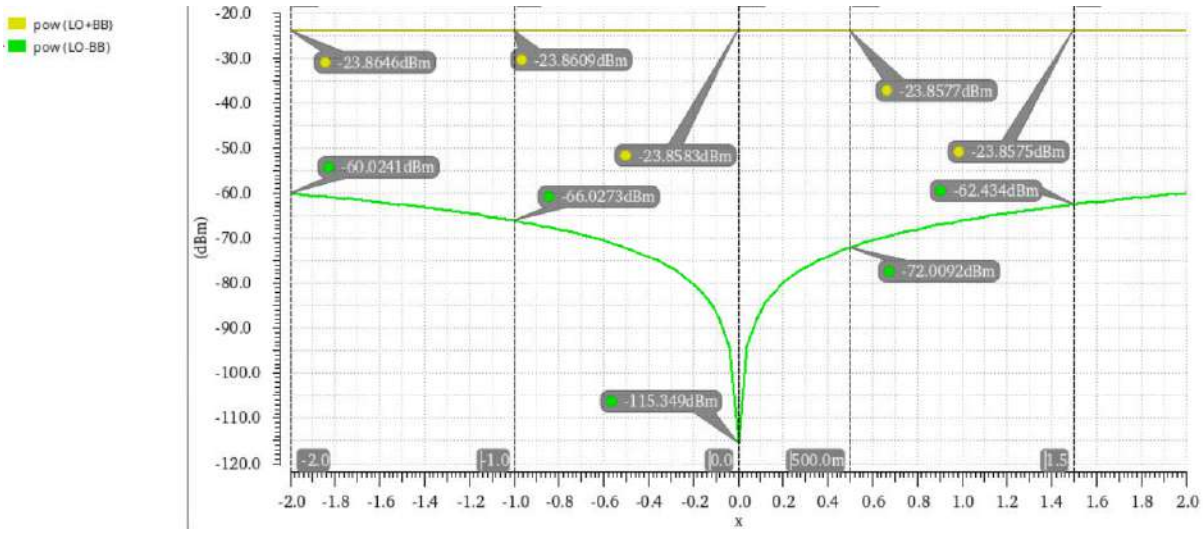
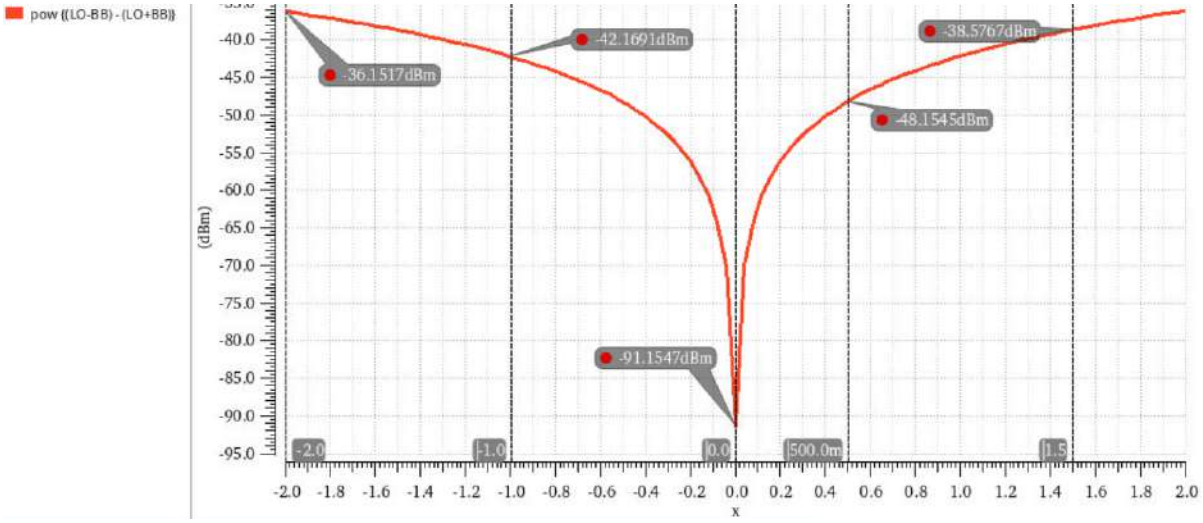


fig 5.2.1 Mixer realized with ideal instances.



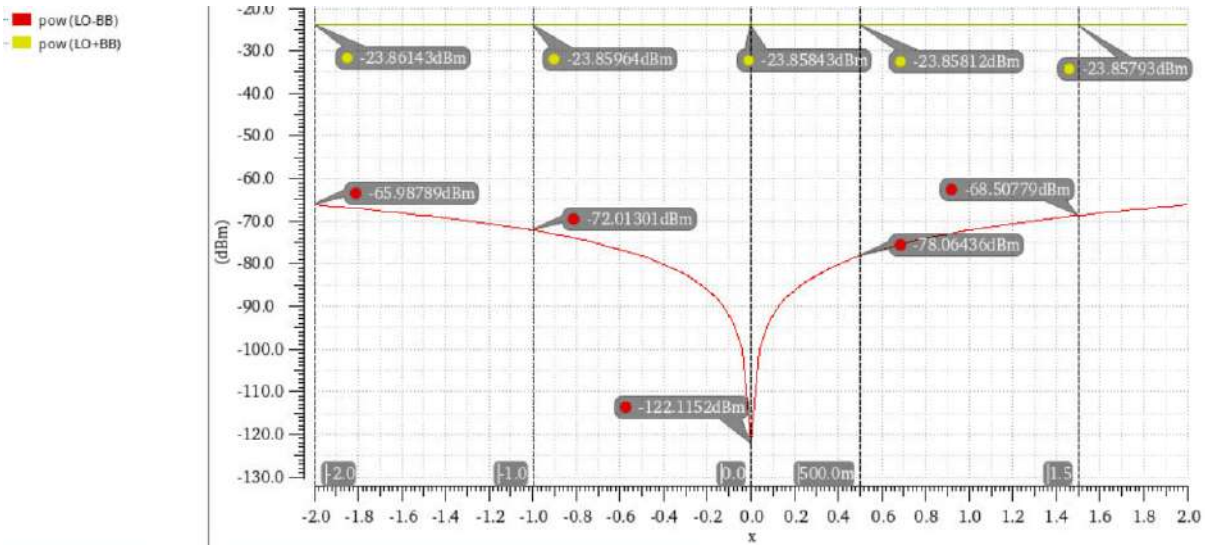
(a)

Fig 5.2.2 (a) power levels of LO+BB and LO-BB signals, when the phases are 0^0, 180^0, $(90+x)^0$, $(270+x)^0$.



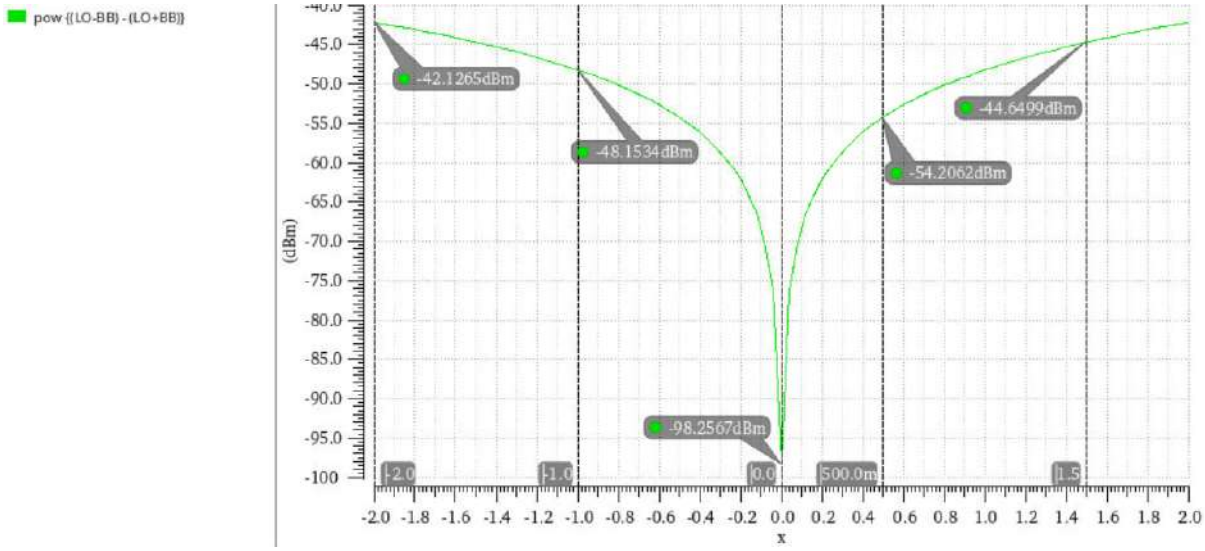
(b)

fig 5.2.2 (b) the difference in the power levels of LO-BB and LO+BB, when the phases are 0^0, 180^0, $(90+x)^0$, $(270+x)^0$.



(a)

Fig 5.2.3 (a) power levels of LO+BB and LO-BB signals, when the phases are 0^0, 180^0, $(90+x)^0$, 270^0.



(b)

fig 5.2.3 (b) the difference in the power levels of LO-BB and LO+BB, when the phases are 0^0, 180^0, $(90+x)^0$, $(270+x)^0$.

5.3 The difference in I & Q amplitudes

The conclusion from section 3.6 is that the difference in the I and Q amplitudes is an effect of the DC offset, due to the multiplication of the same frequencies, which differs the DC characteristics and properties of the transistor. The role of the MOSFET in the voltage mode passive mixer is to act as a switch controlled by a terminal called Gate. The dominant DC parameter that controls the amplitudes is the on-resistance (Ron) of the switch, which is realised using the transistor in the triode (linear) region of operation, fig 5.3.1. An inductor resonates out the parasitic capacitances of the transistor at the load, so the parasitic capacitances is a less dominant contributor to the difference in the amplitudes and phases at the output.

The On-resistance of an n-channel transistor is given by:

$$Ron = L / \{ u_n Cox\ W\ (V_{GS} - Vth - V_{DS}) \} \qquad \text{eqn(5.11)}$$

fig 5.3.1 MOSFET being used as variable resistor.

If the DC voltage at the gate is varied, it alters the Ron and the other DC characteristics of the transistor, which can bring the I and Q amplitudes equal but at the cost of phase imbalance as shown in the figure 5.2.2. There is a trade-off between the amplitudes and phases of the I and Q outputs with the change in the DC voltage at the gates. In the final implementation, the DC voltage at the gates of the I and Q outputs producing mixers is given an off-chip control to adjust the DC value accordingly.

Note that the amplitudes shown in the figure 5.3.2 much are greater than the ones mentioned in the table 3.3. A CSA buffer is used after the passive mixer stage and the plot shown in the figure is the simulation result

at the final schematic stage. The reason for using a buffer after the passive mixer is explained in the next section.

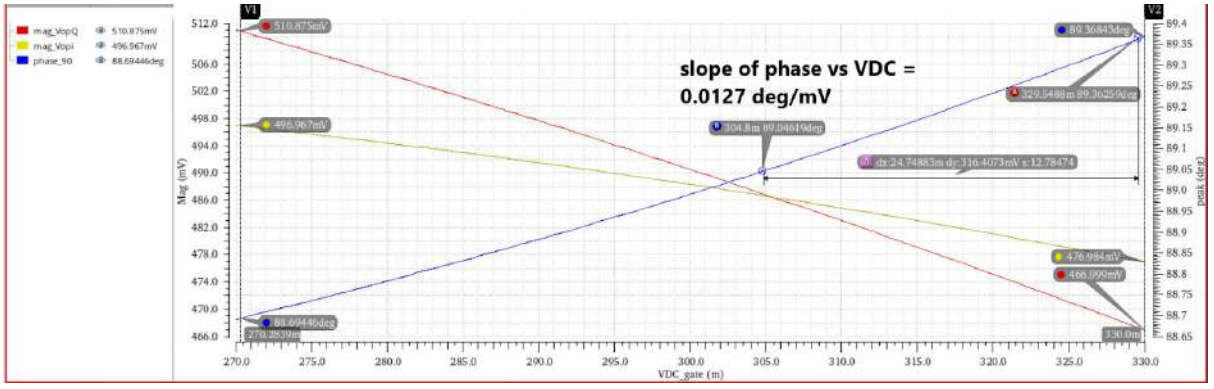


fig 5.3.2 variation of I and Q amplitudes and the I-Q phase w.r.t V_{DC_gate}.

5.4 Sizing the mosfets of the passive mixer

The phase and amplitude imbalance in the frequency doublers is explained by the DC offset phenomenon in the section 3.6. The figures from the previous sections are iterated here for the simple flow of analysis and understanding. The final passive mixer circuit that is implemented is shown in the figure 5.4.1 and 5.4.2. Let's call the circuit that produces I outputs as I-mixer and the circuit that produces Q outputs as Q-mixer. Each phase of the LO sinusoidal signal goes to two gates and two drain in each of the I and Q mixers. There is only one seperate set of bias capacitor and resistor for each phase of the LO waveform that goes to gate and drain of the transistor. In other words, 0^0 sinusoid goes to a total of four drains and four gates. There is only one bias circuit for the 0^0 LO sinusoidal signal that goes to the drain and one bias circuit for the one that goes to the gates. There is no necessity to use four bias circuits for the signal that goes to the four gates or the four drains in total. The bias circuit for a particular phase of LO waveform is shown in the figure 5.4.3.

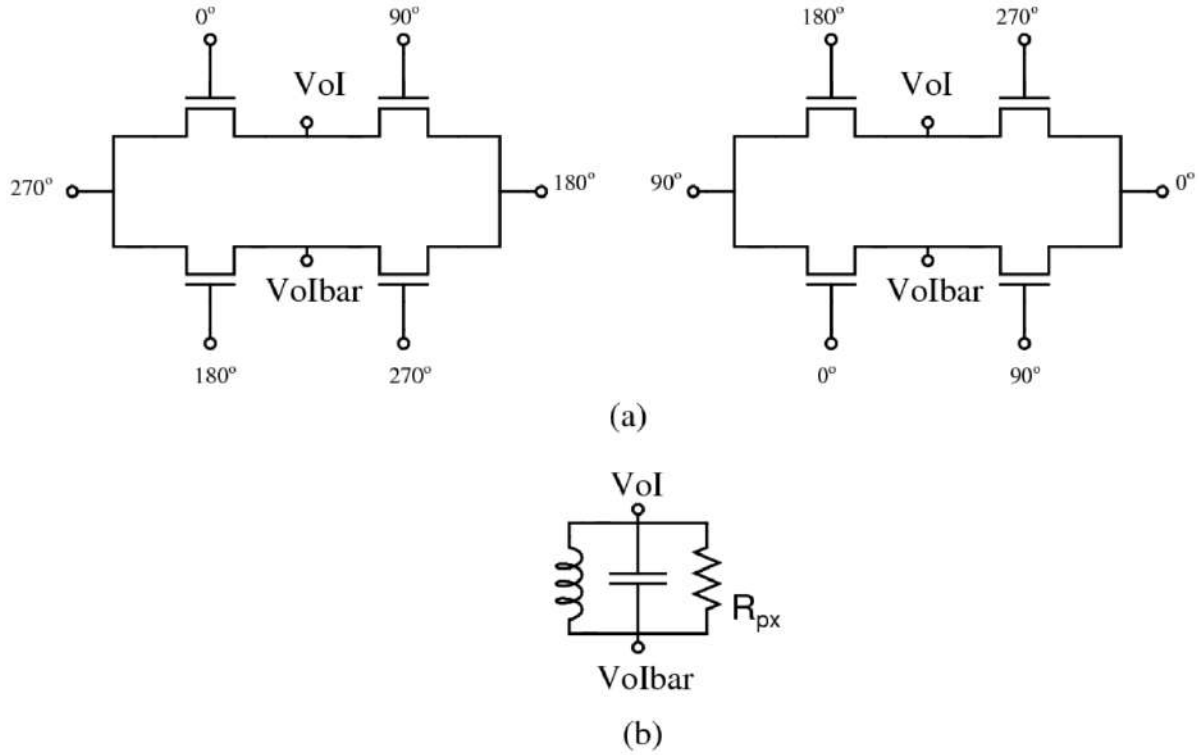


fig 5.4.1 I mixer: (a) switching stage (b) load

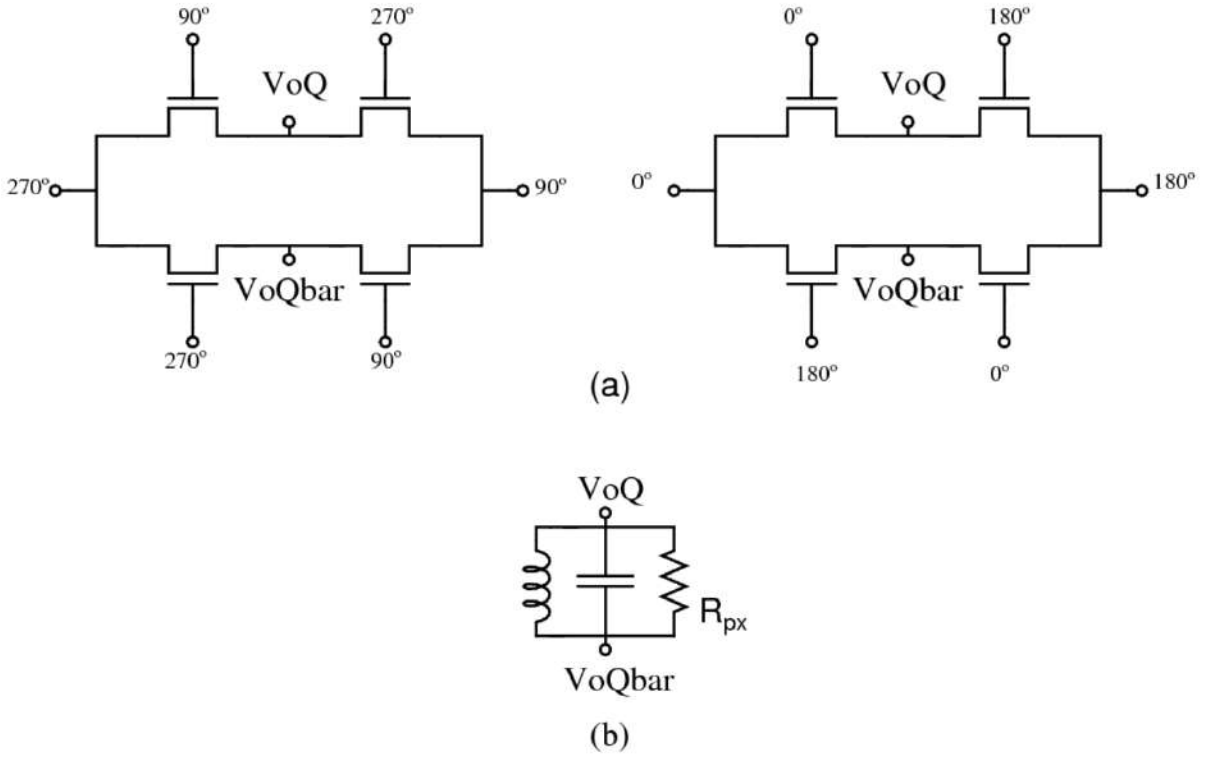


fig 5.4.2 Q mixer: (a) switching stage (b) load

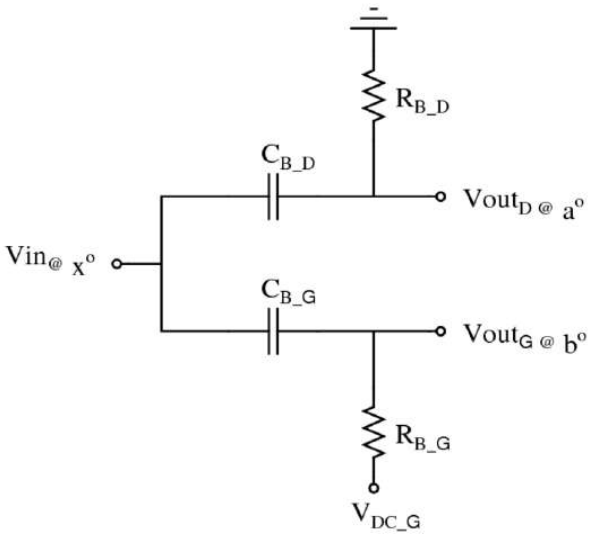


fig 5.4.3 Bias circuit for a particular LO phase.

5.4.1 The transfer function at the gate side

Let's write the transfer function from Vin to $Vout_G$. To analyse the transfer function from Vin to $Vout_G$, it is sufficient if we replace the load shown in the figure 5.4.4 with an appropriate and effective model. Here let's try analyse the I and Q mixers separately, without any connection between i.e., the bias circuits are also different for the I and Q mixers. The gate looking in of a MOSFET can be simply modelled as a combination of gate resistance and the parasitic capacitors as shown in the figure 5.4.5 (a). In reality, it is a complicated R-C ladder model. The bulk of the n-channel MOSFET is connected to the lowest available potential i.e., ground. The gate resistance of the transistor can be neglected from the analysis, which makes the gate looking-in capacitive and the effective capacitive is termed as C_{gg}, as shown in the figure 5.4.5 (b). The load shown in the figure 5.4.4 can be replaced with a capacitor of value twice the value of C_{gg}, as shown in figure 5.4.6, as C_{gg} is the effective gate looking in capacitance of one transistor and the output $Vout_G$ goes to the two gates each in I and Q mixers. Let's call the total capacitance as Cg_{total}.

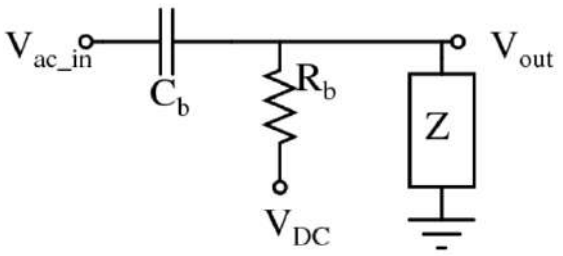


fig 5.4.4 Bias circuit and load at the output node.

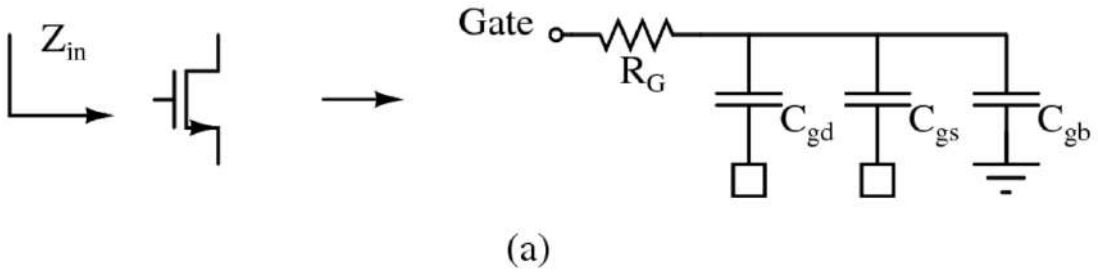


fig 5.4.5 (a) Simple model of a gate looking-in impedance of a transistor.

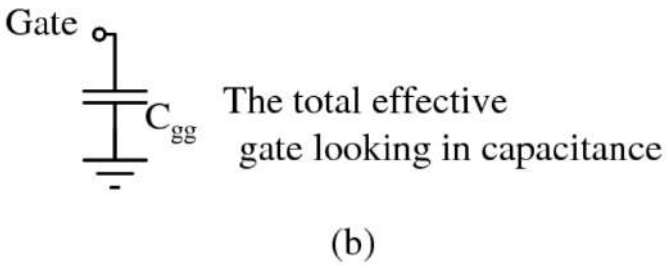


fig 5.4.5 (b) effective model of a mosfet looking in from gate side.

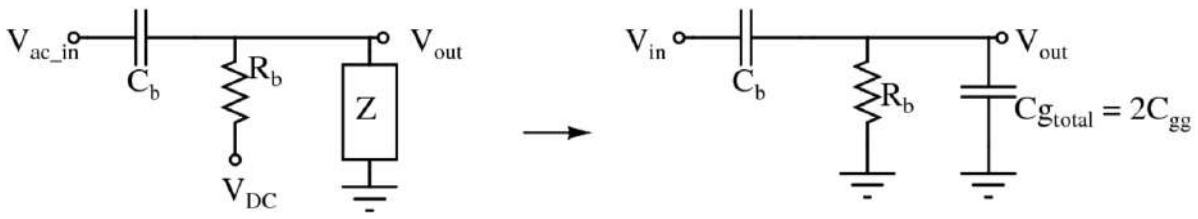


fig 5.4.6 Bias circuit and the gate looking-in modelled.

The transfer function from Vin to Vout can be written by writing KCL or KVL equations and the transfer function is given in the equation 5.12

$$H_{gate}(s) = \frac{Vout(s)}{Vin(s)} = (s\ C_b\ R_b) \ /\ \{\ 1+s(C_b+Cg_{total})\ R_b\} \qquad \text{eqn(5.12)}$$

Let the bias capacitor, C_b, be 1 picofarad and the bias resistor, R_b, be 10 kohms and the total parasitic capacitance from the gates be 100 femtofarads i.e., Cg_{total} = 100 fF. Then the magnitude of $s(C_b+Cg_{total})\ R_b$ at s = jω and at a frequency = 13 GHz is 898.49.

Therefore the magnitude of the transfer function $H_{gate}(s)$ at s = jω and at 13 GHz is very close to 1.

$$|H(j\omega)| \sim 1$$

The phase of $H(j\omega) = 90^0 - \tan^{-1}(\omega\ (C_b+Cg_{total})\ R) = 0.063^0$, which is very close to zero degrees.

Therefore we can consider that the signal at the input of the circuit shown in the figure 5.4.6 is almost equal to the signal at the output. The magnitude and the phase of the transfer function are very close to one and zero respectively, which says that the Vout is very close to the Vin both in terms of magnitude and phase.

5.4.2 The transfer function at the drain side

Similar to the analysis in the section 5.4.1, the transfer function from Vin to $Vout_D$ can be written by replacing the load shown in figure 5.4.4 with an appropriate model. Consider the circuit shown in figure 5.4.7 (a), which shows the drain looking-in view of a balanced passive mixer topology. When LO is high, the switch realised using the MOSFET modelled as a combination of resistance Ron and the effective parasitic capacitance C_{ddon}, as shown in the figure 5.4.7 (b). LO_{bar} is low, so the corresponding transistor can be modelled as a combination of resistance Roff and capacitance C_{ddoff}.

The desired mode of operation is that at any instant either LO is high or LO_{bar} is high. Therefore the effective drain looking-in circuit can be modelled as shown in the figure 5.4.7 (c), with an assumption that the AC voltage at the output node is not dependent on the voltage at the drain and therefore it can be grounded.

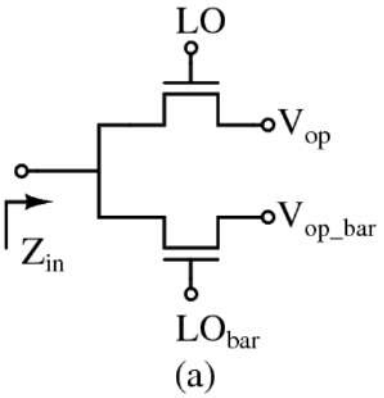


fig 5.4.7 (a) Drain looking-in of a single or double balanced passive mixer.

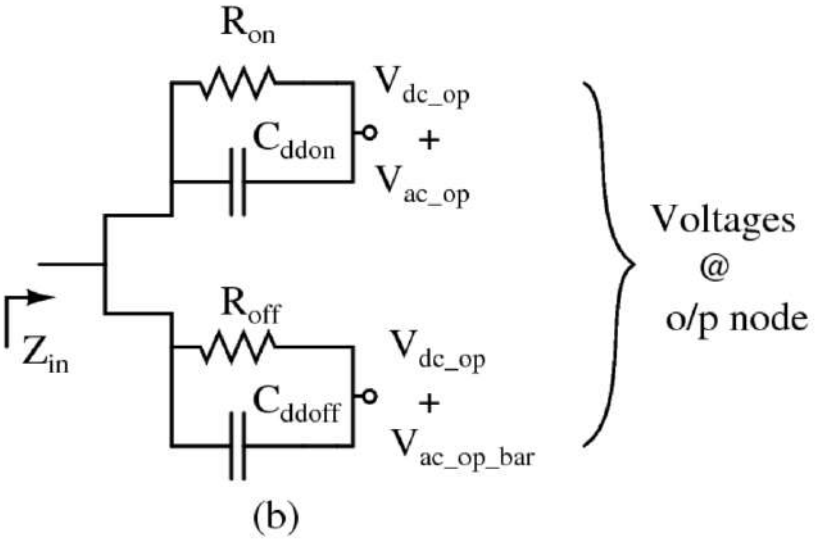


fig 5.4.7 (b) Transistors modelled as a combination of resistance and capacitance.

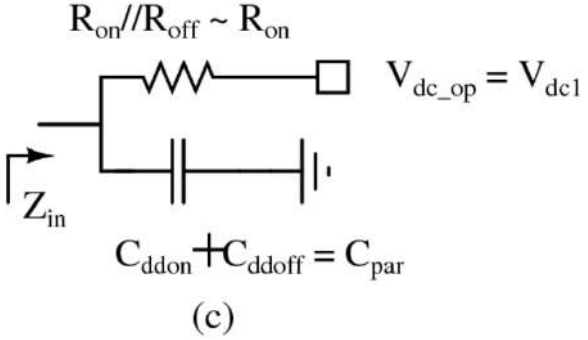
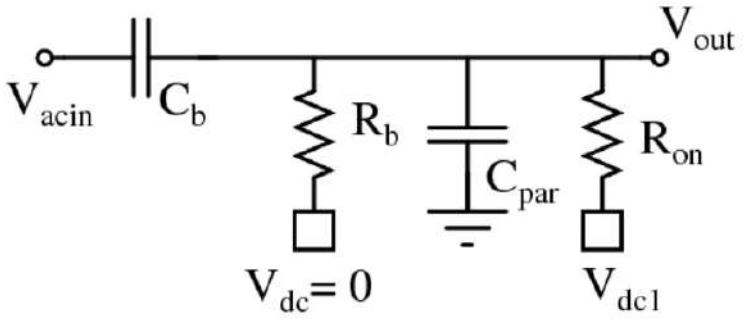


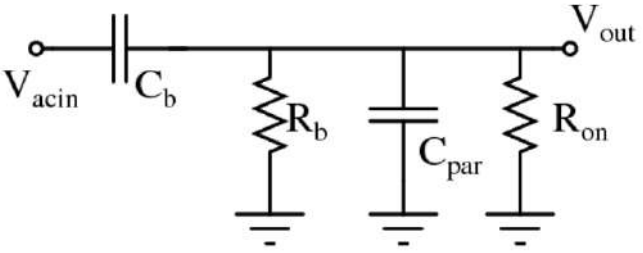
fig 5.4.7 (c) effective drain looking in model

Shown in figure 5.4.8 (a) is the circuit where the load shown in figure 5.4.4 is replaced with the equivalent model of drain looking-in at the either of I or Q mixer. Each phase of LO signal see two drains in the I and Q mixer each, the equivalent model shown in the figures 5.4.8 are complete models. The figure 5.4.8 (b) is the circuit for AC analysis, where the DC source or the signal can be grounded.



(a)

fig 5.4.8 (a) Bias circuit and the gate looking-in modelled.



$R_{on}//R_b \sim R_{on}$

(b)

fig 5.4.8 (b) Bias circuit and the gate looking-in modelled for ac analysis.

The transfer function from Vin to Vout is given in the equation 5.13.

$$H_{drain}(s) = V_{out}(s) / V_{in}(s) = (s\ C_b\ R_{on}) / \{ 1+s(C_b+C_{par})\ R_{on}\} \qquad \text{eqn(5.13)}$$

Let Ron = 50 Ohms. Therefore at 13 GHz the value of $(\omega R_{on} C_b) = 18.389$.

Then the magnitude of the transfer function at 13 GHz is 0.93 which is less than 1.

Phase of $H(j\omega) = 90 - \tan^{-1}(\omega (C_b+C_{par}) R_{on}) = 13.12$ degrees.

This shows that the phase of the transfer function is a strong function of C_b, C_{par} and R_{on}. As the DC characteristics are different for I and Q mixers, the phases at the drains can be different. This makes the phases of $H(j\omega)$ different at the drains of the I and Q mixers different from each other. Let the phase difference be $\Delta\theta$ i.e., the LO waveform at the drains of the Q mixer has an additional phase of $\Delta\theta$ over the phase of LO waveform at the drains of the I mixer. That difference in the phase translates to the output as shown in equations below.

$$\sin(\omega_{in}t) \times \cos(\omega_{in}t) = 0.5 \times \sin(2\omega_{in}t) \qquad \text{eqn(5.14)}$$

$$\sin(\omega_{in}t) \times \sin(\omega_{in}t + \Delta\theta) = 0.5 \times \{\cos(\Delta\theta) - \cos(2\omega_{in}t + \Delta\theta)\} \qquad \text{eqn(5.15)}$$

$$\cos(\omega_{in}t) \times \cos(\omega_{in}t + \Delta\theta) = 0.5 \times \{\cos(\Delta\theta) - \cos(2\omega_{in}t + \Delta\theta)\} \qquad \text{eqn(5.16)}$$

As shown in the equations 5.15 and 5.16, there is a DC term $\cos(\Delta\theta)$ and the phase of the cosine has a phase offset of $\Delta\theta$. The I-Q phase has an offset of $\Delta\theta$ from it's ideal value (90^0). Minimising the contribution of the DC parameters of the transistors will minimise the phase offset $\Delta\theta$. The phase of the transfer function depends on $\tan^{-1}(\omega(C_b+C_{par})R_{on})$. To lower effect of the subtle differences in the values of C_{par} and R_{on} on the values of the phase, the value of $\tan^{-1}(\omega(C_b+C_{par})R_{on})$ should be larger, which can be explained from the $\tan^{-1}$ x plot shown in the figure 5.4.9. As the value of x increases, the slope of $\tan^{-1}$ x decreases, which indicates that the values of $\tan^{-1}$x differs by a small value for different values of x. So the value $(C_b+C_{par})R_{on}$ should be increased. The value of C_b is depended on several factors from the

layout such as area, self resonant frequency (S_{RF}) and the quality factor (Q) of the capacitor. So the value of C_b cannot be increased after a certain limit.

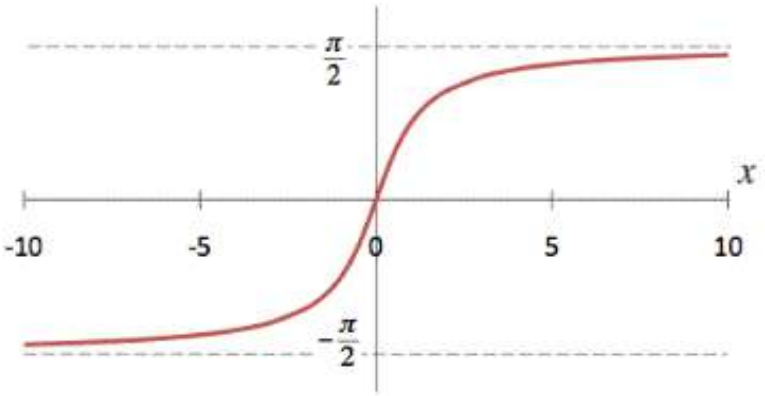


fig 5.4.9 Plot of $\tan^{-1} x$

The other factors that can be increased are the On-resistance or the parasitic capacitance from the transistor. For larger parasitic capacitance, we need larger device sizes. For larger Ron, the W/L ratio of the transistor has to be smaller. This is a trade-off between Ron and C_{par} values, larger device sizes versus smaller device sizes. The simulations for the phases at the output of the frequency douber, I-Q imbalance and the mismatch analysis shows that a larger Ron helps in achieving better phases and lower standard deviation for the I-Q imbalance over larger C_{par} value. Hence the transistors are sized at minimum width and lengths which gives lower parasitic capacitance and larger Ron. Having lower parasitics can be justified from the argument that in the transfer function analysis so far, the parasitic capacitances are considered as a simple capacitor from drain terminal to ground. In reality the capacitance exits between the drain-gate, drain-source and drain-bulk terminals. All these terminals increase the interactions between the terminals, which increases the leakage and non-linearities of the system. Smaller device sizes reduces the parasitics. The increase in Ron reduces the amplitude of the output voltages at 26 GHz. Hence a CSA buffer is used to increase the amplitudes of the LO waveform. This buffer drives the upconverter in the tranmsitter chain, which is a Gilbert cell mixer. The looking-in impedance of the Gilbert cell mixer is nothing but Gate looking-in. The LO switching stages are typically largely

sized to reduce the overdrive voltage of the transistor. Hence the parasitic capacitance Cgg is very large, which loads the CSA buffer. The parasitic capacitances are resonated out with an indutor at the load.

5.5 Mismatch analysis

Monte carlo simulations are run to ensure that the worst case I-Q imbalance is within the tolerance limits. Lowering the device sizes ensures that any small changes or mismatches in the DC parameters of the transistors would not translate as a bigger I-Q phase imbalance at the output of the buffer. The following is a derivation of probability distribution function of the I-Q imbalance. Let's assume that the difference in I-Q phase is a gaussian distribution when a large number of points are taken into consideration for the random and statistical mismatch simulations using monte carlo analysis. From the figures 5.2.2 (b) and 5.2.3 (b), the behavior of I-Q imbalance vs the phase mismatch can be consider as Y = - k/|X|, where K is a positive constant, Y is random variable corresponding to the I-Q imbalance and X is the random variable corresponding to phase mismatch. For simplicity of analysis, let k be 1.

$$\begin{aligned} &Let \quad Y = \frac{1}{X} \\ &and \quad X = X_1 - 90^o \\ &\qquad X = G(0, \sigma) \qquad (zero\ mean\ Gaussian) \end{aligned}$$

Then the Probability Distribution Function (PDF) of X is :

$$PDF(X) = \frac{1}{\sqrt{2\pi\sigma^2}}\ e^{-x^2/(2\pi\sigma^2)} \qquad \text{eqn(5.17)}$$

The Cumulative Distribution Function (CDF) of X is :

$$P(X <= x) = \int_{-\infty}^{x} pdf(x)dx \qquad \text{eqn(5.18)}$$

The probability of X being greater than or equal to - x is

$$P(X >= -x) = 1 - \int_{-\infty}^{x} pdf(x)dx \qquad \text{eqn(5.19)}$$

The CDF of Y is:

$$\begin{aligned} P(Y <= k) &= P(\frac{1}{x} <= k) \\ &= P(x >= \frac{1}{k}) \\ &= P(x <= \frac{-1}{k}) \end{aligned} \qquad \text{eqn(5.20)}$$

From this, the PDF of Y is:

$$PDF(Y) = \frac{1}{\sqrt{2\pi\sigma^2}}\ e^{-(-1/k)^2/(2\pi\sigma^2)} \qquad \text{eqn(5.21)}$$

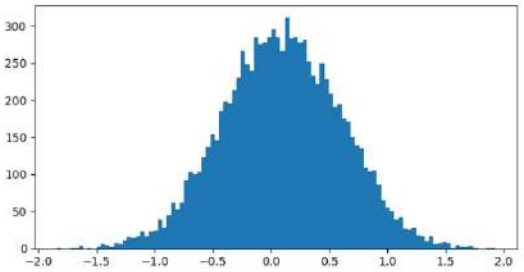
The random variable we have is Y = 1/ |x|

$$Let \quad Y = \frac{1}{\text{mod } X} \qquad (modulus\ of\ X)$$

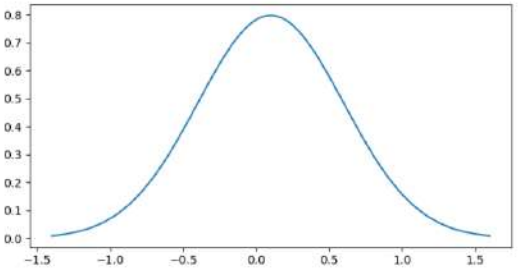
This implies that for each value of Y = k, there are two values of x which are 1/k and -1/k. The PDF of a gaussian distribution is symmetric around its mean. Therefore the PDF of X is symmetric around X = 0, which implies that the probability of X = 1/k and X = -1/k are same.

$$\begin{aligned} Then\ \ P(Y = k) &= 2P(x = \frac{1}{k}) \\ Therefore\ \ PDF(Y) &= 2\frac{1}{\sqrt{2\pi\sigma^2}}\ e^{-(-1/k)^2/(2\pi\sigma^2)} \end{aligned} \qquad \text{eqn(5.22)}$$

Shown in figure 5.5.1 is a graph of 4000 random points generated, which corresponds to the random variable X. The figure 5.5.2 is a pdf of a gaussian distribution. The figure 5.5.2 is an outline representation of the figure 5.5.1.

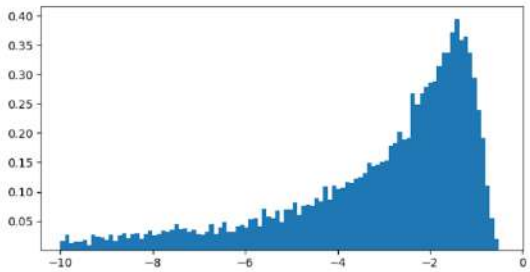


5.5.1 random distribution.

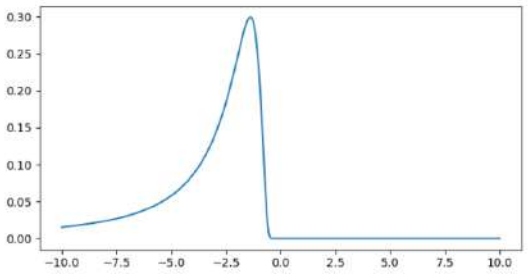


5.5.2 pdf of a gaussian distribution.

Shown in figure 5.5.3 is the distribution generated with Y = - 1 / |X| and X being a 4000 random points generated (shown in fig 5.5.1) and the graph shown in figure 5.5.4 is generated based on the equation 5.22.

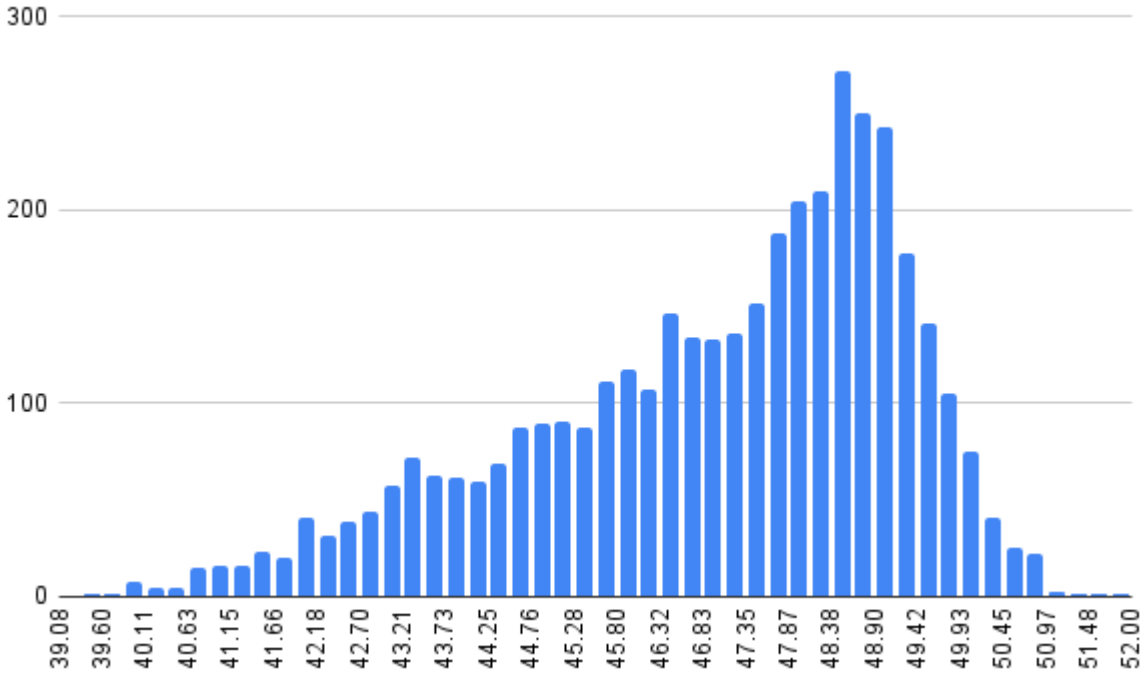


5.5.3 Distribution of Y = - 1 / |X|, where X is random variable.



5.5.4 PDF from the equation 5.22

The result from the montecarlo analysis for the frequency doubler integrated with the transmitter is shown in the figure 5.5.5. The shape or the outline of the distribution looks similar to the distributions shown in the figures 5.5.3 and 5.5.4. This confirms our initial assumption of phase imbalance being a gaussian distribution.



5.5.5 Distribution of I-Q imbalance from Monte Carlo simulation

CHAPTER 6

LAYOUT CONSIDERATIONS

6.1 Layout parasitics considerations

The layout parasitics from the metal layers were analysed and these parasitics are included in the schematic simulations to analyse their effect. The layout parasitics are modelled with inductors and capacitors (lumped elements). A long metal wire would have a considerable amount of inductance and parasitic capacitance to the ground. So it is modelled with a simple inductor-capacitor model. Now consider the circuit shown in fig 6.1.1 (a). The looking in impedance of a CSA is capacitive, considering the series resistance that comes from the gate resistance to be a small value. Let's call the effective gate looking in capacitance Cgg.

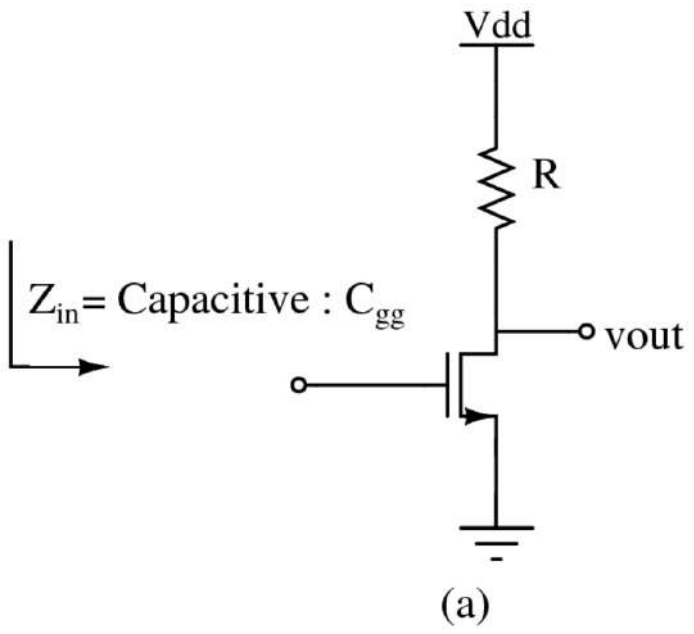


fig 6.1.1 (a) Looking-in impedance of CSA buffer with metal routing

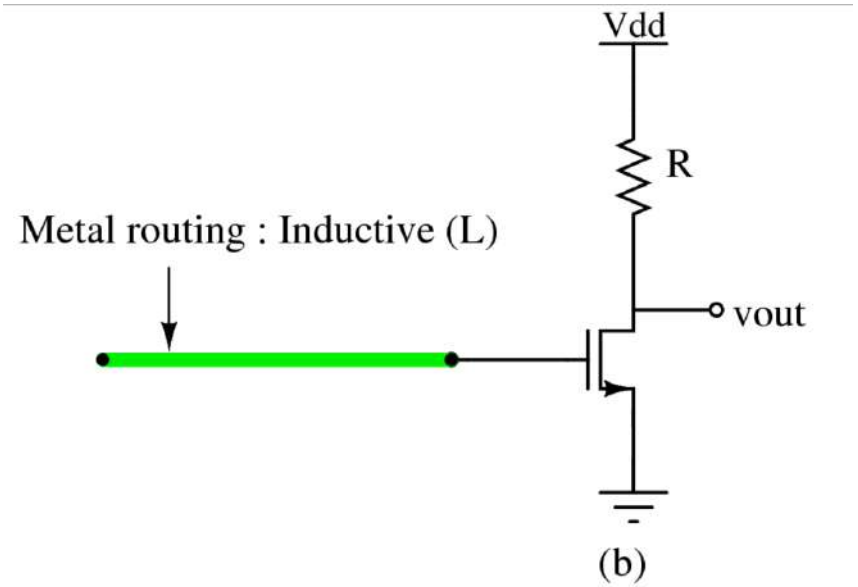


fig 6.1.1 (b) a metal connection to the gate of the buffer shown in green.

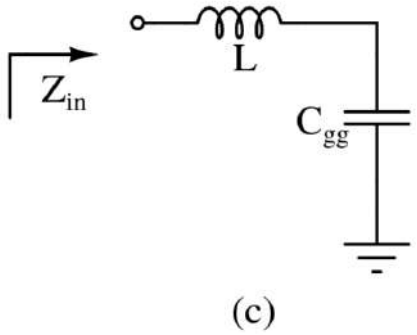


fig 6.1.1 (c) metal connection modelled as inductance 'L'

If a metal wire is connected to this buffer and the model metal wire is modelled as an inductor as shown in figure 6.1.1 (b), then the looking in impedance can still be capacitive but the value of capacitance is larger than Cgg as shown in equation 6.2.

$$\begin{aligned} Z_{in} &= jwL + \frac{1}{jwC_{gg}} \\ &= \frac{1 - w^2 LC_{gg}}{jwC_{gg}} \\ &= \frac{1}{jw\dfrac{C_{gg}}{1 - w^2 LC_{gg}}} \end{aligned}$$

eqn(6.1)

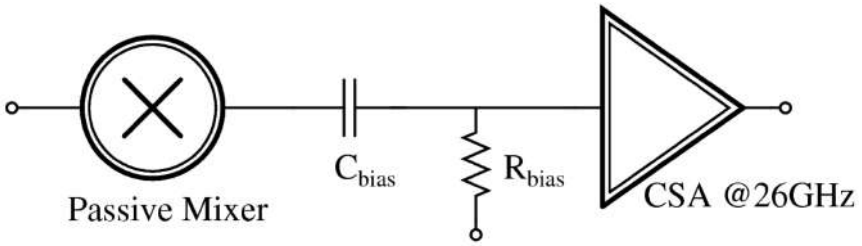
$$C_{eff} = \frac{C_{gg}}{1 - w^2 L C_{gg}}$$

eqn(6.2)

The schematic level design uses ideal wires for interconnections between the blocks, whereas in the layout we connect them with metals. Extending the above analysis, all the interconnections between the blocks in the schematics are replaced with estimated inductances and capacitances modelled with ideal components and simulated to check the performance.

6.2 Loading aspects

Consider the interconnection between the passive mixer and the buffer that loads the passive mixer as shown in figure 6.2.1 a. The entire passive mixer can be simply modelled as an AC current source with current pumping into its LC load as shown in figure 6.2.2 b. The parasitic capacitances of the passive mixer, looking from the load side are shown as capacitance Cpar. The output of the passive mixer is AC coupled and then it is connected to the gate of the mosfet in the CSA buffer. The gate of mosfet, in the CSA, can be modelled simply as a mosfet with appropriate DC biased conditions and the looking in impedance of mosfet can be modelled as a capacitor, Cgg, as shown in figure 6.2.1 c.



(a)

fig 6.2.1 (a) CSA loading the passive mixer

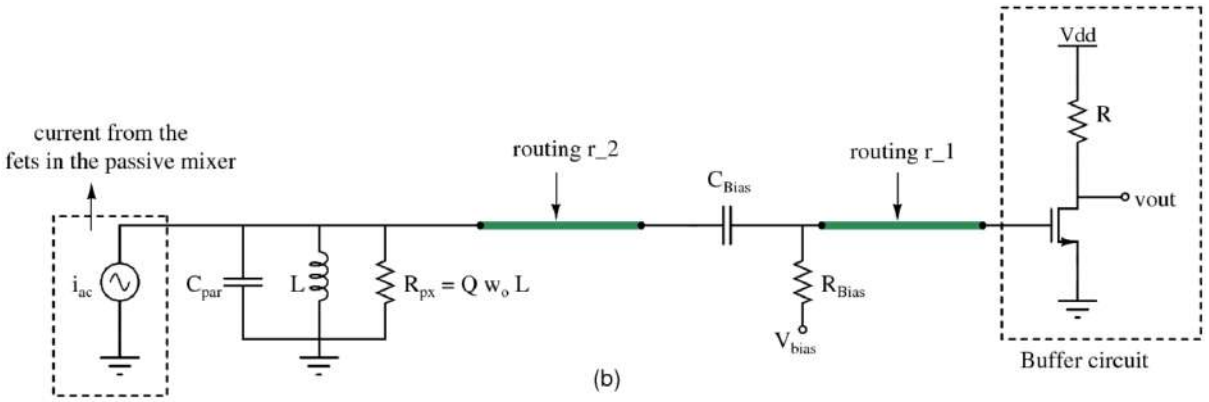


fig 6.2.1 (b) The output stage of the passive mixer modelled as a current source and LC load. The routings between the passive mixer and CSA are shown.

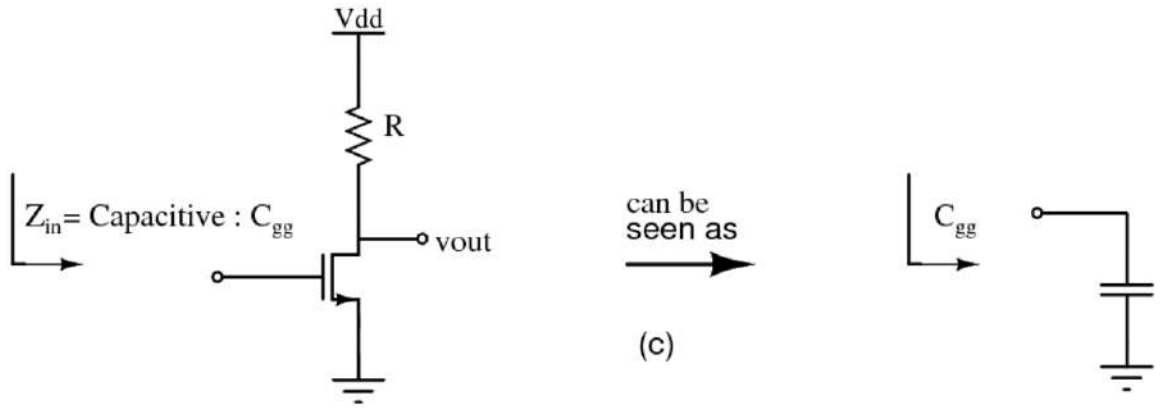


fig 6.2.1 (c) Modelling the CSA buffer as capacitance, Cgg.

Consider the case where routings r_1 and r_2 are just ideal wires, as what happens in the schematic level design and simulations. Since V_{Bias} is a DC signal, it is an AC ground. This makes the resistance R_{Bias} and C_{gg} to be in parallel combination, which can be analysed as a capacitor with a Quality factor 'Q' as shown in figure 6.2.2 b. Now as shown in figure 6.2.2 c, C_{Bias} and Cgg are in series combination which makes the effective capacitance lesser than the least value among the two. Since C_{Bias} is an AC coupling capacitor, its value is much larger than Cgg. The circuit C_{Bias}, R_{Bias} and Cgg effectively look as a Capacitance of value slightly lower than Cgg with a quality factor as shown in figure 6.2.2 c. Hence the overall loading effect at

the output of the passive mixer from the buffer and the AC coupling capacitor and bias resistor can be seen as a capacitor (whose value is slightly lesser than Cgg) with a quality factor.

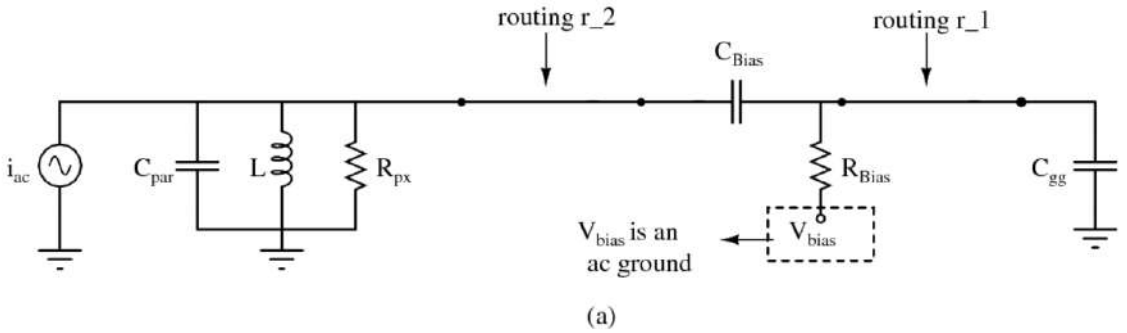


fig 6.2.2 (a) Routings r_1 and r_2 modelled as ideal wires

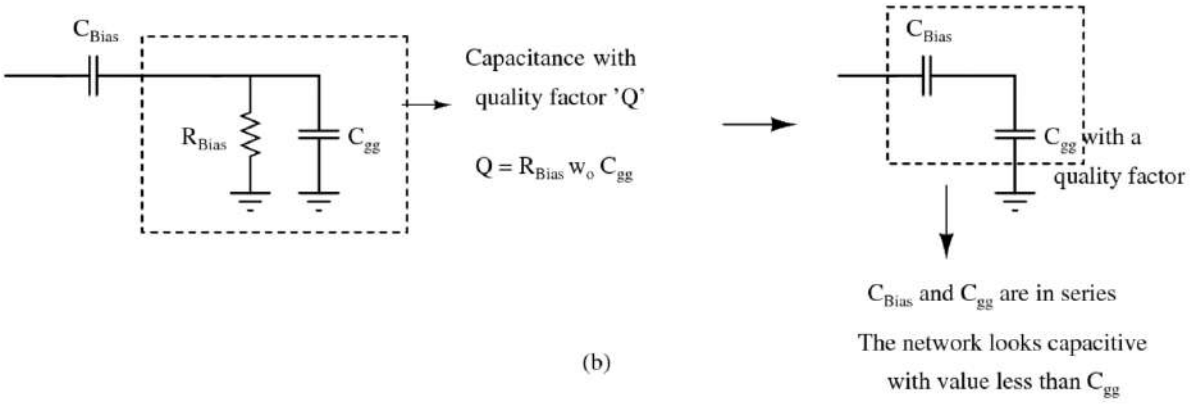


fig 6.2.2 (b) Analysing the combination of C_{Bias}, R_{Bias} and Cgg.

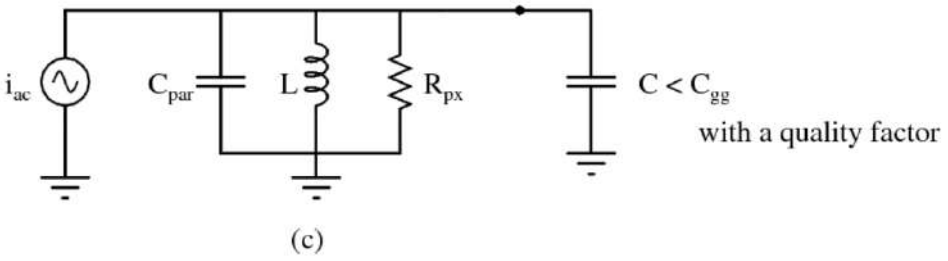


fig 6.2.2 (c) The overall loading on the output of the passive mixer.

The lumped element modelling of layout parasitics provides justification for behaviour in post Layout simulations.

6.3 Dummy filling

The IC fabrication process requires each metal, oxide (OD) and poly (PO) to have certain minimum and maximum density specifications and requirements. Dummies are filled at an appropriate distance away from the critical RF routings and components such that the dummies don't affect the performance. To decide on the distance at which dummy metals are to be filled so that there is no performance difference, the following simulations are done. Most of the critical RF routings are done with the top metal layer M9 as it has lower capacitance to the substrate (as it is farthest from the substrate). A 4u x 40u M9 metal strip is drawn and its inductance (L) and Quality factor (Q) at simulated at 13GHz, 26GHz and 39 GHz. Now, as shown in figure 6.3.1 all the metal, OD and PO layers are drawn one above the other, which mimics the dummy fills. The distance (d) between the M9 strip and dummies is varied and the inductance and quality factor of the metal strip are measured as a function of distance 'd'. The results are shown in figure 6.3.2

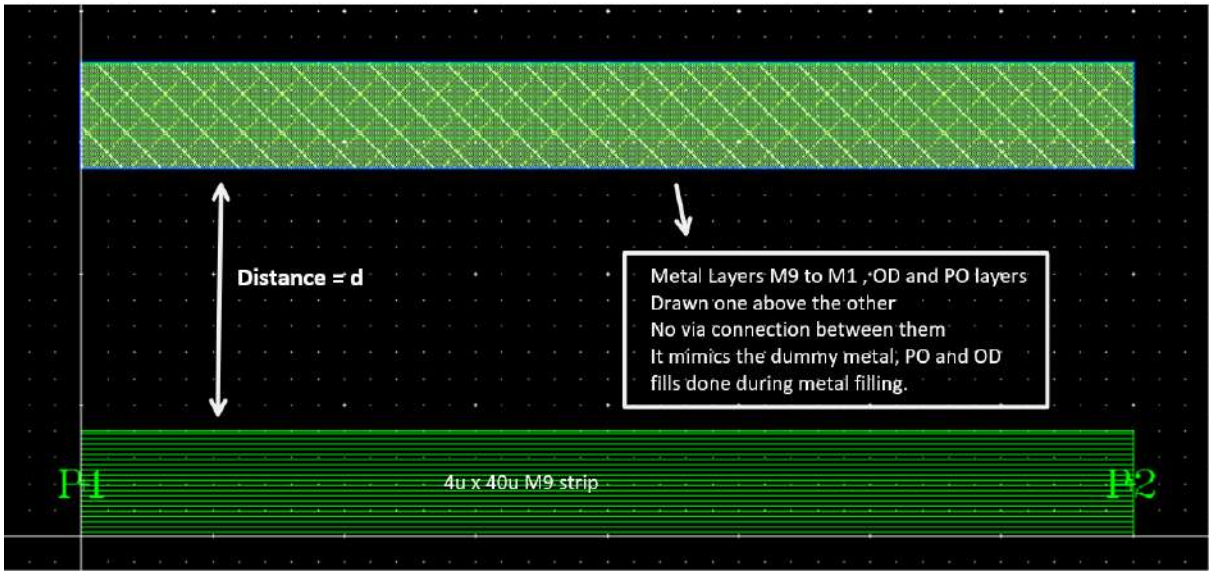


fig 6.3.1 Setup mimicking the situation after metal filling

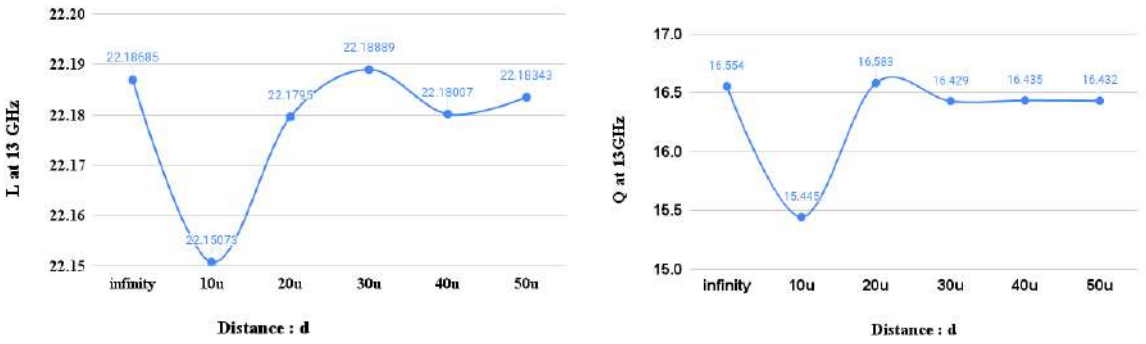


fig 6.3.2 a: Inductance and Quality factor simulated at 13GHz

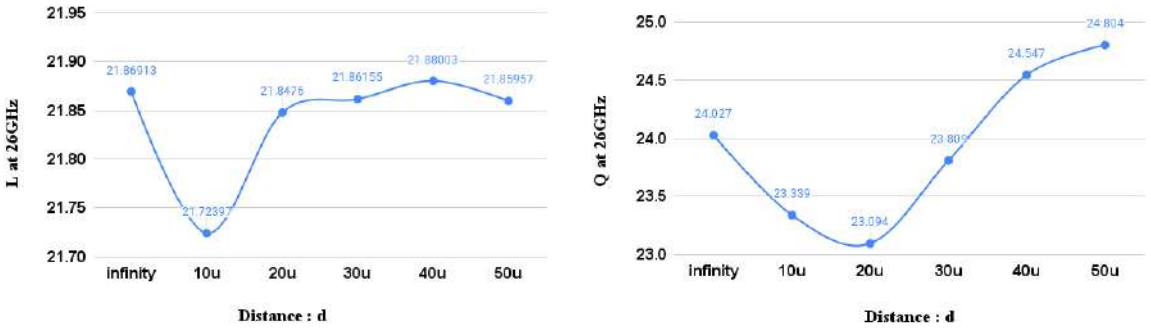


fig 6.3.2 b: Inductance and Quality factor simulated at 26GHz

fig 6.3.2 c: Inductance and Quality factor simulated at 39GHz

The results show a considerable change in the values of inductance and quality factor when the distance is 10u, which implies that the closer

the dummies are, the more parasitics it adds. The results also show that 30u is the optimal distance as the inductance value is almost closer to the one with infinite distance separation. The dummy exclude layers were drawn at 30u distance away which makes the dummies not to be filled within 30u distance from the main RF routings and blocks. Figure 6.3.3 shows a typical example of the dummy exclude layers (DMEXCL layers) and an example of the dummy filling is shown in figure 6.3.4.

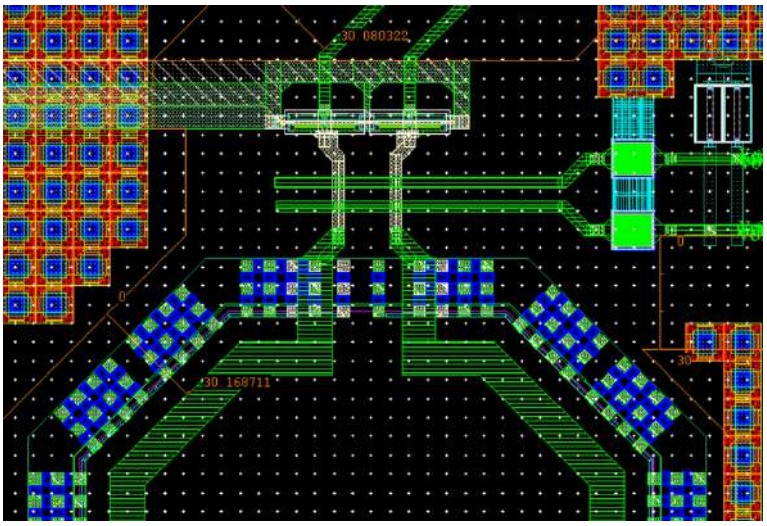


fig 6.3.3 DMEXCL layers drawn at 30u distance from RF lines

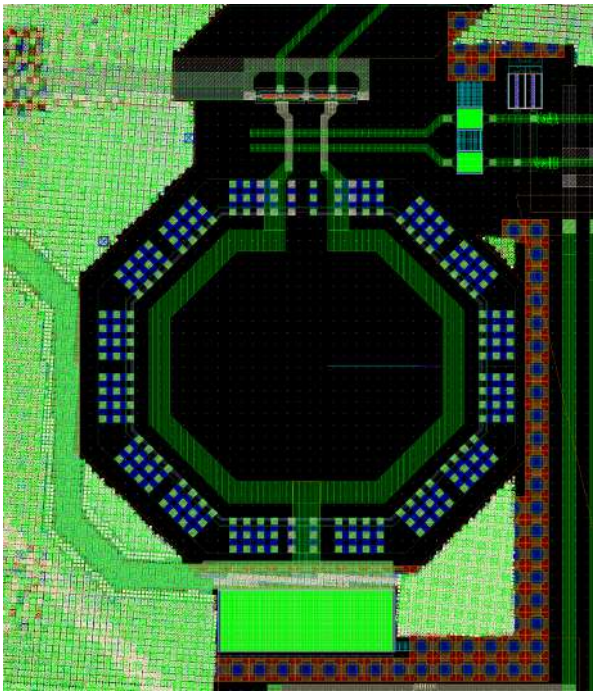


fig 6.3.4 Dummy metal, OD and PO layers filled outside the DMEXCL.

6.4 Other layout considerations and optimizations

The mmWave routings require proper floorplanning for maximum isolation and proper grounding. All RF blocks were bounded (encased) by ground shields to provide (improve) isolation between them. As shown in figure 6.4.1. The process supported 45° degree bends, so they were used for RF routings such there are only 135° degree bends and not orthogonal, to reduce the parasitics.

The same 135° degree bends have been used for the VDD supply and Ground routings, which carry high currents, to avoid electromigration. The supply and ground lines were carefully simulated to ensure that any line inductance or resistance will not deteriorate the performance. The grounds and supply lines were connected to the nearest bond pads available and the grounds of different blocks are connected only at the bond pads to avoid unwanted leakage of current from one block to another block. At high current carrying routings, multiple metal layers were run in parallel to reduce the resistance of the connection.

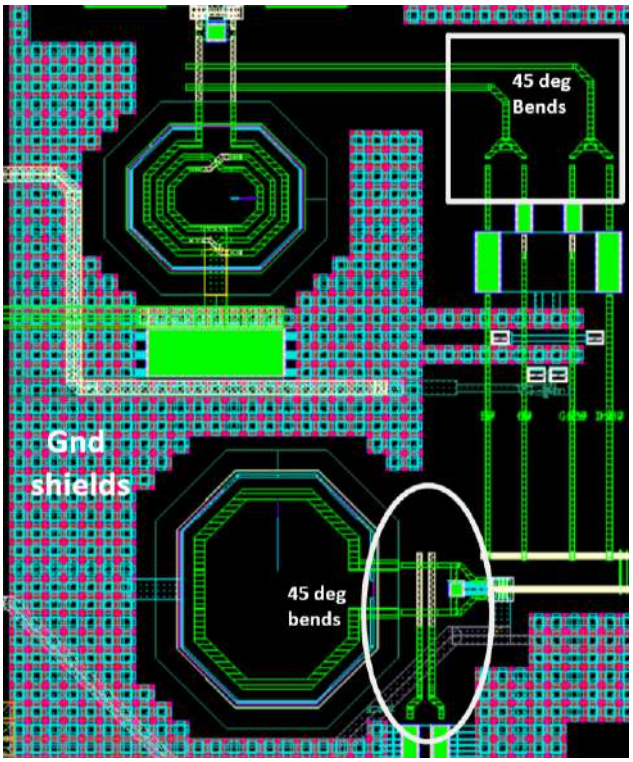


fig 6.4.1 showing ground shields around RF blocks and 45° bends.

CHAPTER 7

MATCHING NETWORK

7.1 The Bond-wire and the Bond-pad model

Bond-pads have aluminium pads, which are exposed to the outside of IC. A gold wire if bonded to the bondpad and the choice of gold is because of the reason gold bonds better with the aluminium. The gold wire here is called bondwire and typically carries an large inductance upto 1nH, with a quality factor of typically around 20 ~ 25 at mmwave frequencies. The bondpad can be simulated with the electromagnetic simulator - EMX but extra care has to be taken with the Electro-Static Discharge diodes, shortly called as ESD diodes. EMX cannot extract the parasitics related to oxide and poly layers. Also it cannot extract the characteristics of the semi-conductor region. Hence the ESD diodes are removed from the model that is extracted by EMX and their parasitics are separately extracted using Parasitic Extraction using calibre, called PEX.

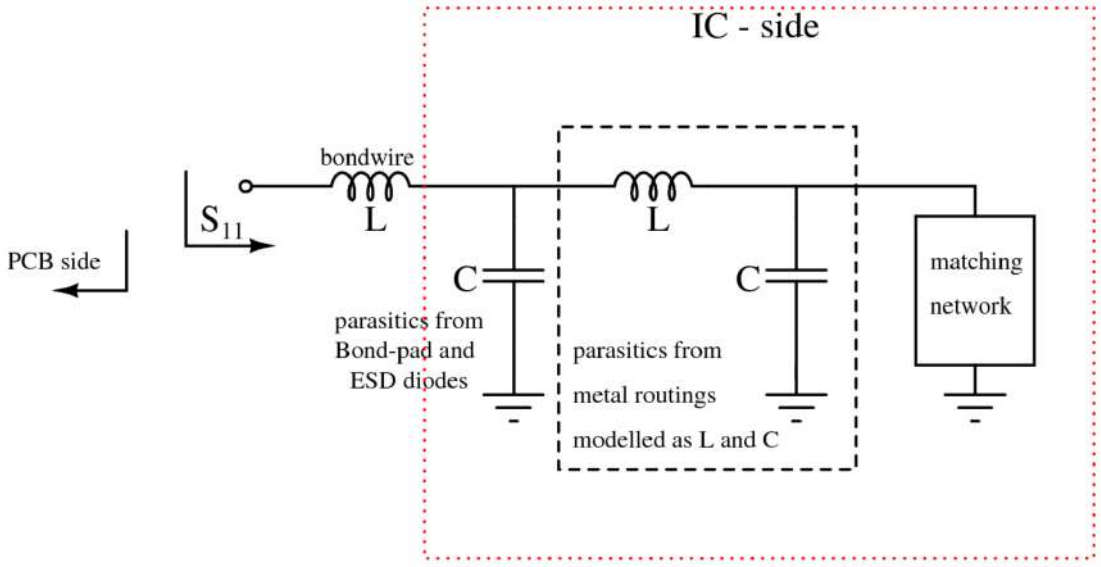


fig 7.1.1 Lumped element modelling of the Bond-wire, bond-pad, metal routing and the parasitics from them.

The bond-pad and the ESD diodes in the bond-pad offer a significant amount of capacitance to substrate and can also deteriorate the performance with its poor quality factor. The metal routings provide substantial amount of inductance and parasitic capacitance to ground. Hence metal routings also play an important role in the matching networks. An effective but simplified RLC model of the circuit combination of the bond-wire, bond-pad and the metal routing is shown in the figure 7.1.1.

The effective circuit combination can behave as a downward or upward impedance transformation depending on the component values and their Quality factors. The inductances and capacitances of this circuit resonate at a particular frequency and provide a narrow band matching network. The parameters that are under our control are the parasitics from the metal routings and the matching network. To match the real part of the impedance to 50 ohms, we need a resistor in the matching network. If the network needs additional capacitance to resonate out at 13 GHz, then a shunt capacitor can be placed at an appropriate location; either right after the bond-pad or in shunt with the resistor in the matching network. If the network demands additional inductance, then it can be brought up from the metal routings. The width and length of the metal routing can be adjusted such that it provides the required inductance and the quality factor. In this case it turns out that a resistor as a matching network is sufficient one. Shown in the figure 7.3.2 is a plot of S11 with different resistance values used as the matching network a function of frequency.

7.2 Need for buffer before passive mixer

The necessity for a buffer before the pasisve mixer stage has two main reasons. They are explained here.

Reason - 1:

As explained in the section 1.2, the maximum power level of the 13 GHz signal before it enters the IC is -5 dBm. The bondwire is modelled and its

parasitics and impedance is extracted using 3D electromagnetic simulator. The circuit combination of bond-wire and the bond-pads shows an Insertion Loss (IL) of -4.425 dB and S11 of -3.104 dB when excited and terminated with a 50 Ω port. The result is shown in the figure 7.2.1

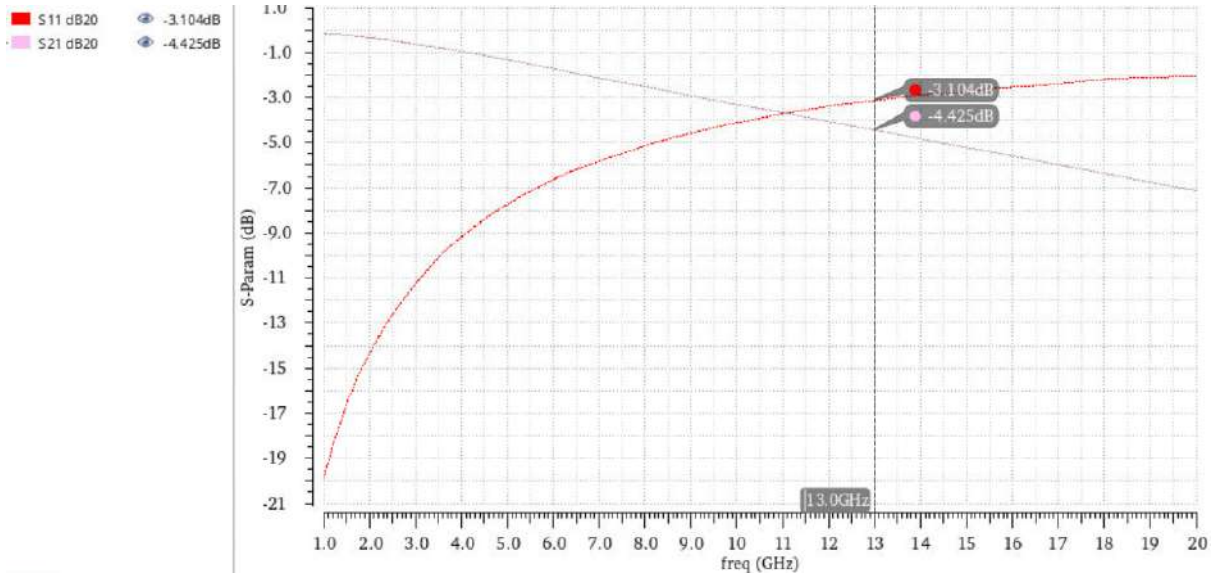


fig 7.2.1 S-parameter simulation result of the circuit combination of bond-wire and bond-pad that is used for RF signal.

Therefore the maximum power level of the signal after the bondpads is around -9 to -10 dBm, with a 50 ohm load, which means the amplitude of the signal is 100 mV. The gate input of the passive mixer needs sufficient swing for it to efficiently turn on and off the transistor. This creates a need for the amplification of the 13 GHz signal. Hence we need a buffer.

Reason - 2:

The voltage mode passive mixer is a bilateral network, which means both the input and output ports have control on the performance of the mixer. So consider there is no buffer between the passive mixer and the off-chip signal component. Any small variations or mismatches in the PCB side would affect the performance of the passive mixer where the actual frequency doubling takes place. Hence it is always optimal to use buffers on the either side of a bilateral network.

7.3 Matching network

The looking-in impedance of a CSA amplifier is nothing but gate looking-in impedance, which is capacitive. The DC bias of this buffer can be provided with a bias resistor of value Rmatch, which can also be used for matching purposes. Since the 13 GHz input waveform is already an AC coupled signal, we don't need a separate AC coupling capacitor as part of a bias network. The value of resistor that is used is 230 ohms. The circuit is shown in the figure 7.3.1.

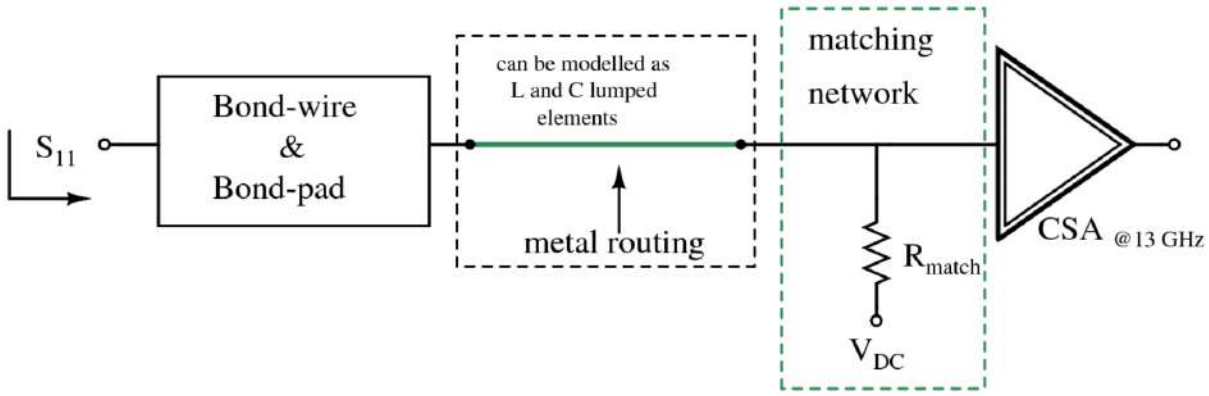


fig 7.3.1 The effective matching network looking-in from the PCB side

Shown in figure 7.3.2 has the matching network, just a resistor which is also used to set the DC value at the gate of the CSA buffer.

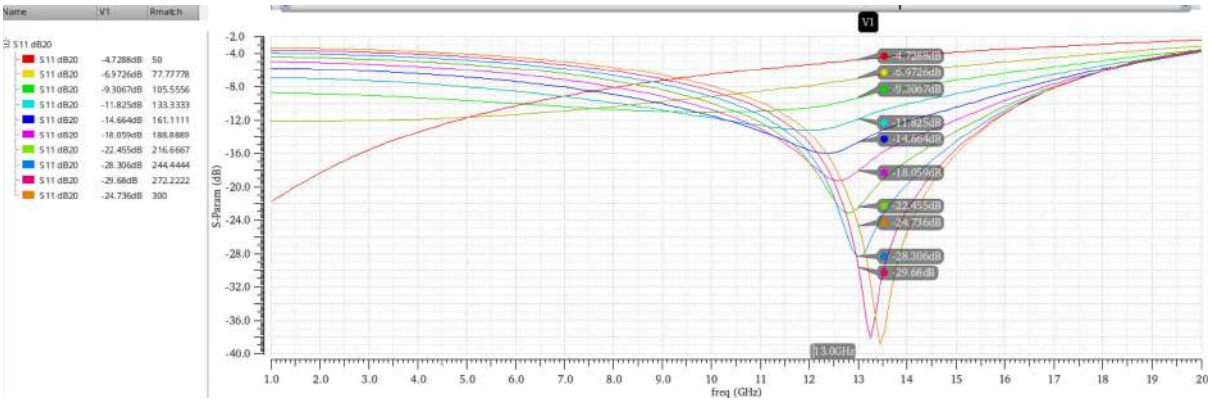


fig 7.3.2 S11 plotted for different values of resistors, Match.

CHAPTER 8

FINAL CIRCUIT AND RESULTS

8.1 Schematic level circuit description

As discussed in the earlier sections, there is a buffer, also called as buffer at 13 GHz, which drives the passive mixer. The input to this buffer is an AC coupled 13 GHz sinusoidal signal, which comes from the off-chip. The matching network that is used inside the IC is a simple DC biasing resistor, of an appropriate value. The passive mixer does the mixing operation and doubles the input frequency. The buffer after the passive mixer, also called as buffer at 26 GHz, amplifies the outputs of the passive mixer and drives the up-conversion gilbert cell mixer. This entire scenario is shown in figure 8.1.1. The tape out, that is done, is a fully bonded IC. Therefore bondwire and bondpads are also shown in the figure.

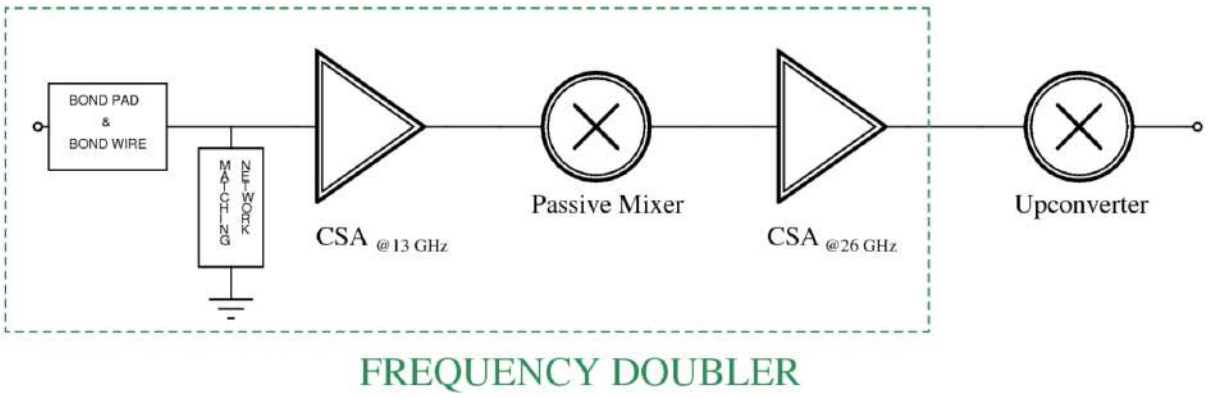
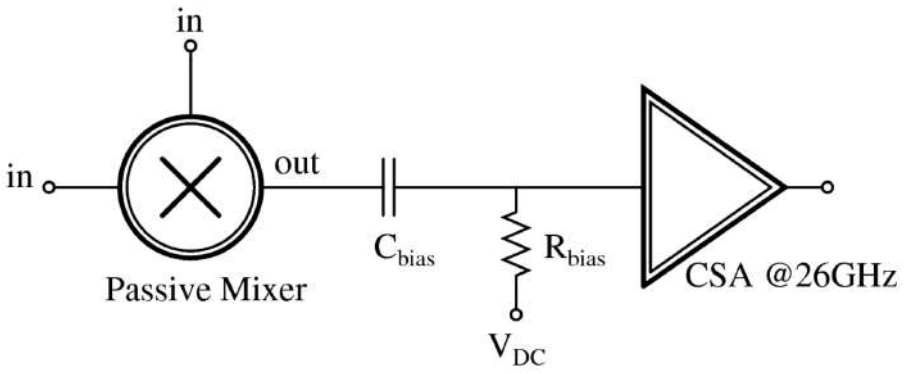


fig 8.1.1 block level description of the frequency doubler.

The upconverter loads the buffer at 26 GHz and the inductor at the load of this buffer is adjusted such that it resonates out the capacitive parasitics of the upconverter, that loads the buffer, and its own parasitics. The outputs of this buffer are directly connected to the gates of the LO stage of the upconversion mixer i.e., there is no bias circuit. The output of the passive mixer is AC coupled and is then fed as input to the buffer at 26 GHz

as shown in the figure 8.1.2. The topology of both the buffers used in the frequency doubler is simple pseudo differential common source amplifier with LC tuned load and we need two buffers, one for each I and Q signals.



8.1.2 Interconnection between passive mixer and Buffer at 26 GHz.

The connection between the buffer at 13 GHz and the passive mixer is described in the section 3.7. There are two buffers, one for each I and Q, and each buffer produces differential outputs. Therefore there are four phases. Each phase goes to gates and drains of the transistors in the passive mixer and the DC value required for the gate and the drain are different. Hence the interconnection between the buffer and the passive mixer is as shown in the figure 8.1.3.

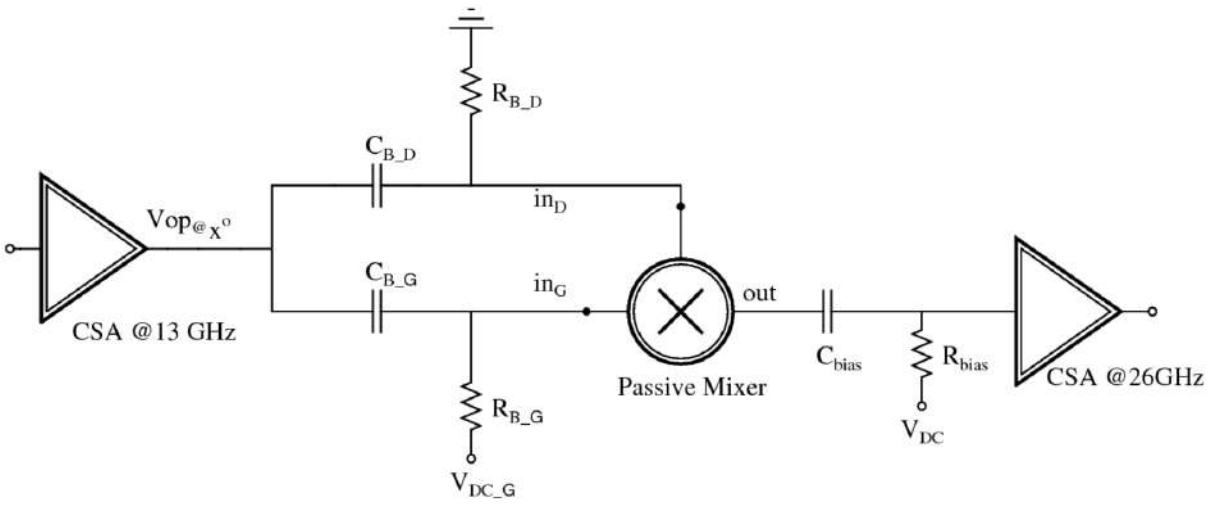


fig 8.1.3 Interconnections between the blocks of frequency doubler.

8.2 Layout

Shown in figure 8.2.1 is the final tapeout of the transmitter which has the blocks in the transmitter chain and the frequency doubler. The blocks that are present in the transmitter chain are Baseband Buffers, a block designed to operate as upconverter and power amplifier, also called as powered mixer, a balun to convert differential output to single ended and an inductor for matching the output to 50 ohms.

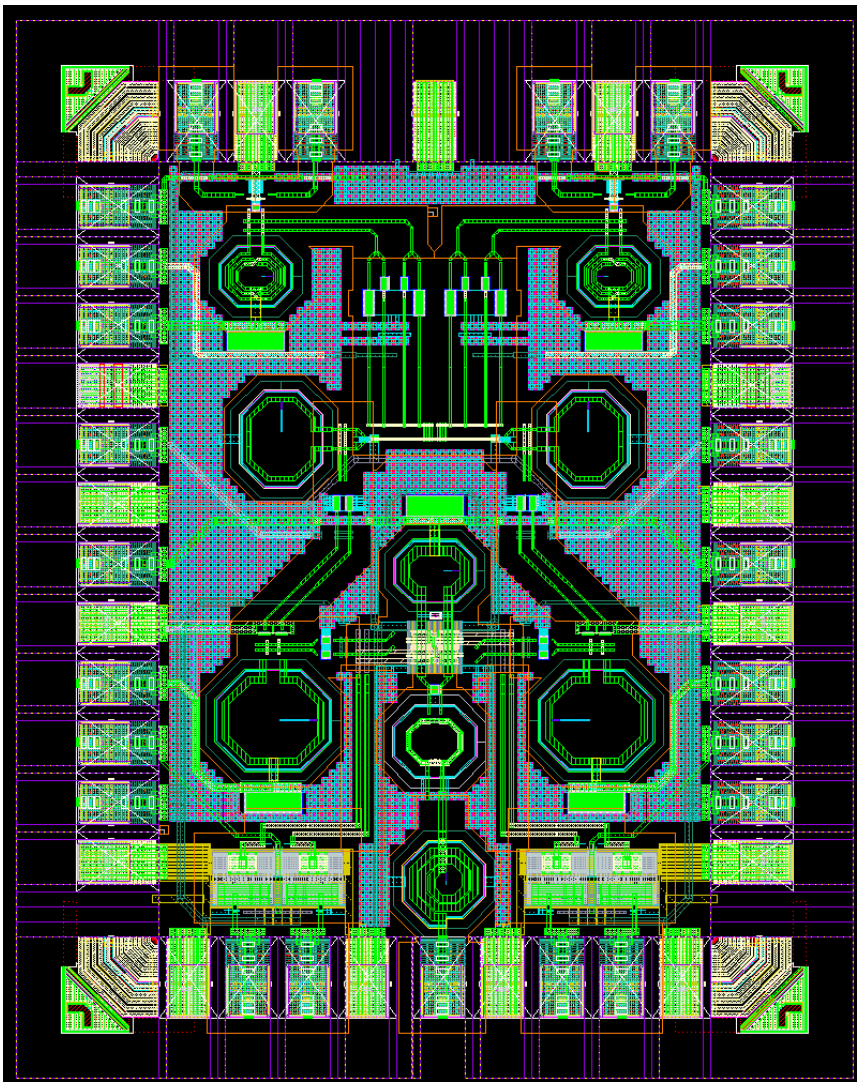


fig 8.2.1 Final layout of the transmitter

Shown in figure 8.2.2 is the final layout with all the individual blocks labelled with numbers. The blocks corresponding to those numbers are:

1. CSA at 13 GHz - I.
2. CSA at 13 GHz - Q.
3. Passive mixer - I.
4. Passive mixer - Q.
5. CSA at 26 GHz - I.
6. CSA at 26 GHz - Q.
7. Powered mixer.
8. Balun after the powered mixer.
9. Baseband section - I.
10. Baseband section - Q.
11. Inductor for output matching.

The figure is shown in the next page.

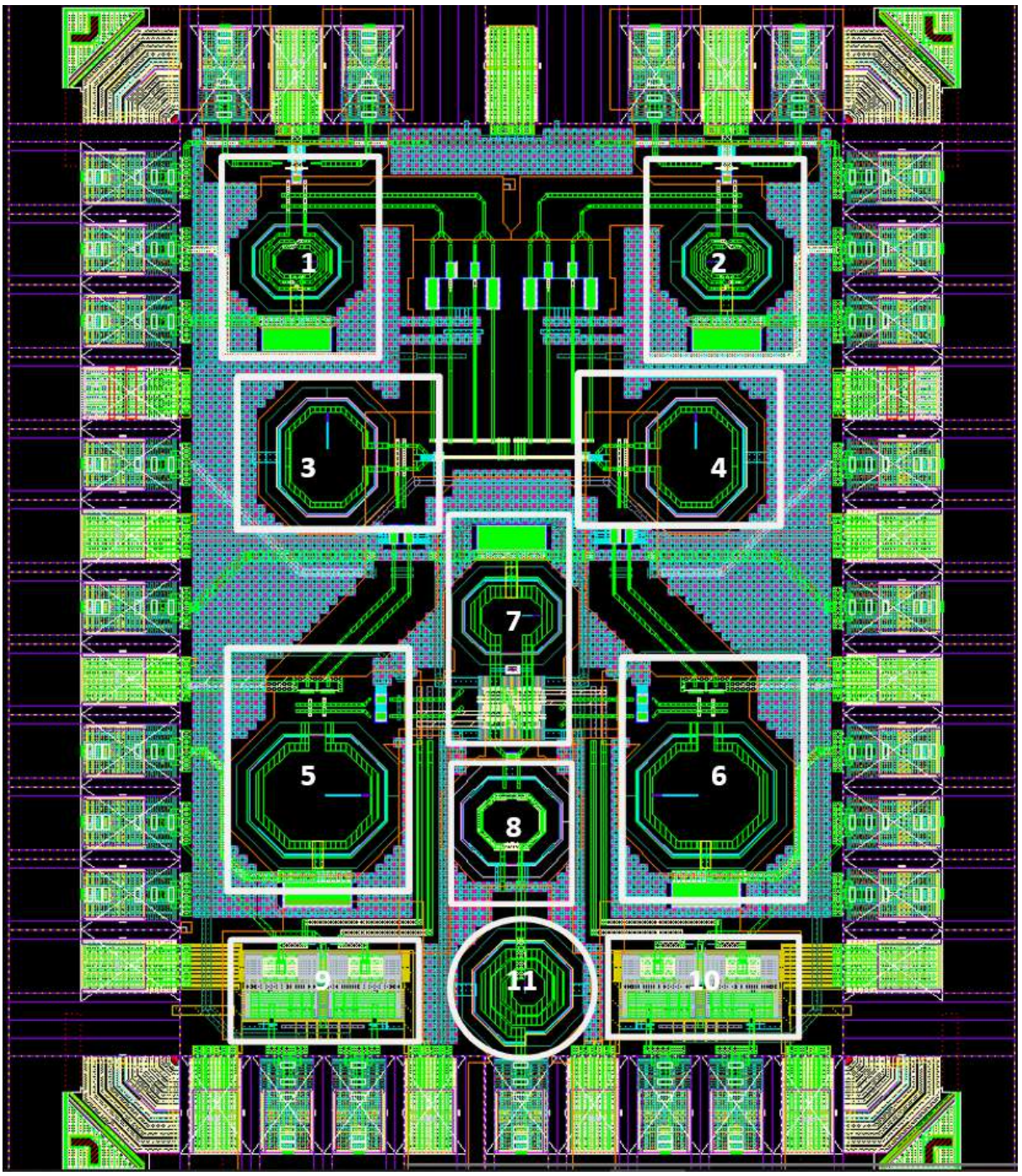


fig 8.2.2 All the individual blocks labelled

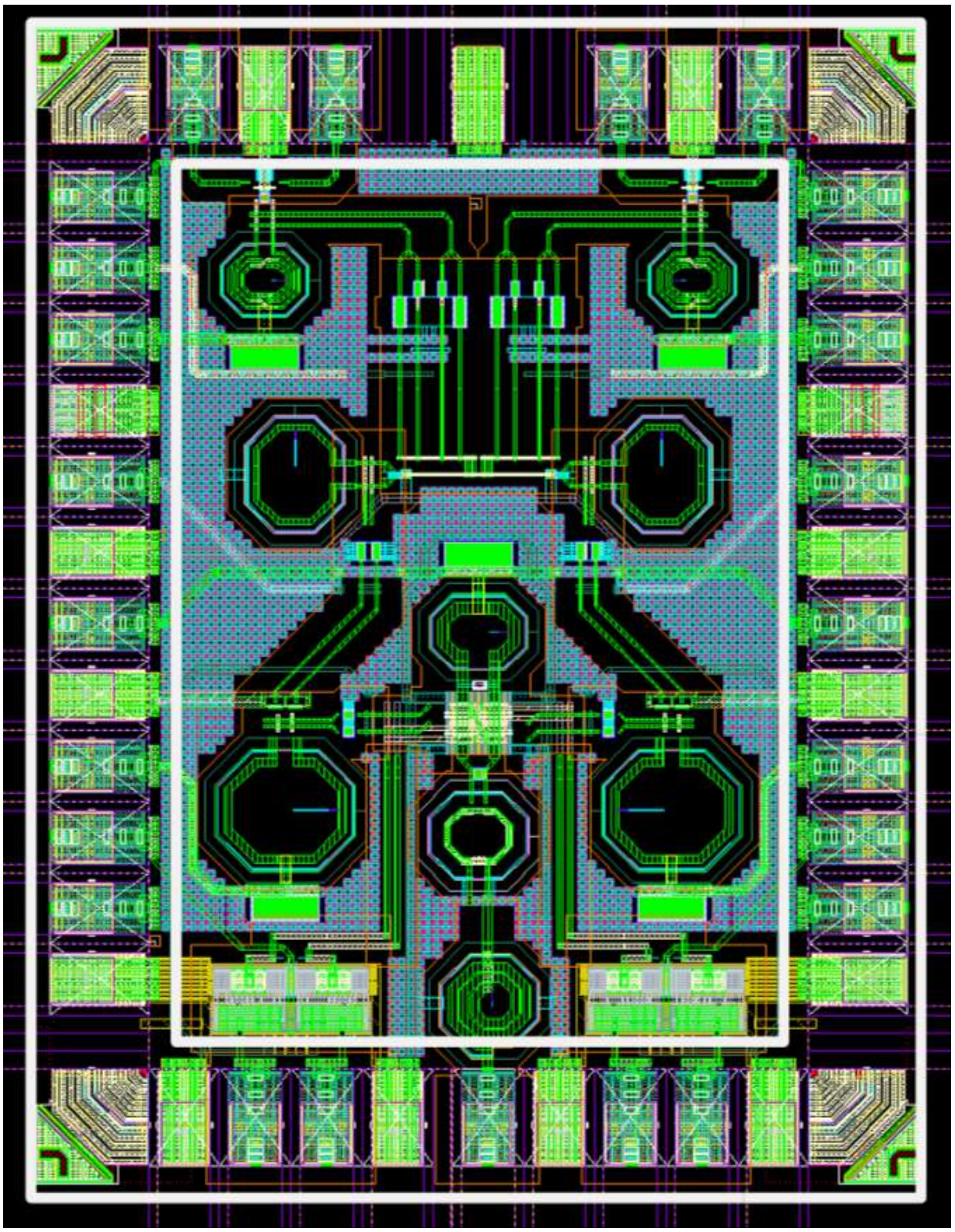


fig 8.2.3 highlighting the bondpads.

Figure 8.2.4 shows the position of the de-coupling capacitors used at the VDD of a particular block. These capacitors provide small impedance to ground for high frequency signals thereby blocking all the unwanted high frequency content to enter the circuit through the power lines.

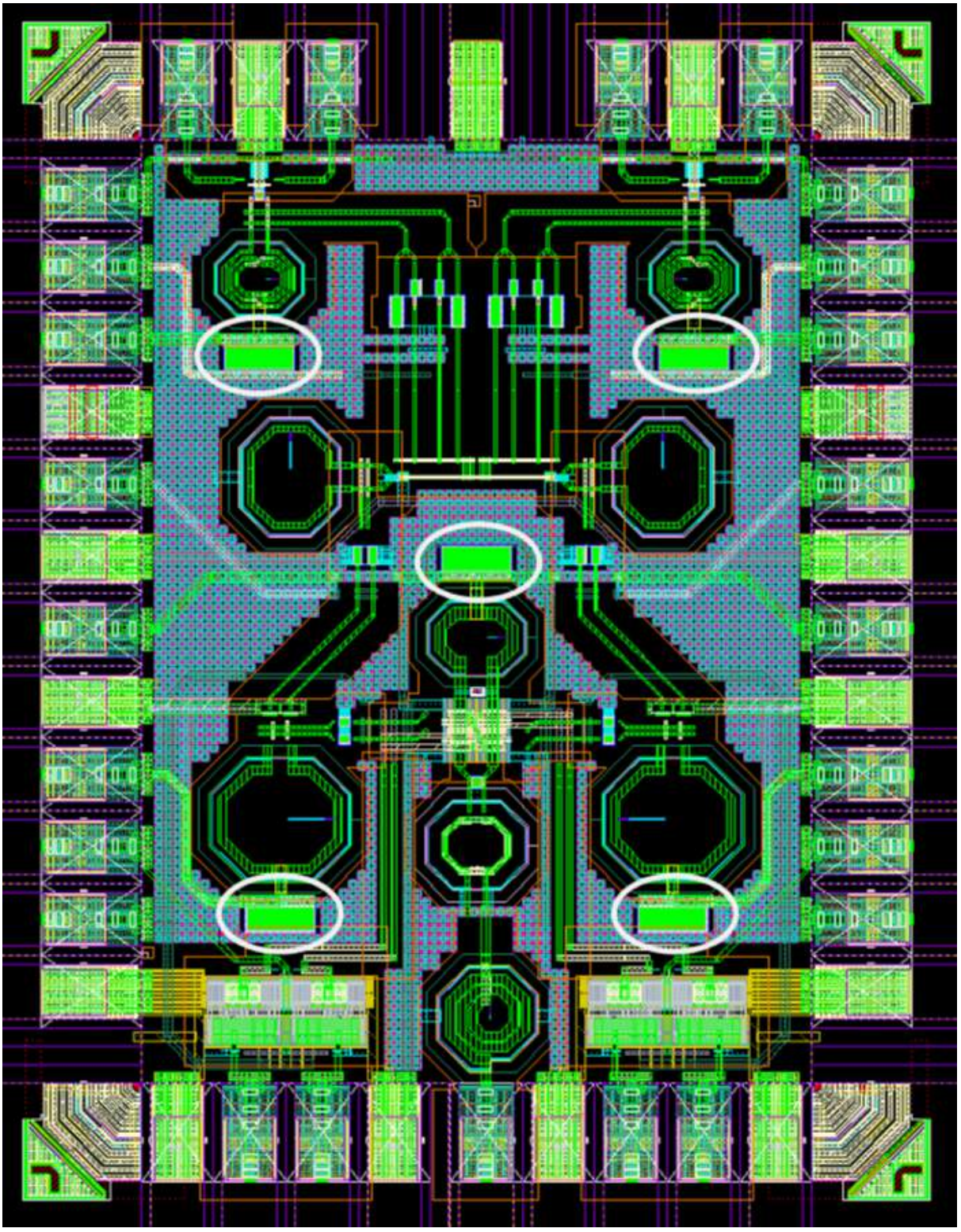


fig 8.2.4 highlighting the de-coupling capacitors.

8.3 Results

1. Input matching looking in from off-chip is S_{11} < -10 dB.

This is discussed in detailed in chapter 7. The final post layout result of S_{11} looking from the PCB end is shown in the figure 8.3.1.

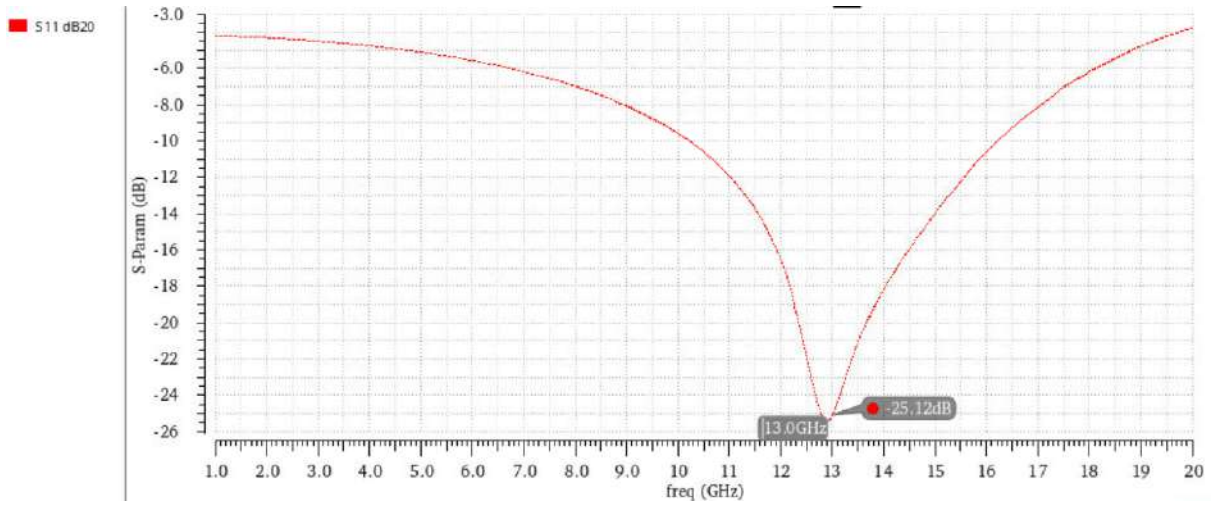


fig 8.3.1 S_{11} looking in from the PCB end.

2. The amplitude range of the 26 GHz LO signal provided to the upconversion mixer is 280mV to 320mV.

The required amplitude for the LO of upconverter is achieved by the LO buffer at 26 GHz. Shown in figure 8.3.2 is the plot showing the magnitudes of the different phases of LO waveform at the gates of the upconverter, obtained from the post layout simulations. The shown is the variation of amplitudes of LO waveform with respect to the DC voltage at the gate of the passive mixer, which is an off-chip signal. The optimal value of the DC voltage can be set off-chip after a certain iterations of testing.

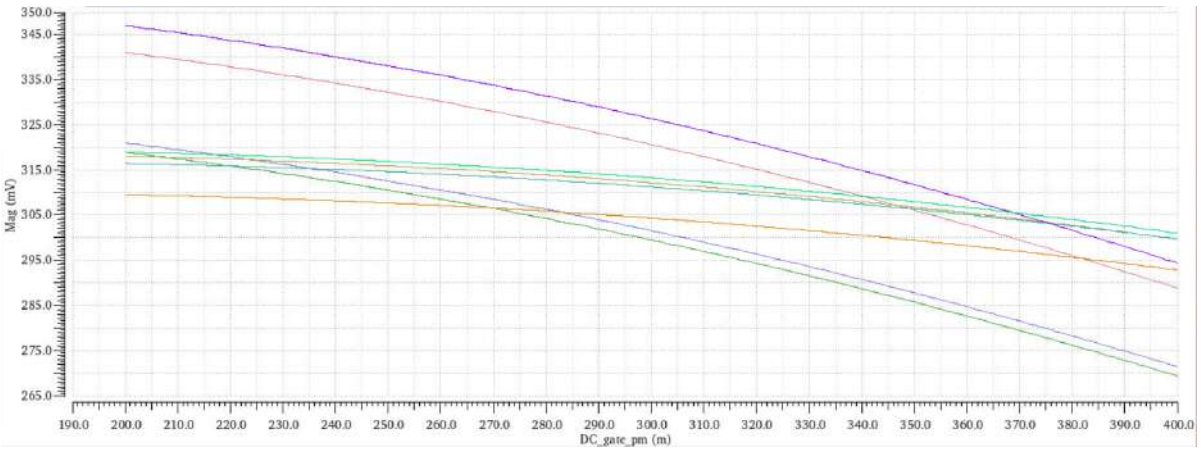


fig 8.3.2 Variation of magnitudes of LO waveform at the gates of upconverter with respect to the DC voltage of the gate of the passive mixer.

3. The I-Q imbalance of the transmitter is < -40 dBm.

This is discussed in detail in chapter 5. The final result obtained from the post layout simulation is shown in the figure 8.3.3

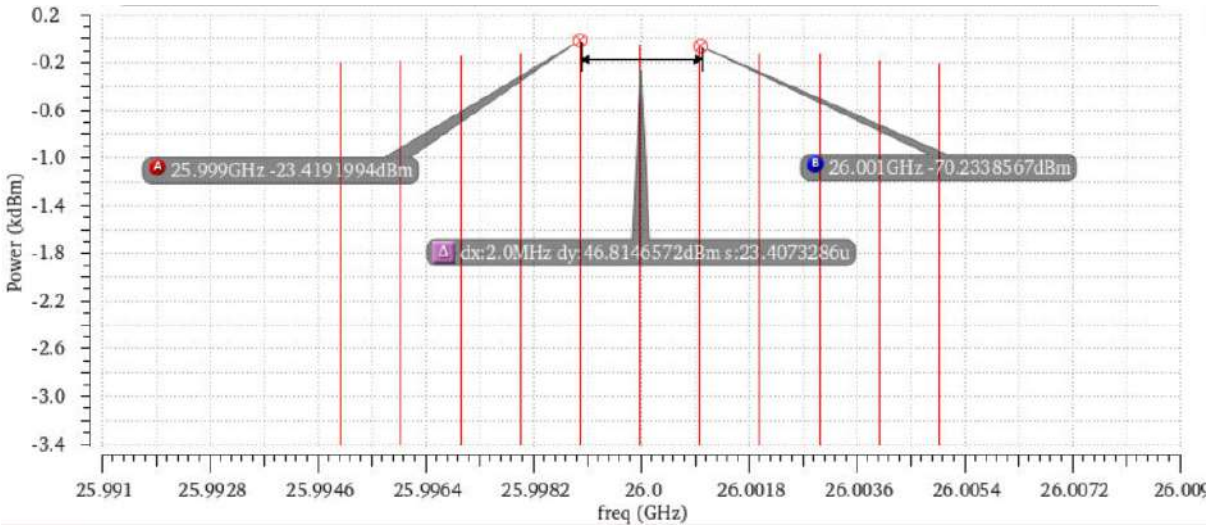


fig 8.3.3 Output power spectrum of the transmitter around the 26 GHz.