Millimeter-Wave Phase-Shifting Transmitter for 5G Networks

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ADITYA SUNDARARAJAN

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THESIS CERTIFICATE

This is to certify that the thesis titled **Millimeter-Wave Phase-Shifting Transmitter for 5G Networks**, submitted by **Aditya Sundararajan**, to the Indian Institute of Technology, Madras, for the award of the degree of **DUAL DEGREE (BACHELOR OF TECHNOLOGY & MASTER OF TECHNOLOGY)** , is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Prof. S. Aniruddhan
Research Guide
Associate Professor
Dept. of Physics
IIT Madras, 600 036

Place: Chennai

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ABSTRACT

KEYWORDS: 5G mobile communication, millimeter wave circuits, transmitters, mixers, phase-shifters, phased arrays, power amplifiers, power mixers, polyphase filters, baluns

A 26GHz transmitter capable of 5-bit phase shifting is designed and laid out in 65nm CMOS for 5G millimeter-wave radio applications. The transmitter primarily consists of single power-mixer that upconverts the baseband signal to 26GHz and also amplifies it before sending the signal to the antenna. The phase-shifting is performed on the LO signal by a phase-shifter that uses the 4 quadrature LO signals. Simulations with EM parasitic extraction shows that the transmitter is able to achieve an OP1dB of 8.88dBm and a Psat of 11.75dBm with a power gain of 45dB. The transmitter is controlled by 5 digital bits that can phase-shift the output signal from 0°to 360°with a maximum DNL of 0.27. The transmitter consumes 260mW from a 1.2V supply and occupies an area of 1.3mm^2

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ABBREVIATIONS

5G	5th Generation (of cellular networks)
MIMO	Multiple-Input Multiple-Output
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
EVM	Error Vector Magnitude
BER	Bit-Error Rate
LO	Local Oscillator
BB	BaseBand
RF	Radio Frequency
DAC	Digital to Analog Converter
I-Q	In-phase and Quadrature signals
IC	Integrated Circuit
DNL	Differential Non-Linearity
LSB	Lowest Significant Bit
ESD	Electro-Static Discharge
LDO	Low-Dropout Regulator

CHAPTER 1

INTRODUCTION

For the 5th Generation (5G) cellular communication and enhanced wireless mobile broadband, the use millimeter-wave frequencies above 6GHz have been vital because of the availability of larger bandwidths for faster data rates and better quality of service. Previous generations using lower carrier frequencies naturally have lower bandwidths that lead to limited capacity and more latency. It is projected that 5G systems will be able to support data rates that are a 1000 times more than 4G systems with better latency, lower power consumption, lower cost and higher spectral efficiency. This will be made possible due to the wider channel bandwidths available at higher frequencies [7][5]

1.1 Key Challenges and Technologies in 5G

There are however, a number of challenges that must first be overcome. A major limitation of using higher frequencies is that the path loss at 26GHz is about 20-25dB higher than that at lower frequencies like 2.5GHz. The effect of shadowing adds an addition 5dB of path loss that must also be accounted for. This increased attenuation in this band demands higher gain and output power from the transmitters that are used.[7]

The increased path loss forces 5G to use smaller cells. This would require a larger number of densely packed base stations and is made possible by the reduced antenna sizes at higher frequencies. Smaller antennas also enables the use of technologies like massive-MIMO and beamforming [1].

Massive-MIMO involves the use of a very large number (maybe even a 1000) antennas on a single antenna array. Besides increasing the output power, it also makes the transmitted signal more tolerant to fading. The use of beamforming, where the output signal is focussed in one specific direction by the use of antenna arrays allows for spatial multiplexing where multiple users can be accommodated while using the same

time-frequency resources. Both these technologies play critical roles in ensuring better quality of service and higher data rates.

1.2 IC Design Challenges at High Frequencies

Traditionally, technologies such as GaAs and InP processes were used to achieve this high power but they involved higher costs too. With the advancements in CMOS technology scaling, better integration and transistors with high unity gain frequencies are made possible at lower costs. A limitation of CMOS designs is however the low breakdown voltages of the devices. This has been overcome in this project by FET stacking as described later. The other more immediate challenge is with the increased parasitics and magnetic effects at higher frequencies that need to be accounted for and require more carefully designed circuits.[5]

Complex digital modulation schemes used in modern communication systems to achieve high data rates require a low error vector magnitude (EVM) to achieve a low bit error rate (BER). A highly linear transmitter is needed for a low EVM that will probably be working in power back-off mode. Image rejection of the modulator and low phase noise from the LO signals are also key to ensuring a good modulation quality.

The phased-array that allows beamforming requires an array of transmitters (or receivers) with independent phase control. This needs an architecture that uses a phase-shifting scheme that is precise but also power and area efficient. As mentioned earlier, the phase-shifts need to be very accurate to ensure a low bit error rate. The phased array will be described in more detail in the next chapter.

Chapter 2 will thus explain beamforming and phase-shifting more in detail at the hardware level. Chapter 3 will then discuss possible transmitter architectures and the final choice that was taken. It also describes the complete signal and LO paths and the functions of the different blocks. Chapters 4 and 5 then go into the details of how each of these blocks were implemented at the circuit level and laid out. Chapter 6 will discuss the bonding details and the testing board. Chapter 7 then presents the final simulations results that were achieved while Chapter 8 will go over the final conclusion and possibilities of future work relating to this project.

Appendix A discusses additional work that was done relating to a wideband transmitter.

CHAPTER 2

Beamforming

As mentioned in the previous chapter, the use of millimeter wave frequencies comes at the cost of increased path loss and loss due to shadowing. One way to counter this is to use antenna arrays that are capable of beamforming. This allows the transmitter and receiver to focus their gain in one direction and can thus transmit (and receive) the signal more efficiently. When used with multiple antennas and users it helps to overcome fading while also improving how efficiently the spectrum is used. More users in different locations can now be supported while using the same time and frequency resources.

At the hardware level for a transmitter, this is achieved by phase-shifting the RF signal sent to each antenna array element by a different amount. As a result, when the signal is transmitted from the antenna, the wavefront will be in a particular direction dictated by the relative phase shifts between array elements. Although the explanation of how this works is not too important to the discussion here, it can be seen as an inversion of the same phenomenon that happens when a wave hits a flat surface at an angle. In such a scenario, different points on the surface receive the signal with different delays (or phase shifts). Similarly, transmitting signals from different points with the same phase shifts will create a wave traveling in the same direction as earlier.[3]

It is also important to draw a distinction between time delays and phase shifts here. Without getting into the mathematics behind it, in the example earlier we see that the for a wave hitting a surface at an angle, different points on the surface receive a signal that delayed in time from each other. Hence, ideally we would like to delay the signal in time before we transmit it. If our signal consisted of only one frequency then this time shift would correspond to an equivalent phase shift and we can thus, phase shift each signal before we transmit it. However, since our communication signals have a large bandwidth (even more so for 5G), the same time delay does not correspond to the same phase shift for all frequencies. However, for a narrow band of signals close in frequency, we can approximately assume that a phase shift by the same amount for

the entire bandwidth corresponds to an equivalent time delay for all of them. We will make this approximation because it is easier to create a phase-shift (as seen later in the phase-shifted design) compared to creating a true time-delay.

As far as the transmitter requirements go, we just need to be able to phase shift the signal that is transmitted by an angle given by some input digital bits.

2.1 The Phase-Shifting Architecture

It is possible to perform the phase shifting at different points in the transmitter chain and these are accordingly named as LO-path phase-shifting, RF-path phase shifting, digital phase-shifting and hybrid phase-shifting. We will assume that our transmitter chain consists of just a DAC and a mixer (as discussed in the next chapter, this will be the final architecture on the signal path). The phase-shifter is a block that will require 4 quadrature signals (separated by 90°from each other) and will add the signals with different relative weights to achieve the required phase shifts.

In RF phase shifting, the phase shifter is added after the up-conversion. The advantage of this is that the circuitry that performs the up-conversion can be common to the different paths that go to the antenna. This saves on hardware and area. However, the phase shifting method that we are using requires 4 quadrature signals (separated from each other by 90°) and this has to be generated specifically after up-conversion. Furthermore, the phase shifter is a lossy block and extra gain stages will have to added to overcome this loss after up-conversion. Another disadvantage is that the RF signal has a large bandwidth and the phase-shifter's operation must be invariant across this bandwidth.

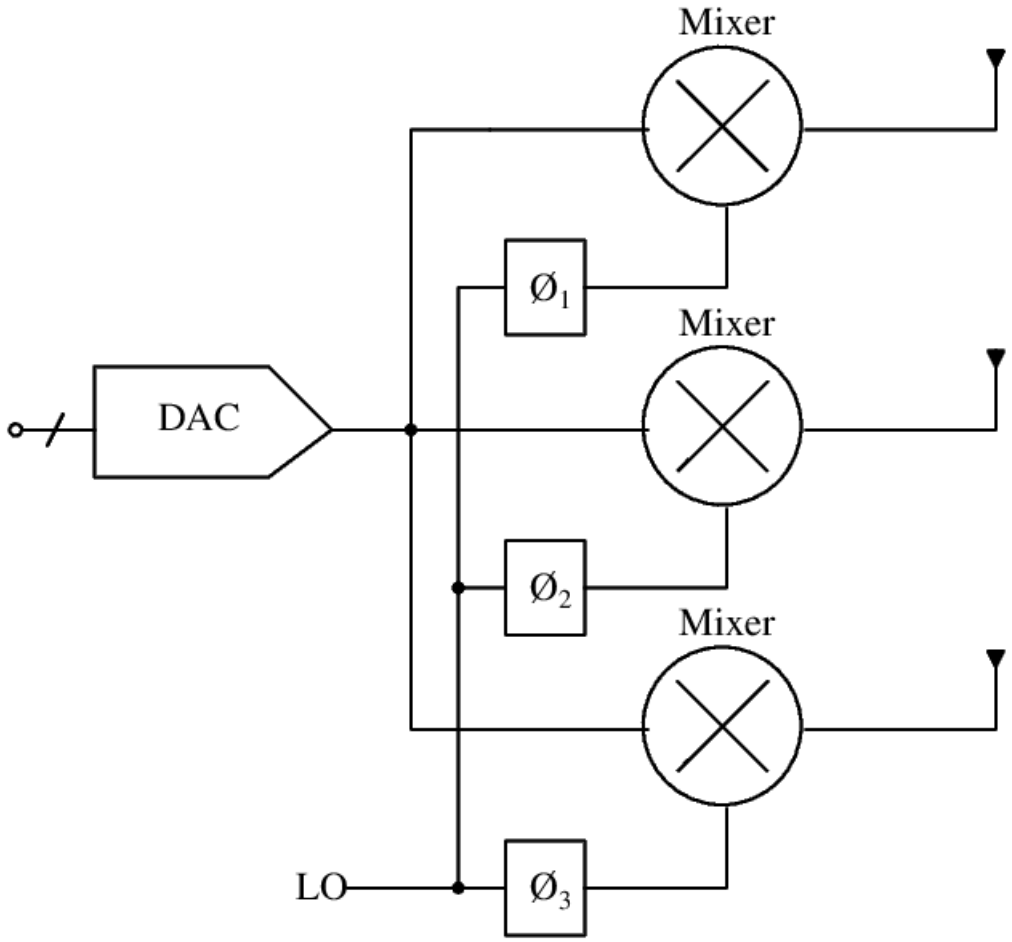

Figure 2.1: LO Phase Shifting

In LO phase-shifting, the phase shifter is added on the LO path and changes the phase of the LO signal and thus effectively, the RF signal too after up-conversion. Since we anyway have 4 quadrature LO signals to drive the I-Q mixer, it is easier to add the phase shifter in the LO path. Furthermore, since we have only a single-stage transmitter using a power mixer, if we were to add the phase shifter after the mixer then we would have to add another gain stage (a power amplifier) to make up for the loss in power. This will make the use of the single-stage power mixer redundant. With the phase-shifter in the LO path, it also needs to only work for one frequency and we do not have the design constraint of maintaining its behaviour over a large bandwidth like RF phase shifting. For these reasons, we have added the phase shifter in the LO path.

Digital and hybrid phase-shifting are more flexible and require much higher power and area as we would require more channels to be processed at baseband itself and hence, multiple DACs.

CHAPTER 3

Transmitter Architecture

The overall transmitter consists of two paths - the signal path and LO path. The signal path consists of the circuitry that filters and then up-converts the baseband signal to RF while the LO path generates the 4 required LO signals and performs the phase-shifting.

3.1 Possible Transmitter Architectures

3.1.1 Mixer and Power Amplifier

In this type of architecture there is a separate mixer and power amplifier. The separate stages aim to perform different functions of up-conversion and amplification and this makes it easier to design. However, it is hard to handle 26GHz signals and pass it through multiple stages that have their own parasitics. To resonate out the input capacitance of the subsequent stage, we also need inductors at the output of every stage. This uses up more space and power. If the blocks are far from each other, we will also need matching networks between them. [4][8][10][6]

3.1.2 NMOS Input Pair Power Mixer

Considering the limitations of the previous architecture, it could be possible that using a single stage to both upconvert and amplify the signal might work out more resource-efficient. A single power-mixer will only need one set of inductors at the output unlike the previous architecture where we would need inductors at the output of every stage. Furthermore, since both stages are combined into one we can reduce power consumption too. The drawback is that we have multiple functions we need to achieve and this might limit the 1dB compression point of the transmitter. [9][2][11]

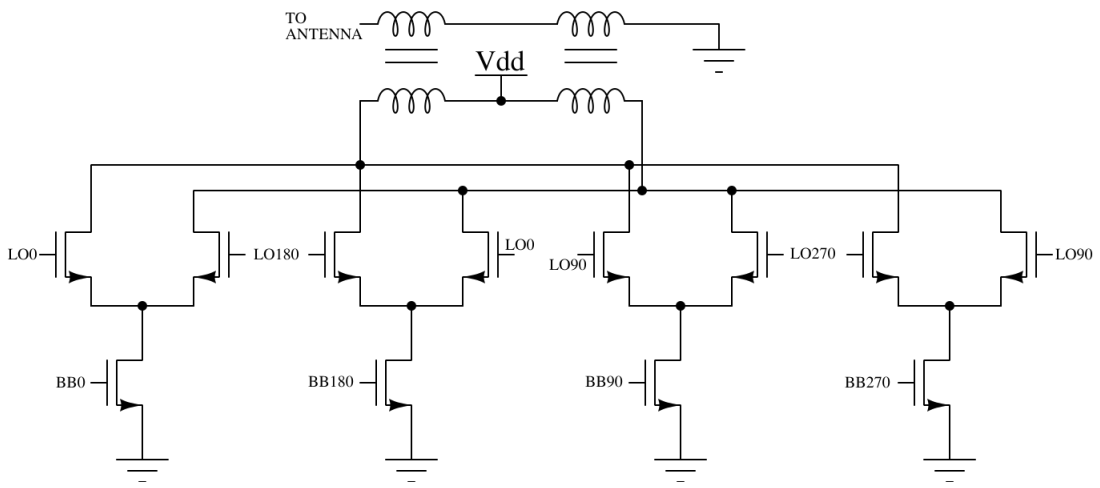

Figure 3.1: Power Mixer with NMOS Input Pair

Using an NMOS input pair and NMOS switches would be the natural choice for such a power-mixer (because of the benefits of an NMOS over a PMOS). The major drawback however, is that despite having an inductor at the output, we cannot have arbitrarily large swings at the drain of the NMOS switches. We would like to limit the overall voltage across any two nodes of the device to be about 1.2V so that we are within the safe operating region of it. Larger swings may lead to breakdown or deviation from the model file in actual operation. Since the mixer switches have their bulk grounded, this severely limits the swing we can tolerate at the drain. If VDD itself is 1.2V then the VDS of the device is 1.2V without any swing. This forces us to use a lower VDD that will limit the linearity of the mixer.

3.1.3 NMOS Input Pair Folded Cascode Power Mixer

One way to counter the above problem is to use a folded-cascode power mixer with an NMOS input pair and PMOS switches. This has two advantages. The first advantage is that the DC operating points move up and then down as we go from the transconductor to the switches. This allows more room for the signal to swing at different nodes and can thus have potentially better linearity. The other advantage is that since we are using PMOS switches, the bulk doesn't have to necessarily be connected to VDD or GND and can be connected to the device's source or even to another bias voltage. This allows for more swing at the drain node without letting the drain-bulk or drain-source voltage getting too large.

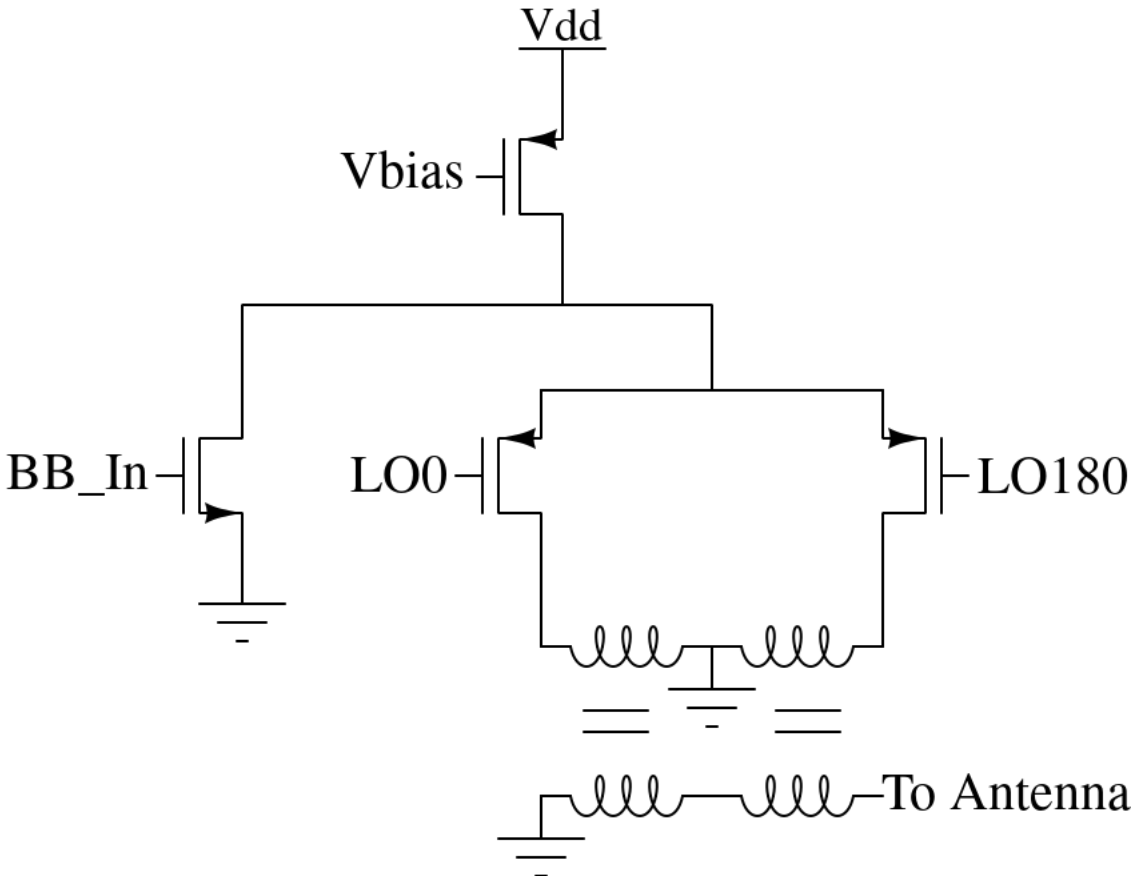

Figure 3.2: Folded Cascode Single-Balanced Mixer with NMOS Input Pair

There is however, increased capacitance at the drain of the transconductors (due to the current source) and this can limit the linearity of the mixer. The PMOS switches also have smaller mobilities and hence need to be of larger sizes to make up for it.

3.1.4 NMOS Input Pair Power Mixer with Deep N-Well Devices

With deep N-well NMOS devices we can freely tie the bulk voltage of the switches to any bias voltage we want. This allows us to use NMOS devices for the switches and overcome both the drawbacks mentioned for the folded-cascode. After optimizing all the architectures, it was found that this one was able to achieve the best 1dB compression point while being the most area and power efficient.

3.2 Signal Path

The block diagram of the signal path can be seen below

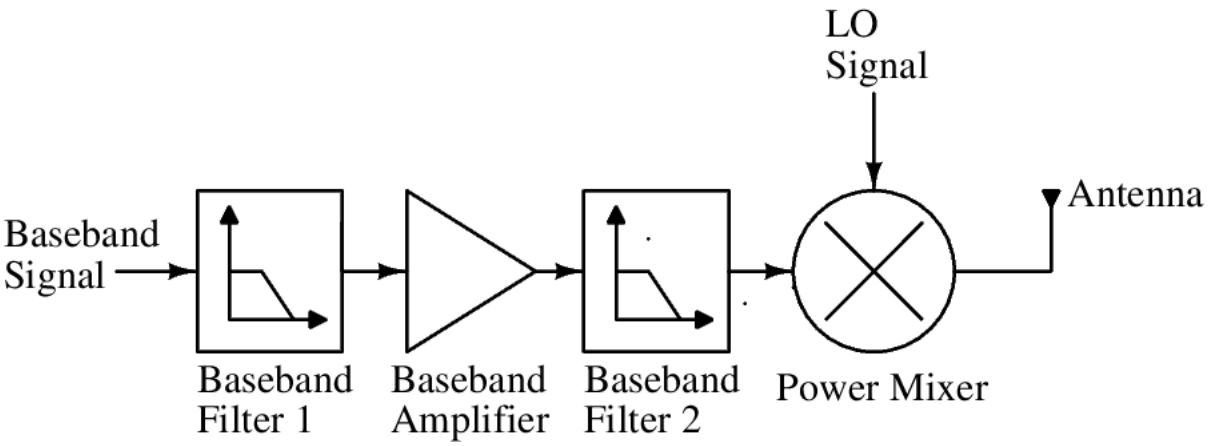

Figure 3.3: The Signal Path

The primary function of the signal path is to up-convert the baseband signal to RF by mixing it with the LO signal and then amplifying it before sending it to the antenna. Other requirements are to filter the baseband signal (since it is generated by a DAC and can have unnecessary higher harmonics) and to amplify the baseband signal enough to drive the mixer.

To save space and power, the up-conversion to RF and amplification functionalities are integrated into one power-mixer (instead of a conventional mixer + power amplifier architecture). The power mixer is a Gilbert cell type mixer with the output matched to 50Ω. The matching is done using a balun that also facilitates differential to single-ended conversion of the output signal.

On the baseband side, the filtering is achieved through two RC low pass filters that remove higher harmonics generated by the DAC. Since, we are working with an input current-mode DAC for the baseband signal we are able to integrate these filters at the input and output of a trans-impedance amplifier that amplifies and generates the voltages required to drive the mixer input.

3.3 LO Path

The input single-ended LO signal must be converted to 4 quadrature signals and phase-shifted based on the input digital phase bits. The signals must also be amplified enough to drive the mixer switches. A larger LO amplitude results in a larger output referred 1dB compression point for the mixer. The major restriction while trying to achieve this is to maintain symmetry between the 4 LO signals at all times and to avoid any unnecessary mixing of them.

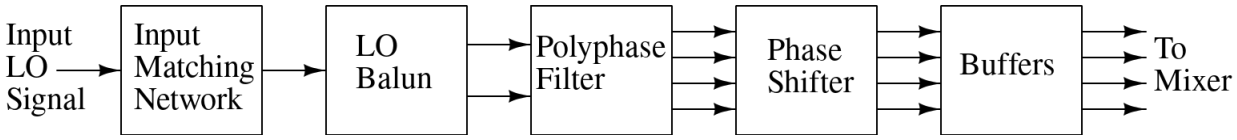

Figure 3.4: The LO Path

The amplification is achieved by buffers placed at different points in the LO path. The LO balun splits the incoming LO signal into differential 0°and 180°signals. These signals then pass through the poly-phase filter to generate the 4 quadrature LO signals. The phase-shifter block then mixes these 4 signals (appropriately weighted) to create the required phase shifts. The 4 signals then pass through 2 buffers before being fed to the mixer switches.

CHAPTER 4

Signal Path Implementation Details

The chapter will discuss the schematic and layout level details of the different blocks in the circuit.

4.1 Power Mixer and Output Balun

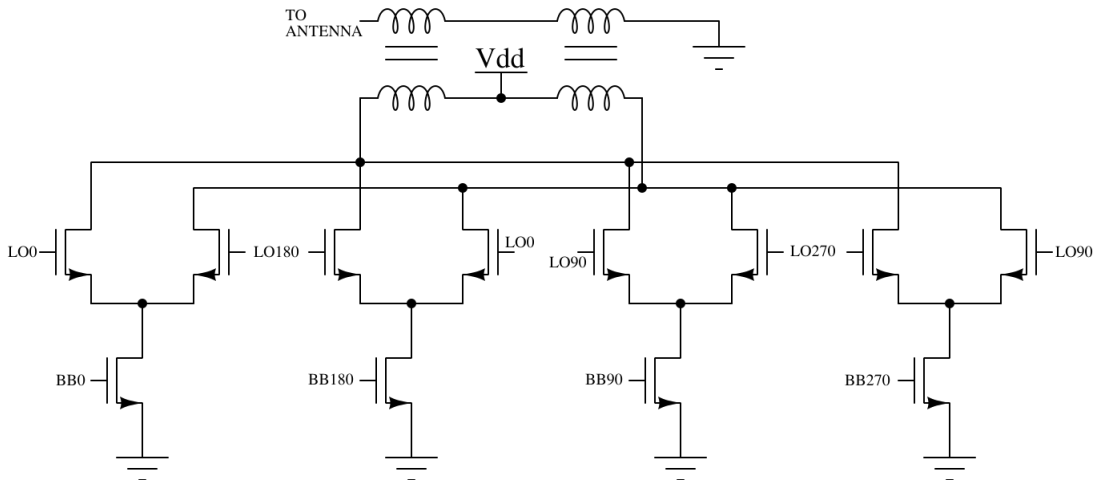

Figure 4.1: Power Mixer

The power mixer is a Gilbert cell type active mixer that up-converts the baseband signal applied to the gate of the trans-conductors using a switching pair controlled by differential LO signals. Four such single-balanced mixers are used to perform differential I-Q modulation and generate the differential output RF signals. The differential RF signals generated are then fed to a balun that performs differential to single-ended conversion before passing it to the antenna.

The main design specification to be met while designing the power mixer was to achieve as high a 1dB compression point (output referred) as possible. A major limitation while trying to achieve this was to ensure that the voltages at different terminals of the MOSFETs do not exceed their maximum permissible values. If VDD was chosen to be 1.2V then we can see that even without any output swing, the drain-bulk voltage of

the mixer switches is 1.2V. To counter this, the bulks of the mixer switches were tied to a bias voltage of 300mV so that the operating point drain-bulk voltage of the switches are 900mV. This bias voltage is generated using a resistor divider. Small changes in the bulk voltage do not have a significant effect on the gain or linearity of the transmitter and can be tolerated.

Another design challenge was to choose the turns ratio and inductance of the balun. This has to be done to maximise the 1dB compression point while also ensuring that the output can easily be matched to 50Ω. If the power mixer compresses at a certain output voltage swing then minimizing the output impedance seen by the mixer will maximize the output power it can generate. However, if the output impedance is too small then it will be harder to match it to 50Ω. Another constraint that further makes this harder is that we require the differential side of the balun to be at resonance to maximize the gain of the mixer while we have no control over the imaginary part of the impedance on the single-ended side. Different values of turns ratio for the balun were tried to maximize the 1dB compression point of the mixer.

We can have independent control over switch and transconductor currents by using a helper current source. However, it was found that when a helper source is used, there is a loss in gain of the switches and increased capacitance at the drain of the transconductor that led to an overall dip in the output referred 1dB compression point. Thus, the helper current source was not used in the final circuit. Overall, an increase in the bias current through the circuit improves its linearity with an increase in power consumption. Extremely large value of bias currents would however negatively impact the linearity since it will get harder for the switches to switch the current from one side to the other.

Laying out the power-mixer is quite challenging since there are 4 single-balanced mixers that all need to be connected symmetrically to the output. While this might be possible with longer metal lines that route to the output and maintain symmetry, such lines add unnecessary inductances at the output of the mixer and the voltage drop across them will not be transferred to the output through the balun. Shorter complicated connections at the output on the other hand either are not able to maintain symmetry or are extremely lossy (due to coupling between metal lines). To tackle this issue, the schematic of the power mixer was changed as follows:

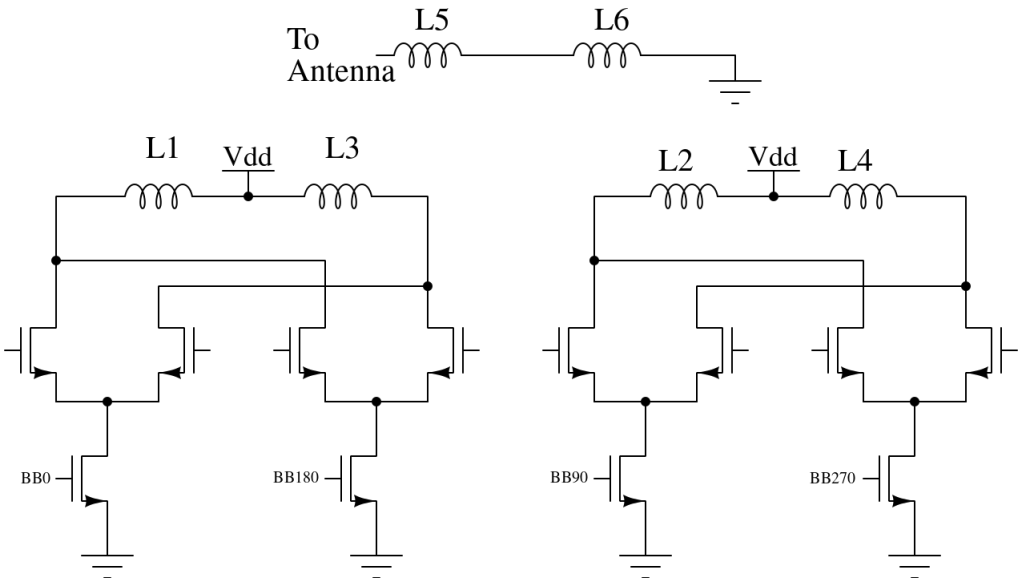

Figure 4.2: Power Mixer with two separate baluns. Note that L5 is coupled with both L1 and L2 while L6 is coupled with both L3 and L4

Earlier, in order to combine all 4 positive (and negative) outputs symmetrically before the balun, we needed longer metal lines. The longer metal lines had their own inductance and thus any current flowing through will cause a voltage drop that is not transferred through the balun. In this version of the circuit, each quadrature half of the mixer has its own primary coil and can thus have shorter metal lines to them while maintaining symmetry. While the current was added in the previous case to combine the outputs of the two quadrature halves, in this circuit the outputs are added as voltages in the secondary (single-ended) side of the balun.

Such a 3-port balun can be laid out by using 3 metal layers, the middle one being the single-ended side and the other two layers being the two differential inputs sides (from each of the quadrature halves). M8 and AP are used for the outer layers since they are more similar in terms of their electrical and magnetic properties while M9 is used for the middle layer that forms the single-ended output side of the balun. This way we can realise the same coupling that was show in the previous schematic where one inductor on the single-ended side is coupled with two inductors on the differential sides. This can be seen below.

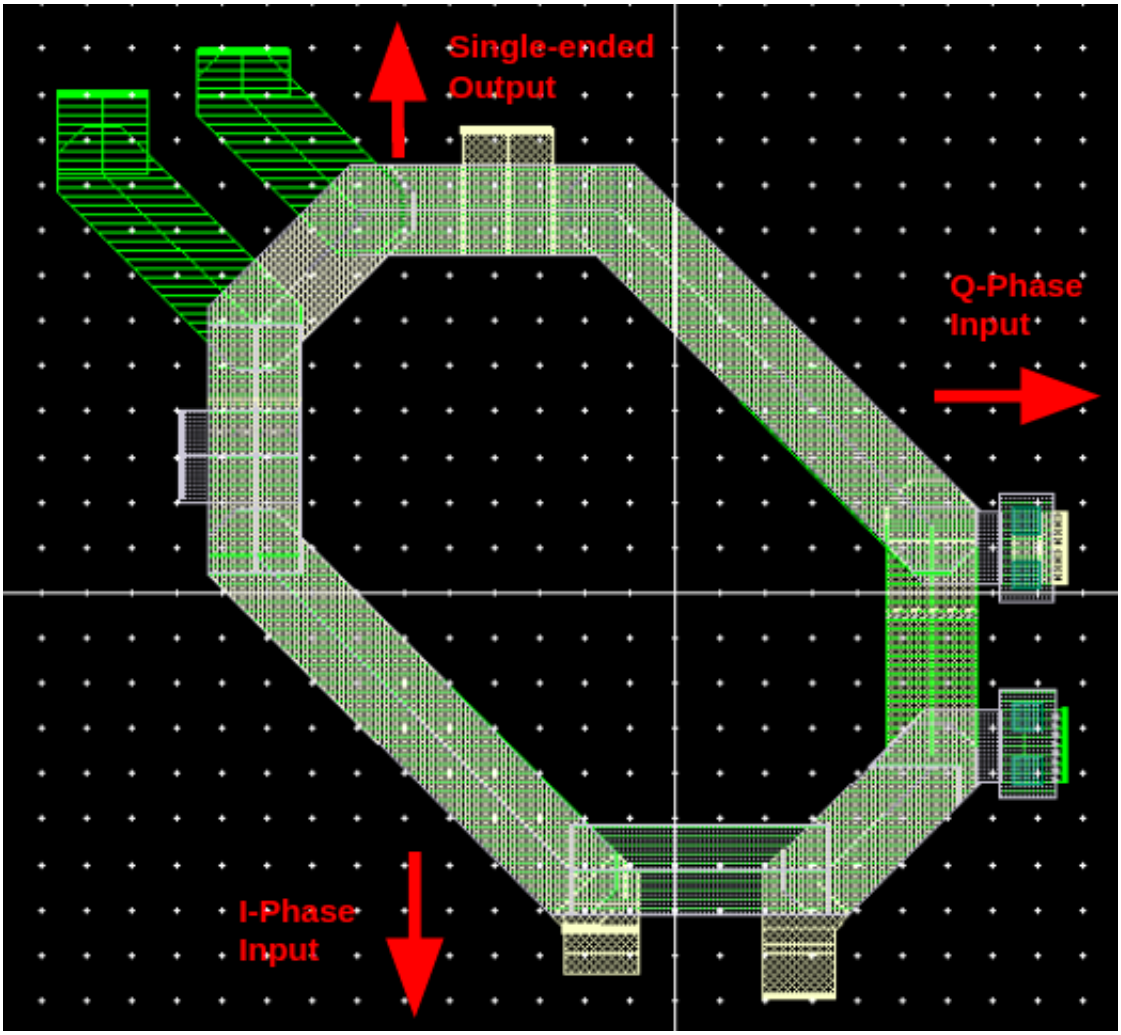

Figure 4.3: Output Balun: The single-ended side is on M9 (green) while the two differential inputs are on M8 and AP (both seen are different shades of white here)

Following the shape of the balun, the two quadrature halves of the mixer are also laid out in an L shape with the I-half laid out horizontally and the Q-half laid out vertically. The alternative is to keep both quadrature halves on opposite sides of the balun. However, considering that all the LO signals are generated and phase-shifted together, it will be quite wasteful in terms of area to separate them before feeding to the mixer. This would also have to be done symmetrically and can lead to unnecessary losses. The final layout of the mixer and balun together is as seen below.

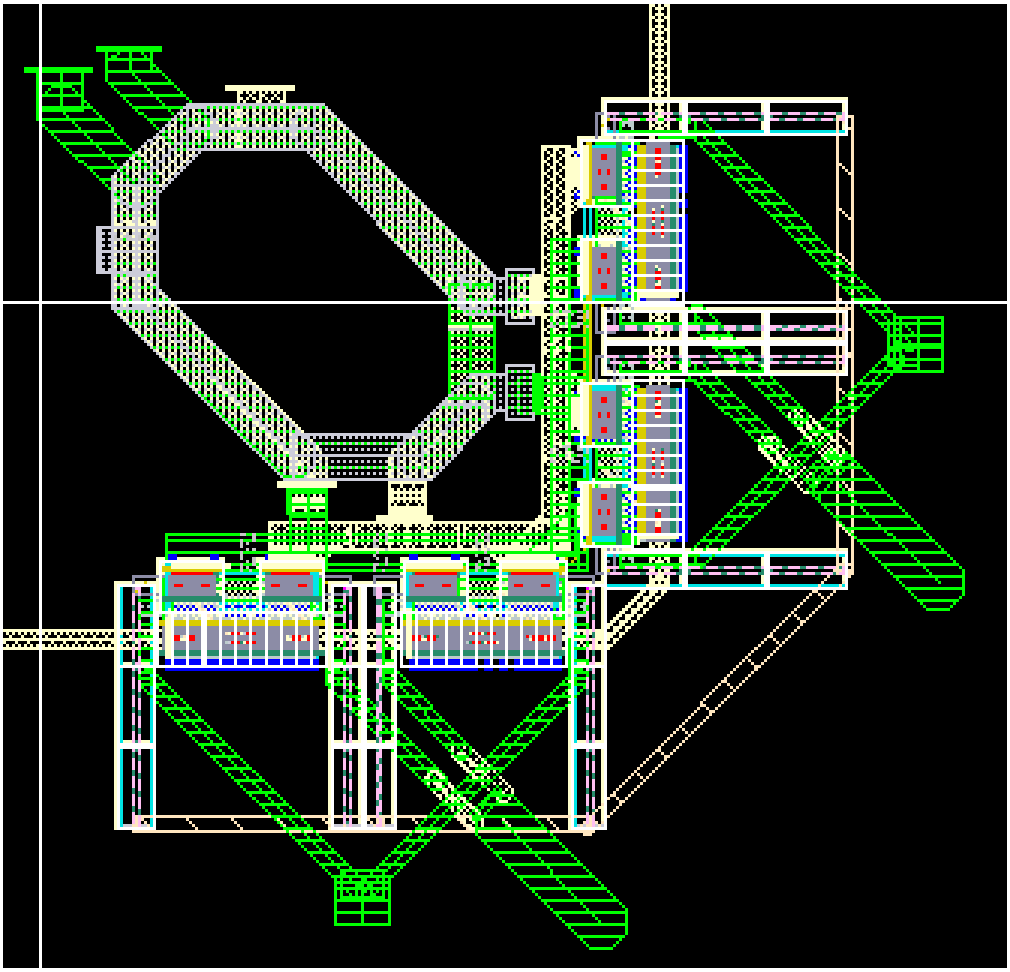

Figure 4.4: Output Balun with the 4 Single-Balanced Mixers

Symmetry must also be maintained while feeding the LO signals to the mixer switches. However, this is relatively easier since the buffers were designed with a series inductor between their output and the mixer switches' gates. Thus, any long metal lines that need to be laid out to maintain symmetry can be absorbed into this series inductor that resonates out the input capacitance of the mixer switches.

4.2 Baseband Filter and Amplifier

The baseband filter and amplifier consists of a cascade of two RC filters and one transimpedance amplifier that converts the input baseband current to a voltage before feeding it to the mixer transconductors. The circuit diagram is given below:

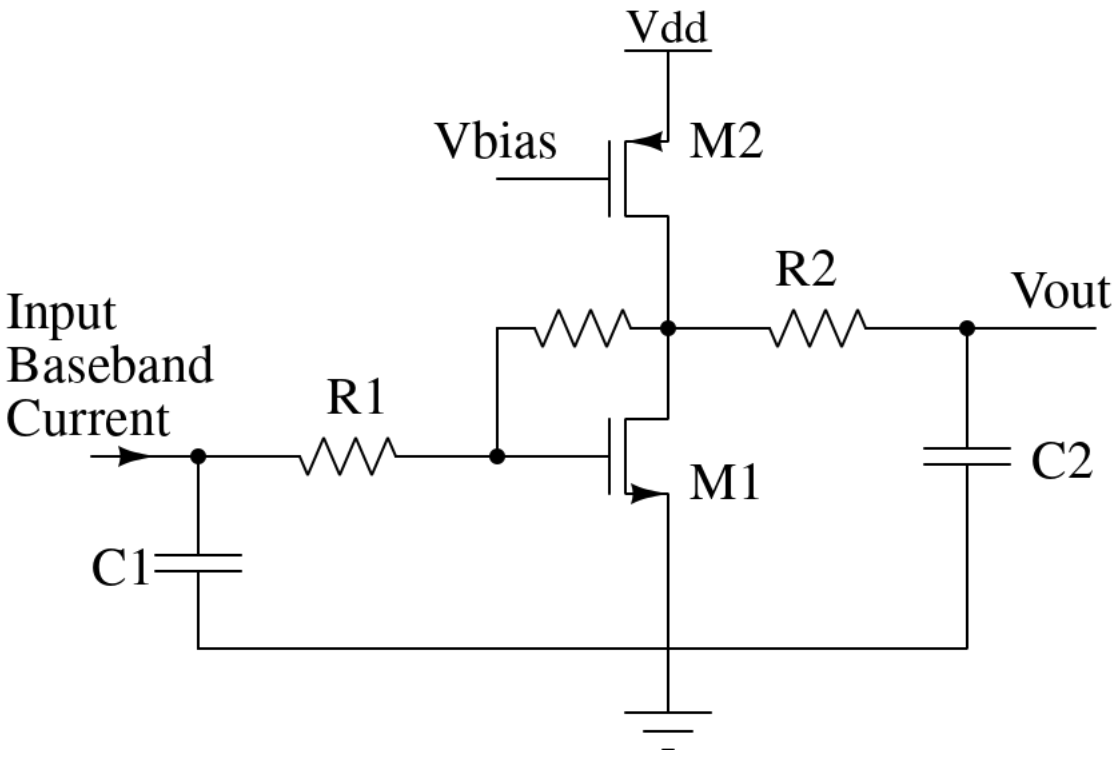

Figure 4.5: Baseband filter

The two RC filters create a -40dB/decade roll in the transmitter response. This will remove any higher harmonics at the output of the DAC (in the input baseband signal). In the final circuit, it was seen that the input capacitance of the mixer transconductors was large enough so the capacitor C2 was not required. The values of R and C also had to be re-adjusted after layout since the long routings from the bondpads to the filter added their own parasitics.

Vbias is generated from a current mirror that uses an ideal reference current source (fed to the IC through a bondpad). The sizes of the MOSFETs were chosen so as to minimize the power consumption in the circuit while providing enough gain to the input signal to drive the mixer.

CHAPTER 5

LO Path Implementation Details

. The amplifier ensures that the baseband signal is strong enough to drive the mixer and achieve the required output power.

5.1 5-bit Phase Shifter

The phase shifter takes in 5 digital input bits and the 4 quadrature LO signals and then phase-shifts them according to the digital bits. The idea behind the working of the phase shifter is that given the 4 quadrature LO signals, we can arbitrarily phase shift them by any amount by adding two signals with different weights. This is easier to achieve in current-mode. As an example, if we were to consider 4 input lines as being the 4 input quadrature LO signals (input0, input90, input180 and input270) and the 4 output lines (output0, output90, output180 and output270) to be as follows - output0 is created from input0 and input90 by combining them (this can be done in current mode by just connecting them to the same node), output90 is created from input90 and input180 by combining them and similarly for output180 and output270 too. We see that by doing this, each of the output lines will be phase-shifted by 45°from the corresponding input lines. This is based off the methodology used in [12]

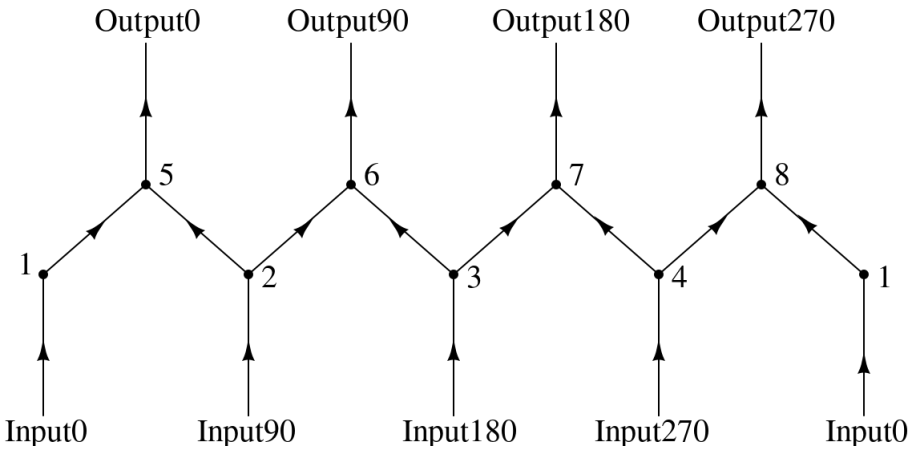

Figure 5.1: Achieving a phase shift of 45°by adding adjacent quadrature currents. Output0 will be phase shifted by 45°with respect to Input0

However, if we look at output0 then it will have only half of input0 and input90 that are added together in quadrature (There is a division of current at nodes 1,2,3 and 4). Thus, the actual output0 will be scaled by $\frac{1}{\sqrt{2}}$ times the original input amplitude (when the currents add up at nodes 5,6,7 and 8, they will be added in quadrature and this accounts for the other factor of $\sqrt{2}$. We can similarly change the amount of current from each of the input phases to effect different amounts of phase change (in this example, both input phases had equal weight).

This can implemented in a circuit by using a trans-conductor to convert the input voltage LO signal to current and then using a variable number of switches to control the "weight" of the input phases that add to create the output. If an equal number of switches are turned on for both input0 and input90 then both will have equal weight and we will achieve a phase shift of 45°like the previous example. If the two input signals on the other hand have different number of switches turned on then we will be able to achieve other values of phase shifts. The control signals for the switches can be generated using digital circuitry that take the 5 digital control bits as input. Thus, every one of the 4 input signals are connected to every one of the 4 output nodes through multiple switches that are turned on based on how much phase shift we require. We can immediately see how to implement phase changes of 0°, 90°, 180°and 270°. One way to do it (for say, 90) would be to turn on all switches that connected input0 to output90, input90 to output180 and so on. Note that there can be multiple switches for each input even to do this simple rotation since switches can be reused for different bit settings. In general we can assume that an optimized scheme would require multiple switches to be turned on for every phase shift. The number of switches to be turned on has to be derived.

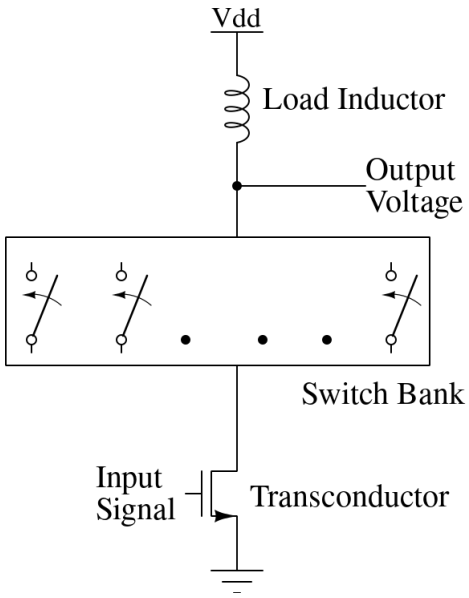

Figure 5.2: Path from one of the inputs to one of the outputs in the phase shifter. The complete phase shifter has a path from every input to every output

For the final phase shifter we have the following constraints to be maintained -

- Relative number of switches that are on for every bit setting must correspond to the correct phase shift that must be effected
- The total current at the output must be the same irrespective of the bit setting so that the gain of the circuit is always the same (this was not there in the previous example where the gain changed)
- For every bit setting, the number of switches that are on for every transconductor must be the same. This has to be done so that the operating point drain voltage of the transconductor is unchanged (otherwise the gain of the different paths might change). This is made more critical by the fact that the signals we are dealing with are quite large and changes in the operating point (even if its the drain) can have a significant effect on the gain of the circuit).

To help achieve this, some dummy switches are also added whose output does not go to the load. For example, if we have a bit setting where the output has higher amplitude than other bit settings then we can turn on the dummy switch in this case to reduce the output amplitude (by routing some of the input current to some other node) and ensure that the gain of the circuit is the same irrespective of the bit setting.

An extension of this above trick would be to realise that if we need to reduce the amount of current from an input flowing into the load by "x" amps then we can instead have "x" amps from the corresponding differential input flow into the load too. The advantage of doing this is that all the switches will have the load at the output and be

symmetric. If some switches do not have the load at the output then they will not see the same output impedance (or output swing) which causes some asymmetry between the switches. Note that we are relying on the switches being symmetric so that if the number of switches that are on are in the ratio 4:3 then the relative weights of the inputs that are added will also be 4:3.

To achieve the above mentioned constraints perfectly would require a large number of switches that will be wasteful and result in a more complicated layout. Instead, we will relax the constraint on the phase-shift that we achieve as long as the DNL is less than 0.5LSB. Since we have 5 bits, this corresponds to 32 combinations from 0°to 360°and thus an LSB of 11.25°. To find the number of switches we can frame this problem in the following way.

First we will frame a scheme to achieve angles from 0°to 45°. Thus, output0 will only require input0 and input90, output90 will only require output90 and output180 and so on. For angles from 45°to 90°we will just have to invert the weights from earlier. So, if we used N_1 switches for input0 and N_2 switches for input90 to achieve a phase shift of x then to achieve a phase shift of $90 - x$ we will use N_2 and N_1 switches corresponding to input0 and input90 respectively. Similarly, to achieve a phase shift in another quadrant (say $x + 180$) we will use N_1 switches for input180 and N_2 switches for input270. Thus, we just need to first create a scheme that works from 0°to 45°(and meet the required constraints) and then we can extend it to all other angles too.

For 0°to 45°, lets say we use N_1 switches from input0 and N_2 switches from input90 to create the required phase change at output0 (the same number of switches will be turned on for every output). Note that when we are doing this, output270 will require N_1 switches to be turned on from input270 and N_2 switches to be turned on from input0. Thus, input0 overall sees $N_1 + N_2$ switches that are turned on. From the constraints mentioned earlier we see that one requirement we need is:

$$N_1 + N_2 = Constant \tag{5.1}$$

The next constraint is that the output magnitude is constant across bit combinations. If the input amplitude of the signals is 1 (without loss of generality), the amount of current flowing into output0 from input1 is $N_1/(N_1 + N_2)$. The overall output magnitude has

to then satisfy:

$$\left(\frac{N_1}{N_1+N_2}\right)^2+\left(\frac{N_2}{N_1+N_2}\right)^2=Constant \tag{5.2}$$

Or equivalently, (using 5.1)

$$N_1^2+N_2^2=Constant \tag{5.3}$$

The final constraint is of course the phase shift that needs to be effected and is thus,

$$tan^{-1}\left(\frac{N_1}{N_2}\right)=x^\circ \tag{5.4}$$

As mentioned earlier, since it hard to achieve these constraints with just two variables, we will add a third variable N_3 which is the number of switches of input180 that will be turned on to connect to output0. The number of switches that turned on between input0 and output0 will also be increased by N_3. However, the effective current flowing into output0 from input0 is still proportional to N_1. Only equation 5.1 is now changed as follows:

$$N_1+N_2+2N_3=Constant \tag{5.5}$$

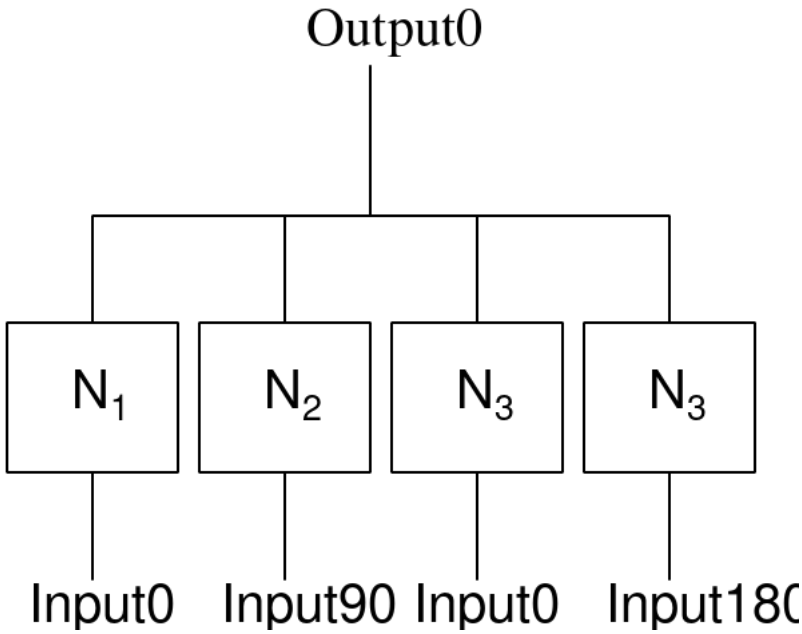

Figure 5.3: Phase Shifter Block Diagram for a phase shift from 0°to 45°(with respect to one output)

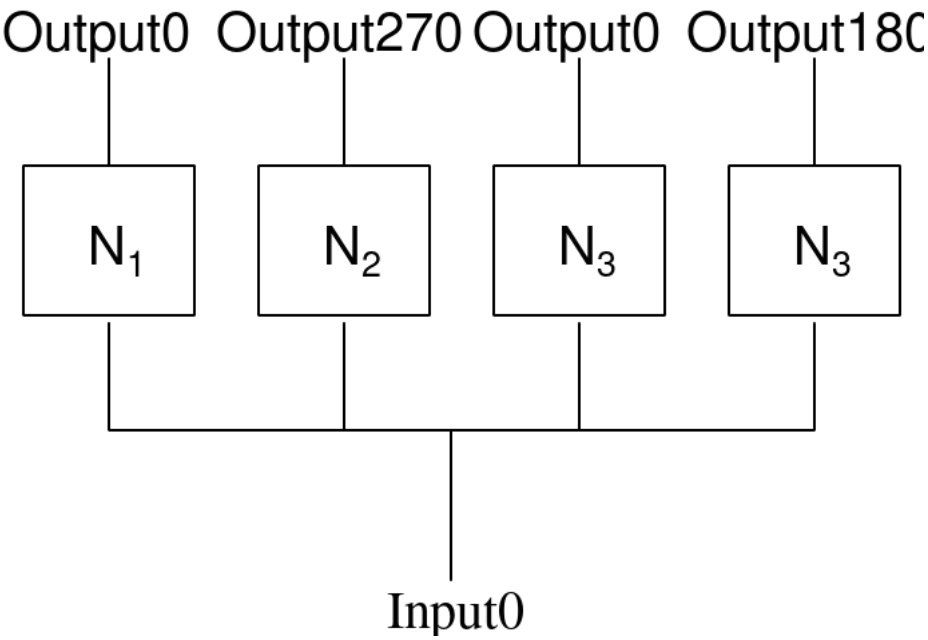

Figure 5.4: Phase Shifter Block Diagram for a phase shift from 0°to 45°(with respect to one input)

The values of these variables were found to minimize the number of switches and the DNL (and also the complexity of the digital circuitry required). As mentioned, every input is connected to every output through a "group" of 4 "types" of switches. Each "type" of switch requires the same control signal (generated by the digital circuitry). Each type of switch itself consists of multiple switches. The first type has 1 switch, the second has 2, the third has 3 and the fourth has 8. A combination of these can achieve any phase shift required. To simplify the digital circuitry, the first three input bits (out of 5) decide which of the 45°sectors we are in while the other two bits decide the final angle (between 0°and 45°). The final theoretical phase shift results achieved can be seen below:

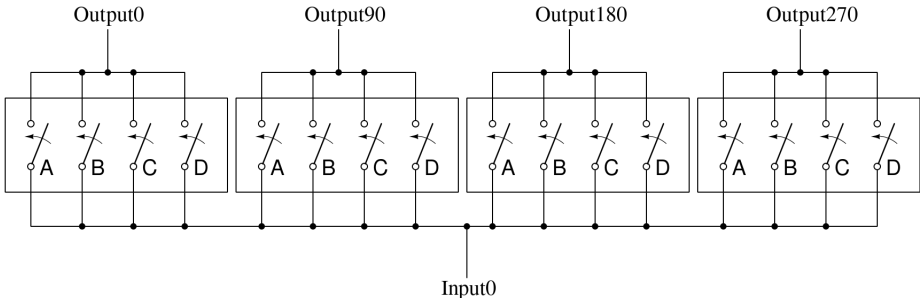

Figure 5.5: Connections of switches from Input0. The same connections will be made from input and hence, every output is also connected to 4 "groups" of switches. Each switch (type A, B, C or D) itself consists of multiple switches. Switches of the same type (A,B,C,D) have the same number of switches within them (1,2,3 or 8). There are 16 digital control signals needed to control these switches

Bit Setting	Phase	DNL	OP1dB
0	0°	-	10.5
1	8.21°	-0.27	10.54
2	20.93°	0.13	10.5
3	33.98°	0.16	10.59
4	45.21°	0.01	10.53

Table 5.1: Table showing achieved phase-shifts and the resultant output referred 1dB compression point.

Note that this 1dB compression point was for an ideal transmitter (just to simplify simulations to evaluate the performance of the phase-shifter) and not the actual one. The final achieved 1dB compression point will be different from this.

As we can see, we were able to achieve a DNL that is less than 0.5LSB. The variation in the output referred compression point is also quite less (since we ensured that the gain of the phase shifter is roughly constant across bit combinations). The above values will extend to all other 45°sectors too.

Since there are a large number of switches, the layout is quite complicated and it is close to impossible to maintain complete symmetry. The switches (which are small in size) are hence closely integrated together so that any asymmetry will be minimized too.

As mentioned earlier, every "group" of switches has (1 + 2 + 3 + 8 =) 14 switches. All of these switches have the same input and output nodes and can thus be connected together. The different "types" of switches will have different control signals that can

easily be routed in any way since they are digital signals. Thus, a "group" switches are very closely laid out together first (a common deep n-well was also manually laid out for them to bring them even closer). In total, we have 16 "groups" since each of them connect one input to one output. The "groups" are then laid out in a 4x4 matrix format where the input lines run horizontally and the output lines run vertically. This minimizes coupling between them and makes it easy to keep track of different switches while laying them out. This can be seen below:

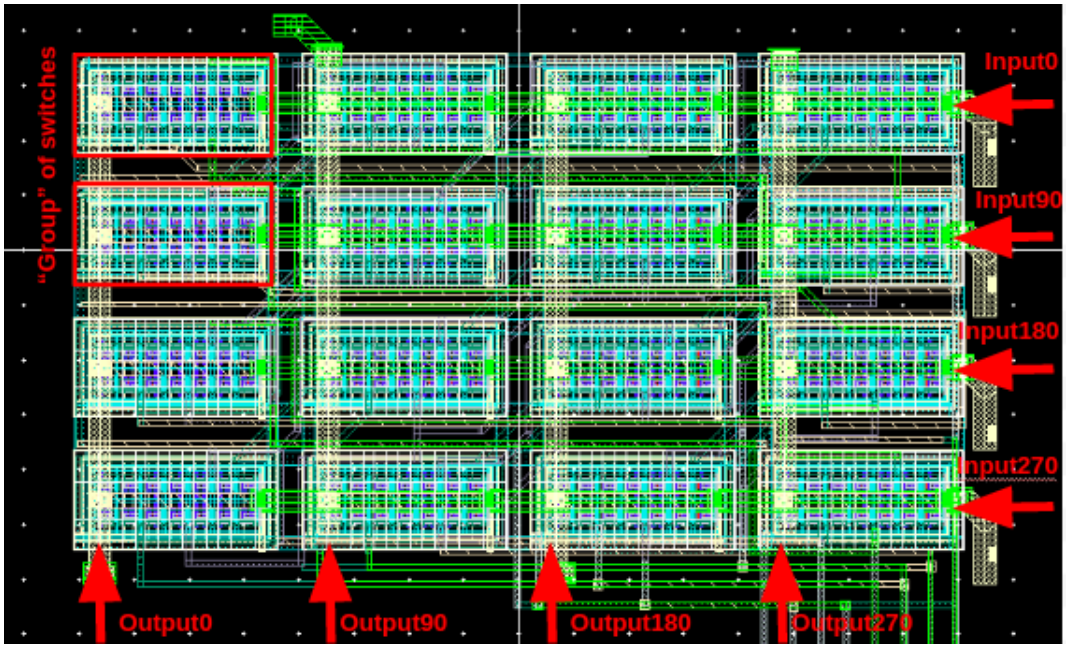

Figure 5.6: Phase Shifter Layout: The red boxes highlighted on the top left indicate a "group" of switches. There are in total 16 such "groups". The input LO lines run from left to right while the output LO lines run from top to bottom (as indicated by the red arrows). This way every input line is connected to every output line through a "group" of switches.

As for the design parameters to be optimised, it was found that smaller switches had smaller parasitics and hence lower losses (especially at 26GHz). Smaller switches also allowed the layout to be compact which was a very important consideration since there are an extremely large number of switches. The transconductor and bias current could be made large to improve the gain of the circuit depending on the power consumption we could afford.

5.2 Polyphase Filter

The circuit of a polyphase filter looks as follows:

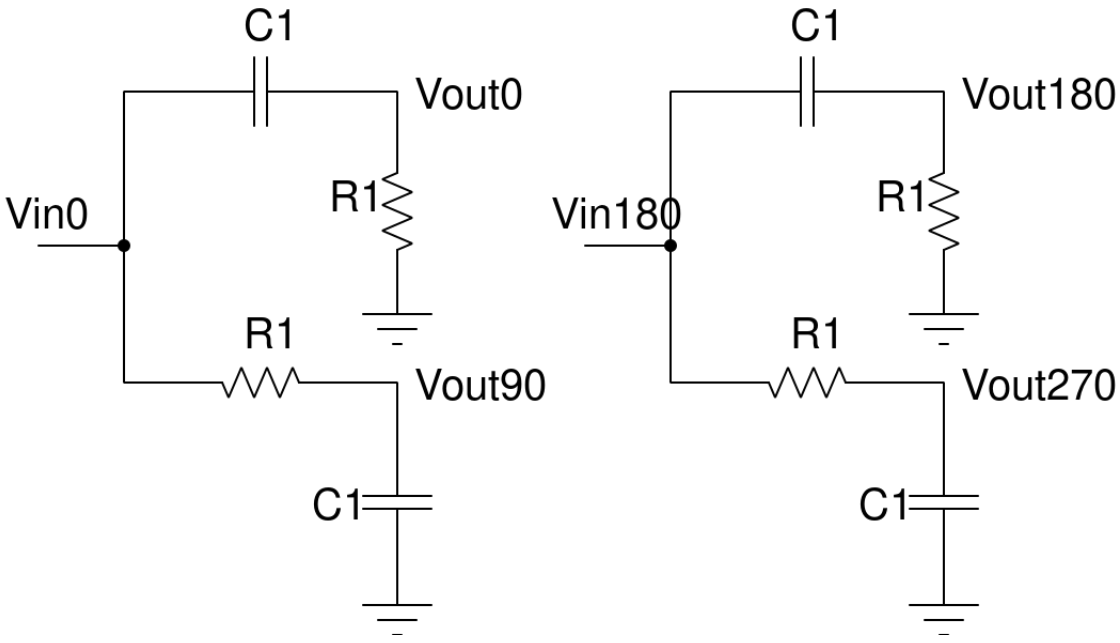

Figure 5.7: Polyphase Filter: Generates the 4 quadrature LO signals from an input differential LO signal

It works on the principle that if the values of R1 and C1 are chosen properly then it will be able to achieve phase changes of +45°and -45°for each of the differential inputs and thus result in 4 quadrature signals. To reduce the effect of process variation and mismatch, each of the resistors and capacitors have a multiplier of 3. The capacitance to substrate in the capacitors did break the symmetry however and had to be compensated for by adjusting the values of R and C. The final layout also had further asymmetry due to the grounds not being ideal. We would have ideally liked to connect the grounds of the two differential halves together first so that any signal current circulates between them but it is quite hard to do this with 4 branches.

The values of R an C were chosen so that they approximately occupied the same amount of area. This helped to keep the layout symmetrical.

5.3 Buffers and Inductors

The buffers are designed as CMOS inverters with both an NMOS and a PMOS. This is done because we also need the PMOS to push the signal down to ground. A downside of this however is the increased input capacitance the circuit offers. This does work better considering that we have used series inductors at the outputs of the buffers and hence do not need an inductor that connects to the supply from the drain. The advantage of series inductors is that in some cases there is anyway a long path from one stage to another and this can be modelled as a series inductor. This way, we don't need to use space on laying out an explicit inductor. It is however, challenging to minimize coupling between these inductors and maintain symmetry across the 4 lines.

The explicit inductors used for the buffers single-turn inductors on M9 as seen in the layout below:

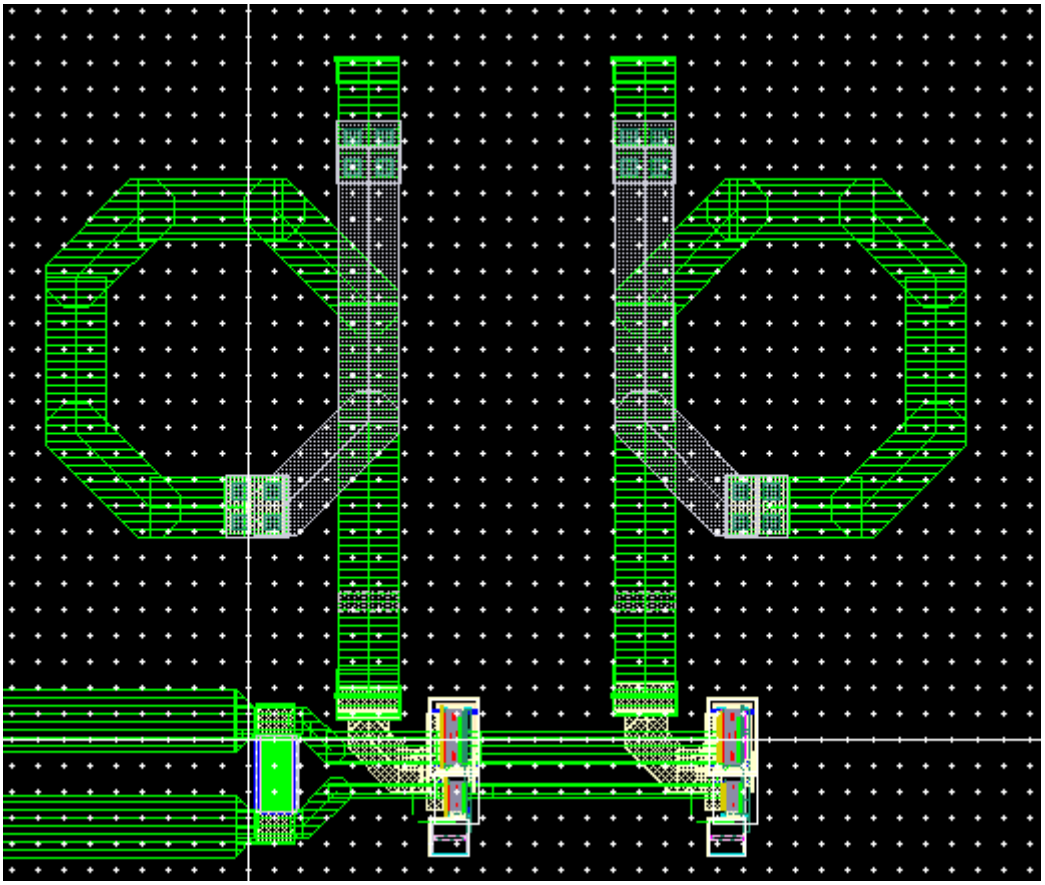

Figure 5.8: Differential LO Buffer with Inductors

5.4 LO Balun

The balun on the LO side converts the input single-ended signal to differential ones. It needs to ensure that the two output signals have equal magnitude and are 180°apart. A standard balun looks as follows:

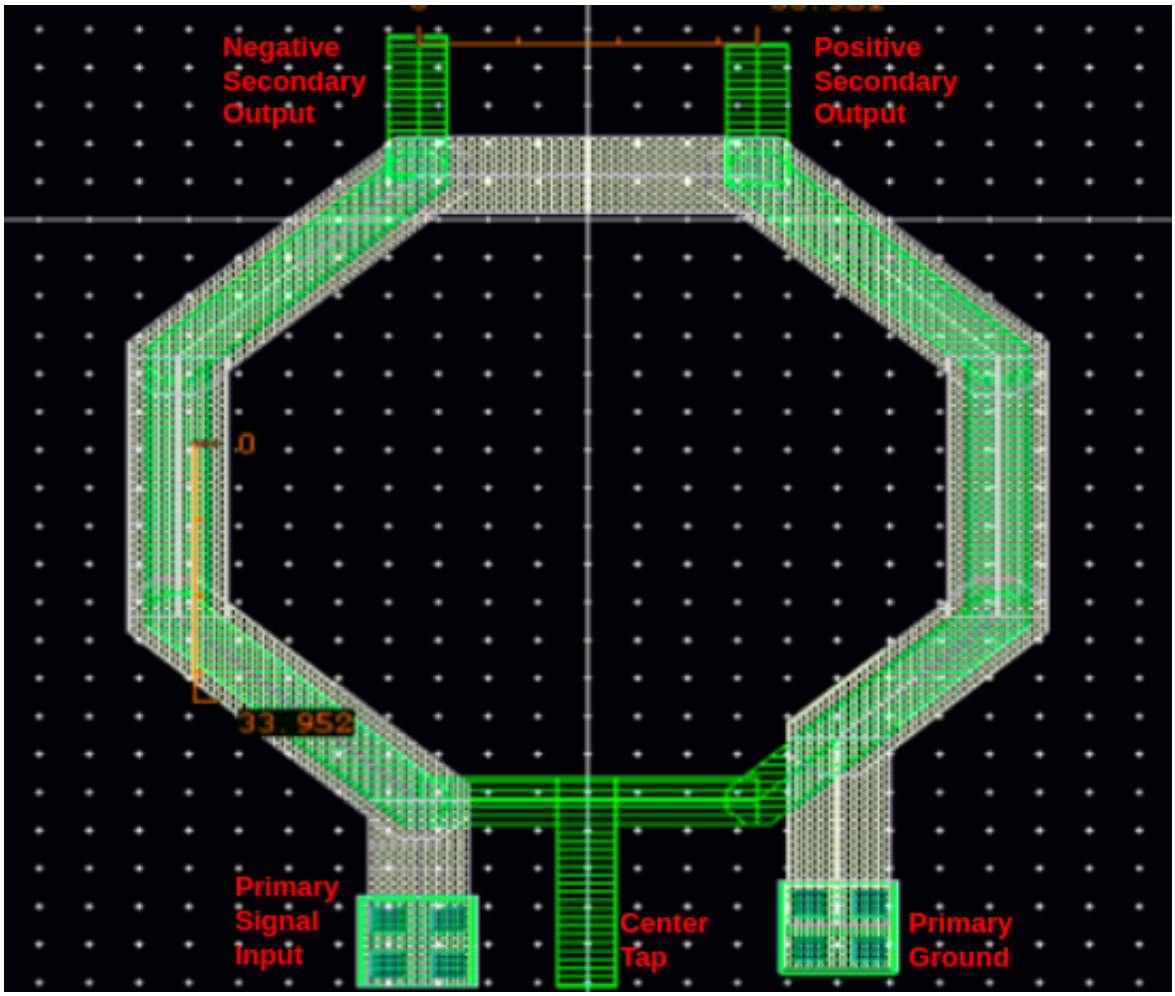

Figure 5.9: Balun

In the above layout the primary coil is on M8 (white) while the secondary coil is on M9 (green). Overlap of the two layers creates the coupling that allows the signal to be transferred from the primary to the secondary. The secondary coil also has a center tap that would be connected to AC ground.

However, there is an inherent asymmetry in this structure due to the fact that the positive secondary output overlaps with the primary ground while the negative secondary output overlaps with the primary input. If the output signals are $+V$ and $-V$ and the

input signal is $+U$ then the potential difference between the positive secondary output and the primary ground is:

$$V_2 - V_1 = (+V) - (0) = +V \tag{5.6}$$

While the potential difference between the negative secondary output and the primary input is:

$$V_2 - V_1 = (-V) - (+U) = -V - U \tag{5.7}$$

Due to this difference in voltages, the amount of current that flows through parasitic capacitances between the two layers differs. This causes an overall magnitude and phase difference between the two differential output signals.

One way to counter this would be to introduce an additional asymmetry that can negate the earlier asymmetry due to the different voltages on the two sides. A few ways in which this can be done is as follows:

- Making the primary coil asymmetric: This can done by making one half of the primary coil shorter than the other.
- Moving the center tap: Instead of keeping the center tap at exactly the middle of the secondary coil, it can be moved to either side to add asymmetry.
- Allowing some swing at the center tap: Ideally we would connect the center tap to ground or connect a large capacitor from it to ground. If this capacitor was made smaller however, the center tap will not be exactly at ground and it could add the necessary asymmetry.

The following balun was finally used where the first two methods described above were used to counter the inherent asymmetry in the balun layout.

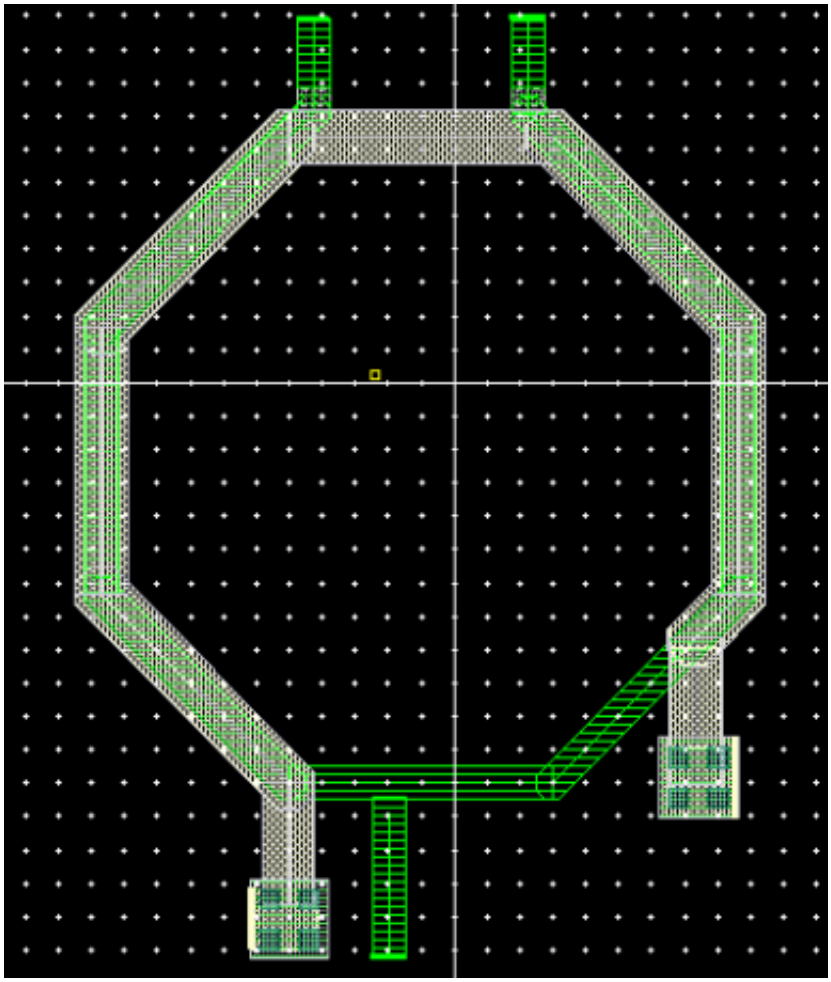

Figure 5.10: Balun adjusted to fix the asymmetry

However, this still does not completely create symmetric outputs. The final layout was made to prioritise achieving a 180°phase difference between the two outputs instead of making the output swing equal. The reason for this is that as the signal go through subsequent stages in the LO path, the smaller swing signals experience more gain while the larger swing signals experience less gain. Thus, the amplitude mismatch can be rectified to some extent as the signal progresses down the LO path. However, the subsequent stages also rely on the input signals being purely differential and hence, this can only fix small differences in output amplitude.

5.5 Digital Circuitry for the Phase-Shifter

The digital circuitry takes in 5 bits and has to create 16 control signals for the switches of the phase-shifter (as described earlier). The 16 control signals have a random com-

bination of minterms of the input bits and cannot be simplified in any way. As a result, the digital circuitry is quite large but can be density integrated since the delay doesn't matter to us and the sizing for the transistors can be minimum. This can be seen below:

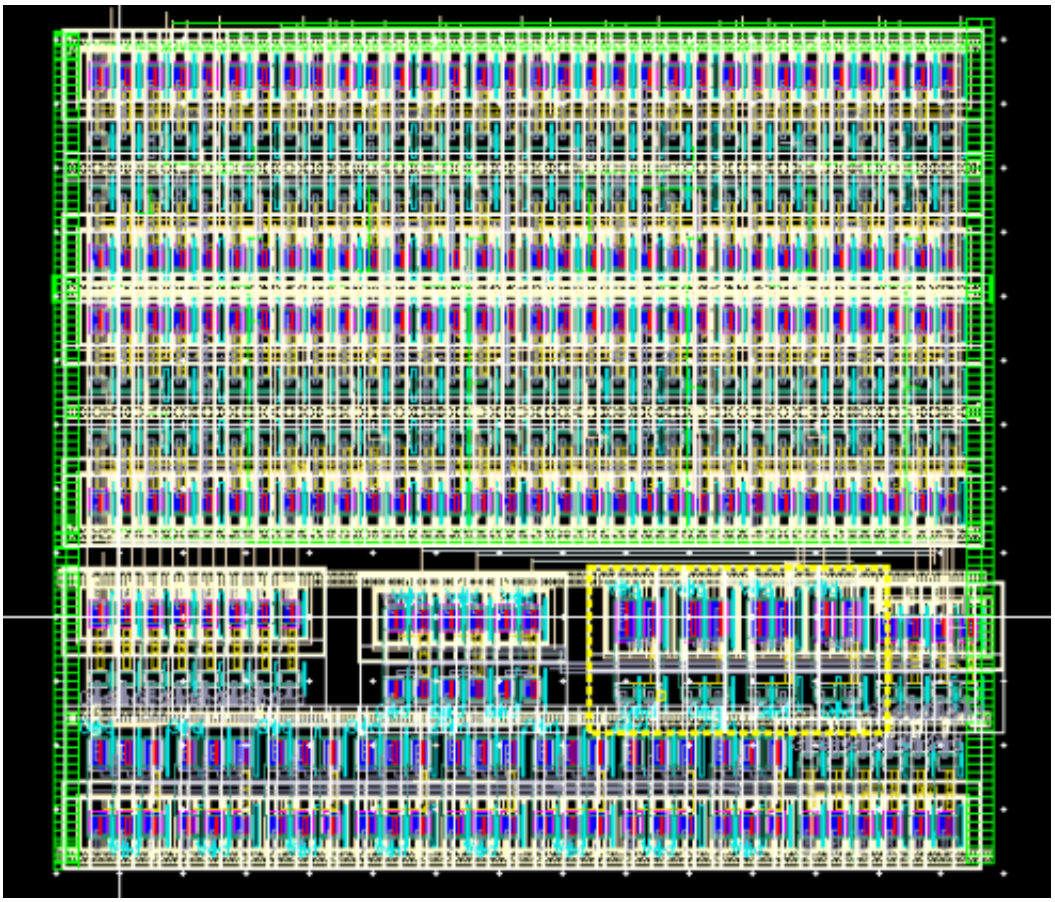

Figure 5.11: Layout of the Digital Circuitry

CHAPTER 6

Board and Bonding Details

6.1 Bond pads and Probe pads

The bond pads are used to connect to the digital and baseband signals and the supply lines. The probe pads on the other hand connect to the input LO and output RF signals.

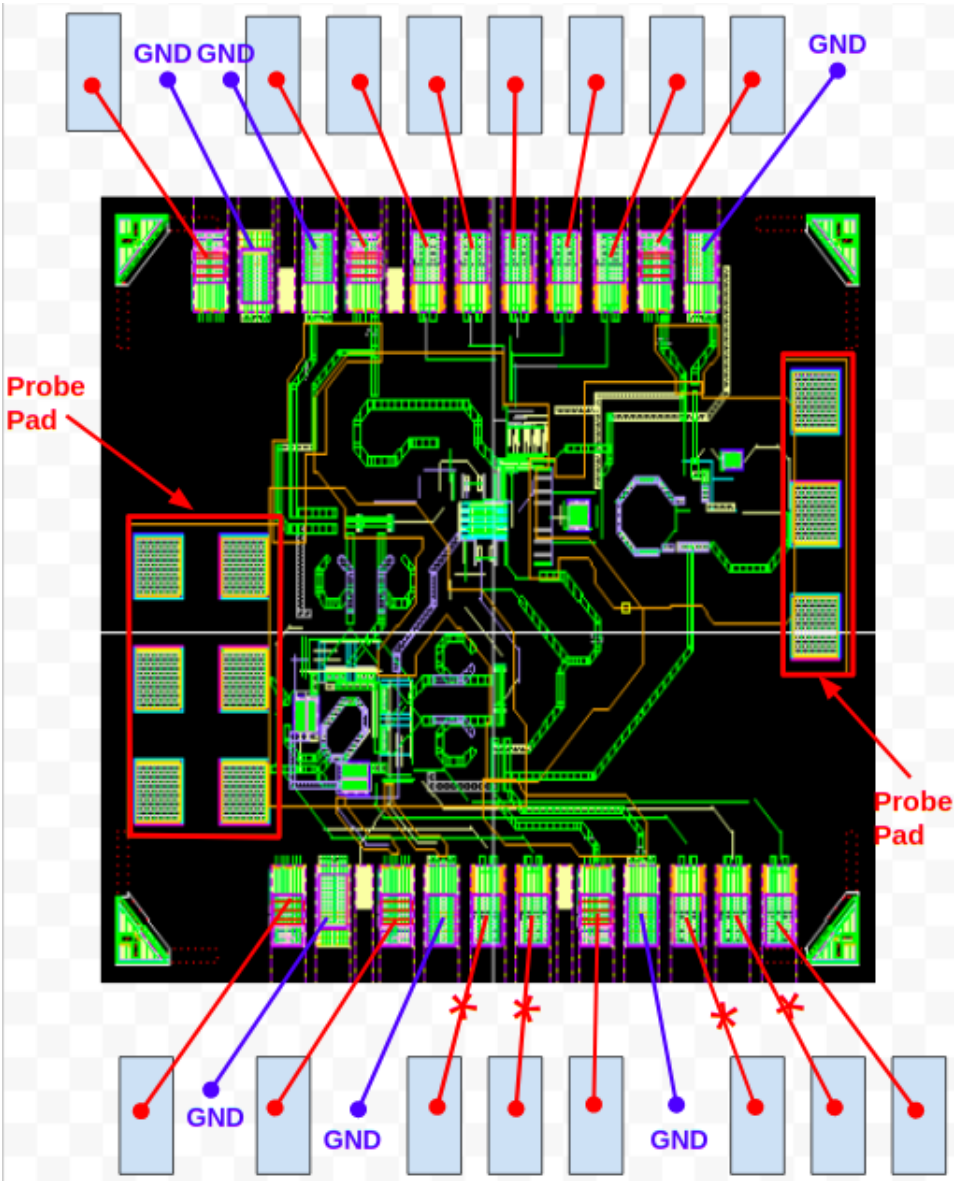

Figure 6.1: Bondpads and Probepads

As seen in the image, there are three sets of probe pads (on the left and right). One of the sets of probe pads on the left side are used for calibration. The probe pads on the right are for the input LO signal while the ones on the left are for the output RF signal.

There are 16 bondwires out of which 4 are for the baseband signals (marked with an *), 5 of them are for the digital input bits, 4 are input supply lines, 1 is for the reference current while the remaining 2 are for ESD.

6.2 Testing Board

The testing board needs to perform the following functions:

- LDOs have to be added for the supply lines with supply decoupling capacitors
- Digital switches need to be present to control the 5 input digital bits
- A potentiometer to vary the reference bias current
- Input matching resistors for the baseband signals

The layout of the board can be seen below:

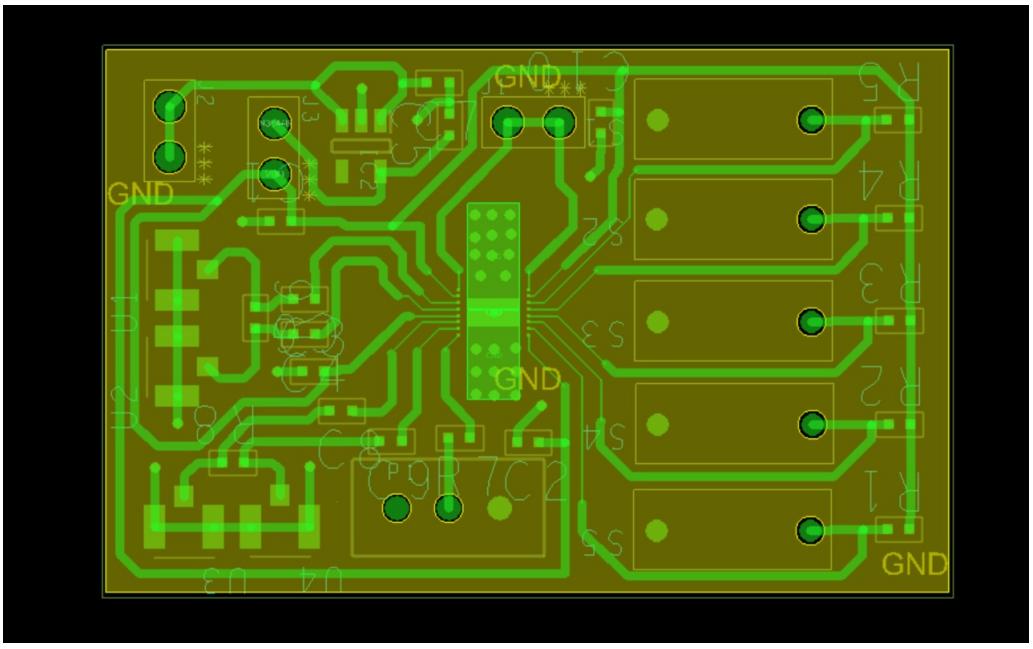

Figure 6.2: The testing board

CHAPTER 7

Results

The taped out IC was not tested and measured so this chapter will go over the results from simulations. The simulation of the complete circuit is very complicated because of the large number of blocks, the high frequency (that requires an increased number of parasitics to be simulated) and its non-linear nature due to the large amplitude signals required to be transmitted and fed to the mixer. Due to this, it is not possible to completely simulate the entire circuit.

The simulation itself consists of two parts. First, we must use EMX to extract parasitics from the layout. At 26GHz, there is increased coupling between nearby metal lines and this simulation is also very demanding. Ways to simplify this would be to reduce the mesh size or the frequency resolution over which the simulation is run. This would give us an approximate estimate of the parasitics in the layout but will not be completely accurate. The next part is to run the actual ADE simulation in Virtuoso to find the 1dB compression point. This simulation itself crashes when trying to run it with the complete layout that has had its parasitics extracted. As a result, we must run this simulation with just some blocks that are EMX extracted individually. This was done for the 3 major blocks - the up-conversion mixer, the phase-shifter and the polyphase filter. Once again, since we have not run this simulation with the complete EMX-extracted file, the results will not be accurate.

One thing to be kept in mind while doing this is that there are coupling effects between blocks that are being neglected while finding the 1dB compression point. To ensure that the circuit works even with the complete EMX-extracted file, the ADE simulation was run for a low input power and lesser harmonics of the input frequencies. This reduces the complexity of the simulation and can hence be run even with the complete EMX-extracted file. It was ensured the gain of the transmitter in this case is close enough to the gain we see when we increase the number of harmonics and run the simulation with 3 separate blocks instead of the complete layout.

The approximate simulations as explained above, will give us slightly better results

than the actual performance of the transmitter. From comparing the effect of such approximations on smaller blocks we can expect the actual transmitter to have a gain and 1dB compression point that is 0.3dB-0.5dB lesser than what is reported in this section. This is because using a smaller mesh size and a smaller frequency resolution will add increased parasitics while coupling between blocks will also cause increased losses. The reported numbers in the following section will however be with simulations run with the above approximations.

7.1 Specifications

There are several specifications to be accounted for while designing the transmitter. The primary design consideration is to maximise the 1dB compression point.

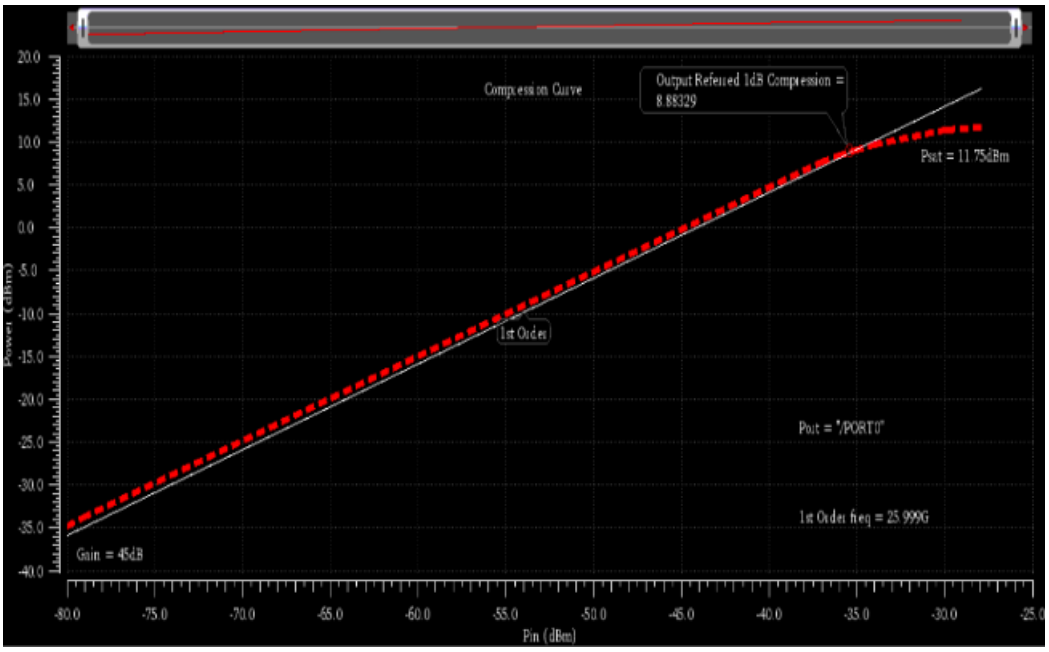

Figure 7.1: Output Referred 1dB Compression Point

The 1dB compression as seen above is 8.88dBm while the saturated output power is 11.75dBm.The gain of the transmitter can also seen to be 45dB.

While achieving this 1dB compression there are a few things that need to ensured. The first is that the drain-source and drain-bulk voltages of the switches do not exceed 1.2V. This is achieved easily once the bulk voltage of the mixer switches was set to a voltage about ground. The second is to make sure that the deviation in phase from the linear region to the compressed region of the output power curve is less than 4°.

The following plots show the variation in output reflection coefficient (S22) and gain of the circuit when the LO signal was varied from 20GHz to 30GHz.

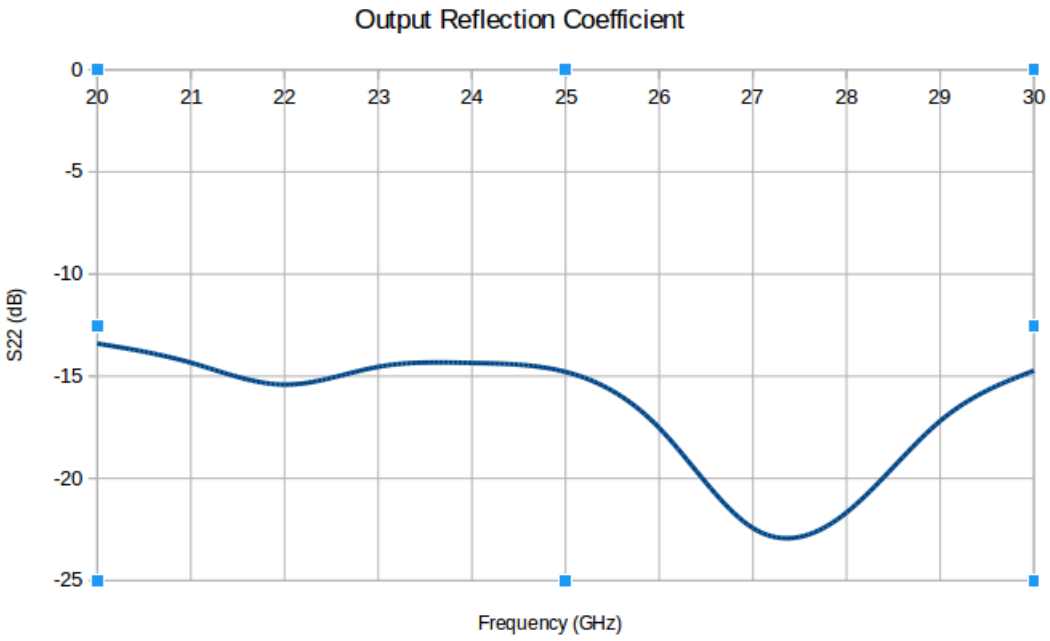

Figure 7.2: Output Reflection Coefficient as the LO frequency is varied

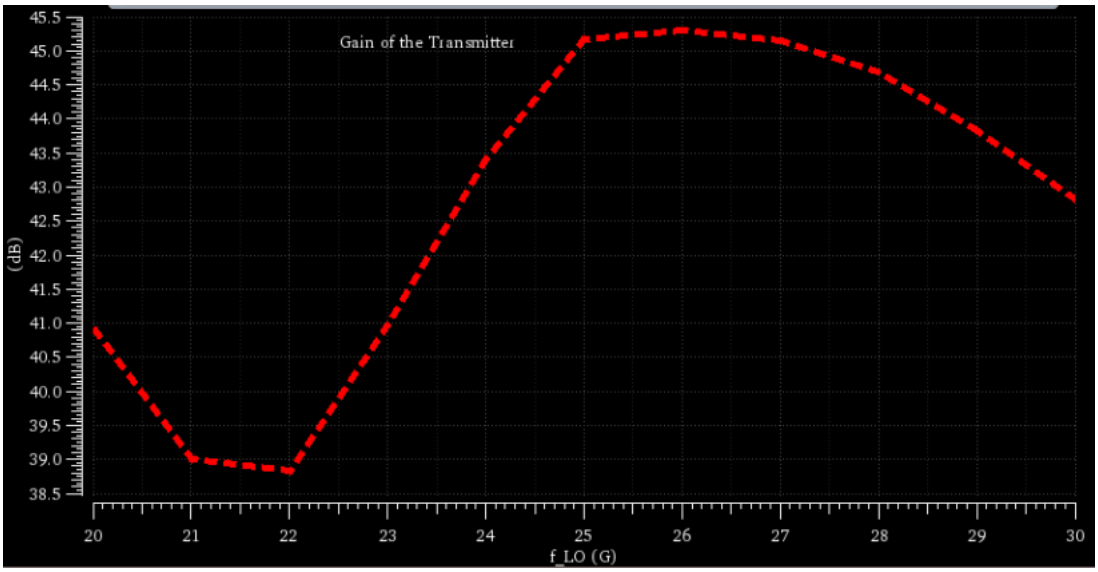

Figure 7.3: Gain of the Transmitter as the LO frequency is varied

The bandwidth of the circuit on the baseband side should be 200MHz. The gain and output reflection coefficient should not vary too much in this bandwidth.

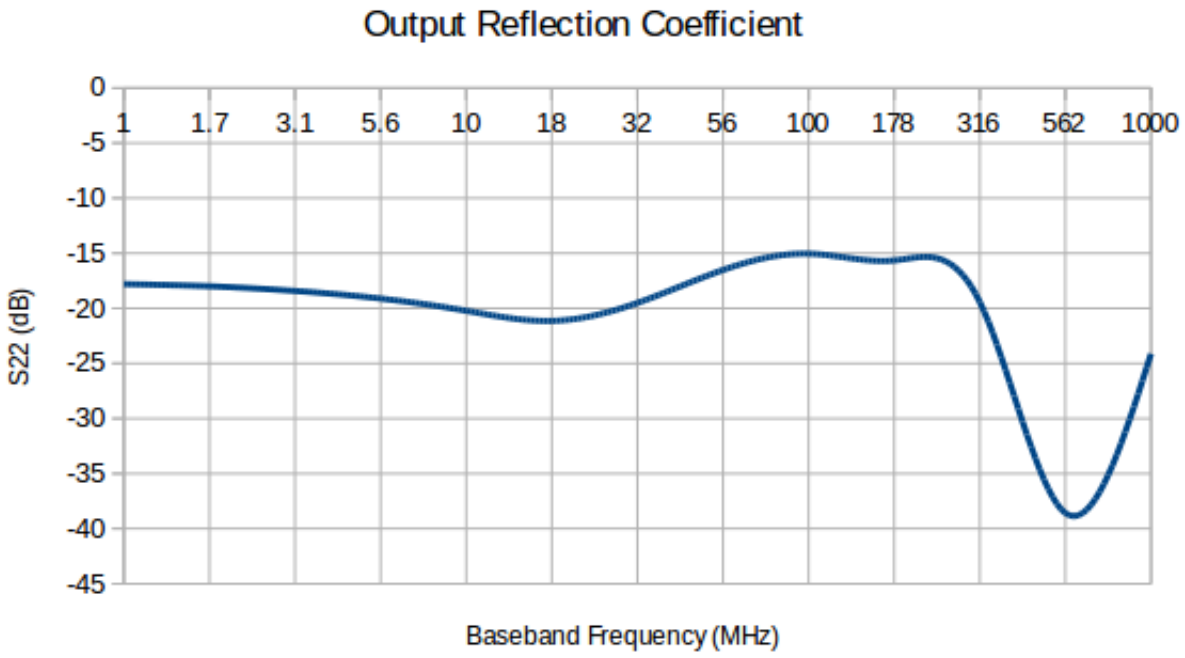

Figure 7.4: Output Reflection Coefficient as the baseband frequency is varied

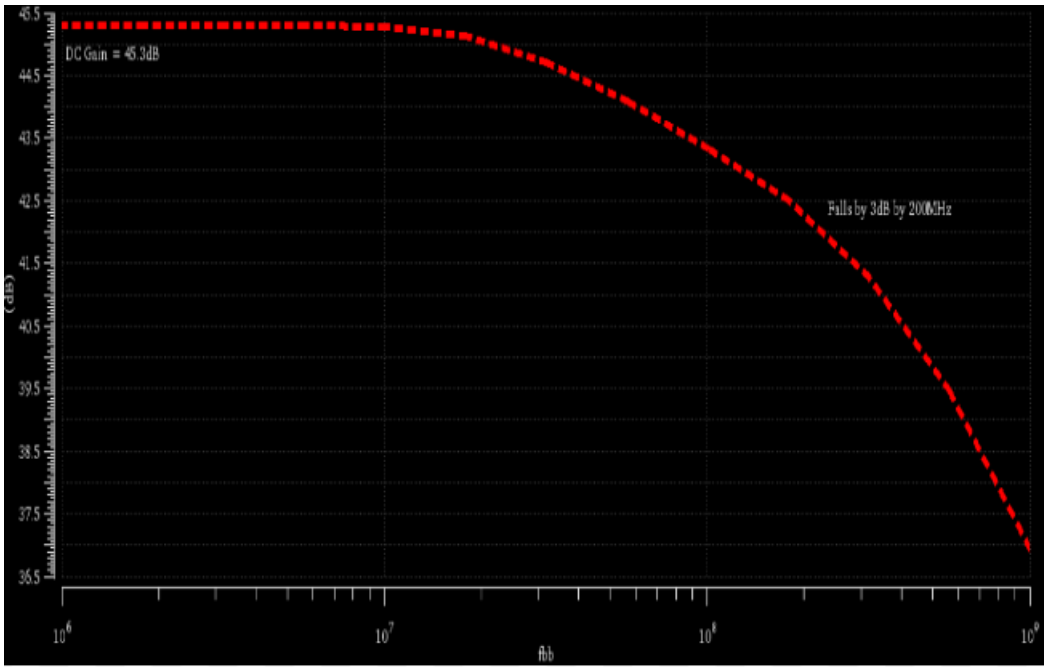

Figure 7.5: Gain of the Transmitter as the baseband frequency is varied

It can be seen that while the output reflection coefficient is less than 15dB within the band of interest, the gain falls by 3dB within this same range of frequencies. This is due to additional layout parasitics.

It was also important to ensure symmetry between all LO lines and between differ-

ential halves in the layout. Loss in symmetry causes other harmonics to be put out from the transmitter. For a carrier signal at the (LO-BB) frequency, the largest unwanted harmonics are at the LO frequency (caused by mismatch between the differential halves) and the (LO + BB)frequency (caused by mismatch between the I and Q halves). The final layout had the output power in the LO frequency to be 35dB less than the carrier while the (LO + BB) frequency was 22dB below the carrier.

The power supply used was 1.2V and the power consumption in the signal path was 174mW while it is 85mW in the LO path. The dimensions of the chip are 1.3mm by 1mm and hence, occupies a total area of 1.3mm^2.

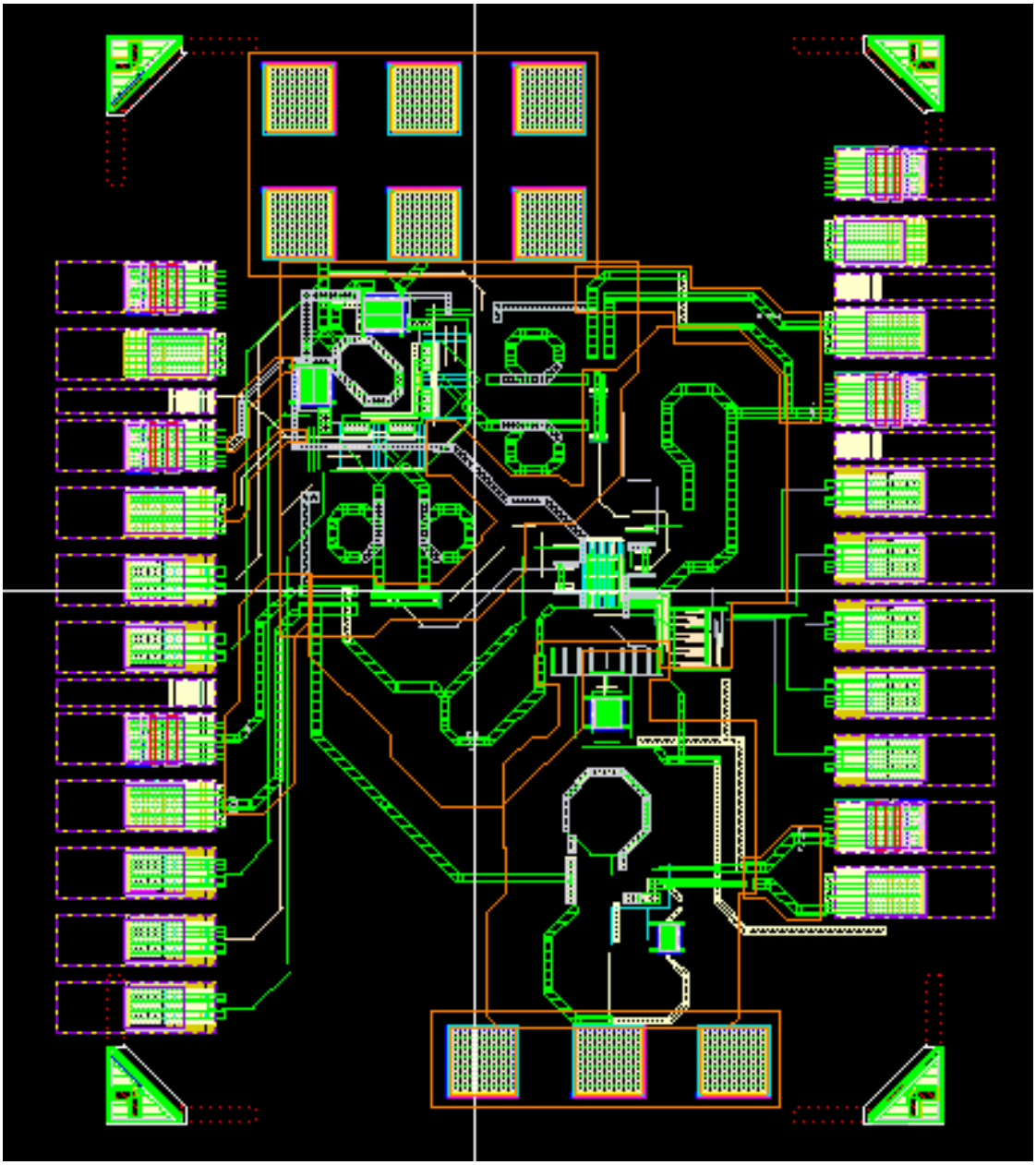

Figure 7.6: Complete Transmitter Layout

CHAPTER 8

Conclusion and Future work

A compact millimeter wave transmitter with beamforming capabilities was presented. Different architectures for the transmitter were considered and compared to optimize performance, area and power. A phase-shifting scheme that can be integrated with this architecture was proposed and its working was explained in detail. Layout at millimeter wave frequency has to be carefully done and hence, different possible ways to lay out the circuits were considered and depicted. A 26GHz transmitter implementing these ideas was designed and taped-out.

This work implements ideas to perform phase-shifting and achieve high transmit powers but there are a few things left to be optimised. The complicated LO circuitry works well at achieving its target but symmetry has to be maintained between the 4 LO lines. The layout of the different blocks and their relative positioning needs to be optimised to ensure this symmetry is maintained. This will reduce the amount of power that is put out into other frequencies. The LO chain itself can also be optimised by moving around or changing blocks to achieve the required output swing with lesser power consumption. Even if the power consumption cannot be reduced significantly, it can be possible to reduce the power consumption on the LO side and instead increase it in the mixer to improve the overall efficiency of the transmitter. Such trade-offs can be considered. This might work better because in the present design, the LO signal was almost rail-to-rail but this is not efficient from a power consumption point of view since the gain of the buffers reduce for larger signals. It is possible that it might be more optimum to use this power to improve the performance of the mixer instead.

The polyphase filter was designed to achieve the required phase shifts at 26GHz. We would however, like the transmitter to work for a larger range of LO frequencies and different architectures for creating quadrature LO signals needs to be considered for this. The polyphase filter itself is highly sensitive to variations in the R and C values and other architectures that avoid this dependency will overcome this issue too.

While the phase shifter design was explained mathematically, the number of switches

was too many and this adds unnecessary asymmetry to the layout. The switches were made very small as this worked better at schematic level but at layout level this makes the performance more sensitive to layout parasitics (since the device parasitics themselves are very small). This has not been accounted for. Lastly, as explained in the chapter on beamforming, we would ideally like to add time delays to the signal while performing beamforming. The phase shifts that are done in this work is only approximately equivalent to a time shift for narrow band signals. Since the 5G signals actually have a large bandwidth, we would need to consider alternate circuits that can add actual time delays to the signals instead of phase shifts for more accurate beamforming.

APPENDIX A

Wideband Transmitter

A small project was also undertaken to add some design changes to a previous designed wideband transmitter operating from 30MHz to 12GHz. The LO signal that is fed to the transmitter is passed through a frequency divider before being fed to the mixer. The earlier frequency divider design was actually two different dividers that operate for low frequencies and high frequencies respectively. The high frequency part was a current-mode latch (CML) while the low frequency part was made of transmission gates. It also had 3 buffers both before and after the divider to amplify the LO signal. While this ensures that the LO chain is now able to achieve the required output swing for all frequencies, the actual small signal gain of the chain is extremely high at low frequencies and can cause stability issues through any parasitic feedback path that may exist in the layout. The gain at higher frequencies are closer to the actual gain that needs to be achieved while at lower frequencies, the gain is unnecessarily high but the output swing is limited due to supply voltage limits.

The two issues to be countered are hence, to create one divider circuitry that works for the entire frequency range and to adjust the frequency response of the LO chain so that the gain is roughly flat for the frequencies of interest.

A.1 Extending the frequencies of operation of the Divider

Without getting into the details of the operation of the divider, it was found that the only limitation due to which the high-frequency part of the divider wasn't working for lower frequencies was because the coupling networks that remove the DC bias between different stages of the chain were not designed to operate at frequencies close to DC. Fixing this issue would require increasing the values of R and C in the coupling network causing the area of the divider to increase. However, it was found that if this increase

was completely done in the resistor and not the capacitor then the increase in area is not too significant. This is because the resistor can be made more compact and dense when laid out compared to the capacitor.

This was able to extend the operation of the divider down to an input frequency of 60MHz without changing anything else in the divider.

A.2 Fixing the gain of the LO chain

The reason that three buffers were cascaded was to make up for the drop in gain at higher frequencies. Cascading buffers will increase the DC gain of the chain itself so that even after the drop at higher frequencies, the chain has enough gain to deliver the required LO swing to the mixer. At lower frequencies, the supply limit will ensure that the output swing is not too large.

To fix this issue of large gain at low frequencies, the number of buffers was reduced and the drop in gain at higher frequencies was fixed by adding inductors at the output. Thus, the final chain has only one buffer before and after the CML and has a series inductor at the output that resonates out the parasitic capacitances seen by the buffer and reduces the drop at higher frequencies. This ensures that the gain at all frequencies is not so large as to cause stability issues due to parasitic paths that may be present in the layout. The use of a series inductor was also found to be advantageous since the drop in gain was not so much as to warrant the use of a shunt inductor and using a series inductor resulted in a smaller inductance and thus, lesser increase in area too.

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