Narrow-Band IoT Receiver and Ultra Wide-Band Transmitter

A THESIS

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled **Narrow-Band IoT Receiver and Ultra Wide-Band Transmitter**, submitted by **Nishant Sanjay Patil**, to the Indian Institute of Technology, Madras, for the award of the degree of **DUAL DEGREE BACHELOR OF TECHNOLOGY & MASTER OF TECHNOLOGY**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: NB-IoT; LTE; 3GPP; Low power receiver; inductorless receiver; low-noise amplifiers; Mixer; Ultra Wide-Band transmitter; Power mixer; Replica biasing; CMOS 65nm.

With 5G communication shifting to a higher frequency range, 4G LTE bands can be used for other applications. One such application is Narrow-Band IoT communication. In India, LTE bands 3 & 5 will be used for NB-IoT communication with a bandwidth of just 200 kHz. Such a low bandwidth allows circuit designers to design high range, low power, and low-cost transceivers.

This thesis presents an inductorless low power-consuming receiver satisfying all 3GPP design specifications. Architectural and circuit level optimizations are done to reduce power consumption. System & circuit level analysis, design procedure, and results are presented in this thesis. The measured results are as expected and showed the receiver's working for all configurations.

Wide-band ICs are helpful in many applications like communication, defense, and sensor. The same IC can be used for many applications with an appropriate off-chip matching network. The second part of the thesis discusses the design and fabrication of an Ultra Wide-band transmitter operating from 30 MHz to 12 GHz. This thesis covers architecture & circuit analysis, layout, packaging & PCB considerations, and simulated results. Measurements are going on while writing this thesis.

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CHAPTER 1

Introduction

The Internet of Things (IoT) has evolved tremendously since its first application in the early 1980s by students of Carnegie Mellon University. IoT has found new uses in low data and low power applications. A few examples can be seen in smart cities, remote health monitoring devices, smart agriculture, etc [1]. A few key features of these applications include:

· Low data rate

· Low bandwidth

· Low power consumption

· Low cost

The Narrow Band Internet of Things (NB-IoT) has been included in the 3rd Generation Partnership Project (3GPP) along with 5G. These NB-IoT guidelines are used to design receivers for the NB-IoT networks in India.

1.1 Receiver Architectures

There are mainly two types of receiver architectures, direct conversion receivers and intermediate frequency (IF) conversion receivers. Direct conversion receivers, also known as homodyne receivers convert RF signals directly to baseband. On the other hand, in the case of IF conversion receivers, also known as heterodyne receivers, RF signals are converted to some intermediate frequency and then converted to baseband [2]. The direct conversion method is favourable due to its low complexity at low RF frequencies. Since NB-IoT transceiver works at a maximum frequency of 2 GHz, the receiver is designed in the direct conversion architecture. Fig. 1.1 shows the important blocks in an RF direct conversion receiver.

In the literature, we find some variations of direct converter receivers like the mixer first receiver, N-Path filter first receiver [3], [4], [5], [6]. These receivers have specific

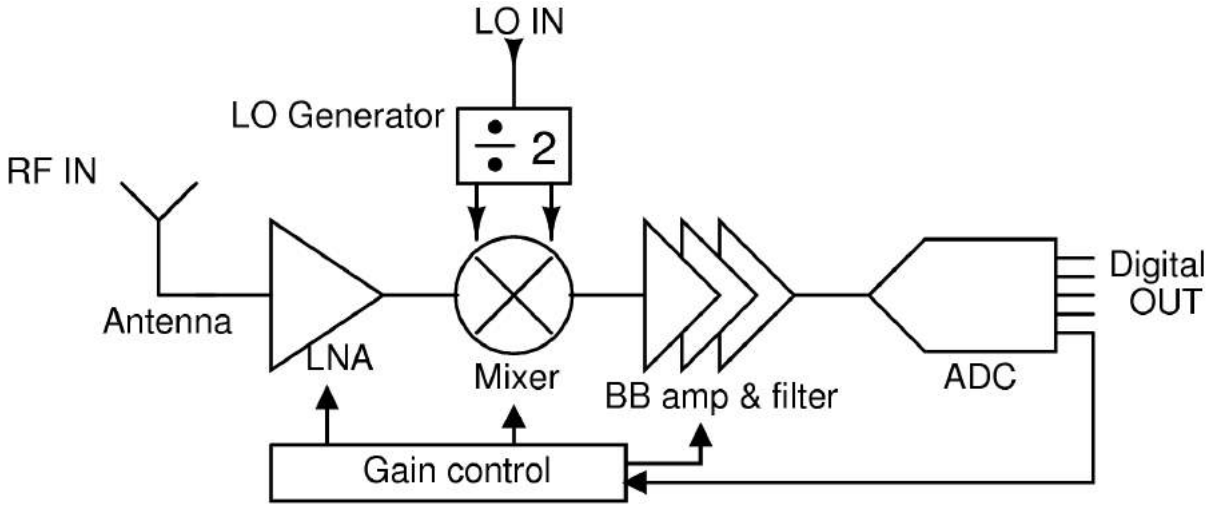

Figure 1.1: Blocks of conventional direct converter receiver.

applications and usually focus on improving one design parameter by a large extent; for example, out of spectrum interface cancellation in N-Path filters. Since the 3GPP specifications for NB-IoT receiver do not require such special performance metrics, the receiver designed in this work uses a conventional receiver architecture as shown in Fig. 1.1.

1.2 Receiver Development Chronology

The organization of this thesis proceeds in the following way. This work starts with understanding the 3rd generation partnership program (3GPP) technical document. We derive design specifications for the receiver and define our scope of work. Once the system level specifications are finalized, we design each block and optimise it. This is followed by optimising the whole receiver chain. We check circuit performance for process corners and temperature variations. If the circuit gives the required performance for all cases, we start layout design. If not, we modify/redesign the circuit. The layout file is sent to Taiwan Semiconductors (TSMC) for fabrication. Upon receiving fabricated dies, we package them in QFN48 packaging. A PCB test bench is designed and fabricated meanwhile. NB-IoT receiver IC is soldered on the PCB and measurements are taken for gain and input matching. The measurements showed promising results.

CHAPTER 2

Receiver Specifications

In the previous chapter, we saw various possible receiver architectures and decided to use the common LNA first direct conversion receiver architecture. Designing the whole receiver chain and optimizing the system is a very time intensive process as each block added increases design time exponentially. Considering the timeline for the dual degree project, we define the scope of work as shown in Fig. 2.1.

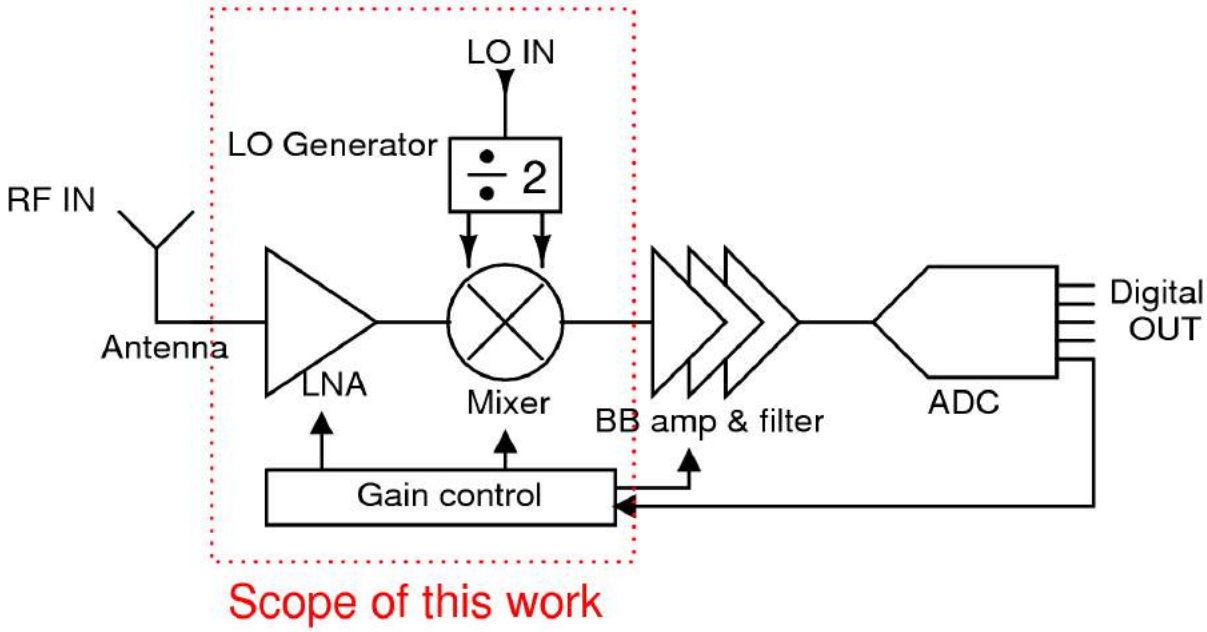

Figure 2.1: Scope of this work.

This work covers the LNA, LO divider and buffers, mixer and gain control blocks. The receiver is inductorless as inductors occupy large die area and hence increase the cost. Overall, the receiver is optimised for power and area.

2.1 Understanding 3GPP Specifications

This work is based on ETSI TS 136 101 V15.9.0 (2020-02) technical specification document by the 3GPP 5G initiative [7]. A few key NB-IoT specifications mentioned in the technical specification document are-

- Indian NB-IoT network will be using LTE band 3 & 5.
- Downlink frequencies are 869-894 MHz and 1805-1880 MHz.
- Channel bandwidth is 200 KHz.
- Two carriers are 200 kHz apart from each other.
- Reference sensitivity level: -108.2 dBm.
- Maximum power received: -25 dBm.
- Modulation- Quadrature Phase Shift Keying

Along with the above details, there are some specifications about baseband filtering and input LO signal quality. Upon comprehensive study of the document, we derived system level specifications for the NB-IoT receiver.

2.1.1 Noise Figure

Noise figure (NF) is the most important specification of the receiver. It is derived from the lowest input RF signal power and signal bandwidth. Often times, designs consume most of the power in order to keep the noise figure low. Noise figure in dB can be calculated using the following formula 2.1-

$$Sensitivity = Thermal\ Noise\ Floor + NF + 10log(BW) + SNR \tag{2.1}$$

The sensitivity level is **-108.2 dBm**. For room temperature, the 50 ω thermal noise floor is **-174 dBm/Hz**. Signal bandwidth is **200 KHz**. For QPSK modulation, required SNR is **-1 dB**. Using these values, required noise figure for receiver is **13.8 dB**.

Considering package loss (1 dB) , PCB trace loss (1 dB), Balun loss (1 dB), margin for baseband filter and amplifier noise (1.8 dB) and margin for errors (3 dB), we decided to design the receiver for **6 dB**.

2.1.2 Gain Range

As we are not designing the baseband filter and amplifier in this work, we will have some relaxation in designing gain. Assuming ADC input requires a signal amplitude of 0 dBm, the receiver chain (this receiver plus baseband amplifier) should give a gain from **25 dB to 108.2 dB**. Usually, we can get a very high gain from the baseband amplifier as the baseband frequency is low. Hence the minimum gain from the Rx should be more than 25 dB and the maximum gain should be less than 108.2 dB.

2.1.3 Linearity

The receiver should be able to process maximum input power. Since we amplify the signal down the chain, linearity requirements for later blocks become tight as they receive amplified signals. This is analysed using the following equation2.2 [2]-

$$\frac{1}{IIP3_{RX}} = \frac{1}{IIP3_{LNA}} + \frac{G_{LNA}}{IIP3_{MIX}} + \frac{G_{LNA}G_{MIX}}{IIP3_{BB}} \tag{2.2}$$

Where, $IIP3_{RX}$ is IIP3 of the receiver, $IIP3_{LNA}$ is IIP3 of the LNA, $IIP3_{MIX}$ is IIP3 of the mixer, and $IIP3_{BB}$ is IIP3 of the baseband block. G_{LNA} is gain of the LNA and G_{MIX} is the gain of the mixer.

Clearly for high gain, that is for high values of G_{LNA} G_{MIX}, linearity constraints on the baseband block will be worst and sometimes impossible to design in the given technology. Hence the minimum gain from the LNA + Mixer block should be designed carefully and the designed receiver should have good IIP3.

1 dB compression point and IIP3 calculations

Derivations for 1 dB compression point and IIP3 for the receiver are as follows-

=> 1-dB compression point = maximum input power + peak-to-average ratio (PAR)

=> peak-to-average ratio (PAR) = 2*ln(N) where N is number of subcarriers.

From 3GPP specifications, N = 12, Maximum input power = -25 dB

=> **1 dB compression point= -20dB**.

=> IIP3 = 1-dB compression point + 10 dB + envelope variation due to BB pulse shaping.

=> envelope variation due to BB pulse shaping - 2 dB

=> **IIP3 = - 8 dBm.**

2.2 Design Specifications for This Work

From the above analysis, we have found the design specifications for the receiver. With reasonable assumptions about noise, gain and the linearity of the baseband block, we can derive specifications for this work as-

- **Noise Figure $<$ 6 dB**
- **Gain range of 25 to 108.2 dB**
- **1 dB compression point $>$ -20 dBm**
- **IIP3 $>$ -8 dBm**
- **S11 $<$ -10 dB (standard requirement)**

In this work, we tried to meet above specifications while minimizing area and power consumption.

In next chapter, we will discuss topology and circuit design to meet the above specifications.

CHAPTER 3

Design and Circuit Analysis

After understanding 3GPP specifications for the RF front end, along with reasonable assumptions, we derived design specifications for the LNA and Mixer block. This work covers the design of the Low noise amplifier (LNA), direct conversion mixer, frequency divider and LO buffers. Fig 3.1 shows a block level representation of this work. We will start with the LNA. Subsequently, we will discuss the mixer, frequency divider, LO buffers and some other features.

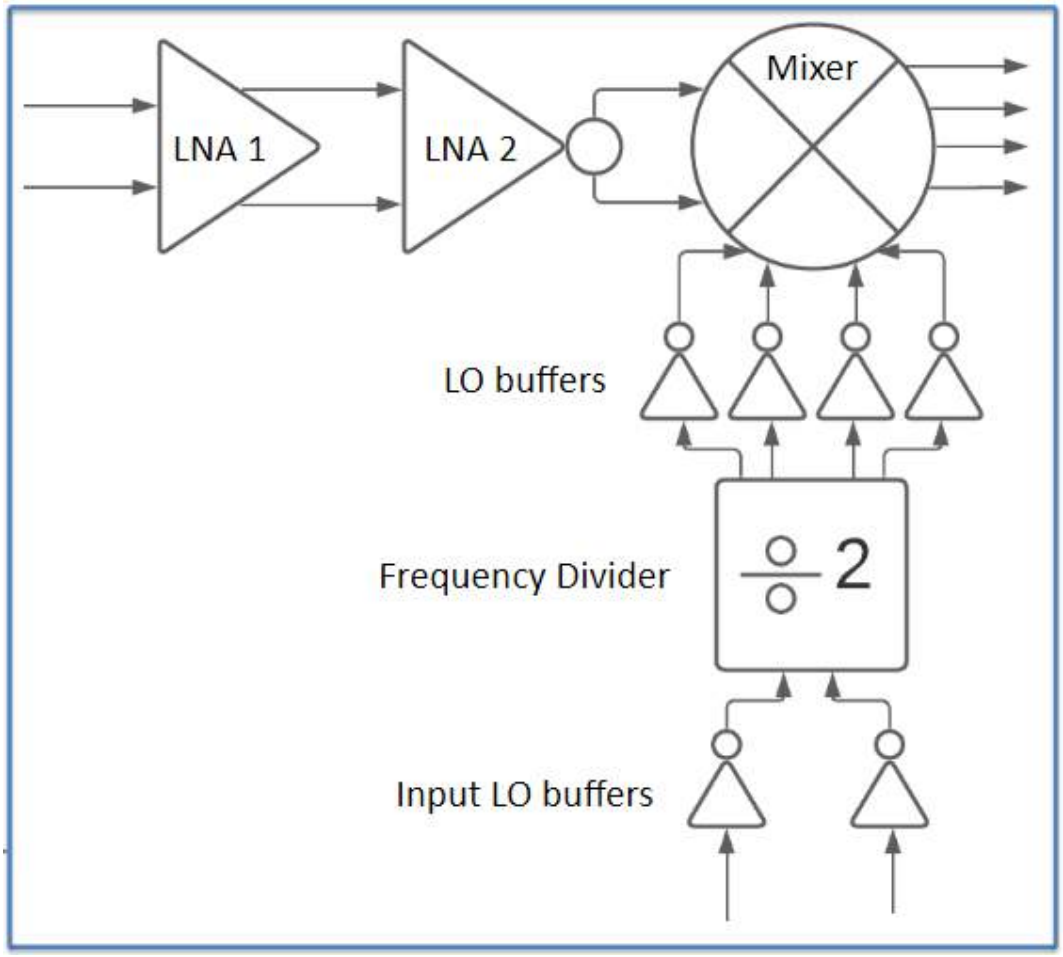

Figure 3.1: NB-IoT receiver block level representation

3.1 Low Noise Amplifier Design

The Low Noise Amplifier (LNA) is the most important block in the receiver chain as its noise figure directly decides the sensitivity of the whole system. Also, LNA consumes the most power in order to reduce NF and get more gain. After studying various inductorless LNA topologies, a comparison chart is shown as follows 3.1- Note- The circuits for above topologies are in the appendix.

LNA topology	Gain	Noise factor	Advantages	Disadvantages
Common source with resistive feedback	$\frac{Rf}{2Rs}$	1 + $\frac{4Rs}{Rf}$ + γ + $\gamma \mathrm{gm}_2 Rs$	Wide Band, No limit on gain due to headroom	High noise figure, Gm1 of 20 mho
Common source with resistive feedback with improved noise figure	$\frac{Rf}{2Rs}$	1 + $\frac{4Rs}{Rf}$ + γ	Gm1 of 10 mho No limit on gain due to headroom	High noise figure, Current source is needed
Common gate with cascode and inductive degeneration	$\frac{R1}{2Rs}$	1 + γ + $\gamma gm_2 Rs + \frac{4Rs}{R1}$	high gain, low power consumption, low noise figure	Inductor is needed, more area, not Wide Band, sensitive to bondwire inductance
Cascode common source stage with inductive degeneration	$\frac{R1}{2L1}$	1 + $\gamma gm_1 Rs(\frac{\omega o}{\omega t})^2$	high gain, low power consumption, low noise figure	Two inductors are needed, more area, not Wide Band, sensitive to bondwire inductance
CG-CS noise-canceling LNA	$\frac{R1}{Rs}$	1 + $\frac{\gamma}{N}$	Ulta low Noise figure possible	High power consumption for input matching
This work- Resistively degenerate capacitor cross-coupled common source LNA	$\frac{R1}{Rs}$	1 + $\frac{\gamma}{2}$	Low power consumption, No inductors, Wide Band, Immune to bondwire inductance variation, Low power consumption mode possible	High Noise figure, Gain limited by headroom, More area due to large capacitor but low compared to inductor

Table 3.1: LNA Topology Comparison

Our LNA is a combination of various topologies, We used a resistive degenerated LNA in order to save inductor's area. We gave input at the source so that we can have

wide band input matching ($\frac{1}{2gm}$ = Rin). We removed cascode NMOS to get higher headroom and hence high gain, low noise figure. We introduced cross couple capacitors in order to reduce gm requirement and noise contribution. Details about the LNA are discussed in the following subsection. The circuit for our LNA is shown in fig 3.2.

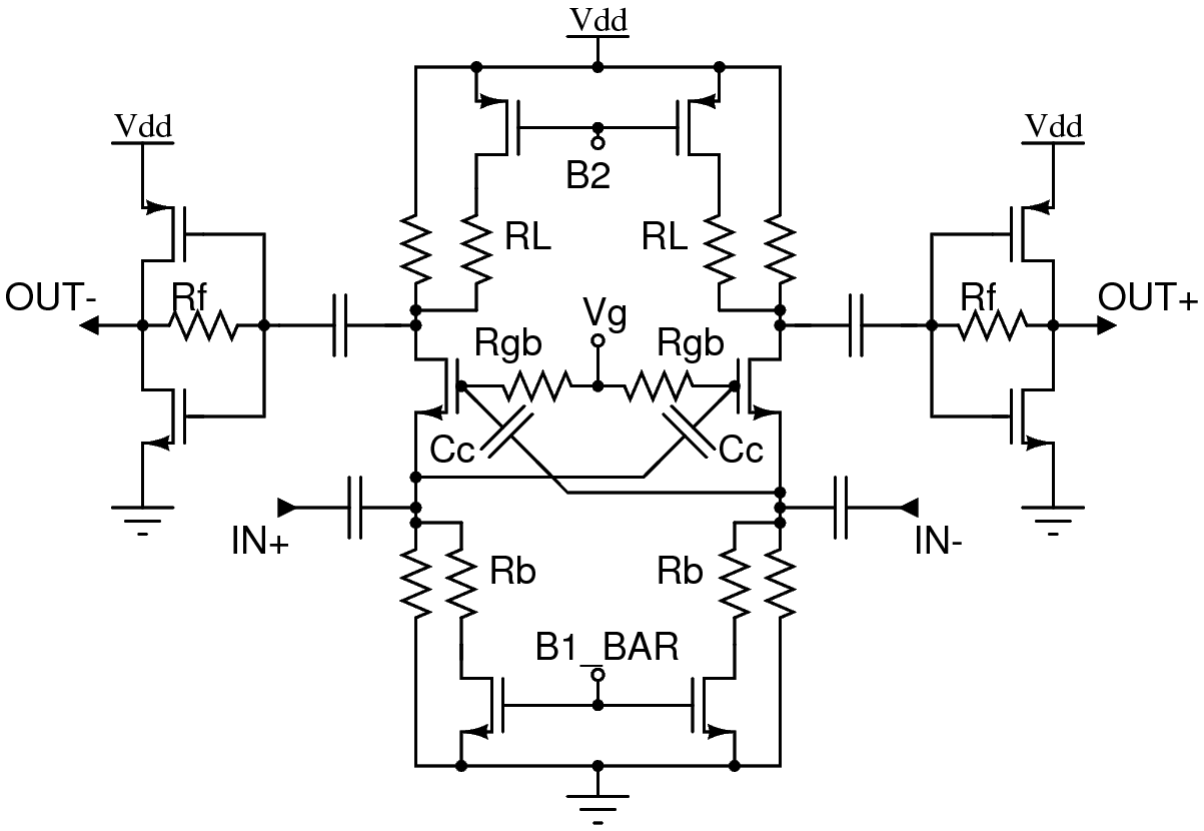

Figure 3.2: Two stage LNA

3.1.1 Our LNA Design

The two stage LNA is used to give maximum gain of 32 dB while maintaining noise figure of 2.7 dB. The first stage is a Resistively degenerate capacitor cross-coupled common source amplifier and the second stage is a self biased CMOS inverter, refer to 3.2. From circuit analysis [8],[9], Input matching requirements are as follows-

- $G_{meff} = (1 + A)G_m$
- Where, A = $\frac{C_C}{C_C+C_{gs}}$

Now, for C_C » C_gs, A $\approx$ 1, Hence $G_{meff} \approx 2 * G_m$. Hence G_m of only 10 mho is needed unlike other common source topologies where gm of 20 mho is needed. This saves bias current and reduced device size.

For Gain calculations,

- Gain = $\frac{RL}{Rs}$, where Rs = 50 ohms

Now, RL value is limited by two things-

- VDD headroom - IR drop across RL increases as RL increases, for the same bias current.
- RC pole at the output - RL and parasitic capacitors will create a pole at the output of the LNA. We have to make sure that the pole is far away from 2 GHz.

As RL reduces, gain reduces and noise contribution from RL increases. But for Rl = 500, that is 20 dB V/V gain, we can assume that the gain is much larger and hence noise contribution from the resistor is negligible.

Hence the gain from first stage is 20 dB V/V and from the inverter stage is 12 dB V/V.

Noise contribution from the MOSFET is given by 1 + $\frac{\gamma}{2}$. The factor of 2 is arises because the value of gm is $\frac{1}{2Rs}$. The actual simulations show that the noise contributions from Rb and RL were significant.

After understanding all trade-offs in the circuit, I implemented the following new techniques-

- **Removing cascode NMOS-** Existing designs use a cascode NMOS in order to improve isolation between the input and the output of the LNA. But this cascode eats headroom and hence the overall gain reduces. S12 can be a good measure for the same. Finding S12 is not a straightforward procedure as the output of the LNA is not shorted to 50 ohms and hence we can't use S parameter analysis. I worked on the simulation setup and developed a procedure to measure S12 (Refer Appendix 2). These simulations allowed me to chose a large enough NMOS without a cascode. Hence, in my design, I cautiously chose the size of the NMOS to get low parasitic caps but at the same time get 10 mmho of gm. These small parasitic caps help in improving S11 (input matching) and S12 (output to input isolation).

- **Using regenerative resistance for input matching**

$$R_{in} = \frac{1 + \frac{RL}{R_{ds}}}{gm(A+1) + \frac{1}{R_{ds}} + \frac{1}{Rb} + \frac{RL}{R_{ds}Rb}} \tag{3.1}$$

  The requirment for a Gm of 10 mmho can be relaxed if we can reduce Rb, the regenerative resistance. With this improvement, we can reduce gm below 10 mmho and reduce power consumption. This mode will be used when the input signal is above sensitivity level and hence the increase in the NF will not be damaging. This way we can reduce LNA power consumption without compromising on S11.

- **Introducing LNA 2 before Mixer** Most of the LNA topologies gives a maximum of 20-25 dB V/V gain. 20 dB, for example, will reduce noise from the mixer by 10 times only, hence we have to pay attention to Mixer noise figure while designing a mixer. Reducing mixer noise requires a lot of current. Hence we introduced another LNA after LNA 1. The requirements for LNA 2 were-
  - Relaxation of the need for 50 ohms input matching
  - Low input capacitance
  - Moderate gain
  - High linearity
  - Low power consumption

  A simple CMOS inverter with a resistor for biasing was the solution. Thus we introduced LNA 2 preceding the mixer. This LNA gives a gain of 12 dB.

3.2 Direct Conversion Mixer Design

For low frequency RF circuits, direct conversion mixer implementation is easy and straightforward. We can implement mixing action by using active circuits or passive circuits. A comparison between active mixers and passive mixers is given in table [2] 3.2

Mixer type	Advantages	Disadvantages
Active Gilbert cell mixer	• Voltage gain is possible. • LO signal of 50% duty cycle is needed. • Input impedance is capacitive hence no constraints on mixer output.	Power consuming
Passive mixer	No power consumption	• No or very limited gain. • LO signal of 25% duty cycle is needed, which is difficult to generate. • Input impedance depends on the loading of the mixer. This imposes constraints on the mixer output due to impedance translation.

Table 3.2: Mixer Comparison

Passive mixers look like a promising option for low power consuming circuits but their requirements of a 25% duty cycle LO signal and impedance translation makes them difficult to implement. Besides this, since we have a high gain (around 32-33 dB V/V) from the LNA, we can make the mixer very noisy and reduce power consumption.

3.2.1 Our Mixer Design

We implemented a Gilbert cell active mixer with both passive and active load. A gain control bit is used to switch between these loads. Refer 3.3

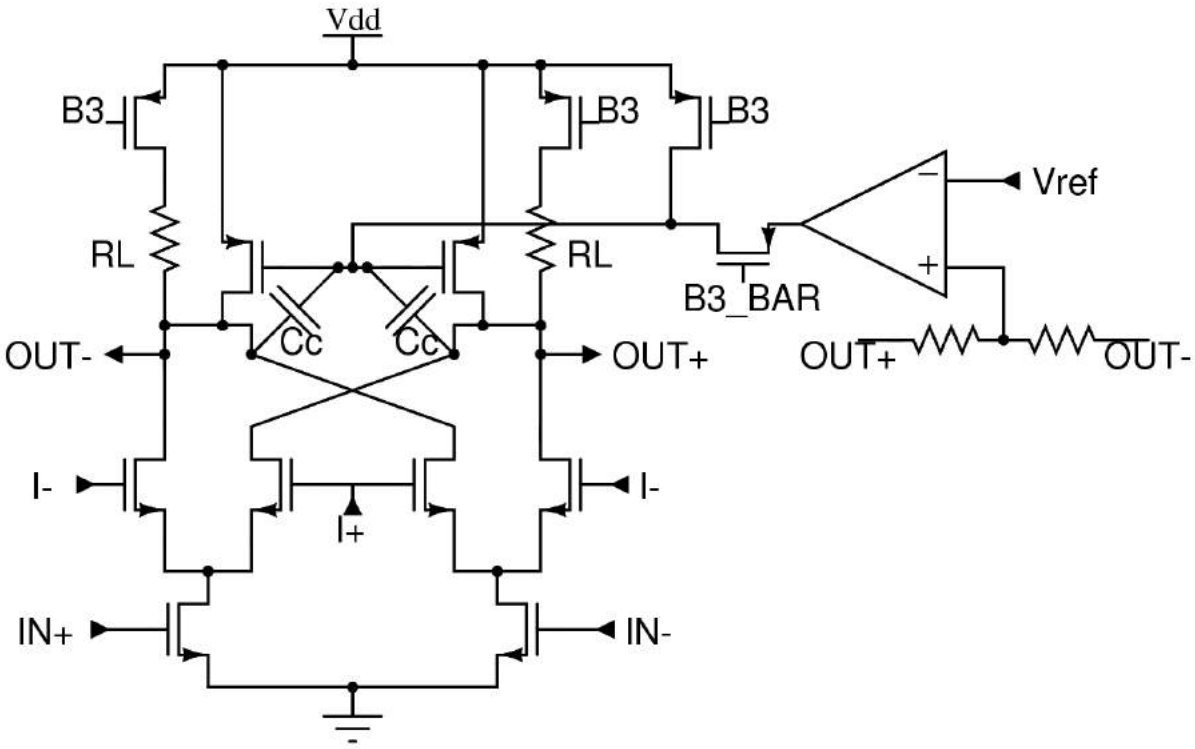

Figure 3.3: Gilbert cell active mixer circuit

Mixer operation modes-

- **Passive load mode, B3 = 0** for B3 = 0, the mixer is operating as a conventional Gilbert cell mixer with passive resistive load. In this configuration, RL = 2K ohms and the mixer shows great linearity. This mode will be used for high power input signals. For B3 = 0, the Opamp is disconnected.
- **Active load mode, B3 = VDD** for B3 = VDD, the mixer is operating with a PMOS active load. The gate voltage of the PMOS is set by a common mode negative feedback loop. Cc is used to Miller compensate the feedback loop. The phase margin of the loop is set to 60 $\deg and \omega$ugb is around 2.2 MHz, which is far higher than the baseband data rate. The $f$active load generated by PMOS is around 48K ohms.

We also loaded the mixer with a large cap in order to create the first baseband pole at 400 kHz. This pole location was calculated from the 3GPP specification document.

3.3 Frequency Divider and LO Buffer Design

An IQ downconverter mixer needs 4 LO phases each separated by 90 degrees. We can externally supply all 4 phases through a signal generator but the mismatch between equipment, RF cables, PCB traces, and bondwires will be too large and we will not get exactly 90 deg phased signals. This mismatch directly affects the performance of the mixer. Hence, we decided to use an on-chip frequency divider to generate 4 phases.

A transmission gate-based D flip flop frequency divider is designed and implemented. CMOS inverter based LO buffers are used as a post and pre-driver for this divider. LO divider and buffers are optimized for power consumption.

3.4 Gain and Band Control

Gain control is essential in wireless communication systems as the receiving signal amplitude varies by a large amount. In the case of the NB-IoT receiver, the input signal range is from -25 dBm to -108.2 dBm. The highest power input signal is almost 200 Million times stronger than the lowest power signal. In order to provide good performance over the large range of input signals, we need a gain control mechanism.

The receiver has 3 bits for gain control which changes gain linearly from 23 dB to 55 dB. We have included one bit for band control as the receiver will be operating in LTE band 3 (around 1.9 GHz) and LTE band 5 (around 0.9GHz). The receiver operates in two modes: A low power and high power mode.

Implementation of Gain control-

The main motivation for gain control is to reduce power consumption substantially when the received signal is not at the Reference sensitivity level i.e minimum power signal. Hence, we have introduced two control bits for the LNA as it consumes more power than the Mixer. One control bit in the mixer is very useful for meeting the linearity criterion for the maximum power input range as the linearity of the systems depends largely on the preceding blocks.

- **B1-** Gain control bit in LNA. This will change the load resistance of the LNA and hence the gain. The current consumption will reduce by a small amount.

- **B2-** Gain control bit in LNA. This will reduce Rb of the LNA which allows us to reduce gm and hence the bias current. As the bias current is reduced, gain will reduce but the power consumption will reduce significantly. Since Rb is now contributing toward the input impedance of the LNA, S11 remains in an acceptable range.
- **B3-** Gain control bit in Mixer. This will switch mixer load between active and passive loads.

  Active load- If RL of 48K ohms is generated through a PMOS load, linearity is bad. **Passive load-** If RL of 2K ohms is generated through a passive poly layer resistor, linearity is excellent.

3.5 Layout

Once the circuit gives the required performance, we design the layout. The final die picture is as shown in fig 3.4

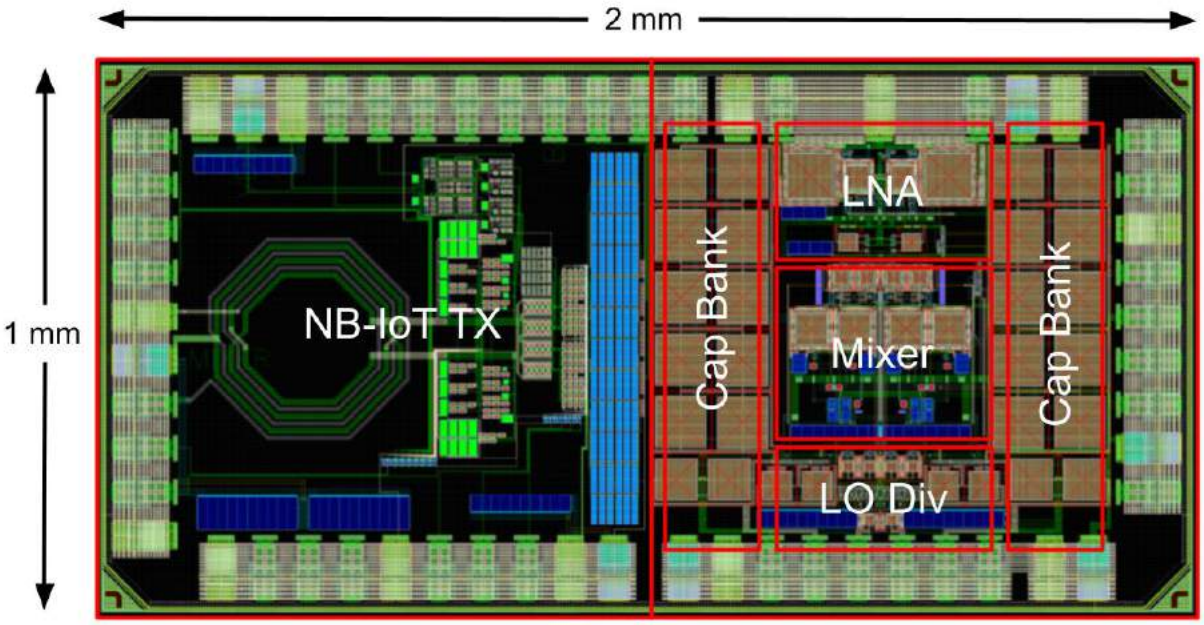

Figure 3.4: NB-IoT Transceiver die picture

Receiver takes the right half area of 2mm X 1mm transceiver. Input RF signal pads are located on the top while output baseband signal pads are on the bottom. A few key details about the layout are as follows-

- **Symmetry in I and Q path-** The mixer is designed such that I and Q paths are symmetric and have minimum phase and gain difference.
- **LO and RF isolation-** LO signals are usually peak to peak signals and RF signals have very low power. If we place them near other, the LO signal will corrupt the

RF signal due to capacitive coupling. In order to avoid this, LO signals are fed from the bottom pads while RF signals are provided from the top (refer 3.4). This ensures minimum coupling between RF and LO signals.

- **Minimizing parasitic capacitance-** We use metals to make electric connections. These metals offer parasitic capacitance to ground and a series resistance. The width and type of these metal connectors were chosen after considering the following factors-
  - Parasitic capacitors lower the bandwidth of the signal and hence the gain at high frequency. Higher the width of the metal lines, the higher is the capacitance. Hence low widths are preferred.
  - Parasitic resistors cause IR drop issues. Higher the width, lower the resistance. Since our circuit draws very less current, IR drop is not a concern. Hence we can have low widths.
  - Current carrying capacity of the metal is directly proportional to the width of metal line. However, since the current requirements are low, low-width metal connections were possible.

  Metal width and type was decided based on the above mentioned factors. Even with low width metals, LO parasitic capacitances were degrading the performance. Thus, the LO buffers are modified such that they can support this extra parasitic capacitance.

Once the RCCC extracted netlist results satisfied design requirements, Metal filling was done to take care of DRC errors. Metal filling did not affect the circuit performance, as important nets were shielded from the metal filling.

3.6 Packaging and Testing PCB design

Fabricated dies were packaged in QFN48 package of size 6mm X 6mm. The packaging diagram is shown in the appendix. The testing PCB uses potentiometers to generate variable bias currents for the LNA and Mixer. Single pole single throw switches are used to generate digital control bits. The test PCB is fabricated in FR4 material. HFSS simulations showed -10 dB input matching with less than a degree mismatch between differential lines. Packaged die and PCB are shown as follows-

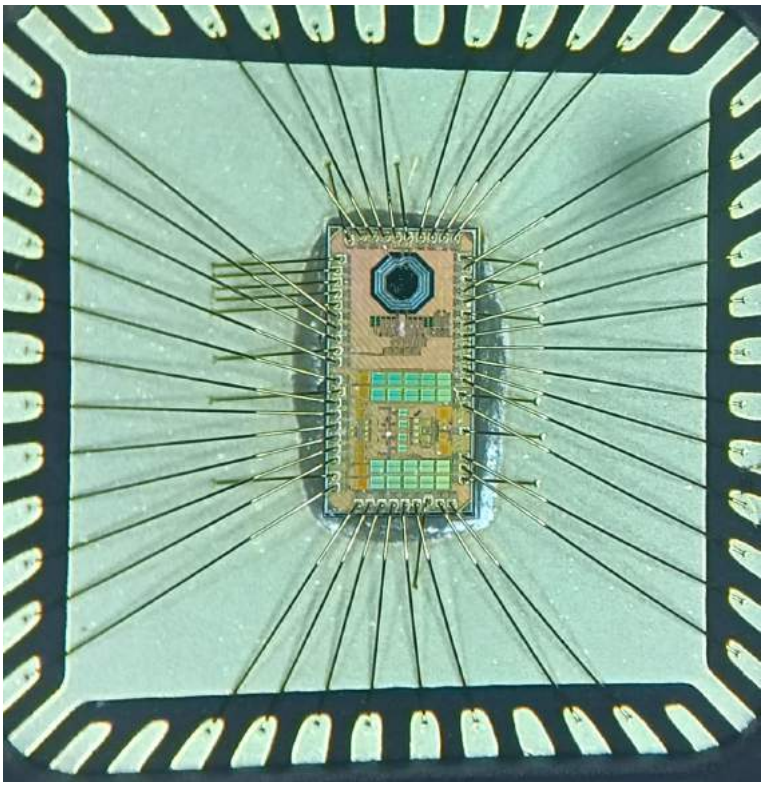

Figure 3.5: NB-IoT Transceiver QFN48 packaging

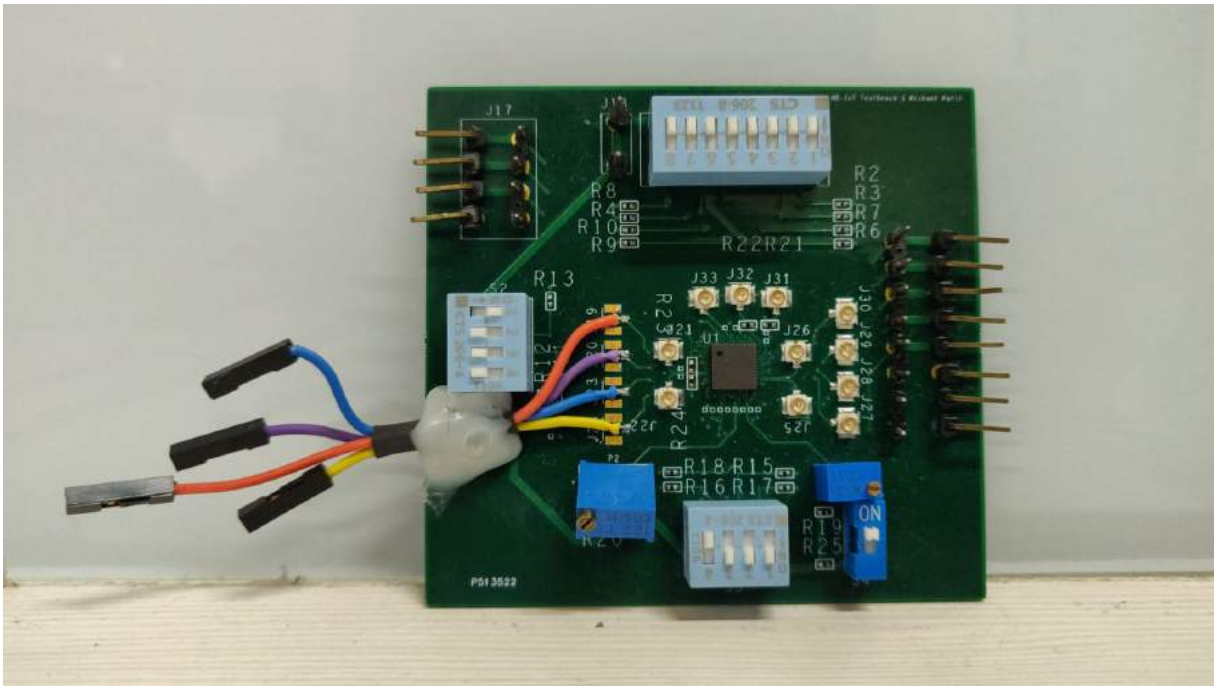

Figure 3.6: NB-IoT Transceiver testing PCB

CHAPTER 4

Measurements and Results

Once the PCB fabrication and QFN packaging were done, we tested IC in the Analog/RF/mm-wave testing lab at IIT Madras. Usually, Voltage Network Analyser (VNA) is used to measure the circuit performance. Output and input for VNA are matched to 50 ohms. However, the output load for this receiver is capacitive and not matched to 50 ohms. Connecting receiver output to 50 ohms instrument will load mixer output and reduce the gain. Hence we used separate instruments to measure the performance, as shown in fig 4.1.

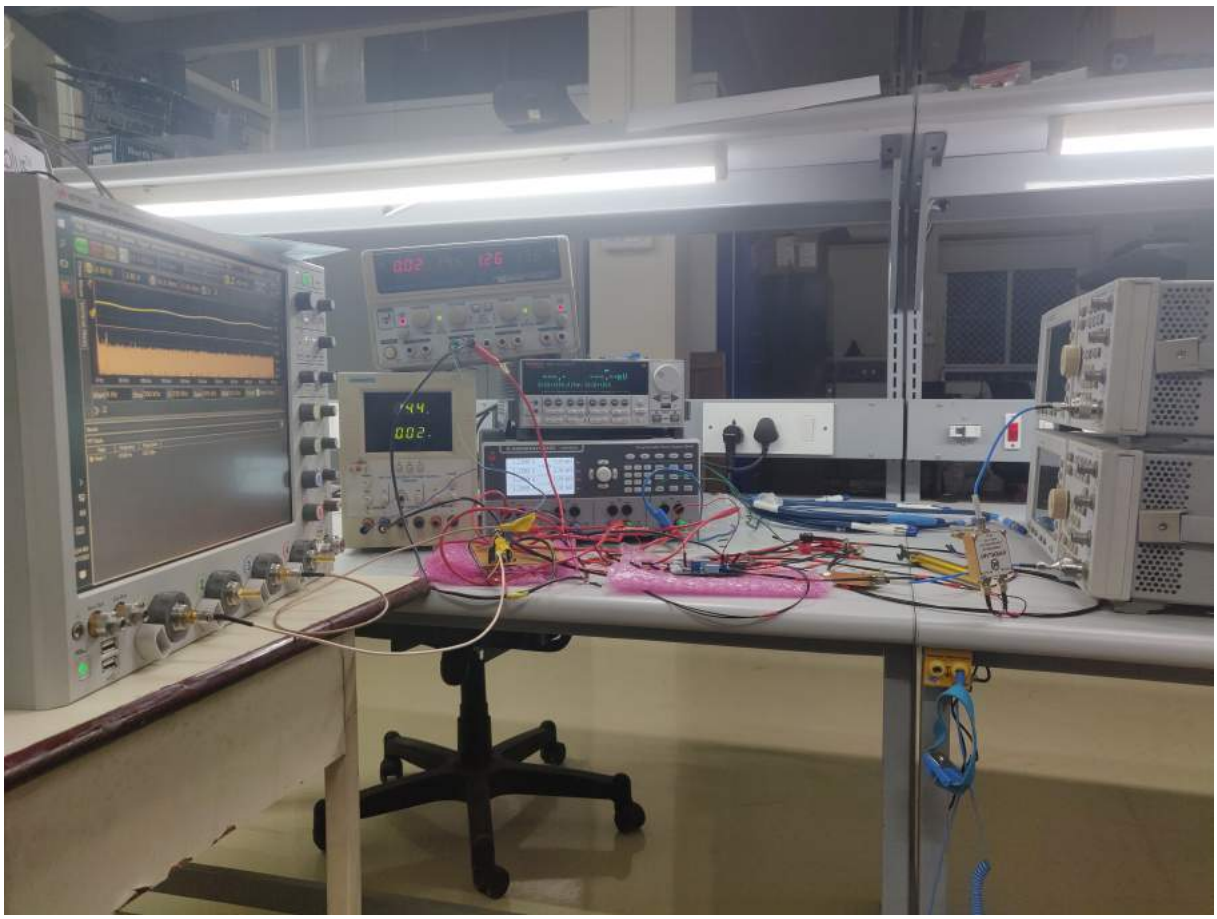

Figure 4.1: Testing setup for measurements

LO and RF input signals were generated using E4422B ESG-A Series Analog RF Signal Generator. HyperLab wideband balun was used to convert single-ended signal from E4422B Signal Generator to differential signal. This signal was fed to the PCB.

Baseband output is fed to DSOS404A High-Definition Oscilloscope, which offers high input impedance. MATH functions were used to find the FFT of the signal.

VNA was used to find input matching of the receiver.

We measured conversion gain, input matching, and power consumption for various gain configurations with the above setup. We could not measure the Noise figure and IIP3 of the circuit as it involves 50 ohms loading of the receiver.

4.1 Simulated Results

The receiver has three gain bit control giving eight different gain configurations. Receiver operates at two frequency bands-

- LTE Band 3 - 1805-1880 MHz referred as High band
- LTE Band 5 - 869-894 MHz referred as Low band

All simulations are done for both bands and gain configurations using RCCC extracted netlist.

4.1.1 Conversion Gain Results

Low Band

Typical corner gain for low band are shown in the fig 4.2. We see a linear gain variation across bits.

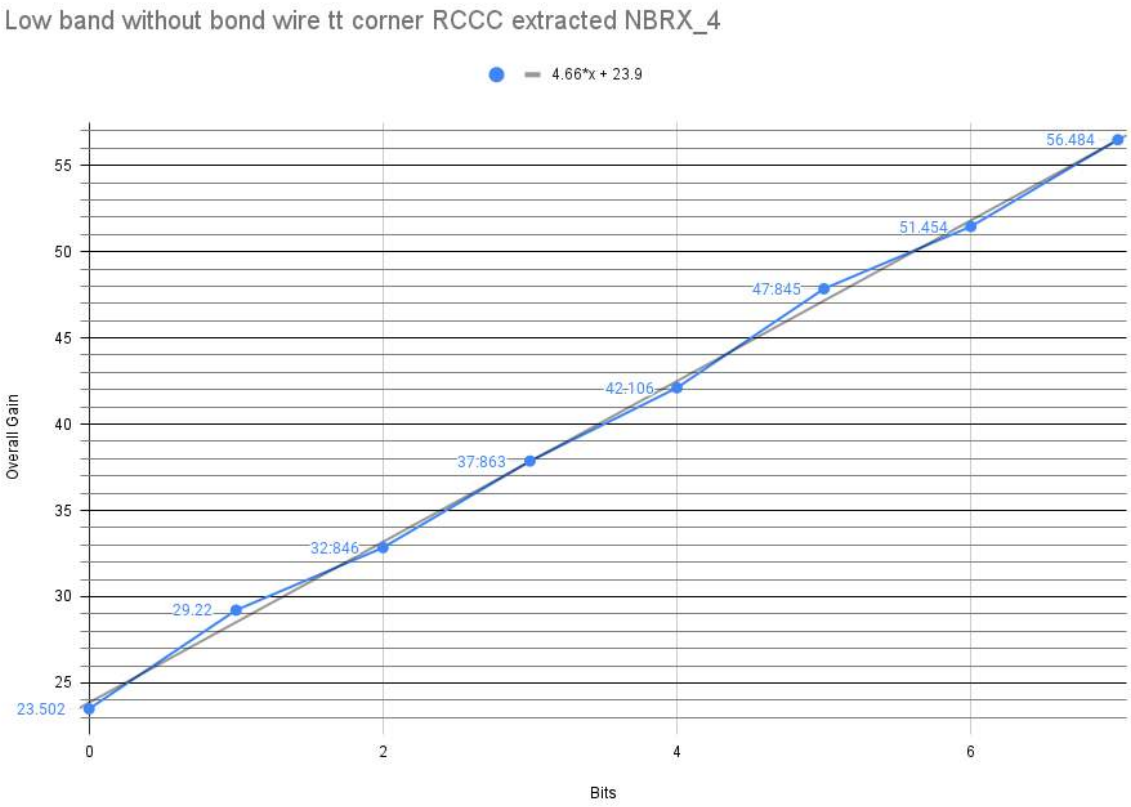

Figure 4.2: Low band TT corner simulation gain results

Process variation- The receiver maintains monotonic gain control for all process coroners as shown in fig 4.3.

High Band

Typical corner gain for high band are shown in the fig 4.4. We see a linear gain variation across bits.

Process variation- The receiver maintains monotonic gain control over all process coroners as shown in fig 4.5.

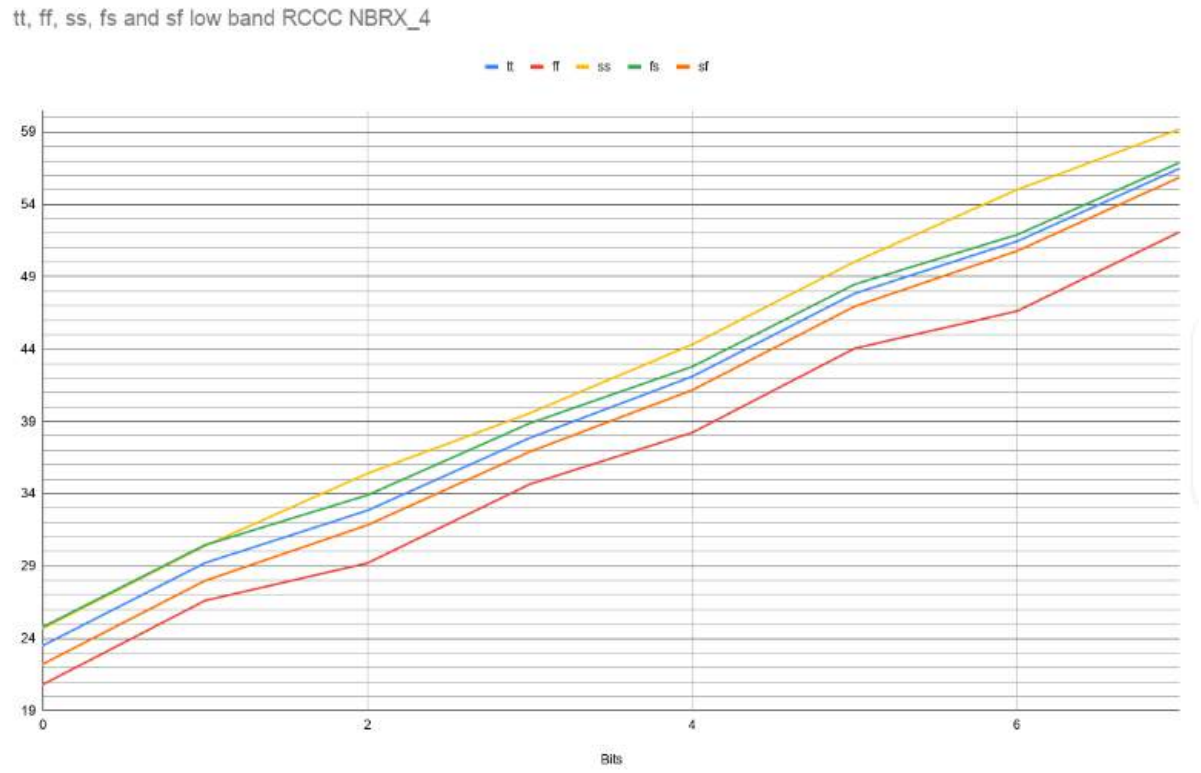

Figure 4.3: Low band process corner simulation gain results

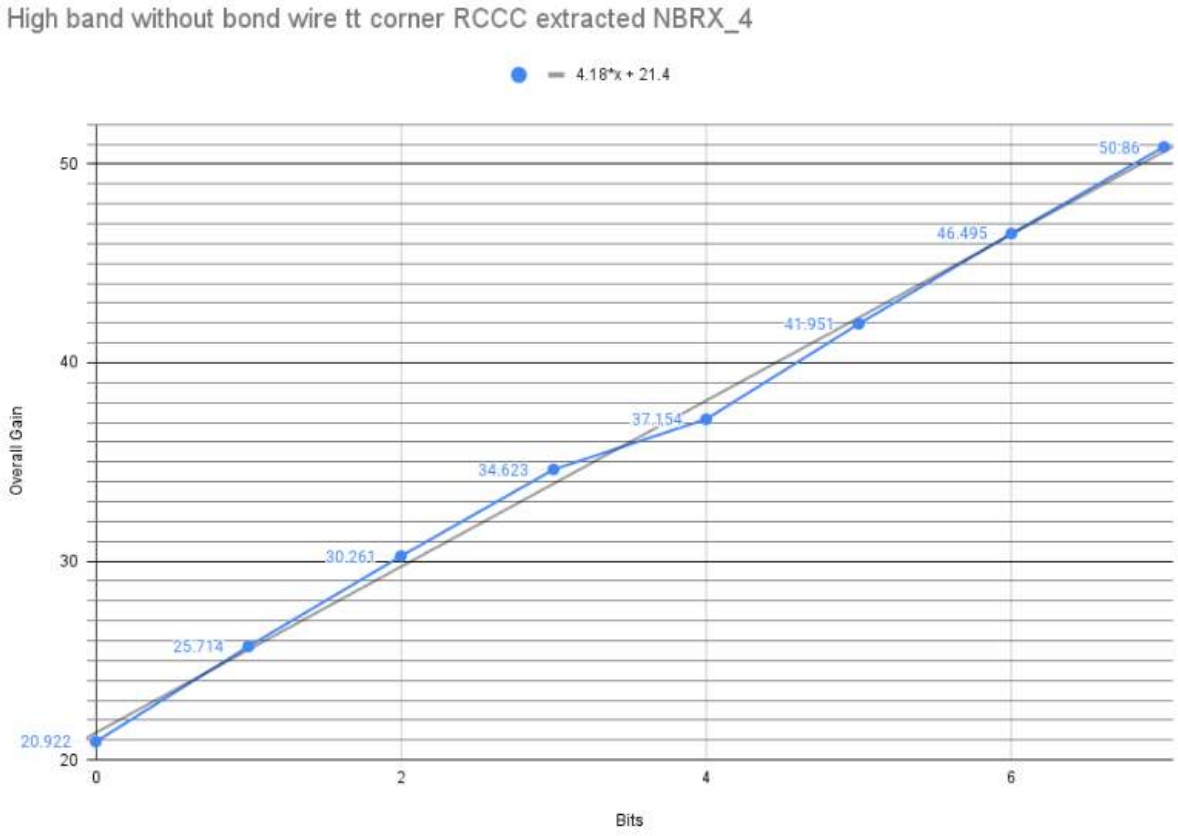

Figure 4.4: High band TT corner simulation gain results

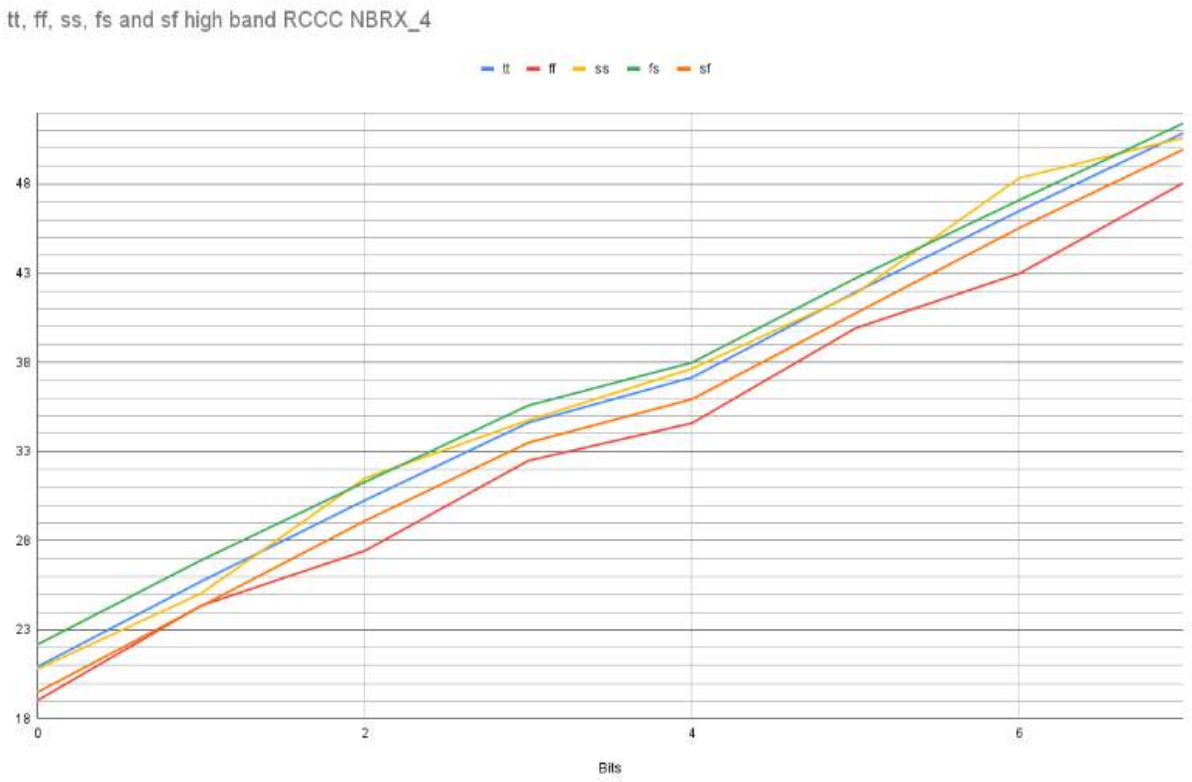

Figure 4.5: High band process corner simulation gain results

4.1.2 The highest Gain Configuration

The highest gain configuration is used when the input RF signal has the lowest power. In this configuration, the receiver offers the highest gain and lowest noise figure and consumes the most power. Receivers noise figure in this configuration is < 6 dB for both bands and hence satisfies 3GPP specification for noise figure 4.7. (refer to derivation of required noise figure in chapter 2.1.1).

Parameter	Low Band @ 894 MHz	High Band @ 1880 MHz
Max Gain at DC	56.39 dB	49.91 dB
Max Gain at 100 KHz	55.32 dB	48.84 dB
Noise Figure	4.235 dB	5.60 dB
Input Matching	-13.57 dB	-12.71 dB
Power Consumption	6.5 mW	7.5 mW

Table 4.1: RCCC extracted results for high gain configuration

4.1.3 The lowest Gain Configuration

The lowest gain configuration is used when the input signal amplitude is maximum. In this configuration, the linearity of the circuit is important. The receiver consumes the least power and offers the highest noise figure in this configuration. 1 dB compression point is > -20 dBm for all process variations and bands. Hence receiver satisfies 3GPP requirements for linearity for both bands, refer 4.2 and 4.4.(refer to derivation of required 1 dB compression point in chapter 2.1.3).

Corner	Overall Gain in dB	Input referred 1 dB compression point in dBm	Output referred 1 dB compression point in dBm
tt	23.86	-13.23	8.871
ff	19.92	-9.47	9.08
ss	25.60	-15.15	8.05
fs	25.10	-14.69	8.65
sf	22.60	-11.98	8.84

Table 4.2: 1 dB compression point for low band

Corner	Overall Gain in dB	Input referred 1 dB compression point in dBm	Output referred 1 dB compression point in dBm
tt	22.08	-14.99	5.37
ff	18.85	-11.95	5.55
ss	22.58	-14.39	5.85
fs	23.27	-17.52	4.04
sf	20.66	-12.74	6.19

Table 4.3: 1 dB compression point for high band

Hence the receiver satisfies all 3GPP specifications for all process corners in both LTE band 3 and LTE band 5.

4.2 Measurement Results

As mentioned earlier, we could not measure the noise figure and 1dB compression point because of the 50 ohms loading issue. Measurement results for input matching and voltage conversion gain are as follows-

4.2.1 Input Matching

We used VNA to measure the input matching of the receiver. The PCB traces were designed with S11 < - 10 dB and RF cables show good matching for the required band.

The measured input matching is better than simulated matching for most cases, as bondwire inductance helped reduce the effect of parasitic capacitance.

B1	B2	B3	Simulated S11 for Low band	Measured S11 for Low band	Simulated S11 for High band	Measured S11 for High band
0	0	0	-17.32 dB	-16.51 dB	-16.75 dB	-18.73 dB
0	0	1	-17.32 dB	-16.51 dB	-16.75 dB	-18.65 dB
0	1	0	-16.63 dB	-15.75 dB	-16.72 dB	-19.00 dB
0	1	1	-16.63 dB	-15.74 dB	-16.72 dB	-19.01 dB
1	0	0	-15.98 dB	-8.47 dB	-13.18 dB	-15.73 dB
1	0	1	-18.98 dB	-8.46 dB	-13.18 dB	-15.71 dB
1	1	0	-13.57 dB	-7.88 dB	-12.35 dB	-14.72 dB
1	1	1	-13.57 dB	-7.85 dB	-12.35 dB	-14.65 dB

Table 4.4: Input matching measurement Vs simulation results

Note- S11 value is not changing much with B3 bit as B3 is used to change mixer's load between active and passive impedance. This will not affect S11 as expected.

4.2.2 Voltage Conversion Gain

The circuit is biased such that power consumption is very close to that of simulated power consumption. Refer to the following subsection for power comparison. With identical power consumption, the measured gain was significantly less than that of simulated results, as shown in table 4.5.

Variation in measured Vs simulated conversion gain is coming because of following parameters-

B1	B2	B3	Simulated Gain for Low band	Measured Gain for Low band	Simulated Gain for High band	Measured Gain for High band
0	0	0	23.06 dB	13.57 dB	19.64 dB	9.41 dB
0	0	1	41.63 dB	29.62 dB	36.23 dB	23.61 dB
0	1	0	28.81 dB	19.46 dB	24.42 dB	14.38 dB
0	1	1	47.40 dB	35.54 dB	41.03 dB	27.7 dB
1	0	0	32.43 dB	18.25 dB	28.89 dB	16.05 dB
1	0	1	51.00 dB	34.2 dB	45.50 dB	30.12 dB
1	1	0	37.49 dB	24.6 dB	33.33 dB	21.18 dB
1	1	1	56.06 dB	42.1 dB	49.94 dB	35.34 dB

Table 4.5: Voltage conversion gain measurement Vs simulation results

- Wire losses- 1 dB at low band, 1.5 dB at high band
- Balun loss- 3 dB
- PCB trace loss- 0.5 to 1 dB
- Output loading due to oscilloscope
- Packaging losses

After considering the above losses, the difference between measured and simulated conversion gain is only 3 to 4 dB. This difference may be coming because of process variation. Further work can be done on PCB design in order to measure gain via VNA. VNA measurements will cancel losses due to RF cables and Balun through calibration. **Monotonic gain control** is retained in the measurement results. All eight gain configurations have almost the same difference. The trade-line also shows a similar slope. This observation supports that the gain reduction is due to external components (which offer the same loss for each configuration) and not due to circuit functionality. Refer fig 4.6 and 4.7.

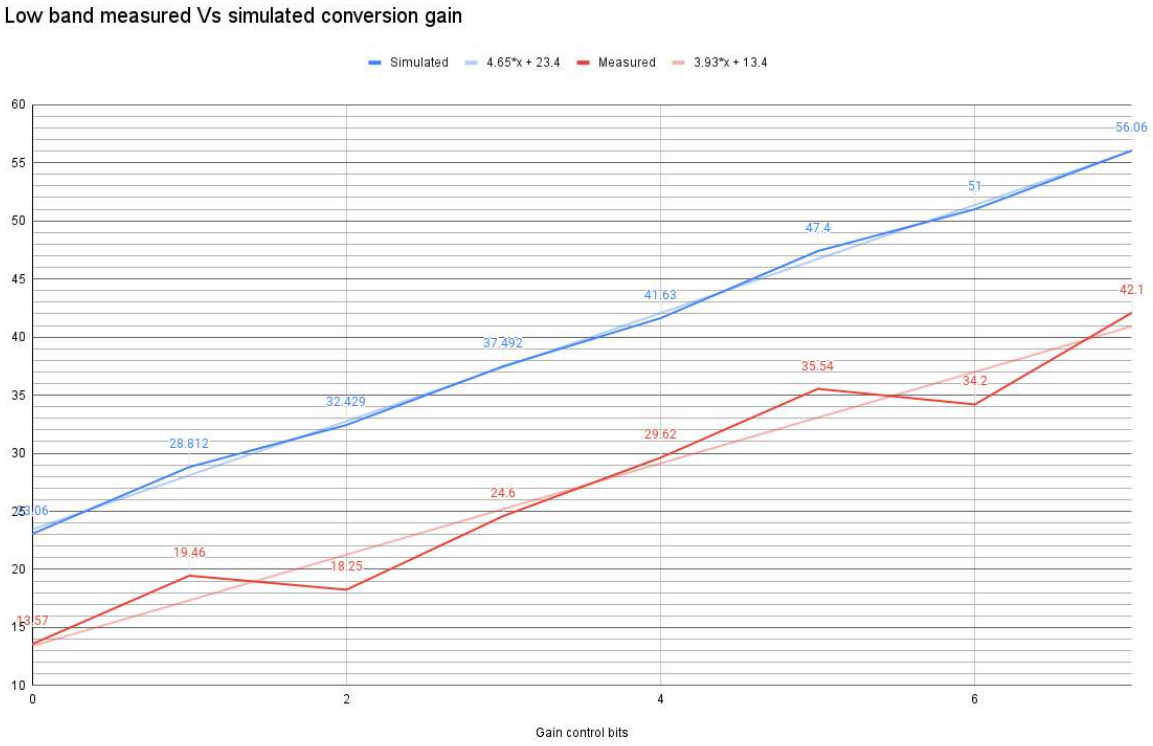

Figure 4.6: Measured and simulated Gain Vs control bits for low band

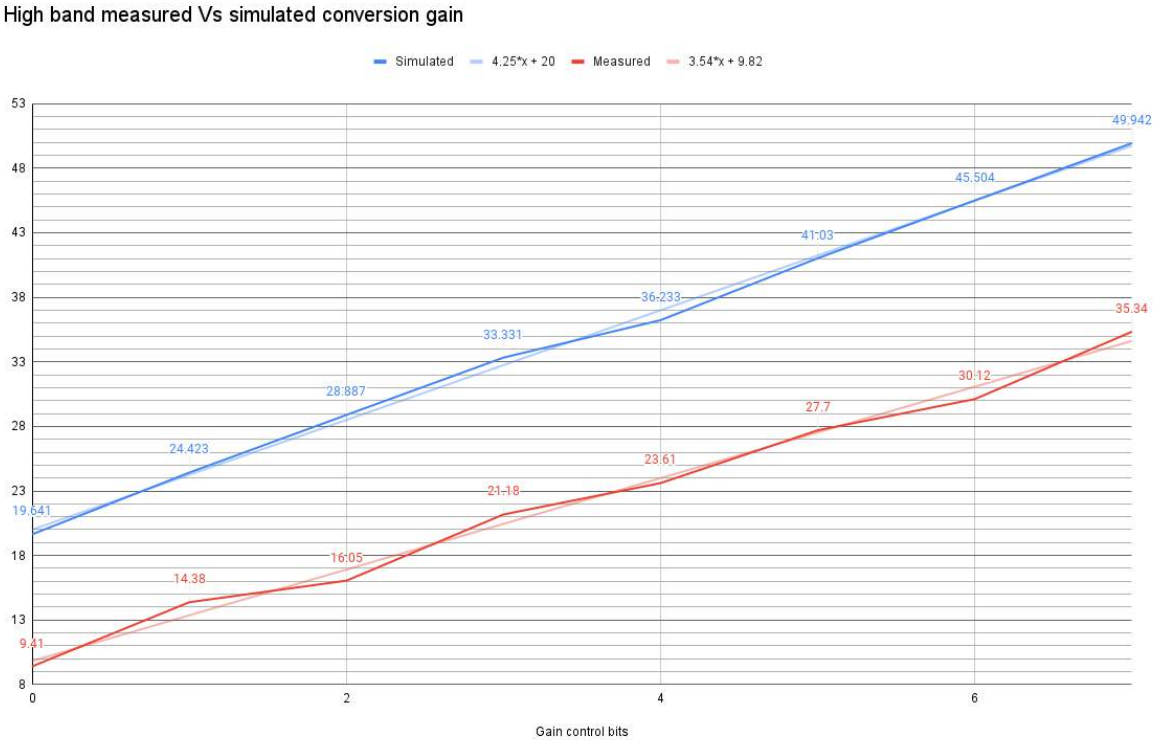

Figure 4.7: Measured and simulated Gain Vs control bits for high band

4.2.3 Power Consumption

Comparison between simulated and measured power consumption is shown in table 4.6.

Design Block	Simulated power consumption	Measured power consumption	(Measured - Simulated) power consumption
Low power mode LNA	1.09 mW	1.71 mW	0.62 mW
High power mode LNA	2.11 mW	2.23 mW	0.12 mW
Mixer	0.33 mW	0.34 mW	0.01 mW
LO divider and buffers @ Low band	2.68 mW	3.10 mW	0.42 mW
LO divider and buffers @ High band	4.89 mW	5.13 mW	0.24 mW
Receiver maximum power consumption	**7.33 mW**	**7.7 mW**	**0.37 mW**

Table 4.6: Simulated Vs measured power consumption

The measurement results align with simulated results for the same power consumption. The whole receiver design is inductorless and consumes less than half power compared to a recent publication in IEEE Transactions on Circuits and Systems on NB-IoT receivers [10].

4.3 Scope for Future Work

4.3.1 On IC Design

This work covers the design and testing of the RF front end for the NB-IoT receiver. The introduction chapter states that this work does not cover baseband filters and amplifiers. Further work can be done in designing these amplifiers and Analog to Digital converters.

4.3.2 On PCB Design and Testing

New PCB can be designed with SMA connectors for RF and LO inputs. Also, a 50 ohms off-chip buffer can be introduced at the baseband output. With these modifications, we can measure noise figure, gain, IIP3, and 1 dB compression point using VNA.

The PCB design for the transceiver does not simultaneously test TX and RX. A surface acoustic wave (SAW) filter can be introduced on PCB for simultaneous testing.

Part II

Ultra Wide-Band Transmitter

CHAPTER 5

Introduction

Ultra Wide-band circuits have many applications in wireless communication, Radar, and sensors. Designing a wide-band circuit is difficult due to parasitic capacitors and bondwire inductance. Existing work [11][12][13] involves various architectures like using multiple power amplifiers or a direct upconverter power mixer. In this work, we designed and fabricated a transmitter operating from 30 MHz to 12 GHz output RF range while giving output power > 6 dBm over the band.

5.1 Design Requirements

This work is a part of the colossal project "VersaComm transceiver." VersaComm project will have a transmitter, receiver, and PLL block. This work covers transmitter design and testing. The requirements for the transmitter are as follows-

- Base Band frequency range- DC to 100 MHz
- Output RF range- 30 MHz to 12 GHz
- Input 2*LO signal from PLL
- Output power > 6 dBm
- Output matched to 50 ohms (Standard requirement)
- Voltage gain required > 0 dB
- VDD = 1.2
- Driven by DAC biased at VDD/2 = 0.6 V

Apart from the above requirements, we have to take care of bond wire inductors and parasitic capacitance due to packaging and PCB.

5.2 Transmitter Architecture

We implemented two-channel upconverter power mixer based transmitter with base-band amplifier and frequency divider circuit as shown in fig 5.1

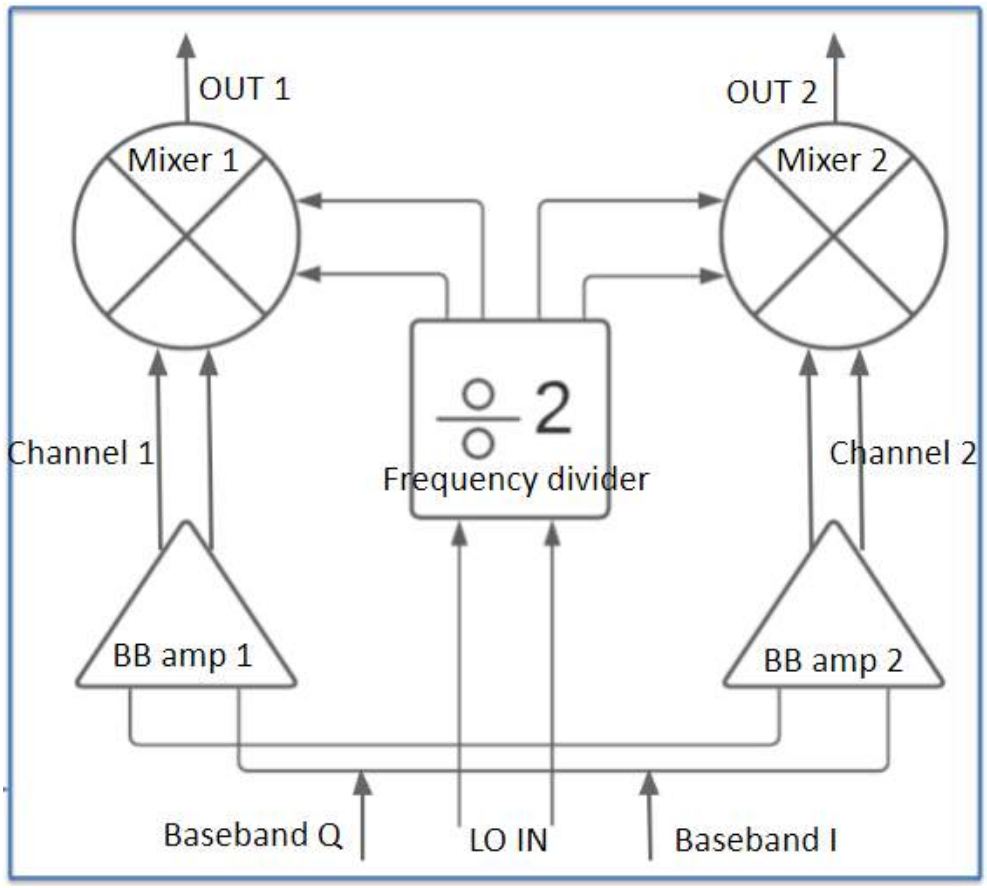

Figure 5.1: Ultra Wide-Band Transmitter Architecture

Two channels are used in order to get high output power. Off chip, a power combiner is used to combine output from two channels. Both channels receive the same baseband and LO signal, and hence their output is in phase.

Input for the LO divider is from 60 MHz to 24 GHz. A single divider circuit was insufficient to cover the whole range, so we used two dividers. Low-frequency divider covers the range of 60 MHz to 5 GHz, while the high-frequency divider covers the range of 4 GHz to 24 GHz. Aditya Narayana designs the high-frequency divider.

Since the input signal is from DC to 100 MHz, we cannot use AC coupling between two stages; hence a special biasing is needed. A baseband amplifier is used to bias the mixer. The mixer's input bias voltage can be set externally.

CHAPTER 6

Design and Circuit Analysis

In this chapter, we will discuss each circuit in detail. We will understand design trade-offs and a few key points about the circuit. We will start with the baseband amplifier, followed by the power mixer and frequency dividers.

6.1 Baseband Amplifier

The motivation to have a separate baseband amplifier comes from the issue of external biasing. As our baseband starts from DC, we cannot use AC coupling capacitors to bias the internal circuit separately. We need to feed the signal directly to the transmitter.

This transmitter will be driven by a digital to analog converter (ADC) with output bias voltage around VDD/2. Since another student will design the ADC, we need some input common-mode range for the transmitter. Circuits like power mixers are susceptible to input bias voltage and do not have an input common-mode range. We implemented OPAMP based baseband amplifier with replica biasing as shown in fig 6.1

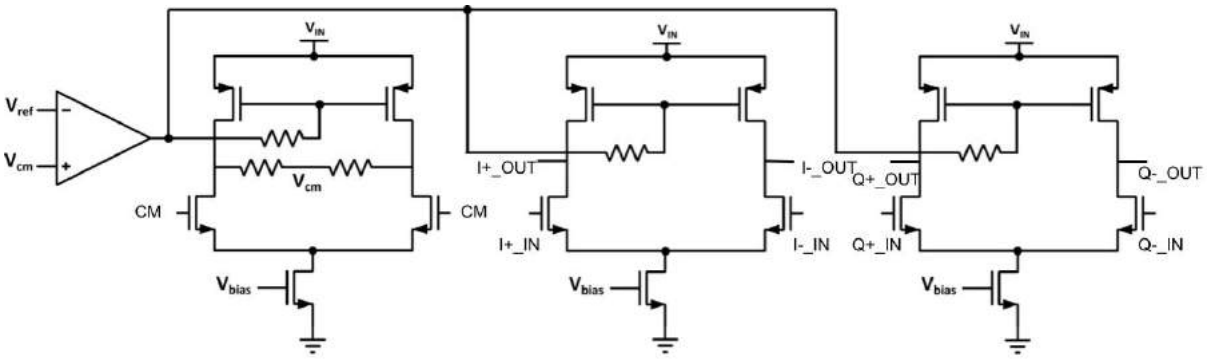

Figure 6.1: Baseband Amplifier circuit

The baseband amplifier gives a gain of 7.3711 dB at 100 KHz and 7.2374 dB at 100 MHz giving a droop of only 0.1337 dB while consuming 68.1 mW of power (for both channels). This is the maximum power consumption, and it can be reduced for low

bandwidth signals by using an External biasing circuit. Sizes of NMOS and PMOS are set to support a wide range of bias currents.

Input common-mode voltage for the amplifier is from 500 mV to 650 mV, giving relaxation on DAC design.

6.2 Power Mixer

Shunt inductive peaking Gilbert cell based power mixer is implemented in this work as shown in fig 6.2.

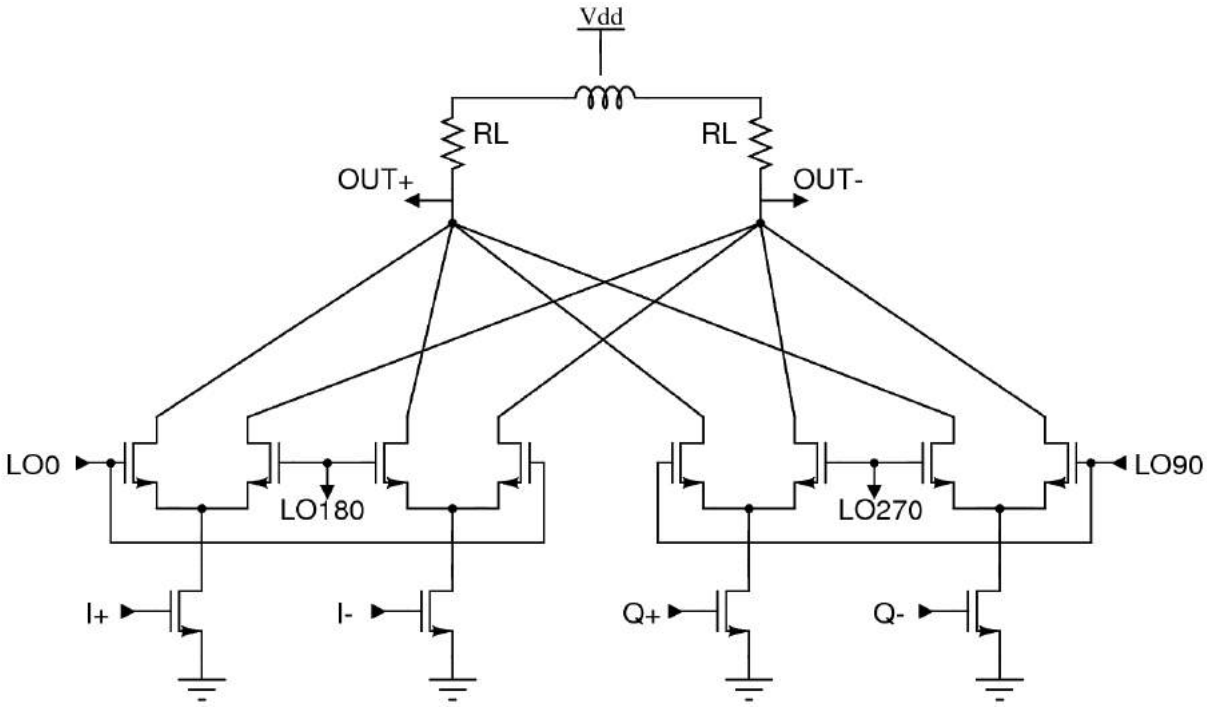

Figure 6.2: Power Mixer circuit

The voltage conversion gain of the mixer is 4.5 dB at 12 GHz. Shut inductor helps to get high gain at high frequencies. Load resistance of 50 ohms is used to avoid external impedance conversation matching circuits for low-frequency range (< 1 GHz). It consumes 25.2 mW (for both channels) while operating at the highest frequency of 12 GHz and 1 dB compression point.

6.3 Frequency Divider and LO Buffers

The frequency divider circuit is implemented using the D flip flop circuit to generate differential I and Q LO signals. We used two frequency dividers because the LO input frequency is vast (60 MHz to 24 GHz). An external digital control bit is used to switch between two dividers. Only one divider will be operating at a time, saving power consumption from another. We used head PMOS and tail NMOS switches to turn off buffers, as shown in fig 6.3.

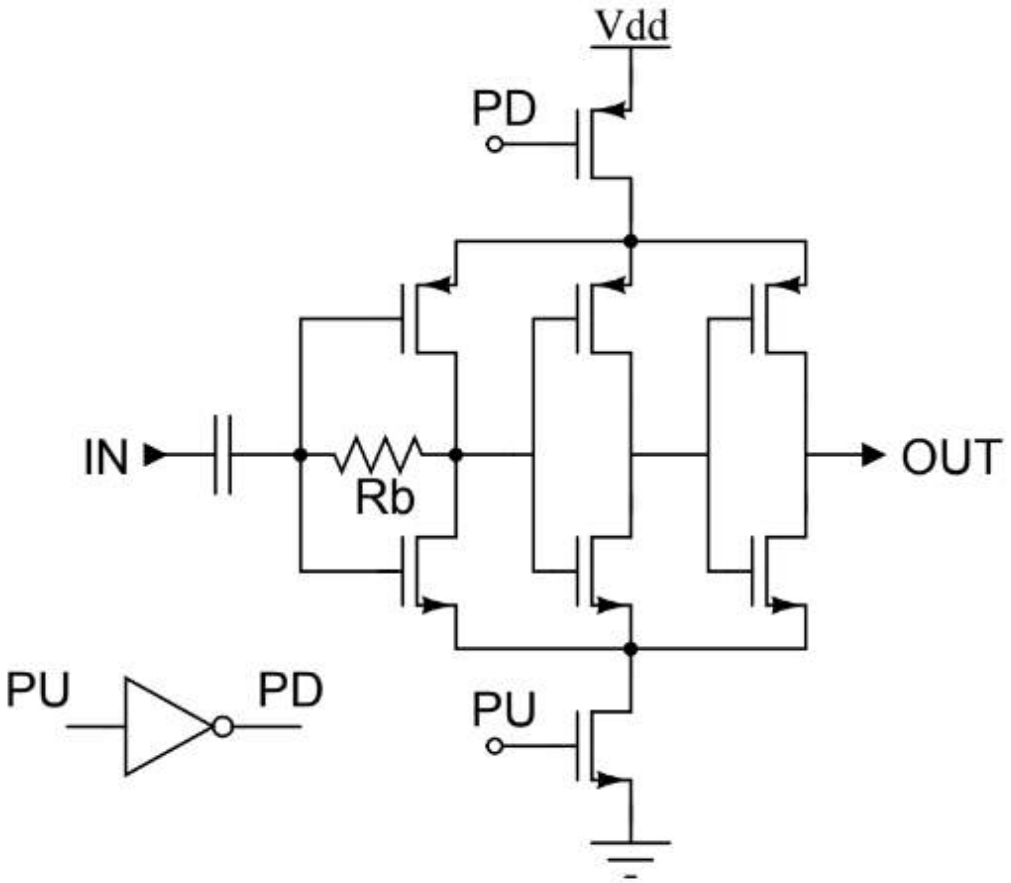

Figure 6.3: LO buffers with power down feature

6.3.1 Low Frequency Divider

The low-frequency divider operates from 30 MHz to 2.5 GHz of the output frequency range. I designed a transmission gate-based D flip flop.

6.3.2 High Frequency Divider

The low-frequency divider operates from 2 GHz to 12 GHz of the output frequency range. Aditya Narayana designed this divider using the Current Mode Logic (CML) based D flip flop.

6.4 Layout

The layout is the most important for high-frequency wideband circuits. A slight mismatch in length can cause a 1-2 deg difference in differential signals as the frequency increases. Also, parasitic capacitance added due to metal connections can kill 3 dB bandwidth for wideband circuits. In the case of the transmitter, the current drawn is high, and hence we have to deal with IR drop also. The layout for the transmitter is as shown in fig 6.4. Two channels are symmetric and have a phase difference of just 0.14 ° at 12 GHz. Even with their symmetric layout, we get a gain difference of 0.9 dB between two channels due to an IR drop in the ground node. This problem can be solved by adding an extra ground pad while integrating with the VersaComm project. (Note- we did not use the symmetric ground pad as available pads were fewer due to the small area.)

Bondwires are used to connect die pads to PCB pads. These Bondwires are made up of Gold and behave inductively, offering high impedance at high frequencies. In order to mitigate this effect, we used two pads in parallel for the output RF signal. This will increase quality inductance by a factor of two.

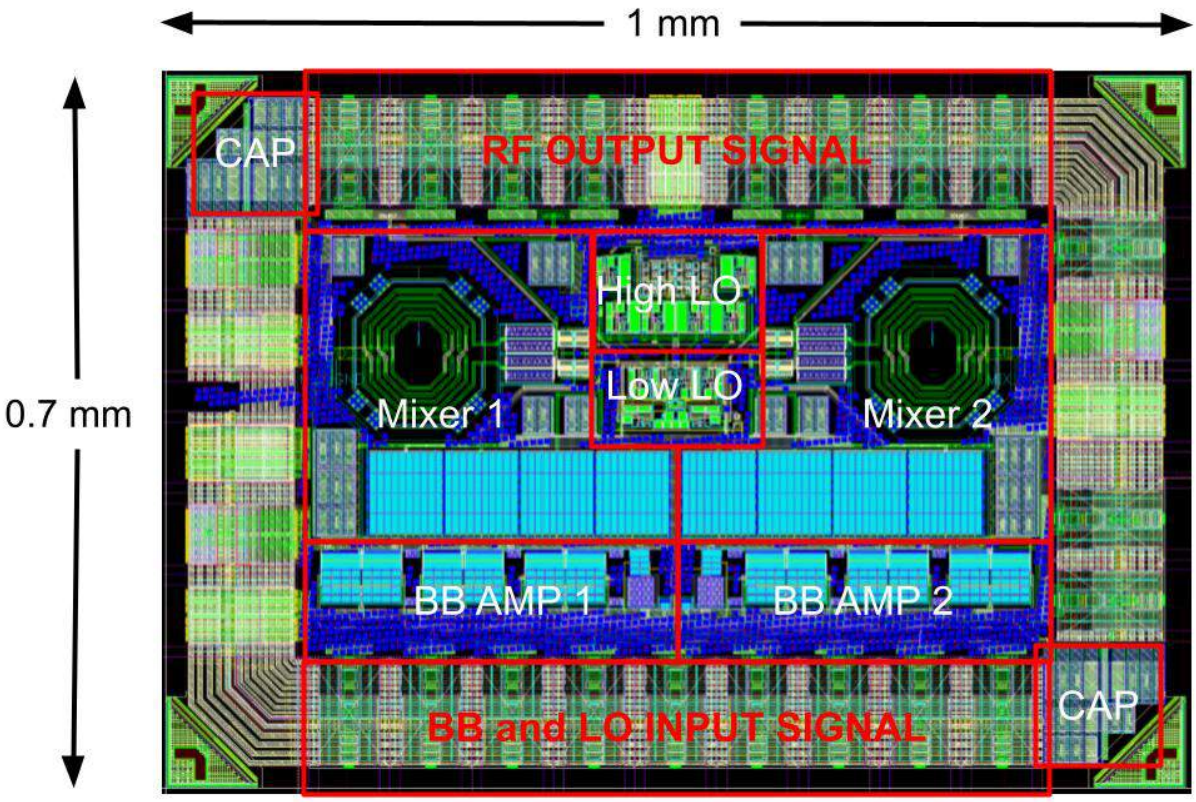

Figure 6.4: Ultra Wideband Transmitter Layout

6.5 Packaging and Testing PCB

As stated earlier, bondwires degrade circuit performance at high frequencies. The length of the bondwire is directly proportional to the inductance value and hence should be minimized. QFN package will offer at least 2-3 mm long wire as the die size is small. This long wire will not allow RF signals to come out or LO signals to enter the die. In order to reduce the length of bondwires, we used Chip onboard packaging, where we directly connect the die to the testing PCB. The packaging diagram is shown in the appendix.

PCB is fabricated on Rogers material as FR4 does not support frequencies > 6 GHz. Custom PCB pads were designed for Chip-on-Board packaging. Output traces are matched to 50 ohms with S11 < -14 dB for the band. All differential signal traces are symmetric with < 1° phase difference till 24 GHz.

PCB has a current bias generating circuit for baseband and baseband opamp amplifiers. A single pole single throw switch is used to implement a digital control bit to

switch between high and low-frequency dividers.

The PCB is shown in fig 6.5.

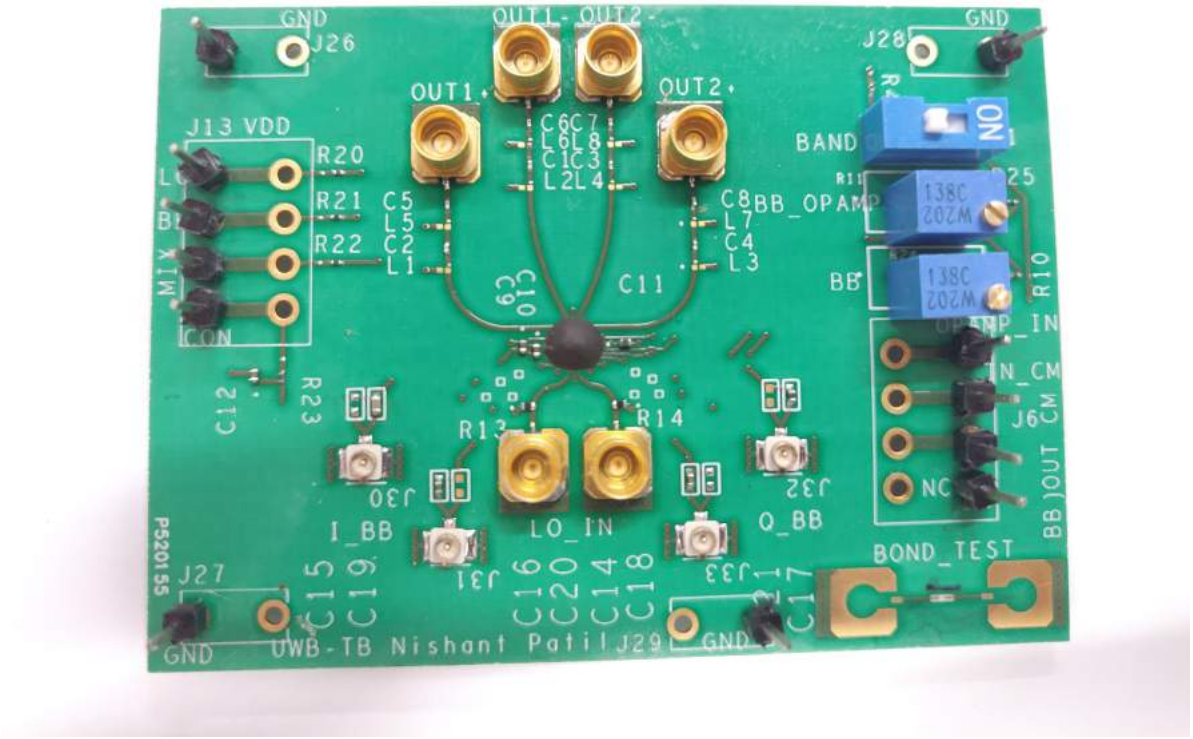

Figure 6.5: Testing PCB for UWB Transmitter

CHAPTER 7

Results and Scope for Future Work

PCB testing is still in progress when writing this report; hence only simulation results are included.

7.1 Simulated Results

RCCC extracted netlist is generated after layout and metal filling. This netlist is used to find voltage conversion gain, 1 dB compression point, and power consumption. We also found a phase mismatch between differential terminals and two channels.

7.1.1 Voltage Conversion Gain

Voltage conversion gain for channel 1 and channel two is found for frequency range of 1 GHz to 12 GHz. The plot is as shown in fig 7.1

7.1.2 1 dB Compression Point

Output 1 dB compression point for two channels is as shown following 7.2. We will use an off-chip power combiner to combine this output power.

The project requires an output power of> 6 dBm after the power combiner, but the simulated results show maximum output power of 4.23 dBm. 1 dB compression point can be increased by biasing mixer at lower potential voltage. Since the 1dB compression point simulation on the RCCC netlist take around 2-3 days, we could not find optimal biasing voltage for the mixer. However, we can find this voltage while testing the IC, as the measurement time for finding a 1 dB compression point is more diminutive than simulations. We expect six dBm output power after biasing optimization.

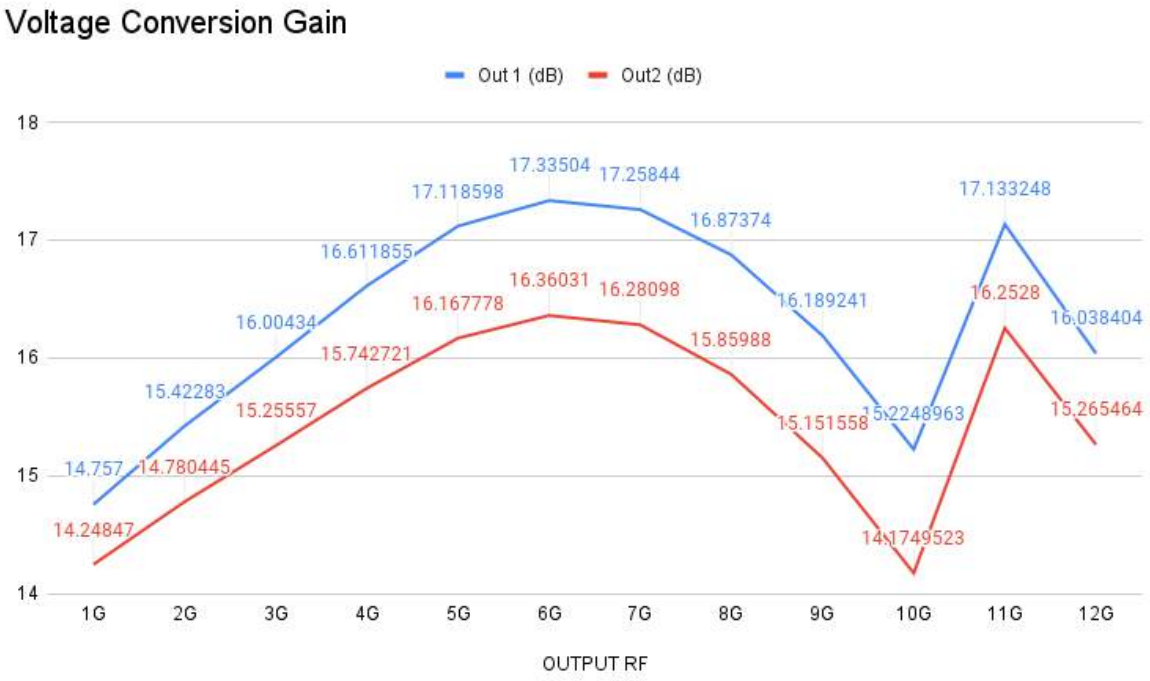

Figure 7.1: Conversion Gain Vs frequency

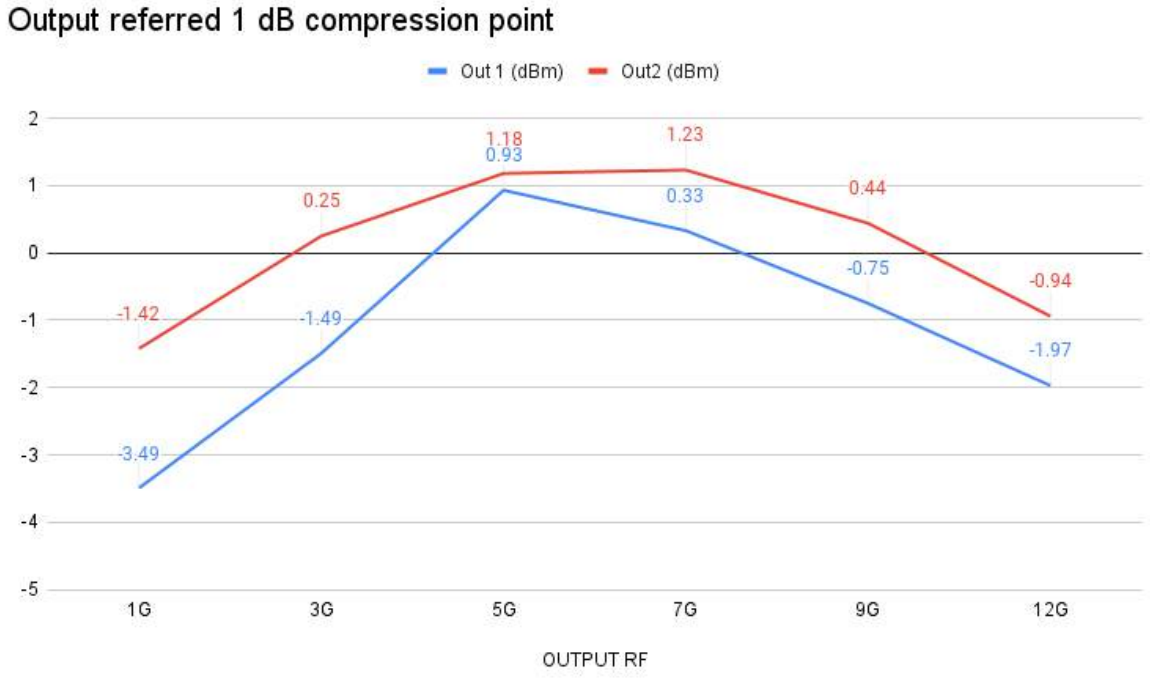

Figure 7.2: 1dB compression point Vs frequency

7.1.3 Maximum Operating Frequency Considerations

The circuit consumes the most power when operating at the highest frequency, 1 dB compression point. Hence this subsection will report the block-wise highest power consumption. Also, the differential signals will show maximum mismatch for 12 GHz as the wavelength is shortest.

- Phase mismatch- Differential phase error for channel 1- 0.32° Differential phase error for channel 2- 0.46° Differential phase error between two channels- 0.14°
- Power consumption including both channels- Baseband Amplifier- 68.1 mW Power Mixer- 25.2 mW LO divider and buffers- 39.4 mW
- Output matching at 12 GHz, after using matching network- -10.5 dB

7.2 Scope for Future Work

This IC covers the design of a baseband amplifier, power mixer, and frequency divider. This transmitter can be driven by a DAC or baseband filter. Furthermore, the LO signal is fed externally to this IC, and we faced an issue due to the high impedance of bond-wires at 24 GHz. PLL operating from 60 MHz to 24 GHz can be integrated into this IC to avoid that issue.

APPENDIX A

LNA topology circuits

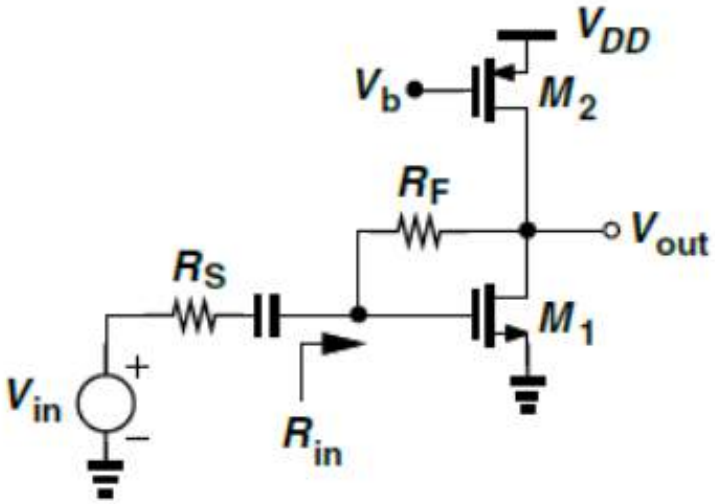

Figure A.1: Common source with resistive feedback Circuit

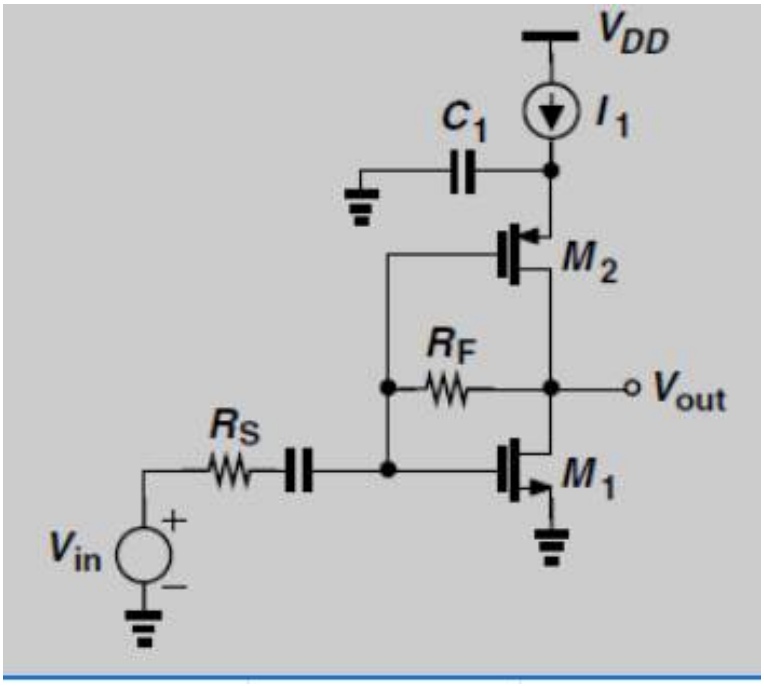

Figure A.2: Common source with resistive feedback with improved noise figure

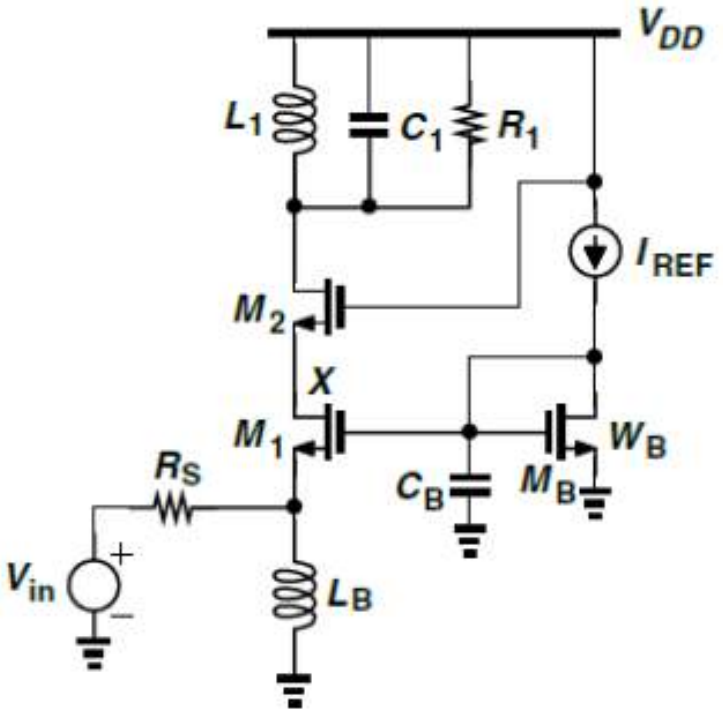

Figure A.3: Common gate with cascode and inductive degeneration

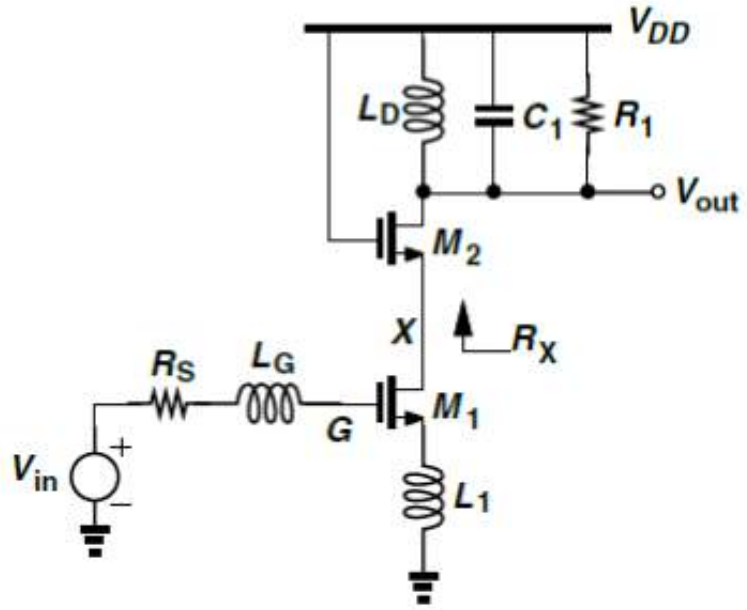

Figure A.4: Cascode common source stage with inductive degeneration

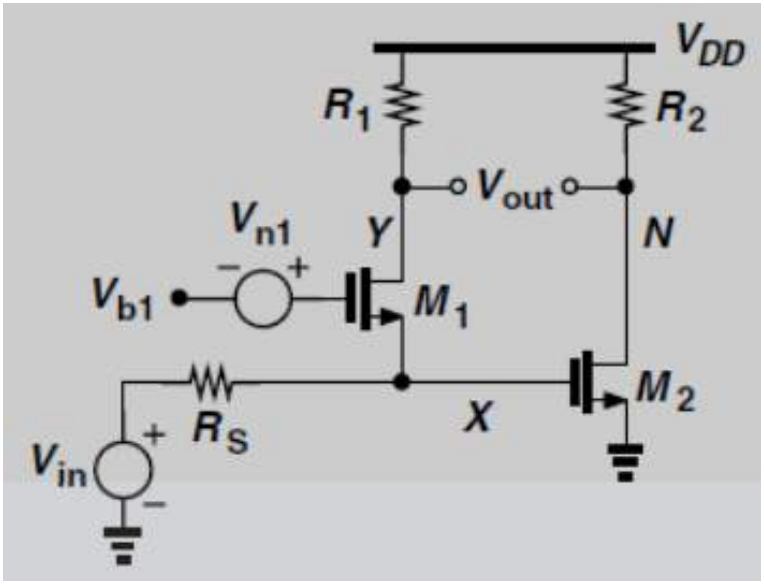

Figure A.5: CG-CS noise canceling LNA

APPENDIX B

Packaging Bonding Diagram

B.1 Narrow-Band IoT Receiver

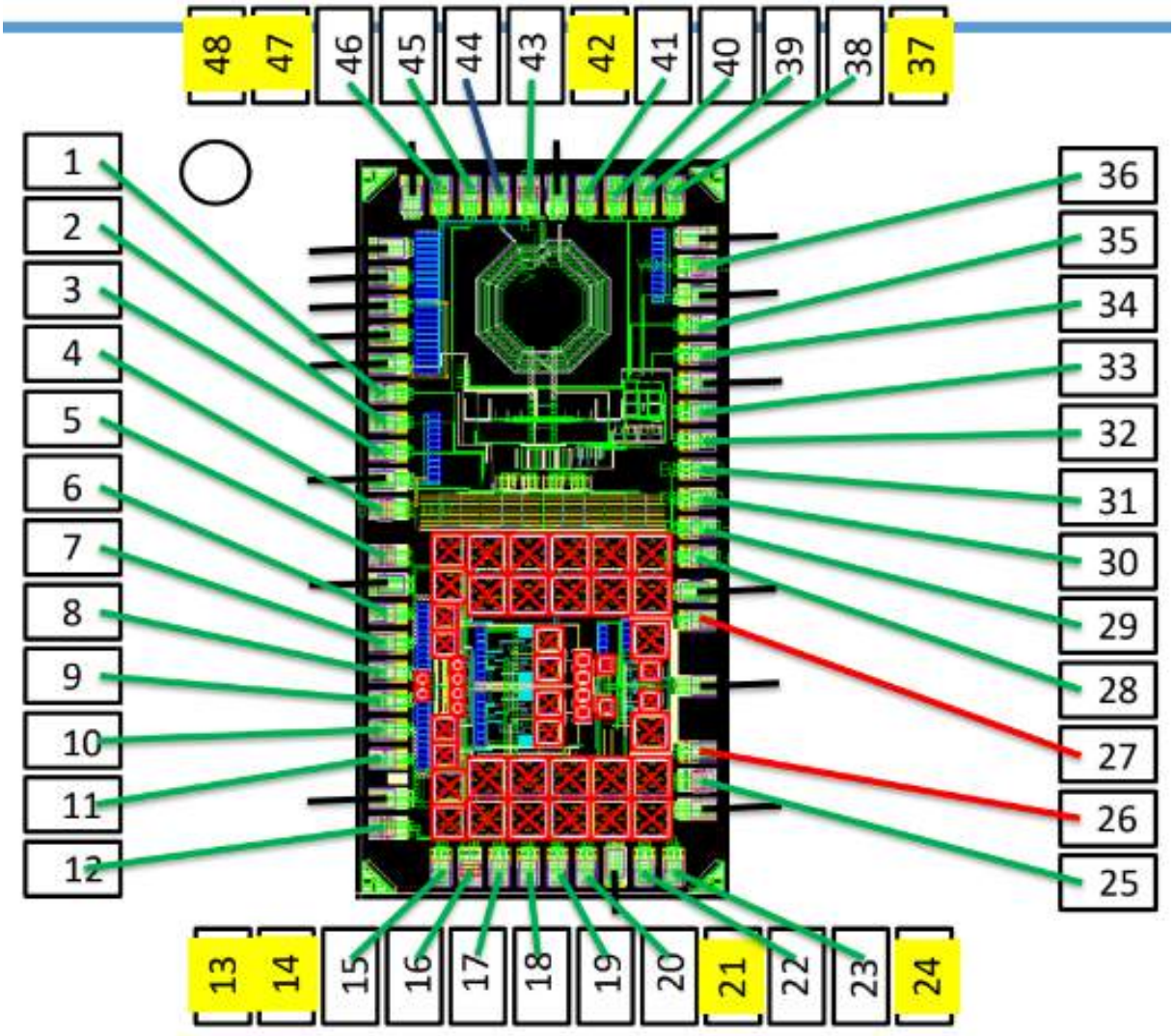

Figure B.1: QFN48 bonding diagram

B.2 Ultra Wide-Band Transmitter

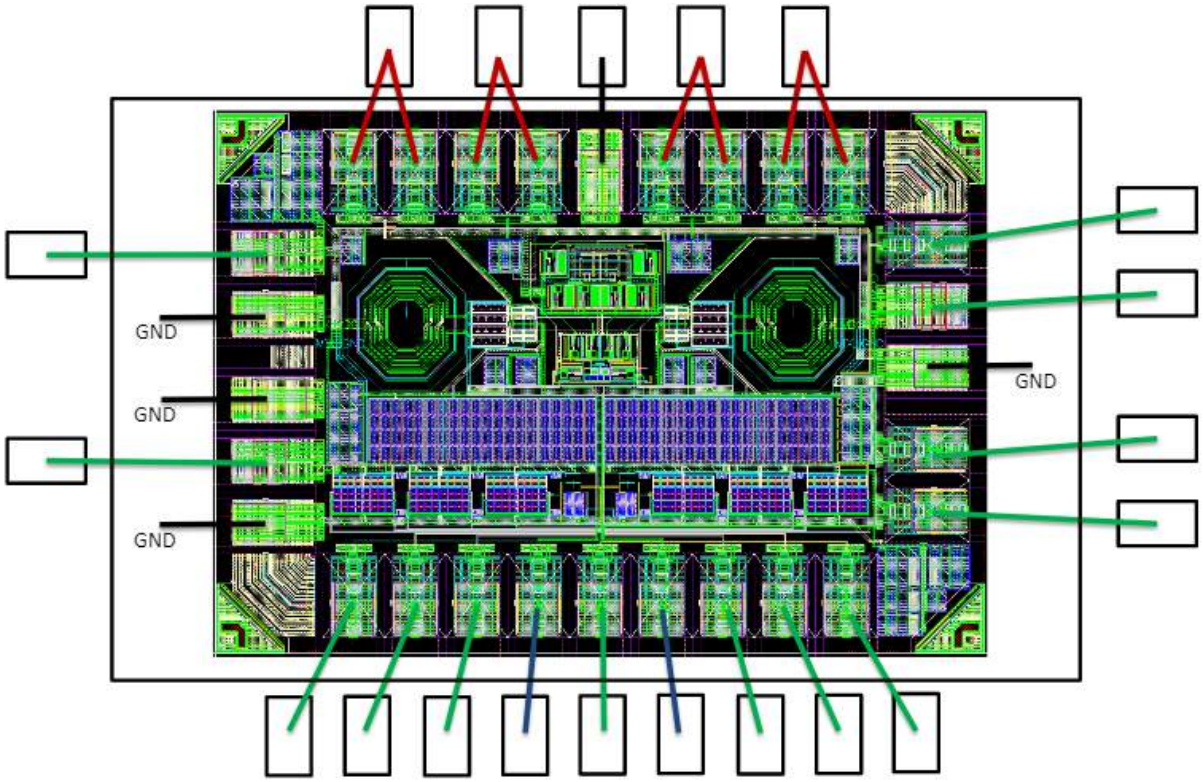

Figure B.2: Chip on Board bonding diagram

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