FAULT TOLERANT CASCADED H-BRIDGE INVERTER FED INDUCTION MACHINE

A Project Report

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THESIS CERTIFICATE

This is to certify that the thesis titled **FAULT TOLERANT CASCADED H-BRIDGE INVERTER FED INDUCTION MACHINE**, submitted by **MANOJ B ANURAG**, to the Indian Institute of Technology Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the project work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Abstract

Multilevel inverters are a class of power converters which form a very important part of a medium voltage drive. These converters are preferred choice over conventional two-level Voltage Source Inverters (VSI) for MV applications as they can be built using devices of lower voltage rating and also have a greatly reduced THD for the output voltage.

Some of the popular multilevel topologies include Neutral Point Clamped inverter (NPC), Flying Capacitor Inverter, Cascaded H-Bridge Inverter. To produce Nlevels in the output phase voltage of the inverter the minimum number of switches required is $2(N-1)$ in each leg of the inverter. However, the usage of more number of switches affects the reliability of the inverter. Multilevel inverter topologies are generally prone to converter faults due to the presence of more number of switches which increase the probability switch related faults. Among the popular topologies mentioned, the Cascaded H-Bridge Inverter has a better fault-tolerant capability making it preferable choice in critical applications.

The main aim of this project is to study different modulation and control schemes for a cascaded H-bridge inverter fed induction motor drive and also develop control schemes for improving the fault tolerance of the Cascaded H-Bridge Inverter freely enabling drive operation even under faulted conditions. Simulation studies are carried out in MATLAB/Simulink environment. Hardware implementation is done with 13.5kVA,7-level cascaded H- bridge inverter fed Induction motor drive.

KEYWORDS: Medium Voltage drive; Multi-level Inverter

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ABBREVIATIONS

AC	Alternating Current
ADC	Analog - Digital Converter
CAN	Controller Area Network
CHB	Cascaded H Bridge
DC	Direct Current
FACTS	Flexible AC Transmission Systems
FC	Flying capacitor
IGBT	Insulated Gate Bipolar Transistor
JTAG	Joint Test Action Group
MCB	Miniature Circuit Breaker
PD	Protection and Delay
PI	Proportional and Integral
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modualtion
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
VVVF	Variable Voltage Variable Frequency
IM	Induction Motor

NOTATIONS

v_{sd}, v_{sq}	Instantaneous stator voltage in *dq0*, V
i_{sd}, i_{sq}	Instantaneous stator voltage in *dq0*, I
R_s	Stator resistance, Ω
R_r	Rotor resistance, Ω
L_s	Stator inductance, H
L_r	Rotor inductance, H
L_m	Magnetising Inductance, H
τ_r	Rotor Time Constant, s
ω	Electrical speed of Rotor, rad/s
ω_m	Mechanical speed of Rotor, rad/s
ω_s	Electrical speed of the rotor flux phasor, rad/s
i_{mrref}	Rated value of the magnetising current, A
ρ	angular position of the rotor flux phasor, rad
V_{ar}	The RMS value of phase voltage of phase A, V
V_{br}	The RMS value of phase voltage of phase B, V
V_{cr}	The RMS value of phase voltage of phase C, V
V_{abr}	The RMS value of line - line voltage between phases A and B, V
V_{bcr}	The RMS value of line - line voltage between phases B and C, V
V_{car}	The RMS value of line - line voltage between phases C and A, V
I_{ar}	The RMS value of phase current of phase A, V
I_{br}	The RMS value of phase current of phase B, V
I_{cr}	The RMS value of phase current of phase C, V

CHAPTER 1

Introduction

1.1 Medium Voltage Drives

Medium voltage drives are an important part of industries with high power requirement. Generally, a medium voltage drive operates at voltage ratings of 2.3kV-13.8kV and power ratings of ranging from hundreds of kW to tens of MW. Medium voltage drives are used in compressors and pumps in oil and gas industries, extruders, pumps and fans in cement industries, boiler feed pumps and conveyors in power in industries, marine applications and petrochemical industries.

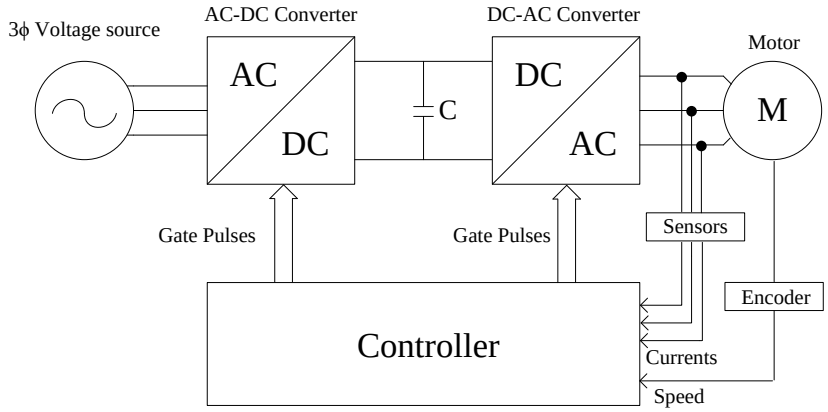

Figure 1.1: Power Structure of a Medium Voltage Drive

In a medium voltage drive, AC-DC converter is used to convert AC input voltage to DC voltage. AC-DC converters include multi-pulse diode bridge rectifiers, multi-pulse SCR rectifiers or pulse-width-modulated rectifiers. DC voltage is converted to AC voltage by a DC-AC converter or an inverter. The frequency and amplitude of the AC voltage depend on the speed at which the motor is operated. AC-DC converter and DC-AC converter are connected through a capacitor. This capacitor with DC voltage acts as a voltage source to the inverter. Generally, Voltage Source Inverter (VSI) is used as a DC-AC converter. There are different topologies for a VSI. The most common topology of a VSI is the conventional

two-level inverter. VSI consists of semiconductor devices which act like switches. Different modulation schemes are used to control the VSI so that balanced sinusoidal currents are injected into the machine. Some of the popular modulation schemes are sinusoidal PWM, space vector PWM.

Conventional two-level VSIs have some disadvantages. Devices used in a conventional two-level VSI should block the DC bus voltage which is in a range of 3kV-15kV. This results in high $\frac{dv}{dt}$ across the device. Though the devices of higher rating are available, they are very expensive. Another disadvantage is the harmonic component present in the voltage which produces a ripple in the motor currents due to which copper losses in the machine are increased. A pulsating torque is developed in motor due to the ripple present in the current which can affect the mechanical components of the motor. In order to reduce the harmonic content in the voltages applied to the motor passive filter like L filter and LC filters are used. But as the power rating is large the size of these filters is also large.

1.2 Multi-level Inverters

To overcome these difficulties, Multi-level inverters are used. Multi-level Inverters are a class of power converters where the number of levels in a pole voltage is more than two. The number of levels in output voltage depends on the number of devices in each phase and modulation index of the modulating signal. Multi-level inverters are used in medium voltage drives and FACTS devices. The advantages of Multi-level inverters are:

- Devices of lower rating can be used.
- Harmonic Content in the output voltage can be decreased which results in the reduction of ripple current.
- As the harmonic content is very less, usage of filters is not required.

In multi-level inverters, devices are connected in series with a different arrangement of diodes and capacitors. Some of the popular topologies are:

- Neutral Point Clamped Inverter(NPC).

- Flying Capacitor Inverter(FC).
- Cascaded H-Bridge Inverter.

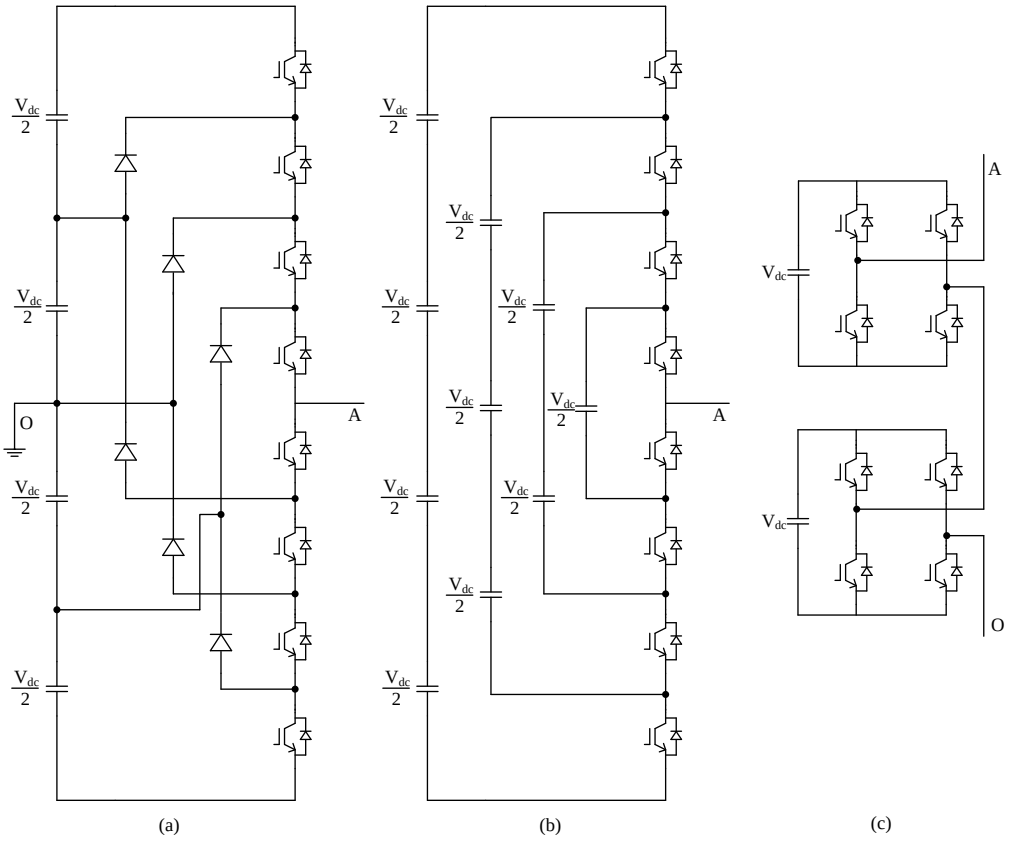

Figure 1.2: A single leg of a (a):7-level Neutral Point Clamped Inverter (b):7-level Flying Capacitor Inverter (c):7-level Cascaded H-Bridge Inverter

1.2.1 Neutral Point Clamped Inverter(NPC)

Neutral point clamped Inverter is also known as Diode Clamped Inverter. One leg of NPC inverter is shown in *Fig:1.2(a)*. In this topology, the neutral point is the point which divides DC bus voltage into two equal halves. It is connected to the point which is in between the series connection of two clamping diodes. The minimum number of switches required to get N levels is $2(N-1)$ in each leg of the inverter.

Advantages

- All the legs share a common DC bus.
- Control schemes are relatively simple.
- Reactive power flow can be controlled.

Disadvantages

- Clamping diodes of different voltage rating are required.
- Number of clamping diodes increases with the number of levels.
- The fluctuations in neutral point voltage results in uneven voltages of the devices.

1.2.2 Flying Capacitor Inverter(FC)

Flying Capacitor Inverter is also known as Capacitor Clamped Inverter. One leg of FC inverter is shown in *Fig:1.2(b)*. In this topology, the series connection of two clamping diodes is replaced by the series connection of clamping capacitors. The minimum number of switches required to get N levels is $2(N-1)$ in each leg of the inverter. All the switches are connected in series.

Advantages

- Neutral point fluctuations are not present.
- Active and reactive power flow can be controlled.

Disadvantages

- The number of capacitors increases with the demand of the number of levels in each leg of the inverter.
- Complex control is required to maintain capacitor's voltage balance.
- The size of the inverter is increased with the presence of a large number of capacitors.
- Size of the capacitor is large as it carries carries load current.
- Complex bus bar design.

1.2.3 Cascaded H Bridge Inverter(CHB)

Cascaded H Bridge Inverter is one of the most popular multi-level inverter topologies used in industries. One leg of CHB inverter is shown in *Fig:1.2(c)*. The minimum number of switches required to get N levels is $2(N-1)$ in each leg of the inverter. In this topology, the devices are not connected in series but the full H bridge inverters are connected in series or cascaded.

Advantages

- The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.
- No extra clamping diodes or voltage balancing capacitors are necessary.
- Control methods are simple.

Disadvantages

- It requires isolated DC sources to all the H-Bridge inverters.
- In all the three topologies discussed if the rating of the device is same then the number of devices required in each leg of CHB inverter is double that of the number of devices required in each leg of NPC and FC inverters because DC voltage of the capacitors.
- If the number of devices in each leg of the inverter for all the three topologies is same then, the device rating of devices in CHB inverter is more than the device rating of the devices in NPC and FC inverters.

The main disadvantage of multi-level inverters is reduced reliability. The number of devices in the multi-level inverters is high, so the probability of a device failure is also high. If any failure of a device happens in one phase, then that phase of the inverter is open which results in unbalance of the currents. This unbalances of the currents results in oscillations of the speed which is not desirable for operating the machine. Because of this unbalanced currents, the motor is forced to shut down which interrupts the process in any application. This type of fault is more prominent in the NPC and FC multi-level inverter topologies because of the series connection of the switches. There is no methodology to overcome these faults with respect to these converters.

In cascaded H-Bridge multilevel inverter topology, this type of problems can be resolved. The cascaded Multilevel inverter is constructed using different cells consisting of a full H Bridge inverter.Each H-Bridge inverter is represented as one cell or one block. All these cells are connected in series or cascaded. So, if any device failure happens in any of the cells, then that cell can be bypassed and the inverter can be operated. This results in an unbalance in the phase voltages of the inverter which leads to unbalanced line voltages and unbalanced currents in the machine. The machine only sees the line voltages. In order to get balanced line voltages, the modulating signals which are given to the inverter should be modified.

This process should be done in short period of time so that the operation of the motor is not affected.

1.3 Organization of thesis

This thesis is organized into four chapters.

Chapter 2 explains about cascaded H-Bridge multi-level inverter topology and control schemes for fault rectification with both scalar control and vector control techniques, and develops an algorithm for the smooth transition under faulty conditions.

Chapter 3 discusses hardware organization of cascaded H-bridge multi-level inverter-fed induction machine drive. A brief discussion about DSP-FPGA based hybrid board, Protection & Delay card and details of sensors is also included.

Chapter 4 discusses the simulation of cascaded H-bridge inverter-fed induction machine under fault conditions using scalar control and vector control techniques and hardware implementation of control schemes with a 10 kVA Cascaded H Bridge Inverter on a 30 kW induction machine.

Chapter 5 discusses the conclusions and future scope of the work.

CHAPTER 2

Control Schemes for Cascaded H-Bridge inverter

2.1 Cascaded H-Bridge Inverter

Cascaded H-Bridge Inverter is one of the most widely used topology of the multi-level inverters in medium voltage drive. It consists of full H-Bridge inverters which are connected in series in each phase. Generally, each of these full H-bridge inverters has an isolated DC source which can be a renewable energy source or a charged capacitor. Each H-Bridge inverter has a capacitor which acts as a DC voltage source. It is charged by a diode bridge rectifier. If the total DC bus voltage that is required is V_{dc} then each capacitor must be charged to a voltage of $\frac{V_{dc}}{N}$. The input to the diode bridge rectifier is given from the secondary of a step-down transformer. Each H-Bridge inverter with a parallel combination of a capacitor and a resistor with large resistance and a diode bridge rectifier is considered as one cell. The resistance is connected in parallel to the capacitor for the discharging of the capacitor when the power is turned off. If there are N cells in each phase of the multi-level inverter, then the maximum number of levels that are possible in the phase voltage of the inverter is $2N + 1$. The power structure of cascaded H-bridge inverter and internal configuration of each cell is described in *Fig.2.1* and *Fig.2.2* respectively. The advantages of this topology :

- It can be scaled for both voltage and power levels by adding cells.
- It has good fault tolerance compared to other topologies because of it's cascading nature.
- Cascaded cell can be developed as pluggable modules that can be easily inserted/removed for maintenance

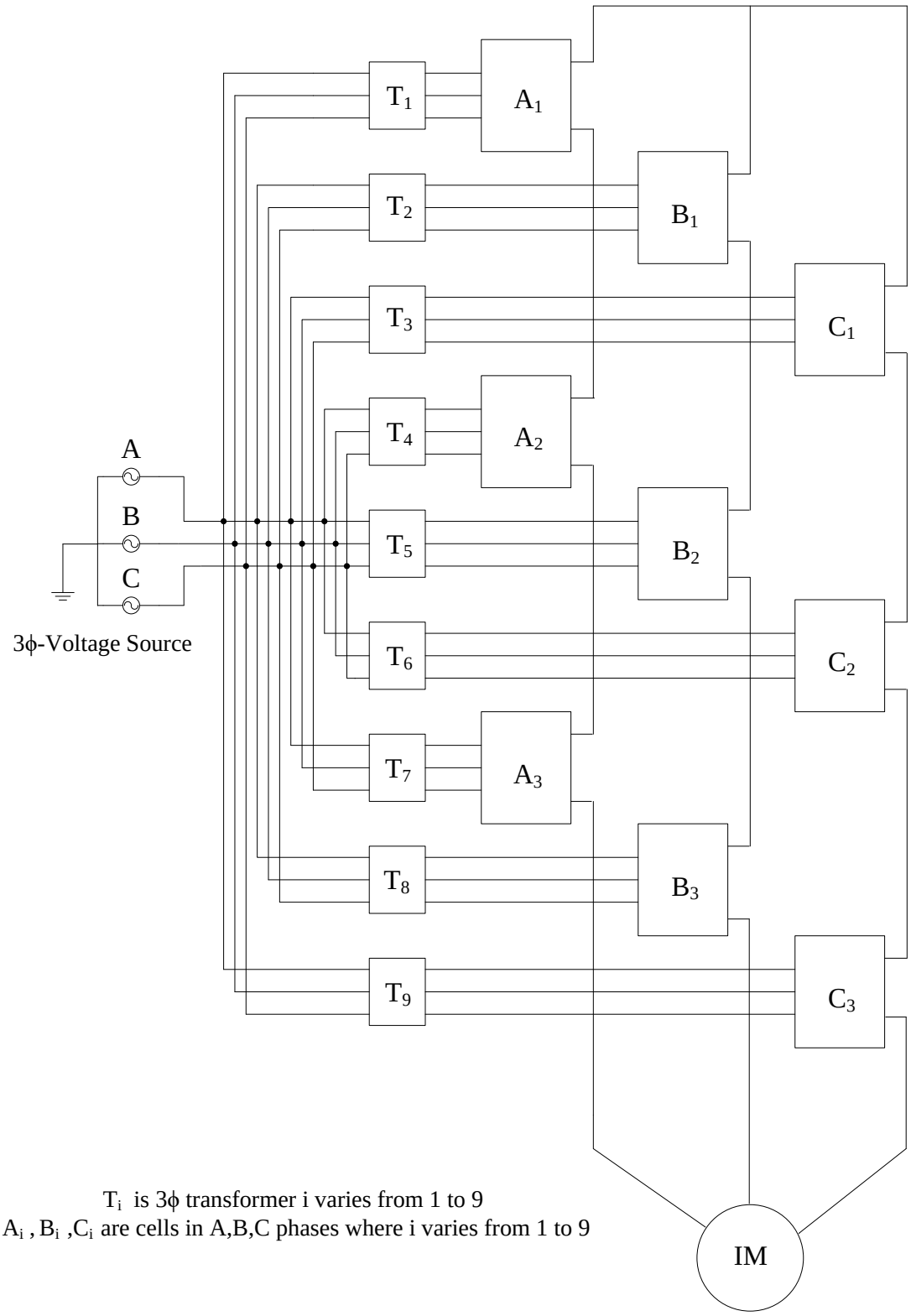

Figure 2.1: Cascaded H-Bridge Multi-level Inverter fed Induction machine

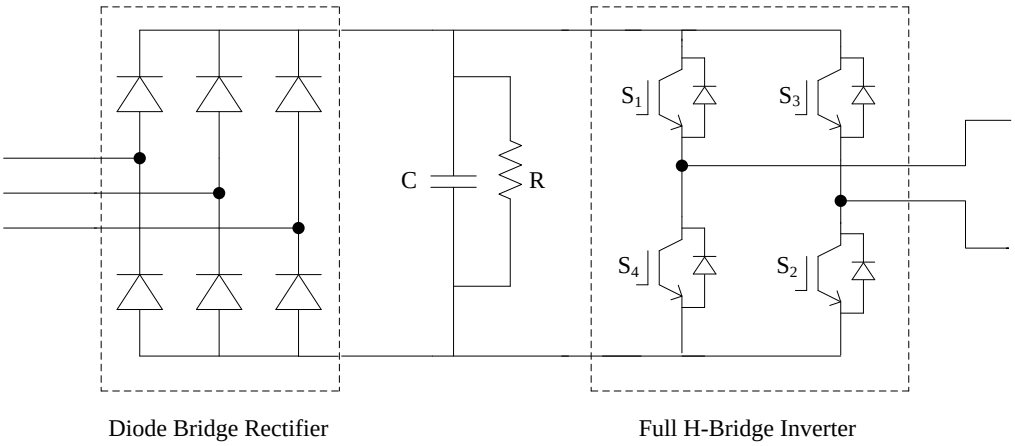

Figure 2.2: Internal Configuration of a Cell Cascaded H-Bridge Inverter

2.2 PWM Techniques

Input currents to the machine are required to be balanced with fixed frequency and amplitude based on the speed requirement. In order to draw these currents, devices should be switched in the appropriate manner so that voltages given to the machine from the inverter contain the required sinusoidal component. But as the inverter cannot generate perfect sinusoidal voltage, it contains some harmonics. This way of controlling the switches and generating voltages is called Sinusoidal Pulse Width Modulation(SPWM). Here, the modulating signal is a sinusoidal wave and the carrier signal is a triangular wave. These two signals are compared and the appropriate switching signal is given to each device.

In conventional VSI, one modulating signal and one carrier signal are used in each phase. So, only two levels are possible. In cascaded H-Bridge multi-level inverter, one or two modulating signals and carrier signals depending on the number cells in the inverter are used. There are two different ways in which carrier signals are generated.

- Level Shifted Carrier Signal Generation.
- Phase Shifted Carrier Signal Generation

2.2.1 Level Shifted Carrier Signal Generation(LSCSG)

Generally, carrier signal is triangular wave with peak to peak voltage is $2V_c$ and average value is zero. Let the number of cells be N, then of levels that are possible $2N+1$.The total number of carrier signals that are required are $2N$.In LSCSG ,amplitude of each carrier signal is scaled down by a value of $2N$ and shifted by a value of $dfrac(2k-1)2NV_c$ where k varies from N to $(-N+1)$.In unipolar SPWM , the number of carrier signals that are required is reduced to N. Here harmonic component is present at the switching frequency f_s.In case of unipolar SPWM , the harmonic component is present at $2f_s$.

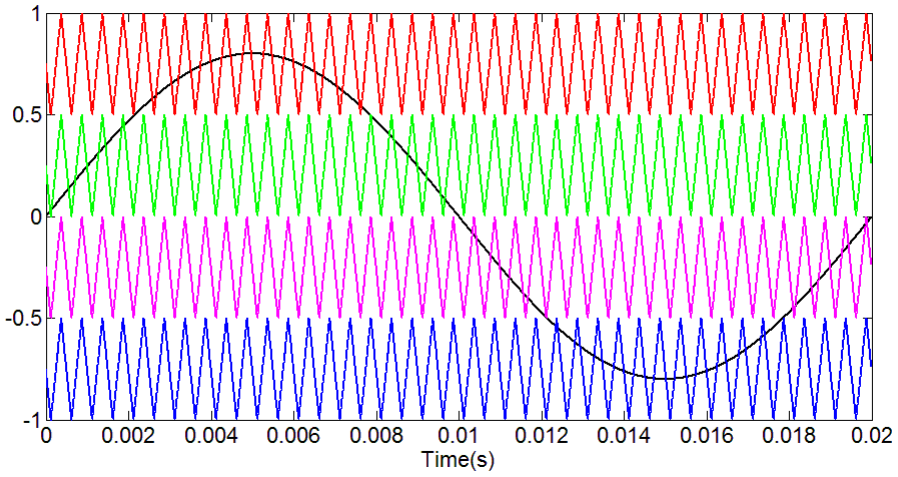

Figure 2.3: Level shifted carrier signals and Modulating signal

2.2.2 Phase Shifted Carrier Signal Generation(PSCSG)

In phase shifted carrier signal generation, the amplitude of the carrier signal is not changed but the phase of the carrier signal is shifted by $\frac{2k\pi}{2N}$ where k varies from 0 to $(2N-1)$. In unipolar SPWM, the number of carrier signals that are required is reduced to N and phase are shifted by an angle $\frac{2k\pi}{2N}$. Here harmonic component is present at $2Nf_s$ where f_s is switching frequency.

Generally, PSCSG with unipolar PWM technique is preferred over LSCSG because the conduction losses are more for pulses generated using LSCSG. In case of PSCSG with unipolar PWM technique, the number of carrier signals is less compared to other methods of carrier signal generation.

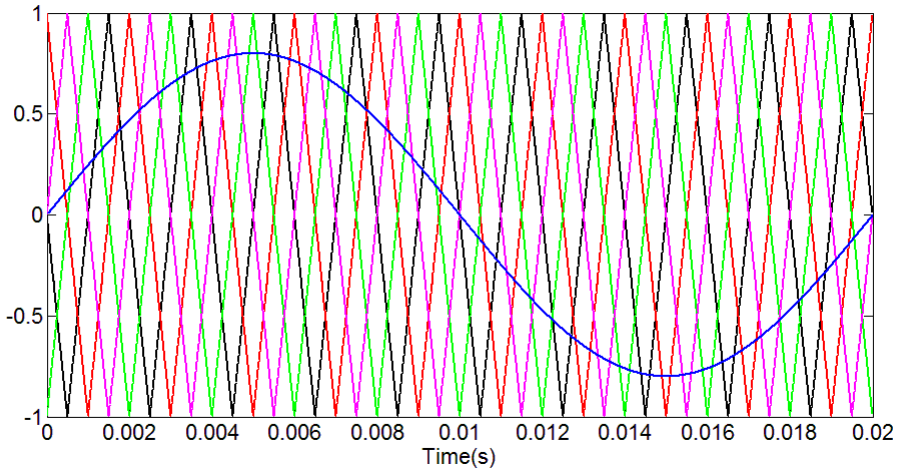

Figure 2.4: Phase shifted carrier signals and Modulating signal

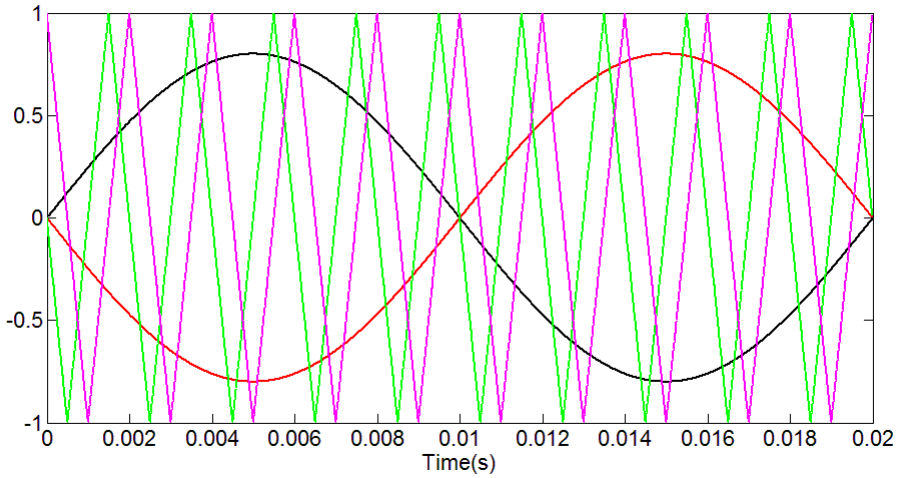

Figure 2.5: Phase shifted carrier signals and Modulating signal in Uni polar SPWM

2.3 Faults in Cascaded H-bridge Multi level Inverter

Semiconductor devices such as MOSFETs and IGBTs are used as switches in multilevel inverters. These devices are temperature dependent. If the temperature of the device exceeds its limit, then the device may break down. This is a case of device fault.

- Open Circuit Fault
- Short Circuit Fault

If a switching pulse is given to the gate of the device, and the device is not

turning on this condition is called open circuit fault. In this case, the switch remains opens in all the conditions. Short Circuit fault is a condition where the device remains turned on in all the conditions regardless of the pulses. Open circuit fault does not serious damages compared to short circuit fault because in case of open circuit fault as the device is not conducting the path for the flow of current is not closed so, current does not flow. But in case of short circuit faults, as the device is always conducting, this affects the devices and elements that are connected in series with the faulty device.

In case of a Multi-level inverter, the number of devices that are being used is very high. So, when a fault is detected all the pulses to all the devices are turned off. One way of rectifying the fault is the traditional way in which faulty device is replaced with a new device. But this method takes a lot of time. Another way is to bypass the faulty device and continue the process. But bypassing the device requires additional circuitry between the adjacent devices which makes the circuit more complex. In case of cascaded H-bridge multi-level inverter, if a device is faulty then the cell which consists of that device is bypassed instead of the device. This bypass operation requires less circuitry compared to circuitry required for bypassing the device.

2.4 Methods of Fault tolerance

After the faulty cell has been by-passed, the number of cells in each phase are not equal. This results in an unbalance in the phase voltages of the inverter. This results in unbalanced line-line voltages. As the machine neutral and inverter neutral are not connected, the only line -line voltages appear across the machine terminals. As the machine voltages are unbalanced it draws unbalanced currents. This results in pulsating torque which is not good for the operation of the machine. If the line -line voltages are balanced, then machine, then machine draws balanced currents and operates normally. In order to get balanced line-line to voltages across the terminals of the inverter, some modifications are done in control strategies of the inverters.

Let N be number of cells in each phase, N_a, N_b, N_c be number of cells which

are not faulty in phases A, B, C respectively in post fault condition, m_a be the modulation index or the amplitude of the modulating signal in pre-fault condition, m_{a1}, m_{a2}, m_{a3} be modulation indices of the modulating signals of the phase A, B, C respectively. Let V_{dc} be the voltage of the capacitor of each cell which remains constant. Let V_a, V_b, V_c be the peak value of the fundamental components of the voltages of Phase A, B, C respectively. Let the rated frequency of the machine be f_r, peak value of the rated phase voltage of the machine be V_p and peak value of the rated line - line voltage of the machine be V_l. Let α, β, γ be the angles between the voltage phasors of phase voltages of the inverter.

2.4.1 Adjustment of Number of Cells in Each Phase (Scheme 1)

In this method, the number of cells in each phase are modified in such a way that the inverter phase voltages are balanced.If

$$N_a = N_b = N_c$$

then phase voltages are balanced and line - line voltages are also balanced.In this condition the bypassing of the cells is not required. If

$$N_a \neq N_b \neq N_c$$

then some cells are bypassed, so that the number cells in each phase are equal. As the number cells in each phase in post-fault condition is less compared to the number of cells in pre-fault condition, the output voltage is reduced. As the speed of machine is controlled by Scalar Control technique, operating speed of machine is reduced because the voltage of the machine is reduced. This method is not preferable because the cells which are healthy are by-passed. Inverter is not operated at it's full capacity.

2.4.2 Adjustment of Amplitudes of the Modulating Signals (Scheme 2)

In this method, the amplitudes of the modulating signals are modified in such away that inverter voltages are balanced. In pre-fault case,

$$V_a = V_b = V_c = N m_a V_{dc}$$

In post fault case,

$$V_a = N_a m_{a1} V_{dc}$$

$$V_b = N_b m_{a2} V_{dc}$$

$$V_c = N_c m_{a3} V_{dc}$$

Voltages in pre-fault case and post-fault case should be equal to get balanced phase voltages. After equating the voltages in pre-fault case and post-fault case, equations are obtained for calculating the modulation indices of the post case are given by

$$m_{a1} = \frac{N}{N_a} m_a \tag{2.1}$$

$$m_{a2} = \frac{N}{N_b} m_a \tag{2.2}$$

$$m_{a3} = \frac{N}{N_c} m_a \tag{2.3}$$

From the *Eqns:(2.1-2.3)*, it is evident that m_{a1}, m_{a2}, m_{a3} are greater than m_a because N_a, N_b, N_c are less than N. In post fault condition, the inverter may operate in operate in over modulation region which is not desirable.As the inverter should not be operated in over modulation region, the range of operating voltage in post fault condition is limited. In scalar control, ratio of peak value of the applied voltage(V) and operating frequency(f) is constant for the values of speed less than the rated speed.

$$k_p = \frac{V_p}{f_r} = \frac{V}{f} \tag{2.4}$$

As voltage is proportional to frequency, the range of operating frequency is also limited. The maximum operating frequency depends on the no of cells present in

each phase in post condition because the phase with less no of cells has more modulation index which evident from the *Eqns:(2.1-2.3)*. Let N_{min} be the minimum value of N_a, N_b, N_c.The maximum operating frequencyf_{max} is given by

$$f_{max} = \frac{0.95 N_{min} V_{dc}}{k} \tag{2.5}$$

In this method, the machine should be operated at lower speeds in the post fault condition as the maximum operating frequency is less than the rated frequency.

2.4.3 Adjustment of Phase Angles of the Modulating Signals (Scheme 3)

In this method, the phase angles of the modulating signals are modified in such a way that the line to line voltages of the machine are balanced.

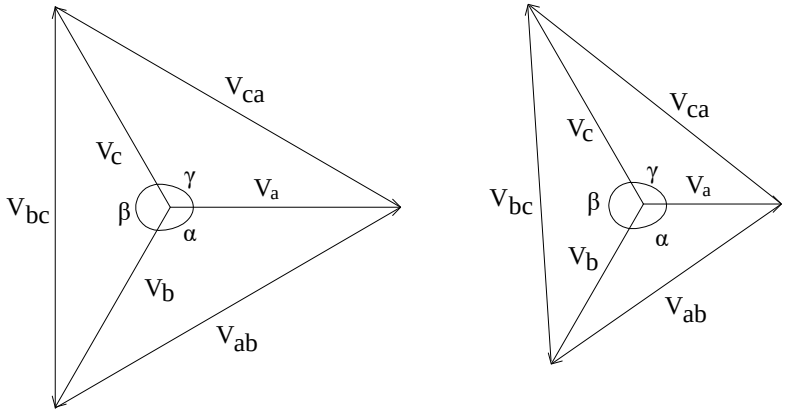

Figure 2.6: Phasor diagram for Pre fault case and post fault case

Voltages of the inverter in pre-fault case and post fault case without any modification of angles are shown in phasor diagram in *Fig:3.7*. In the pre-fault case, amplitudes and phase angles of voltages are given by

$$V_a = V_b = V_c = N m_a V_{dc}$$

$$\alpha = \beta = \gamma = 120^\circ$$

$$V_{ab} = V_{bc} = V_{ca} = V' = \sqrt{3} N m_a V_{dc}$$

In the pre-fault case with out modification of angles, amplitudes and phase angles of voltages are given by

$$V_a = N_a m_a V_{dc}$$

$$V_b = N_b m_a V_{dc}$$

$$V_c = N_c m_a V_{dc}$$

$$\alpha \neq \beta \neq \gamma \neq 120^\circ$$

$$V_{ab} \neq V_{bc} \neq V_{ca}$$

The angles are modified in such way that the line -line voltages are balanced. The modified phasor diagram is shown in the *Fig:3.8*

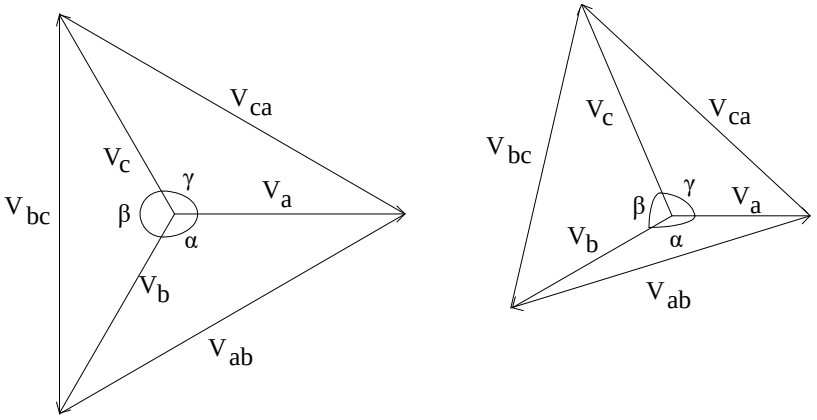

Figure 2.7: Phasor Diagram for pre-fault case and modified post-fault case

In the modified post fault case,

$$V_a = N_a m_a V_{dc}$$

$$V_b = N_b m_a V_{dc}$$

$$V_c = N_c m_a V_{dc}$$

$$\alpha \neq \beta \neq \gamma \neq 120^\circ$$

$$V_{ab} = V_{bc} = V_{ca} = V''$$

The angles and the line-line voltage in modified post fault case are calculated by the equations

$$V''^2 = V_a^2 + V_b^2 - 2V_a V_b \cos\alpha \tag{2.6}$$

$$V''^2 = V_b^2 + V_c^2 - 2V_bV_c\cos\beta \tag{2.7}$$

$$V''^2 = V_c^2 + V_a^2 - 2V_cV_a\cos\gamma \tag{2.8}$$

$$\alpha + \beta + \gamma = 360^\circ \tag{2.9}$$

As the equations are simultaneous non linear equations, numerical methods are used to solve these equations. In this method, in the post fault condition line-line voltage is less compared to pre fault condition. As the line-line voltage is reduced, the operating frequency is also reduced which given by the equation

$$f' = \frac{V''}{\sqrt{3}k} \tag{2.10}$$

2.4.4 Adjustment of Amplitudes and Phase angles of the Modulating signals (Scheme 4)

This method is combination of both the discussed above subsection. In this methods both angles and modulation indices are modified are in such way that the line-line voltage in the pre-fault case and the post fault case are balanced and equal. In this method the modulation index of the modulating signal in the pre-fault case (m_a) is change to other modulation index (m'_a).

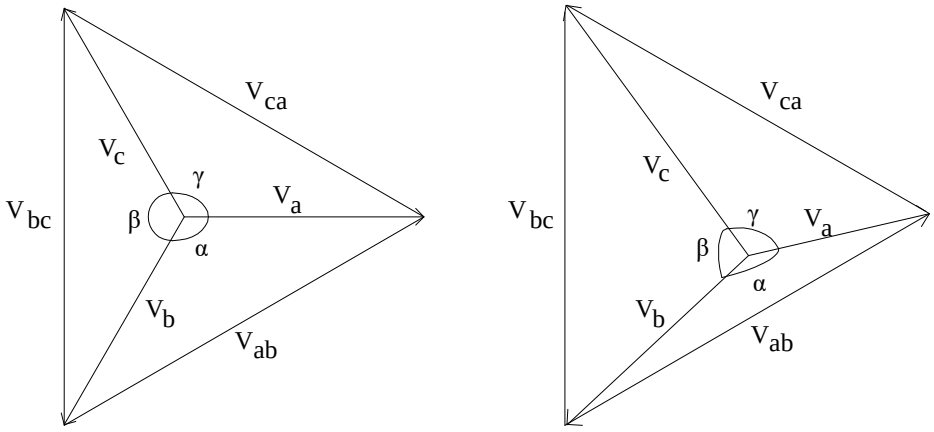

Figure 2.8: Phasor diagram for Pre fault case and modified post fault case

The phasor diagram is *Fig:3.9* describes the line-line voltages in pre-fault and post-fault condition with modification.

$$V_a = V_b = V_c = Nm_aV_{dc}$$

$$\alpha = \beta = \gamma = 120^\circ$$

$$V_{ab} = V_{bc} = V_{ca} = V' = \sqrt{3} N m_a V_{dc}$$

In the modified post fault case

$$V_a = N_a m'_a V_{dc}$$

$$V_b = N_b m'_a V_{dc}$$

$$V_c = N_c m'_a V_{dc}$$

$$\alpha \neq \beta \neq \gamma \neq 120^\circ$$

$$V_{ab} = V_{bc} = V_{ca} = V' = \sqrt{3} N m_a V_{dc}$$

The equations required to get the values of angles and new modulation index(m'_a) are

$$\cos\alpha = \frac{N_a^2 + N_b^2 - (\sqrt{3}XN)^2}{2N_a N_b} \tag{2.11}$$

$$\cos\beta = \frac{N_b^2 + N_c^2 - (\sqrt{3}XN)^2}{2N_b N_c} \tag{2.12}$$

$$\cos\gamma = \frac{N_c^2 + N_a^2 - (\sqrt{3}XN)^2}{2N_c N_a} \tag{2.13}$$

$$\alpha + \beta + \gamma = 360^\circ \tag{2.14}$$

where

$$X = \frac{m_a}{m'_a}$$

The equations are simultaneous non linear equations.So, numerical methods are required to solve these equations. On solving these equations it is observed that (m'_a) is greater than (m_a). It is important to restrict the value of (m'_a) so that the inverter may not operate in the over modulation region. In that condition the the value of (m_a) should be reduced in such way that the value of (m_a) is 0.95. This can be done by changing the frequency command in the drive. The maximum frequency upto which the inverter is operated so that it does not enter

over modulation region is given by

$$f_{max} = \frac{0.95XNV_{dc}}{k} \tag{2.15}$$

If the operating frequency (f) in the pre-fault case is greater than the maximum frequency ($f_{max)}$) that is calculated then the frequency reference should be changed to the maximum frequency (f_{max}) else it not required. This ensures that inverter does not operate in over modulation region. The values of ($f_{max)}$) are calculated for different cell configurations in post-fault case and stored in look-up table.

The angles which are calculated using equations *Eqns:(2.11-2.14)* are the angles between the phasors. Let the phase angles be δ_1, δ_2, δ_3.

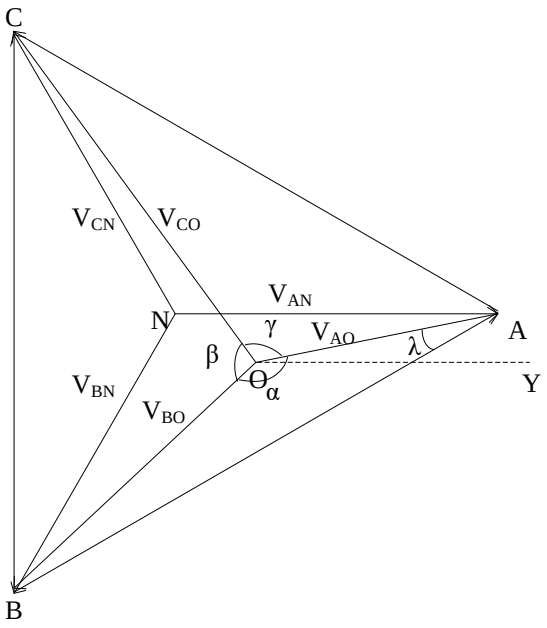

Figure 2.9: Phasor diagram with inverter voltages and machine voltages

In the phasor diagram shown in *Fig:10*, the inverter neutral point is shown as O and machine neutral point as N. Let AN, BN, CN be the phasors for phase voltages of the machine and AO, BO, CO be the phasors for the phase voltages of the inverter. From the phasor diagram,

$$\angle AOY = \delta_1$$

$$\angle BOY = \delta_2$$

$$\angle COY = \delta_3$$

$$\angle OAC = \lambda$$

By applying properties of triangles and properties of angles the values of δ_1, δ_2, δ_3 are calculated in terms of α, β, γ and λ.

$$\delta_1 = 30^\circ - \lambda \tag{2.16}$$

$$\delta_2 = 30^\circ - \lambda + \gamma \tag{2.17}$$

$$\delta_3 = 30^\circ - \lambda + \gamma + \beta \tag{2.18}$$

where λ is calculated using the equation

$$\cos\lambda = \frac{N_a^2 + (\sqrt{3}XN)^2 - N_b^2}{2\sqrt{3}XNN_a} \tag{2.19}$$

Let v_a, v_b, v_c be instantaneous values of the modulating signals given to the inverter, $v_{s\alpha}$,$v_{s\alpha}$ be the values obtained from the $(\alpha\beta 0 - abc)$ transformation.The instantaneous values of v_a, v_b, v_c are calculated for the pre-fault and post-fault case are given by

$$v_a = \frac{2}{3X}(v_{s\alpha}\cos\delta_1 - v_{s\beta}\sin\delta_1) \tag{2.20}$$

$$v_b = \frac{2}{3X}(v_{s\alpha}\cos\delta_2 - v_{s\beta}\sin\delta_2) \tag{2.21}$$

$$v_c = \frac{2}{3X}(v_{s\alpha}\cos\delta_3 - v_{s\beta}\sin\delta_3) \tag{2.22}$$

These equations can be used in pre-fault and post-fault case. In pre-fault condition

$$\delta_1 = 0^\circ$$

$$\delta_2 = -120^\circ$$

$$\delta_2 = 120^\circ$$

$$X = 1$$

In post-fault condition, the values of δ_1, δ_2, δ_3 and X are calculated using equations *Eqns:(2.11-2.14)* and *Eqns:(2.16-2.19)*. The calculation of phase angles and ratio of modulation indices requires a lot of computations which cannot be performed

while changing from pre-fault case to post-fault case. So, the values of sine and cosine of phase angles and ratio of modulation indices are calculated and stored in lookup table for different fault conditions.Scheme 4 is considered as a better choice among all the four schemes because the decrement in the line -line voltage from pre-fault condition to post-fault condition is minimum.

2.5 Detection of a faulty cell

Device faults are detected using a gate driver.Gate driver is a component which acts as an interface between the controller from which generates the pulses and the semiconductor device. The gate driver circuit has an inherent fault protection circuit. If a device is faulty, the gate driver generates a signal which is used for the detection of the faults of the device. This signal is called Gate Error Signal. This signal is used in the protection algorithm.

Generally, the gate error signal is low when the device fault is present and high when the device fault is absent or vice-versa. The gate drivers that are used in all cells are identical, the convention remains same for all the cells. All the gate error signals in each cell are combined by an appropriative logical operation to get a single signal. This signal is referred as a fault signal of a cell. This signal is used to detect the presence of fault in a cell.

2.6 By-pass operation of a faulty cell

The faulty cell should be isolated from the inverter. Additional circuitry is included into the cell for bypassing the cell. The internal configuration of the cell is modified for this purpose.

In order to bypass the cell, it is necessary to isolate the cell electrically. Two electro-mechanical switches are included into the cell to isolate the cell from its input side and the output side. A by-pass switch is connected in between the two output terminals of the cell. These two electro-mechanical switches are relay operated circuit breakers and a by-pass switch is a semiconductor device. If the

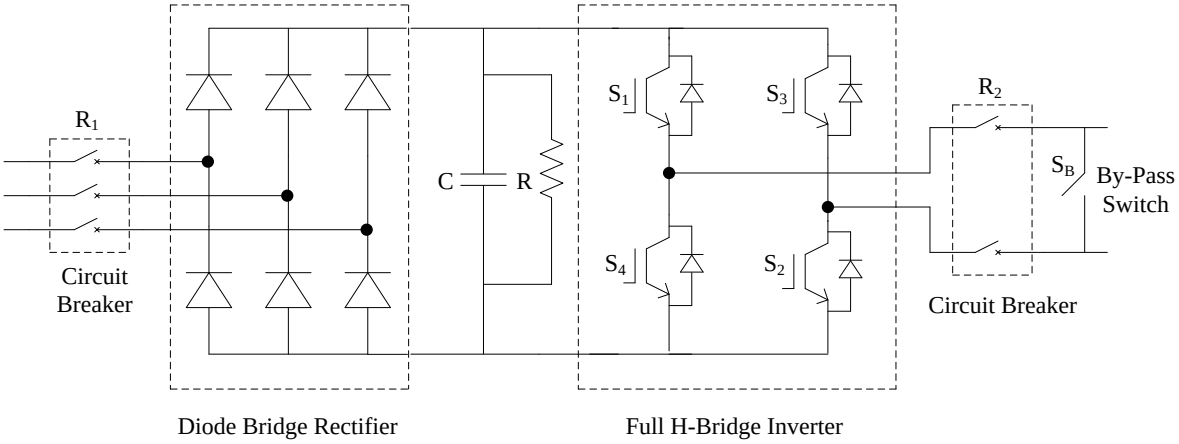

Figure 2.10: Modified Internal Configuration of Cell

cell is not faulty then two circuit breakers remain closed and bypass switch remains open. If the cell is faulty then the two circuit breakers are opened. As electro-mechanical switches are slower compared to semiconductor devices, they take some time to open. Generally, the time taken by the circuit breakers to open is in terms of milliseconds. Once they are opened completely, the bypass switch is closed and the faulty cell is isolated. While the bypass operation is being carried out the pulses to the faulty cell should be disabled so, that the capacitor and other components are not affected. Otherwise, when the bypass switch is closed, the capacitor may get short-circuited and cause serious damage to the converter. So, it is advisable to disable all the pulses to the inverter during the bypass operation.

2.7 Implementation of fault tolerance algorithm in a VVVF drive

2.7.1 VVVF control of induction machine

Variable Voltage Variable Frequency(VVVF) control is also called as scalar control of induction machine or Constant Flux control. This is based on steady state model of the induction machine.

The above diagram is steady state circuit diagram of the single phase of an induction machine. All quantities are per phase quantities. V_s is the rated voltage given as input voltage. V_m is the voltage across the magnetizing inductance(L_m).

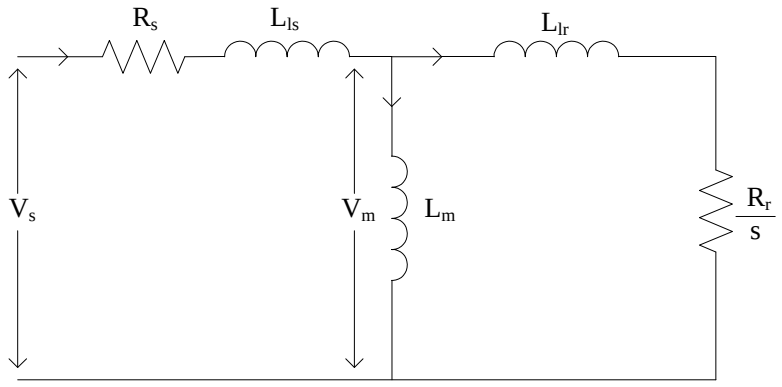

Figure 2.11: Steady State Model of Induction machine

At the rated voltage conditions V_m is approximately equal to V_s neglecting drop across stator leakage inductance(L_{ls}) and stator winding resistance(R_s). Now ratio $\frac{V_s}{f_s}$ is the amplitude of air gap flux of the induction machine. Here V_s and f_s are varied in such way that ratio of V_s and f_s remains constant and the values are increased up to the rated values. As flux remains constant, it is called Constant Flux Control.

At the time starting when V_s is very small, the resistance and leakage reactance voltage drop cannot be neglected. The applied voltage appears across the stator resistance and V_m is almost equal to zero. As V_m is almost equal to zero flux is zero, so the machine does not move. To develop the flux in the machine should be operated with some voltage at zero frequency and after some time both V_s and f_s can be varied till the rated values. This is called slow start.

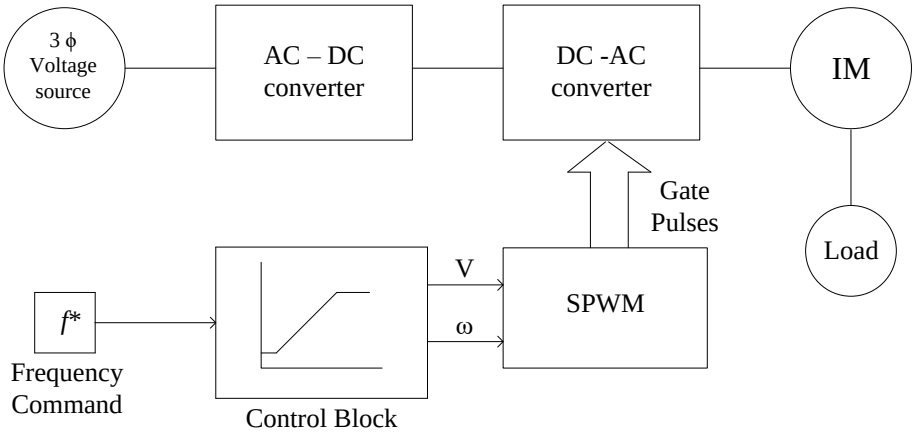

Figure 2.12: Block Diagram for Scalar Control

$f^\star$ is the frequency command that is given to control block .Control block is look up table which voltage and frequency are estimated and they are given to the

sinusoidal PWM block which generates pulses for the inverter.

2.7.2 Implementation of fault tolerance algorithm

The fault signals of the inverter are used to detect a faulty cell in the inverter. These fault signals are given as an input to the frequency command block and fault rectification block as shown in the *Fig:2.13*.

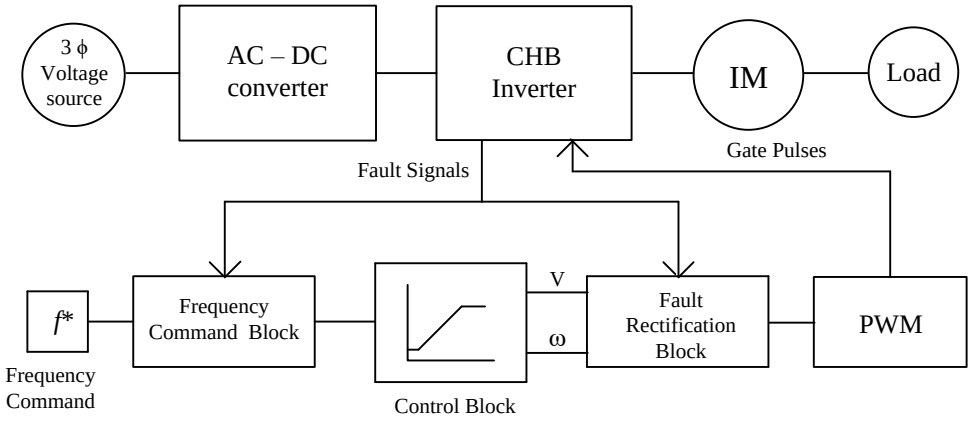

Figure 2.13: Block Diagram of VVVF drive with fault tolerance algorithm

The frequency command block gives the frequency at which the converter should operate. The internal configuration of the block is as shown in the *Fig:2.14*.

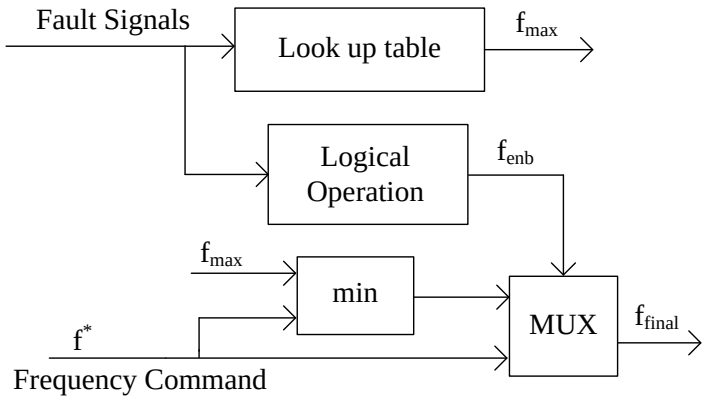

Figure 2.14: Frequency command block

In frequency command block, all the fault signals are combined to a single signal which detects the fault.This signal is a fault enable signal (f_{enb}).If f_{enb} is high then a fault is present else fault is not present. If a fault is present, then the frequency at which the converter should operate depends on the cell configuration in post-fault case. The maximum frequency at which the converter can operate is

obtained from the look-up table. The look-up table has all the values of maximum frequencies for all possible cell configurations with the fault condition. f_{final} is the output of the frequency command block.

$S.No$	f_{enb}	f_{final}
1	low	$f^{\star}$
2	$high$	$min(f_{max}, f^{\star})$

In fault rectification block, the amplitude (V) and frequency (ω) are given as inputs to the sine wave generator which generates three balanced sinusoidal signals v_{sa}, v_{sb}, v_{sc}. The three modulating signals are given to a ($abc-\alpha\beta0$) transformation block which generates $v_{s\alpha}$, $v_{s\beta}$. The fault signals give the information about the presence of fault and cell configuration in the presence of fault. The phase angles δ_1, δ_2, δ_3 and X are obtained by the look-up table. The look-up table consists of all the values of δ_1, δ_2, δ_3 and X for all the possible cell configuration. The modified modulating signals are generated using the *Eqns:(2.20-2.22)*. These signals are given to the PWM block from pulses are generated and given to the inverter.

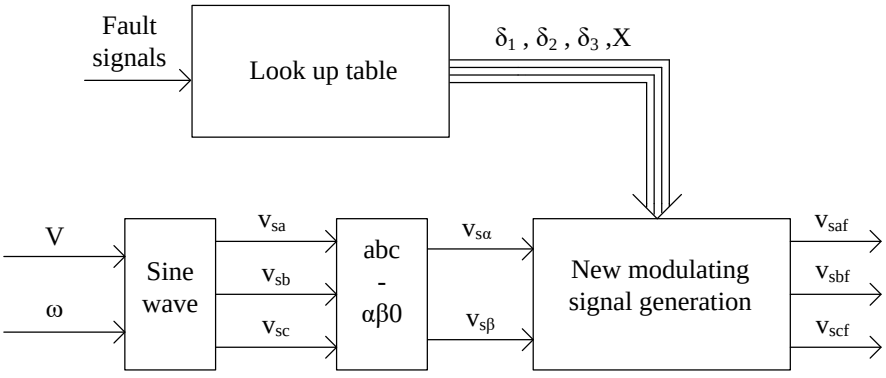

Figure 2.15: Fault rectification block

When a cell is detected as a faulty one in the inverter, all the pulses to the inverter are disabled. The faulty cell is bypassed. The by-pass operation takes some considerable amount of time because the circuit breakers take some time to open completely. Generally, the time constants of the circuit breakers are in terms of tens of milliseconds. During this time the pulses to the inverter are disabled and stator currents decay to zero within a half cycle. Flux starts decaying with rotor time constant and the machine starts decelerating. When the cell is by-passed, the flux may not be decayed to zero completely. If it not decayed to zero completely,

then some back emf is present on the stator terminals. In order to apply voltages from the inverter, position of the flux angle is required. The applied voltage should be in phase with the back emf of the stator so that large currents are not drawn which can damage the converter. In VVVF drive the angle of the flux cannot be estimated. In order to apply the voltages, the flux should completely decay to zero. During that time speed also decreases and when voltages are applied to the machine, the machine takes a considerable amount of time to attain the required speed. As the time has taken is large, the speed of the machine may come to zero if it is loaded. So, in order to achieve a smooth transition from pre-fault condition to post-fault condition without a considerable amount of decrement in speed, the information of the position of the flux angle is necessary. This problem can be solved in a vector controlled drive where the position of the flux angle can be estimated.

2.8 Implementation of fault tolerance algorithm in a vector control drive

2.8.1 Vector control of induction machine

The position of the flux angle is not known or cannot be estimated using steady state model of induction machine. It is possible in vector control. Vector control is also called as Field Oriented Control (FOC). This is based on the dynamic model of induction machine. In vector control technique, the stator currents are divided into two orthogonal components. They are flux producing component and torque producing components. As these two components are decoupled, they can be controlled independently just like in the case of a DC machine.

In dynamic model of induction machine, stator voltages and stator currents in natural reference frame are converted into rotor flux reference frame. The equations in rotor flux reference frame are given by

$$v_{sd} = i_{sd}R_s + \sigma L_s \frac{di_{sd}}{dt} - \sigma L_s \omega_s i_{sq} + (1-\sigma) L_m \frac{di_{mr}}{dt} \tag{2.23}$$

$$v_{sq} = i_{sq}R_s + \sigma L_s \frac{di_{sq}}{dt} + \sigma L_s \omega_s i_{sd} + (1-\sigma)\omega_s L_s i_{mr} \tag{2.24}$$

$$\tau_r \frac{di_{mr}}{dt} + i_{mr} = i_{sd} \tag{2.25}$$

$$\omega_s = \frac{d\rho}{dt} = \omega + \omega_{slip} = \omega + \frac{i_{sq}}{\tau_r i_{mr}} \tag{2.26}$$

$$J\frac{d\omega_m}{dt} + B\omega_m = K_t i_{mr} i_{sq} - M_l \tag{2.27}$$

$$\omega = \frac{P\omega_m}{2} \tag{2.28}$$

where $\sigma = 1 - \frac{L_m^2}{L_s L_r}$, $\tau_r = \frac{L_r}{R_r}$, $K_t = \frac{2PL_m}{6}$.

All the voltages and currents in rotor flux frame of reference are considered as DC quantities. So, traditional control techniques can be used in control algorithms. Speed controller, flux controller and two current controllers are Proportional Integral Controller (PI). Flux controller and speed controller generate i_{sdref} and i_{sqref} respectively. Two current controllers take i_{sdref} and i_{sqref} as the reference values and generate v_{sdref} and v_{sqref}. v_{ffd} and v_{ffq} are the feed forward terms which are added to v_{sdref} and v_{sqref} respectively to improve the dynamic response of the d-axis current i_{sd} and q-axis current i_{sq} respectively.After the addition of v_{ffd} and v_{ffq} to v_{sdref} and v_{sqref} respectively, the summation terms are given to $(dq0 - abc)$ transformation block which transforms stator voltages in rotor flux frame of reference $(dq0)$ to natural frame of reference (abc). These signals are to the PWM block which generates pulses and are given to the inverter. The PI controllers are designed by selecting appropriate bandwidths for the two current controllers, flux controller and speed controller.

The line currents are sensed and transformed into rotor flux reference frame using $(abc - dq0)$ transformation. A speed sensor or an encoder is used to sense of the rotor ω_m. i_{sd}, i_{sq}, ω_m are used to estimate the flux angle ρ which used in $(abc - dq0)$ and $(dq0 - abc)$ transformation.This is called as Sensored vector control.Generally, encoder requires additional circuitry and it is very expensive. The method in which the speed sensor is not used is called Sensorless-vector control.In sensor-less vector control, angle of the flux is estimated using line currents and DC bus voltage.

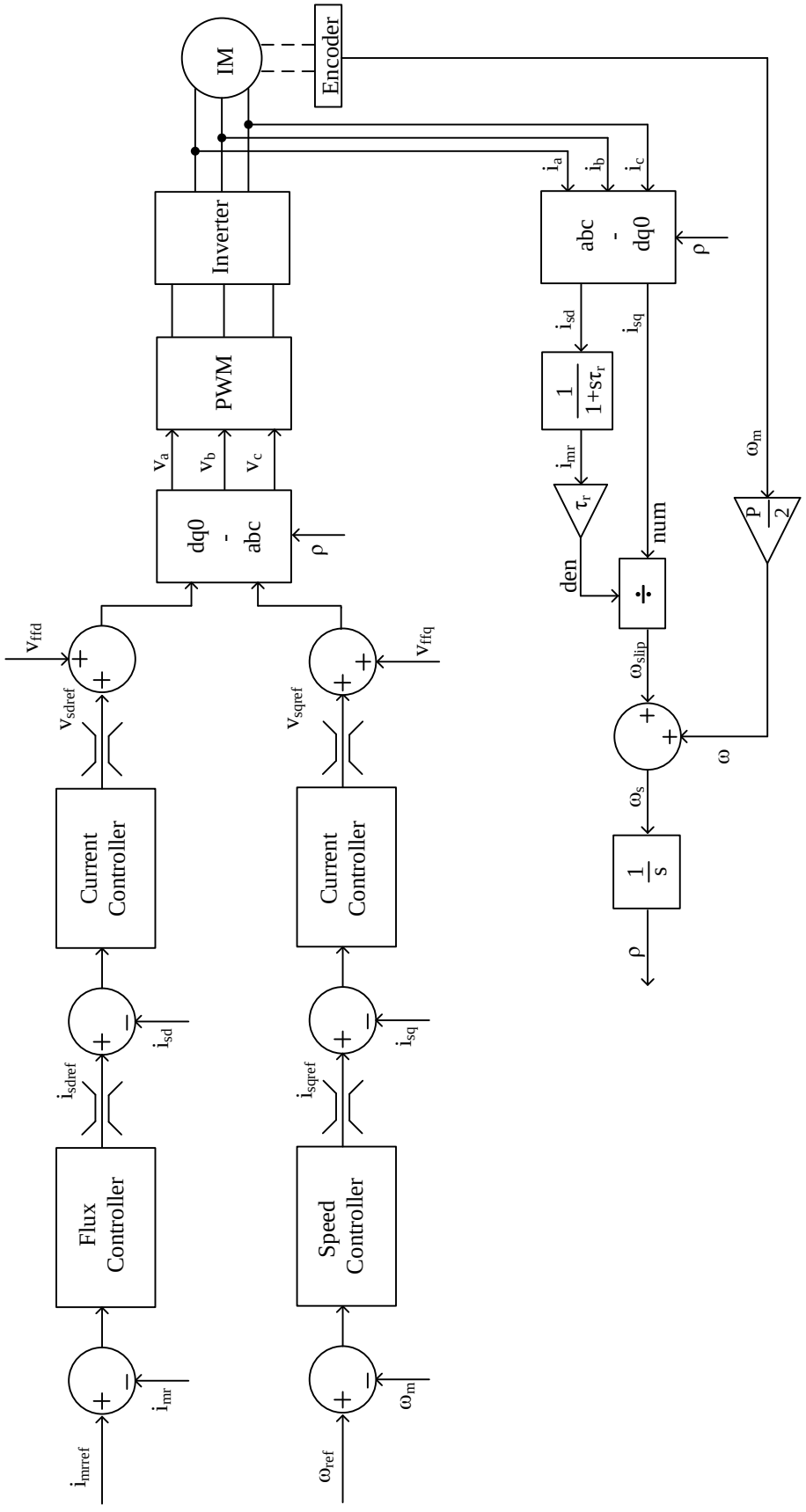

Figure 2.16: Block diagram for Vector Control

2.8.2 Calculation of maximum speed (ω_{max})

As discussed in Scheme(4) in (*section* : 2.4), the inverter is allowed to operate only in certain range of speeds or frequency in faulted condition so that the inverter does not operate in operate in over-modulation region. In VVVF drive, it is achieved by adjusting the frequency based on the cell configuration in fault condition. In vector control drive, it is done by adjusting the speed. In order to adjust the speed, maximum speed for different cell configurations in fault condition is required.

The machine equations in rotor flux frame of reference in steady state are given by

$$v_{sd} = i_{sd}R_s + \sigma L_s \omega_s i_{sq} \tag{2.29}$$

$$v_{sq} = i_{sq}R_s + \sigma L_s \omega_s i_{sd} + (1-\sigma)\omega_s L_s i_{mr} \tag{2.30}$$

$$i_{mr} = i_{sd} \tag{2.31}$$

$$\omega_s = \omega + \omega_{slip} = \omega + \frac{i_{sq}}{\tau_r i_{mr}} \tag{2.32}$$

$$B\omega_m = K_t i_{mr} i_{sq} - M_l \tag{2.33}$$

$$M_l = k\omega_m \tag{2.34}$$

where $k = \frac{T_{rated}}{\omega_{rated}}$ and load is considered as a generator type load. In steady state, $v_{sd} = V_{sd}, v_{sq} = V_{sq}, i_{mr} = i_{sd} = I_{mr}, i_{sq} = I_{sq}$. Using $(abc - dq0)$ transformation,

$$\sqrt{V_{sd}^2 + V_{sq}^2} = \frac{3}{2} m_a N V_{dc} \tag{2.35}$$

The maximum modulation index in post fault case is 0.95. So,

$$m_a = 0.95X \tag{2.36}$$

Substituting the *Eqns:(2.29-2.34)* and *Eqns:(2.36)* in *Eqn: 2.35* the obtained quadratic equation is given by,

$$a_1 I_{sq}^4 + a_2 I_{sq}^2 + a_3 = 0 \tag{2.37}$$

where

$$a_1 = \sigma L_s k_1$$

$$a_2 = -(2R_s L_s I_{mr} \sigma k_2) + (R_s + L_s I_{mr} k_2)^2$$

$$a_3 = (R_s I_{mr})^2 - (\frac{8.55XNV_{dc}}{16})^2$$

$$k_1 = \frac{P}{2}k_2 + \frac{1}{\tau_r Imr}$$

$$k_2 = \frac{K_t I_{mr}}{B + k}$$

After solving the quadratic equation in *Eqn:2.37*, the positive value of is chosen I_{sq} is chosen.The maximum speed ω_{max} is given by

$$\omega_{max} = \frac{K_t I_{mr} I_{sq}}{B + k} \tag{2.38}$$

The maximum speed is calculated for different cell configurations in fault condition and stored in a lookup table.

2.8.3 Implementation of fault tolerance algorithm

The faulty cell is detected by the information of the fault signals from the CHB inverter. These signals are used in speed command block shown in the *Fig:2.17* to give appropriate speed reference (ω_{final}) so, that the inverter does not operate in over modulation region.

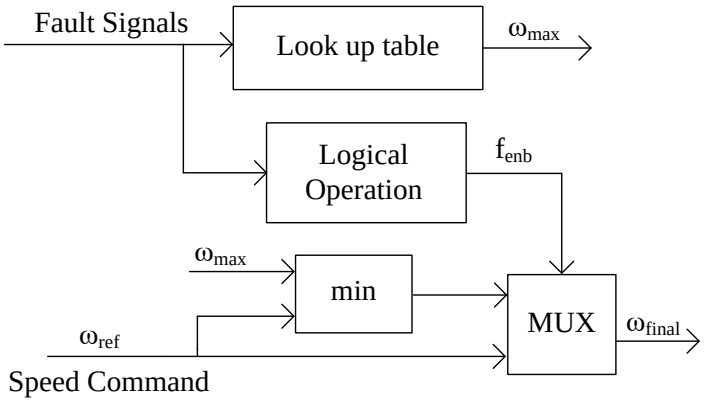

Figure 2.17: Speed command block

In Speed Command Block, all fault signals are combined to a single signal f_{enb}

which is used to detect the fault. If f_{enb} is high then fault is present else fault is absent. Thhe maximum value of the allowable speed is obtained from the lookup table. If the fault is present,speed reference in the pre fault condition (ω_{ref}) is compared with the maximum speed (ω_{max}) and the minimum value is taken as ω_{final}. If the fault is not present, ω_{ref} is taken as ω_{final}. ω_{final} is given as the final speed reference to the speed controller.

$S.No$	f_{enb}	ω_{final}
1	low	ω_{ref}
2	$high$	$min(\omega_{max}, \omega_{ref})$

$(dq0 - abc)$ transformation block shown in the *Fig:2.16* contains two blocks. First block transforms voltages from rotor flux frame of reference $(dq0)$ to stationary frame of reference $(\alpha\beta0)$ and second block transforms voltages from stationary frame of reference $(\alpha\beta0)$ to natural frame of reference (abc). In fault tolerant algorithm, the $(dq0 - abc)$ transformation block transformation block is modified. v_{sd} and v_{sq} are transformed to $v_{s\alpha}$ and $v_{s\beta}$. The fault signals give the information about the presence of fault and cell configuration in the presence of fault. The phase angles δ_1, δ_2, δ_3 and X are obtained by the look-up table. The look-up table consists of all the values of δ_1, δ_2, δ_3 and X for all the possible cell configuration. The modified modulating signals are generated using the *Eqns:(2.20-2.22)*. These signals are given to the PWM block from which pulses are generated and given to the inverter.

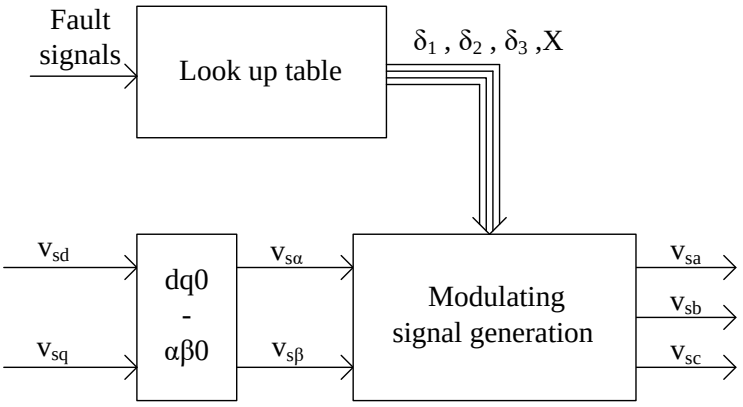

Figure 2.18: Modified $(dq0 - abc)$ transformation block

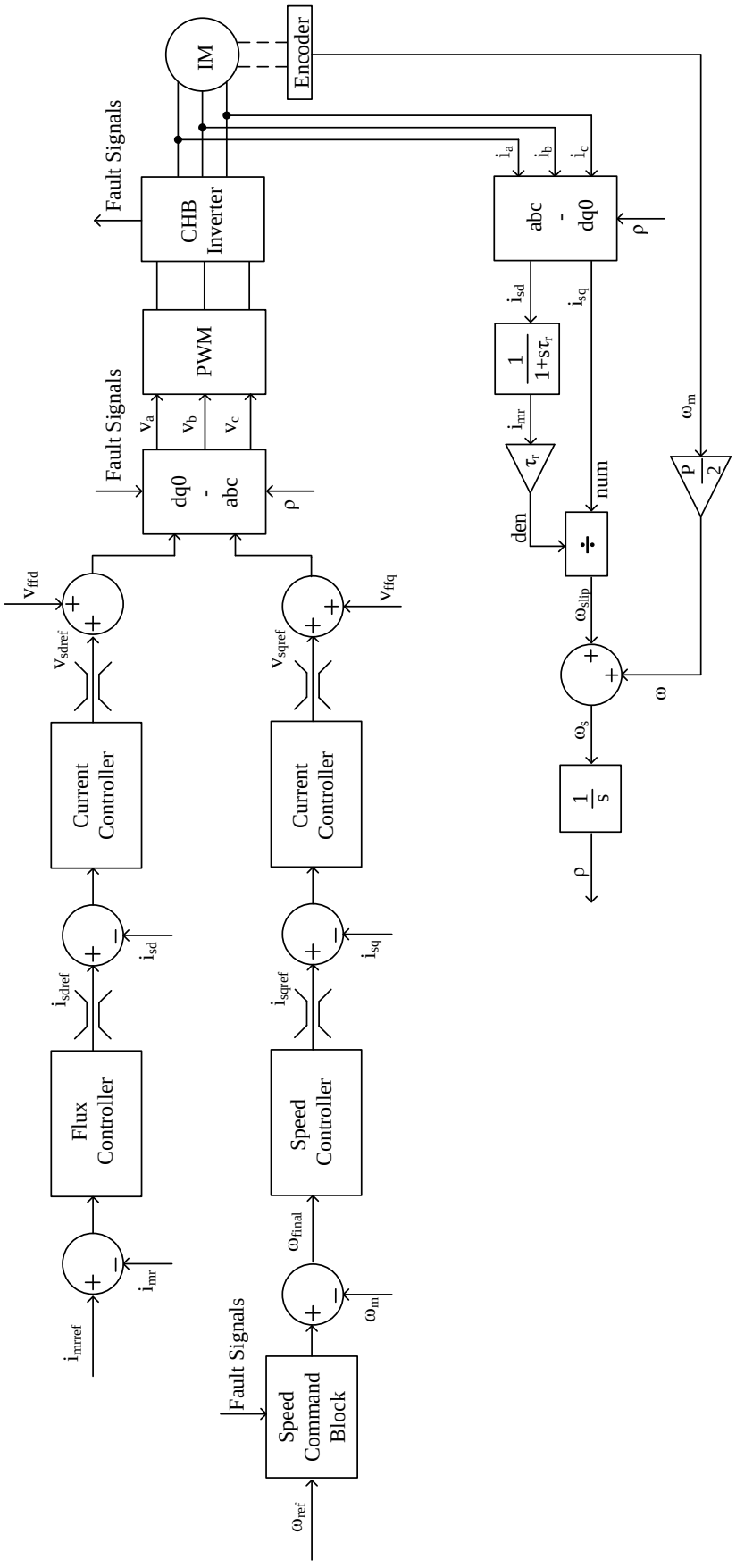

Figure 2.19: Block diagram for Vector Control drive with fault tolerance algorithm

When a cell is detected as faulty one, pulses to the inverter are disabled. Then the cell is by-passed. During the by-operation, the angles and speed reference to the speed controller are changed based on the cell configuration in post fault condition. Once the cell is by-passed, all the PI controllers are reset. Then, the pulses are given to the inverter. The sequential steps that are involved in bypassing the cell in vector control drive are explained in the flow chart in *2.20*.

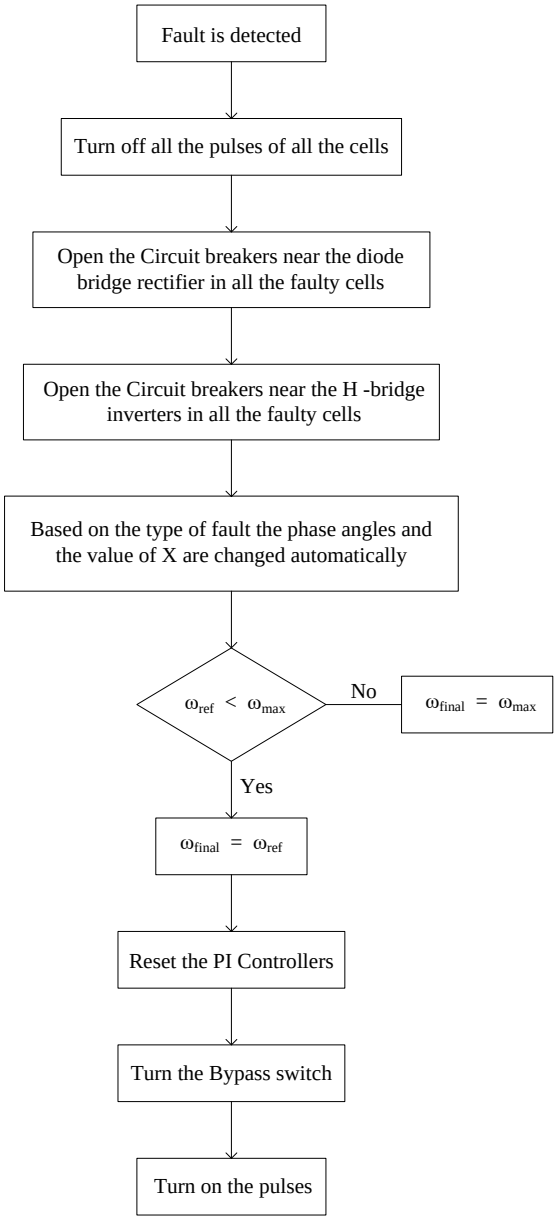

Figure 2.20: Flow chart for the fault tolerance algorithm in vector control drive

During the transition period from pre-fault to post-fault condition, the flux decays with rotor time constant until the pulses are enabled. The transition period is determined by the time constant of the circuit breaker which are generally in terms of milliseconds. During that time the speed also decreases but as the time is

small the decrement in the speed is less because of high mechanical time constant of the machine. In sensored vector control, position of rotor flux angle is estimated. When the pulses are given back to the inverter, the problem of phase mismatch between the applied voltage and back emf is resolved.As dynamic performance of vector control drive is better than VVVF drive, the required speed in post fault condition is achieved in faster in vector control drive than in VVVF drive. In sensor less vector control, the angle estimation is difficult because the data of the speed is not available and currents are decayed to zero. In sensor less vector control, this problem may be resolved by placing voltage sensors across the machine terminals to get voltages so that the rotor flux angle can be estimated.

2.9 Conclusion

This chapter has outlined different control schemes of overcoming the faults in CHB inverter. Methods of detection of a faulty cell and by-pass operation of a faulty cell are presented. A fault tolerance algorithm is discussed for a vector control drive is presented. The hardware organisation will be discussed in the next chapter.

CHAPTER 3

Hardware Organisation for Fault tolerant Cascaded H Bridge Inverter fed Induction motor drive

3.1 Introduction

In this chapter, hardware organisation of a fault tolerant cascaded H bridge inverter fed induction motor drive is explained. A brief discussion on DSP - FPGA based hybrid board, Protection and Delay card ,external boards and sensor boards is given.

3.2 Cascaded H bridge inverter

A 7 level cascaded H bridge inverter is developed to study the and implement the studies of faults in the converter. CHB inverter has three cell in each phase and total number of cells present is 9. Each cell is made of two SEMIKRON half bridge IGBT modules with a rating of 1200V 100A, a SEMIKRON three phase diode bridge rectifier module with rating of 1600V 80A and capacitor of 4700 μF. The IGBT modules and the diode bridge rectifier are placed on the heat sink. The heat dissipated by the devices due to losses is conducted by the heat sink to the ambient. Breeder resistor is connected in parallel to the capacitor. This is responsible for discharging of the capacitor after the power is turned off. The capacitor is charge through a diode bride rectifier. The input to the diode bridge rectifier is given through a step down transformer. The ratings of the transformer are given in the table *Table: 3:1.* As there are nine cells, nine step - down transformers are required. A 3 ϕ transformer which is used in setup is shown in the *Figure :3.1*

Table 3.1: Step-down Transformer specifications

S.No	Parameter	Value
1	Power	1.5 KVA
2	Primary side voltage	440 V
3	Secondary side voltage	65 V / 107 V
4	Primary side current	2 A
5	Secondary side current	13.3 A / 8.09 A
6	Primary side connection	Star connected
7	Primary side connection	Star connected

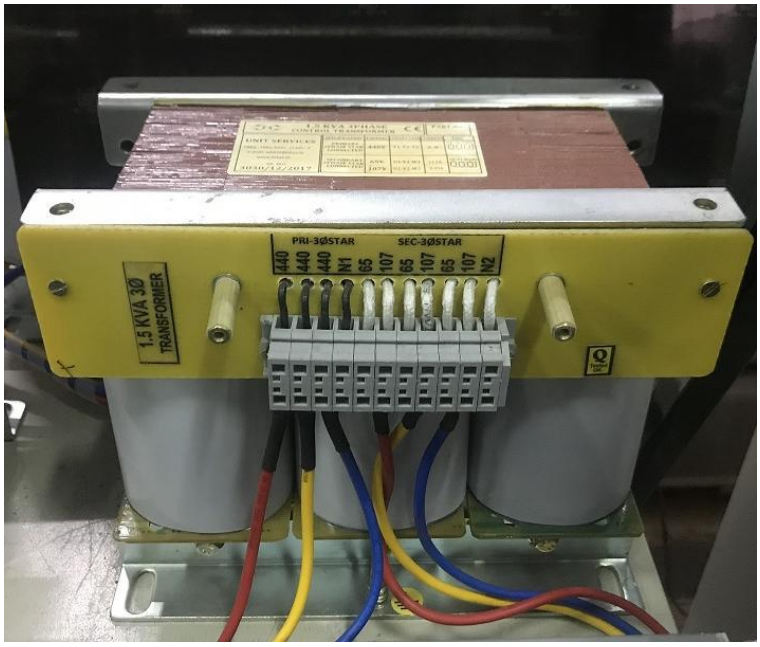

Figure 3.1: 3 phase step down transformer

First cell in each phase has the circuitry required for bypass operation. A three pole relay operated circuited breaker is connected at the input of diode bridge rectifier and two pole MCB is connected at the output of the cell which are poles of the IGBT modules. sA by- pass switch is connected in between the two out terminals of the cells. By-pass switch is a semiconductor device which should not allow the current if the pulses are not given.

SEMIKRON IGBT module has 7 accessible points. Point 3 is the collector of the top switch. Point 1 is the emitter of the top switch which is connected to the collector of the bottom switch. Point 2 is the emitter of the bottom switch. Points 4 and 6 are the gates of the top and bottom switches respectively. Points 5 and 7 are connected to Points 5 and 7 are connected to points 1 and 2 respectively.

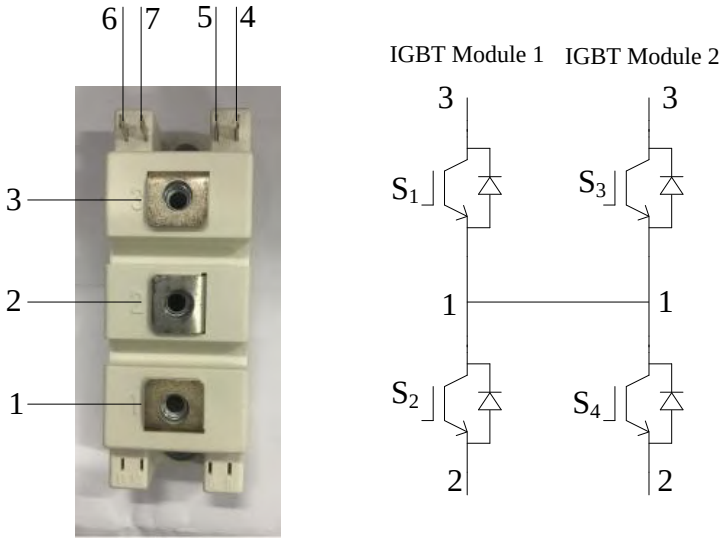

Figure 3.2: Circuit connection of a bypass switch

Two IGBT modules are connected as shown in the *Figure:3.2.* The point 1 in both of the IGBT modules are connected and point 3 in both of the IGBT modules are connected to the output terminals of the cell. This connection is also valid for point 2. The same switching pulse should be given to both switches. If the pulses are not given the diodes do not allow the current to flow.

Figure 3.3: Bypass switch in the hardware setup

Two gate drivers are required for two IGBT modules. PWM board is present which acts like interface between the gate drivers and the control circuit. In this PWM board, the error signals from the gate drivers are taken and combined into

one signal and are taken into the control circuit for protection and control algorithm.

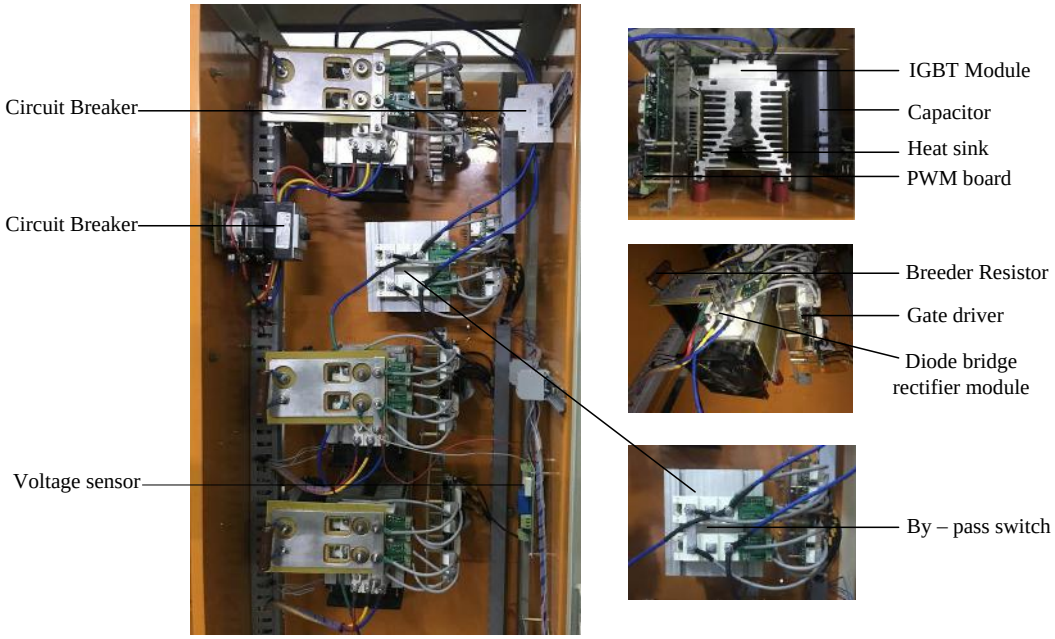

Figure 3.4: One leg of the CHB inverter in the hardware setup

3.3 DSP - FPGA based Hybrid board

DSP - FPGA based hybrid board consists of two processors. They are TMS320F28335 and EP4CE30F23I7N./ TMS320F28335 is a Digital Signal controller which has 32 bit DSP core with modified harvard architecture. It also has a single precision IEEE754 floating point unit. The C/C++ engine of device supports the user to implement the control algorithm in high level languages. Real-time JTAG of the device supports the user for real time debugging alone with Code Composer Studio(CCS) from Texas instruments. It also has 88 GPIO pins multiplexed with other peripherals like PWM,capture unit, ADC etc. The standard communications interface like I2C and CAN are supported by the controller.

EP4CE30F23I7N belongs to Cyclone IV E device family manufactured by Altera. It has 30k logic elements and 324 user (I/O)'s. The device can be programmed by JTAG programming and Active serial programming using QUARTUS II software. The communication interfaces like RS-232, RS-485, CAN and

USB are supported by the controller. This device is chosen to meet the industrial grade temperature ($-40°/85°$).

The hybrid board has an analog conditioning section for both DSP and FPGA section seperately. Some of the pins of TMS320F28335 and EP4CE30F23I7N are connected internally on the board through traces which enables communication between processors.

3.4 Protection and Delay card

PD card consists of Altera MAX II EPM1270 processor. It is based on Look Up Table(LUT) Architecture. It is programmed using QUARTUS II software. The main features of PD card are

- PD card contains analog comparator circuits where the sensed currents and voltages are compared with the reference values. The reference values are adjusted using the potentiometers present on the board. These output signals of the comparators are used for protection against faults.
- PWM signals are taken into the board and complimentary signals are generated with a dead time.
- All the relay signals are given from the PD card.

3.5 Current and Voltage sensors

Voltage and current sensors are used to sense DC voltage and phase current. LA100P and LV25P are hall effect based voltage and current sensors.The output of the voltage sensor and current sensors are taken into PD card for protection purpose. They are taken into the hybrid board for control algorithms. The burden resistors are chosen in such way that the output voltage of the current sensor is 5 V if the actual current is 100A and the output voltage of voltage sensor is 5 V if the actual voltage is 1000 V.

3.6 Hardware Setup

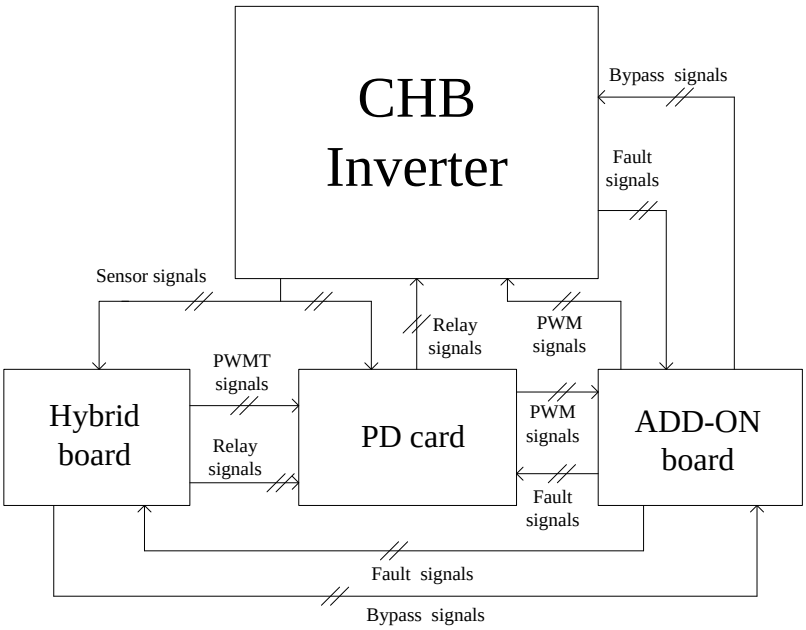

Figure 3.5: Block diagram of signal flow between control circuit and power circuit

The block diagram in *Figure:3.5* explains the flow of the signal from control to power circuit. Add on board is the interface board through which all the PWM signals and the bypass signals are given to the inverter.

Figure 3.6: DSP - FPGA based Hybrid board

The DSP - FPGA based hybrid board which is developed in the lab is shown in*Figure: 3.6.*

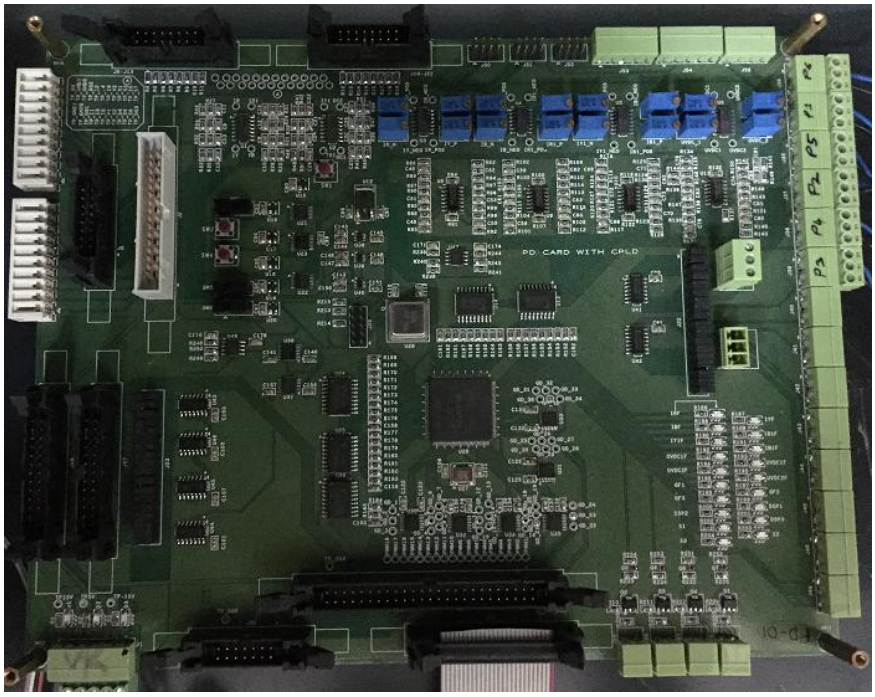

Figure 3.7: Protection and Delay card

Protection and Delay card which is developed in the lab is shown in the *3.7*.

Figure 3.8: Add on board

Add on board which is developed in the lab is shown in *Figure:3.8*.

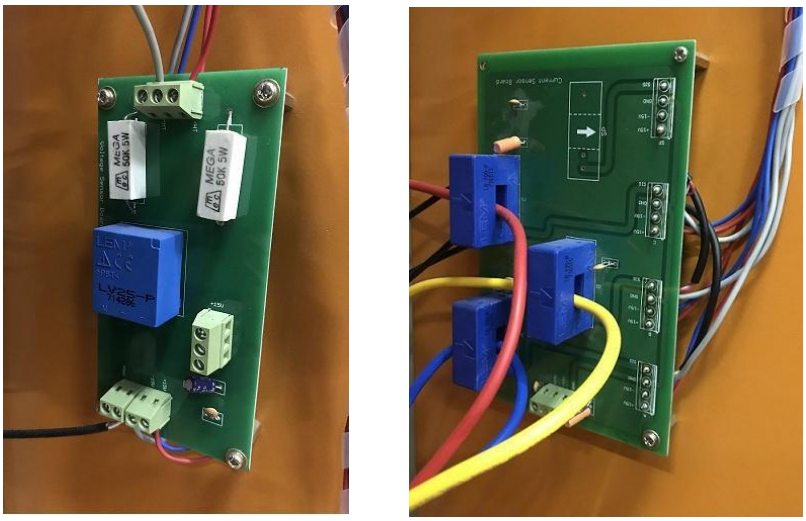

Figure 3.9: Voltage and current sensors

The voltage and current sensors used in the setup are shown in the *Figure: 3.9*

Figure 3.10: CHB Inverter set up

Cascaded H bridge inverter setup which is developed in the lab is shown in the *Figure: 3.10.*

Figure 3.11: Voltage and current sensors

Arrangement of the 9 step-down transformers is as shown in the *Figure:3.11*

Figure 3.12: Induction machine in lab

30 kW induction machine which is used in hardware implementation

3.7 Conclusion

This chapter has outlined different components of the cascaded H bridge converter. The additional boards which are required in hardware implementation are discussed. The voltage and current sensing equipment is also discussed. All the cells and boards are tested. In the next chapter simulation and hardware results will be presented.

CHAPTER 4

Results and Inferences

4.1 Simulation Results

The simulation of cascaded H bridge inverter fed induction motor drive with fault tolerance algorithm is done in SIMULINK with a cascaded H bridge inverter which has five cells in each phase and a 3.7 kW induction motor. The simulation studies are done for three different cell configurations of cascaded H Bridge inverter which are possible in fault conditions. The machine specification and parameters are given in *Table:4.1* and *Table:4.2* respectively.

Table 4.1: Machine Specifications

S.No	Parameter	Value
1	Power	3.7 kW
2	Voltage	460 V
3	Frequency	60 hz
4	Poles	4
5	Speed	1750 rpm
6	Rotor Type	Squirrel cage

Table 4.2: Model parameters

R_s	R'_r	L_{ls}	L_{lr}	J
1.115 Ω	1.083 Ω	5.974 mH	5.974 mH	0.2 $kg - m^2$

4.1.1 (455) Cell Configuration

CHB inverter has five cells in pre-fault condition.A fault is detected at time $t = 8.5$ in phase A and the cell is bypassed and pulses are enabled at time $t = 8.6$. In post fault condition, legs A,B and C have four,five and five cells respectively. The phase angles and speed reference in pre-fault and post fault condition are given in the *Table:4.3*

Table 4.3: Phase angles and speed reference in pre-fault and post-fault condition

Fault condition	δ_1	δ_2	δ_3	Speed reference
Pre-Fault	0°	−120°	120°	183.25 rad/sec
Post-fault	0°	−126.42°	126.42°	183.25 rad/sec

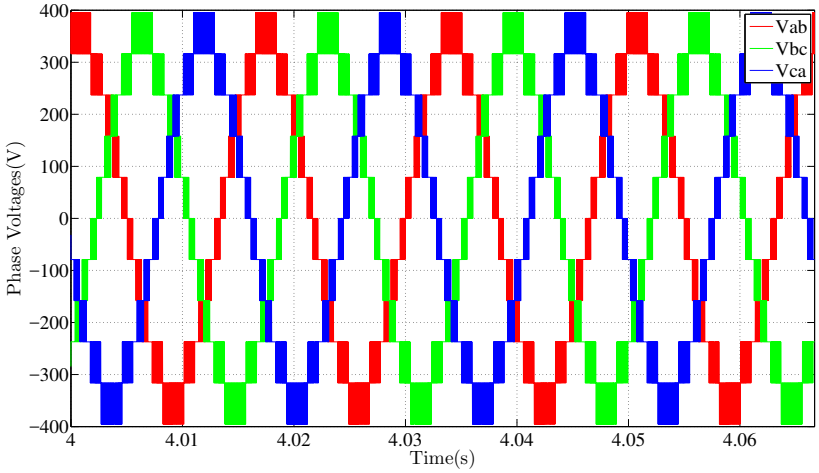

Figure 4.1: *Simulation result*: Phase Voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.1 shows the phase voltages of the CHB Inverter in pre-fault condition. V_{ar}= 238.5 V, V_{br} = 238.1 V, V_{cr}= 238.4 V

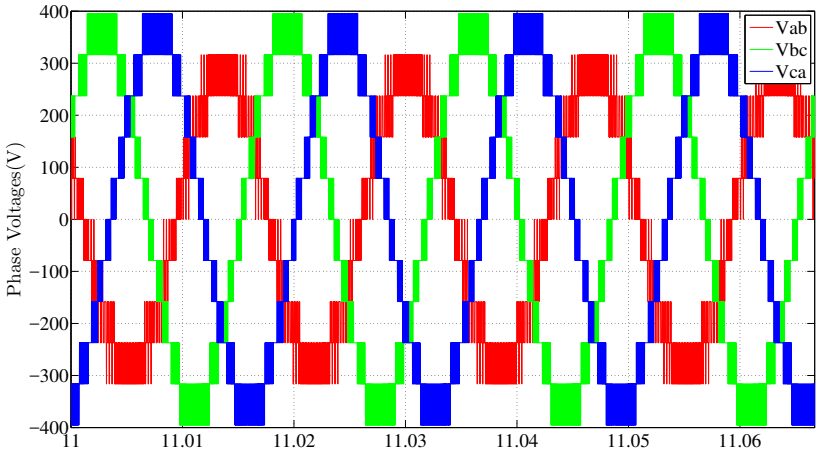

Figure 4.2: *Simulation result*: Phase Voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.2 shows the phase voltages of the CHB Inverter in post-fault condition. V_{ar} = 205.2 V, V_{ar} = 256.2 V, V_{ar}= 256.7 V

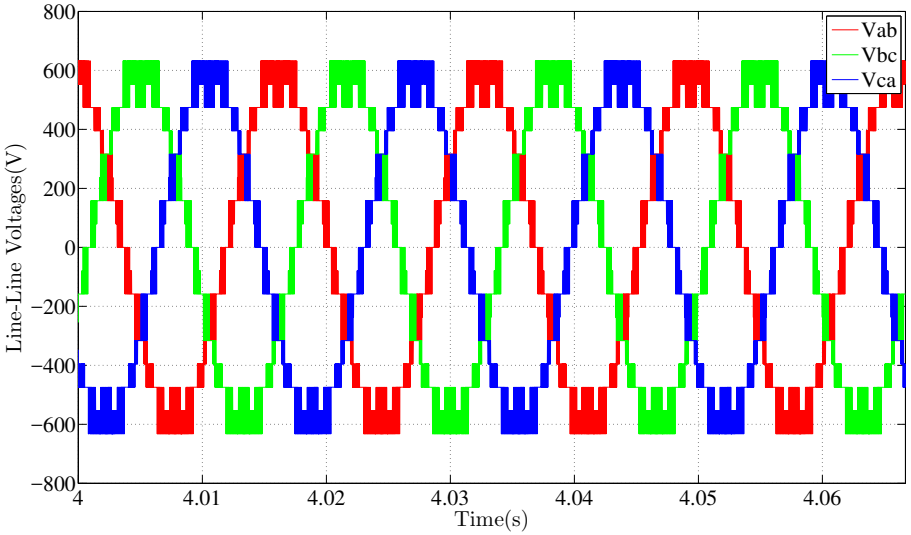

Figure 4.3: *Simulation result*: Line - Line voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.3 shows the line - line voltages of the inverter in the pre-fault condition. $V_{abr} = 412.8$ V, $V_{bcr} = 412.5$ V, $V_{car} = 413.1$ V

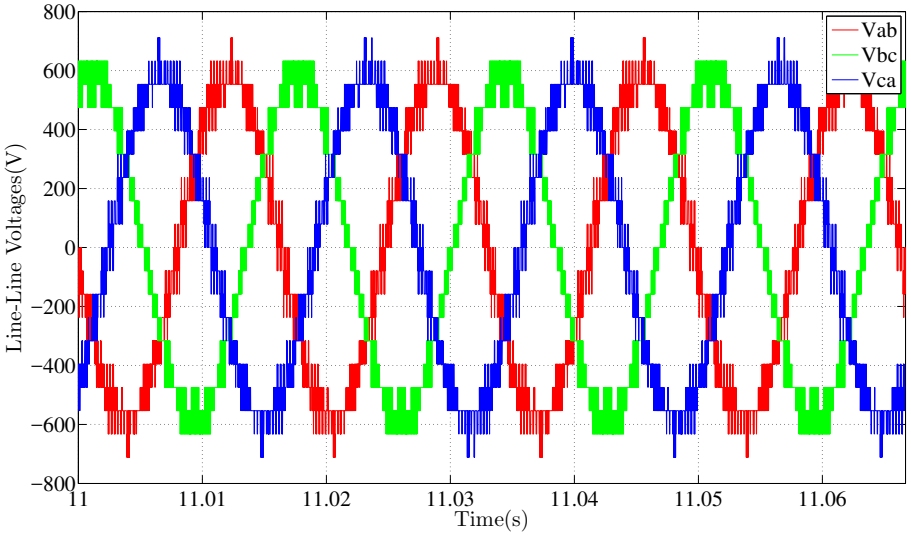

Figure 4.4: *Simulation result*: Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.4 shows the line - line voltages in post fault condition.

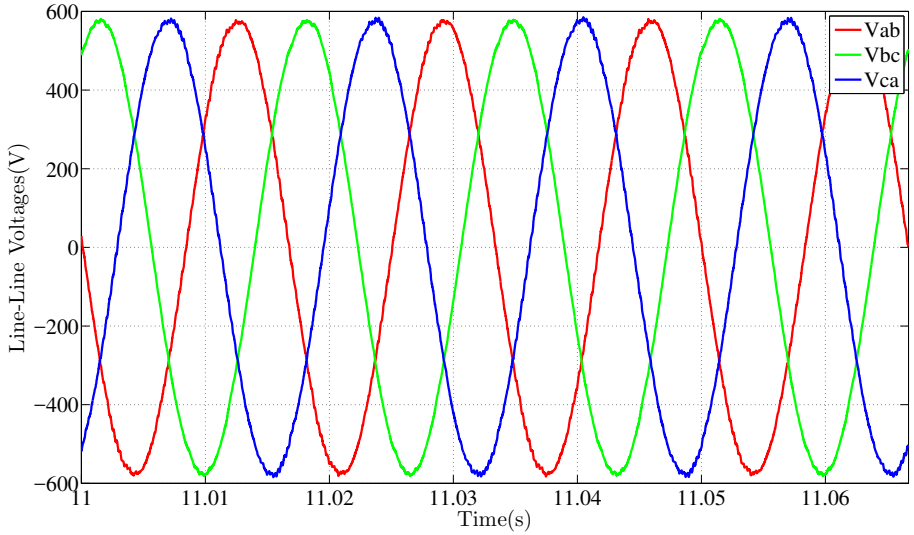

Figure 4.5: *Simulation result*: Fundamental components of Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis:200V/div)*

Figure: 4.5 shows the fundamental components of the line - line voltages of the inverter. V_{abr} = 412.6 V V, V_{bcr} = 412.5 V, V_{car} = 413 V

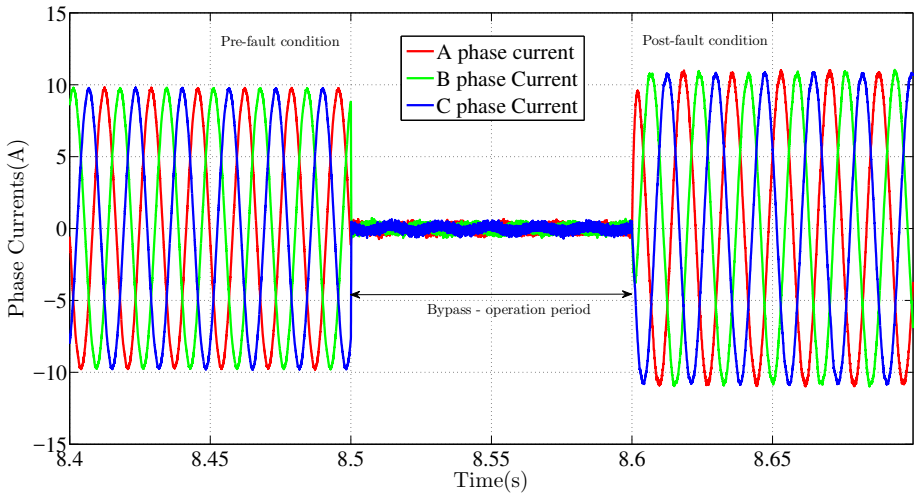

Figure 4.6: *Simulation result*: Magnified view of the phase currents during t = *8.4* to t = *8.7*. *(Scale: X-axis: 0.05s/div, Y-axis:5A/div)*

Figure: 4.6 shows the phase currents of the inverter. During the time period between t = *8.5* to t = *8.6*, the pulses to the inverter are disabled. So, the currents are zero and currents in pre-fault and post fault condition are balanced.

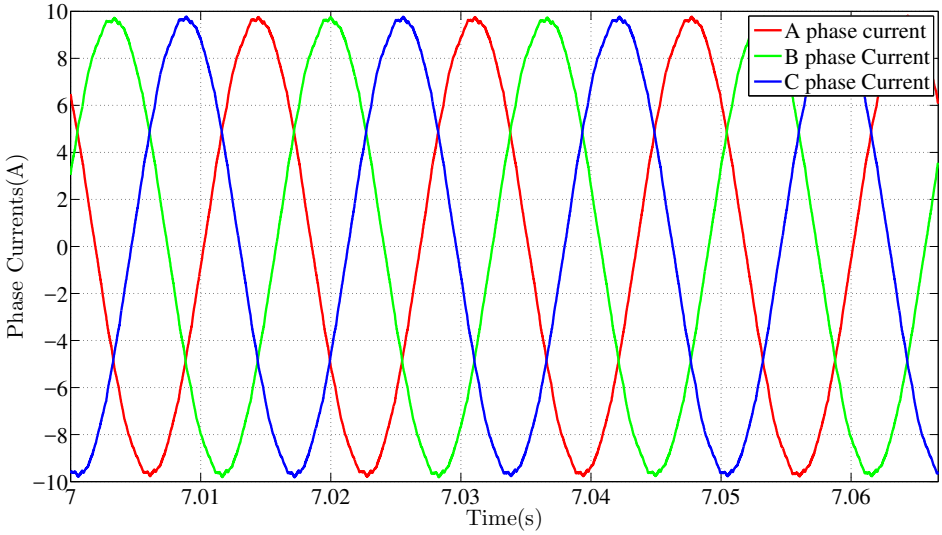

Figure 4.7: *Simulation result*: Phase currents in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.7 shows the phase currents of the inverter in the pre - fault condition. $I_{ar} = 6.85$ A, $I_{br} = 6.855$ A, $I_{cr} = 6.855$ A

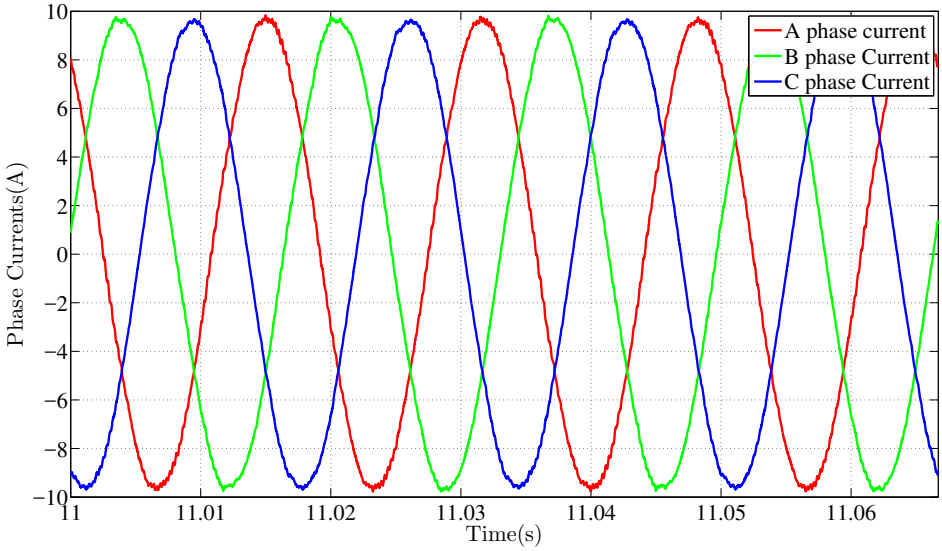

Figure 4.8: *Simulation result*: Phase currents in post-fault condition .*(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.8 shows the phase currents of the inverter in the post - fault condition. $I_{ar} = 6.85$ A, $I_{br} = 6.855$ A, $I_{cr} = 6.855$ A

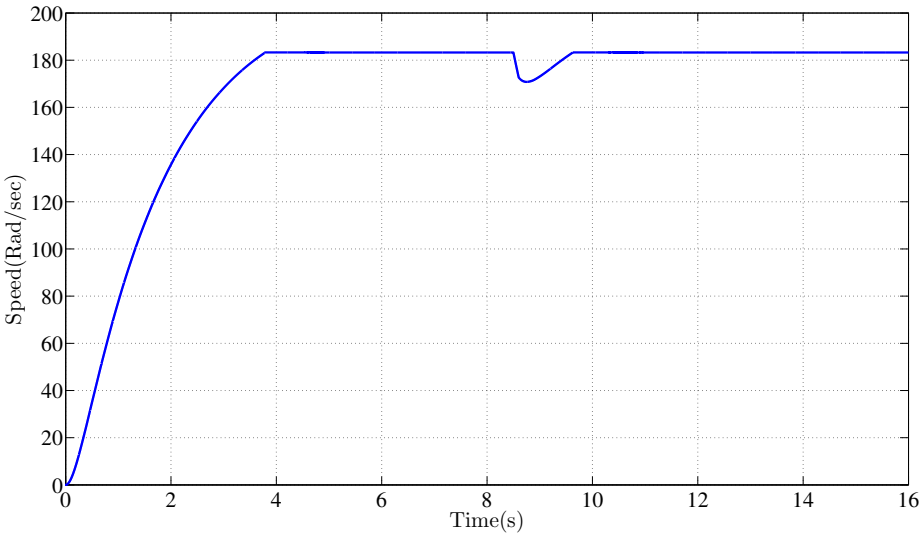

Figure 4.9: *Simulation result*: Speed of the motor in pre-fault and post fault condition. *(Scale: X-axis: 2s/div, Y-axis: 20(rad/s)/div)*

Figure: 4.9 shows the speed of the machine.Speed of the motor in the pre-fault condition is 183.25 rad/sec. During the time period between $t = 8.5$ to $t = 8.6$, the pulses to the inverter are disabled so the speed of the motor is decreasing. At $t = 8.6$ pulses are enabled and speed of the motor starts increasing and reaches a steady state value of 183.25 rad/sec.

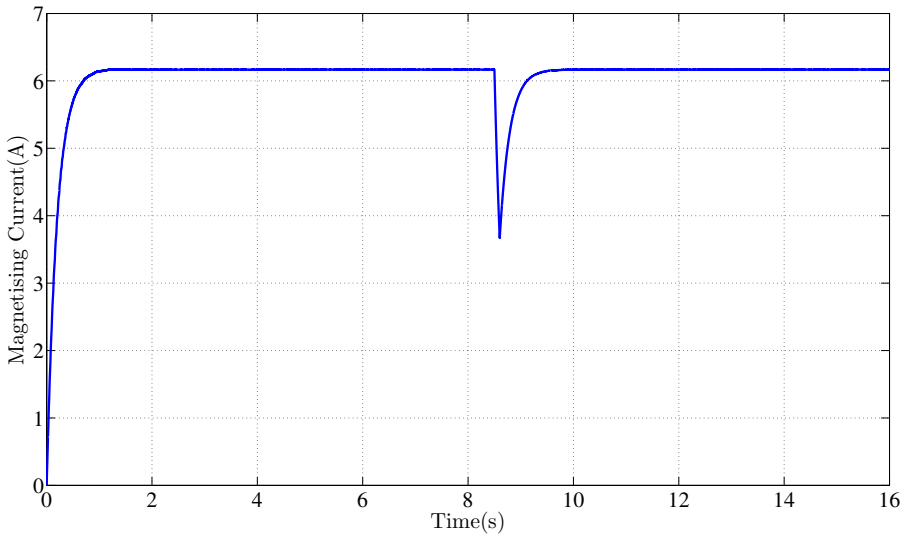

Figure 4.10: *Simulation result*: Change in magnetising current during fault condition. *(Scale: X-axis: 2s/div, Y-axis: 1A/div)*

Figure: 4.10 shows the change in magnetising current (i_{mr}) during the by -

pass operation period. During the by -pass operation period, i_{mr} value is decreasing. At the end of the by - pass operation period, the pulses are enabled and i_{mr} increases and settles at a steady state value which is same as pre-fault case.

4.1.2 (445) Cell Configuration

CHB inverter has five cells in pre-fault condition. A fault is detected at time $t = 8.5$ in phase A and the cell is bypassed and pulses are enabled at time $t = 8.6$. In post fault condition, legs A,B and C have four,four and five cells respectively. The phase angles and speed reference in pre-fault and post fault condition are given in the *Table:4.4*

Table 4.4: Phase angles and speed reference in pre-fault and post-fault condition

Fault condition	δ_1	δ_2	δ_3	Speed reference
Pre-Fault	0°	−120°	120°	183.25 rad/sec
Post-fault	8.68°	−128.68°	120°	175.82 rad/sec

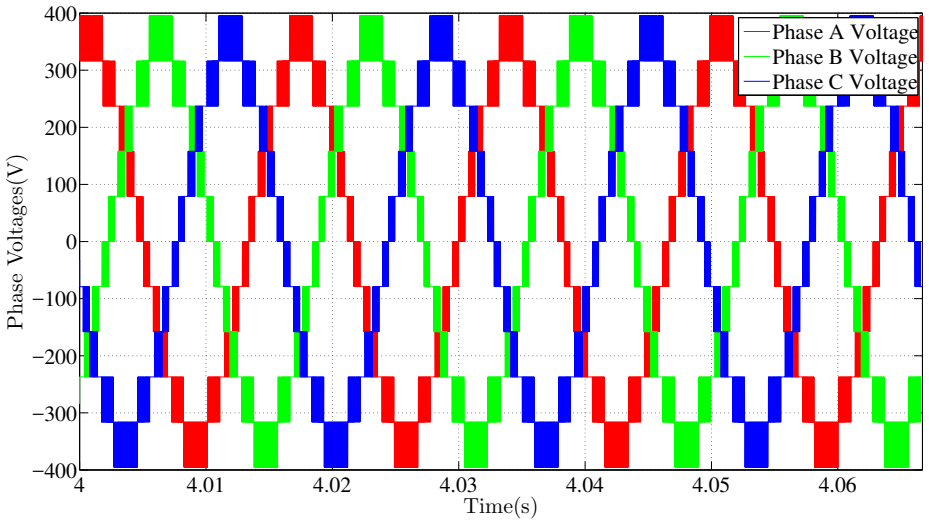

Figure 4.11: *Simulation result*: Phase Voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.11 shows the phase voltages of the CHB Inverter in pre-fault condition. V_{ar}= 238.5 V, V_{br} = 238.1 V, V_{cr}= 238.4 V

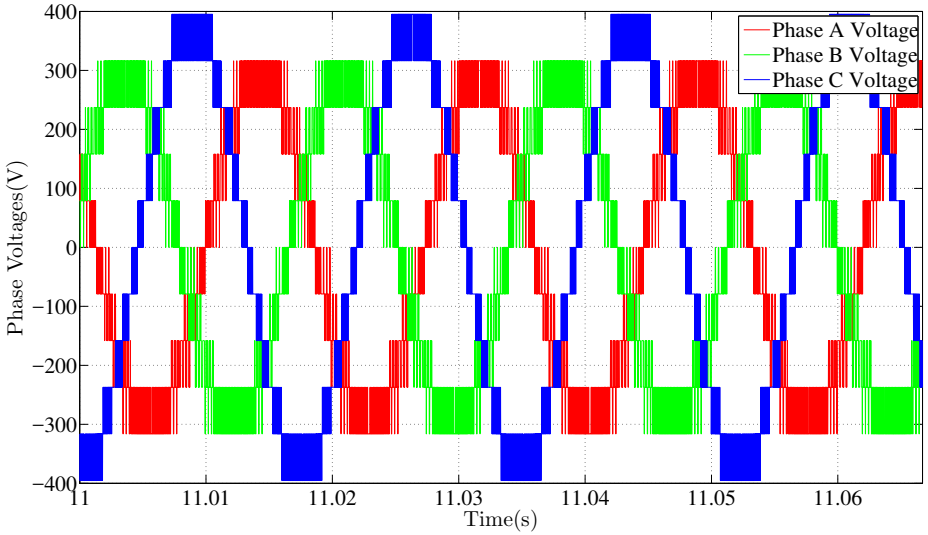

Figure 4.12: *Simulation result*: Phase Voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.12 shows the phase voltages of the CHB Inverter in post-fault condition. V_{ar} = 212.5 V, V_{br} = 212.4 V,V_{cr}= 265.6 V

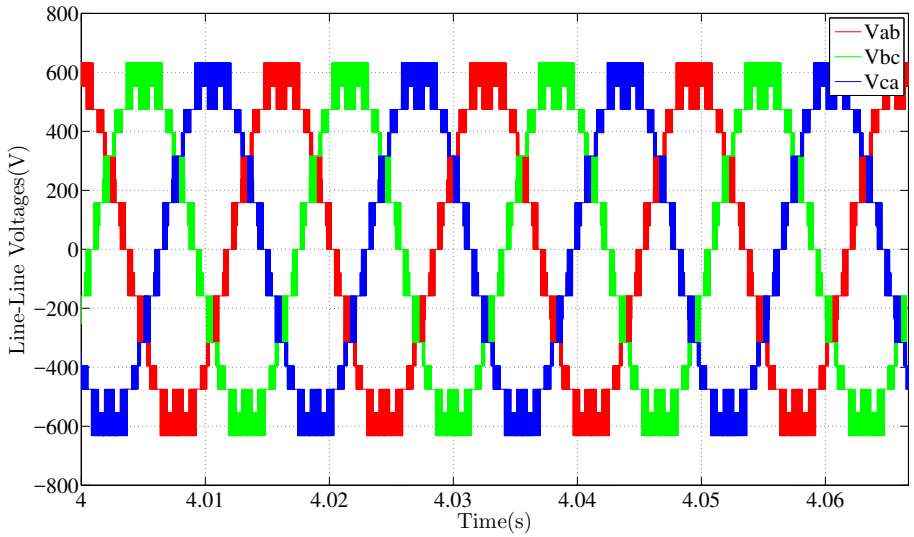

Figure 4.13: *Simulation result*: Line - Line voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.13 shows the line - line voltages of the inverter in the pre-fault condition. V_{abr} = 412.8 V V, V_{bcr} = 412.5 V, V_{car} = 413.1 V

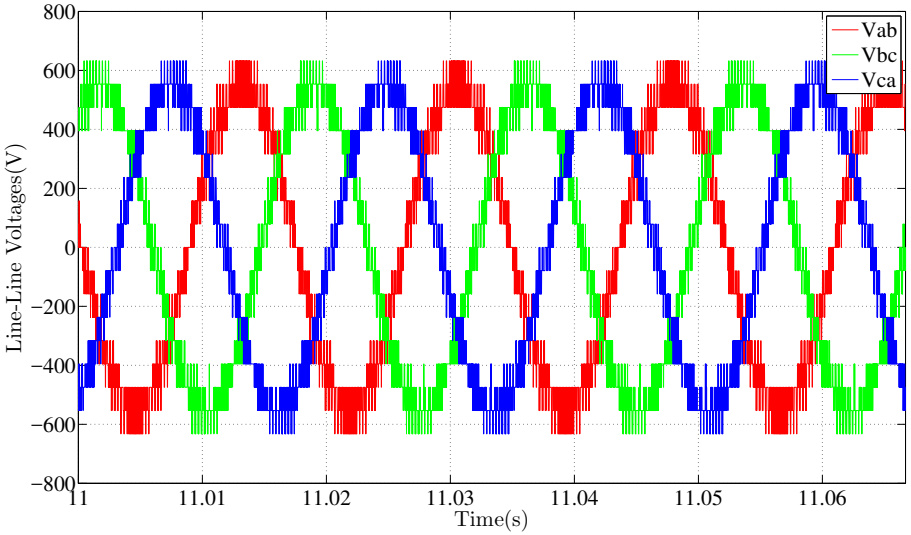

Figure 4.14: *Simulation result*: Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.14 shows the line - line voltages in post fault condition.Voltages are balanced

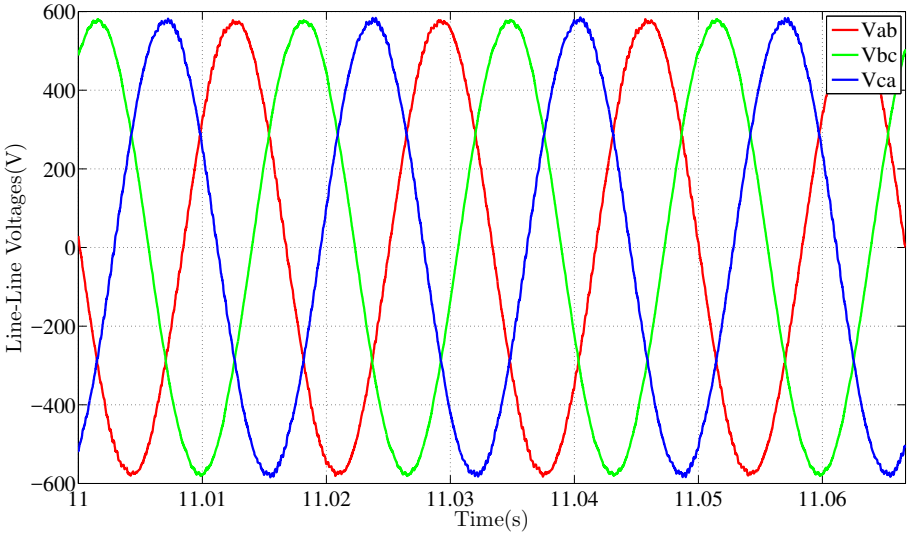

Figure 4.15: *Simulation result*: Fundamental components of Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis:200V/div)*

Figure: 4.15 shows the fundamental components of the line - line voltages of the inverter. $V_{abr} = 395.9$ V, $V_{bcr} = 395.7$ V, $V_{car} = 395.9$ V

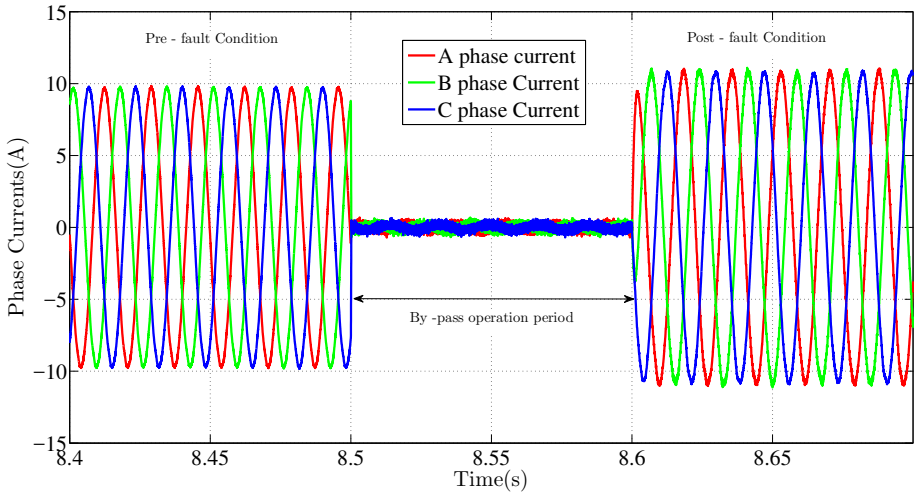

Figure 4.16: *Simulation result*: Magnified view of the phase currents during $t = 8.4$ to $t = 8.7$. *(Scale: X-axis: 0.05s/div, Y-axis:5A/div)*

Figure: 4.16 shows the phase currents of the inverter. During the time period between $t = 8.5$ to $t = 8.6$, the pulses to the inverter are disabled. So, the currents are zero and currents in pre-fault and post fault condition are balanced.

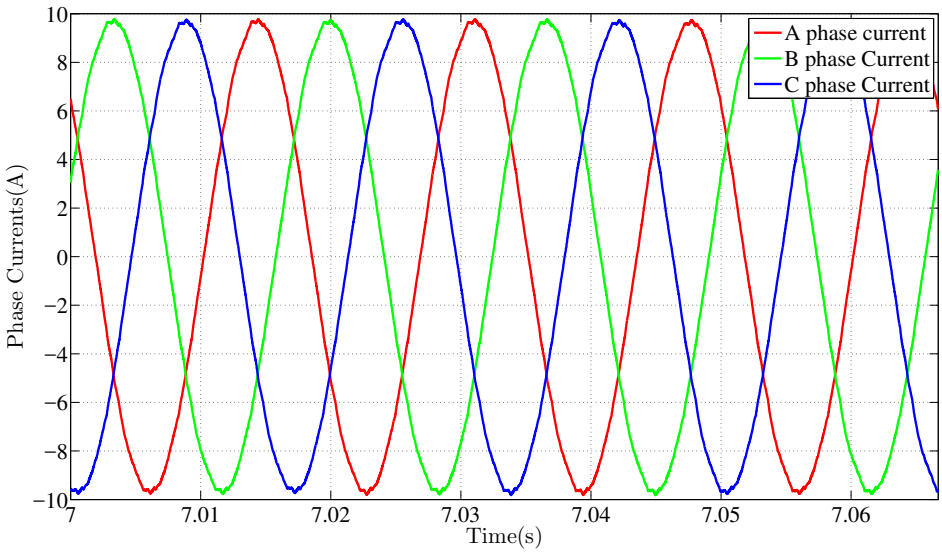

Figure 4.17: *Simulation result*: Phase currents in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.17 shows the phase currents of the inverter in the pre - fault condition. $I_{ar} = 6.85$ A, $I_{br} = 6.855$ A, $I_{cr} = 6.855$ A

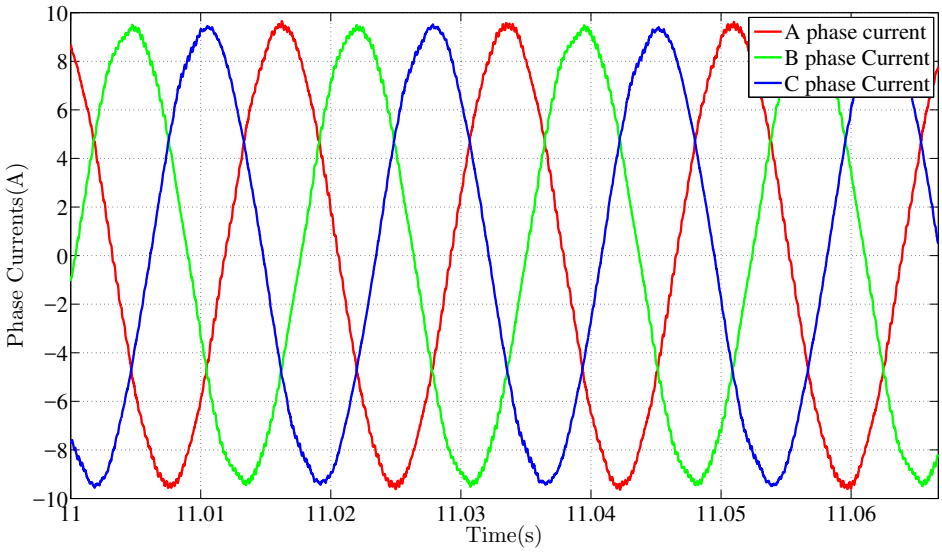

Figure 4.18: *Simulation result*: Phase currents in post-fault condition .*(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.18 shows the phase currents of the inverter in the post - fault condition. $I_{ar} = 6.631$ A, $I_{br} = 6.617$ A , $I_{cr} = 6.62$ A

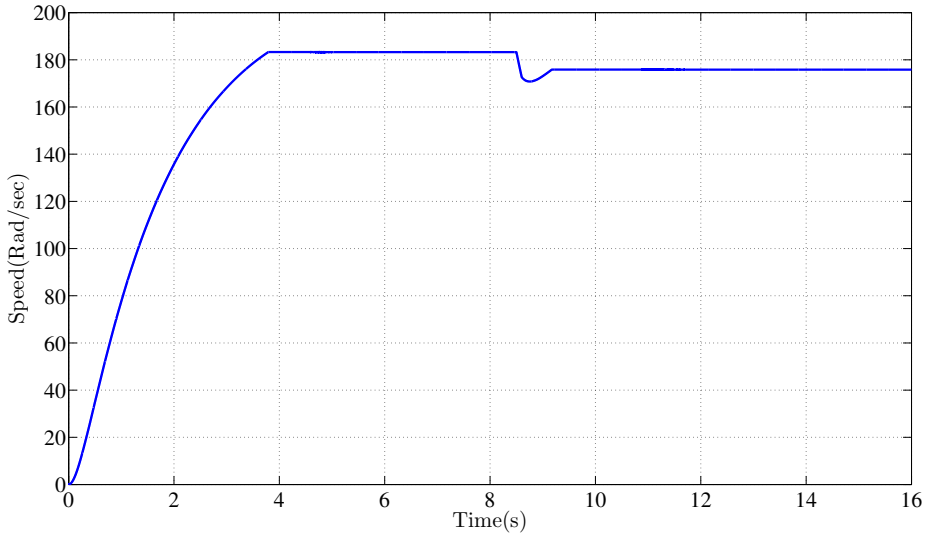

Figure 4.19: *Simulation result*: Speed of the motor in pre-fault and post fault condition. *(Scale: X-axis: 2s/div, Y-axis: 20(rad/s)/div)*

Figure: 4.19 shows the speed of the machine.Speed of the motor in the pre-fault condition is 183.25 rad/sec. During the time period between $t = 8.5$ to $t = 8.6$, the pulses to the inverter are disabled so the speed of the motor is decreasing. At $t = 8.6$ pulses are enabled and speed of the motor starts increasing and reaches

a steady state value of 175.82 rad/sec.

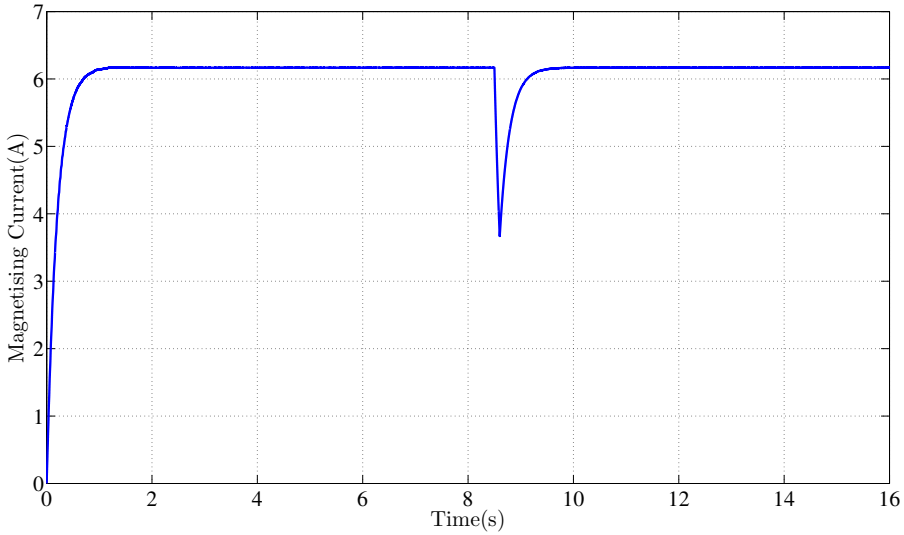

Figure 4.20: *Simulation result*: Change in magnetising current during fault condition. *(Scale: X-axis: 2s/div, Y-axis: 1A/div)*

Figure: 4.20 shows the change in magnetising current (i_{mr}) during the by -pass operation period. During the by -pass operation period, i_{mr} value is decreasing. At the end of the by - pass operation period, the pulses are enabled and i_{mr} increases and settles at a steady state value which is same as pre-fault case.

4.1.3 (345) Cell Configuration

CHB inverter has five cells in pre-fault condition.A fault is detected at time $t = 8.5$ in phase A and the cell is bypassed and pulses are enabled at time $t = 8.6$. In post fault condition, legs A,B and C have three, four and five cells respectively. The phase angles and speed reference in pre-fault and post fault condition are given in the *Table:4.5*

Table 4.5: Phase angles and speed reference in pre-fault and post-fault condition

Fault condition	δ_1	δ_2	δ_3	Speed reference
Pre-Fault	$0°$	$-120°$	$120°$	183.25 rad/sec
Post-fault	$12.81°$	$-137.19.42°$	$125.94°$	159.81 rad/sec

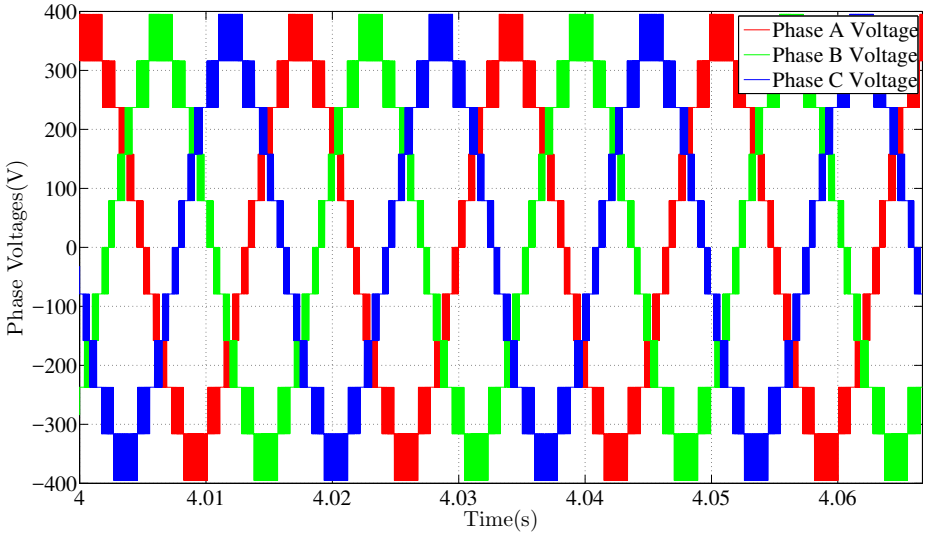

Figure 4.21: *Simulation result*: Phase Voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.21 shows the phase voltages of the CHB Inverter in pre-fault condition. V_{ar}= 238.5 V, V_{br} = 238.1 V, V_{cr}= 238.4 V

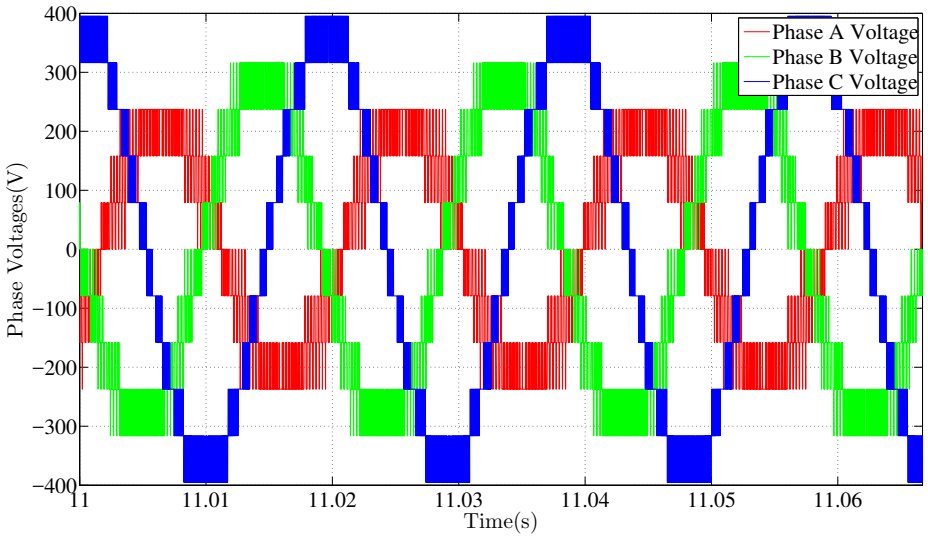

Figure 4.22: *Simulation result*: Phase Voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.22 shows the phase voltages of the CHB Inverter in post-fault condition. V_{ar} = 159.23 V, V_{br} = 212.3 V, V_{cr}= 265.2 V

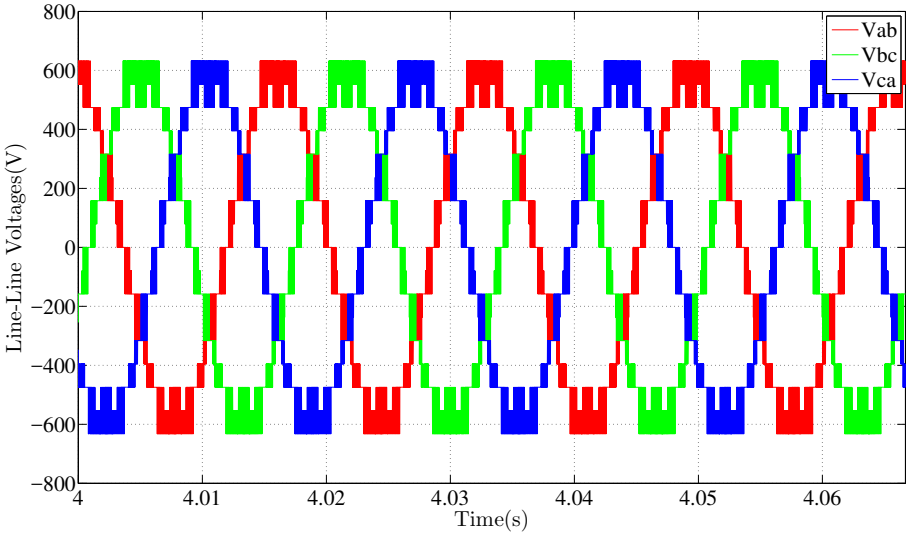

Figure 4.23: *Simulation result*: Line - Line voltages in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.23 shows the line - line voltages of the inverter in the pre-fault condition. V_{abr} = 412.8 V V, V_{bcr} = 412.5 V, V_{car} = 413.1 V

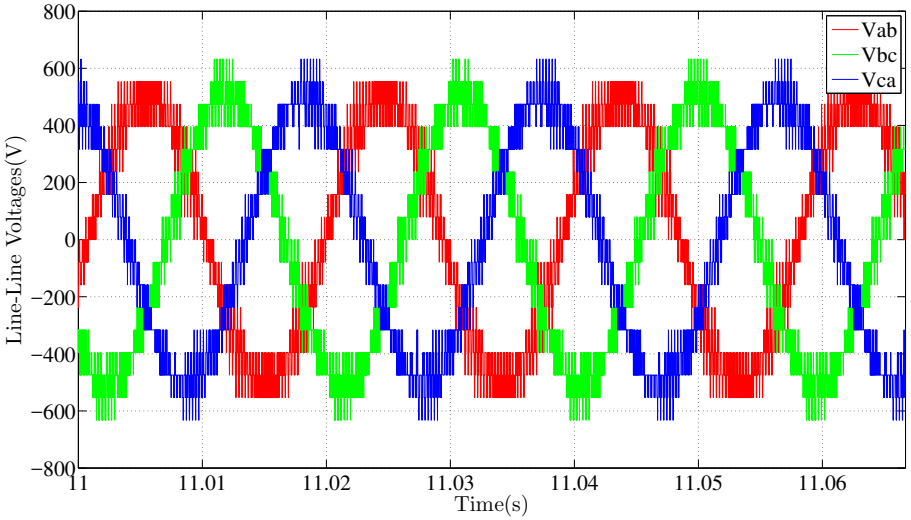

Figure 4.24: *Simulation result*: Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 200V/div)*

Figure: 4.24 shows the line - line voltages in post fault condition.

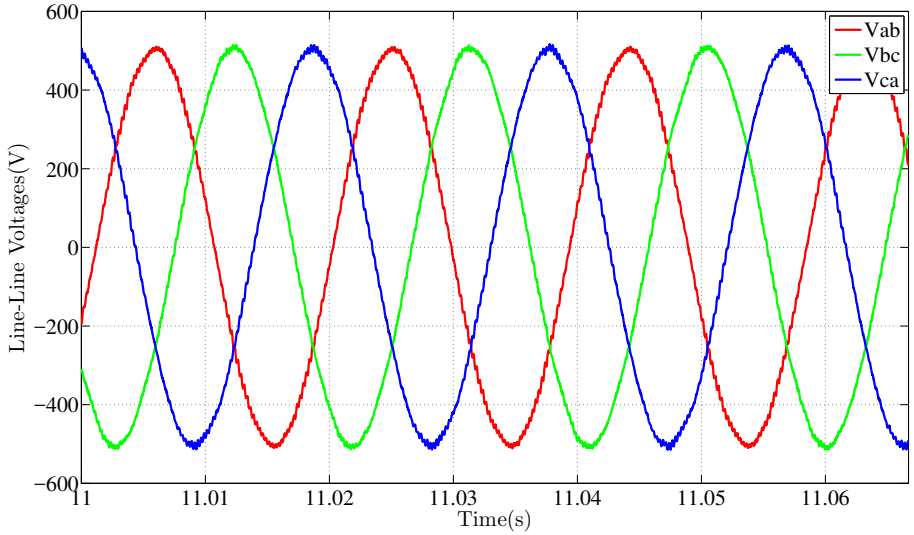

Figure 4.25: *Simulation result*: Fundamental components of Line - Line voltages in post-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis:200V/div)*

Figure: 4.25 shows the fundamental components of the line - line voltages of the inverter. V_{abr} = 359.8 V, V_{bcr} = 359 V, V_{car} = 359.8 V

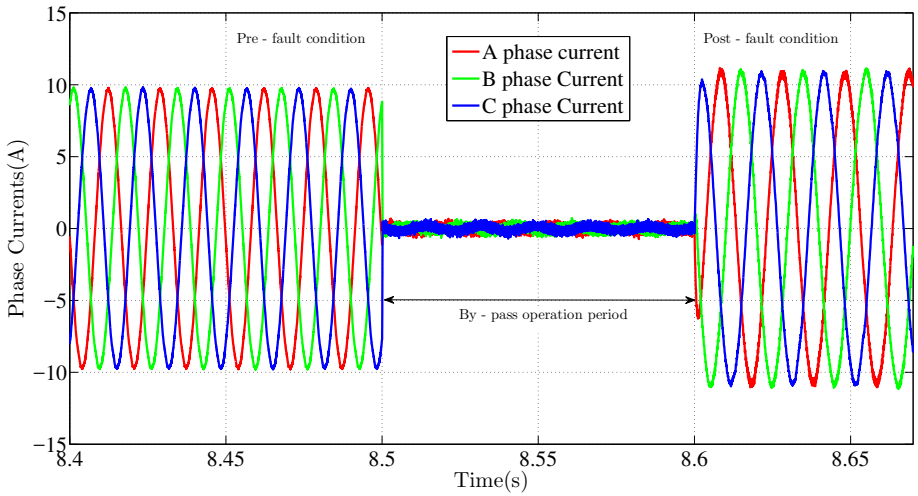

Figure 4.26: *Simulation result*: Magnified view of the phase currents during t = *8.4* to t = *8.7*. *(Scale: X-axis: 0.05s/div, Y-axis:5A/div)*

Figure: 4.26 shows the phase currents of the inverter. During the time period between $t = 8.5$ to $t = 8.6$, the pulses to the inverter are disabled. So, the currents are zero and currents in pre-fault and post fault condition are balanced.

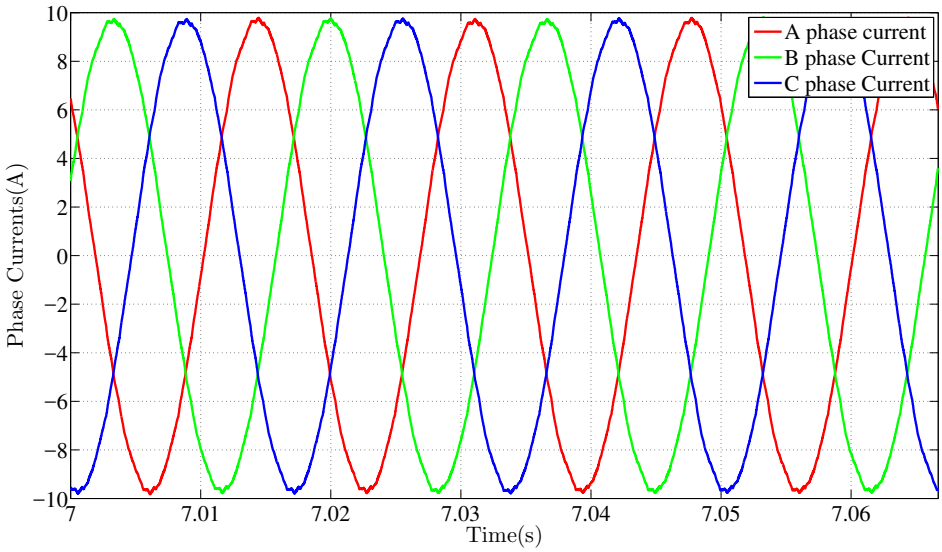

Figure 4.27: *Simulation result*: Phase currents in pre-fault condition. *(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.27 shows the phase currents of the inverter in the pre - fault condition. $I_{ar} = 6.855$ A, $I_{ar} = 6.85$ A, $I_{br} = 6.855$ A, $I_{cr} = 6.855$ A

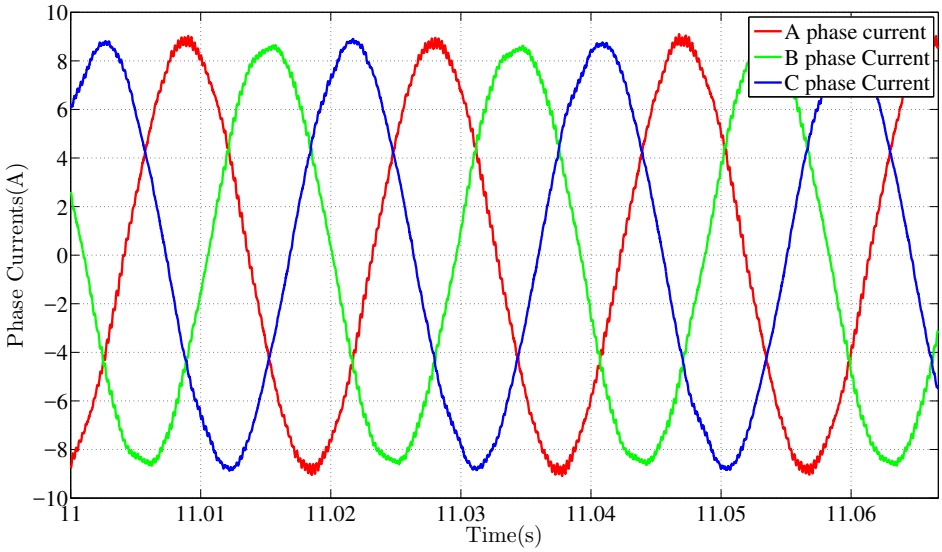

Figure 4.28: *Simulation result*: Phase currents in post-fault condition .*(Scale: X-axis: 0.01s/div, Y-axis: 2A/div)*

Figure: 4.28 shows the phase currents of the inverter in the post - fault condition. $I_{ar} = 6.158$ A, $I_{br} = 6.127$ A, $I_{cr} = 6.132$ A

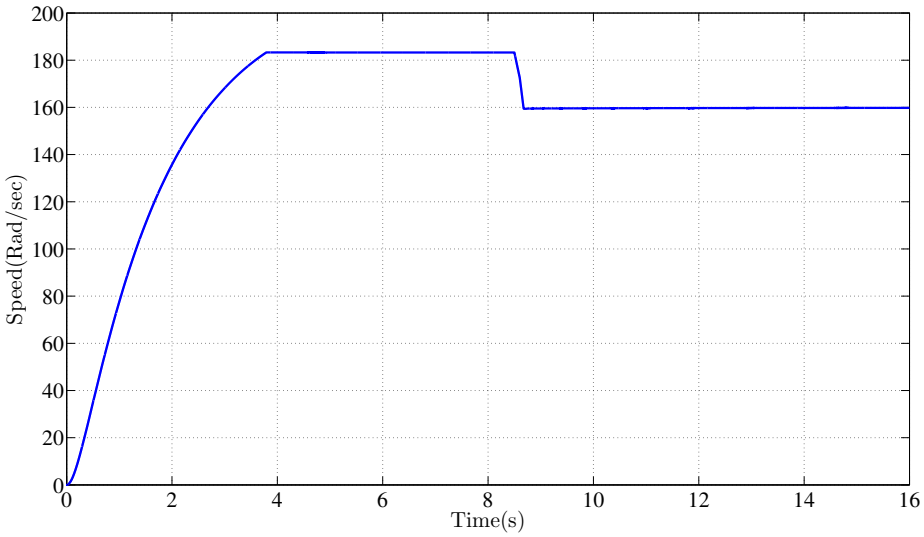

Figure 4.29: *Simulation result*: Speed of the motor in pre-fault and post fault condition. *(Scale: X-axis: 2s/div, Y-axis: 20(rad/s)/div)*

Figure: 4.29 shows the speed of the machine.Speed of the motor in the pre-fault condition is 183.25 rad/sec. During the time period between $t = 8.5$ to $t = 8.6$, the pulses to the inverter are disabled so the speed of the motor is decreasing. At $t = 8.6$ pulses are enabled and speed of the motor starts increasing and reaches a steady state value of 159.81 rad/sec.

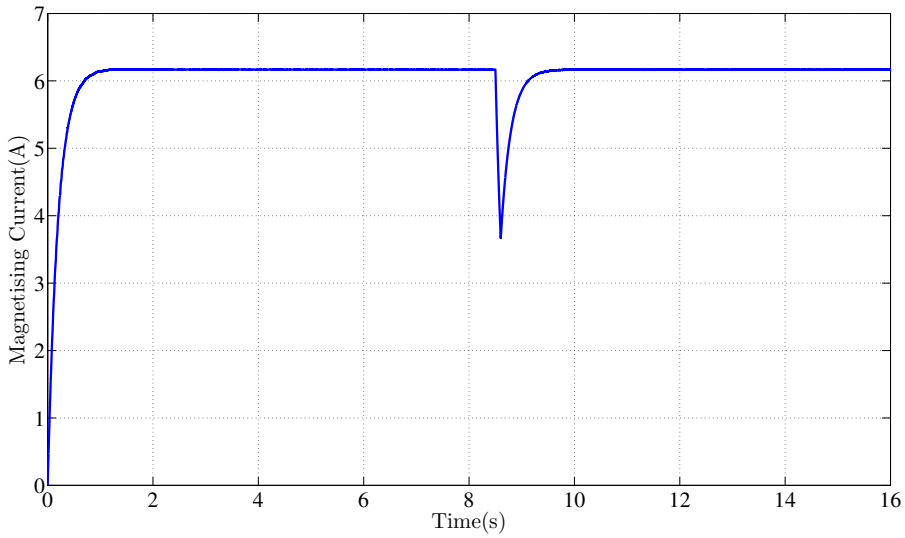

Figure 4.30: *Simulation result*: Change in magnetising current during fault condition. *(Scale: X-axis: 2s/div, Y-axis: 1A/div)*

*Figure: 4.30*shows the change in magnetising current (i_{mr}) during the by -

pass operation period. During the by -pass operation period, i_{mr} value is decreasing. At the end of the by - pass operation period, the pulses are enabled and i_{mr} increases and settles at a steady state value which is same as pre-fault case.

4.2 Hardware results

The hardware implementation is done with a 7-level cascaded H bridge inverter of rating 13.5 kVA and a 30 kW induction machine. The specifications and the model parameters of the machine given in *Table:4:6*

Table 4.6: Machine Specifications

S.No	Parameter	Value
1	Power	30 kW
2	Voltage	380 V
3	Current	59 A
4	Frequency	50 hz
5	Power factor	0.88
6	Speed	1450 rpm
7	Rotor Type	Squirrel cage

Table 4.7: Model parameters

R_s	R'_r	L_{ls}	L_{lr}	J
0.127 Ω	0.127 Ω	1.341 mH	1.341 mH	1.631 $kg - m^2$

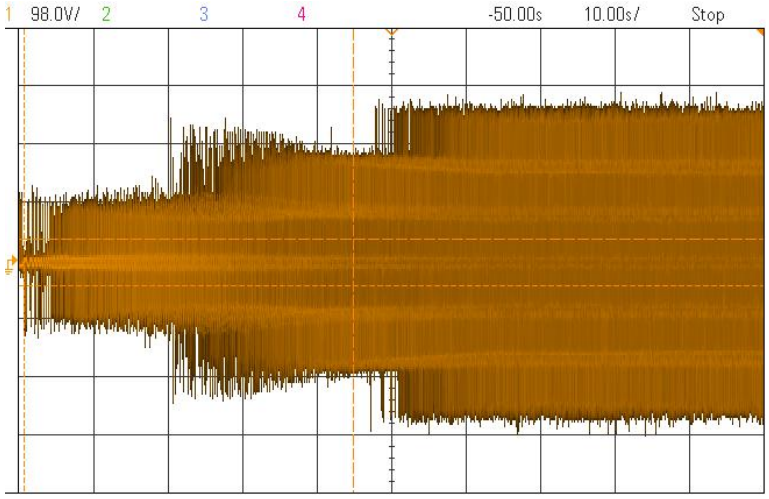

Figure 4.31: *Hardware result*: Phase A voltage profile in a VVVF drive. *(Scale: X-axis: 10s/div, Y-axis: 98V/div)*

Figure: 4.31 shows oscilloscope waveform of the Phase A Voltage profile with a frequency reference of 1 pu.

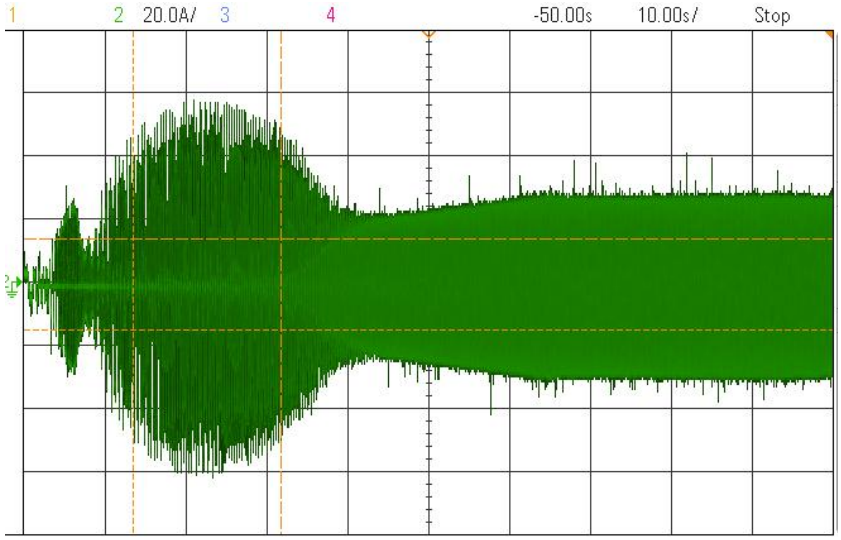

Figure 4.32: *Hardware result*: Phase A current profile in a VVVF drive. *(Scale: X-axis: 10s/div, Y-axis: 10A/div)*

Figure: 4.32 shows oscilloscope waveform of the phase A current profile with a frequency reference of 1 pu.

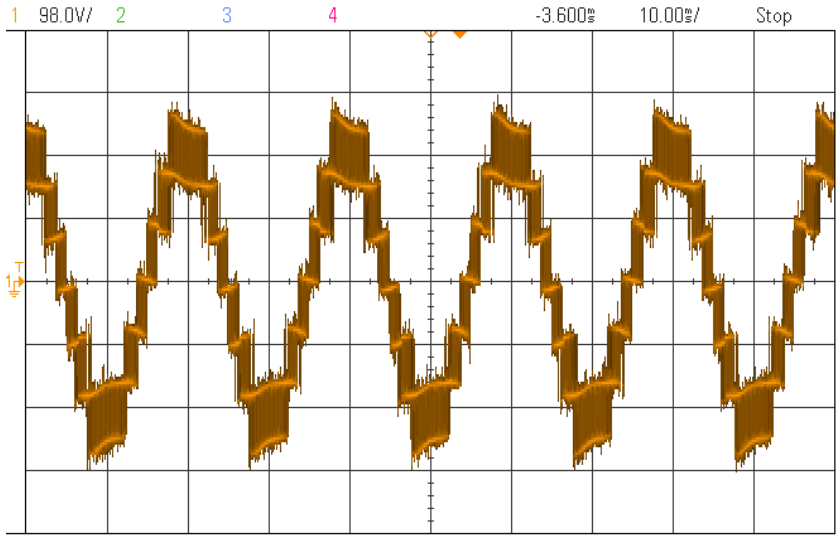

Figure 4.33: *Hardware result*: Phase A voltage. *(Scale: X-axis: 0.01s/div, Y-axis: 98V/div)*

Figure: 4.33 shows oscilloscope waveform of the phase voltage of A phase. The number of levels in phase A is 7.

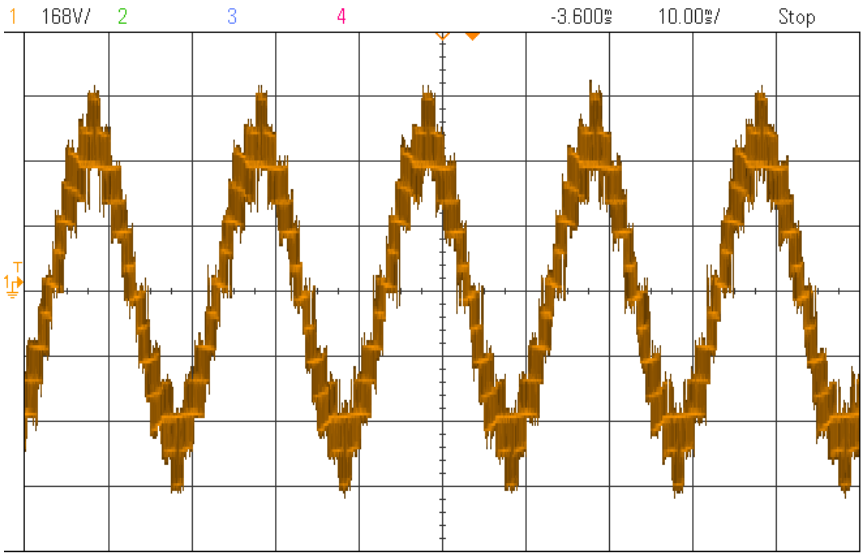

Figure 4.34: *Hardware result*: Line - line voltage . *(Scale: X-axis: 0.01s/div, Y-axis: 168V/div)*

Figure: 4.34 shows oscilloscope waveform of the Line - Line voltage between phases A and B.

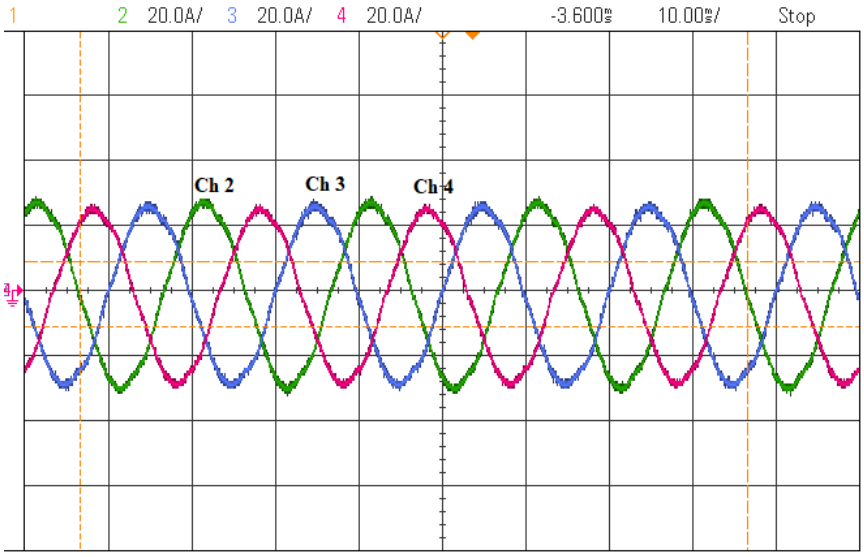

Figure 4.35: *Hardware result*: Currents in phases A, B, C. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.35 shows oscilloscope waveform of the currents in phases A, B ,C.

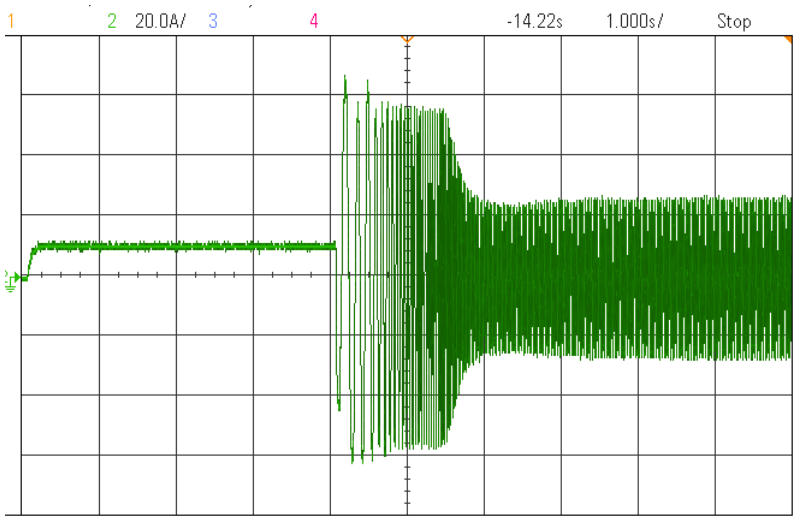

Figure 4.36: *Hardware result*:Phase A current profile in a vector control drive . *(Scale: X-axis: 1s/div, Y-axis: 20A/div)*

Figure: 4.36 shows oscilloscope waveform of the phase A current profile in vector control drive with a speed reference of 0.7 pu.

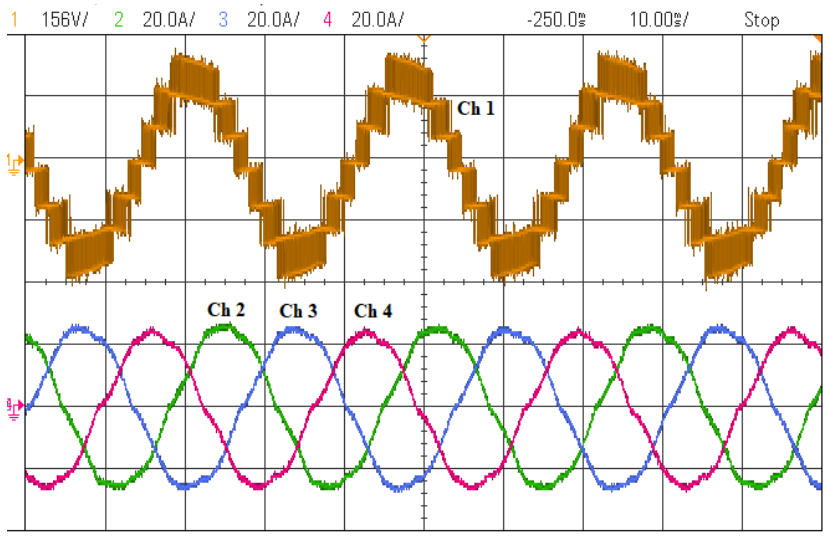

Figure 4.37: *Hardware result*: Phase A voltage and Currents of phases A, B, C. *Ch 1 - Phase A voltage, Ch 2 - A phase Current, Ch 3 - B phase Current, Ch 4 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch1 - 156V/div, Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.37 shows oscilloscope waveforms of phase A voltage and currents of phases A, B, C

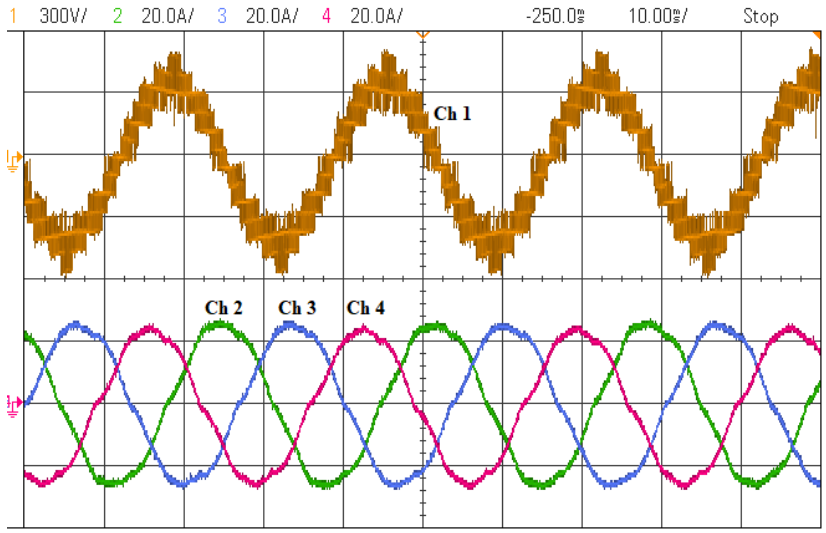

Figure 4.38: *Hardware result*: Line - Line voltage and Currents of phases A, B, C. *Ch 1 - Phase A voltage, Ch 2 - A phase Current, Ch 3 - B phase Current, Ch 4 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch1 - 300V/div, Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.38 shows oscilloscope waveforms of Line - Line voltage between phases A and B and currents of phases A, B, C.

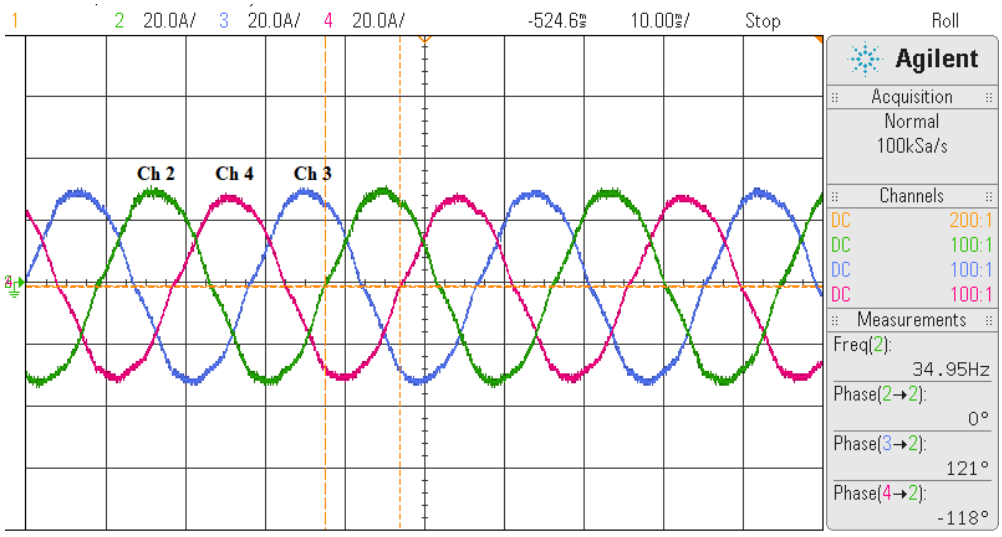

Figure 4.39: *Hardware result*: Currents of phases A, B, C in pre-fault condition. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.39 shows oscilloscope waveforms of currents of phases A, B, C in pre fault condition.

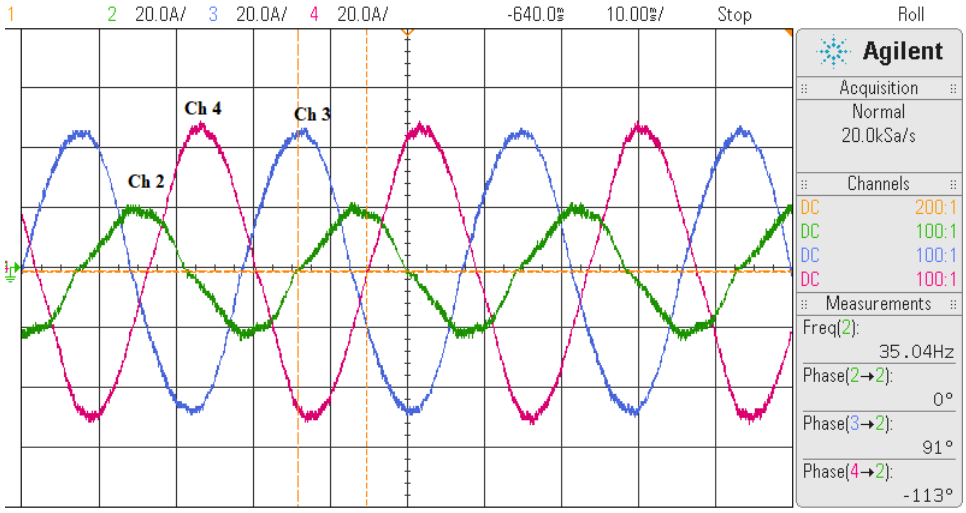

Figure 4.40: *Hardware result*: Currents of phases A, B, C in post-fault condition without modification. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.40 shows oscilloscope waveforms of currents of phases A, B, C in post-fault condition without modification in (233) cell configuration.

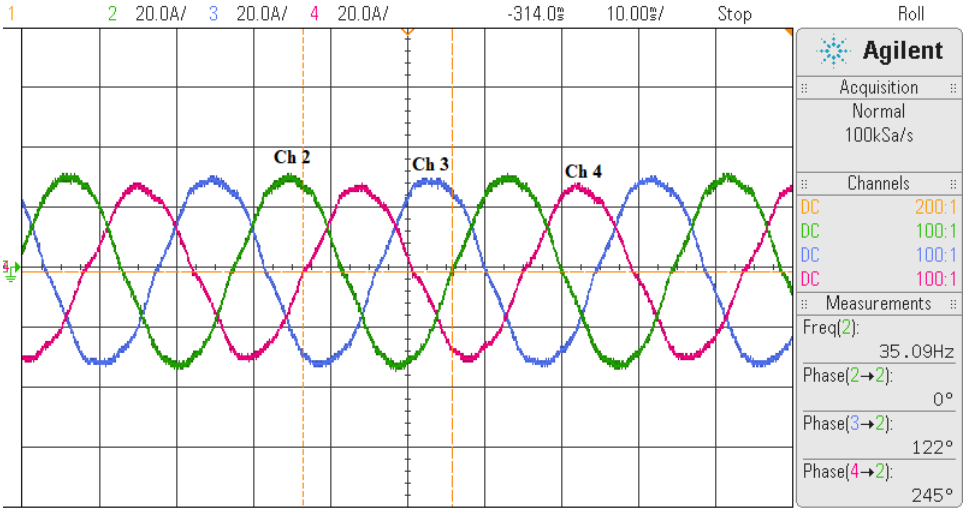

Figure 4.41: *Hardware result*: Currents of phases A, B, C in post-fault condition with modification. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.41 shows oscilloscope waveforms of currents of phases A, B, C in post - fault condition with modification in (233) cell configuration.

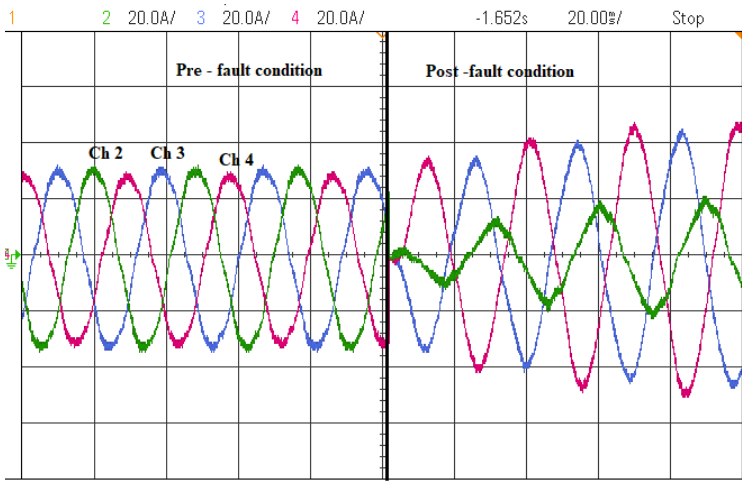

Figure 4.42: *Hardware result*: Currents of phases A, B, C in pre - fault condition and post- - fault condition without modification. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.42 shows oscilloscope waveforms of currents of phases A, B, C in pre fault condition and post - fault condition without modification in (233) cell configuration.

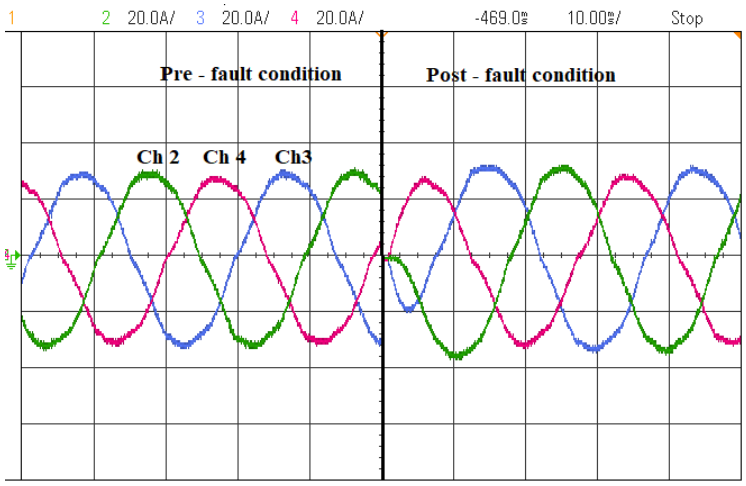

Figure 4.43: *Hardware result*: Currents of phases A, B, C in pre - fault condition and post- - fault condition with modification. *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.01s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.43 shows oscilloscope waveforms of currents of phases A, B, C in pre fault condition and post - fault condition with modification in (233) cell configuration.

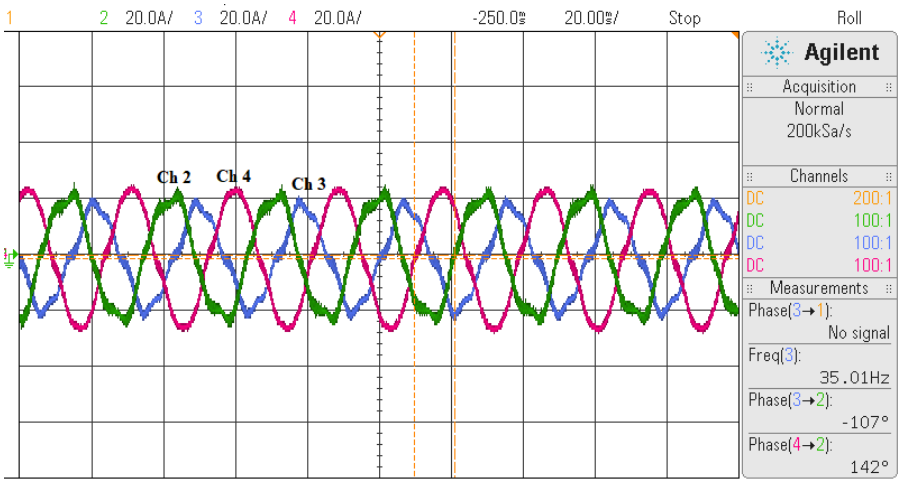

Figure 4.44: *Hardware result*: Currents of phases A, B, C in post - fault condition without modification in a vector control drive *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.02s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.44 shows oscilloscope waveforms of currents of phases A, B, C in post - fault condition without modification in (233) cell configuration in a vector control drive.

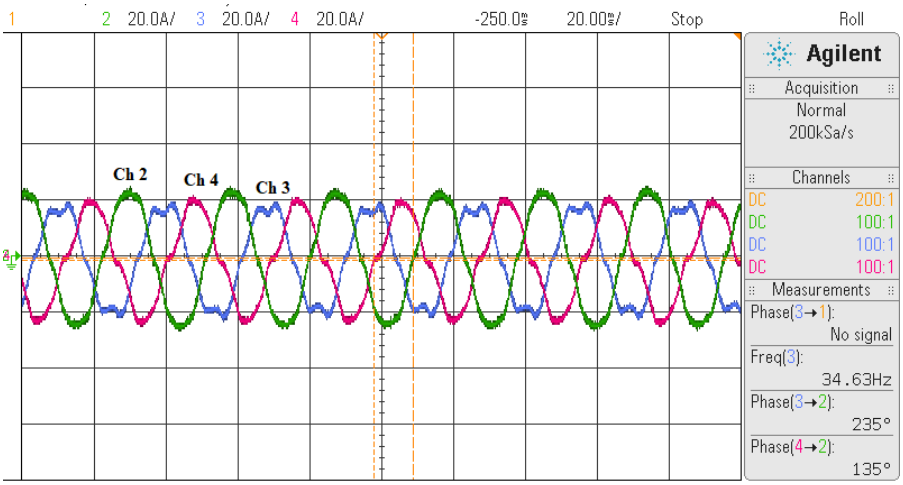

Figure 4.45: *Hardware result*: Currents of phases A, B, C in post - fault condition with modification in a vector control drive *Ch 2 - A phase Current, Ch 4 - B phase Current, Ch 3 - C phase Current (Scale: X-axis: 0.02s/div, Y-axis: Ch2 - 20A/div, Ch3 - 20A/div, Ch4 - 20A/div)*

Figure: 4.45 shows oscilloscope waveforms of currents of phases A, B, C in post - fault condition with modification in (233) cell configuration in a vector control drive.

4.3 Conclusion

The simulation results of 11 level cascaded H bridge inverter fed induction motor drive are discussed. The three different cell - configurations in fault condition are discussed. The simulation results which are obtained validate the theory discussed in chapter 2. In hard ware implementation Hardware results of the 7 level cascaded H bridge inverter fed drive are presented. Simulation and hard ware results validate the method discussed in Scheme 4 which explains about the calculation of the phase angles of the modulating signals in the post fault condition.

CHAPTER 5

Conclusion

5.1 Summary of the present work

Hardware implementation of VVVF control of 30 kW induction machine with a 7-level cascaded H-bridge inverter is done. At the lower speeds, some sub harmonic oscillations are observed. At the higher speeds, the results are satisfactory. Hardware implementation of Vector control of induction machine with 7-level cascaded H bridge inverter is done. The results are satisfactory. The simulation of fault tolerance algorithm was done with a 11 level cascaded H-bridge inverter in a vector control drive. The simulation of fault tolerance algorithm was done for three cell configuration in post condition. The angles were calculated using Scheme 4 which was discussed in chapter 2. Hardware implementation is done on 7 level cascaded H inverter to verify the phase angle calculations and the results are satisfactory. Hardware implementation of fault tolerance algorithm in a vector control drive is done.

5.2 Future scope of work

Problem of sub harmonic oscillations at the lower speeds an be solved. Fault tolerance algorithm can be implemented in a vector control drive for different cell configuration in post-fault condition. In post condition, machine cannot operate at higher speeds. Stabilisation of vector control drive can be done.

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