Interfacing a Gas Sensor using Auto-Balancing Capacitance-to-Pulse-Width-Converter

A Project Report

submitted by

YERRAMSETTY ASHLESHA

EE16B154

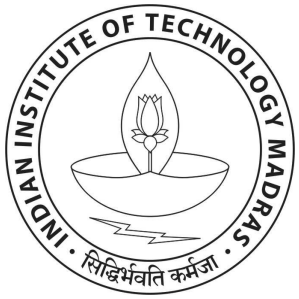
in partial fulfilment of the requirements

for the award of the degree of

BACHELOR OF TECHNOLOGY

&

MASTER OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2021

THESIS CERTIFICATE

This is to certify that the thesis titled **INTERFACING A GAS SENSOR USING AUTO-BALANCING CAPACITANCE-TO-PULSE-WIDTH-CONVERTER** , submitted by **Yerramsetty Ashlesha (EE16B154)**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology & Master of Technology**, is a bonafide record of the project work done by her under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Prof.Boby George
Project Guide
Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date: June 2021

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I am thankful to my family and friends at IIT Madras, who have always unconditionally supported and encouraged me. I thank the IIT Madras community for the great experience in this institute. Above all, I thank the Almighty for the person that I am today.

ABSTRACT

Over the past five decades, there has been an increasing demand for inexpensive, accurate and reliable gas sensors. Nanosized gas sensor elements are potentially faster, require lower power, operate at lower temperatures, obviate the need for expensive catalysts. Nanostructured Metal oxide semiconductors(MOS) are the most commonly used materials for gas sensing. Advanced nano- or micro–nanogas sensors have attracted much attention owing to a variety of possible applications.

In this thesis, we first discuss the possible implementation of a gas sensor using MOS semiconductors whose membrane is coated with nano powder. When the membrane is exposed to LPG gas there will be accumulation on the membrane and it's resonance frequency changes. Later we use a capacitance to pulse width converter that uses sinusoidal excitation which can help in working of gas sensor. This circuit provides the difference between capacitors as pulse width. From this PWM signal, a ratiometric output is obtained for a differential sensor. The interfacing circuit has been designed an it's functionality and performance have been studied in this work.

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ABBREVIATIONS

PWM	Pulse Width Modulation
CPC	Capacitance to Pulse Width Converter
LPF	Low Pass Filter

CHAPTER 1

INTRODUCTION

1.1 Background

Gas sensors are used to detect and identify different types of gases. They are most commonly used for detecting toxic gases and gas concentration. Gas sensors are often employed in factories to detect gas leaks and to detect smoke and Carbon monoxide in homes. There are various types of gas sensors Metal Oxide based gas sensor, Optical gas sensor, Electrochemical gas sensor, Capacitance-based gas sensor.

A Capacitance based gas sensor consists of an insulating substrate, a metal electrode and a micro thin-film heater wire which are formed on the same layer as insulating substrate. Nano powder layer is coated on metal electrode and micro thin-film heater wire for detection of gases. The capacitance based gas sensor is easy to fabricate and have excellent characteristics high sensitivity, high selectivity, high stability, and low power consumption[1].

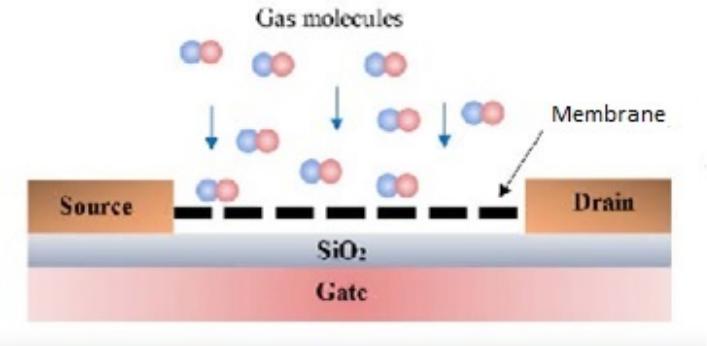

Figure 1.1: Capacitance based Gas Sensor[2]

1.2 Method and Objective

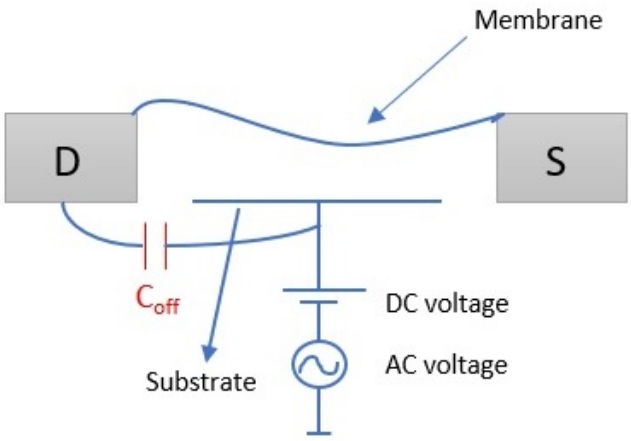

Figure 1.2: Gas Sensor with coated membrane

The membrane in Figure 1.2 is coated with nano powder which causes accumulation when exposed to LPG gas. The membrane's resonance frequency should alter as a result of this accumulation. When there is accumulation on membrane, it results in a capacitance between substrate and membrane say C_x; however, the distance between membrane and substrate can be fabricated only in microns which will result in a very small C_x due to large distance. To overcome this, a DC voltage is given to substrate, which pulls the membrane down, increasing capacitance C_x. The measurement sensitivity of this capacitance has improved.

An AC voltage is applied to ensure the flow of current, which can be measured using an ammeter. This current through ammeter is a function of C_x. As a result of the gas accumulating on the nano powder coated membrane, we have C_x, which can be measured using an ammeter.

Issue : There is also an offset capacitance C_{off} between the substrate and the drain, in addition to the capacitance C_x between the substrate and the membrane caused by accumulation. Because the offset capacitance is typically much higher than C_x, it can't be ignored and causes ammeter readings to alter.

To solve the problem of offset capacitance, we can have two structures, one sensitive to gas and the other not. The structure with coated nano powder is sensitive to gas, whereas the one without coating is not. C_x and C_{off} will be present in the coated structure, whereas only C_{off} will be present in the non-coated structure.

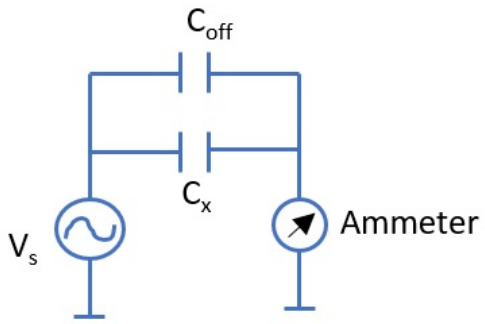

Figure 1.3: Sensor model with nano coating

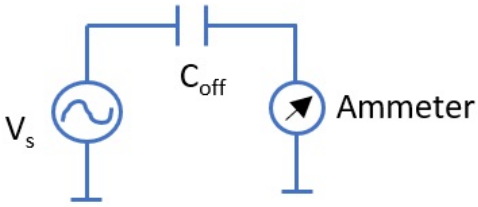

Figure 1.4: Sensor model without nano coating

The gas sensor model in Figure 1.3 has a nano powder coating on its membrane. Capacitance Cx is sensitive to the amount of gas deposited on the membrane. Coff will account for a considerable amount of the current measured by an ammeter, while Cx will account for a smaller percentage. For our application, we are solely interested in Cx. As a result, we build a model that is not sensitive to gas, as illustrated in Figure 1.4. We can get the ammeter current for capacitance Cx alone by taking the difference between these two values.

For this purpose we employ an auto-balancing capacitance to pulse width converter with two variable capacitances, and the resulting PWM waveform is a function of these capacitances. C_1 and C_2 are the two variable capacitances. For our application we can consider

$$C_1 = C_x + C_{off} \tag{1.1}$$

$$C_2 = C_{off} \tag{1.2}$$

CHAPTER 2

CAPACITANCE TO PULSE-WIDTH CONVERTER

In this chapter we discuss about the working of capacitance to pulse width converter and some modifications done to it.

2.1 Schematic

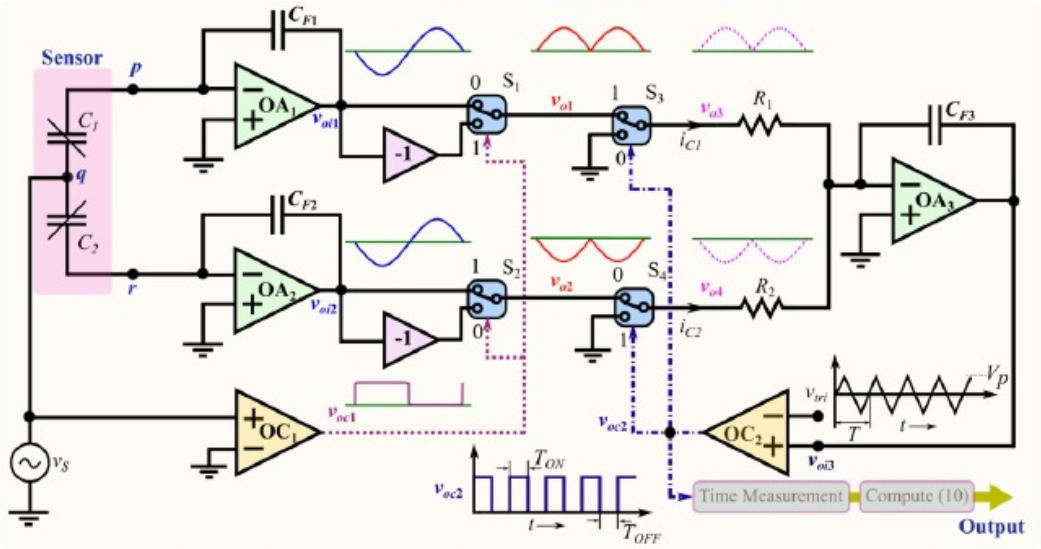

Figure 2.1: Simplified Circuit diagram of CPC[3]

OA_1, OA_2 - Charge Amplifiers

OA_3 - Difference Integrator

OC_1, OC_2 - Comparators

S_1, S_2, S_3, S_4 - Switches

2.2 Working

The circuit diagram of proposed CPC is shown in Figure 2.1. Here, the variable capacitances C_1 and C_2 represent the differential capacitive sensor. The circuit is excited by a sinusoidal voltage signal v_s whose frequency is f_s. The maximum frequency at which C_1 and C_2 change is assumed to be much less compared to f_s. OA_1, C_1, C_{F1} constitute a charge amplifier i.e amplitude of v_{oi1} is amplified when compared to v_s. Similarly OA_2, C_2, C_{F2} also constitute a charge amplifier.

$$v_{oi1} = -v_s . \frac{C_1}{C_{F1}} \tag{2.1}$$

$$v_{oi2} = -v_s . \frac{C_2}{C_{F2}} \tag{2.2}$$

v_{oi1}, v_{oi2} are processed by switches S_1 and S_2 respectively and two unidirectional voltage signals of opposite polarity v_{o1}, v_{o2} respectively are obtained. Both S_1 and S_2 are controlled by v_{oc1} which is the output of comparator OC_1. The inputs of OC_1 are v_s at non-inverting terminal and ground at inverting terminal. When v_s is greater than 0, v_{oc1} is high and when v_s is less than 0, v_{oc1} is low. Thus v_{oc1} is a square wave with frequency f_s same as that of v_s.

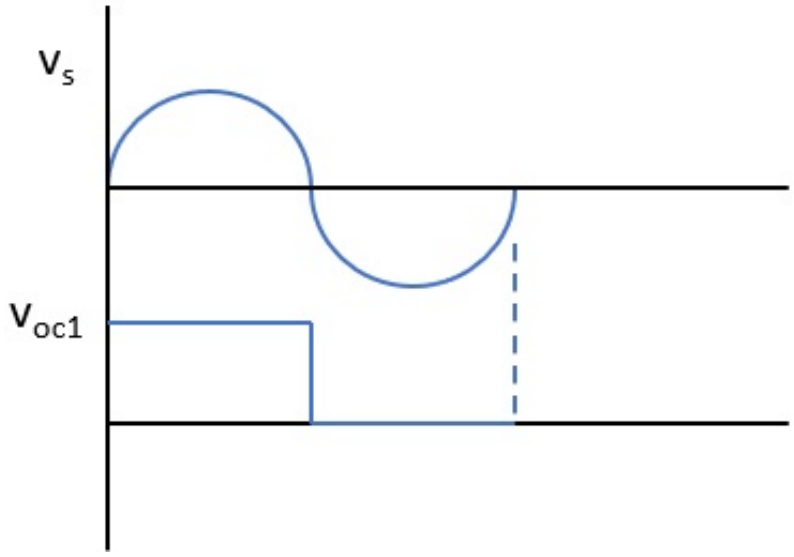

Figure 2.2: Working of Comparator OC_1

When v_{oc1} is low, switch S_1 and S_2 are at position 0. Thus $v_{o1} = v_{oi1}$ and $v_{o2} = -v_{oi2}$. When v_{oc1} is high, switch S_1 and S_2 are at position 1. Thus $v_{o1} = -v_{oi1}$ and $v_{o2} = v_{oi2}$. The waveforms of these signals can be seen in Figure 2.1. These signals are fed into S_3 and S_4 respectively. S_3 and S_4 are controlled by v_{oc2} which is the output of comparator OC_2. When v_{oc2} is low, S_3 and S_4 are at position 0. Thus $v_{o3} = 0$, $v_{o4} = v_{o2}$. When v_{oc2} is high, S_3 and S_4 are at position 1. Thus $v_{o3} = v_{o1}$, $v_{o4} = 0$. v_{o3} and v_{o4} are inputs via R_1 and R_2 into inverting terminal of OA_3. The non-inverting terminal of OA_3 is connected to ground. R_1, R_2, OA_3 along with the feedback capacitor C_{F3} form an inverting summing amplifier. Output of OA_3 is v_{oi3}.

$$\frac{v_{o3}}{R_1} + \frac{v_{o4}}{R_2} = -v_{oi3}.(sC_{F3}) \tag{2.3}$$

$$v_{oi3} = \frac{-1}{sC_{F3}}.[\frac{v_{o3}}{R_1} + \frac{v_{o4}}{R_2}] \tag{2.4}$$

Voltage v_{oi3} is given to non-inverting terminal of OC_2. A reference triangular waveform v_{tri} with time period $T = \frac{1}{f_{tri}}$ is given to inverting terminal of OC_2. The pulse width of v_{oc2} depends on v_{oi3} and v_{tri}. When $v_{oi3} > v_{tri}$, v_{oc2} is high and when $v_{oi3} < v_{tri}$, v_{oc2} is low. The frequency of v_{tri}, f_{tri} is set such that $f_{tri} \gg f_s$. Thus during one cycle of v_{tri} v_{oi3} is almost constant. Thus v_{oi3} can be assumed to be DC during one cycle of v_{tri}. When $v_{oi3} = 0$, the pulse width of v_{oc2} is $\frac{T}{2}$ and the duty cycle D = 0.5. T_{ON} is the duration for which v_{oc2} is high and T_{OFF} is the duration for which v_{oc2} is low. Thus $T = T_{ON} + T_{OFF}$.

The currents through R_1 and R_2 are i_{c1} and i_{c2} respectively. The average current $\overline{i_{c1}}$ is proportional to C_1 and $\overline{i_{c2}}$ is proportional to C_2.

When $C_1 = C_2$ then $\overline{i_{c1}} = -\overline{i_{c2}}$, thus $v_{oi3} = 0$. And

$$v_{oi3} = \frac{-1}{C_{F3}}.\int_0^{T_s}(i_{c1} + i_{c2})dt \tag{2.5}$$

When $C_1 < C_2$, then $|\overline{i_{c1}}| < |\overline{i_{c2}}|$ and $\overline{i_{c2}}$ is negative. Thus $i_{c1} + i_{c2} < 0$ which implies v_{oi3} is positive.

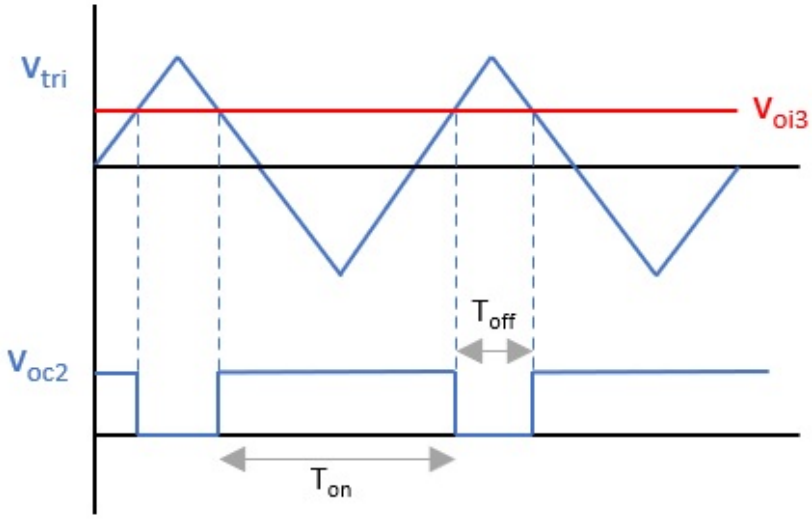

Figure 2.3: Working of OC_2 when $C_1 < C_2$

As shown in Figure 2.3, $T_{on} > T_{off} \implies$ duty cycle D increases. Since v_{oc2} is 1 for more duration, v_{o1} is passed more compared to v_{o2}. This will cause an increase in $|\overline{i_{c1}}|$ and it continues till $\overline{i_{c1}} = -\overline{i_{c2}}$. When this condition is met the the loop reaches Steady State.

When $C_1 > C_2$, then $|\overline{i_{c1}}| > |\overline{i_{c2}}|$ and $\overline{i_{c2}}$ is negative. Thus $i_{c1} + i_{c2} > 0$ which implies v_{oi3} is negative.

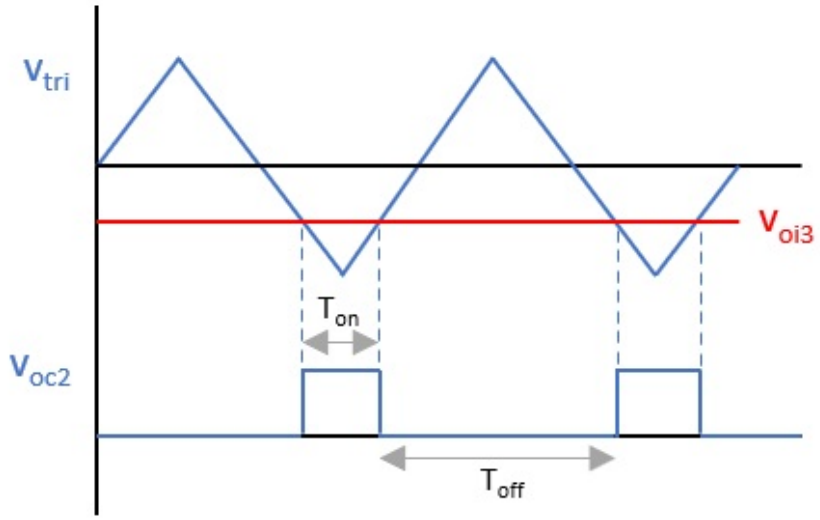

Figure 2.4: Working of OC_2 when $C_1 > C_2$

As shown in Figure 2.4, $T_{on} < T_{off} \implies$ duty cycle D reduces. Since v_{oc2} is 0 for more duration, v_{o2} is passed more compared to v_{o1}. This will cause an increase in $|\overline{i_{c2}}|$ and it continues till $\overline{i_{c1}} = -\overline{i_{c2}}$. When this condition is met the the loop reaches Steady State. As already mentioned during steady state i.e when $\frac{d(v_{oi3})}{dt} = 0$, i_{c1} and i_{c2} are related as follows

$$\overline{i_{c1}} = -\overline{i_{c2}} \tag{2.6}$$

Considering $\overline{i_{c1}}$ directly proportional to C_1 and D, $\overline{i_{c2}}$ directly proportional to C_2 and (1-D), equation (2.6) can be re-written as

$$C_1 \times D = C_2 \times (1 - D) \tag{2.7}$$

Re-arranging C_1 and C_2 and expressing equation (2.7) in terms of T_{on} and T_{off} gives

$$\frac{C_1}{C_2} = \frac{T_{off}}{T_{on}} \tag{2.8}$$

Further modifying into ratiometric form equation (2.8) becomes

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{T_{off} - T_{on}}{T_{off} + T_{on}} \tag{2.9}$$

2.3 Addition of 2nd order LPF

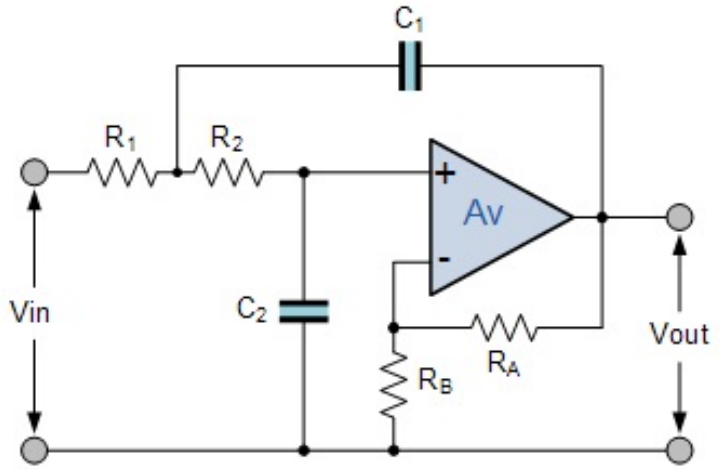

Figure 2.5: Schematic of 2nd order LPF[4]

A 2nd order LPF is added at the output of OA_3 to filter out the ripples in v_{oi3}. This filtered v_{oi3} is sent to the non-inverting terminal of comparator OC_2.

Figure 2.5 represents a Sallen Key 2nd order LPF. The filter design includes a non-inverting op-amp configuration so the filters gain, A will always be greater than 1. Also the op-amp has a high input impedance so it can be cascaded in any part of circuit without altering the circuit's functioning. A 2nd order LPF is prefered over 1st order LPF due to it's higher stop band roll-off which is 40 dB/decade. Th cut-off frequency(f_c) above which filtering occurs is

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \tag{2.10}$$

If $R_1 = R_2$ and $C_1 = C_2$ then

$$f_c = \frac{1}{2\pi RC} \tag{2.11}$$

CHAPTER 3

SIMULATION RESULTS

3.1 Results with ideal components

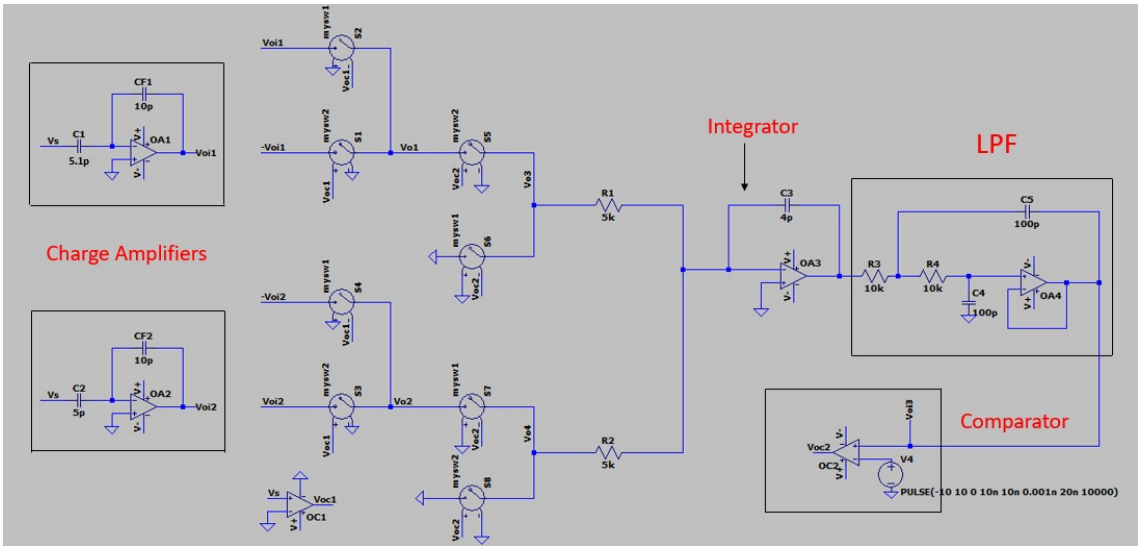

Figure 3.1: Schematic of the proposed CPC

As shown in Figure 3.1, we have considered C_1 = 5.1 pF, C_2 = 5 pF. The following are the component values used in simulation

C_{F1} = 10 pF, C_{F2} = 10 pF, C_{F3} = 4 pF

R_1 = 5 kΩ, R_2 = 5 kΩ

f_s (Frequency of sinusoidal excitation) = 10 kHz

f_{tri} (Frequency of triangular waveform) = 50 MHz

When C_1 = 5 pF and C_2 = 5.1 pF, the average value of v_{oi3} = 0.1004 V

Here $C_1 < C_2$, thus v_{oi3} is positive.

When C_1 = 5.1 pF and C_2 = 5 pF, the average value of v_{oi3} = -0.0952 V

Here $C_1 > C_2$, thus v_{oi3} is negative.

Case 1 - C_1 = 5 pF, C_2 = 10 pF

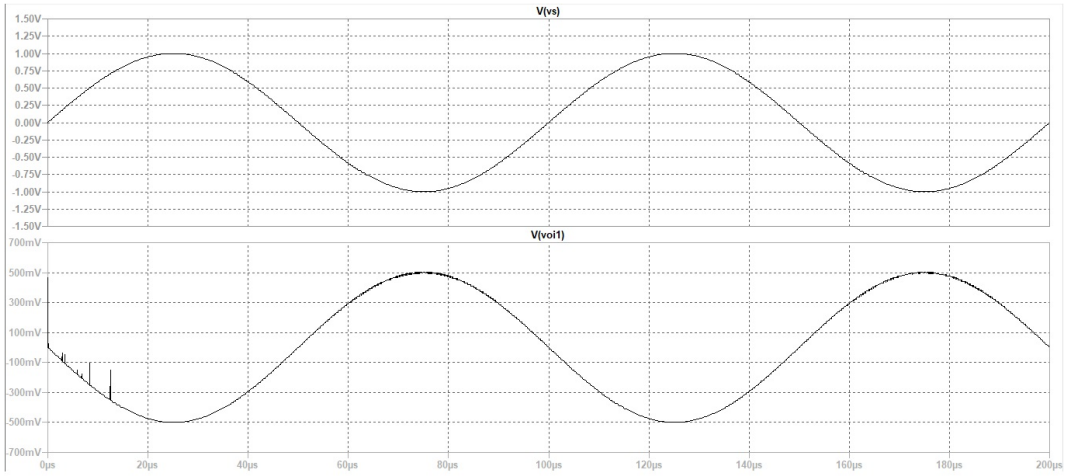

Figure 3.2: Graph plotting v_s and v_{oi1} vs time

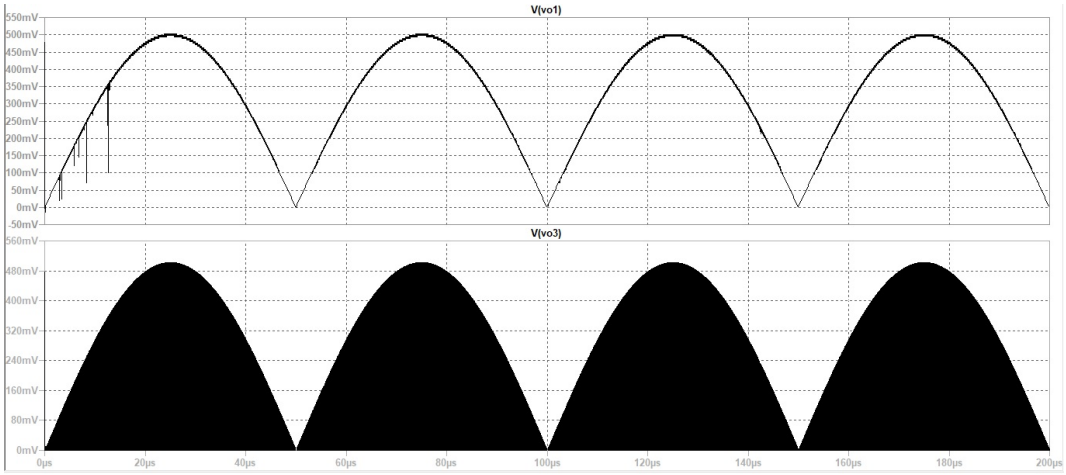

Figure 3.3: Graph plotting v_{o1} and v_{o3} vs time

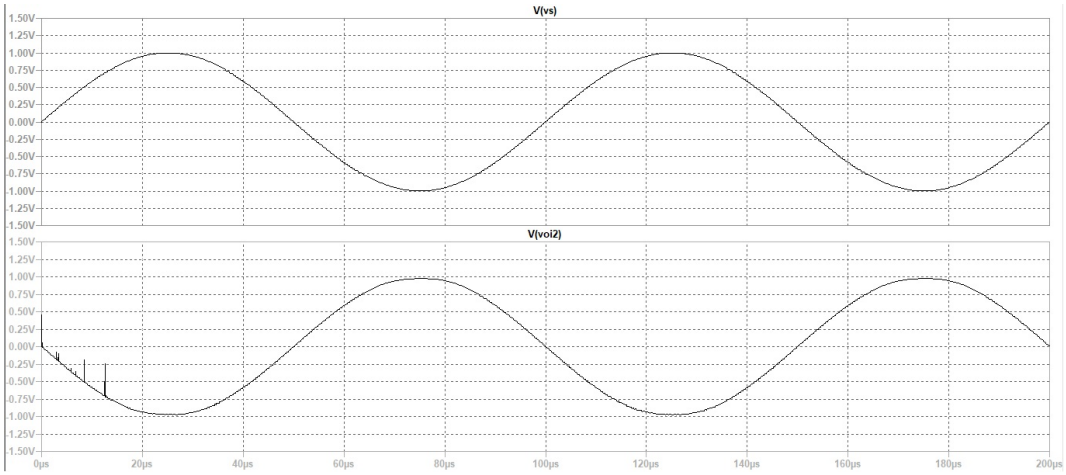

Figure 3.4: Graph plotting v_s and v_{oi2} vs time

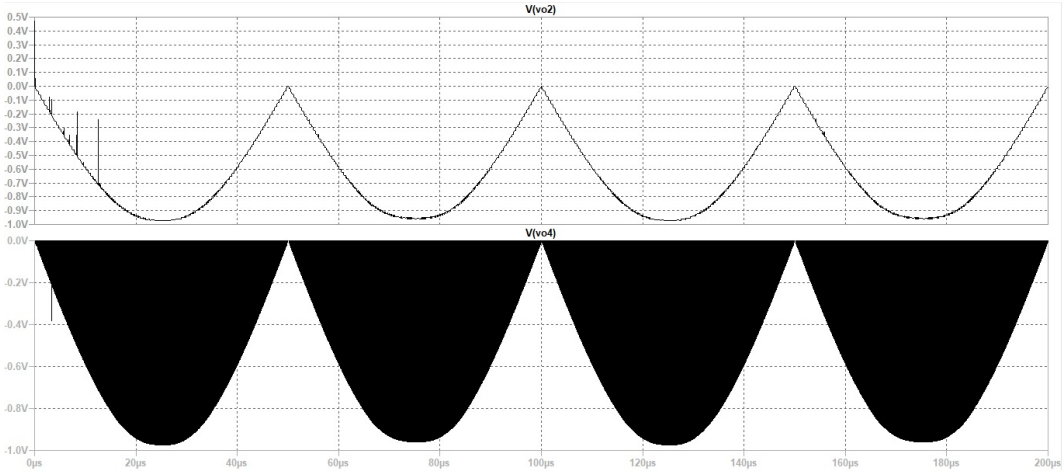

Figure 3.5: Graph plotting v_{o2} and v_{o4} vs time

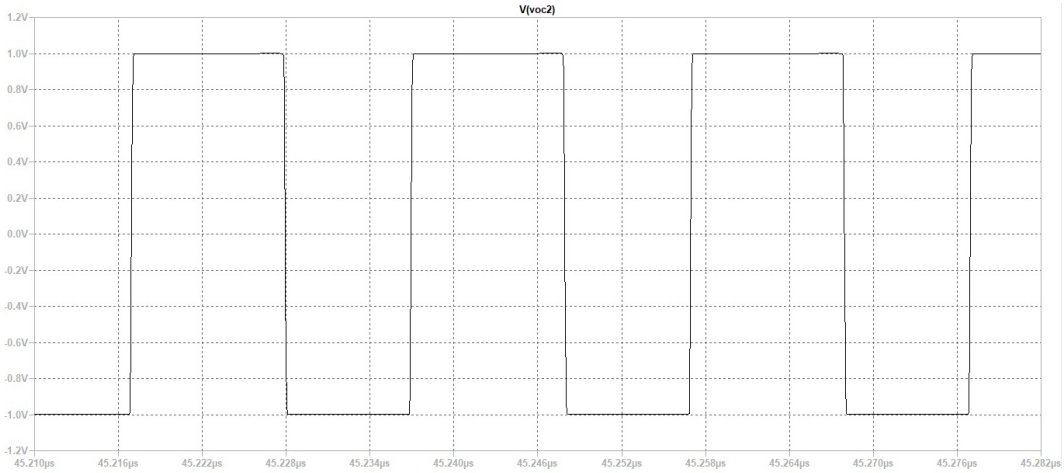

Figure 3.6: Graph plotting v_{oc2} vs time

As considered earlier when $C_1 < C_2$, duty cycle of v_{oc2} increases. From Figure 3.6 we can infer that $T_{ON} > T_{OFF}$. Hence our simulations are equivalent to our considerations.

Case 2 - C_1 = 10 pF, C_2 = 5 pF

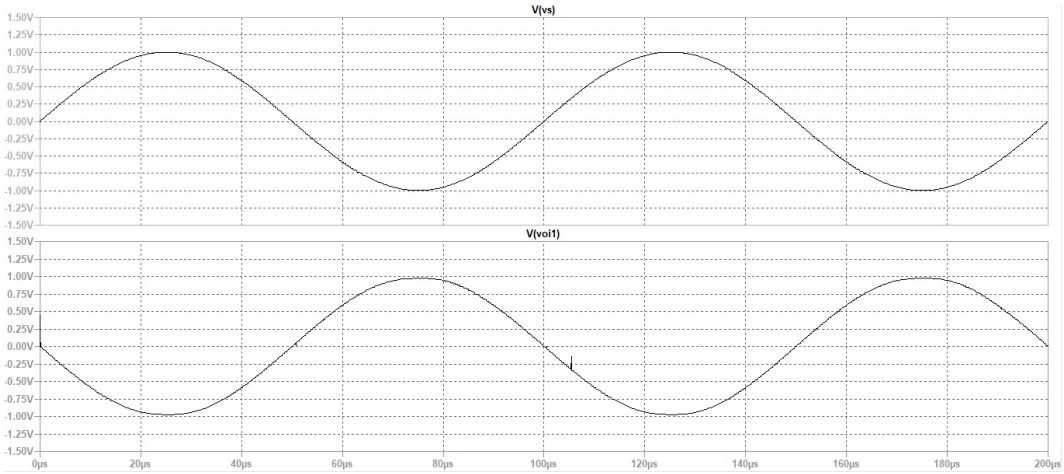

Figure 3.7: Graph plotting v_s and v_{oi1} vs time

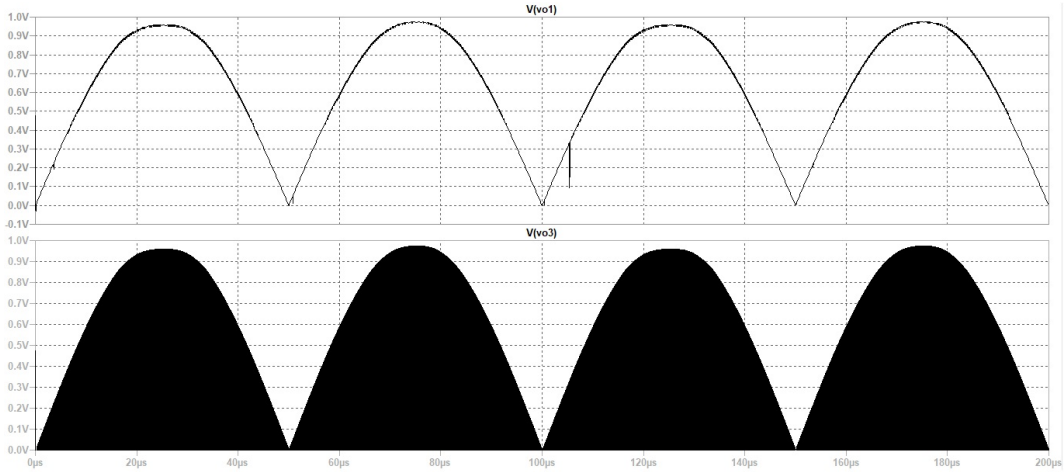

Figure 3.8: Graph plotting v_{o1} and v_{o3} vs time

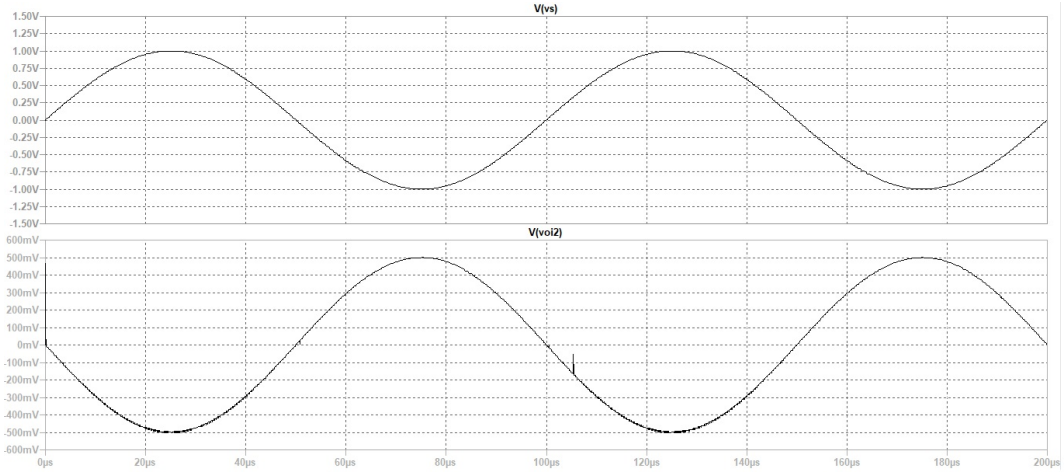

Figure 3.9: Graph plotting v_s and v_{oi2} vs time

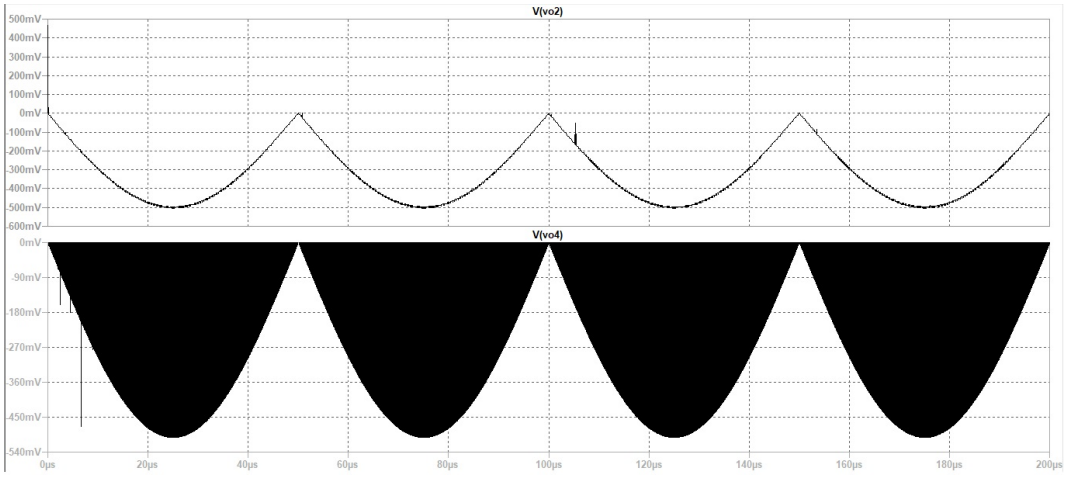

Figure 3.10: Graph plotting v_{o2} and v_{o4} vs time

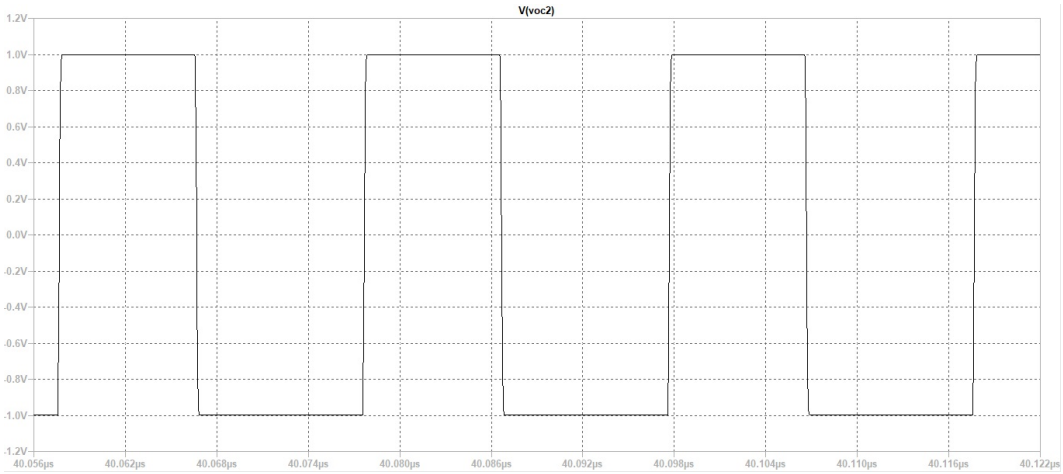

Figure 3.11: Graph plotting v_{oc2} vs time

As considered earlier when $C_1 > C_2$, duty cycle of v_{oc2} reduces. From Figure 3.11 we can infer that $T_{ON} < T_{OFF}$. Hence our simulations are equivalent to our considerations.

3.2 Noise

Noise is an unwanted disturbance in electrical signal. There are different types of noise generated by different processes. They are

Thermal Noise

Shot Noise

Flicker Noise

Noise is a random process which is characterized by stochastic properties such as it's variance, distribution, and spectral density. Noise voltage density can be expressed in volts per root hertz(V/$\sqrt{Hz}$)[5].

In our simulation a random noise source is added at input of the circuit to know it's effect at output i.e at v_{oi3}. All the resistors are considered noisy and all ideal opamps are replaced by AD8618.

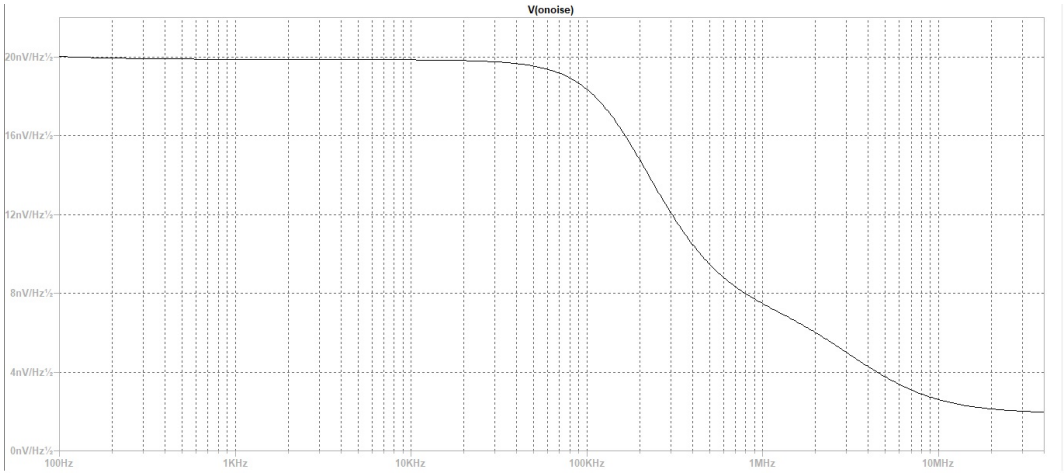

Figure 3.12: Graph plotting effective circuit noise at v_{oi3}

3.3 Charge Injection

MOSFETs are used as switches in our circuit. These MOSFETs must be biased to alter between cut-off and saturation states in order to function as switches. There is no current flow through the device during cut-off, and there is a constant flow of current through the device during saturation, emulating the behaviour of open and closed switches, respectively[6].

When used as switches, MOS devices have some non-idealities. One of them is Charge Injection. The gate capacitance of MOSFETs causes this. The movement of charges in the gate-source and gate-drain capacitance injects or subtracts charge from the conduction channel when the gate voltage is altered to turn the switch on or off (depending upon the gate polarity change). This manifests itself as a voltage spike in the signal carried by the MOSFET. Thus to reduce charge injection, use MOSFETs with the minimum feasible gate capacitance, which is usually the smallest MOSFET device with a low enough ON resistance for the signal being switched.

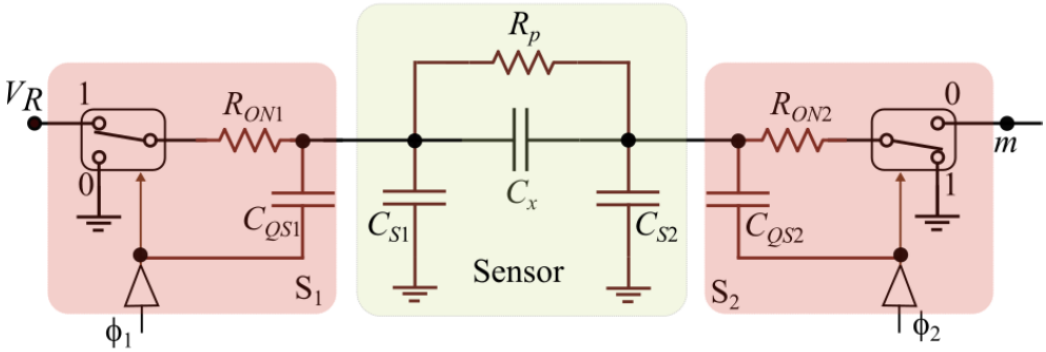

Figure 3.13: Schematic showing charge injection[7]

As shown in Figure 3.13, when $\phi_1$is high C_{QS1} charges and injects the same charge into the network. When ϕ_1 is set to a low value, it again discharges to the rest of the network.

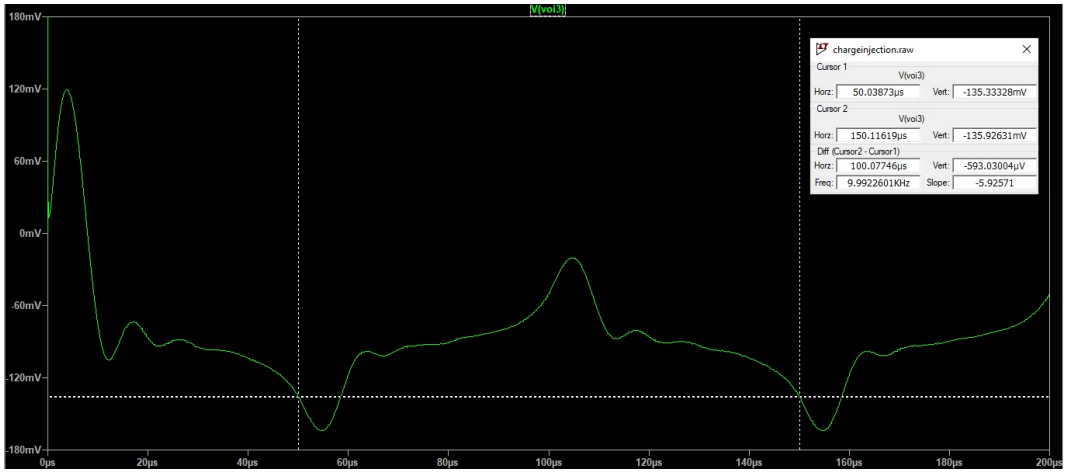

Figure 3.14: Graph plotting v_{oi3} when C_{QS1} = 0 pF

We can observe from Figure 3.14 that v_{oi3} repeats itself every 100 μs. As a result, all the simulations are run for 160 μs, and data is saved from 60 μs to 160 μs.

Consider C_1 = 5.1 pF and C_2 = 5 pF. When

C_{QS1} = 0 pF then Avg(v_{oi3}) = -0.0952 V
C_{QS1} = 10 pF then Avg(v_{oi3}) = -0.0933 V
C_{QS1} = 12 pF then Avg(v_{oi3}) = -0.09062 V
C_{QS1} = 13 pF then Avg(v_{oi3}) = -0.0895 V

Consider C_1 = 5 pF and C_2 = 5.1 pF. When

C_{QS1} = 0 pF then Avg(v_{oi3}) = 0.1004 V
C_{QS1} = 10 pF then Avg(v_{oi3}) = 0.1059 V
C_{QS1} = 12 pF then Avg(v_{oi3}) = 0.1093 V
C_{QS1} = 13 pF then Avg(v_{oi3}) = 0.1125 V

As can be seen from the preceding data, when C_{QS1} surpasses 12 pF, the average value of v_{oi3} changes at the second decimal point. As a result, the highest value of C_{QS1} that the circuit can tolerate without causing measurement error is 12 pF.

CHAPTER 4

CONCLUSION

In this project, an auto-balancing capacitance to pulse-width converter is simulated and it's use in the operation of gas sensor is presented. The suggested CPC uses sinusoidal excitation and provides a linear output. It is unaffected by parasitic capacitance, and non-idealities such as offset voltage, bias current, and charge injection have negligible impact. Many capacitive-based systems use sinusoidal AC excitation, and the CPC described in this research provides an efficient way to digitise the capacitive sensor output in these applications. Using this CPC, we can design a low-cost nano powder-coated gas sensor.

APPENDIX A

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