TIMING ANALYSIS-HIERARCHY AND POWER ESTIMATION OF CORES IN ASIC AND FPGA

A Project Report

submitted by

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in partial fulfilment of the requirements
for the award of the degree of

MASTER OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2017

THESIS CERTIFICATE

This is to certify that the thesis titled "**Timing Analysis-Hierarchy and Power Estimation of Cores In ASIC and FPGA"**, submitted by **BANAVATH VALYA** , to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology(Microelectronics and VLSI design)**, is a bonafide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 19th June 2017

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude towards Prof.Dr.Nitin Chandrachoodan for backing and guiding me throughout the journey of this project.He gave me enough space and freedom to explore my ideas,pursue and tackle so turned out to be interesting problem statements.His immense knowledge in both software and hardware has helped me into getting out-of-the-box perspectives and interesting insights into the project,which only rose the bar of what we aimed at achieving ,one step at a time.

I thank my friends Bibin basheer, Ravi chandra, Nagaraju and Shivani who were with me throughout the project

Lastly and most importantly, I owe my accomplishments to my beloved parents, who always stood by me.They are and always have been my source of inspiration,motivation for hard work and self-belief. I am deeply grateful to them for believing in me and shaping me into what i am today. Seeing them content and proud of my achievements makes this all worthwhile.

ABSTRACT

KEYWORDS: ASIC and FPGA.

In-order to create a robust design,all chips must pass the timing checks and meet user specified timing constraints before fabrication. Statistical timing analysis is a method of validating the timing performance of the design by checking all possible paths for timing violations under worst case conditions.

Power has always been a design consideration, though a lower priority has been given to power than the most of the variables(Speed/Performance,risk,etc). Power translates to significant system cost. FPGA's can be significantly aid the design in reducing the challenges associated with power consumption.The power dissipation in ASIC comprised of power in the digital core logic, memories , analog macros and other IO interfaces.The power dissipation in the digital logic and memory macros can be due to switching activity, called active power, and the leakage power which is present even with zero switching activity in the design.

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ABBREVIATIONS

IITM	Indian Institute of Technology, Madras
RTFM	Read the Fine Manual
FPGA	Field Programmable Gate Array
ASIC	Application Specific Integrated circuits
STA	Static timing analysis
DTA	Dynamic timing analysis
SSTA	Statistical Static timing analysis
DRC	Design check rule

CHAPTER 1

INTRODUCTION

1.1 Introduction

As the increase in complexity of digital designs and the requirements in various design stages make static timing analysis critical. Each design stage utilizes static timing analysis to evaluate the system performance, and then optimizes the design accordingly. An accurate and efficient timing analysis package is crucial for the success of whole design process. Timing is important because just designing the chip is not enough , we need to know how fast the chip is going to run, how fast the chip is going to interact with other chips, how fast the input reaches the output.

Timing analysis is used to perform the timing constraints of the design . Timing verification is an important phase in timing analysis as incorrect constraints lead to chip failures. Logic circuits generally consists of large number of paths through which signals cannot propagate in functional mode analysis, these paths are known as unsensitizable paths, or simply false paths. Timing analysis tools can report true critical and false paths . The critical paths reported by the timing tools may or may not be synthesizable. In ASIC timing analysis can be applied in both pre-layout and post lay-out. In pre-layout delay calculation is an estimation of the incorrect delay values. In post-layout timing analysis the delays values are accurate. Morever static timing analysis cannot provide the details of how many critical paths exist in the circuit. A path can also be called as false path if the transitions on the input cannot be propagated to the output along the path. If any one false critical path is right regarded as the a critical path, the results are conservative and the performance of the circuit would be affected. There may be 30 percent of paths in the circuit that are reported as false paths.

Power is always been a design consideration , though a lower priority has been given to power than the most of the variables (Speed/ Performance ,risk etc.). Power translates to significant system cost. FPGAs can be significantly aid the design in reducing the challenges associated with power consumption.

The power dissipation in ASIC comprised of power in the digital core logic, memories, analog macos and other IO interfaces.

1.2 Motivation

Motivation behind this tool is to facilitate an open-source unified academic timing engine that performs timing analysis and to enable timing driven flows.
Many commercial tools like Synopsis,Cadence design compiler are well known and widely used industry-wide as well as in academia for timing verification of digital designs at various stages of VLSI design flow.

1.3 Objectives and Contributions

Following points highlights the objectives of this thesis:
1. To understand how ASIC and FPGA size changes with the timing constraint.
2. To estimate how power changes with the timing constraint in ASIC and FPGA.
3. Compare results of ASIC and FPGA and understand the similarities .
4. To know what is logic depth(Gates in critical path from input to output).

In this thesis, we present how the size (Number of Gates, FF, IO, BUFG) changes with timing constraints, the resource available and how much resource is utilized including percentage of resource utilized is also mentioned in the thesis. Power is calculated in both ASIC and FPGA, In FPGA total on-chip power, Dynamic power(Power utilized for clocks, Logic, Signals , IO) and device static power are estimated for various timing constraint and how the power is changing with variation of timing constraint is reported. Also in FPGA,static timing analysis which includes Worst neative slack, Total negative slack , Number of failing end points, Total number of failing end points , Path delay, Logic delay, Net delay , Clock skew , Slack , High fan-out, cumulative fan-out for critical setup path and critical hold path are reported. Power and delay analysis framework is necessary for FPGA power and delay optimization.
In ASIC Changes in size(Gates) with changes in time period is studied, Variation of leakage power and Total power with changes in timing constraint is reported and timing

slack is calculated for various clock periods and the clock period at which the timing slack becomes 0 is reported.

1.4 Organization of thesis

The rest of the thesis is organized in the following manner:

chapter2: Background

This chapter discusses the related work, definitions involved along the theoretical background on timing analysis, power and Hierarchy.

chapter3: Timing Analysis

This chapter discusses how timing verification is important phase in timing analysis. How fast the chip is going to interact with other chips, how fast the chip is going to run, how fast input reaches the output.

Chapter4: Power in FPGA and ASIC

This chapter discusses the basic understanding of power and how the power varies with timing constraint in ASIC and FPGA.

Chapter5: Results and Discussions

The synthesis results of both ASIC and FPGA are reported and discussed how power and Size Of ASIC and FPGA changes with timing constraint.

Chapter6 : Conclusions

CHAPTER 2

Background

Miniaturization of transistor size comprises in increasing the complexity of digital designs. So, timing analysis is performed to meet the user specified timing constraints of the design, All chips must pass the timing checks and meet the user specified the timing constraints of the design before fabrication. Static timing analysis is a method of validating the timing performance of the design by checking all possible paths got timing violations under worst-case conditions. The characteristics of static timing analysis only consider the delay of each logic gates and cells in the path and doesn't take functional behaviour of the logic cells into account. All timing paths will not active in real work environment. These paths which are not activated are known as false paths. The traditional static timing analysis results are overly pessimistic. Static timing analysis results are estimation as many critical paths are not true paths and most of the critical paths are false paths or non-functional paths. In classic design flow, the critical path delay is calculated through static timing analysis. This approach may leads to enormous results as static timing analysis cannot accurately calculate path delay of all critical paths

Elimination of false paths provides area and power advantage. Moreover static timing analysis cannot provide the details of how many critical paths exist in the circuit. A path can also be called as false path if the transition on the input cannot be propagated to the output along the path. If any one false critical path is right regarded as a critical path, the results are conservative and performance of the circuit would be affected. There may up to 30% of paths in the circuit are reported as false paths. So, it is predicted that static timing analysis reported in critical paths may be false. The corresponding delay of the circuit may or may not be accurate and overly pessimistic. The main drawback of static time analysis is inability to detect accurate false path automatically and also the number of false critical paths.The other one is static timing analysis is neglect the simultaneous input transitions.

CHAPTER 3

Timing Analysis

3.1 Introduction

High-performance integrated circuits have traditionally been characterized by the clock frequency at which they operate. Gauging the ability of a circuit to operate at the specified speed requires ability to measure its delay at numerous steps during the design process. There are mainly two approaches for timing analysis : Static and dynamic timing analysis.

3.2 Static timing analysis

Static timing analysis is a method of computing the expected timing a digital circuit without requiring circuit level simulation. By giving each circuit component an "associated delay", it doesn't need to test all possible input vectors. In this way, it treats circuit component delay independently as a solution of a whole system. STA therefore greatly reduces the time to compute the delay at the expense of accuracy. On the contrary, dynamic timing analysis uses the circuit simulation and tries on large number of samples of input vectors. Therefore, it is time consuming.
In ASIC design flow static timing analysis is applied in both pre-layout and post-layout. In the synthsis phase all the timing requirements clock, input load, output load and user defined timing constraint are specified. Timing analysis is applied to match the user specified design constraints. In design for testing the phase design check rule (DRC) is performed to identify all the timing violations, and therefore floor planning phase all the timing all the timing violations are removed. After floor planning parasitics are extracted which contains the delay values.

3.3 Critical path

The critical path is defined as the path between an input and output with maximum delay. The critical path can easily be found by using a trace back method.

3.4 Dynamic Vs Static Timing Analysis

- **Timing analysis is an integral part of ASIC/FPGA design flow. It has to be accomplished and the functionality of the design must be cleared before the design is subjected to Static timing analysis. Anything can be compromised but not timing.**

- **In addition to the above discussed STA, dynamic timing analysis(DTA) can be used to verify functionality of the design by applying input vectors and checking for correct output vectors.**

- **In contrast, STA checks static delay requirements of the circuit without any input or output vectors.**

- **Dynamic timing analysis is a circuit level simulation used for the characterization of timing properties of a complete cell, which most of the time is logic gate. Dynamic timing analysis and STA are not alternatives to each other. The quality of the DTA increases of input test vectors. Increased test vectors increase simulation time.**

- **DTA can be used for synchronous as well as asynchronous designs. STA can't run on asynchronous designs and therefore DTA is the best way to analyze asynchronous designs. It is the best suited for designs having clocks crossing multiple domains. Finally, DTA is also carried to on post layout netlist to verify that functionality of the design has not changed . Test vectors remain same for both.**

3.5 Advantages of static Timing Analysis

- **Static timing analysis(STA) considers all the timing paths ,whether it may be functional or non-functional paths. STA analysis is very fast and exhaustive compared to statistical static timing analysis(SSTA) and dynamic timing analysis.**
- **STA is analyzed for best, worst and typical cases, while dynamic simulation it is not possible. Static timing analysis calculates the delay through delay models, STA results are pessimistic in nature and fast. DTA is slow and accurate, as it checks the functionality of the design. DTA is very complex compared to STA.**

3.6 Disadvantages of static Timing Analysis

- **Since STA is pessimistic and considers the false critical path as false critical path is non-functional path. In general STA critical paths are false in nature. If a false path is considered for circuit delay calculation, the output will conservative and results are affected.**
- **STA will add the delay of the gates and logic cells along the path, it doesn't take functionality of the design onto account. STA cannot be applicable to synchronous circuits.**

3.7 Advantages of dynamic Timing Analysis

- **Very accurate but slow and the quality depends on input vectors. Dynamic timing analysis is non-exhaustive.**

CHAPTER 4

Power in FPGA and ASIC

Power has always been a design considerations. Traditionally, though, a lower priority has been assigned to power than to most other variables.
Power consumption in ASIC comprised of power in the digital core logic, memories and IO interfaces.

There are traditionally four power components that are important when considering a design using FPGA products. These are 1. pre-programmed static device power consumption. 2. Inrush programming power consumption . 3. Post-programmed static power consumption. 4. Dynamic power consumption. Pre-Programmed static power consumption is the amount of power consumed by the FPGA prior to the device being programmed. For quiescent device power consumption the FPGA is in a non-programmed state, Yet has been powered. It is important that the device not consume significant power during this time.

Post-Programmed static device power consumption is a very significant component of FPGA power consumption. This is due to the large number of transistors on FPGAs. The leakage on these transistors typically is always on and drawing power whether the transistor is used or not. Typically, Post-programmed static power is equal to the or greater than the previously described quiescent static power. There are some recent innovations addressing power grids and removing power to the transistor,etc., which will impact static power.
Dynamic power is a significant component in power analysis and , depending on the type of design being implemented.

CHAPTER 5

Results and Discussions

5.1 Variation of Power in FPGA with Timing Constraint

5.1.1 Project Core : AES_128

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.316
10	0.279
20	0.261
50	0.249

Table 5.1: Shows Variation of power with timing constraint for the project core AES_128.

5.2 Discussion

The clock period is varied from 5ns to 50ns, Power is decreased from 0.316Watts to 0.249Watts. This clearly indicates that as the timing constraint is increases, power is decreasing gradually for the project core AES_128.

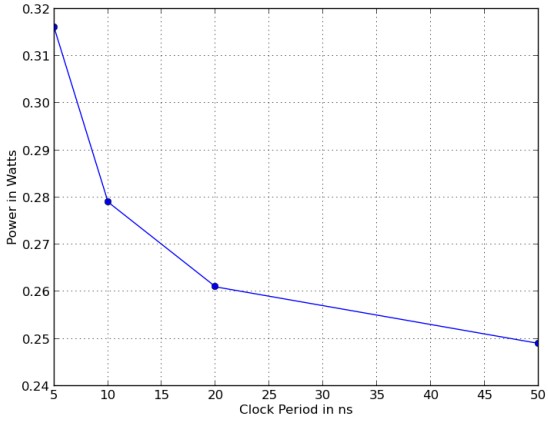

Figure 5.1: Shows Variation of Power with timing constraint from 0ns to 50ns.

5.2.1 Project Core : Configurable Cordic Core

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.316
10	0.279
20	0.261
50	0.249

Table 5.2: Shows Variation of Power with timing constraint from 5ns to 50ns.

5.2.2 Discussion

From the above table, Power is 0.316Watts at clock period 5ns, 0.279Watts at clock period 10ns , 0.261Watts at clock Period 20ns and 0.249Watts at clock Period 50ns. As the clock period varies from 0ns to 50ns, power is decreased from 0.316Watts to 0.249Watts. From the above analysis it clear that as the clock period is increases power decreases gradually.

Same as project core AES_128, Power is decreasing as the timing constraint is keep on increasing for the project core : Configurable Cordic Core. From the power analysis of project core AES_128 and Configurable cordic Core it is clear that as the timing constarint is keep on increasing, Power is decreases in FPGA.

As the timing constraint is varied, Power is also varied that is as the clock poeriod is keep on increasing incase of FPGA , Power is keep on decreasing gradually. From the analysis of the project cores AES_128 and Configurable cordic core it is clear that as the power is keep on decreasing as the clock period is keep on increasing. All tha analysis above also shown graphically from which we can clearly understand how the power is varying with the variation of timing constraint.

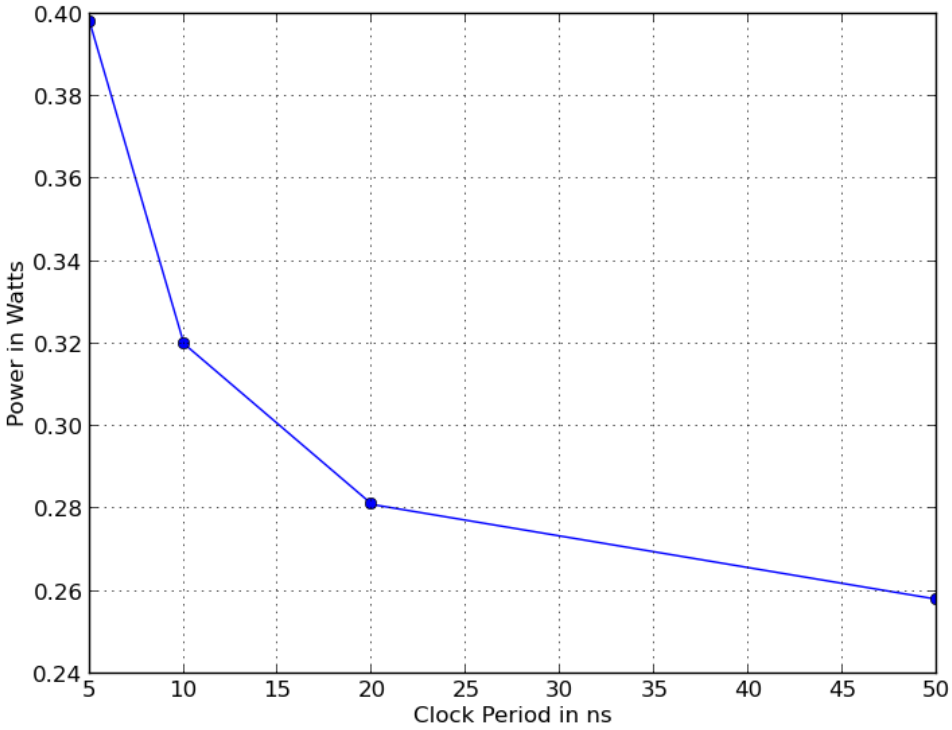

Figure 5.2: Shows Variation of power with timing constraint for the project core Configurable Cordic Core.

5.2.3 Project Core :Cordic polar2rect

The follwing table shows how Power changes with variation of clock periods. :

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.36
10	0.301
20	0.272
50	0.250

Table 5.3: Shows Variation of Power with timing constraint from 0ns to 50ns.

From the above table, Power is 0.36Watts for the clock period 5ns, 0.301Watts for the clock period 10ns, 0.272Watts for the clock period 20ns and 0.250Watts for the clock period 50ns. As the clock period is keep on increasing from 5ns to 50ns, power is decreased from 0.36Watts to 0.250Watts. From the above analysis it is clear that as the timing constraint is keep on increasing power is decreasing gradually in case of FPGA.

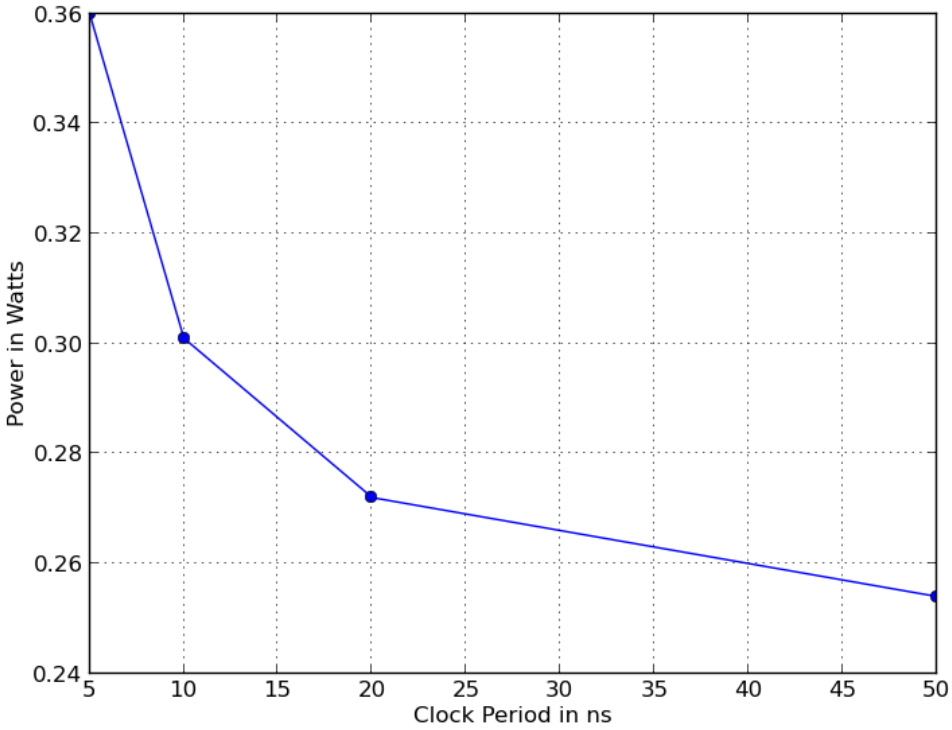

Figure 5.3: Shows Variation of power with timing constraint for the project core Cordic polar2rect.

5.2.4 Project Core :Cordic rect2polar

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.402
10	0.322
20	0.282
50	0.258

Table 5.4: Shows Variation of Power with timing constraint from 0ns to 50ns.

Discussion :

From the above table, Power is 0.402Watts for the clock period 5ns, 0.322Watts for the clock period 10ns, 0.282Watts for the clock period 20ns and 0.258Watts for the clock period 50ns. As the clock period is keep on increasing from 5ns to 50ns, power is decreased from 0.402Watts to 0.258Watts. From the above analysis it is clear that as the timing constraint is keep on increasing power is decreasing gradually in case of FPGA.

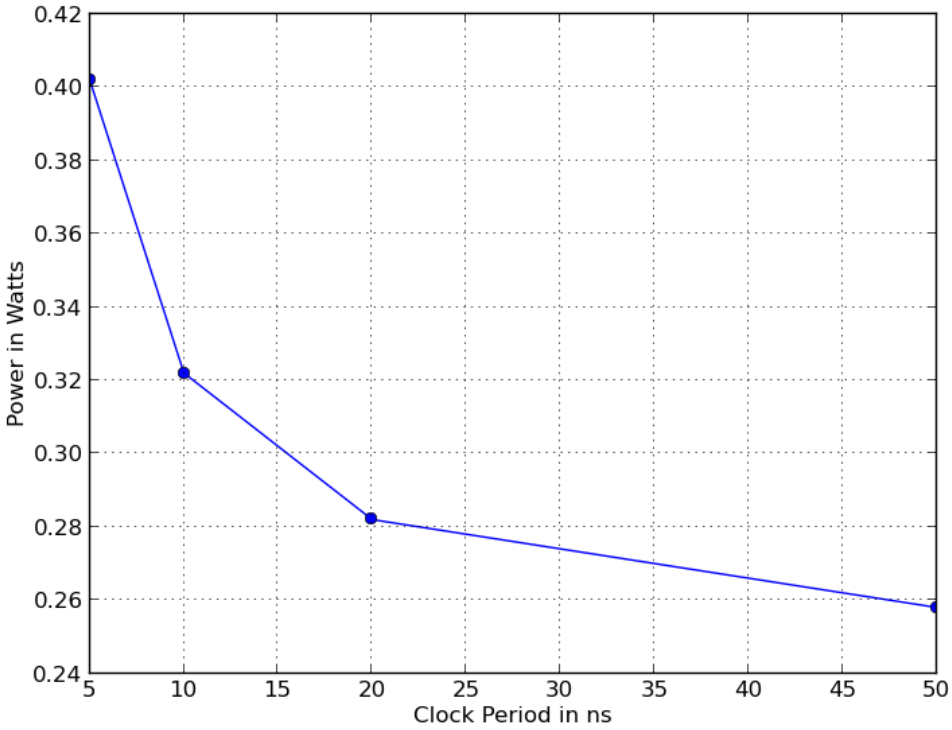

Figure 5.4: Shows Variation of power with timing constraint for the project core Cordic rect2polar.

5.2.5 Project Core :Fixed Point Arithmatic Module :Divider

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.254
10	0.248
20	0.245
50	0.243

Table 5.5: Shows Variation of Power with timing constraint from 0ns to 50ns.

Discussion :

From the above table, Power is 0.254Watts for the clock period 5ns, 0.248Watts for the clock period 10ns, 0.245Watts for the clock period 20ns and 0.243Watts for the clock period 50ns. As the clock period is keep on increasing from 5ns to 50ns, power is decreased from 0.254Watts to 0.243Watts. From the above analysis it is clear that as the timing constraint is keep on increasing power is decreasing gradually in case of FPGA.

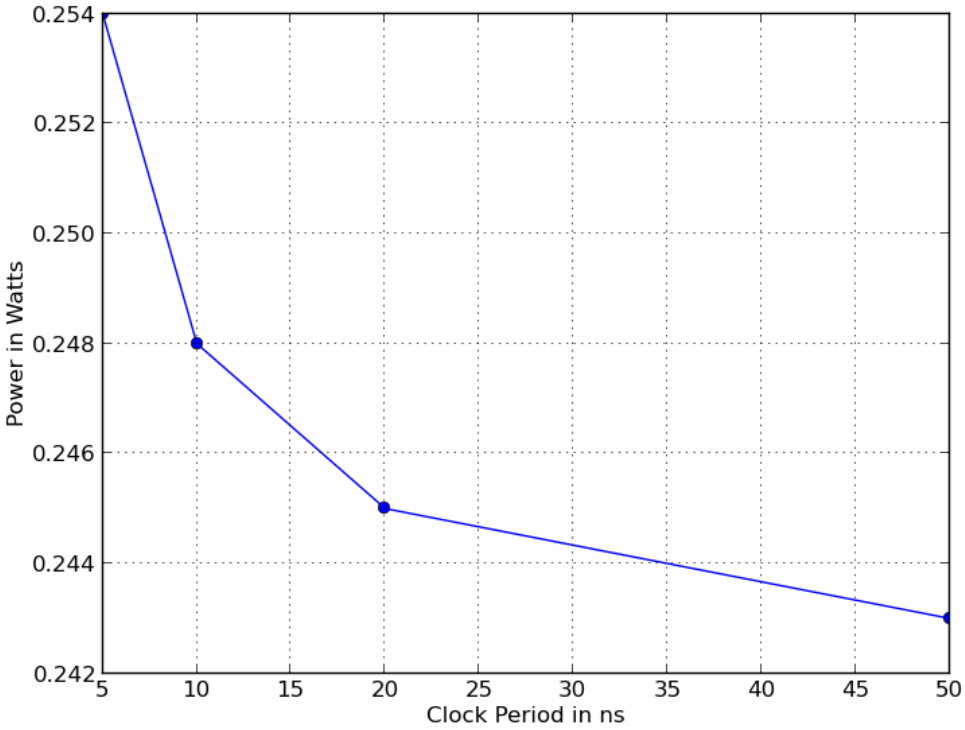

Figure 5.5: Shows Variation of power with timing constraint for the project core Fixed Point arithmatic module: Divider.

5.2.6 Project Core :Fixed Point Math Library :Divider

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ns)$	$Power(inWatts)$
5	0.259
10	0.251
20	0.246
50	0.244

Table 5.6: Shows Variation of Power with timing constraint from 0ns to 50ns.

Discussion :
From the above table, Power is 0.254Watts for the clock period 5ns, 0.248Watts for the clock period 10ns, 0.245Watts for the clock period 20ns and 0.243Watts for the clock period 50ns. As the clock period is keep on increasing from 5ns to 50ns, power is decreased from 0.254Watts to 0.243Watts. From the above analysis it is clear that as the timing constraint is keep on increasing power is decreasing gradually in case of FPGA.

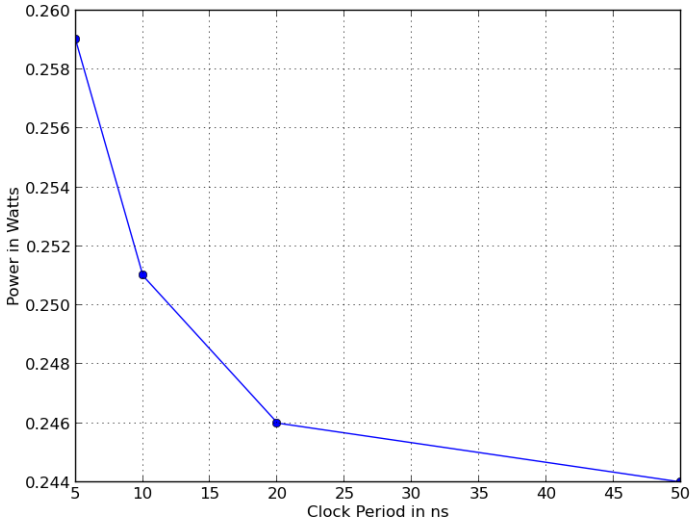

Figure 5.6: Shows Variation of power with timing constraint for the project core Fixed Point math library: Divider.

5.3 Variation of Power in ASIC with Timing Constraint

5.3.1 Project Core : AES_128

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ps)$	$Power(inmW)$
0	3.9177
500	3.6248
1000	3.2492
1100	2.8261
1200	2.4865
1250	2.3369
1280	2.3251

Table 5.7: Shows Variation of power with timing constraint for the project core AES_128.

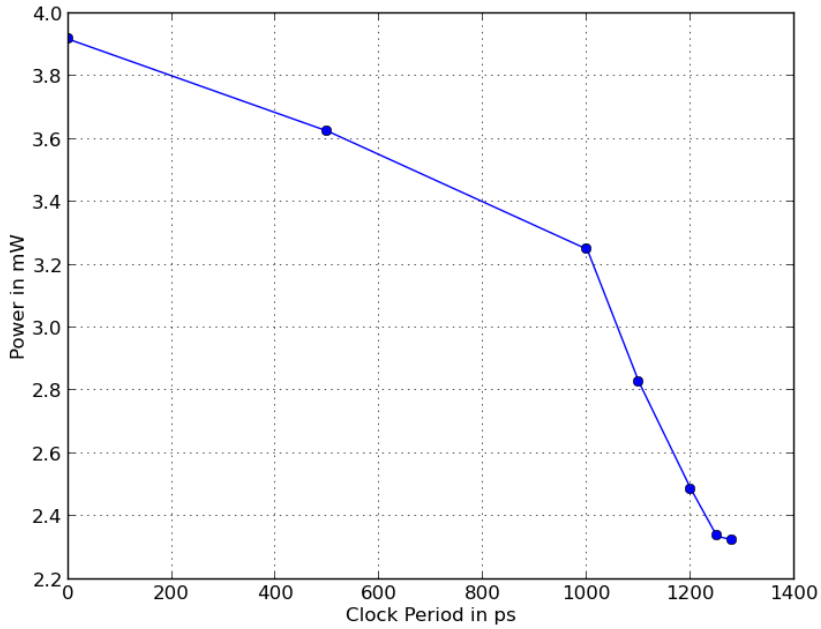

Figure 5.7: Shows Variation of power with timing constraint for the project core aes_128.

Discussion :

From the the above figure and table, as the clock period is increased from 0ps to 1280ps, Power is decreased from 3.9177mWatts to 2.3251mWatts. From the above analysis it is clear that as that timing constraint is keep on increasing, power consumption is keep on decreasing incase of ASIC.

5.3.2 Project Core : Configurable Cordic Core

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ps)$	$Power(inmW)$
0	4.026
500	2.864
600	2.928
700	2.169
750	1.184

Table 5.8: Shows Variation of power with timing constraint for the project core Configurable cordic core.

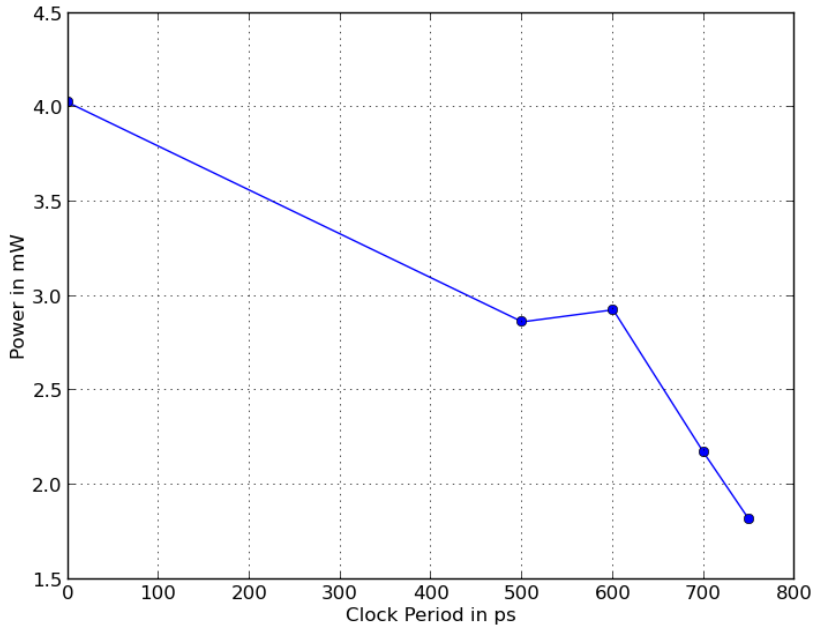

Figure 5.8: Shows Variation of power with timing constraint for the project core Configurable cordic core.

Discussion :

From the the above figure and table, as the clock period is increased from 0ps to 750ps, Power is decreased from 4.026mWatts to 1.184mWatts. From the above analysis it is clear that as that timing constraint is keep on increasing, power consumption is keep on decreasing incase of ASIC.

5.3.3 Project Core : Cordic_polar2rect

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ps)$	$Power(inmW)$
0	2.865
500	1.614
600	1.429
700	1.248
750	1.086
755	0.991

Table 5.9: Shows Variation of power with timing constraint for the project core Configurable cordic_polar2rect.

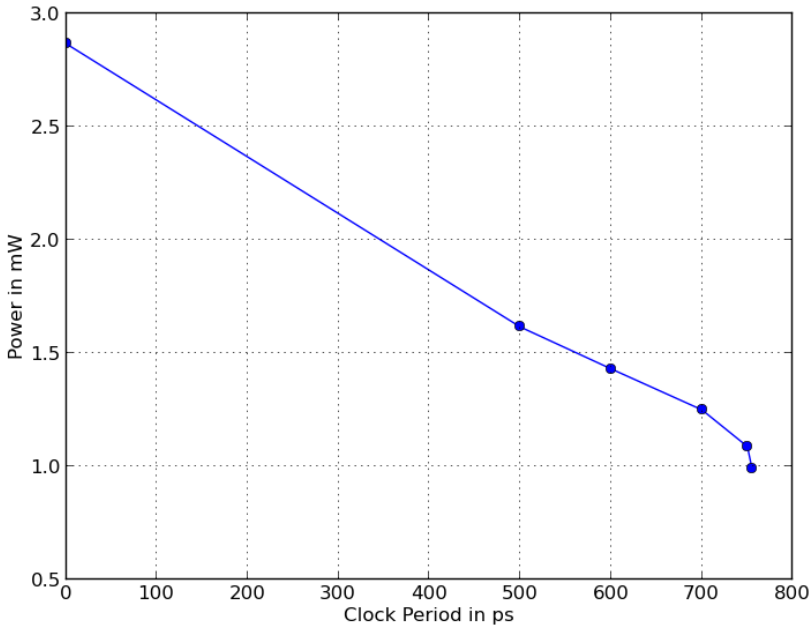

Figure 5.9: Shows Variation of power with timing constraint for the project core cordic_polar2rect.

Discussion :

From the the above figure and table, as the clock period is increased from 0ps to 755ps, Power is decreased from 2.865mWatts to 0.991mWatts. From the above analysis it is clear that as that timing constraint is keep on increasing, power consumption is keep on decreasing incase of ASIC.

5.3.4 Project Core :Fixed point math library_divider

The follwing table shows how Power changes with variation of clock periods.

$ClockPeriod(ps)$	$Power(inmW)$
0	2.614
500	1.412
600	1.2958
700	1.061
750	0.983
770	0.964

Table 5.10: Shows Variation of power with timing constraint for the project core Fixed point math library$_d ivider$.

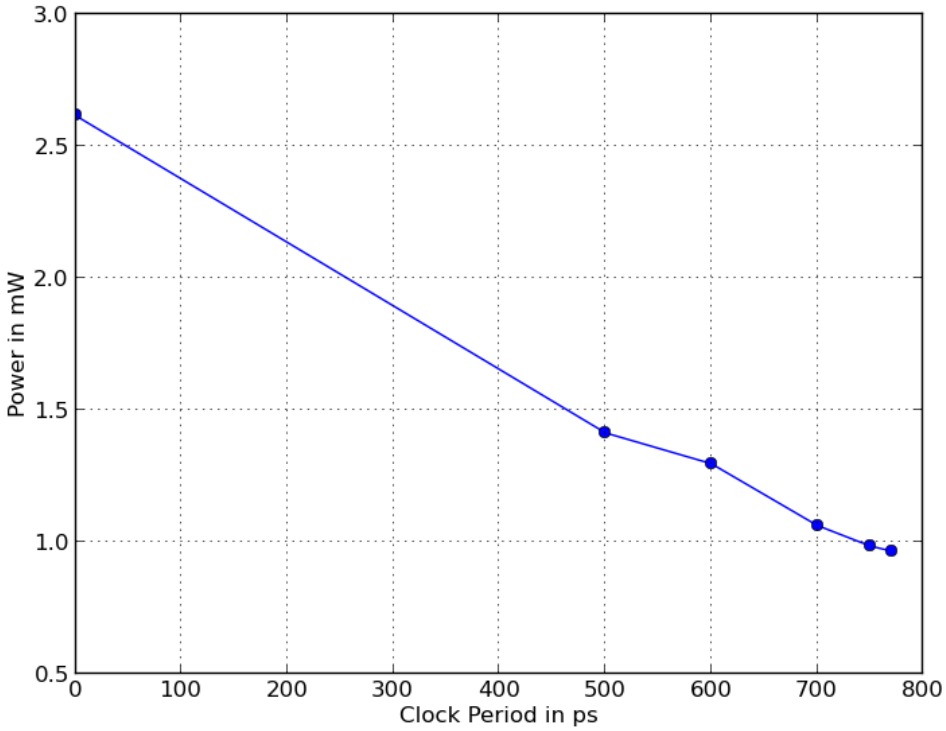

Figure 5.10: Shows Variation of power with timing constraint for the project core Fixed point math library_divider.

Discussion :

From the the above figure and table, as the clock period is increased from 0ps to 770ps, Power is decreased from 2.614mWatts to 0.964mWatts. From the above analysis it is clear that as that timing constraint is keep on increasing, power consumption is keep on decreasing incase of ASIC.

5.4 Variation of FPGA Size with Timing Constraint

5.4.1 Project Core : AES_128

- **Clock Period = 5ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	2041	0.67
FF	607200	910	0.15
IO	700	79	11.29
BUFG	32	1	3.13
Total	911532	**3031**	15.24

Table 5.11: Shows clock period 5ns with Utilization 15.24%.

- **Clock Period = 10ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	2041	0.67
FF	607200	910	0.15
IO	700	79	11.29
BUFG	32	1	3.13
Total	911532	**3031**	15.24

Table 5.12: Shows clock period 10ns with Utilization 15.24%.

- **Clock Period = 20ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	2041	0.67
FF	607200	910	0.15
IO	700	79	11.29
BUFG	32	1	3.13
Total	911532	**3031**	15.24

Table 5.13: Shows clock period 20ns with Utilization 15.24%.

- **Clock Period = 50ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	2041	0.67
FF	607200	910	0.15
IO	700	79	11.29
BUFG	32	1	3.13
Total	911532	**3031**	15.24

Table 5.14: Shows clock period 50ns with Utilization 15.24%.

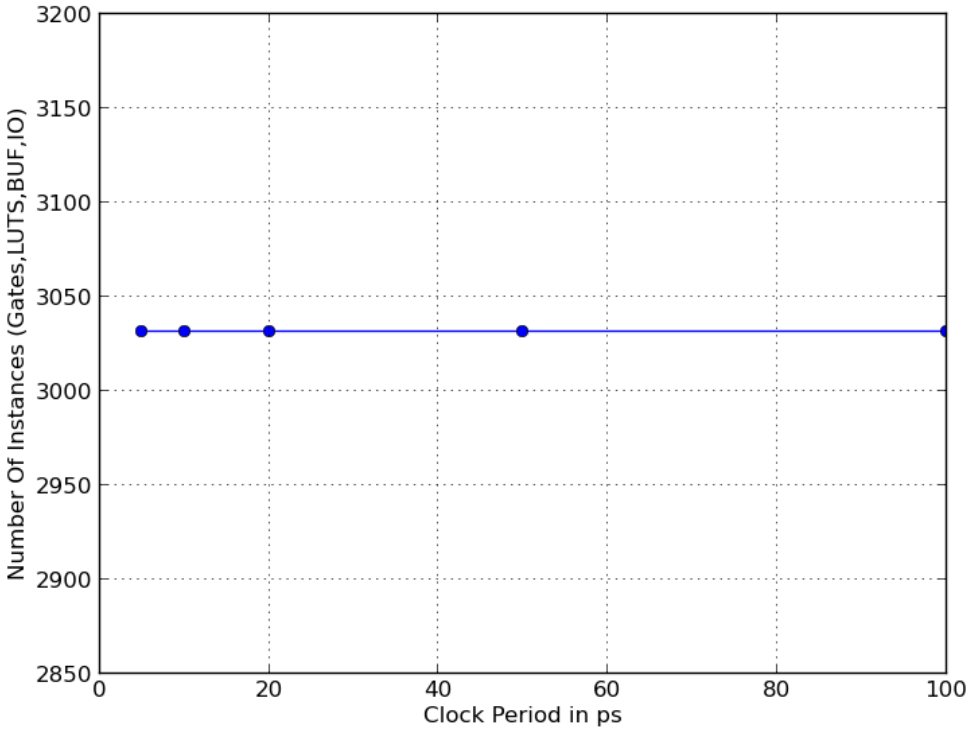

Figure 5.11: Shows Variation of FPGA size with timing constraint for the project core AES_128.

- **Clock Period = 100ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	2041	0.67
FF	607200	910	0.15
IO	700	79	11.29
BUFG	32	1	3.13
Total	911532	**3031**	15.24

Table 5.15: Shows clock period 100ns with Utilization 15.24%.

Discussion :

From the above table and figure, As we increase the clock period from 0ns to 100 ns, the number of instances(Gates, LUTs, BUF, IO) are same all clock periods. From the above analysis it is clear that as we keep on increasing the clock periods there is no effect on number of instances. In case of FPGA the timing constraint doesn't effect the number of instances.

5.4.2 Project Core : Configurable cordic core

- **Clock Period = 5ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	735	0.24
LUTRAM	130800	7	0.01
FF	607200	739	0.12
IO	700	104	14.86
BUFG	32	1	3.13
Total	911532	**1586**	18.36

Table 5.16: Shows clock period 5ns with Utilization 18.36%.

- **Clock Period = 10ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	735	0.24
LUTRAM	130800	7	0.01
FF	607200	739	0.12
IO	700	104	14.86
BUFG	32	1	3.13
Total	911532	**1586**	18.36

Table 5.17: Shows clock period 10ns with Utilization 18.36%.

- **Clock Period = 20ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	735	0.24
LUTRAM	130800	7	0.01
FF	607200	739	0.12
IO	700	104	14.86
BUFG	32	1	3.13
Total	911532	**1586**	18.36

Table 5.18: Shows clock period 20ns with Utilization 18.36%.

- **Clock Period = 50ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	735	0.24
LUTRAM	130800	7	0.01
FF	607200	739	0.12
IO	700	104	14.86
BUFG	32	1	3.13
Total	911532	**1586**	18.36

Table 5.19: Shows clock period 50ns with Utilization 18.36%.

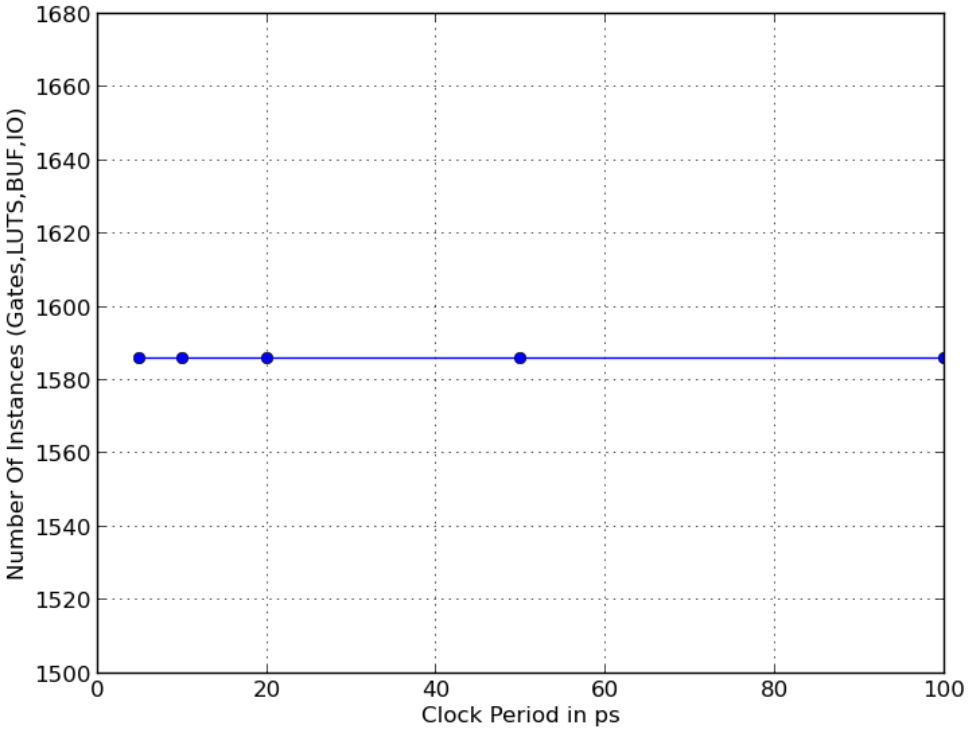

Figure 5.12: Shows Variation of FPGA size with timing constraint for the project core Configurable cordic core.

- **Clock Period = 100ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	735	0.24
LUTRAM	130800	7	0.01
FF	607200	739	0.12
IO	700	104	14.86
BUFG	32	1	3.13
Total	911532	**1586**	18.36

Table 5.20: Shows clock period 100ns with Utilization 18.36%.

Discussion :

From the above table and figure, As we increase the clock period from 0ns to 100 ns, the number of instances(Gates, LUTs, BUF, IO) are same all clock periods. From the above analysis it is clear that as we keep on increasing the clock periods there is no effect on number of instances. In case of FPGA the timing constraint doesn't effect the number of instances.

5.4.3 Project Core : Cordic_polar2rect

- **Clock Period = 5ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	705	0.23
FF	607200	689	0.11
IO	700	50	7.14
BUFG	32	1	3.13
Total	911532	**1445**	10.61

Table 5.21: Shows clock period 5ns with Utilization 10.61%.

- **Clock Period = 10ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	705	0.23
FF	607200	689	0.11
IO	700	50	7.14
BUFG	32	1	3.13
Total	911532	**1445**	10.61

Table 5.22: Shows clock period 10ns with Utilization 10.61%.

- **Clock Period = 20ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	705	0.23
FF	607200	689	0.11
IO	700	50	7.14
BUFG	32	1	3.13
Total	911532	**1445**	10.61

Table 5.23: Shows clock period 20ns with Utilization 10.61%.

- **Clock Period = 50ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	705	0.23
FF	607200	689	0.11
IO	700	50	7.14
BUFG	32	1	3.13
Total	911532	**1445**	10.61

Table 5.24: Shows clock period 50ns with Utilization 10.61%.

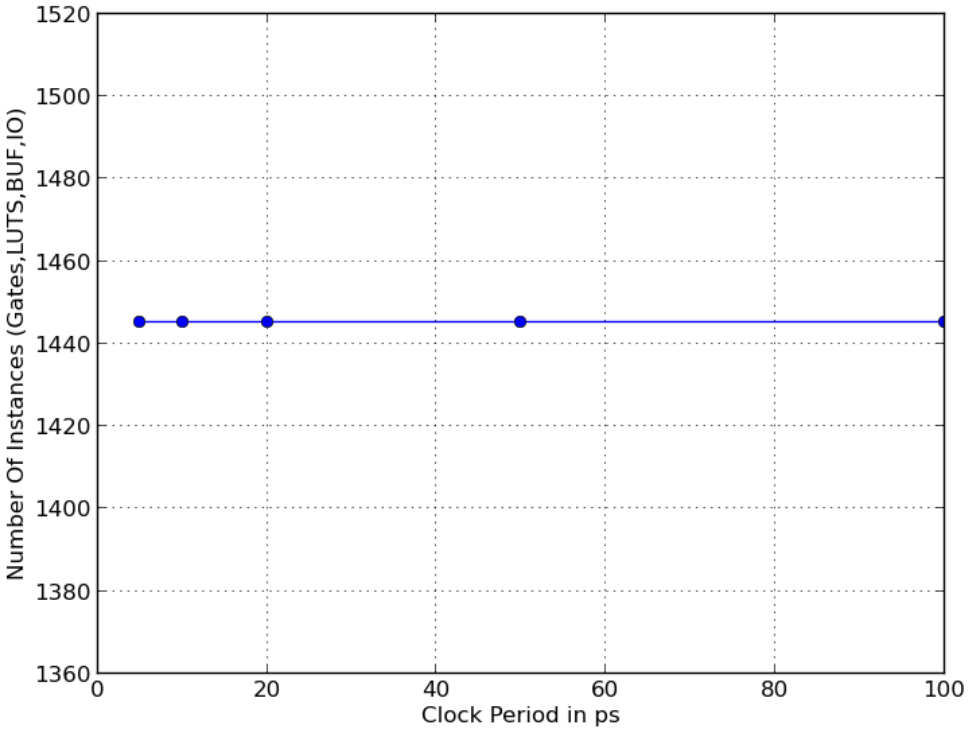

Figure 5.13: Shows Variation of FPGA size with timing constraint for the project core cordic_polar2rect.

- **Clock Period = 100ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	705	0.23
FF	607200	689	0.11
IO	700	50	7.14
BUFG	32	1	3.13
Total	911532	**1445**	10.61

Table 5.25: Shows clock period 100ns with Utilization 10.61%.

Discussion :

From the above table and figure, As we increase the clock period from 0ns to 100 ns, the number of instances(Gates, LUTs, BUF, IO) are same all clock periods. From the above analysis it is clear that as we keep on increasing the clock periods there is no effect on number of instances. In case of FPGA the timing constraint doesn't effect the number of instances.

5.4.4 Project Core : Cordic_polar2rect

- **Clock Period = 5ns**

Resource	*Available*	*Utilization*	*Utilization*(%)
LUT	303600	353	0.12
FF	607200	265	0.04
IO	700	101	14.43
BUFG	32	1	3.13
Total	911532	**720**	17.72

Table 5.26: Shows clock period 5ns with Utilization 17.72%.

- **Clock Period = 10ns**

Resource	*Available*	*Utilization*	*Utilization*(%)
LUT	303600	353	0.1
FF	607200	265	0.04
IO	700	101	14.43
BUFG	32	1	3.13
Total	911532	**670**	17.67

Table 5.27: Shows clock period 10ns with Utilization 17.67%.

- **Clock Period = 20ns**

Resource	*Available*	*Utilization*	*Utilization*(%)
LUT	303600	353	0.1
FF	607200	265	0.04
IO	700	101	14.43
BUFG	32	1	3.13
Total	911532	**670**	17.67

Table 5.28: Shows clock period 20ns with Utilization 17.67%.

- **Clock Period = 50ns**

Resource	*Available*	*Utilization*	*Utilization*(%)
LUT	303600	353	0.1
FF	607200	265	0.04
IO	700	101	14.43
BUFG	32	1	3.13
Total	911532	**670**	17.67

Table 5.29: Shows clock period 50ns with Utilization 17.67%.

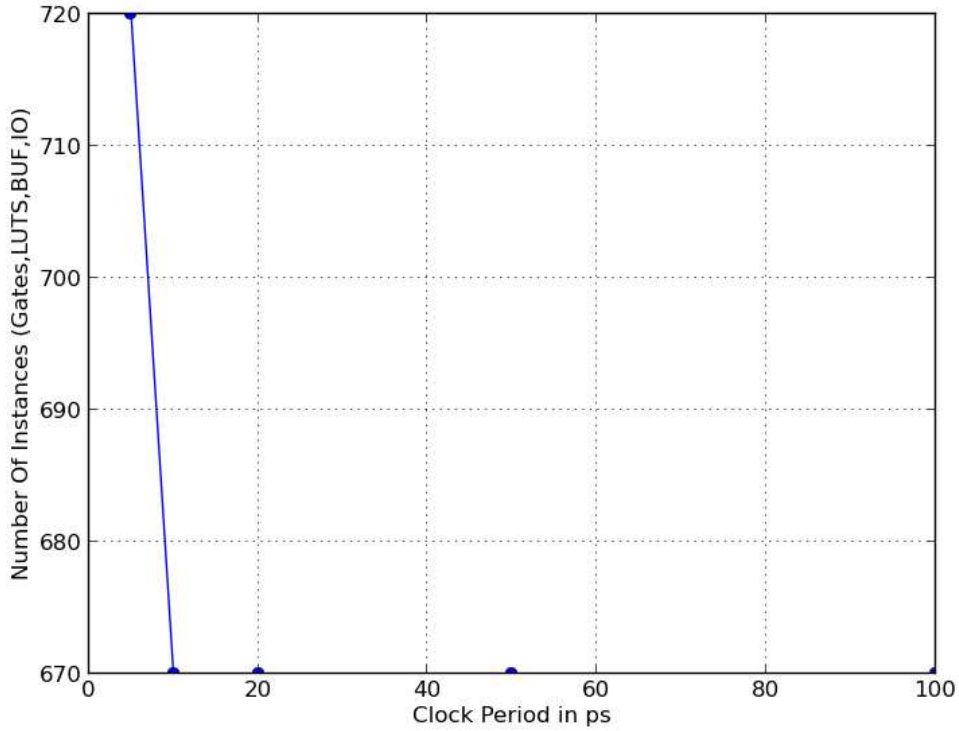

Figure 5.14: Shows Variation of FPGA size with timing constraint for the project core Fixed point math library$_d ivider$.

- **Clock Period = 100ns**

Resource	*Available*	*Utilization*	*Utilization(%)*
LUT	303600	353	0.1
FF	607200	265	0.04
IO	700	101	14.43
BUFG	32	1	3.13
Total	911532	**670**	17.67

Table 5.30: Shows clock period 100ns with Utilization 17.67%.

Discussion :

From the above table and figure, As we increase the clock period from 0ns to 100 ns, the number of instances(Gates, LUTs, BUF, IO) are same all clock periods. From the above analysis it is clear that as we keep on increasing the clock periods there is no effect on number of instances. In case of FPGA the timing constraint doesn't effect the number of instances.

5.5 Variation of ASIC Size with Timing Constraint

5.5.1 Project Core : AES_128

The follwing tables shows how ASIC size changes with variation of clock periods.

- **Clock Period = 0ps *Timing Slack = -1298ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	667	3123.120	11.4
Buffer	393	1270.920	4.6
Logic	6168	17152.520	62.7
Sequential	910	5791.24	21.2
Total	9138	**27337.800**	100

Table 5.31: Shows clock period 0ps with timing Violation of -1298ps.

- **Clock Period = 100ps *Timing Slack = -1206ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1504	2868.880	10.7
Buffer	370	1208.8	4.5
Logic	6017	16900.24	63.1
Sequential	910	5790.4	21.6
Total	8801	26767.720	100

Table 5.32: Shows clock period 100ps with timing Violation of -1206ps.

- **Clock Period = 200ps *Timing Slack = -1092ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1564	2993.480	10.9
Buffer	380	1251.040	4.6
Logic	6060	17362.520	63.30
Sequential	910	5804.960	21.20
Total	8914	27412	100

Table 5.33: Shows clock period 200ps with timing Violation of -1092ps.

- **Clock Period = 300ps** ***Timing Slack = -992ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1595	3123.12	11.2
Buffer	371	1202.04	4.3
Logic	6075	17670.8	63.60
Sequential	910	5810	20.90
Total	8951	27805.96	100

Table 5.34: Shows clock period 300ps with timing Violation of -992ps.

- **Clock Period = 400ps** ***Timing Slack = -898ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1634	3204.6	11.4
Buffer	393	1284.08	4.6
Logic	6226	17759.56	63.30
Sequential	910	5808.6	20.70
Total	9163	28056.84	100

Table 5.35: Shows clock period 400ps with timing Violation of -898ps.

- **Clock Period = 500ps** ***Timing Slack = -798ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1624	3183.04	11.1
Buffer	399	1360.8	4.8
Logic	6235	18247.6	63.80
Sequential	910	5795.72	20.30
Total	9168	28587.160	100

Table 5.36: Shows clock period 500ps with timing Violation of -798ps.

- **Clock Period = 600ps** ***Timing Slack = -715ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1617	3327.8	11.80
Buffer	378	1264.76	4.5
Logic	6042	17806.04	63.10
Sequential	910	5828.2	20.60
Total	8947	28226.8	100

Table 5.37: Shows clock period 600ps with timing Violation of -715ps.

- **Clock Period = 700ps** ***Timing Slack = -600ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1576	3111.920	11
Buffer	361	1217.720	4.3
Logic	6048	18129.72	64.1
Sequential	910	5825.4	20.60
Total	8895	28284.76	100

Table 5.38: Shows clock period 700ps with timing Violation of -600ps.

- **Clock Period = 800ps** ***Timing Slack = -547ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1725	3473.96	11.2
Buffer	438	1643.32	5.3
Logic	6617	19972.4	64.7
Sequential	910	5803.28	18.8
Total	9690	30892.96	100

Table 5.39: Shows clock period 800ps with timing Violation of -547ps.

- **Clock Period = 900ps** ***Timing Slack = -453ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1873	3775.52	12.4
Buffer	413	1392.44	4.6
Logic	6432	19384.12	63.80
Sequential	910	5821.76	19.2
Total	9628	30373.84	100

Table 5.40: Shows clock period 900ps with timing Violation of -453ps.

- **Clock Period = 1000ps** ***Timing Slack = -314ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1704	3131.52	10.9
Buffer	410	1529.08	5.3
Logic	6129	18216.24	63.60
Sequential	910	5756.52	20.1
Total	9153	28633.360	100

Table 5.41: Shows clock period 1000ps with timing Violation of -314ps.

- **Clock Period = 1100ps** ***Timing Slack = -197ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1804	3186.12	11
Buffer	454	1578.08	5.5
Logic	6007	18389.56	63.60
Sequential	910	5779.2	20
Total	9175	28932.96	100

Table 5.42: Shows clock period 1100ps with timing Violation of -197ps.

- **Clock Period = 1200ps** ***Timing Slack = -95ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1710	2737	9.8
Buffer	481	1508.92	5.4
Logic	5914	18389.56	63.60
Sequential	910	5759.88	20.6
Total	9015	27984.32	100

Table 5.43: Shows clock period 1200ps with timing Violation of -95ps.

- **Clock Period = 1250ps** ***Timing Slack = -35ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1926	5780.32	20.3
Buffer	436	1243.48	4.4
Logic	5968	18258.52	64.10
Sequential	910	5780.32	20.3
Total	9240	28468.16	100

Table 5.44: Shows clock period 1250ps with timing Violation of -35ps.

- **Clock Period = 1275ps** ***Timing Slack = -15ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1911	2898.28	11
Buffer	405	1094.24	4.1
Logic	5894	16684.36	63.1
Sequential	910	5743.64	21.7
Total	9120	26420.52	100

Table 5.45: Shows clock period 1275ps with timing Violation of -15ps.

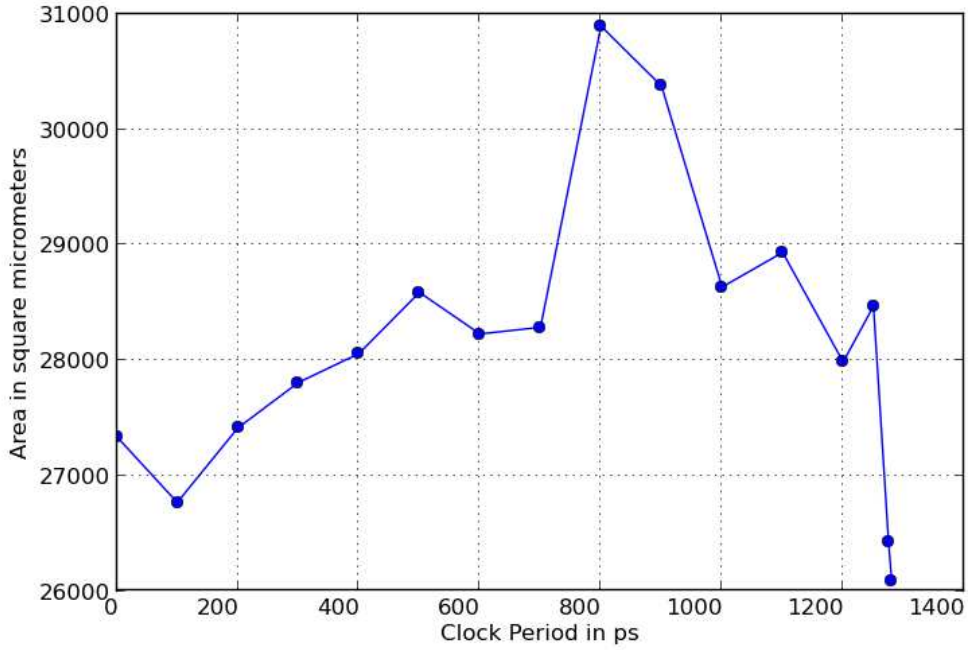

Figure 5.15: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 27337.8 Square micrometre)** to 1280ps (**Clock period at which timing slack is 0 : Area = 26092.36)**

- **Clock Period = 1280ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1911	2898.28	11
Buffer	405	1094.24	4.1
Logic	5894	16684.36	63.1
Sequential	910	5743.64	21.7
Total	9120	**26420.52**	100

Table 5.46: Shows clock period 1280ps with timing slack of 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 1280ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates incase of ASIC, area is decreased from clock period 0ps to clock period at which the timing constarint is 0.

5.5.2 8-bit Vedic Multiplier

- **Clock Period = 0ps** ***Timing Slack = -1144ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	142	182.24	9.4
Buffer	16	24.92	1.3
Logic	482	1733.76	89.3
Sequential	0	0	0
Total	640	1940.92	100

Table 5.47: Shows clock period 0ps with timing Violation of -1144ps.

- **Clock Period = 100ps** ***Timing Slack = -1070ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	129	159.6	9
Buffer	18	35	2
Logic	443	1581.44	89
Sequential	0	0	0
Total	590	1776.04	100

Table 5.48: Shows clock period 100ps with timing Violation of -1070ps.

- **Clock Period = 200ps** ***Timing Slack = -969ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	137	160.72	9.1
Buffer	24	49.28	2.8
Logic	449	1556.24	88.1
Sequential	0	0	0
Total	610	1766.24	100

Table 5.49: Shows clock period 200ps with timing Violation of -969ps.

- **Clock Period = 300ps** ***Timing Slack = -847ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	150	191.24	9.8
Buffer	26	48.720	2.5
Logic	486	1702.960	87.60
Sequential	0	0	0
Total	662	1942.92	100

Table 5.50: Shows clock period 300ps with timing Violation of -847ps.

- **Clock Period = 400ps** ***Timing Slack = -774ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	132	165.48	8.9
Buffer	15	25.760	1.4
Logic	471	1670.760	89.70
Sequential	0	0	0
Total	618	1862	100

Table 5.51: Shows clock period 400ps with timing Violation of -774ps.

- **Clock Period = 500ps** ***Timing Slack = -651ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	134	178.36	9.3
Buffer	21	38.920	2.0
Logic	445	1701.840	88.70
Sequential	0	0	0
Total	600	1919.12	100

Table 5.52: Shows clock period 500ps with timing Violation of -651ps.

- **Clock Period = 600ps** ***Timing Slack = -556ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	131	173.88	9.5
Buffer	21	35.840	1.9
Logic	454	1629.88	88.60
Sequential	0	0	0
Total	606	1839.6	100

Table 5.53: Shows clock period 600ps with timing Violation of -556ps.

- **Clock Period = 700ps** ***Timing Slack = -4666ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	122	166.6	8.7
Buffer	25	48.16	2.5
Logic	468	1708.84	88.80
Sequential	0	0	0
Total	615	1923.6	100

Table 5.54: Shows clock period 700ps with timing Violation of -466ps.

- **Clock Period = 800ps** ***Timing Slack = -334ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	116	146.44	7.1
Buffer	31	59.64	2.9
Logic	491	1842.4	89.9
Sequential	0	0	0
Total	638	2048.48	100

Table 5.55: Shows clock period 800ps with timing Violation of -334ps.

- **Clock Period = 900ps** ***Timing Slack = -237ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	142	196.56	9.5
Buffer	23	47.04	2.3
Logic	494	1825.04	88.2
Sequential	0	0	0
Total	659	2068.64	100

Table 5.56: Shows clock period 900ps with timing Violation of -237ps.

- **Clock Period = 1000ps** ***Timing Slack = -164ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	132	175.56	9.2
Buffer	21	41.44	2.2
Logic	453	1696.8	88.7
Sequential	0	0	0
Total	606	1913.8	100

Table 5.57: Shows clock period 1000ps with timing Violation of -164ps.

- **Clock Period = 1100ps** ***Timing Slack = -41ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	147	189	9.4
Buffer	25	54.60	2.7
Logic	488	1762.04	87.9
Sequential	0	0	0
Total	660	2005.64	100

Table 5.58: Shows clock period 1100ps with timing Violation of -41ps.

- **Clock Period = 1140ps** ***Timing Slack = -13ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	117	153.72	8.2
Buffer	21	31.08	1.7
Logic	431	1685.04	90.1
Sequential	0	0	0
Total	569	1869.04	100

Table 5.59: Shows clock period 1140ps with timing Violation of -13ps.

- **Clock Period = 1150ps** ***Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	117	153.72	8.2
Buffer	21	31.08	1.7
Logic	431	1685.04	90.1
Sequential	0	0	0
Total	569	**1869.04**	100

Table 5.60: Shows clock period 1150ps with timing Slack 0ps.

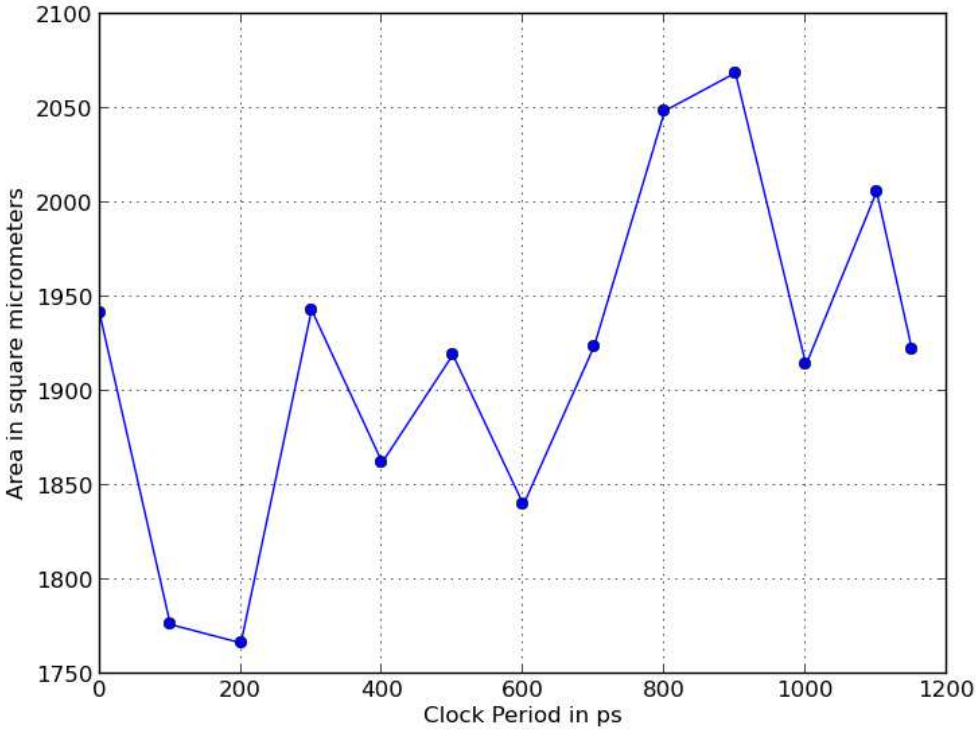

Figure 5.16: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 1940.92 square micrometre)** to 1150ps (**Clock period at which timing slack is 0: Area = 1921.92 Square micrometre)**

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 1150ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates incase of ASIC, area is decreased from clock period 0ps to clock period at which the timing constarint is 0.

5.5.3 Configurable Cordic Core

- **Clock Period = 0ps *Timing Slack = -751ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3805	7175.56	15.8
Buffer	800	2586.64	.75
Logic	10031	30621.92	67.6
Sequential	767	4909.24	10.8
Total	15400	45293.36	100

Table 5.61: Shows clock period 0ps with timing Violation -751ps.

- **Clock Period = 100ps *Timing Slack = -647ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3880	7364.28	16.1
Buffer	821	2566.48	5.6
Logic	10234	31034.08	67.6
Sequential	764	4912.88	10.7
Total	15699	45877.72	100

Table 5.62: Shows clock period 100ps with timing Violation -647ps.

- **Clock Period = 200ps *Timing Slack = -549ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3818	7414.68	16
Buffer	801	2649.92	5.7
Logic	10109	31286.36	67.6
Sequential	764	4918.48	10.6
Total	15492	46269.44	100

Table 5.63: Shows clock period 200ps with timing Violation -549ps.

- **Clock Period = 300ps *Timing Slack = -442ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3645	7413	15.4
Buffer	855	2924.6	6.1
Logic	10461	32926.040	68.3
Sequential	764	4925.76	10.2
Total	15725	48189.4	100

Table 5.64: Shows clock period 300ps with timing Violation -442ps.

- **Clock Period = 400ps** ***Timing Slack = -359ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3609	7932.4	16
Buffer	764	2657.48	5.4
Logic	10497	34158.04	68.8
Sequential	764	4922.12	9.9
Total	15634	49670.04	100

Table 5.65: Shows clock period 400ps with timing Violation -359ps.

- **Clock Period = 500ps** ***Timing Slack = -247ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3345	7628.88	15.1
Buffer	854	3099.32	6.1
Logic	10451	34851.6	69
Sequential	764	4952.64	9.8
Total	15414	50532.44	100

Table 5.66: Shows clock period 500ps with timing Violation -247ps.

- **Clock Period = 600ps** ***Timing Slack = -139ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3640	8487.36	16.2
Buffer	855	2995.16	5.7
Logic	10102	35916.16	68.16
Sequential	764	4938.92	9.4
Total	15361	52337.6	100

Table 5.67: Shows clock period 600ps with timing Violation -139ps.

- **Clock Period = 700ps** ***Timing Slack = -53ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3479	7601.72	15.1
Buffer	952	3122	6.2
Logic	9783	34722.8	68.9
Sequential	764	4937.24	9.8
Total	14978	50383.76	100

Table 5.68: Shows clock period 700ps with timing Violation -53ps.

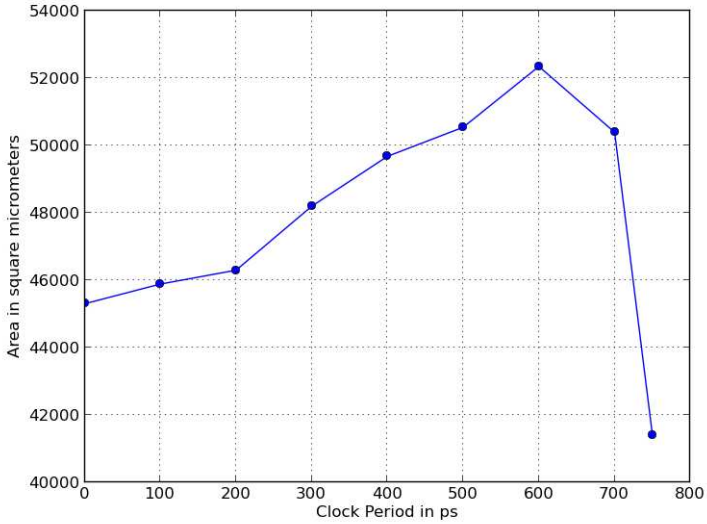

Figure 5.17: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 45293.36 square micrometres)** to 750ps (**Clock period at which timing slack is 0: Area = 41384.28 Square micrometres)**

- **Clock Period = 750ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3061	5911.08	14.3
Buffer	585	1733.2	4.2
Logic	9431	28799.68	69.6
Sequential	764	4940.32	11.9
Total	15361	52337.6	100

Table 5.69: Shows clock period 750ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 750ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.4 CORDIC CORE: cordic polar2rect

- **Clock Period = 0ps** ***Timing Slack = -751ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3753	6974.52	16.6
Buffer	748	2365.44	5.6
Logic	10212	28661.08	68.2
Sequential	670	4001.2	9.5
Total	15383	42002.24	100

Table 5.70: Shows clock period 0ps with timing Violation -730ps.

- **Clock Period = 100ps** ***Timing Slack = -627ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3856	7208.32	16.7
Buffer	778	2574.04	6
Logic	10230	29290.24	68
Sequential	670	3997.2	9.3
Total	15534	43070.44	100

Table 5.71: Shows clock period 100ps with timing Violation -627ps.

- **Clock Period = 200ps** ***Timing Slack = -534ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3853	7363.44	17.1
Buffer	763	2457.56	5.7
Logic	10072	29286.04	67.9
Sequential	670	4004.56	9.3
Total	15358	43111.6	100

Table 5.72: Shows clock period 200ps with timing Violation -534ps.

- **Clock Period = 300ps** ***Timing Slack = -433ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3113	6486.76	15.7
Buffer	675	2215.64	5.4
Logic	10006	28478.8	69.1
Sequential	670	4023.32	9.8
Total	14464	41204.52	100

Table 5.73: Shows clock period 300ps with timing Violation -433ps.

- **Clock Period = 400ps** ***Timing Slack = -319ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3189	6956.04	15.7
Buffer	707	2566.48	5.8
Logic	10185	30878.4	69.5
Sequential	670	4025.56	9.1
Total	14751	44426.48	100

Table 5.74: Shows clock period 400ps with timing Violation -319ps.

- **Clock Period = 500ps** ***Timing Slack = -238ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3171	7095.48	16.1
Buffer	712	2496.76	5.7
Logic	9936	30538.48	69.2
Sequential	670	4024.44	9.1
Total	14489	44155.16	100

Table 5.75: Shows clock period 500ps with timing Violation -238ps.

- **Clock Period = 600ps** ***Timing Slack = -118ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3417	7662.76	16.5
Buffer	913	3341.8	7.2
Logic	9587	31495.52	67.7
Sequential	669	4015.76	8.6
Total	14586	46515.84	100

Table 5.76: Shows clock period 600ps with timing Violation -118ps.

- **Clock Period = 700ps** ***Timing Slack = -20ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3103	6198.36	15.1
Buffer	859	2655.24	6.5
Logic	8999	28102.48	68.5
Sequential	669	4058.04	9.9
Total	13630	41014.12	100

Table 5.77: Shows clock period 700ps with timing Violation -20ps.

- **Clock Period = 750ps *Timing Slack = -1ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	2758	4978.68	14.1
Buffer	669	1919.96	5.4
Logic	8465	24239.6	68.8
Sequential	672	4090.8	11.6
Total	12564	35229.04	100

Table 5.78: Shows clock period 750ps with timing Violation -1ps.

- **Clock Period = 755ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	2696	4805.64	13.8
Buffer	702	1996.68	5.7
Logic	8436	24038.56	68.8
Sequential	672	4080.16	11.7
Total	12506	34921.040	100

Table 5.79: Shows clock period 755ps with timing Slack 0ps.

- **Clock Period = 760ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	2822	4919.04	14.2
Buffer	745	2169.16	6.3
Logic	8418	23501.24	67.8
Sequential	672	4074.56	11.8
Total	12657	34664	100

Table 5.80: Shows clock period 760ps with timing Slack 0ps.

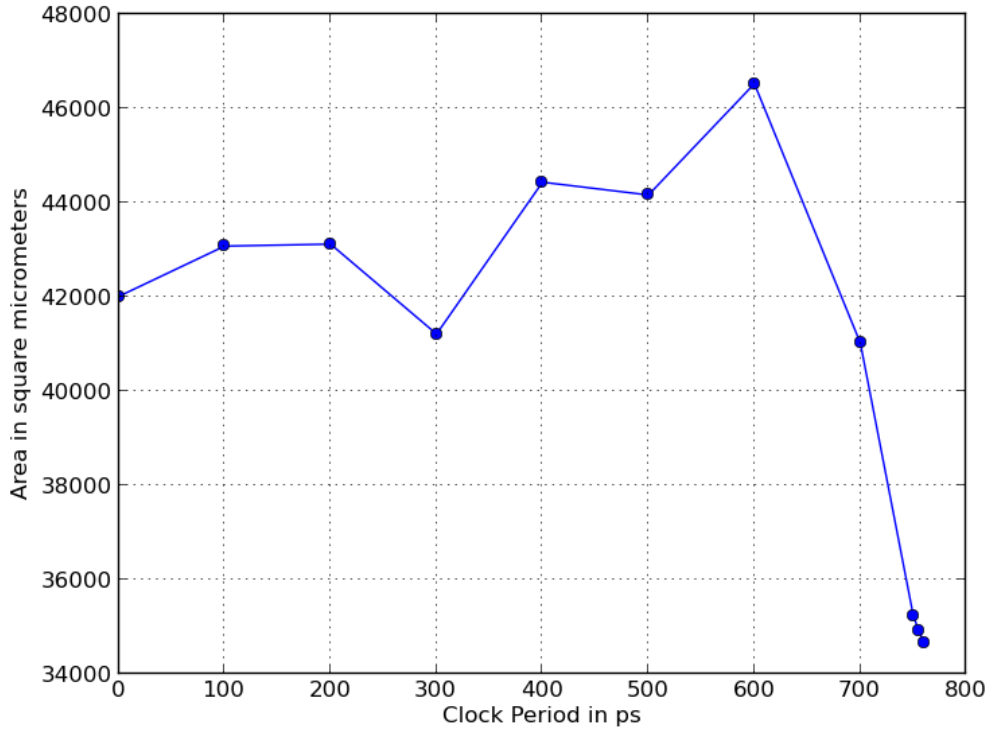

Figure 5.18: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 42002.24 square micrometre)** to 760ps (**Clock period at which timing slack is 0: Area = 34664 Square micrometre)**

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 760ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates incase of ASIC, area is decreased from clock period 0ps to clock period at which the timing constarint is 0.

5.5.5 CORDIC CORE : cordic rect2polar

- **Clock Period = 0ps** ***Timing Slack = -764ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	5130	10121.6	10
Buffer	1037	3327.52	5.4
Logic	13886	42072.24	68.2
Sequential	1033	6142.64	10
Total	21086	61663.56	100

Table 5.81: Shows clock period 0ps with timing Violation -764ps.

- **Clock Period = 100ps** ***Timing Slack = -661ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	5191	10527.44	16.7
Buffer	1024	3239.88	5.1
Logic	13930	43122.8	68.4
Sequential	1038	6151.6	9.8
Total	21178	63041.72	100

Table 5.82: Shows clock period 100ps with timing Violation -661ps.

- **Clock Period = 200ps** ***Timing Slack = -562ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	5121	10598	16.8
Buffer	1010	3201.24	5.1
Logic	13817	43134.84	68.4
Sequential	1033	6141.52	9.7
Total	20981	63075.6	100

Table 5.83: Shows clock period 200ps with timing Violation -562ps.

- **Clock Period = 300ps** ***Timing Slack = -462ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4394	9335.2	15.2
Buffer	939	3341.8	5.4
Logic	14077	42694.4	69.3
Sequential	1033	6193.04	10.1
Total	20443	61564.44	100

Table 5.84: Shows clock period 300ps with timing Violation -462ps.

- **Clock Period = 400ps** ***Timing Slack = -372ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4261	9088.8	14.9
Buffer	1012	3612.84	5.9
Logic	14251	42321.72	69.2
Sequential	1033	6146.84	10
Total	20557	61170.2	100

Table 5.85: Shows clock period 400ps with timing Violation -372ps.

- **Clock Period = 500ps** ***Timing Slack = -285ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4476	9519.16	15.6
Buffer	961	3684.8	6
Logic	13561	41585.6	68.3
Sequential	1033	6139.28	10.1
Total	20031	60928.84	100

Table 5.86: Shows clock period 500ps with timing Violation -285ps.

- **Clock Period = 600ps** ***Timing Slack = -161ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4514	9919	15.5
Buffer	1167	4263.56	6.7
Logic	13556	43615.88	68.2
Sequential	1033	6154.120	9.6
Total	20270	63952.56	100

Table 5.87: Shows clock period 600ps with timing Violation -161ps.

- **Clock Period = 700ps** ***Timing Slack = -56ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4633	9851.24	15.3
Buffer	1357	4433.24	6.9
Logic	13098	43986.88	68.2
Sequential	1033	6200.6	9.6
Total	20119	64471.96	100

Table 5.88: Shows clock period 700ps with timing Violation -56ps.

- **Clock Period = 750ps *Timing Slack = -17ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4331	8691.2	14.8
Buffer	1146	3524.36	6
Logic	12252	40467	68.7
Sequential	1033	6200.88	10.5
Total	18762	58883	100

Table 5.89: Shows clock period 750ps with timing Violation -17ps.

- **Clock Period = 760ps *Timing Slack = -12ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4135	7855.68	13.9
Buffer	1174	3612.56	6.4
Logic	12371	38938.2	68.8
Sequential	1033	6195.84	10.9
Total	18713	56602.280	100

Table 5.90: Shows clock period 760ps with timing Violation of -12ps.

- **Clock Period = 770ps *Timing Slack = -0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	4041	7554.68	14.2
Buffer	962	2895.48	5.4
Logic	12107	36559.6	68.7
Sequential	1033	6199.2	11.7
Total	18143	53208.96	100

Table 5.91: Shows clock period 770ps with timing Slack -0ps.

- **Clock Period = 775ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	3899	7004.48	14.4
Buffer	569	1913.8	3.9
Logic	11758	33418.56	68.8
Sequential	1033	6202.56	12.6
Total	17259	48539.4	100

Table 5.92: Shows clock period 770ps with timing Slack 0ps.

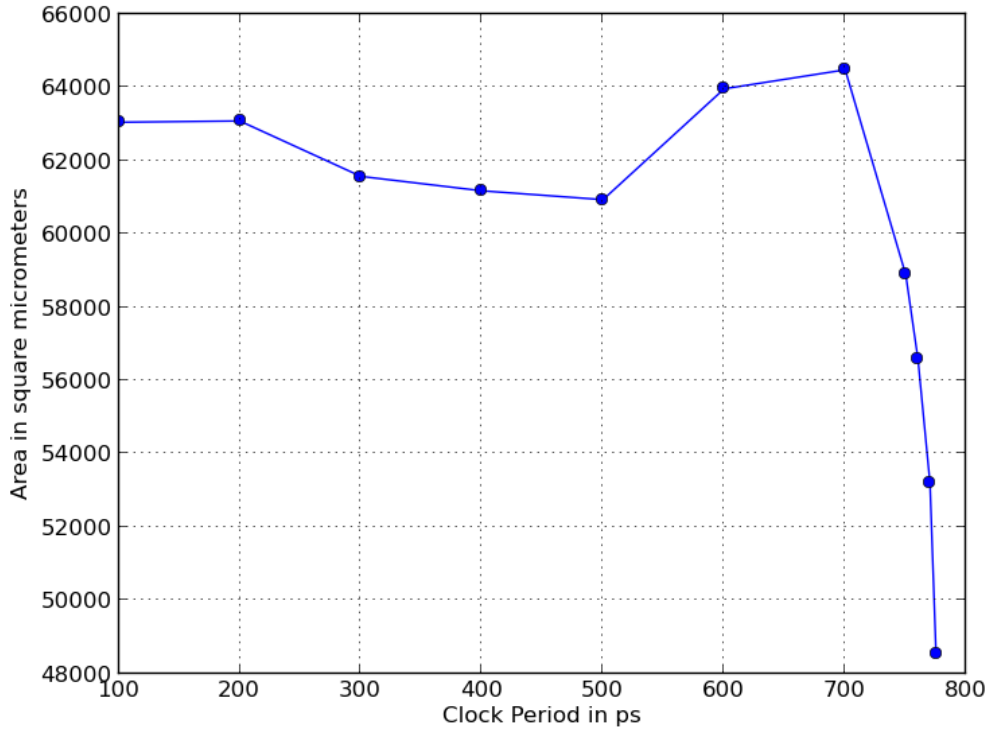

Figure 5.19: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 61663.56 square micrometre)** to 770ps (**Clock period at which timing slack is 0: Area = 48539.4 Square micrometre)**

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 7700ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates incase of ASIC, area is decreased from clock period 0ps to clock period at which the timing constarint is 0.

5.5.6 FIXED_POINT_ARITHMATIC_MODULE: Adder

- **Clock Period = 0ps** ***Timing Slack = -707ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	293	530.6	15.9
Buffer	36	66.92	2.0
Logic	890	2745.4	82.1
Sequential	0	0	0
Total	1219	3342.92	100

Table 5.93: Shows clock period 0ps with timing Violation -730ps.

- **Clock Period = 100ps** ***Timing Slack = -592ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	289	526.12	15.2
Buffer	36	58.52	1.7
Logic	943	2883.44	83.1
Sequential	0	0	0
Total	1268	3468.08	100

Table 5.94: Shows clock period 100ps with timing Violation -592ps.

- **Clock Period = 200ps** ***Timing Slack = -496ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	298	547.12	15.7
Buffer	33	53.2	1.5
Logic	906	2875.88	82.7
Sequential	0	0	0
Total	1237	3476.2	100

Table 5.95: Shows clock period 200ps with timing Violation -496ps.

- **Clock Period = 300ps** ***Timing Slack = -404ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	296	535.64	15.7
Buffer	36	71.12	2.1
Logic	864	2800.28	82.2
Sequential	0	0	0
Total	1196	3407.04	100

Table 5.96: Shows clock period 300ps with timing Violation -404ps.

- **Clock Period = 400ps** ***Timing Slack = -307ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	331	590.8	16.9
Buffer	29	72.24	2.1
Logic	914	2826.6	81.1
Sequential	0	0	0
Total	1274	3489.64	100

Table 5.97: Shows clock period 400ps with timing Violation -307ps.

- **Clock Period = 500ps** ***Timing Slack = -209ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	307	582.96	16.5
Buffer	51	90.44	2.6
Logic	875	2859.08	80.9
Sequential	0	0	0
Total	1233	3532.48	100

Table 5.98: Shows clock period 500ps with timing Violation -209ps.

- **Clock Period = 600ps** ***Timing Slack = -113ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	300	607.44	16.8
Buffer	41	100.24	2.8
Logic	858	2914.24	80.5
Sequential	0	0	0
Total	1199	3621.52	100

Table 5.99: Shows clock period 600ps with timing Violation -113ps.

- **Clock Period = 700ps** ***Timing Slack = -2ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	304	558.6	15.9
Buffer	68	119.56	3.4
Logic	856	2828.28	80.7
Sequential	0	0	0
Total	1228	3506.44	100

Table 5.100: Shows clock period 700ps with timing Violation -2ps.

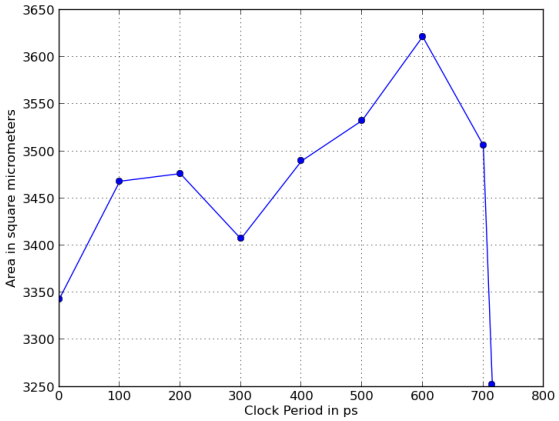

Figure 5.20: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 3342.92 square micrometre)** to 750ps (**Clock period at which timing slack is 0: Area = 3252.48 Square micrometre)**

- **Clock Period = 715ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	280	464.28	14.3
Buffer	46	84.28	2.6
Logic	830	2703.4	83.1
Sequential	0	0	0
Total	1156	3252.48	100

Table 5.101: Shows clock period 750ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 750ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.7 FIXED_POINT_ARITHMATIC_MODULE: Multiplier

- **Clock Period = 0ps *Timing Slack = -2090ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1685	3832.08	13.6
Buffer	344	1238.16	4.4
Logic	5533	23083.76	82.0
Sequential	0	0	0
Total	7562	28154	100

Table 5.102: Shows clock period 0ps with timing Violation -2090ps.

- **Clock Period = 500ps *Timing Slack = -1613ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1717	3809.96	14
Buffer	294	1034.6	3.8
Logic	5518	22369.2	82.2
Sequential	0	0	0
Total	7529	27213.76	100

Table 5.103: Shows clock period 500ps with timing Violation -1613ps.

- **Clock Period = 1000ps *Timing Slack = -1103ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1699	3798.2	14
Buffer	307	1068.76	3.9
Logic	5516	22264.2	82.1
Sequential	0	0	0
Total	7522	27131.16	100

Table 5.104: Shows clock period 1000ps with timing Violation -1103ps.

- **Clock Period = 1500ps *Timing Slack = -582ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1715	3942.12	14.1
Buffer	312	1098.44	3.9
Logic	5521	22984.92	82
Sequential	0	0	0
Total	7548	28025.48	100

Table 5.105: Shows clock period 1500ps with timing Violation -582ps.

- **Clock Period = 2000ps** ***Timing Slack = -85ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1773	3899.84	14
Buffer	370	1338.96	4.8
Logic	5390	22589.84	81.2
Sequential	0	0	0
Total	7533	27828.64	100

Table 5.106: Shows clock period 2000ps with timing Violation -85ps.

- **Clock Period = 2100ps** ***Timing Slack = -26ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1650	3700.76	13.8
Buffer	281	1020.88	3.8
Logic	5409	22100.12	82.4
Sequential	0	0	0
Total	7340	26821.76	100

Table 5.107: Shows clock period 2100ps with timing Violation -26ps.

- **Clock Period = 2150ps** ***Timing Slack = -2ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1562	3488.52	12.9
Buffer	289	1048.32	3.9
Logic	5435	22462.44	83.2
Sequential	0	0	0
Total	7286	26999.28	100

Table 5.108: Shows clock period 2150ps with timing Violation -2ps.

- **Clock Period = 2175ps** ***Timing Slack = -26ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1546	3180.52	12.7
Buffer	283	1002.68	4
Logic	5249	20796.72	83.3
Sequential	0	0	0
Total	7078	24979.92	100

Table 5.109: Shows clock period 2175ps with timing Violation -26ps.

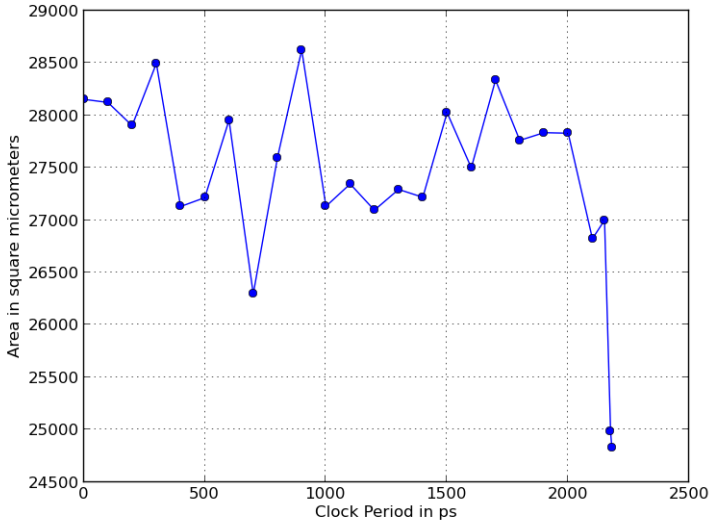

Figure 5.21: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 28154 square micrometre)** to 2180ps (**Clock period at which timing slack is 0: Area = 24832.64 Square micrometre)**

- **Clock Period = 2180ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1561	3282.16	13.2
Buffer	243	898.8	3.6
Logic	5443	20651.68	83.2
Sequential	0	0	0
Total	7247	24832.64	100

Table 5.110: Shows clock period 2180ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 2180ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.8 FIXED_POINT_ARITHMATIC_MODULE: Divider

- **Clock Period = 0ps** ***Timing Slack = -724ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	264	442.12	14.7
Buffer	40	71.4	2.4
Logic	756	1746.92	58.2
Sequential	131	741.16	24.7
Total	1196	3001.6	100

Table 5.111: Shows clock period 0ps with timing Violation -724ps.

- **Clock Period = 100ps** ***Timing Slack = -627ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	283	451.64	14.9
Buffer	40	76.16	2.5
Logic	755	1755.32	58.1
Sequential	131	739.76	24.5
Total	1209	3022.88	100

Table 5.112: Shows clock period 100ps with timing Violation -627ps.

- **Clock Period = 200ps** ***Timing Slack = -539ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	268	435.4	14.3
Buffer	37	68.32	2.2
Logic	758	1793.4	59
Sequential	131	741.16	24.4
Total	1194	3038.28	100

Table 5.113: Shows clock period 200ps with timing Violation -539ps.

- **Clock Period = 300ps** ***Timing Slack = -439ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	263	433.72	14.1
Buffer	40	71.4	2.3
Logic	753	1822.8	59.4
Sequential	131	741.44	24.2
Total	1187	3069.36	100

Table 5.114: Shows clock period 300ps with timing Violation -439ps.

- **Clock Period = 400ps** ***Timing Slack = -338ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	268	430.64	13.7
Buffer	43	99.68	3.2
Logic	760	1865.64	59.5
Sequential	131	738.64	23.6
Total	1202	3134.6	100

Table 5.115: Shows clock period 400ps with timing Violation -338ps.

- **Clock Period = 500ps** ***Timing Slack = -216ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	320	480.92	14.4
Buffer	64	121.24	3.6
Logic	753	2007.88	59.4
Sequential	131	764.68	22.6
Total	1268	3380.72	100

Table 5.116: Shows clock period 500ps with timing Violation -216ps.

- **Clock Period = 600ps** ***Timing Slack = -110ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	314	446.88	13.7
Buffer	73	139.72	4.3
Logic	697	1897.56	58.3
Sequential	131	768.88	23.6
Total	1215	3253.040	100

Table 5.117: Shows clock period 600ps with timing Violation -110ps.

- **Clock Period = 700ps** ***Timing Slack = -18ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	241	339.92	11.3
Buffer	85	143.08	4.7
Logic	666	1769.04	58.6
Sequential	131	764.4	25.3
Total	1123	3016.44	100

Table 5.118: Shows clock period 700ps with timing Violation -18ps.

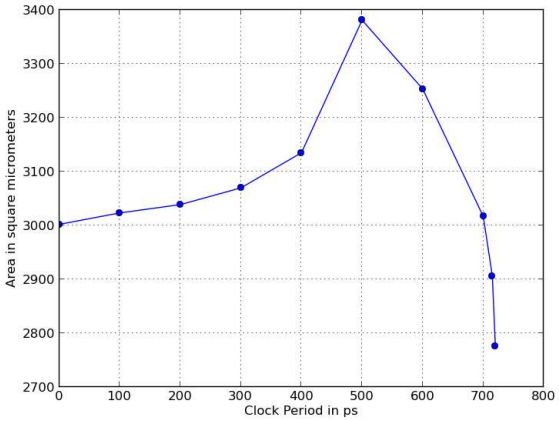

Figure 5.22: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 3001.6 square micrometre)** to 720ps (**Clock period at which timing slack is 0: Area = 2775.08 Square micrometre)**

- **Clock Period = 715ps *Timing Slack = -19ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	254	344.4	11.9
Buffer	68	116.76	4
Logic	662	1688.4	58.1
Sequential	131	756.28	26
Total	1115	2905.84	100

Table 5.119: Shows clock period 715ps with timing violation -19ps.

- **Clock Period = 720ps *Timing Slack = -0ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	242	322	11.6
Buffer	48	80.08	2.9
Logic	684	1617	58.3
Sequential	131	756	27.2
Total	1105	2775.08	100

Table 5.120: Shows clock period 720ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 720ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.9 FIXED_POINT_ARITHMATIC_MODULE:Twoscomp

- **Clock Period = 0ps *Timing Slack = -579ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	44	107.52	19.5
Buffer	36	51.8	9.4
Logic	98	391.16	71.1
Sequential	0	0	0
Total	178	550.48	100

Table 5.121: Shows clock period 0ps with timing Violation -579ps.

- **Clock Period = 100ps *Timing Slack = -483ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	48	82.32	16.7
Buffer	35	49.28	10
Logic	99	360.92	17.3
Sequential	0	0	0
Total	182	492.52	100

Table 5.122: Shows clock period 100ps with timing Violation -483ps.

- **Clock Period = 200ps *Timing Slack = -382ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	49	86.52	17.2
Buffer	35	49.28	9.8
Logic	99	365.96	72.9
Sequential	0	0	0
Total	183	501.76	100

Table 5.123: Shows clock period 200ps with timing Violation -382ps.

- **Clock Period = -284ps *Timing Slack = -439ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	51	90.44	17.6
Buffer	36	52.64	10.2
Logic	100	371.28	72.2
Sequential	0	0	0
Total	187	514.36	100

Table 5.124: Shows clock period 300ps with timing Violation -284ps.

- **Clock Period = 400ps** ***Timing Slack = -197ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	55	131.04	22.9
Buffer	37	45.36	7.9
Logic	97	394.8	69.1
Sequential	0	0	0
Total	189	571.2	100

Table 5.125: Shows clock period 400ps with timing Violation -197ps.

- **Clock Period = 500ps** ***Timing Slack = -94ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	50	86.520	16.2
Buffer	38	49.28	9.2
Logic	98	397.6	74.5
Sequential	0	0	0
Total	186	533.4	100

Table 5.126: Shows clock period 500ps with timing Violation -94ps.

- **Clock Period = 550ps** ***Timing Slack = -54ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	35	50.96	10.9
Buffer	34	38.08	8.1
Logic	98	378.84	81.0
Sequential	0	0	0
Total	1215	3253.040	100

Table 5.127: Shows clock period 550ps with timing Violation -54ps.

- **Clock Period = 600ps** ***Timing Slack = -9ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	46	86.52	18.9
Buffer	39	54.32	11.9
Logic	92	315.84	69.2
Sequential	0	0	0
Total	177	456.68	100

Table 5.128: Shows clock period 600ps with timing Violation -9ps.

- **Clock Period = 620ps** ***Timing Slack = -8ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	24	42	10.9
Buffer	34	38.08	9.9
Logic	87	304.64	79.2
Sequential	0	0	0
Total	145	384.72	100

Table 5.129: Shows clock period 620ps with timing violation -8ps.

- **Clock Period = 640ps** ***Timing Slack = -3ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	24	42	10.9
Buffer	34	38.080	9.9
Logic	87	304.64	79.2
Sequential	0	0	0
Total	145	384.72	100

Table 5.130: Shows clock period 640ps with timing Violation -3ps.

- **Clock Period = 645ps** ***Timing Slack = 0ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	36	80.36	19.5
Buffer	36	49.84	12.1
Logic	83	282.24	68.4
Sequential	0	0	0
Total	155	412.44	100

Table 5.131: Shows clock period 645ps with timing Violation 0ps.

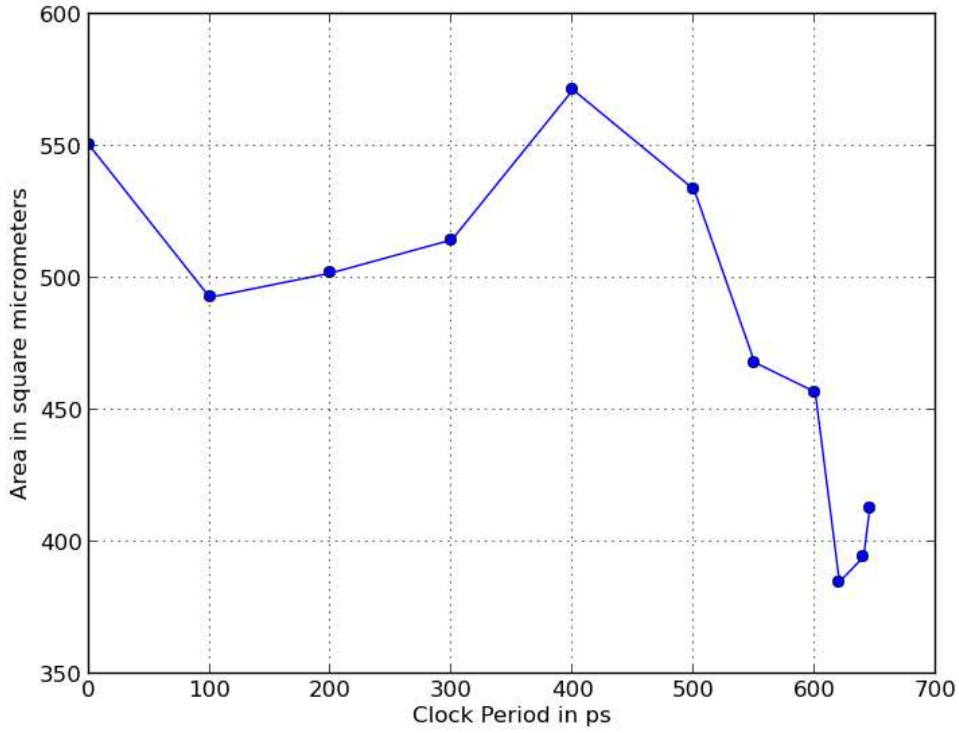

Figure 5.23: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 550.48 square micrometre)** to 645ps (**Clock period at which timing slack is 0: Area = 412.44 Square micrometre)**

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 645ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.10 FIXED_POINT_MATH_LIBRARY:Adder

- **Clock Period = 0ps *Timing Slack = -805ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	221	389.480	13.8
Buffer	36	52.9	1.9
Logic	770	2374.4	84.3
Sequential	0	0	0
Total	1027	2816.8	100

Table 5.132: Shows clock period 0ps with timing Violation -805ps.

- **Clock Period = 100ps *Timing Slack = -696ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	240	379.68	13.2
Buffer	26	36.68	1.3
Logic	804	2449.72	85.5
Sequential	0	0	0
Total	1070	2866.08	100

Table 5.133: Shows clock period 100ps with timing Violation -696ps.

- **Clock Period = 200ps *Timing Slack = -609ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	215	387.24	13.8
Buffer	30	42.84	1.5
Logic	790	2381.12	84.7
Sequential	0	0	0
Total	1035	2811.2	100

Table 5.134: Shows clock period 200ps with timing Violation -609ps.

- **Clock Period = 300ps *Timing Slack = -508ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	252	421.4	14.7
Buffer	18	29.12	1
Logic	799	2425.36	84.3
Sequential	0	0	0
Total	1069	2875.88	100

Table 5.135: Shows clock period 300ps with timing Violation -508ps.

- **Clock Period = 400ps** ***Timing Slack = -403ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	227	397.32	14.1
Buffer	25	37.24	1.3
Logic	773	2388.68	84.6
Sequential	0	0	0
Total	1025	2823.24	100

Table 5.136: Shows clock period 400ps with timing Violation -403ps.

- **Clock Period = 500ps** ***Timing Slack = -316ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	245	412.44	14.5
Buffer	30	43.68	1.5
Logic	775	2384.48	83.9
Sequential	0	0	0
Total	1050	2840.6	100

Table 5.137: Shows clock period 500ps with timing Violation -316ps.

- **Clock Period = 600ps** ***Timing Slack = -229ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	226	352.24	13.4
Buffer	22	35	1.3
Logic	706	2241.4	85.3
Sequential	0	0	0
Total	954	2628.64	100

Table 5.138: Shows clock period 600ps with timing Violation -229ps.

- **Clock Period = 700ps** ***Timing Slack = -98ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	253	438.76	14
Buffer	40	61.04	1.9
Logic	805	26241.24	84.1
Sequential	0	0	0
Total	1098	3141.04	100

Table 5.139: Shows clock period 700ps with timing Violation -98ps.

- **Clock Period = 750ps** ***Timing Slack = -47ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	225	447.72	14.1
Buffer	52	80.64	2.5
Logic	812	2638.72	83.3
Sequential	0	0	0
Total	1119	3167.08	100

Table 5.140: Shows clock period 750ps with timing violation -47ps.

- **Clock Period = 775ps** ***Timing Slack = -28ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	237	375.2	12.5
Buffer	48	77.56	2.6
Logic	781	2542.4	84.9
Sequential	0	0	0
Total	1066	2995.16	100

Table 5.141: Shows clock period 775ps with timing Violation -28ps.

- **Clock Period = 800ps** ***Timing Slack = -1ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	222	354.2	12.9
Buffer	32	45.64	1.7
Logic	758	2336.6	85.4
Sequential	0	0	0
Total	1012	2736.44	100

Table 5.142: Shows clock period 800ps with timing Violation -1ps.

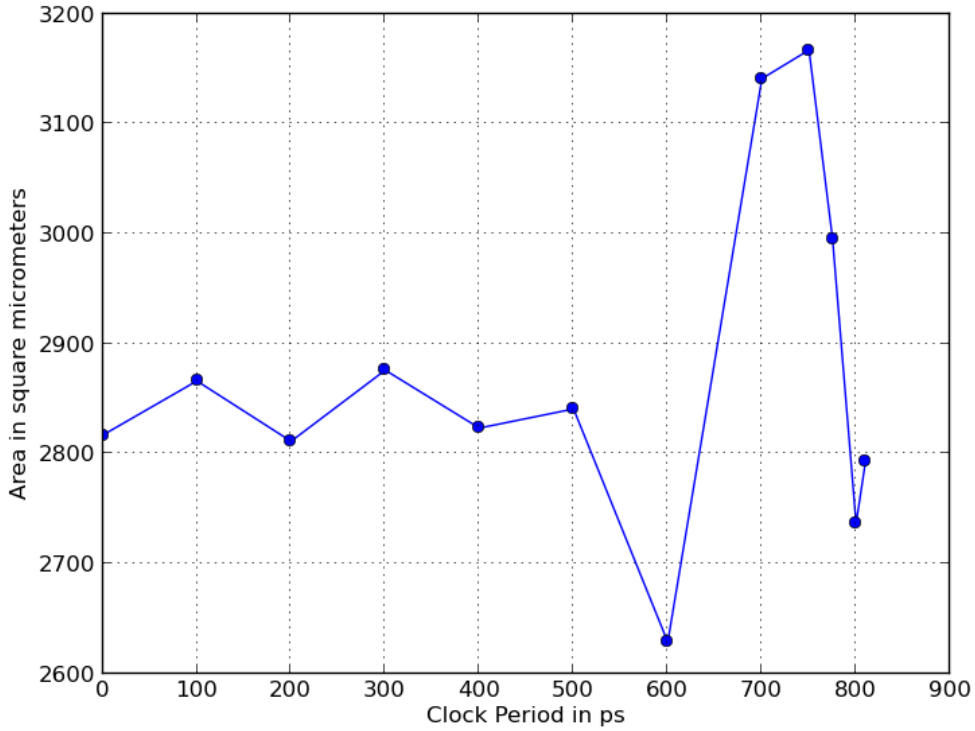

Figure 5.24: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 2816.8 square micrometre)** to 810ps (**Clock period at which timing slack is 0: Area = 2793 Square micrometre)**

- **Clock Period = 810ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	207	372.68	13.3
Buffer	20	34.72	1.2
Logic	728	2385.6	85.4
Sequential	0	0	0
Total	955	2793	100

Table 5.143: Shows clock period 810ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 810ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.11 FIXED_POINT_MATH_LIBRARY:Multiplier

- **Clock Period = 0ps** ***Timing Slack = -1486ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1479	3095.96	12.3
Buffer	313	993.16	4
Logic	5381	21018.76	83.7
Sequential	0	0	0
Total	7173	25107.88	100

Table 5.144: Shows clock period 0ps with timing Violation -1486ps.

- **Clock Period = 200ps** ***Timing Slack = -1264ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1503	3124.52	12.6
Buffer	309	975.52	3.9
Logic	5431	20742.68	83.5
Sequential	0	0	0
Total	7243	24842.72	100

Table 5.145: Shows clock period 200ps with timing Violation -1264ps.

- **Clock Period = 400ps** ***Timing Slack = -1072ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1498	3191.44	12.6
Buffer	307	922.88	3.6
Logic	5446	21286.12	83.8
Sequential	0	0	0
Total	7251	25400.48	100

Table 5.146: Shows clock period 400ps with timing Violation -1072ps.

- **Clock Period = 600ps** ***Timing Slack = -858ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1529	3185.84	12.5
Buffer	306	939.68	3.7
Logic	5450	21336.84	83.8
Sequential	0	0	0
Total	7285	25462.36	100

Table 5.147: Shows clock period 600ps with timing Violation -858ps.

- **Clock Period = 800ps** ***Timing Slack = -648ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1542	3352.16	13.1
Buffer	320	974.96	3.8
Logic	5454	21324.52	83.1
Sequential	0	0	0
Total	7316	25651.64	100

Table 5.148: Shows clock period 800ps with timing Violation -648ps.

- **Clock Period = 1000ps** ***Timing Slack = -453ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1618	3482.64	13.3
Buffer	318	1057	4
Logic	5478	21616	82.6
Sequential	0	0	0
Total	7414	26155.64	100

Table 5.149: Shows clock period 1000ps with timing Violation -453ps.

- **Clock Period = 1200ps** ***Timing Slack = -294ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1669	3602.2	13.3
Buffer	355	1150.8	4.3
Logic	5359	22312.08	82.4
Sequential	0	0	0
Total	7383	27065.08	100

Table 5.150: Shows clock period 1200ps with timing Violation -294ps.

- **Clock Period = 1400ps** ***Timing Slack = -35ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1708	3775.24	13.7
Buffer	277	1179.64	4.3
Logic	5377	22501.92	82
Sequential	0	0	0
Total	7362	27456.8	100

Table 5.151: Shows clock period 1400ps with timing Violation -35ps.

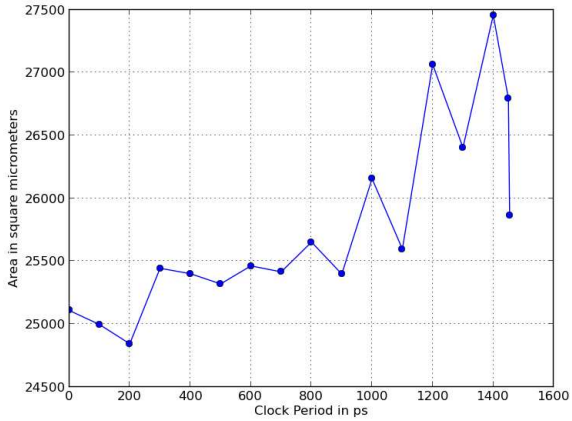

Figure 5.25: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 2816.8 square micrometre)** to 1454ps (**Clock period at which timing slack is 0: Area = 25861.08 Square micrometre)**

- **Clock Period = 1450ps *Timing Slack = -17ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1662	3639.16	13.6
Buffer	334	1178.8	4.4
Logic	5265	21975.24	82
Sequential	0	0	0
Total	7261	26793.2	100

Table 5.152: Shows clock period 1450ps with timing violation -17ps.

- **Clock Period = 1454ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	1530	3269.28	12.6
Buffer	276	1018.08	3.9
Logic	5204	21573.72	83.4
Sequential	0	0	0
Total	7010	25861.08	100

Table 5.153: Shows clock period 1454ps with timing Slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 1454ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.12 FIXED_POINT_MATH_LIBRARY:Divider

- **Clock Period = 0ps** ***Timing Slack = -768ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	491	775.04	12.82
Buffer	110	243.32	4
Logic	1489	3551.24	58.6
Sequential	205	1489.88	24.6
Total	2355	6059.48	100

Table 5.154: Shows clock period 0ps with timing Violation -768ps.

- **Clock Period = 100ps** ***Timing Slack = -669ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	515	846.16	13.4
Buffer	110	292.16	4.6
Logic	1491	3661	58.1
Sequential	265	1496.32	23.8
Total	2381	6296.08	100

Table 5.155: Shows clock period 100ps with timing Violation -669ps.

- **Clock Period = 200ps** ***Timing Slack = -568ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	512	817.88	13.2
Buffer	104	265.72	4.3
Logic	1481	3633.84	58.5
Sequential	265	1499.4	24.1
Total	2362	6216.84	100

Table 5.156: Shows clock period 200ps with timing Violation -568ps.

- **Clock Period = 300ps** ***Timing Slack = -468ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	516	865.2	13.6
Buffer	127	248.08	3.9
Logic	1497	3741.36	58.9
Sequential	265	1496.88	23.6
Total	2405	6351.52	100

Table 5.157: Shows clock period 300ps with timing Violation -468ps.

- **Clock Period = 400ps** ***Timing Slack = -362ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	519	867.44	13.3
Buffer	112	261.8	4
Logic	1508	3880.24	84.6
Sequential	265	1498.56	23
Total	2404	6508.04	100

Table 5.158: Shows clock period 400ps with timing Violation -362ps.

- **Clock Period = 500ps** ***Timing Slack = -280ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	476	833.28	13.5
Buffer	109	224	3.6
Logic	1468	3631.6	58.8
Sequential	265	1489.32	24.1
Total	2318	6178.2	100

Table 5.159: Shows clock period 500ps with timing Violation -280ps.

- **Clock Period = 600ps** ***Timing Slack = -182ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	571	868.84	13.9
Buffer	123	281.68	4.5
Logic	1372	3591.28	57.4
Sequential	265	1513.12	24.2
Total	2331	6254.92	100

Table 5.160: Shows clock period 600ps with timing Violation -182ps.

- **Clock Period = 700ps** ***Timing Slack = -74ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	507	743.12	12.5
Buffer	129	227.92	3.8
Logic	1332	3510.08	58.8
Sequential	265	1485.96	24.9
Total	2233	5967.08	100

Table 5.161: Shows clock period 700ps with timing Violation -74ps.

- **Clock Period = 750ps** ***Timing Slack = -26ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	406	581.84	10.7
Buffer	112	177.52	3.3
Logic	1296	3198.72	58.8
Sequential	265	1479.52	27.2
Total	2079	5437.6	100

Table 5.162: Shows clock period 750ps with timing violation -26ps.

- **Clock Period = 765ps** ***Timing Slack = -3ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	402	540.4	10.3
Buffer	119	208.88	4
Logic	1278	3024.28	57.7
Sequential	265	1470.56	28
Total	2064	5244.12	100

Table 5.163: Shows clock period 765ps with timing Violation -3ps.

- **Clock Period = 770ps** ***Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	386	472.64	9.9
Buffer	71	136.36	2.9
Logic	1266	2668.368	56.1
Sequential	265	1475.32	31
Total	1988	4753	100

Table 5.164: Shows clock period 770ps with timing Slack 0ps.

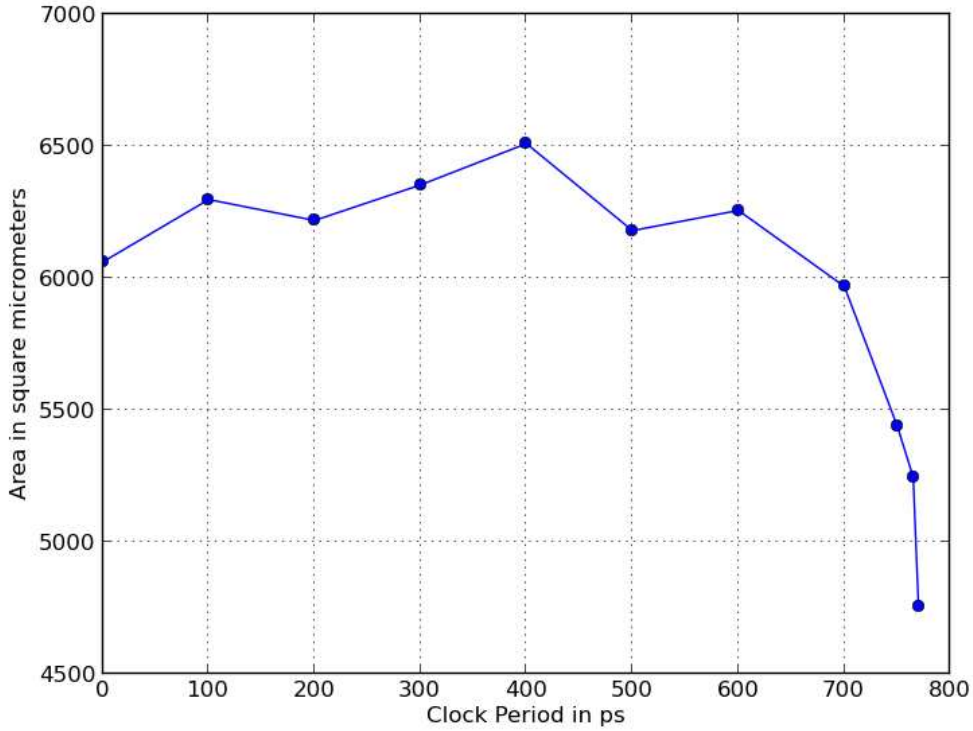

Figure 5.26: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 6059.48 square micrometre)** to 770ps (**Clock period at which timing slack is 0: Area = 4753 Square micrometre)**

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 770ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

5.5.13 FIXED_POINT_MATH_LIBRARY:Mults

- **Clock Period = 0ps** ***Timing Slack = -752ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	505	801.64	14.8
Buffer	108	225.12	4.2
Logic	1289	3249.4	60.1
Sequential	192	1127.84	20.9
Total	2094	5404	100

Table 5.165: Shows clock period 0ps with timing Violation -752ps.

- **Clock Period = 100ps** ***Timing Slack = -647ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	509	872.2	15.6
Buffer	10.5	223.16	4
Logic	1292	3365.04	60.2
Sequential	192	1128.4	20.2
Total	2098	5588.8	100

Table 5.166: Shows clock period 100ps with timing Violation -647ps.

- **Clock Period = 200ps** ***Timing Slack = -554ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	495	837.2	15
Buffer	103	228.48	4.1
Logic	12911	3405.92	60.8
Sequential	192	1128.12	20.1
Total	2081	5599.72	100

Table 5.167: Shows clock period 200ps with timing Violation -554ps.

- **Clock Period = 300ps** ***Timing Slack = -443ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	506	887.6	15.56
Buffer	115	224.28	3.9
Logic	1288	3466.96	60.7
Sequential	192	1133.16	19.8
Total	2101	5712	100

Table 5.168: Shows clock period 300ps with timing Violation -443ps.

- **Clock Period = 400ps** ***Timing Slack = -350ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	497	861.28	14.4
Buffer	145	368.76	6.2
Logic	1303	3605.28	60.4
Sequential	192	1133.44	19
Total	2137	5968.76	100

Table 5.169: Shows clock period 400ps with timing Violation -350ps.

- **Clock Period = 500ps** ***Timing Slack = -257ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	484	832.44	14.1
Buffer	124	312.76	5.3
Logic	1239	3610.6	61.3
Sequential	192	1134.84	19.3
Total	2039	5890.64	100

Table 5.170: Shows clock period 500ps with timing Violation -257ps.

- **Clock Period = 600ps** ***Timing Slack = -165ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	484	765.8	14
Buffer	117	221.76	4.1
Logic	1181	3348.8	61.3
Sequential	192	1129.52	20.7
Total	1974	5465.88	100

Table 5.171: Shows clock period 600ps with timing Violation -165ps.

- **Clock Period = 700ps** ***Timing Slack = -38ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	531	804.16	14
Buffer	158	285.88	5
Logic	1267	3534.44	61.5
Sequential	192	1121.4	19.5
Total	2148	5745.88	100

Table 5.172: Shows clock period 700ps with timing Violation -38ps.

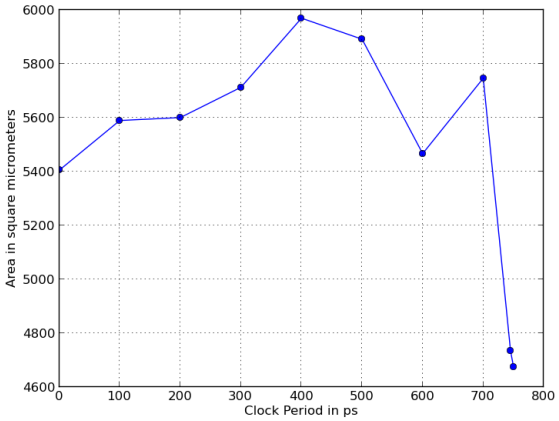

Figure 5.27: Shows Variation of ASIC size with variation of timing constraint from 0ps(**Area = 5404 square micrometre)** to 775ps (**Clock period at which timing slack is 0: Area = 4673.76 Square micrometre)**

- **Clock Period = 745ps *Timing Slack = -0ps (Timing Violation)**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	448	577.08	12.2
Buffer	85	152.06	3.2
Logic	1196	2895.76	61.2
Sequential	192	1109.08	23.4
Total	1921	4733.96	100

Table 5.173: Shows clock period 745ps with timing violation -0ps.

- **Clock Period = 750ps *Timing Slack = 0ps**

$Gates(Type)$	$Instances$	$Area$	$Area(\%)$
Inverter	464	589.96	12.6
Buffer	108	182.56	3.9
Logic	1151	2799.44	59.9
Sequential	192	1101.8	23.6
Total	1915	4673.76	100

Table 5.174: Shows clock period 750ps with timing slack 0ps.

Discussion :

From the above tables and figure, As we increase the clock period from 0ps to 775ps, Area is different for different clock periods but if we compare the area from clock period 0ps to clock period at which the timing slack is 0,the area is decreased. This clearly indicates in case of ASIC, area is decreased from clock period 0ps to clock period at which the timing constraint is 0.

CHAPTER 6

CONCLUSIONS

1. Variation of Power in ASIC and FPGA with timing constraint are studied and reported.

2. Variation of ASIC and FPGA size with timing constraint are studied and reported.

3. Understood the difference between ASIC and FPGA interms of power and area.

CHAPTER 7

References

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