Effect of Parasitics in High Voltage Bipolar Flyback Converter for Lightly Loaded Resistive Loads

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THESIS CERTIFICATE

This is to certify that the thesis titled **Effect of Parasitics in High Voltage Bipolar Flyback Converter for Lightly Loaded Resistive Loads**, submitted by **Kunchala Siva Prasad**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Flyback; Parasitics; Network Analyser; Minimum Voltage Switching.

In high voltage (HV) flyback charging circuits, the importance of transformer parasitics holds a significant part in the overall system parasitics. The resonance between inductance and capacitance, cause significant deviations in voltage gain. This effect is predominant in the case of very lightly loaded high voltage flyback converters when used for bipolar output voltages. In this report, two circuit configurations are proposed to obtain the bipolar output voltage from a high voltage (HV) flyback for lightly loaded circuits. The operational similarities and the advantages/limitations of the two approaches are presented. The effect of Transformer winding capacitance on the achievable gain in a bipolar operation is analyzed in both the approach. The analysis is verified in simulation and hardware implementation for high voltage bipolar flyback converters with valley mode switching to achieve minimum switching loss and device stress.

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ABBREVIATIONS

DCM	Discontinuous conduction mode
CCM	Continuous conduction mode
HV	High voltage
LV	Low voltage
SMPC	Switch Mode Power Converters
CPLD	Complex Programmable Logic Device
DSP	Digital Signal Processor
ZVS	Zero Voltage Switching
MOSFET	Metal Oxide Silicon Field Effect Transistor
PCB	Printed Circuit Board
USB	Universal Serial Bus
GPIO	General Purpose Input and Output

NOTATION

L_m	Magnetizing inductance
C_r	Resonant capacitance referred to primary
P_1	Primary side switch
S_1	Approach 1 secondary side first winding switch
S_2	Approach 1 secondary side second winding switch
D_{b1}	Blocking diode corresponds to S_1
D_{b2}	Blocking diode corresponds to S_2
V_g	Input voltage
V_0	Output voltage
Z_c	Characteristic impedance
w_r	Resonant frequency
n	Transformer turns ratio
C_{w1}	Winding capacitance corresponds to first secondary
C_{w2}	Winding capacitance corresponds to second secondary
C_{d1}	Device capacitance corresponds to D_{b1}
C_{d2}	Device capacitance corresponds to D_{b2}
C_{s1}	Device capacitance corresponds to S_1
C_{s2}	Device capacitance corresponds to S_2
C_p	Device capacitance corresponds to P_1

CHAPTER 1

INTRODUCTION

Among DC-DC converters, high voltage low power converters find application in printers, cathode ray tubes(CRT) in TVs, monitors, and ion deflectors etc. Further, high voltage bipolar power supplies serve many applications like deflecting the ions in both directions in ion deflectors [9] etc. For high voltage low power operations, flyback converter is commonly used [3]. This is due to its simplicity and low element count. Detailed analysis of flyback converter is given in [1]-[3]. Flyback converter operating in discontinuous conduction mode (DCM) ensures complete energy transfer from primary side to secondary side of the converter. In DCM operation, minimum switch voltage turn ON is possible. The flyback converter voltage gain when operating in DCM is more than that in CCM [3].

In HV applications, the parasitic elements, namely leakage inductance and winding capacitance of the power transformer have a significant influence on the converter operation. Usually, only the effect of leakage inductance of the transformer is accounted for in literature and the effect of transformer stray capacitance is neglected. However, in the case of high voltage low power applications, the effect of stray winding capacitance cannot be ignored. The effect of winding capacitance gets magnified by the high turns ratio when seen from the primary side. The low-frequency oscillation of energy between magnetising inductance and stray winding capacitance consumes a significant portion of energy in every switching cycle, which therefore cannot be neglected. Conventional wire wound magnetic transformers cannot achieve high power rating and compact size simultaneously in SMPC applications. In recent days, research on planar transformers has gained attention. Planar magnetics aid in achieving the significant reduction in both size and interwinding capacitance compared to the conventional transformer. Owing to its advantages and suitability in this work, an attempt to design a planar transformer based flyback converter was carried out. Planar transformer of N87 material with the ELP22/6/16 core has been designed and built to meet the requirements.

In order to achieve bipolar high voltage across a single load, the conventional flyback topology cannot be used. Since the requirement is to obtain a controllable bipolar output voltage from the same converter, it is proposed in this thesis that two conventional flyback converters be connected suitably. Therefore, two flyback based converter configurations are proposed and analysed in this thesis.

Chapter 2 describes the two topologies which are suitable to achieve a high voltage low power bipolar supply. Each converter configuration is analysed and the merits and demerits of the topologies are highlighted.

Chapter 3 discusses the effect of transformer parasitics in the converter based on mathematical analysis . This chapter also compares the values of the parasitic elements in both the configurations.

Chapter 4 presents the control algorithm for the converter topologies. This chapter also describes the design of CPLD control card for the hardware implementation of the control algorithm.

Chapter 5 presents the simulation results of the two topologies and compares their performance.

Chapter 6 discusses the hardware implementation for selected topologies. Experimental results are used to validate the suitability of the proposed configurations.

CHAPTER 2

TOPOLOGY ANALYSIS

Various configurations each with distinct advantages and disadvantages have been presented in the literature [1]-[5]. Switched Mode Power Conversion topologies with high switching frequency are preferred to achieve high performance with reduced cost and size. Converter topologies with inherent boost capability are the fundamental basis for topology selection for voltage step up requirements. Flyback converters are best suited for voltage levels less than 10kV and power levels less than 100W. Some attractive features of flyback include: isolation between load and source side, requirement of only a capacitive filter, compact with the lesser component count etc [2]. Resonant converter topologies are also suited for obtaining high voltages [5]. The family of resonant topologies include: parallel resonant converters (PRC) , Phase shifted bridge, Multi element resonant converters. In parallel resonant converters, the current flowing in the primary side is independent of the load. The efficiency of PRC cannot be maintained at varying loads or varying input voltage conditions. Further, it requires a filter inductor at the high voltage side whose size becomes comparable to the high voltage transformer. Multi-element resonant converters, though combine the merits of series and parallel resonant topologies, suffer from circuit complexity and difficulty in control. In short, resonant converters could partially or wholly use the transformer parasitics to achieve soft switching, yet present a complicated circuitry. Considering the application requirements, flyback based converter topology is the potential candidate for implementation. Further, the sinusoidal switch voltage oscillations due to the parasitics could be utilised to achieve ZVS thus minimising the turn-on loss.

Two converter configurations for obtaining a bipolar output voltage with a high voltage flyback converter operating in DCM with minimum voltage switching is presented in the sections below.

2.1 Circuit Configuration 1

In this configuration, the two winding transformer in conventional flyback converter is replaced with a three winding transformer. This three winding transformer will comprise of one primary and two secondary windings. Through controllable switches, two secondary windings will be connected across the load in such a way that, one secondary will give positive voltage and other will give negative voltage, individually as shown Fig.2.1. Secondary side MOSFETs need to be rated for higher voltages because when the switch S_1 is in conduction, the switchS_2 is required to handle twice the output voltage across it and vice versa. The secondary side floating MOSFETs also require high side gate driving circuits.These high side gate drivers require proper bootstrap capacitors.

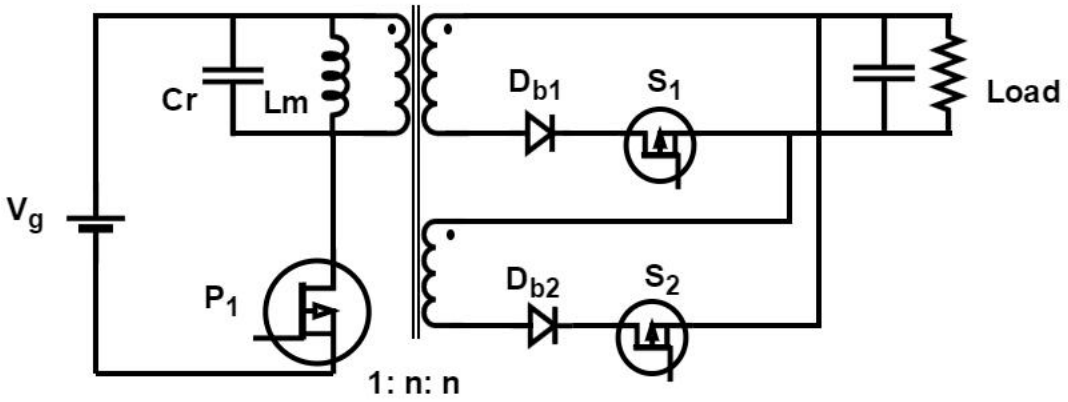

Figure 2.1: Configuration 1, flyback converter with three winding transformer

2.2 Circuit Configuration 2

In this approach, two individual flyback converters will be connected in a modular fashion. Outputs of two modules will be connected in anti-series manner as shown in Fig.2.2. The converter operational modes will be decided by the requirement of output voltage, either positive or negative. All the individual modules are similar to each other. Analysis of one module will be sufficient to judge the performance of the total converter. In this configuration, controllable switches are not required on the high voltage side, which makes the converter much simpler. The component count on the low

voltage side will double in this configuration, but high voltage side component count is reduced. For controlling the output voltage, switch control on the primary side is sufficient. Switching stresses will be lower in this configuration.

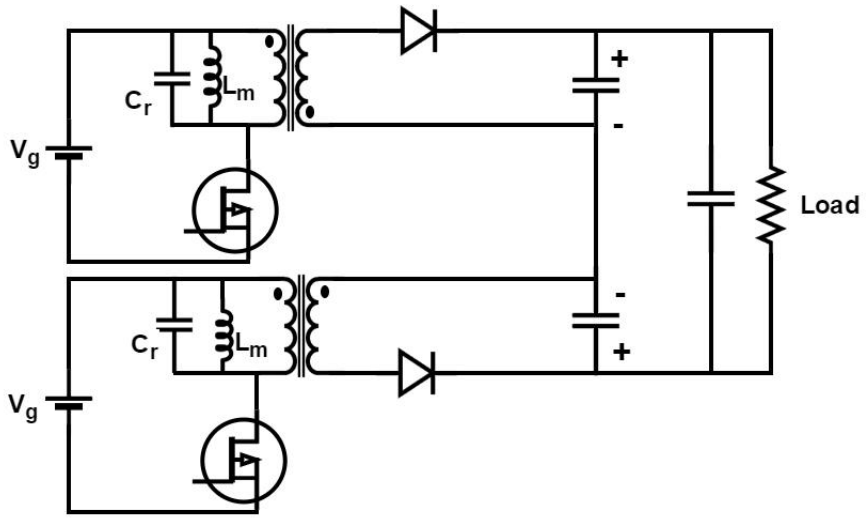

Figure 2.2: Configuration 2, two flyback converters in modular approach.

CHAPTER 3

OPERATIONAL MODES

The converter operational modes are similar for the both configurations [5]. In the second configuration, the analysis of one module is sufficient since both the modules are identical. In both configurations, the characteristic impedance Z_c, and resonant frequency w_r will be different and can be calculated from the knowledge of device capacitances and transformer parameters. The operational modes for configuration 1 are explained in this chapter, and these are same for configuration 2, except for mode 3.

In the analysis of operational modes at steady state, the following assumptions are made

1. The semiconductor devices are ideal, i.e., there is no forward voltage drop in the on-state, no leakage current in the off-state, and no time delay at both turn-on and turn-off.

2. The converter is operated in the discontinuous conduction mode (DCM).

3. The output capacitance C_0 is sufficiently large. Therefore the output voltage can be assumed to be a constant DC voltage during the switching period T_s.

4. The following variables are defined as follows:

Characteristic impedance $Z_c = \sqrt{\frac{L_m}{C_r}}$

Resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_m C_r}}$

3.1 Computation of Resonant Capacitance

Parasitic capacitance of each switching element and that of the transformer winding plays a major role in this converter. To avoid complexity in the analysis all parasitic capacitances are referred to the primary side and the secondary side can be considered as ideal. The circuit diagram with parasitic capacitances is shown in Fig.3.1.

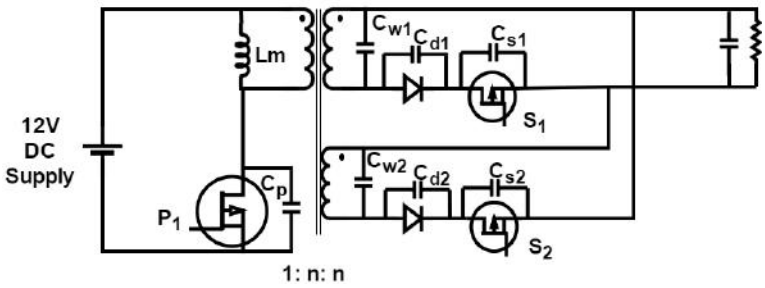

Figure 3.1: Circuit diagram of flyback converter with one primary and two secondaries with parasitic capacitances

Equivalent capacitance on each secondary side will be

$$C_1 = C_{w1} + \frac{C_{d1}C_{s1}}{C_{d1} + C_{s1}} \tag{3.1}$$

$$C_2 = C_{w2} + \frac{C_{d2}C_{s2}}{C_{d2} + C_{s2}} \tag{3.2}$$

And the total capacitance referred to primary will be given as

$$C_r = C_p + n^2(C_1 + C_2) \tag{3.3}$$

3.2 Mode 1

During this mode P_1 starts conducting through magnetizing inductance L_m, it takes the path $source - L_m - switch$. The current through L_m increases linearly. Peak value of this current depends upon T_{on}. During this period, load capacitance will maintain the output voltage. At the starting stage, in this mode (that is in first few switching cycles) the inductor current starts from zero and after a few cycles, it starts from a negative value.

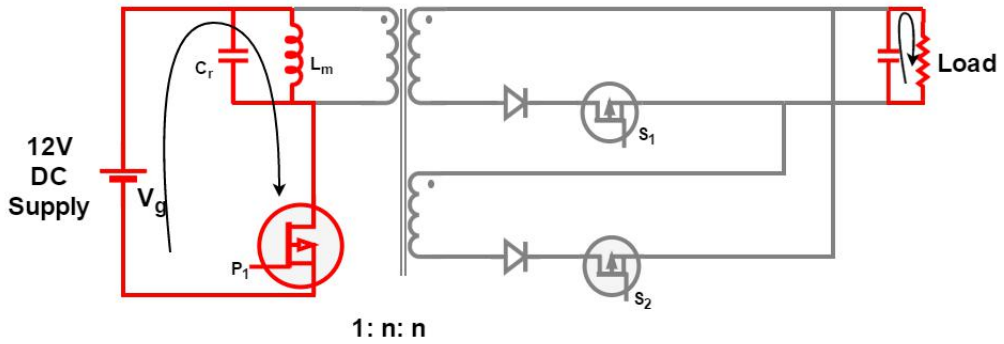

Figure 3.2: Charging interval of configuration 1.

3.3 Mode 2

After the switch P_1 is turned OFF, energy stored in magnetizing inductance L_m is not transferred immediately, this is because the secondary side switches are not in forward bias. During this period, L_m resonates with the resonant capacitor C_r. At the end of this mode the voltage across L_m will reach $\frac{-V_0}{n}$, and switches will become forward biased.

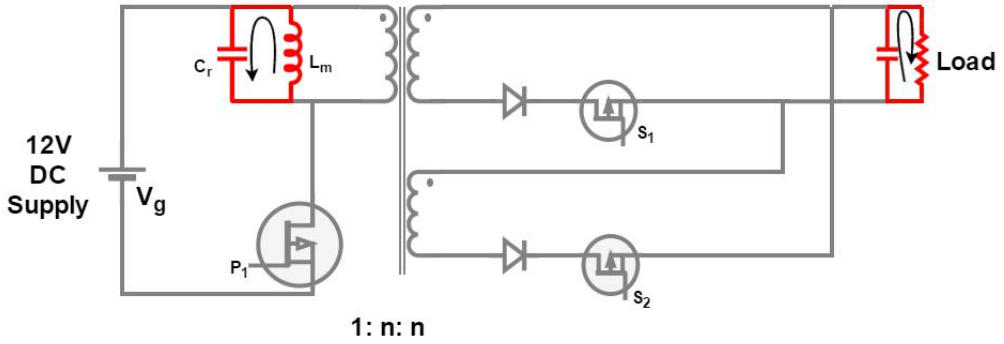

Figure 3.3: First resonant interval of configuration 1.

In this resonant interval the equations for voltage across the magnetizing inductance and current through it is given by (3.4)(3.5)

$$v_{cr}(t) = V_g cosw_r t - i(t_1) sinw_r t \tag{3.4}$$

$$i_{Lm}(t) = \frac{V_g}{Z_c} sinw_r t + i(t_1) cosw_r t \tag{3.5}$$

In this mode, output voltage is maintained by the energy stored in the capacitor. At the end of this mode, secondary side switches will be forward biased. Based on the requirement, one of the MOSFETs will be turned ON by application of the gate pulse.

3.4 Mode 3

During this mode, depending upon the polarity of the output voltage, secondary side switches will controlled. Energy stored in magnetising inductance is transferred to the load at end of this mode. This mode is also called as discharge mode. The voltage across L_m remains constant at $-nV_0$.

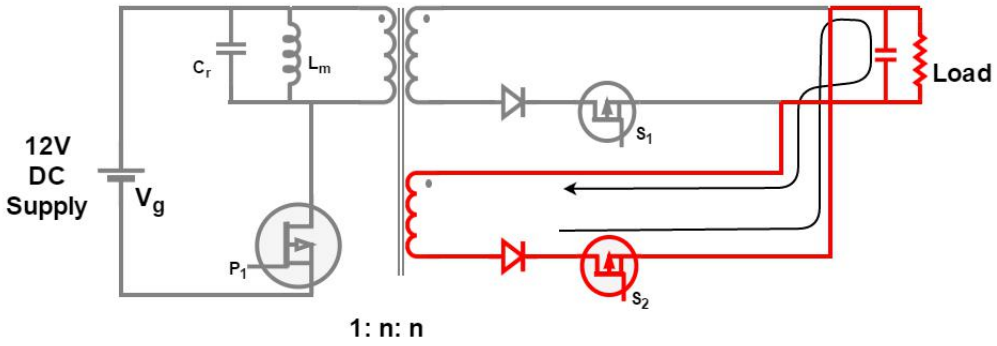

Figure 3.4: Discharge interval of configuration 1.

In the second configuration, each module has only one secondary winding, hence, there is no requirement for selection of switch for control. The transformer winding will discharge the energy through the load.

3.5 Mode 4

After the energy stored in L_m is completely discharged to the load, the voltage across the primary switch will be at $V_g + \frac{V_0}{n}$. Again resonance occurs with C_r and L_m. This mode continues till voltage across the primary switch falls to a minimum value. This will ensure minimum voltage switching.

During this mode, equations for voltage across magnetizing inductance and current is given by (3.6)(3.7)

$$v_{cr}(t) = -\frac{V_0}{n} cosw_r t \tag{3.6}$$

$$i_{Lm}(t) = -\frac{V_0}{nZ_c} sinw_r t \tag{3.7}$$

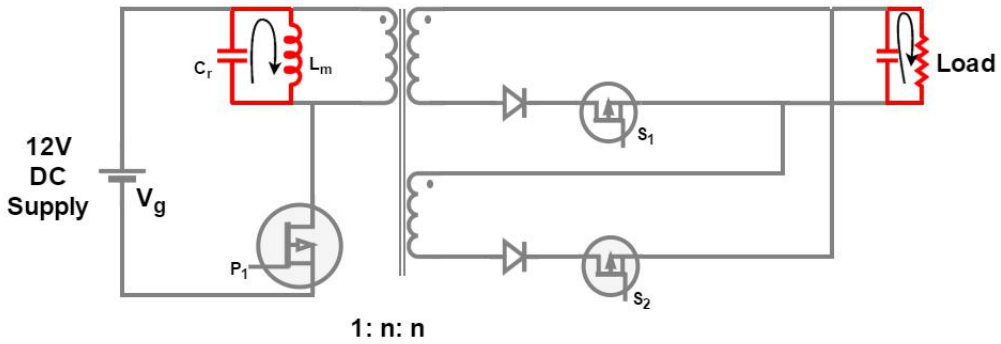

Figure 3.5: Second resonant interval of configuration 1.

overall end expression is given by (3.8)

$$V_0 = nV_g\left(\frac{(t_{on}+t_z)w_r + sin(\theta_2) + \frac{Z_c i_1}{V_g}cos(\theta_2)}{w_r t_d + sin\theta_4}\right) \tag{3.8}$$

where,

Characteristic impedance $Z_c = \sqrt{\frac{L_m}{C_r}}$

Resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_m C_r}}$

t_z = delay time to ensure ZVS of switch

i_1 = peak current reached after mode 1

θ_2 = mode 2 duration in radians

t_d = diode turn on time.

CHAPTER 4

PARASITICS ANALYSIS

For high voltage and frequency operation, the effect of parasitics is high. Parasitics elements in this converter are the leakage inductance and self-capacitance of the transformer. These parasitics are more significant in the case of wire wound transformer. In the planar transformer, the effect of these elements will be less. When compared to a two winding transformer, effect of these parasitics are more in the case of three winding transformer. These parasitic elements can be calculated using the network analyser, this process is called as transformer characterization. Using the network analyser, the system frequency response can be plotted.

To find transformer parameters, characterization of the transformer is required using the network analyser,i.e, frequency response of transformer is required .To characterise the transformer APLAB Network analyser of frequency range 10Hz to 30MHz has been employed. To compute the parameters, the following two separate tests results are required

a. Sinusoidal signal with variable frequency applied to Primary side, and Secondary side kept Open.

b. Sinusoidal signal with variable frequency applied to Primary side, and Secondary side short.

After obtaining all the results, analysis is done using bode plots. To understand the effect of the two secondary windings one on the other it is required to characterise two types of transformers i.e., the transformer with one primary and one secondary winding, and transformer with one primary and two secondary windings.

4.1 Configuration 1: Characterization of Transformer

Network analyser has three output probes, one will power the circuit, other two probes namely A and B will sense the current through externally connected 1Ω resistor and

voltage across the externally connected 1Ω resistor respectively. The network analyser does B/A operation with the sensed signals and produces the bode plots.

A planar transformer with 4 turns primary and two 36 turn secondary windings has been used. The characterization as follows,

4.1.1 Secondary Windings Open

In this case, significant parameters are primary resistance(R_p), magnetizing inductance(L_m), and secondary side parasitic capacitances(C_{w1},C_{w2}). To perform the bode analysis, the equivalent circuit model is required and it can be obtained by referring secondary side elements to primary side with 'n^2' factor. The equivalent circuit can be define with

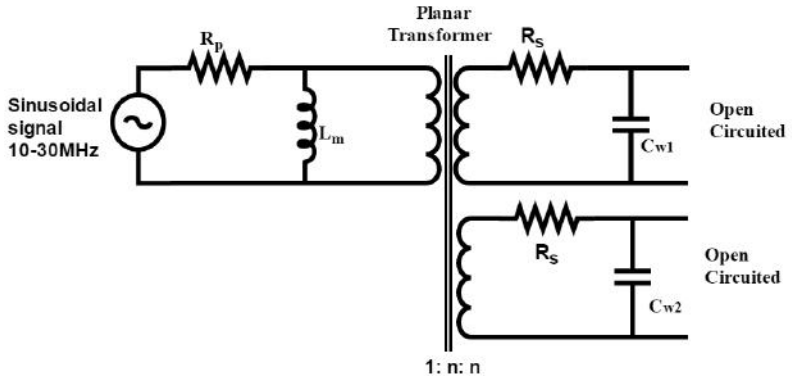

Figure 4.1: Equivalent circuit diagram for two secondary side windings open

following equation,

$$(sL_m + R_p) \parallel \frac{1}{sn^2C_{w1}} \parallel \frac{1}{sn^2C_{w2}} \tag{4.1}$$

It can be equivalently represented as,

$$(sL_m + R_p) \parallel \frac{1}{sn^2(C_{w1} + C_{w2})} \tag{4.2}$$

It is noted that two secondary windings are identical in all respect, therefore, it can be assumed that $C_{w1} \approx C_{w2}$. By solving this equation,

$$\frac{(s + \frac{R_p}{L_m})}{s^2 + \frac{R_p}{L_m}s + \frac{1}{n^2(C_{w1}+C_{w2})L_m}} \tag{4.3}$$

From (4.3), bode plot can be obtained, and the initial system gain, and corner frequencies as follows,

$$r_p = 20log(R_p)dB \tag{4.4}$$

$$f_1 = \frac{R_p}{2\pi L_m} Hz \tag{4.5}$$

$$f_2 = \frac{1}{2\pi\sqrt{n^2(C_{w1} + C_{w2})L_m}} Hz \tag{4.6}$$

The impedance characteristic plot for the first configuration with secondary windings open is shown in Fig.4.2, From figure and the equations we can calculate the fol-

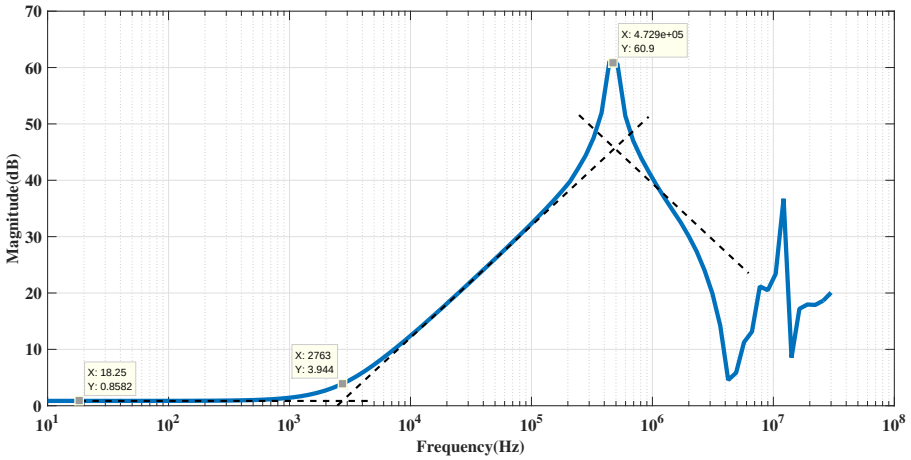

Figure 4.2: Impedance characteristics of transformer with secondary side windings open

lowing parameters

4.1.2 Secondary Windings Short

When secondary is short circuited, the significant parameters are primary resistance(R_p),secondary resistance(R_s) and leakage inductance(L_{lkp}). The equivalent circuit can be can be derived as all elements are in series. The transfer function is

$$sL_{lkp} + R_p + \frac{R_s}{2n^2}$$

From this transfer function, initial magnitude, and corner frequency can be derived equivalent to bode plot as follows,

$$r_s = 20log(R_p + \frac{R_s}{2n^2})dB$$

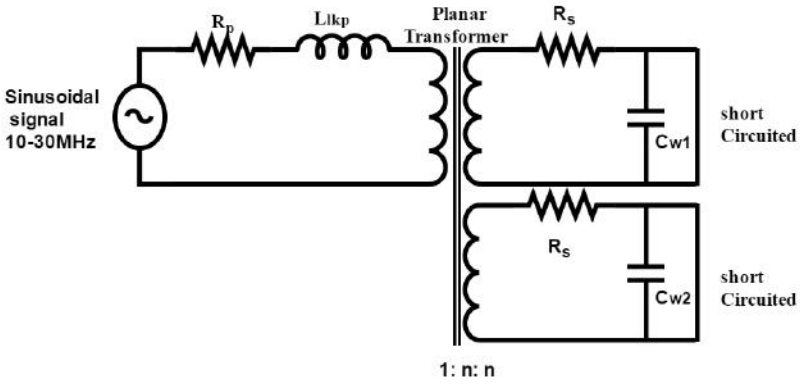

Figure 4.3: Equivalent circuit diagram for two secondary side windings short

$$f_3 = \frac{R_p + \dfrac{R_s}{2n^2}}{2\pi L_{lkp}} Hz$$

The impedance characteristic plot for the first approach with secondary windings short is as shown below,

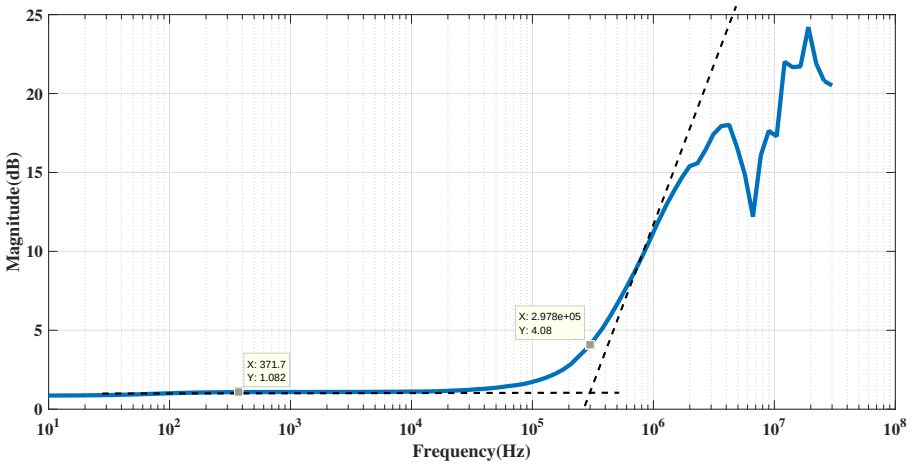

Figure 4.4: Impedance characteristics of transformer with secondary side windings short

Equivalent capacitance on each secondary side will be

$$C_1 = C_{w1} + \frac{C_{d1}C_{s1}}{C_{d1} + C_{s1}}$$

$$C_2 = C_{w2} + \frac{C_{d2}C_{s2}}{C_{d2} + C_{s2}}$$

And the total capacitance referred to primary will be given by

$$C_r = C_p + n^2(C_1 + C_2)$$

Here,

C_p= Primary MOSFET capacitance

C_{d1}, C_{d2}= Blocking diode capacitances

C_{s1}, C_{s2}= Secondary MOSFET capacitances

4.2 Configuration 2: Characterization of Transformer

The characterization of two winding transformer is also similar as depicted in earlier section. A planar transformer with 4 turn primary and 36 turn secondary winding has been used. The characterization as follows,

4.2.1 Secondary Winding Open

When transformer secondary is open circuited, significant parameters are primary resistance(R_p), magnetizing inductance(L_m), and secondary side parasitic capacitance(C_w). To do the bode analysis, the equivalent circuit model is required and it can be obtained by referring secondary side elements to primary side with 'n^2' factor.

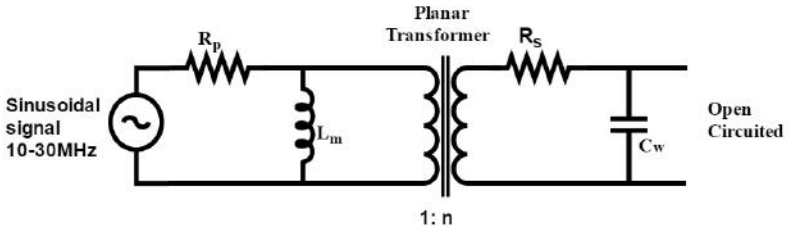

Figure 4.5: Equivalent circuit diagram for secondary side winding open

Primary resistance(R_p) is not external resistance it is internal resistance of primary winding, so equivalent connection of R_p and L_m is series. Total equivalent circuit reproduced by

$$(sL_m + R_p) \parallel \frac{1}{sn^2C_w} \tag{4.7}$$

By solving this equation,

$$\frac{(s + \frac{R_p}{L_m})}{s^2 + \frac{R_p}{L_m}s + \frac{1}{n^2C_wL_m}} \tag{4.8}$$

From this equation bode plot can be obtained, and initial system gain, and corner frequencies are,

$$r_p = 20log(R_p)dB \tag{4.9}$$

$$f_1 = \frac{R_p}{2\pi L_m} Hz \tag{4.10}$$

$$f_2 = \frac{1}{2\pi\sqrt{n^2 C_w L_m}} Hz \tag{4.11}$$

The impedance characteristic plot for the second approach with secondary winding open is as shown in Fig.4.6,

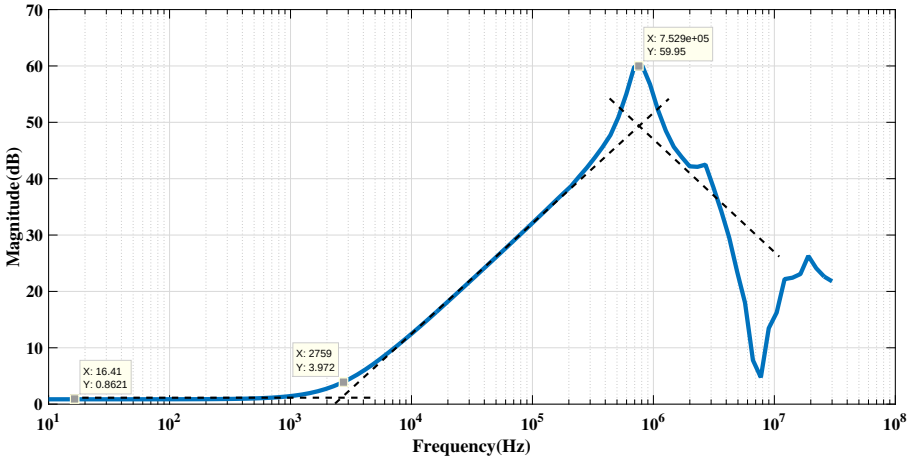

Figure 4.6: Impedance characteristics of transformer with secondary side winding open

4.2.2 Secondary Winding Short

When secondary is short circuited, significant parameters are primary resistance(R_p), secondary resistance(R_s) and leakage inductance(L_{lkp}). The equivalent circuit can be

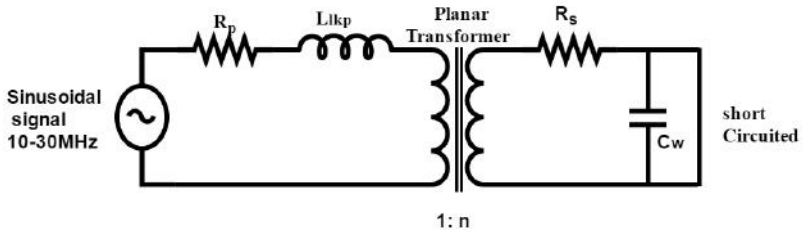

Figure 4.7: Equivalent circuit diagram for secondary side winding short

framed to be all elements are in series. And the transfer function as shown in (4.12),

$$sL_{lkp} + R_p + \frac{R_s}{n^2} \tag{4.12}$$

From this transfer function initial magnitude, and corner frequencies can be derived equivalent to bode plot as follows,

$$r_s = 20log(R_p + \frac{R_s}{n^2})dB \tag{4.13}$$

$$f_3 = \frac{R_p + \frac{R_s}{n^2}}{2\pi L_{lkp}} Hz \tag{4.14}$$

The impedance characteristic plot for the second approach with secondary winding short is as shown in Fig.4.8,

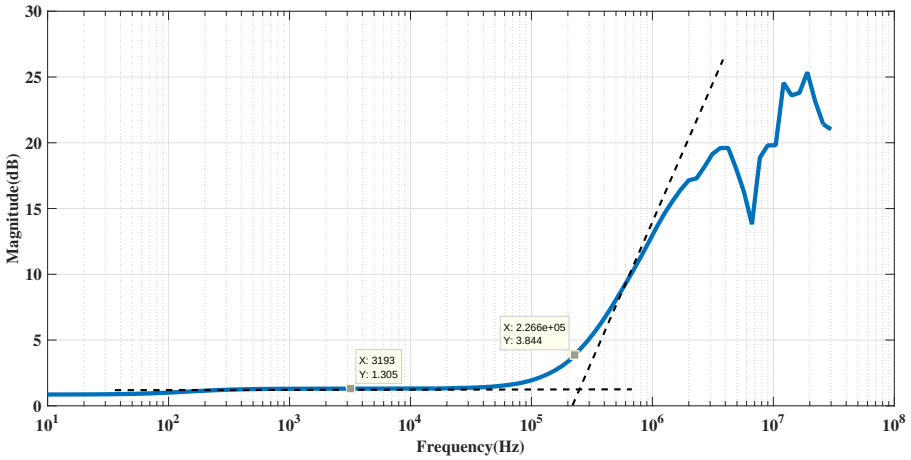

Figure 4.8: Impedance characteristics of transformer with secondary side short

The total capacitance referred to primary will be given as,

$$C_r = C_p + n^2(C_w + C_d)$$

Here,

C_p= Primary MOSFET capacitance

C_d= Blocking diode capacitance

C_s= Secondary MOSFET capacitance

Table 4.1: Results comparison of configuration 1, configuration 2 transformers

Transformer parameter	Configuration 1 transformer	Configuration 2 transformer
R_p	0.1038Ω	0.104Ω
L_m	$63.60\mu H$	$63.72\mu H$
C_w	$22.061pF$	$8.6851pF$
R_s	4.7213Ω	4.6821Ω
L_{lkp}	$0.6063\mu H$	$0.817\mu H$

From table.4.1 it is clear that presence of second secondary winding increasing the parasitic capacitance.

CHAPTER 5

CONTROL ALGORITHM

Converters operation is generally classified as Continuous (CCM) or Discontinuous (DCM) depending on continuity of the inductor current. In high voltage low power applications, energy oscillates in the converter, the effect of winding capacitance of the transformer is explained before and the converter enters into the absolute DCM at a very low frequency. Absolute DCM in this context is defined as the region where all the natural oscillations of the converter completely damp out and the energy stored in the magnetizing inductance becomes zero. On the other hand, operation in CCM demands higher switching frequencies, also other higher switching stress. Valley mode switching scheme is proposed to be the efficient control scheme for converters with similar behaviour as flyback converter. In this chapter valley mode switching along with fixed on time control is proposed and implemented.

5.1 Valley Mode Switching

Minimum switch voltage mode switching scheme is proposed to be the suitable control scheme to minimize switching losses in the converters. Generally, the converter operation can be viewed as two regions.1) Low Voltage Region (LV) where the output voltage $V_0 < nV_g$. 2) High Voltage Region (HV) where the output voltage $V_0 > nV_g$. Minimum switch voltage mode switching ensures turning on the converter at minimum switch voltage in LV region and at Zero Voltage zone in HV region.

In the minimum switch voltage mode switching can be realized by the above-mentioned algorithm. The basic requirement of zero voltage switching is sensing the voltage across the primary switch by using the resistor divider. And compare with the input voltage of the converter. The comparator output is given with appropriate primary delay by calculating the resonant frequency minimum voltage point can be sensed. This is because comparison is done with input voltage not with minimum voltage.

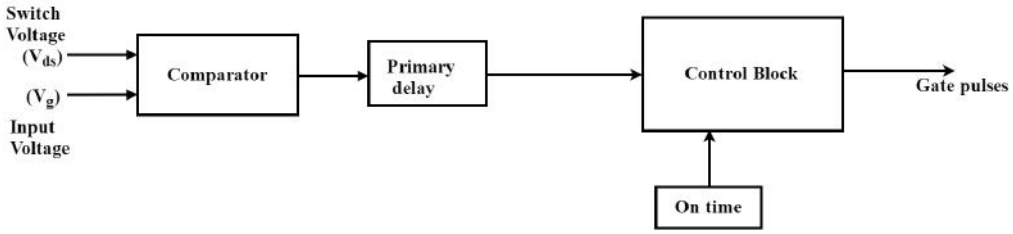

Figure 5.1: Block diagram for Minimum switch voltage mode switching

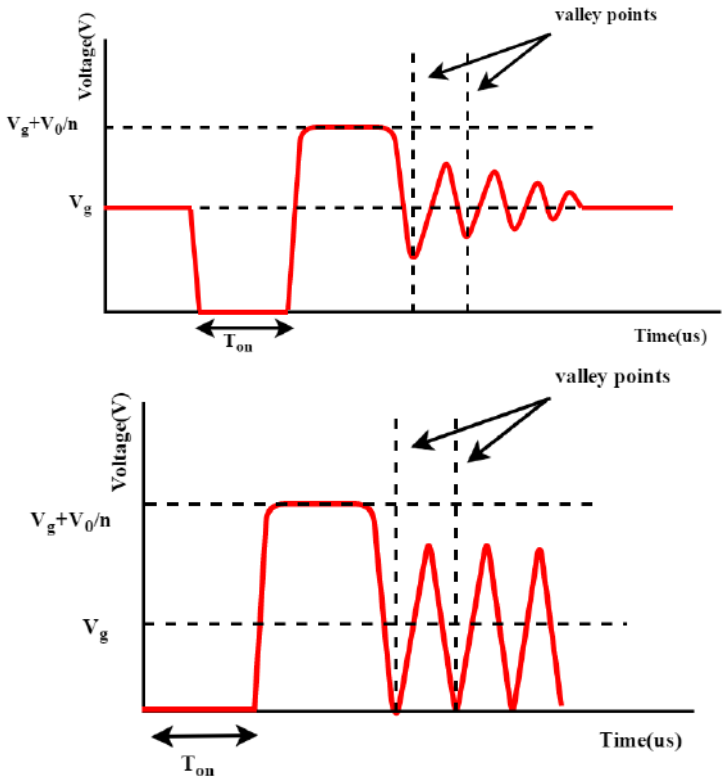

Figure 5.2: (a)Voltage across the switch in LV region.(b)Voltage across switch in HV region

In low voltage region, the voltage across switch oscillate around V_g without zero touching. In high voltage region voltage across switch come down to zero and oscillate around V_g. This control algorithm ensures minimum voltage switching in LV region and zero voltage switching in HV region.

5.2 CPLD Control Card Design

5.2.1 Advantages of CPLD over DSP

Digital signal processing (DSP) underpins modern wireless and wire line communications, medical diagnostic equipment, military systems, audio and video equipment, and countless other products, becoming increasingly common in consumers lives. Due to advances in semiconductor technology, ever more complex DSP algorithms, protocols and applications are now feasible, which, in turn, increase the complexity of the systems and products. As the complexity increases, the system reliability is no longer solely defined by the hardware platform reliability, typically quantified in mean time between failure (MTBF) calculations. System reliability is increasingly determined by hardware and software architecture, development and verification processes, and the level of design maintainability.

One fundamental architecture issue is the type of hardware platform. DSP functions are commonly implemented on two types of programmable platforms: digital signal processors and complex programmable logic devices(CPLD). Digital signal processors are a specialized form of the microprocessor, while CPLDs are a form of highly configurable hardware. In the past, the use of digital signal processors was nearly ubiquitous, but with the needs of many applications outstripping the processing capabilities of digital signal processors (measured in millions of instructions per second (MIPS), the use of CPLDs is growing rapidly. Currently, the primary reason most engineers choose use a CPLD over a digital signal processor is driven by the application's MIPS requirements. Thus, the comparison between digital signal processors and CPLDs focuses on MIPS comparison, which, while certainly important, is not the only advantage of a CPLD. Equally important, and often overlooked, is the CPLD inherent advantage in product reliability and maintainability.

A few of the more common causes of DSP software bugs are due to

1. Non-uniform assumptions regarding processor resources by multiple engineers simultaneously developing and integrating disparate functions

2. Failure of interrupts to completely restore processor state upon completion

3. Blocking of critical interrupt by another interrupt or by an uninterruptible process

4. Undetected corruption or non-initialization of pointers

5. Failing to properly initialize or disable circular buffering addressing modes

6. Memory leaks, the gradual consumption of available volatile memory due to failure of a thread to release all memory when finished

7. Dependency of DSP routines on specific memory arrangements of variables

8. Unexpected memory rearrangement by optimizing memory linkers and compilers

5.2.2 MAX V Control Card Hardware Implementation

MAX V devices contain a two-dimensional row and column based architecture to implement custom logic. Row and column interconnect provide signal interconnect between the logic array blocks (LABs). Each LAB in the logic array contains 10 logic elements (LEs). An LE is a small unit of logic that provides the efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The multi-track interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures. The I/O elements (IOEs) located after the LAB rows and columns around the periphery of the MAX V device feeds the I/O pins. Each IOE contains a bidirectional I/O buffer with several advanced features. MAX V devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device. You can also use the global clock lines for control signals such as clear, preset or output enable.

Altera MAX V CPLD with 570 logic elements and 256 pins has been chosen for the control card implementation.This MAX V series CPLD require the 3.3V power supply. To provide that power supply linear regulator(LTC3670) has been employed, this linear regulator takes 5V supply and converts into 3.3V and 1.8V supplies. It is

provided with power LED and four user LEDs, and push buttons to start or stop any process. For programming the CPLD, USB blaster is required and through USB JTAG pins programming can be done.

This control card functions with 10MHz clock signals, 10MHz oscillator provided on the back side of the control card. In 256 pins some are power pins and ground pins, mostly GPIO pins. These GPIO pins categorized as AGPIO and BGPIO pins. Here as per the requirement only a few pins are brought out The complex programmable logic

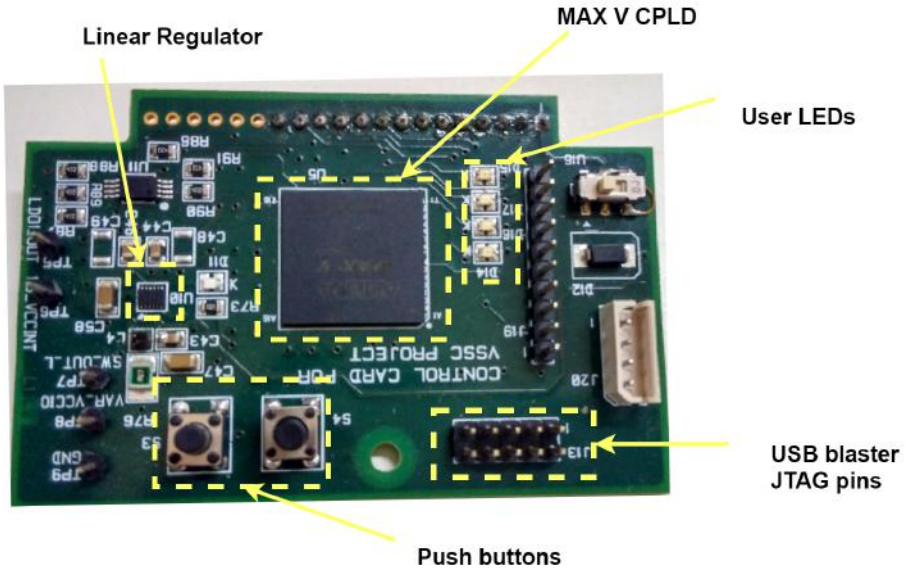

Figure 5.3: Top view of the control card

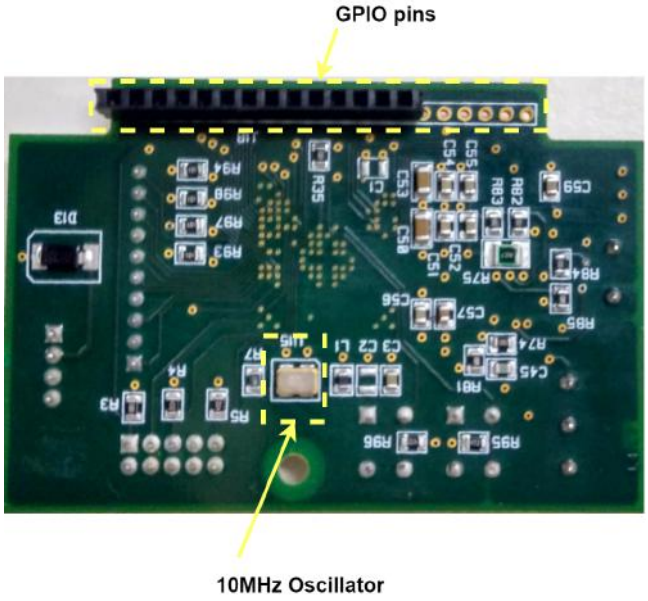

Figure 5.4: Bottom view of the control card

device can be configure using Quartus software.

CHAPTER 6

SIMULATION ANALYSIS

Simulation analysis is presented in this chapter for the both the configurations. The simulation analysis is based on some assumptions like the transformer block is considered as an ideal. The magnetizing inductance, leakage inductance, and winding resistances can be added externally by characterization of the transformer. Two transformers are modelled for two configurations. Parasitics effects of two transformers are different and causes the difference in output voltage reach for the same ON time.

6.1 Configuration 1: Simulink Analysis

Simulation analysis of configuration 1 is presented in this section. After obtaining the characterization results of the transformer from chapter 4, transformer block needs to design with an ideal block along with parameters. From the Table 6.1, the parameters can obtain for only first approach transformer and they are, Simulink diagram are shown

Table 6.1: Parameters of configuration 1 transformer

Transformer parameter	Configuration 1 transformer
R_p	0.1038Ω
L_m	$63.60\mu H$
C_w	$22.061pF$
R_s	4.7213Ω
L_{lkp}	$0.6063\mu H$

below,

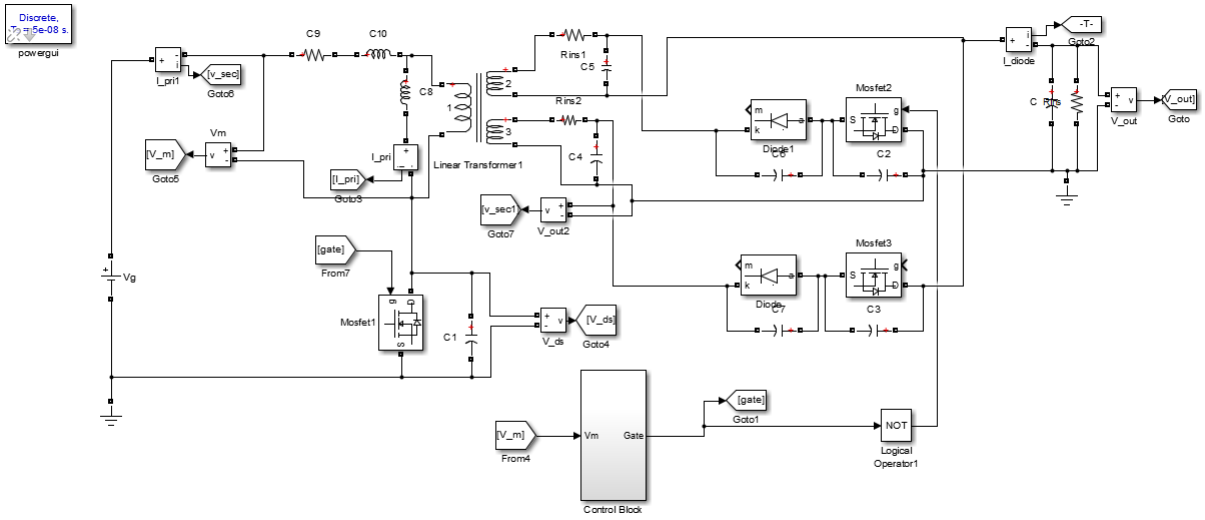

Figure 6.1: Simulink diagram for bipolar high voltage flyback converter with one primary two secondary windings

6.2 Configuration 2: Simulink Analysis

In this section, the simulink analysis of single module of configuration 2, and complete configuration 2 are presented individually. Simulation analysis of module with one primary and one secondary can be extended to modular approach (configuration 2) that means outputs of the modules can be connected in series to get bipolar voltages. Therefore the study of this gives the results for configuration 2. The parameters of a transformer with one primary and one secondary can be obtained from chapter 4 and tabulated in Table.6.2,

Table 6.2: Parameters of configuration 2 transformer

Transformer parameter	Configuration 2 transformer
R_p	0.104Ω
L_m	$63.72\mu H$
C_w	$8.6851pF$
R_s	4.6821Ω
L_{lkp}	$0.817\mu H$

Some of scope results are given below,

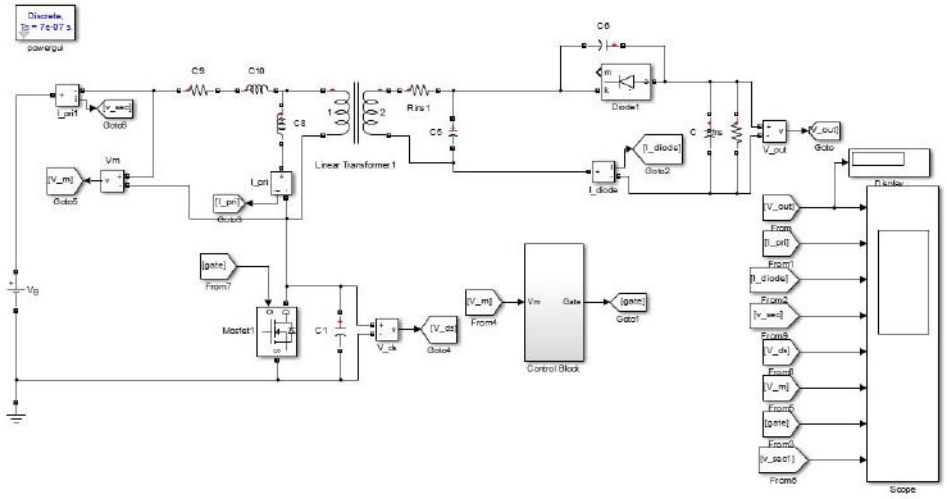

Figure 6.2: Simulink diagram for unipolar high voltage flyback converter with one primary one secondary winding

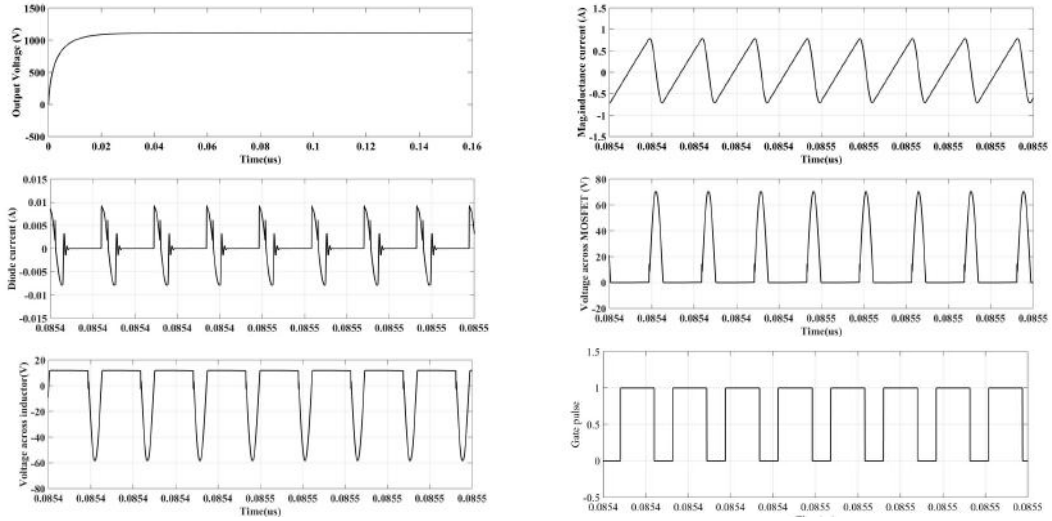

Figure 6.3: Waveforms corresponding to positive voltage

Here the results from the simulations is tabulated in Table.6.3 to study the behaviour of the different modules with different transformers. Clearly it is understood that by using transformer with one primary and two secondary windings, there is a reduction in the voltage considerably and this is because the effect of one secondary winding on the other. This is because all the windings are there under the single core. This problem is not there with the two module approach. In configuration 2 all the parasitic effects are localized with the modules.

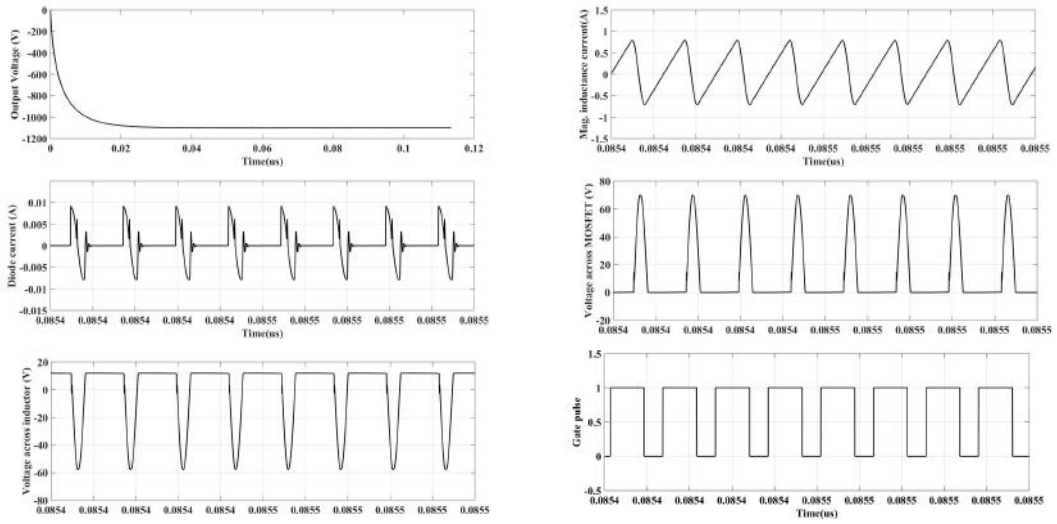

Figure 6.4: Waveforms corresponding to negative voltage

Table 6.3: Comparison of output voltages of different modules

Time (us)	Second approach voltage(V)(one module)	First approach	
		+ve voltage(V)	-ve voltage(V)
2	300	383	-383
3	505	507	-507
4	645	636	-636
5	850	761	-761
6	1213	858	-858
7	1390	984	-984
8	1565	1104	-1104
9	1730	1230	-1230

Total Simulink analysis of approach based on modular approach is presented here by connecting the two modules output in anti-series fashion. And the transformer with one primary and one secondary is used with the parameters mentioned in Table 6.2.

Table 6.4: Simulation results of modular approach

$T_{on1}(us)$	$T_{on2}(us)$	Output Voltage(V)
0	7	-1037
0	3	-470
0	0	0
5	0	760
8	0	1232

Here T_{on1},T_{on2} are ON times of module 1 and module 2 respectively. Similarly for different combination of ON times different bipolar output voltages can be achieved.

CHAPTER 7

HARDWARE IMPLEMENTATION AND RESULTS

Hardware implementation is presented for the configuration 1, that is module with one primary two secondary transformer with $V_g = 12V$, load resistance $R_{load} = 20M\Omega$ and load capacitance $C_{load} = 10nF$. It can be modified to get results for configuration 2, that is the module with one primary one secondary transformer. And two such modules outputs can be connected in series to get bipolar voltages(configuration 2).

In configuration 1 required high voltage side controllable switches. In this project, IXT02N450HV is used which is IXYS make and rated for 4500V and 200mA. Primary side MOSFET is low rating device, here FDS2672 is used, which is rated for 200V and 3.9A. Configuration 1 required the high side gate driver on secondary side because source potential is not at ground potential. For turning ON the MOSFET 15V has to apply over the source potential. For high side gate driving UCC21520, texas instruments make gate driver with the capacitor at the gate signal end is employed. High voltage side track width and spacing has to take care. For primary side MOSFET, low side gate driver is enough, EL7104 is used to drive this. Comparator TLV3507 is used to send the signals to control logic. Here the comparator output based on the switch voltage, whenever it crosses input voltage comparator output will be toggled. It will drive the gate driver circuit, this will ensure the minimum voltage turn ON. Hardware results of both the modules are identical with different values. Output voltages of two modules for same ON time have been tabulated.

In table.7.1 hardware results are tabulated. In configuration 2 study of one module is enough to give the total performance. By connecting one more module at the output in anti-series fashion bipolar voltage could be achieved. It is clear that configuration 2 can give satisfactory results than configuration 1, this is already verified using simulink.

From fig.7.4 it is clear that for same T_{on} module with three winding transformer gives less voltage, this is due to increase in parasitic capacitance. Voltage deviation

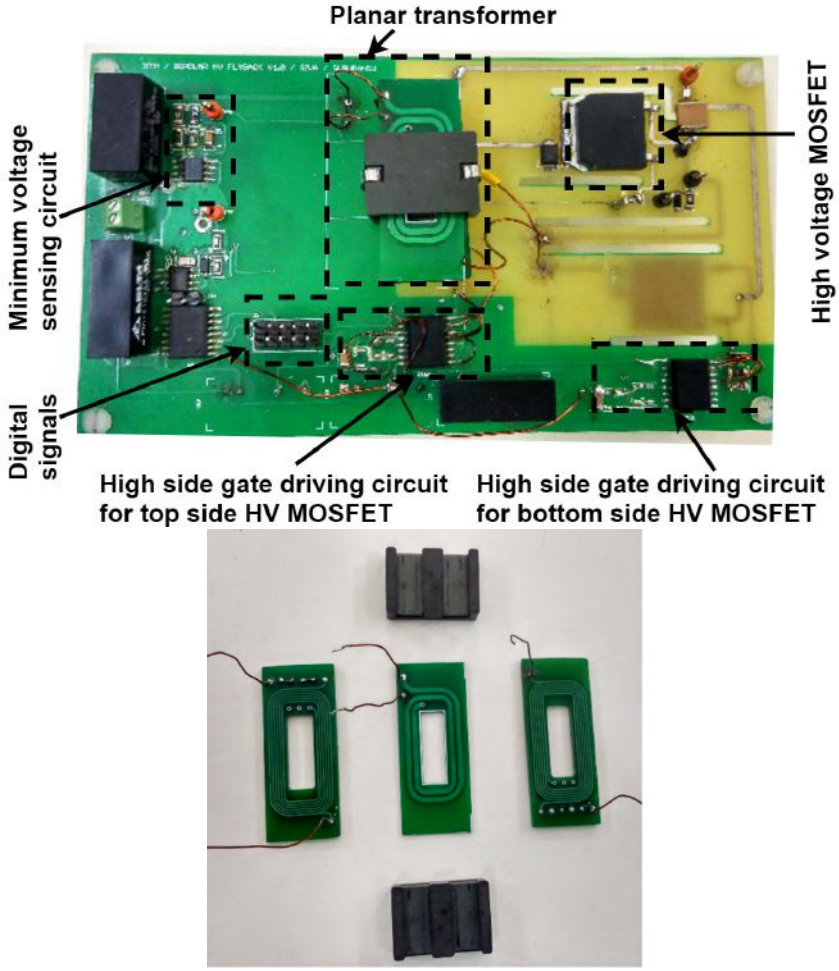

Figure 7.1: (a)Top view of High voltage low power bipolar DC-DC converter. (b)Planar transformer winding plates and core

from approach 1 to the single module of approach 2 is less in the case of low voltages and more in the case of higher voltages.

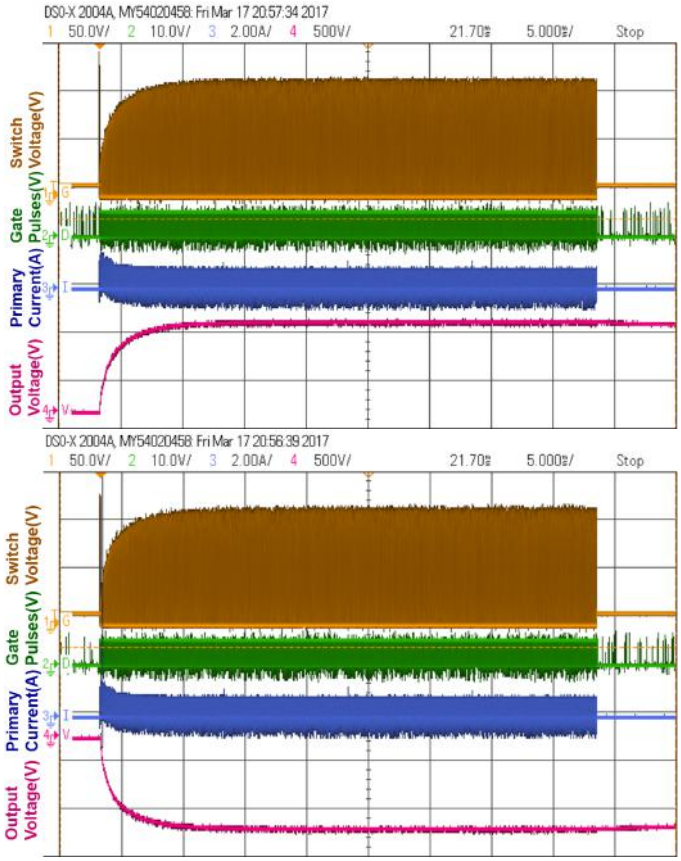

Figure 7.2: Building up of voltages (a)Positive and (b)Negative

Table 7.1: Comparison of output voltages of different modules

Time	circuit 1		Circuit 2
(us)	+ve voltage(V)	-ve voltage(V)	voltage(V)(one module)
2	420	-400	420
3	520	-500	520
4	540	-550	640
5	640	-660	780
6	740	-740	920
7	860	-840	1050
8	940	-940	1170
9	1030	-1050	1290

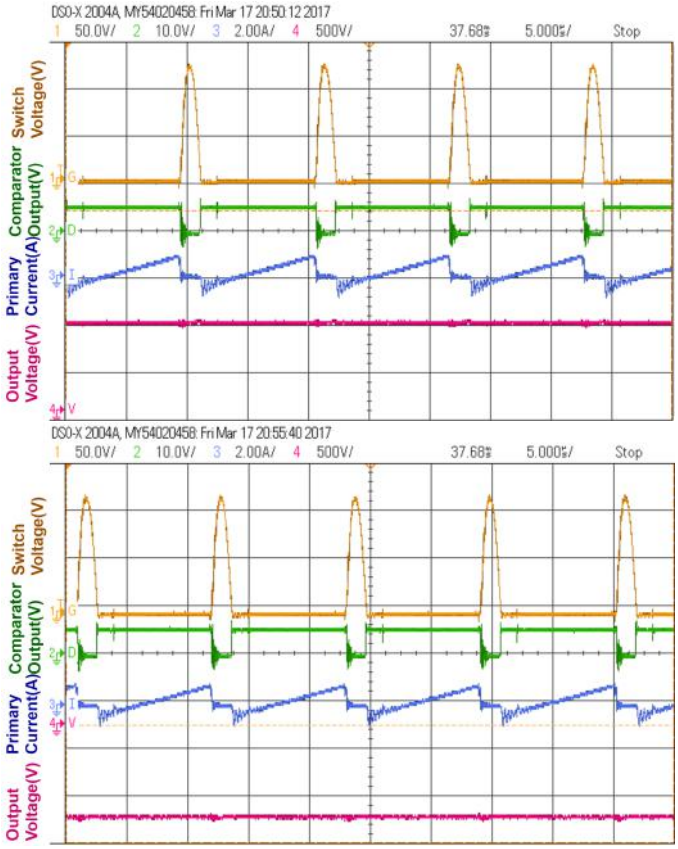

Figure 7.3: Expanded view of switching cycles of (a)Positive and (b)Negative voltages

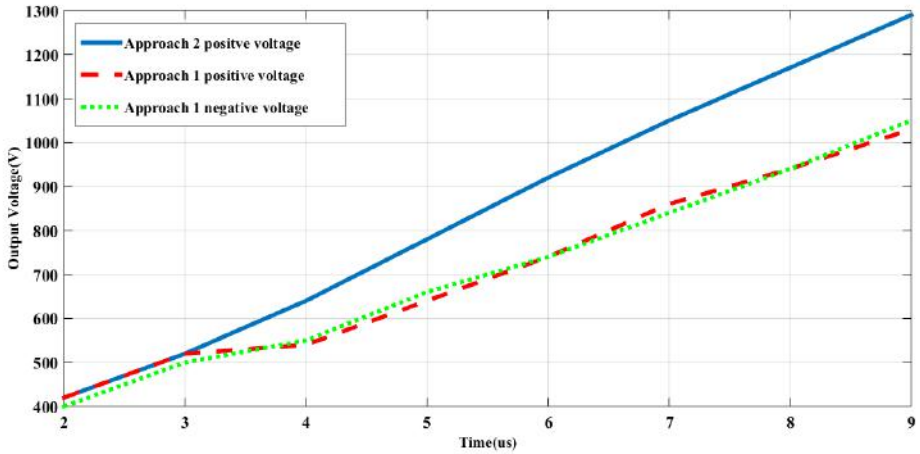

Figure 7.4: Voltage comparison of two configuration

CHAPTER 8

CONCLUSION

In this report, as explained in previous chapters, the first circuit configuration has an upper limit on the practically achievable output voltage due to the non-availability of high rated devices on the secondary side. Devices on the secondary side should be capable of withstanding atleast twice the output voltage across them. Increase in the winding parasitic capacitance will reduce the achievable output voltage significantly when compared to the module with two winding transformer which can provide unipolar voltage. In configuration 1, high side gate driver is required with suitable bootstrap capacitance. Insulation requirements on high voltage side will be critical.

On the other hand, using the second approach, higher output voltages can be easily achieved. Secondary side devices with half the rating of those in the first configuration is sufficient. The degree of controllability will be increased with primary side control for both the modules. Parasitic capacitance is also lower in this configuration.

Comparing the two circuit configurations based on the simulation and hardware results, it can be concluded that the performance of configuration 2 is better. Therefore, it is preferred to go with the modular approach for achieving bipolar high voltages.

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2. Kunchala Siva Prasad, Dr. Lakshminarasamma N, “Effect of Parasitics in High Voltage Bipolar Flyback Converter for Lightly Loaded Resistive Loads", *IEEE SPICES*,2017,(under review)