A 25-39 GHz Mixer First Receiver Employing Direct Down-Conversion of the 15th Harmonic of Clocking Frequency

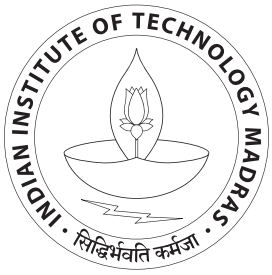
A Project Report

submitted by

VINAY CHENNA

in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY



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THESIS CERTIFICATE

This is to certify that the thesis entitled **A 25-39 GHz Mixer First Receiver Employing Direct Down-Conversion of the 15th Harmonic of Clocking Frequency**, submitted by **Vinay Chenna** (**EE15B126**), to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Technology** is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: Mixer-First Receivers, Harmonic Downconversion, mm-Wave, RF Filtering, LPTV

A 25-39 GHz mixer-first receiver is presented in this thesis. The receiver operates by direct down-conversion of the 15th harmonic of the clock frequency. This permits the use of low frequency clock phases (<3 GHz) to directly down-convert mm-Wave signals. Techniques are also proposed to improve RF filtering characteristics of the receiver. LPTV analysis is shown to support the proposed ideas. Performance of the proposed receiver is compared to other state-of-the-art mm-Wave receivers.

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ABBREVIATIONS

RF	Radio Frequency
LTI	Linear Time-Invariant
LTV	Linear Time-Varying
LPTV	Linear Periodically Time-Varying
HTF	Harmonic Transfer Function
OTA	Operational Trans-conductance Amplifier
TSPC	True Single Phase Clocked
NF	Noise Figure
DSB	Double Side Band
NPF	*N*-Path Filter

NOTATION

t	Time of Observation
τ	Impulse applied τ units before the observation time
$H_k(f)$	k^{th} Harmonic Transfer Function of an LPTV system
$\hat{x}(t)$	Signal in the adjoint network corresponding to $x(t)$ in the original network
S_i	i^{th} non-overlapping clock phase

CHAPTER 1

INTRODUCTION

Commercial 5G deployments are expected to operate across multiple bands in the 24-40 GHz range. Passive mixer-first receivers are an example of a class of re-configurable receivers whose center frequency can be tuned by controlling the frequency of the clocks that are used to drive them. Such receivers have extensively been studied and implemented over the past 10-15 years. Most of the work on these receivers, however, has only been limited to the sub-5 GHz range and the W/E bands (60-100 GHz).

The requirement to operate over a wide range of frequencies in mm-Wave bands poses several challenges in the design of compact circuitry that can function over the entire frequency range. To operate passive mixers at mm-Wave frequencies, it is necessary to generate clocks at these frequencies. Since passive mixers have the problem of harmonic folding, it is necessary to use sufficiently large number of non-overlapping clock phases to minimize this effect. This necessitates the need to generate multiple non-overlapping clock phases at mm-Wave frequencies which becomes impractical due to the power requirements and due to the finite rise and fall time ($\approx$ 10-20 ps) limitations of the technology.

The challenges associated with clock generation elicit the need to employ low-frequency clocking to down-convert the high-frequency input signals. However, such sub-sampled systems often have excessive noise folding. It is therefore, necessary to come up with schemes that would down-convert only the required harmonics without down-converting too many other harmonics.

Towards these ends, a novel technique is proposed which permits low frequency clocking of passive mixers to down-convert mm-Wave input signals, while down-converting only those harmonics which are odd multiples of 3. Further, because the RC passive-mixer provides limited far-away attenuation, a technique is proposed to improve the RF filtering characteristics of the receiver.

In summary, described in this thesis is a passive mixer-first receiver that enables direct down-conversion of the 15th harmonic of the clocking frequency with improved RF filtering. In addition, a wide-band matching network is designed to obtain input matching across 24-39 GHz frequency range.

The organization of this thesis is as follows:

- Chapter 2 reviews the properties of LTI, LTV, LPTV and sampled LPTV networks.
- Using the theory in chapter 2, the proposed circuit is derived in chapter 3 and brief analysis is shown to describe the operation of the circuit.
- Chapter 4 briefly describes the circuit blocks that were used to build the receiver.
- Chapter 5 shows the performance characteristics of the circuit and compares it to the state of the art.
- The appendix briefly describes all the other research attempts that were made during the B.Tech. project.

CHAPTER 2

Review of LTI and LPTV Theory

Passive mixers are linear periodically time varying (LPTV) systems and hence their analysis requires a proper understanding of LPTV theory. In this chapter, basics of LTI and LPTV systems will be reviewed. A brief discussion on LPTV systems with sampled outputs is also presented.

2.1 Linear Time Invariant (LTI) Systems

A system is *linear* if it follows superposition. For example, if the response of the system, with zero initial conditions, to $x_1(t)$ is $y_1(t)$ and to $x_2(t)$ is $y_2(t)$, then the response of the system to $\alpha_1 x_1(t) + \alpha_2 x_2(t)$ is $\alpha_1 y_1(t) + \alpha_2 y_2(t)$, where α_1 and α_2 are complex constants. If,

$$x_1(t) \rightarrow y_1(t)$$

$$x_2(t) \rightarrow y_2(t)$$

Then,

$$\alpha_1 x_1(t) + \alpha_2 x_2(t) \rightarrow \alpha_1 y_1(t) + \alpha_2 y_2(t) \tag{2.1}$$

A system is *time invariant* if delaying the input by a given amount also delays the output by the same amount. In other words, for a given *shape* of the input signal, the output is always of the same *shape*.

If

$$x_1(t) \rightarrow y_1(t)$$

Then,

$$x_1(t-\tau) \rightarrow y_1(t-\tau) \tag{2.2}$$

When the conditions in equations (2.1) and (2.2) are met, it can be shown that the output is related to the input by the following convolution integral.

$$y(t) = \int_0^\infty x(\tau)h(t-\tau)d\tau = \int_0^\infty h(\tau)x(t-\tau)d\tau \tag{2.3}$$

Observe that the '$h(\tau)$' term in the integral indicates the response to an impulse applied at a time '$t-\tau$', which is 'τ' units of time before the time of observation. More specifically, the response to a complex exponential $e^{j2\pi ft}$ can be shown to be,

$$y(t) = H(f) \times e^{j2\pi ft} \tag{2.4}$$

$$H(f) = \int_0^\infty h(\tau) \times e^{-j2\pi f\tau}d\tau$$

where, $H(f)$ is the Fourier transform of the impulse response of the system, $h(t)$. Note that $H(f)$ *does not* depend on either the time of application of the input or the time of observation of the output. The complex exponential is therefore, an eigen-function of an LTI system. This property of LTI systems implies that the output signal cannot contain frequency components that are not present in the input signal.

2.2 Linear Time-Varying (LTV) Systems

Unlike LTI systems, in LTV systems, the shape of the response for a given shape of the input signal is not fixed, but instead depends on the time of application of

the input, i.e, if

$$\delta(t) \rightarrow h(t)$$

Then,

$$\delta(t-\tau) \nrightarrow h(t-\tau)$$

Linearity, however, still allows the output to be expressed as the following convolution integral

$$y(t) = \int_0^\infty h(t,\tau) \times x(t-\tau) d\tau \tag{2.5}$$

The form of eqn. (2.5) is similar to that of eqn. (2.3) with the important difference being that the impulse response is dependent on even the time of observation (or equivalently, on the time of application of the input for a given 'τ').

The response to a complex exponential can shown to be,

$$y(t) = H(f,t) \times e^{j2\pi ft} \tag{2.6}$$

where,

$$H(f,t) = \int_0^\infty h(t,\tau) \times e^{-j2\pi f\tau} d\tau$$

The above expressions clearly show that the frequency response of the LTV system is time dependent.

2.3 Linear Periodically Time Varying (LPTV) systems

LPTV systems are a special case of LTV systems in which the shape of the response to an impulse varies *periodically* with the time of application of the input, i.e,

$$h(t + T_S, \tau) = h(t, \tau) \tag{2.7}$$
$$H(f, t + T_S) = H(f, t)$$

$$\text{where,} \quad T_s \rightarrow \text{Fundamental Period of the System}$$

This implies that, if,

$$x(t) \rightarrow y(t)$$

Then,

$$x(t - nT_S) \rightarrow y(t - nT_s) \quad \text{where } n \in \mathbb{Z}$$

However,

$$x(t - t_0) \nrightarrow y(t - t_0) \quad \text{if } t_0 \neq nT_s$$

2.3.1 Response to a Complex Exponential

Equation (2.7) implies $H(f, t)$ can be expanded as a fourier series with a fundamental period T_S. Thus,

$$H(f, t) = \sum_{k=-\infty}^{\infty} H_k(f) \times e^{j2\pi k f_S t} \tag{2.8}$$

Substituting the above expression in the convolution integral yields the following response to the complex exponential, $e^{j2\pi ft}$,

$$y(t) = H(f,t) \times e^{j2\pi ft} = \sum_{k=-\infty}^{\infty} H_k(f) \times e^{j2\pi(f+kf_S)t} \tag{2.9}$$

Equation (2.9) can be interpreted as follows. Any complex exponential at a frequency f, when passed through an LPTV system gets translated to around all the harmonics of the fundamental frequency of the system. The k^{th} conversion gain, viz., the gain from $f \rightarrow f + kf_S$ is denoted by $H_k(f)$ which is known as the k^{th} *Harmonic Transfer Function* (HTF) of the LPTV system.

The work presented in this thesis concentrates on utilizing $H_{-15}(f)$ of a passive RC mixer to enable low frequency clocking to down-convert signals at mm-Wave frequencies.

2.3.2 LPTV Networks with Sampled Outputs

The analysis of certain LPTV circuits and systems becomes greatly simplified when just the samples of voltages at certain nodes are known ([5], [7]). It is therefore useful to study the properties of sampled LPTV systems.

From equation (2.9), it is known that, the response to a complex exponential of an LPTV network varying with a frequency f_s is given as

$$y(t) = \sum_{k=-\infty}^{\infty} H_k(f) \times e^{j2\pi(f+kf_s)t}$$

When the output is sampled with a period $T_s = 1/f_s$, the sampled output of the

LPTV system is

$$y(nT_s) = e^{2\pi f n T_s} \times \sum_{k=-\infty}^{\infty} H_k(f) \tag{2.10}$$

Now consider an LTI system with the transfer function,

$$H_{eq}(f) = \sum_{k=-\infty}^{\infty} H_k(f)$$

Let $\hat{y(t)}$ be the output of the system when the system is excited by a complex exponential. If $\hat{y}(t)$ is sampled at a rate $T_s = 1/f_s$, we obtain,

$$\hat{y}(nT_s) = e^{2\pi f n T_s} H_{eq}(f) = e^{2\pi f n T_s} \sum_{k=-\infty}^{\infty} H_k(f) \tag{2.11}$$

From equations (2.10) and (2.11), it can be inferred that as far as the *output samples* are concerned, the LTI system with the transfer function $H_{eq}(f)$ and the LPTV system of equation (2.9) are equivalent. One method to determine $H_{eq}(f)$ (or equivalently $h_{eq}(t)$) could be to determine the HTFs of the LPTV system and then sum them up. However, this often involves very cumbersome algebra. A simpler method is to use the adjoint (or interreciprocal) network as proposed in [7].

2.3.3 Determining $h_{eq}(t)$

Consider a 2-Port LPTV network excited by a voltage input $v_i(t)$ as shown in figure 2.1[1](a) and suppose we are interested in the samples of $v_2(t)$ taken at the instants $lT_s + t_o$. There exists an equivalent LTI system $h_{eq}(t)$, which when excited by $v_i(t)$ produces an output whose samples are same as $v_2(lT_s + t_o)$. $h_{eq}(t)$ can be determined using the adjoint network as shown in 2.1(b). To determine the LTI system corresponding to the *voltage* samples of the LPTV filter's output at $lT_s + t_o$,

[1]Redrawn referring [5]

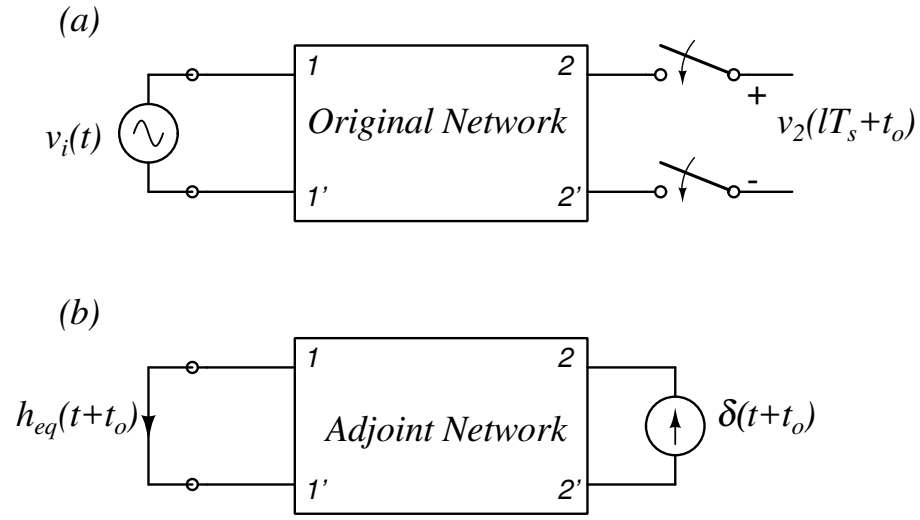

Figure 2.1: (a) An LPTV network varying at f_s , whose output $v_2(t)$ is periodically sampled at f_s. (b) Determining the impulse response $h_{eq}(t)$ of the equivalent LTI systen using the adjoint network.

the output port of the adjoint network has to be excited by a *current* impulse at $-t_o$.

To determine the adjoint network, one needs to follow the element-by-element substitutions as mentioned in [7]. The results are summarized as follows:

1. A branch that contains linear elements (viz., R, L or C) in the original network remains unchanged in the adjoint network.
2. A periodically operated switch in the original network controlled by a waveform $S(t)$ is replaced in the adjoint by a switch controlled by the waveform $S(-t)$.

CHAPTER 3

Architectural Evolution of the 15th Harmonic Direct Down-conversion Receiver

The evolution of the topology of the proposed receiver will be explained in this chapter. The analysis of an RC mixer with first order kernel will be shown using the technique presented in [5]. After that, using LPTV theory, the operating principle of the proposed receiver will be explained.

3.1 The Passive RC Mixer

Figure 3.1 shows the passive RC mixer with a first order low-pass kernel. As shown in the figure, the switch is controlled using a pulsed waveform of on-time 'τ' with a period T_S.

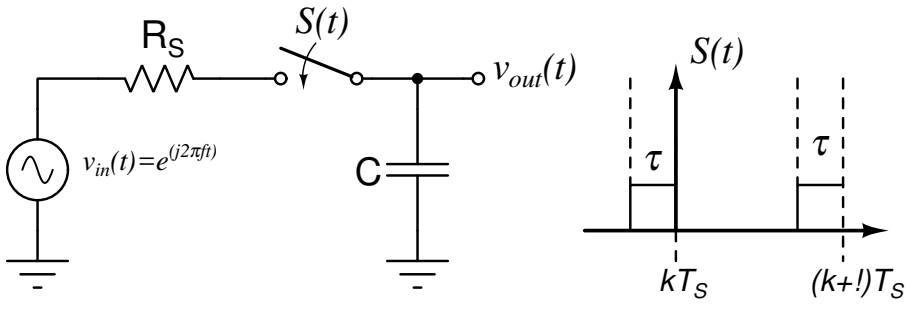

Figure 3.1: Passive RC Mixer with First Order Kernel

From equation (2.9), it is clear that, for a complex exponential input, $e^{j2\pi ft}$, $v_{out}(t)$ takes the form,

$$v_{out}(t) = \sum_{k=-\infty}^{\infty} H_k(f) \times e^{j2\pi(f+kf_S)t} \tag{3.1}$$

To determine the output waveform, it is sufficient if the HTFs, $H_k(f)$, are known. Since down-conversion properties of the mixer are of interest in this thesis, all HTFs with negative k values are to be determined.

These HTFs can be found using the discussion on sampled LPTV Networks in sections 2.3.2 and 2.3.3. The analysis procedure is briefly described as followed:

1. The sequence $V_{out}[k]$ is first found using the adjoint network.
2. The voltage $V_{out}(kT_S)$ is perfectly held by the capacitor until the switch at the source side is closed.
3. When the switch at the source side closes, the output voltage consists of two parts:
   - An exponential decay due to the stored capacitor voltage at $t = kT_S - \tau$.
   - Response due to the windowed version of the input signal (the windowing function being $S(t)$).

   Note: While performing this calculation, care should be taken to ensure that the contribution due to the windowed version of the input signal is 0 for $kT_s < t < (k+1)T_S - \tau$.

Intuitively, we expect the circuit to operate in the mixer or tracker modes based on the relationship between the clocking frequency and the RC time constant of the kernel. For example, the circuit behaves in the

- Mixer mode if $R_S C >> T_S$.
- Track and Hold mode if $R_S C << T_S$.

Furthermore, in the mixer mode, the circuit can be thought of as a high-Q second order band-pass filter cascaded by an ideal multiplier as shown

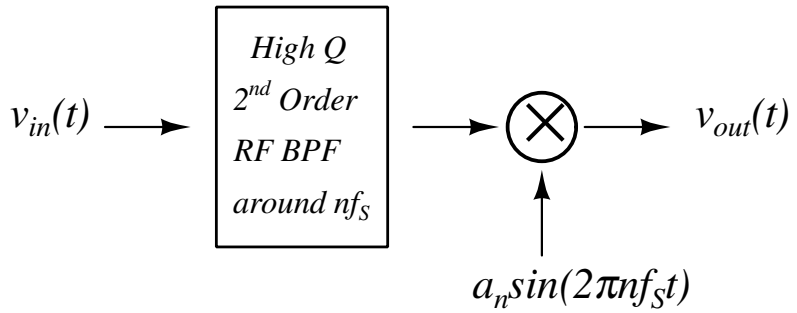

Figure 3.2: $H_{-n}(f)$ of an RC Mixer as a Second Order Band-Pass filter in Cascade with an Ideal Multiplier

3.1.1 Determining $h_{eq}(t)$

We begin the analysis by finding the waveform $h_{eq}(t)$ (assuming $R_{SW} = 0$ since its effect can easily be incorporated in the final expression by performing suitable transformations). This can be found using the adjoint network shown in figure 3.3(a).

As explained in section 2.3.3, the adjoint network can be obtained by replacing the switching waveforms by their time-reversed versions. Using the results shown in figure 2.1, $h_{eq}(t)$ can be found by measuring the current i_{out} in figure 3.3(a) when the adjoint network is excited by an impulse as shown in the figure. When the impulse is applied to the circuit, all the impulse current flows into the capacitor and charges it to a value $v_i = 1/C$, where the '1' is actually '1 Coulomb' of charge. This voltage v_i, then discharges through the source resistance with a time constant $R_S C$ for a duration of τ. At this point, the voltage on the capacitor has dropped to βv_i, where $\beta = e^{-\tau/R_S C}$. During this duration, the current i_{out} starts with an initial value of $i_o = 1/R_S C$ and decays exponentially to a value βi_{out}, at which point, it drops to zero after the switch at the source side opens.

In essence, the capacitor voltage at the end of a given period is β = times lesser than the capacitor voltage at the beginning of that particular period. If i_{out} in the first period is given by the waveform $q(t)$ (figure 3.3(b)), which a result of the capacitor

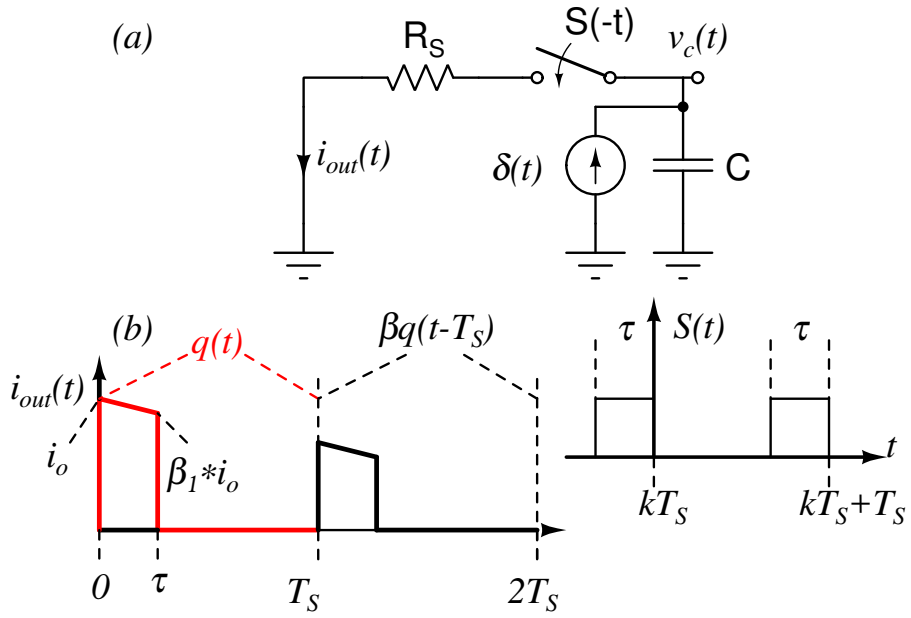

Figure 3.3: (a) Kernel of the RC Mixer's adjoint (b) Waveform of $h_{eq}(t)$

initially being charged to a voltage of $1/C$ Volts, the following relation holds true,

$$i_{out} = q(t) + \beta q(t - T_S) + \beta^2 q(t - 2T_s) + ... \tag{3.2}$$

Noting that $h_{eq} = i_{out}$, eqn. 3.2 can be re-written as the following recursive relation,

$$h_{eq}(t) = q(t) + \beta h_{eq}(t - Ts) \tag{3.3}$$

Taking the fourier transform, we obtain,

$$H_{eq}(f) = \frac{Q(f)}{1 - \beta e^{-j2\pi f T_s}} \tag{3.4}$$

It can be seen from figure 3.3(b) that,

$$q(t) = \frac{1}{R_S C} \times e^{-t/R_S C} \times (u(t) - u(t - \tau)) \tag{3.5}$$

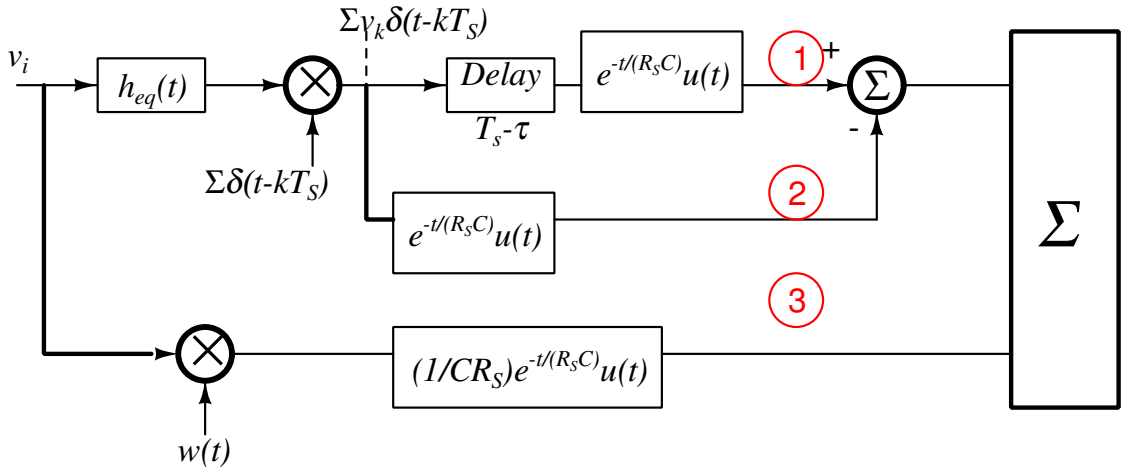

Figure 3.4: Signal Flow Graph of the Passive RC Mixer

This gives us,

$$Q(f) = \frac{1 - \beta e^{-j2\pi f\tau}}{1 + j2\pi R_S C} \tag{3.6}$$

From equations (3.4) and (3.6), we obtain,

$$\boxed{H_{eq}(f) = \frac{1}{(1 + j2\pi f R_S C)} \frac{1 - \beta e^{-j2\pi f\tau}}{1 - \beta e^{-j2\pi f T_S}}} \tag{3.7}$$

where,

$$\beta = e^{-\tau/R_S C}$$

3.1.2 Determining the Complete Response

The signal flow graph is shown in 3.4. As mentioned in section 3.1, the output waveform consists of 2 parts, due to the voltage stored on the capacitor just before the switch closes and due to the applied input signal. The former is simply an exponential decay which is shown by the branch labelled (1) in figure 3.4. The latter part can be found by windowing the input with a function $w(t)(= S(t)$ in this case) and feeding it to a system having the impulse response $h(t) = \frac{1}{R_S C} e^{-t/R_S C} u(t)$.

This is represented by branch (3) in figure 3.4.

As noted in section 3.1, the contribution due to the input signal, needs to be zero when $S(t) = 0$. From the adjoint network, we know the value of the capacitor voltage at $t = kT_s$ is, say, v_k. Therefore, the net contribution due to the branches (1) and (3) at $t = kT_s$ is v_k. If the switch continued to remain ON, the capacitor voltage would decay exponentially with a time constant of $R_S C$. Therefore, we need to subtract this amount from (1) and (3) to obtain the contribution due to the input signal. This is modelled by branch (2) in figure 3.4.

To include the effect of the switch resistance, R_{sw}, one needs to perform the following transformation: $R_S \rightarrow R_S + R_{sw}$.

Consider an input, $v_i(t) = e^{j2\pi ft}$. Since the waveform $w(t)$ is periodic, it can be expanded as a Fourier series as follows,

$$w(t) = \sum_{k=-\infty}^{\infty} a_k \times e^{j2\pi k f_S t} \tag{3.8}$$

From the signal flow graph, the output, viz., the capacitor voltage can therefore be written as,

$$\begin{aligned} v_c(t) = -\left[\left(H_{eq}(f) \times e^{j2\pi ft}\right) \times \left(\sum_{k=-\infty}^{\infty} \frac{e^{j2\pi k f_S t}}{T_S}\right)\right] * \mathcal{F}^{-1}\left[\frac{R_S C(1 - e^{j2\pi f(T_s - \tau)})}{1 + j2\pi f R_S C}\right] \\ + \\ \left[\left(e^{j2\pi ft}\right) \times \left(\sum_{k=-\infty}^{\infty} a_k \times e^{j2\pi k f_S t}\right)\right] * \mathcal{F}^{-1}\left[\frac{1}{1 + j2\pi f R_S C}\right] \end{aligned} \tag{3.9}$$

Simplifying the above expression, we obtain

$$v_c(t) = \sum_{k=-\infty}^{\infty} \underbrace{\left(\frac{-H_{eq}(f) \times R_S C(1 - e^{j2\pi(f+kf_S)(T_s-\tau)}) + T_S a_k}{T_S \times (1 + j2\pi(f + kf_S)R_S C)} \right)}_{H_k(f)} \times e^{j2\pi(f+kf_s)t} \tag{3.10}$$

We thus have, the harmonic transfer functions of the passive RC Mixer as, $H_k(f)$ as,

$$\boxed{H_k(f) = \frac{T_S a_k - R_S C \times H_{eq}(f)(1 - e^{j2\pi(f+kf_S)(T_s-\tau)})}{T_S\,(1 + j2\pi(f + kf_S)R_S C)}} \tag{3.11}$$

3.2 15th Harmonic Direct Down-Conversion Mixer-First Receiver

Consider two passive RC mixers driven using phase-shifted clocks as shown in figure 3.5. Since the clock driving the second mixer is delayed by t_d with respect

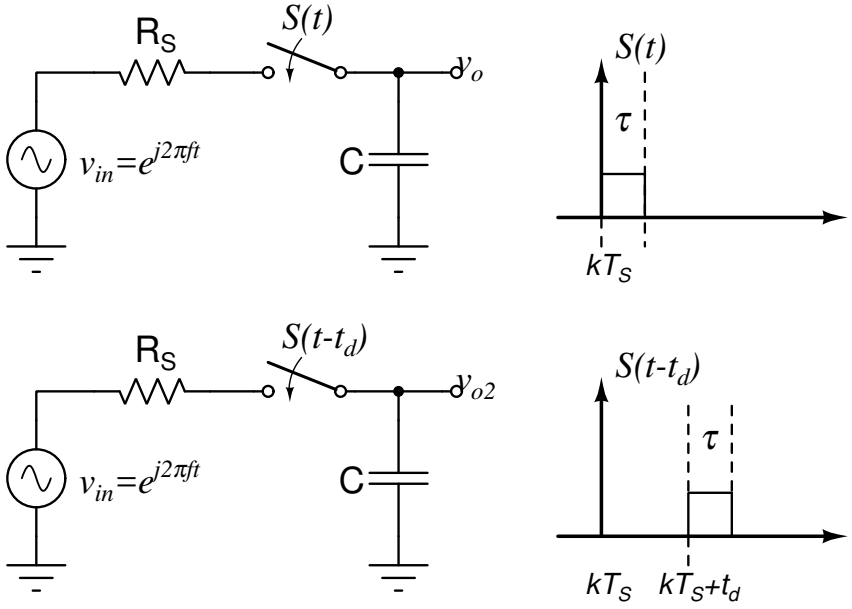

Figure 3.5: RC Mixers driven using Phase-Shifted Clocks

to the first mixer, the following relation holds true in relation to equation (2.8).

$$v_{in}(t - t_d) * h_2(t, \tau) = v_{in}(t - t_d) * h(t - t_d, \tau)$$

Thus,

$$h_{2,k}(\tau) = h_k(\tau) \times e^{-j2\pi k f_S t_d}$$

Therefore, if,

$$v_o(t) = \sum_{k=-\infty}^{\infty} H_k(f) \times e^{j2\pi(f+kf_S)t}$$

Then,

$$v_{o,2}(t) = \sum_{k=-\infty}^{\infty} \underbrace{\left(H_k(f) \times e^{-j2\pi k \frac{t_d}{T_S}}\right)}_{H_{k,2}(f)} e^{j2\pi(f+kf_S)t} \tag{3.12}$$

Thus,

$$\boxed{H_{k,2}(f) = H_k(f) \times e^{-j2\pi k \frac{t_d}{T_S}}} \tag{3.13}$$

Now consider N Mixers driven using N non-overlapping clock phases as shown in figure 3.6. In figure 3.6,

$$S_1(t) = \begin{cases} 1, & kT_S < t < kT_S + \frac{T_S}{N} \\ 0, & Otherwise \end{cases}$$

and

$$S_n(t) = S_1\left(t - \frac{(n-1)T_S}{N}\right);\ n = 1, 2, .., N \tag{3.14}$$

Using equations (3.14) and (3.12), we have,

$$\boxed{v_{o,n}(t) = \sum_{k=-\infty}^{\infty} \left(H_k(f) \times e^{-j\frac{2\pi(n-1)k}{N}}\right) e^{j2\pi(f+kf_S)t};\ n = 1, 2, .., N} \tag{3.15}$$

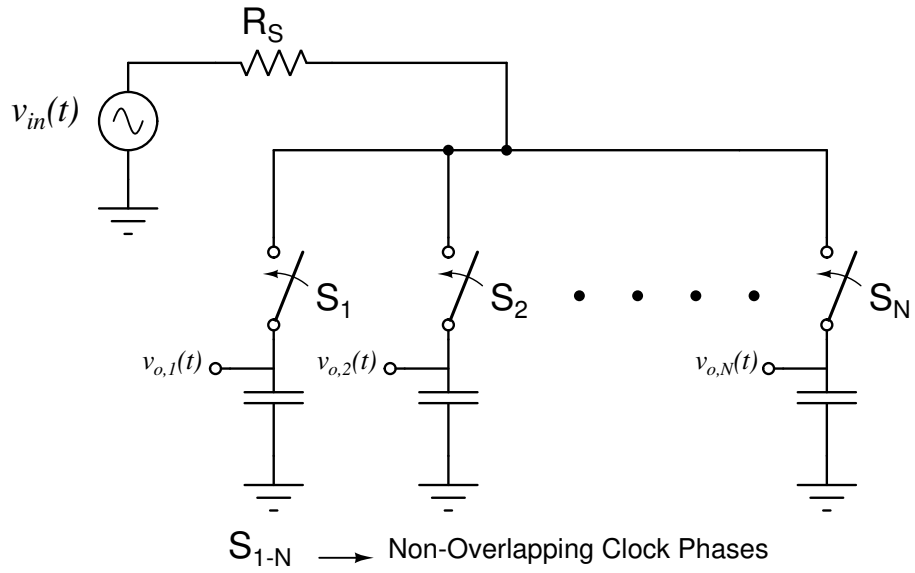

Figure 3.6: N Mixers driven using N Non-Overlapping Clock Phases

Taking a case of $N = 6$ in equation (3.15) and performing the operation,

$$v_{o,1} + v_{o,3} + v_{o,5} - v_{o,2} - v_{o,4} - v_{o,6}$$

it is easy to verify that the above summation yields the following value,

$$6 \times \left(H_{-3}(f) e^{j2\pi(f-3f_S)t} + H_{-9}(f) e^{j2\pi(f-9f_S)t} + H_{-15}(f) e^{j2\pi(f-15f_S)t} + .. \right)$$

In summary,

$$v_{o,1} + v_{o,3} + v_{o,5} - v_{o,2} - v_{o,4} - v_{o,6} = \sum_{k=-\infty}^{\infty} 6H_{6k+3}(f) e^{j2\pi\left(f+(6k+3)f_S\right)t} \tag{3.16}$$

The following observations can be made from equation (3.16)

- The only non-zero HTFs are those which are odd multiples of 3, eg., ...,-15,-9,-3,3,9,15...
- The gain of all the non-zero HTFs is 6 times higher than that in the passive RC mixer.

The above observations imply the following,

- Firstly, since most of the harmonics have been cancelled, to down-convert a high frequency signal, low frequency clocks can be used without worrying about too many signals (and too much noise) from other harmonics folding onto the desired down-converted signal.
- Since the gain of the HTFs is enhanced by 6 (= 15.5 dB), higher harmonics can be used for down-conversion with a sufficient gain.

3.2.1 Circuit Realization

To realize the summation of equation (3.16), the circuit in figure 3.7 can be used. The operation of the circuit is as follows. There are 6 passive mixers driven using

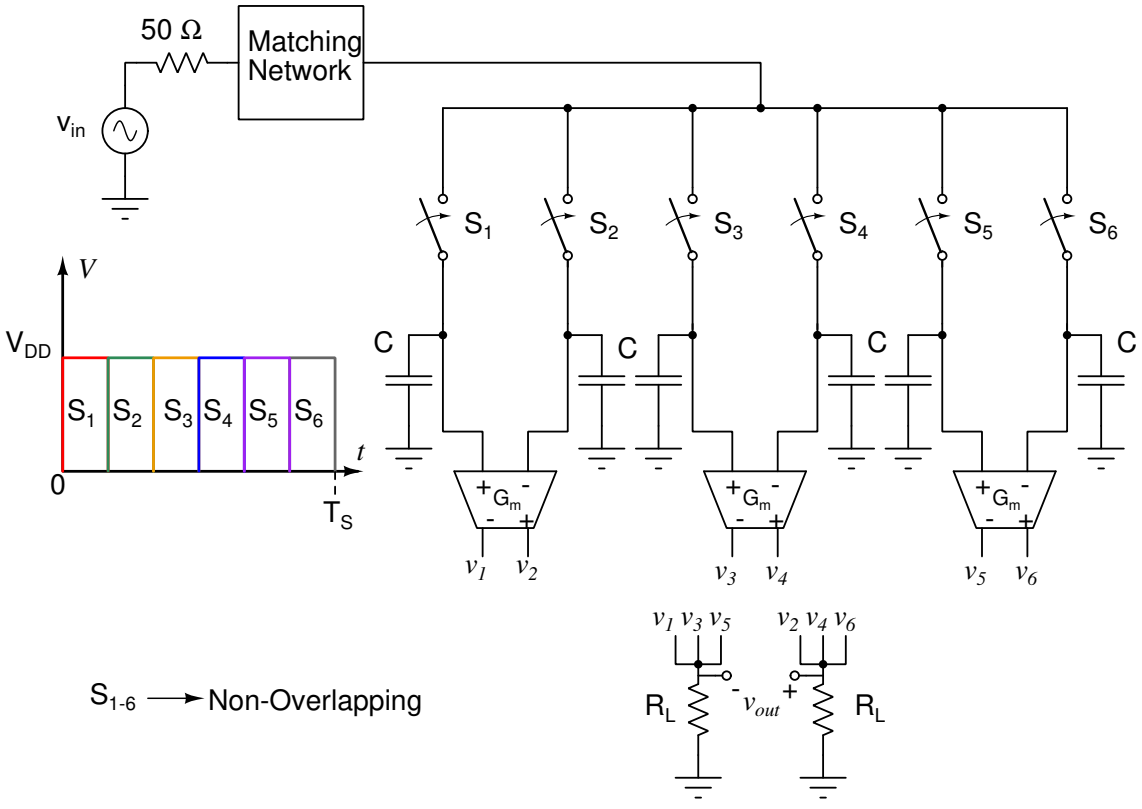

Figure 3.7: Circuit realization of the summation of equation (3.16)

non-overlapping clock phases. To perform the summation of equation (3.16), the voltages of the capacitors are fed to the inputs of base-band operational trans-

conductance amplifiers (OTAs). All the voltages on the capacitors in the ”odd-numbered” paths are given as inputs to the positive terminals of the OTAs and those of ”even-numbered” paths are given as inputs to the negative terminals of the OTAs. The summation is therefore realized by summing up the base-band currents.

3.2.2 Increasing the Far-Away Attenuation

The HTFs of passive mixers provide limited far-away attenuation because of switch and clock non-idealities. To mitigate this effect, a capacitor is placed across the inputs of the OTAs as shown in figure 3.8.

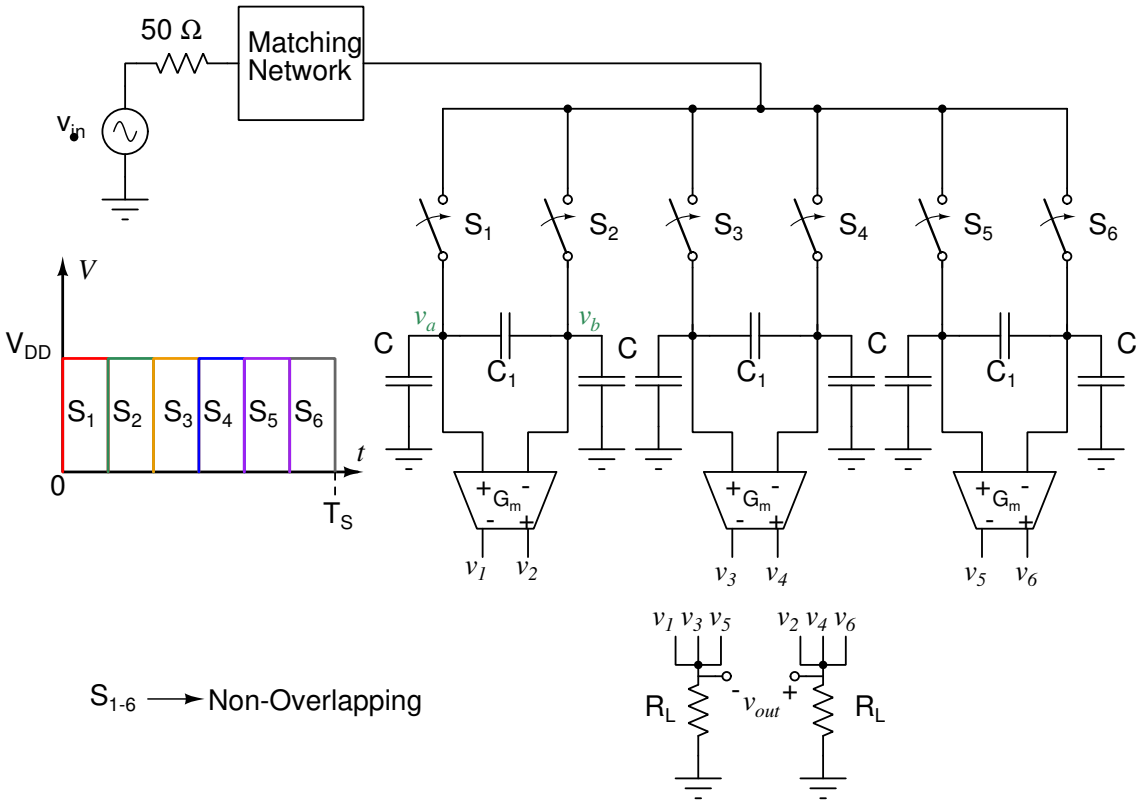

Figure 3.8: Receiver with increased far-away attenuation

To intuitively understand why this proposed technique works, it is useful to examine the behavior across nodes *a* and *b* in the figure.

Figure 3.9 shows the close-up view when switch S_1 is on and switch S_2 is off.

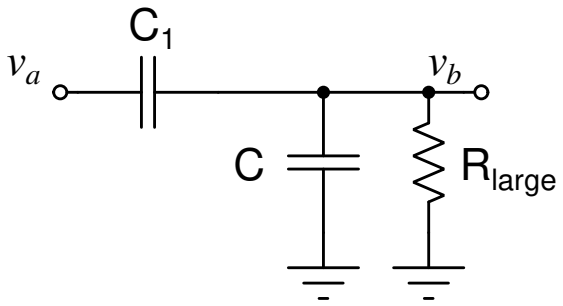

Figure 3.9: Intuituve explanation of the increased far-away attenuation

A large resistor R_{large} can be thought of hanging off node b to ground which is due to the large switch resistance, finite Q of C and the input resistance of the OTA. The transfer from a to b is given by,

$$\frac{v_b}{v_a} = \frac{sR_{large}C_1}{1 + sR_{large}(C_1 + C)} \tag{3.17}$$

Equation (3.17) indicates that the response from a to b is a high pass. This implies that all the high frequency at a appears at b when $C_1 >> C$. This means that any high frequency content that appears at a, appears as a common-mode input to the OTA and therefore gets rejected.

The capacitors in figure 3.8 form a Π-Network at the inputs of the OTA. It was

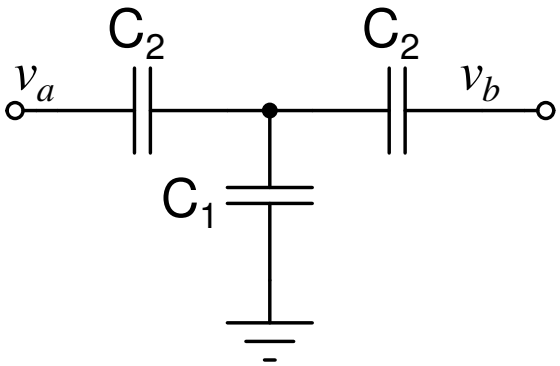

Figure 3.10: A T-network of capacitors at the input of the OTAs

noticed via simulations that a T-Network results in better noise, linearity and base-band bandwidth numbers while maintaining similar far-away attenuation. The analysis is beyond the scope of this work since the kernels have multiple capacitors which share charge with each other. The resulting capacitor network across the inputs of the OTA is shown in figure 3.10.

The resulting schematic of the receiver is shown in figure 3.11

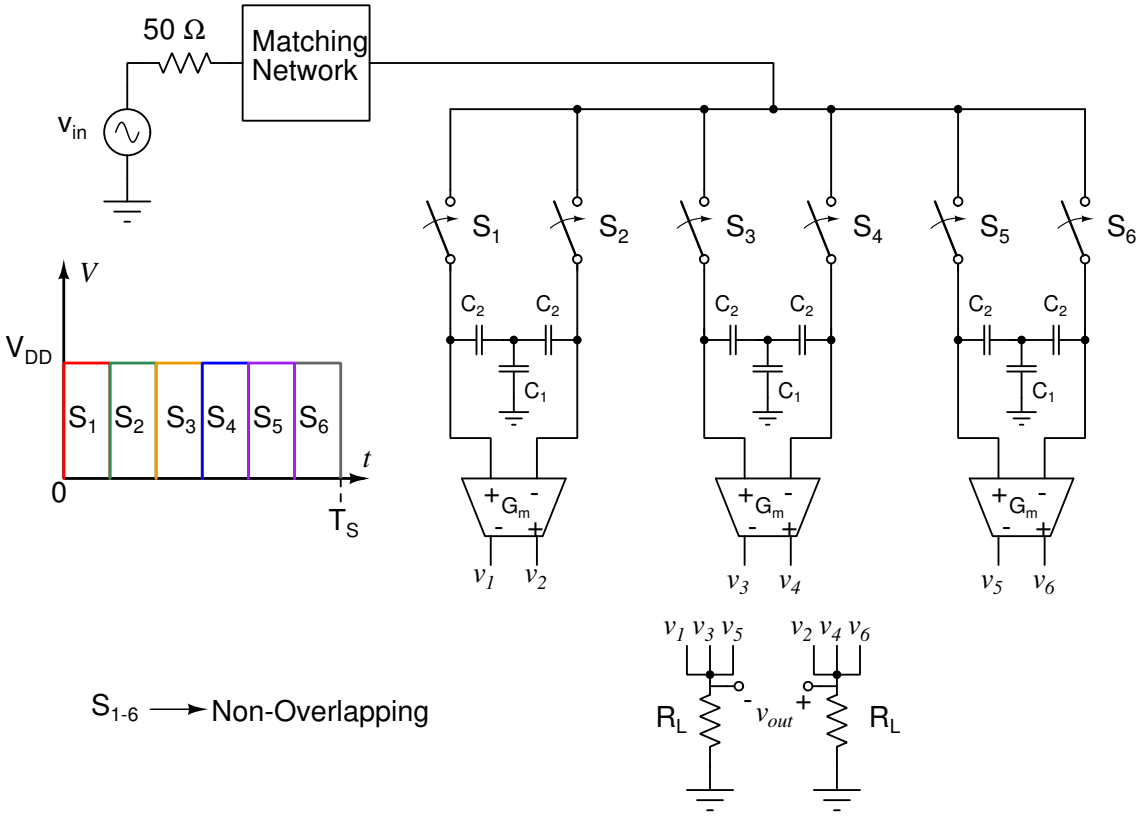

Figure 3.11: Complete Receiver Architecture with a T-Network of capacitors at the input of the OTAs.

CHAPTER 4

Design of Circuit Blocks

The circuit shown in figure 3.11 has the following blocks: clock generation block, OTAs, input matching networks and switches. Design of these blocks is briefly discussed in this chapter.

4.1 Clock Generation Circuitry

The entire clock generation circuitry, along with the power consumption of each sub-circuit at the maximum frequency of operation is shown in figure 4.1.

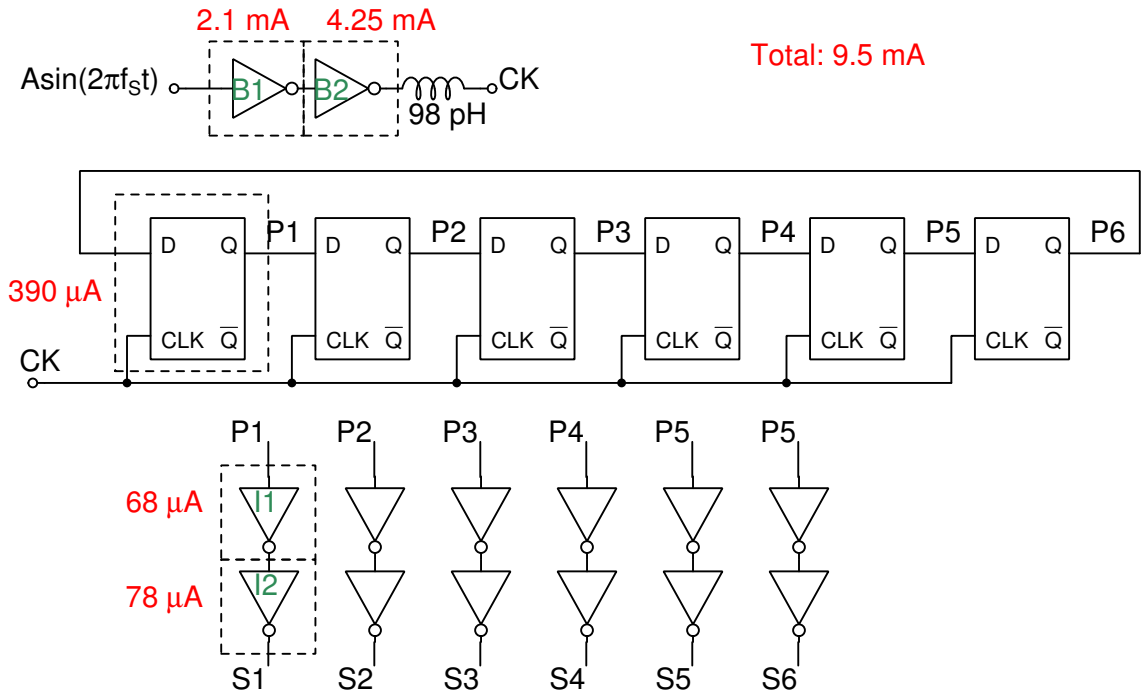

Figure 4.1: Clock Generation Circuitry

The operation of the circuit is as follows. A high frequency sinusoid (10-15.6 GHz) is given as an input to the circuit via the inverter buffer 'B1'. Inverters 'B1' and 'B2' are used to convert the sinusoid into a square. This square is applied as the clock to a ring counter which divides the frequency by 6 and produces 6 non-overlapping clock phases[1]. The inductor placed after B2 is used for extending the bandwidth of the inverter[10] which helps reduce the rise and fall times of the clock phases. This is useful because it helps reduce the switch noise thereby improving the noise figure of the circuit slightly. The non-overlapping clock phases generated by the ring-counter are buffered through inverters which drive the switches.

4.1.1 Flip-Flop Design

TSPC (True Single Phase Clocked) flip-flops were used to realize the flip-flops in figure 4.1 because of their ability to operate at high frequencies with a low power consumption[8]. The topology is shown in figure 4.2.

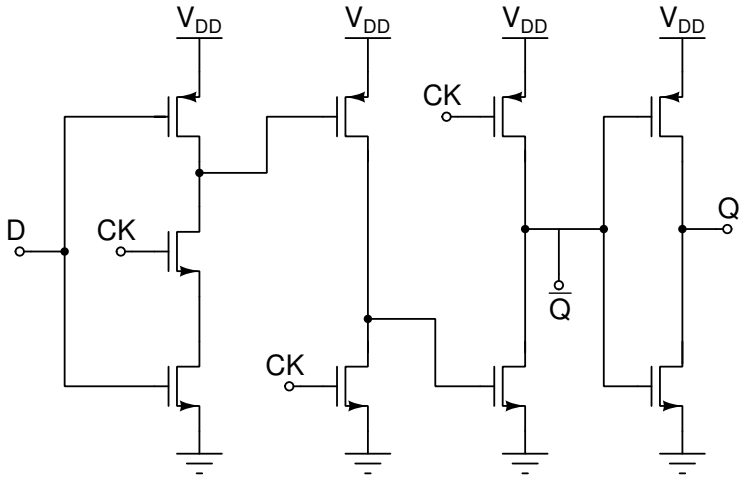

Figure 4.2: TSPC Flip Flop

All the transistors were chosen to be of same size except for the NMOS transistor

[1]The circuit therefore operates at a frequency of (10/6)*15 GHz to (15.5/6)*15 GHz = 25 GHz to 39 GHz

of the second stage, which is thrice as large as the other transistors. This sizing scheme is necessary for operation at high frequencies[8].

4.1.2 Performance Summary

Table 4.1 shows the performance summary of the non-overlapping clock generation circuitry.

Table 4.1: Performance Summary of the Clock Generation Summary

Number of Clock Phases	6
Frequency of Input Sinusoid (GHz)	10-15.6
Frequency of Non-Overlapping Clocks (GHz)	1.6-2.6
Current Consumption (mA)	7.5-9.9
Supply Voltage (V)	1.2

4.2 Wide-Band Input Matching Network

The input signals lie in the range of 25-39 GHz. It is therefore necessary to have a matching network that helps match the input over the entire frequency range. Matching over the entire range can be done either by using a tunable narrow-band matching network having switch-capacitor banks or by using a single wide-band matching network. It turned out that using a capacitor bank at these frequencies was not very feasible because the parasitic capacitance offered by the switches exceeded the required capacitance values. Therefore, a wide-band matching network as shown in figure 4.3 was used.

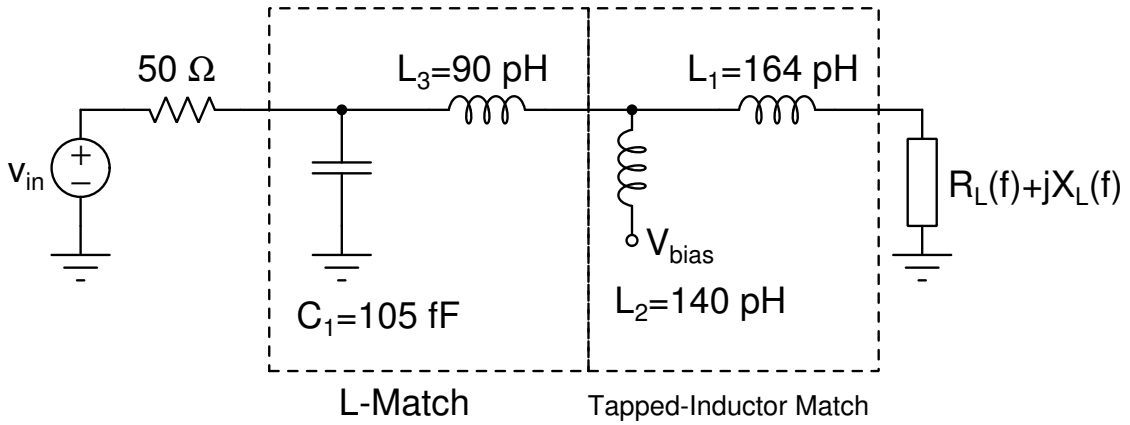

Figure 4.3: Two-Stage Wide-Band Matching Network

4.2.1 Design Procedure

The matching network consists of two-stages. The first stage is a tapped-inductor match and the second stage is an L-match. These choices were made based on the fact that the load looks like a resistor in series with a capacitor. The design procedure is as follows:

- Q of the tapped-inductor match is chosen as

$$Q_{TI} = \sqrt{\frac{R_i}{\overline{R_L}}}$$

  Here, $\overline{R_L}$ is the average value of the real part of the input impedance.

- Q of the lowpass L-match is chosen as

$$Q_L = \sqrt{\frac{R_S}{R_i}}$$

- The intermediate resistance, R_i, is chosen as

$$R_i = \sqrt{R_S \times \overline{R_L}}$$

- A part of the inductance (L_1) is also used for (partially) cancelling the load capacitance.

- Since the capacitors and the inductors as well as the input impedance of the circuit are frequency dependant, iteration is required to determine the optimum component sizes.

4.2.2 Performance Summary

Figure 4.4 shows the S_{11} as a function of the input frequency.

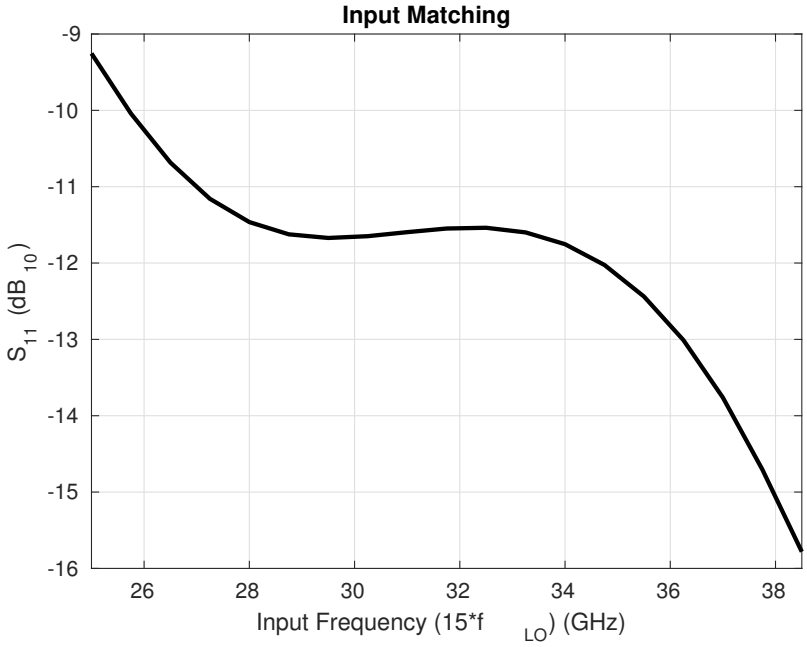

Figure 4.4: S_{11} VS Input Frequency

As seen in the figure, S_{11} <-10 dB is obtained over the entire frequency range.

4.3 Switches

As seen in figure 3.11, 6 switches are required in the signal path. The switches were realized using NMOS transistors. In the simulations, *nmos_rf* with deep n wells were used as switches. This choice was motivated by the fact that the DC bias of the drain/source of the switch is expected to be close to zero due to the inductor L_2 in the matching network. Further, deep-n-well was used to remove the effect of body-effect so that lower switch-on resistance could be achieved. The switch size was chosen to be $18 \times (600/60)$ μm, where '18' is the total number of fingers used.

4.4 Base-band OTAs

3 OTAs are required to perform the summation of (3.16). The schematic of the OTA is shown in figure 4.5. As seen in the figure, the load consists of a resistor in

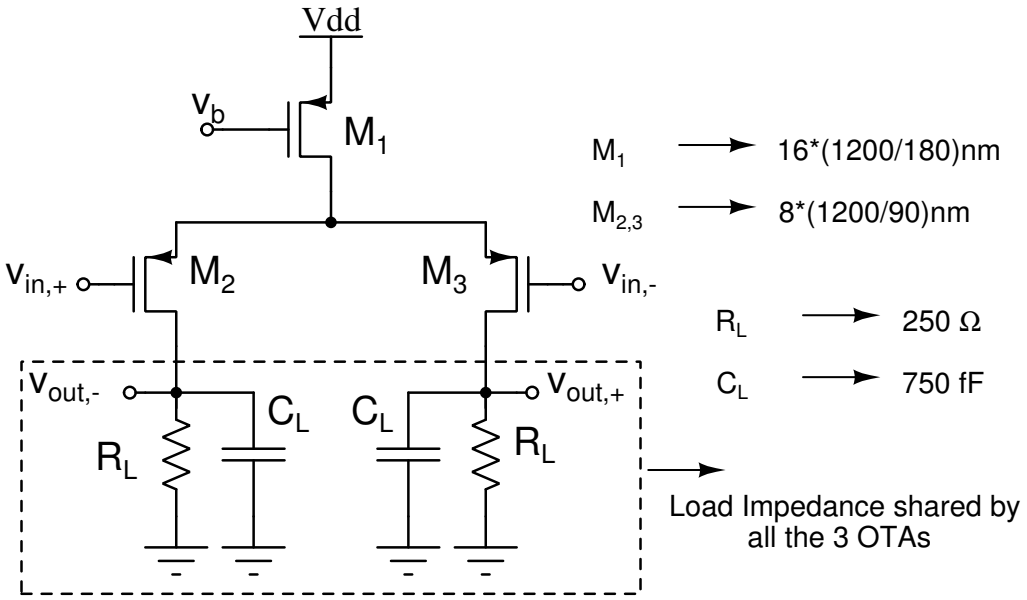

Figure 4.5: OTA Schematic

parallel with a capacitor. The capacitor is placed to suppress the high frequency ripple at the output due to clock feed-through via the switches.

Thin-oxide FETs were chosen to build the OTA despite their lower intrinsic gains and lower swing handling capabilities than thick-oxide FETs. This is because, a base-band bandwidth of few 100s of MHz is desired for the circuit and this is not easily achievable through thick-oxide OTAs without a high power budget.

Table 4.2: Performance Summary of the OTAs

Gain of the 3 OTAs combined (dB)	6
3dB Bandwidth (GHz)	1.2
Current Consumption of the 3 OTAs Combined (mA)	2.25
Current of the Biasing Circuitry (μA)	200
Supply Voltage (V)	1.2

CHAPTER 5

Performance and Simulation Results

Simulation results are presented in this chapter. Summary of the performance is presented at the end of the chapter and is compared with other state of the art mm-Wave receivers.

5.1 Frequency Response

Figure 5.1 shows the frequency response, $H_{-15}(f)$ as a function of the input frequency for an LO frequency of 2.5 GHz. Figure 5.2 shows the same plot with

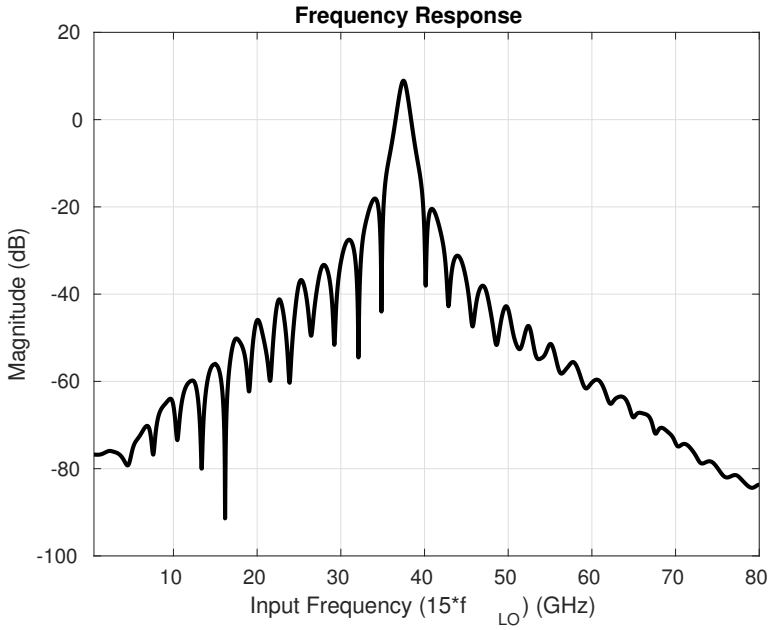

Figure 5.1: $H_{-15}(f)$ for f_{LO} = 2.5 GHz w.r.t. input frequency

respect to the output frequency.

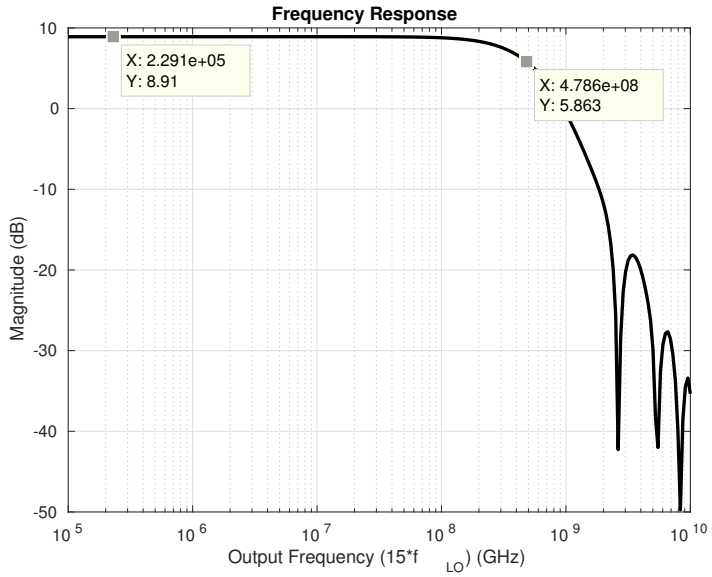

Figure 5.2: $H_{-15}(f)$ for f_{LO} = 2.5 GHz w.r.t. output frequency

5.1.1 RF Filtering Characteristics

Fig. 5.3 shows the RF filtering characteristics of the receiver. It was measured by plotting the frequency response from the input port to the input of the OTA.

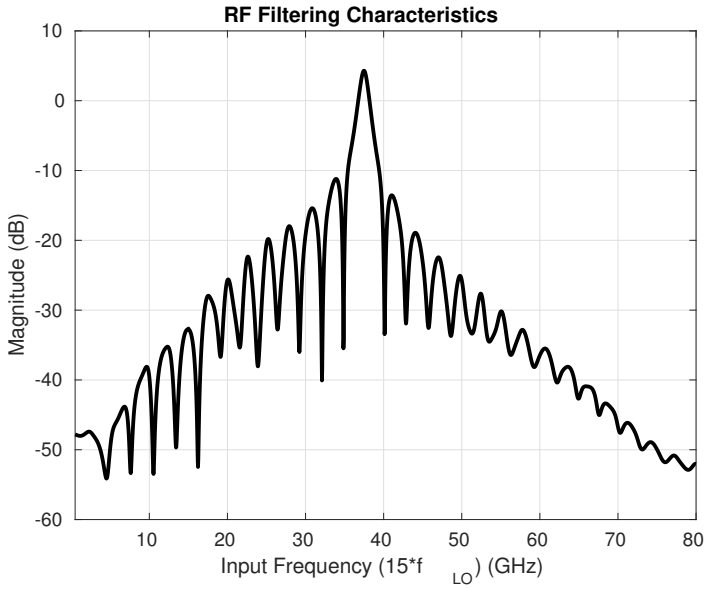

Figure 5.3: RF Filtering Characteristic of $H_{-15}(f)$ for f_{LO} = 2.5 GHz

5.2 Noise Performance

Figure 5.4 shows the integrated double side band (DSB) Noise Figure(NF) of the receiver with the integration bandwidth being 1-400 MHz.

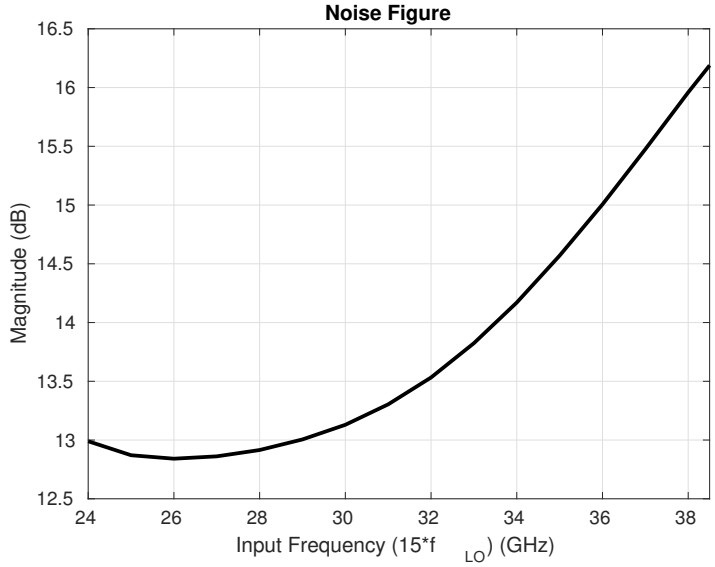

Figure 5.4: Integrated Noise Figure (DSB) VS Input Frequency

5.3 Power Consumption

The only power consuming blocks are the non-overlapping clock generator and the OTAs. Table 5.1 summarizes the power consumption of the receiver.

Table 5.1: Power Consumption Summary of the Receiver

Current Consumption of the clock generator (mA)	7.5-9.9
Current Consumption of the 3 OTAs Combined (mA)	2.25
Current of the Biasing Circuitry (μA)	200
Supply Voltage (V)	1.2
Total Power Consumption (mW)	11.94-14.82

5.4 Linearity Performance

Figures 5.5 and 5.6 show the 1-dB compression points of the circuit at 37.5 GHz and 25 GHz respectively.

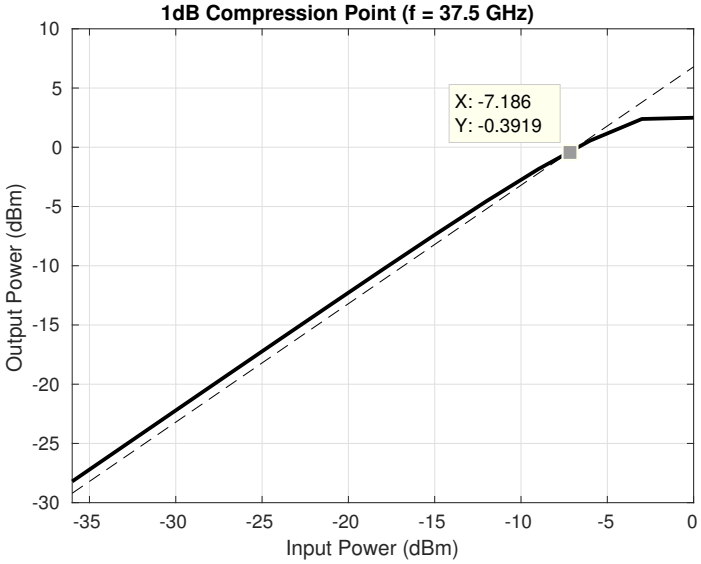

Figure 5.5: 1dB Compression point @ 37.5 GHz

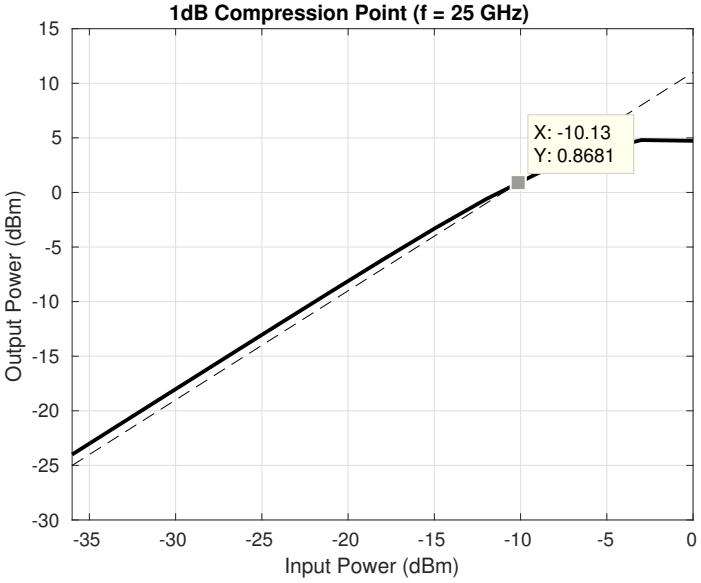

Figure 5.6: 1dB Compression point @ 25 GHz

5.5 Comparison with State-of-the-Art mmWave Receivers

Table 5.2 compares the performance of the proposed receiver with the state-of-the-art.

Table 5.2: Performance summary of the receiver and comparison with state-of-the-art mm-Wave receivers

	This Work	[1]	[11]	[2]	[3]	[4]	[12]
Technology	65 nm CMOS	28 nm CMOS	28 nm CMOS	65 nm CMOS	45 nm CMOS SOI	65 nm CMOS	45 nm RF SOI
Architecture	Mixer-First Direct-Conv	Mixer-First Direct-Conv	Sliding IF heterodyne	Direct Conv	Direct Conv	Mixer-First Direct-Conv	Mixer-First Direct-Conv
Frequency(GHz)	24-38.5	70-100	65-95	75-91	45-66	49-67	20-30
Baseband BW (GHz)	0.48	1.8	N/A	9	1.2	0.32	0.25
Gain (dB)	9-13	21-26	23.6	13	23.2	13	8.9-20.6
NF, DSB(dB)	12.5-16.2	8-12.7	9.5-12.9	5.5-7.5	7.7-12	11-14	8-10.4
IP1dB (dBm)	-10.1 - -7	-26.5 - -18	-30.7 - -25	-16	-28	-12	-13 - -9.3
IP1dB (normalized[a], dBm)	2-2.9	-0.5 - 3	-7 - -1.4	-3	-4.8	1	-0.4 - +7.6
Pdc (mW)	11.9-14.8	12	57	89	22	14	41

[a] IP1dB + Gain - The theoretical IP1dB for 0dB gain

33

CHAPTER 6

Ongoing and Future Work

- Complete analysis of the receiver to obtain closed form expressions of the HTFs using the analysis techniques presented in [6].
- Achieving a better noise figure.
- Monte-carlo and mismatch simulations.
- Layout of the whole chip.
- Post-layout and EM simulations.

APPENDIX A

Ideas That did not Work

This appendix lists other ideas that have been looked into during this research attempt which didn't fully work. Harmonic N-Path filter(NPF), capacitor-stacked harmonic NPF and capacitor-stacked hamonic down-converter were some of them. A brief description of these efforts is mentioned in this chapter.

A.1 Harmonic N-Path Filter

The idea is to add the outputs of k phase-shifted N-Path filters to enhance the value of $H_0(f)$ at a frequency kf_S. By doing so, low frequency clocking can be employed to obtain filtering at only the higher harmonics of the clocking frequency. Figure A.1 shows an example of a 8-phase 4th harmonic filter. The 4 phase shifted N-path filters are obtained by using the technique presented in [9]. The outputs of these filters are then added using an adder. Figure A.2 shows the kernel of the harmonic NPF. This kernel was analyzed using the technique presented in [5] and the corresponding signal-flow graph is shown in figure A.3. Spectre and MATLAB simulations are compared and shown in figure A.4. Excellent agreement is seen. Complete analysis of the structure is not described in this thesis. Therefore, if interested in more detailed analysis, please contact the author.

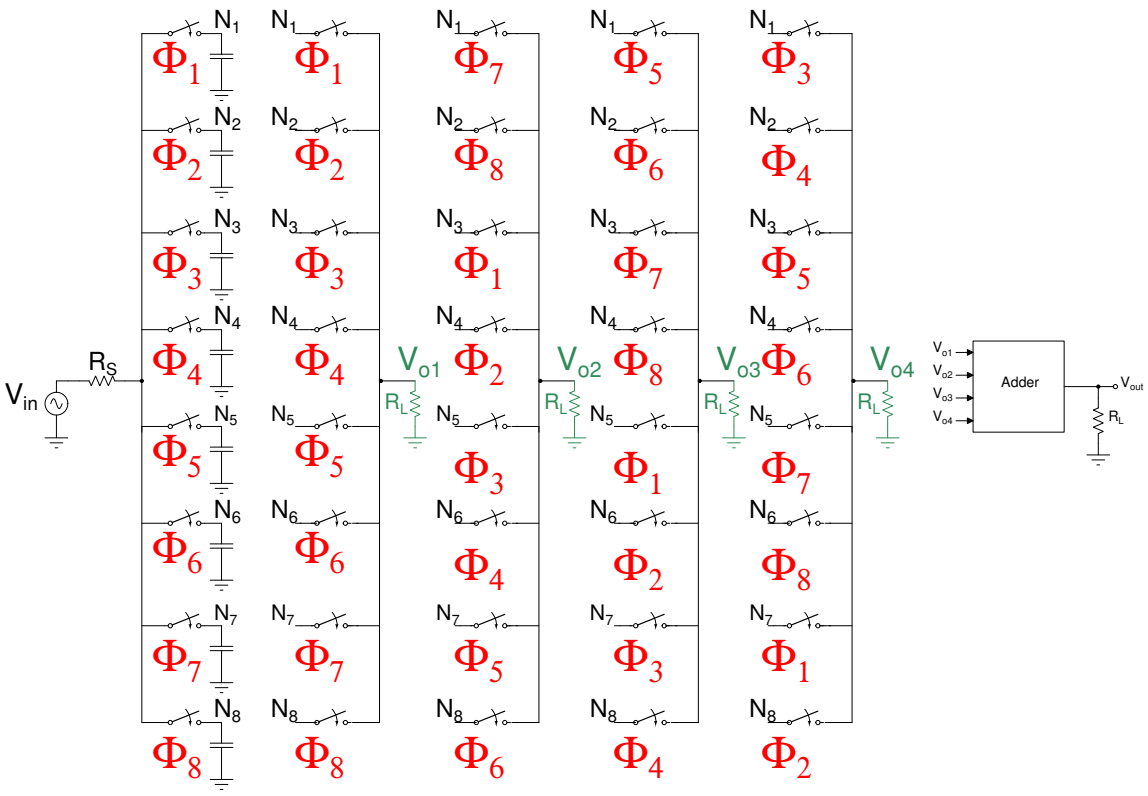

Figure A.1: Harmonic *N*-Path filter conceptual realization

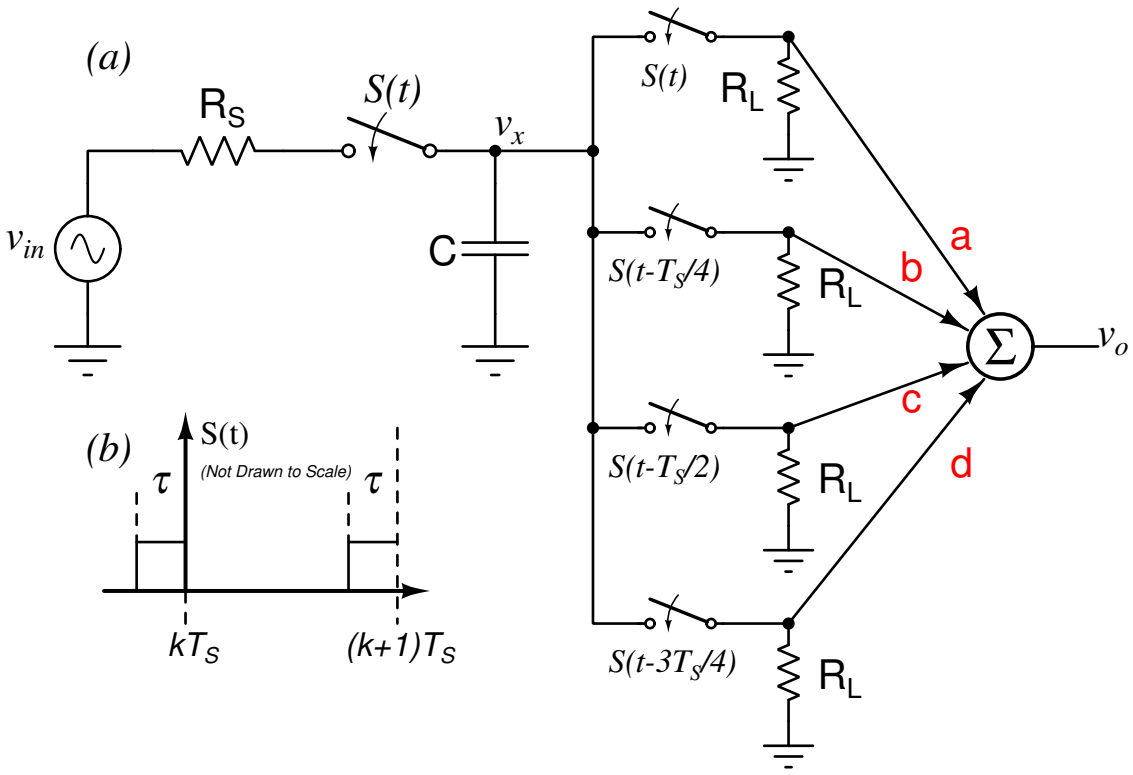

Figure A.2: Kernel of the Harmonic NPF

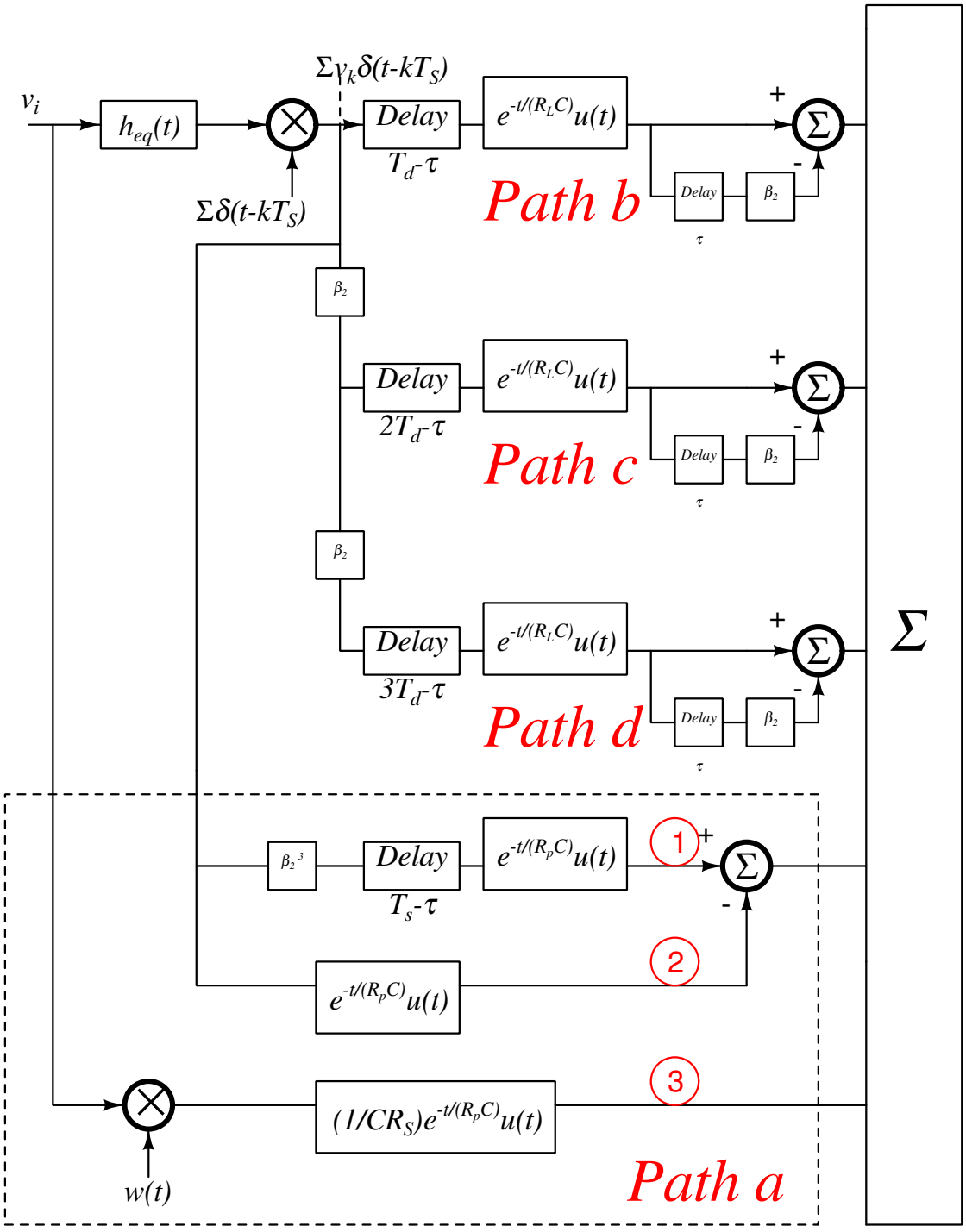

Figure A.3: Signal flow graph of the Harmonic NPF

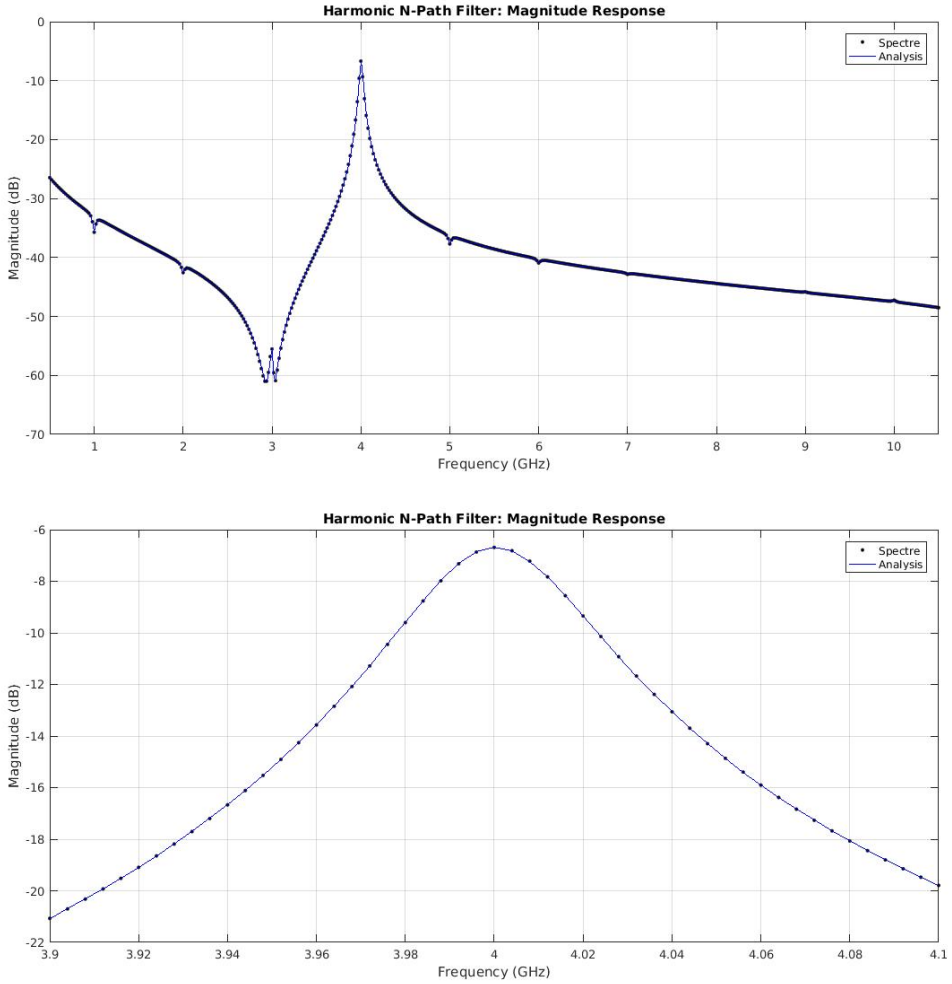

Figure A.4: Harmonic NPF: Spectre VS MATLAB

Realization of this scheme requires an adder. This adder cannot be passive because a passive power combiner can't provide more power at the output than what is received at the antenna input. An active adder, on the other hand, defeats the purpose of using a filter-first receiver, which is to suppress the blockers at the LNA/mixer input. Therefore, a stacked capacitor approach was tried to realize the addition. This is explained in the next section.

A.2 Capacitor-Stacked Harmonic N-Path Filters

Consider the capacitors shown in figure A.1. Let the capacitors be labelled as C_1, C_2, ..., C_8 (from top to bottom). By the virtue of the passive mixing action, the voltage across these capacitors is at DC frequency whenever the input frequency is harmonically related to the clock frequency. More specifically, when the input frequency is 4 (or any other multiple of 4) times the clocking frequency, capacitors $\{C_1, C_3, C_5, C_7\}$ store the same voltage equal to V_0 while $\{C_2, C_4, C_6, C_8\}$ store a voltage equal to V_{180}. In the case of 0 input-DC voltage, $V_0 = -V_{180}$.

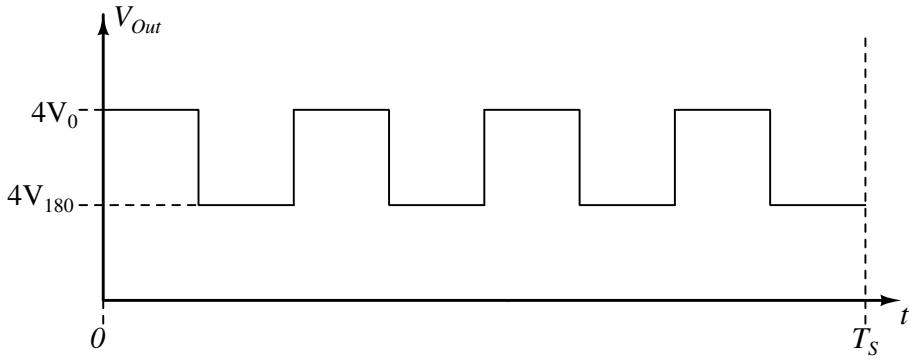

Figure A.5: Output Waveform of the Harmonic N-Path Filter

Figure A.5 shows the output waveform, V_{Out} of the filter. As seen in the figure, the output voltage is a square that toggles between the values $4V_0$ and $4V_{180}$ at a frequency 4 times the switching frequency ($f_S = 1/T_S$). Thus, when compared to a regular N-Path filter, the output of the Harmonic N-Path filter is 4 times larger in amplitude at the 4^{th} harmonic. However, since the capacitors store DC voltages, they can be added by just stacking the appropriate capacitors, at appropriate time instants.

A.2.1 Circuit Realization

Figure A.6 shows how the proposed scheme can be realized using a circuit. Let the capacitor that is connected to the switch S_i, for $i = 1, 2, ...8$, be labelled as C_i. Due to the intuition discussed previously, capacitors $\{C_1, C_3, C_5, C_7\}$ (or $\{C_2, C_4, C_6, C_8\}$) hold the same charge. Therefore, when neither of the switches $\{S_1, S_3, S_5, S_7\}$ (or $\{S_2, S_4, S_6, S_8\}$) are on, the capacitors $\{C_1, C_3, C_5, C_7\}$ (or $\{C_2, C_4, C_6, C_8\}$) can be stacked. The corresponding logic for the control waveforms for stacking are shown in the figure as S_9 and S_{10}.

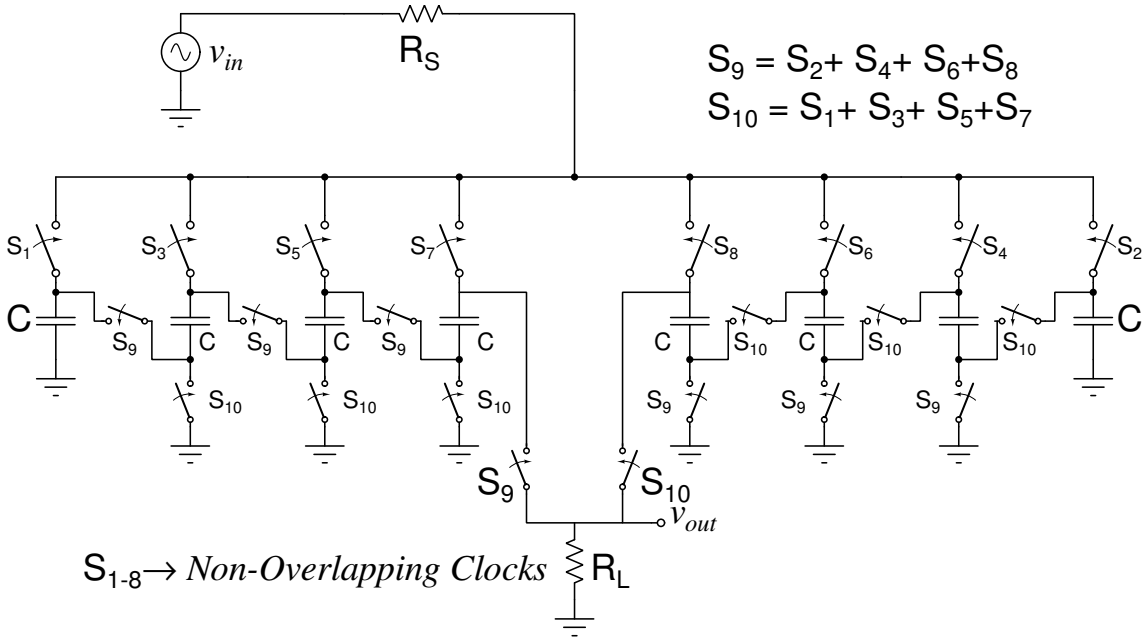

Figure A.6: Schematic of the Proposed Stacked-Capacitor Harmonic N-Path Filter

Due to this, the output waveforms of the filters shown in both figures A.1 and A.6 are expected to be similar to that shown in figure A.5.

A.2.2 *Approximate* Analysis

Due to the charge sharing that occurs between the capacitors, the conventional method of adjoint network cannot easily be applied to calculate the desired transfer function, $H_o(f)$. However, in order to get a rough insight, it is useful to perform the analysis with some approximations for the kernel shown in figure A.7. The following approximations are made to simplify the analysis:

1. The ON-resistance of the switches which connect the capacitors to the ground is zero.
2. Assume that no charge distribution happens among the capacitors during the stacking phases,i.e, it all the charge which a given capacitor loses during a stacking phase is assumed to go completely into the load without effecting the charges on the other capacitors in the stack.

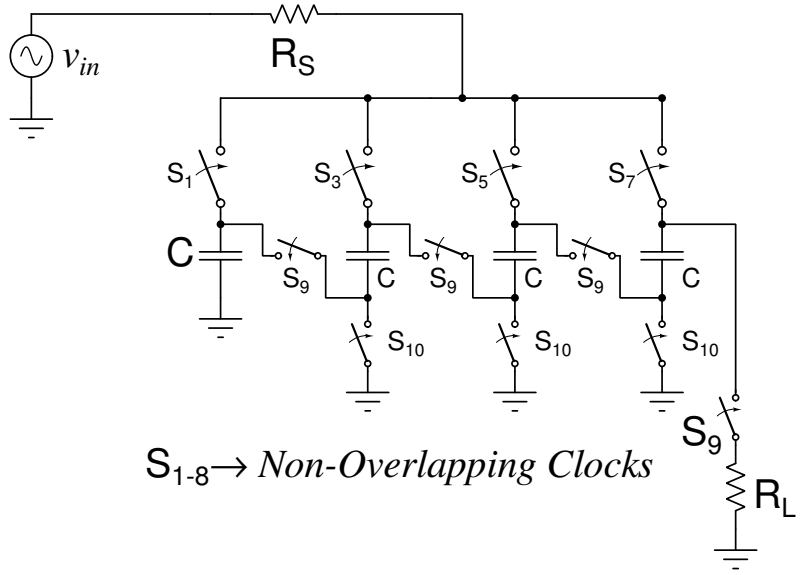

Figure A.7: Kernel of the Stacked-Capacitor Harmonic *N*-Path Filter

With these approximations made, the signal flow graph shown in figure A.8 is obtained for a *sub*-kernel[1]. Spectre and MATLAB results are shown in figure A.9.

[1]Contact the author if interested in the details

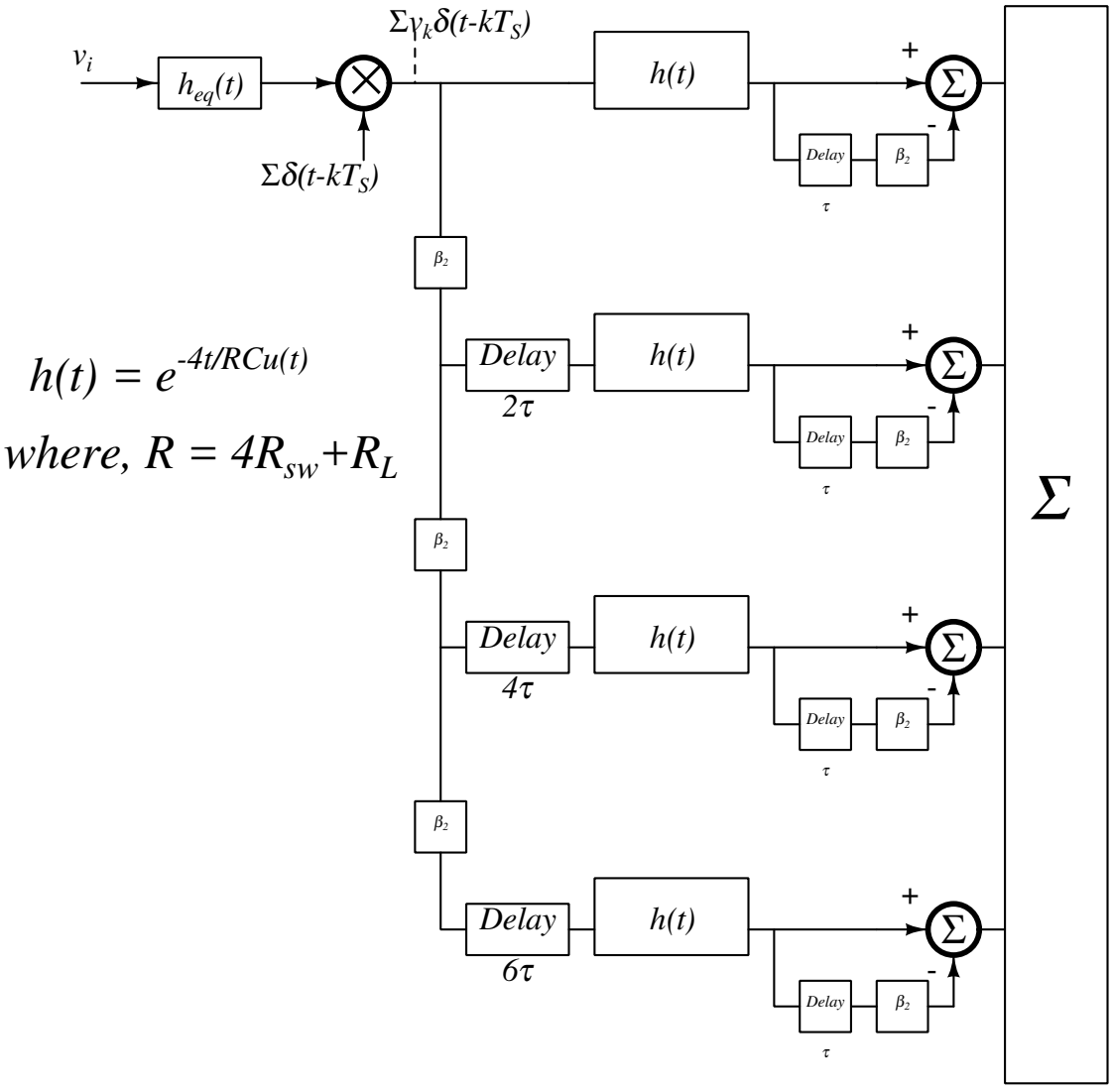

Figure A.8: Signal Flow Graph to determine the $H_0(f)$ of one sub-kernel

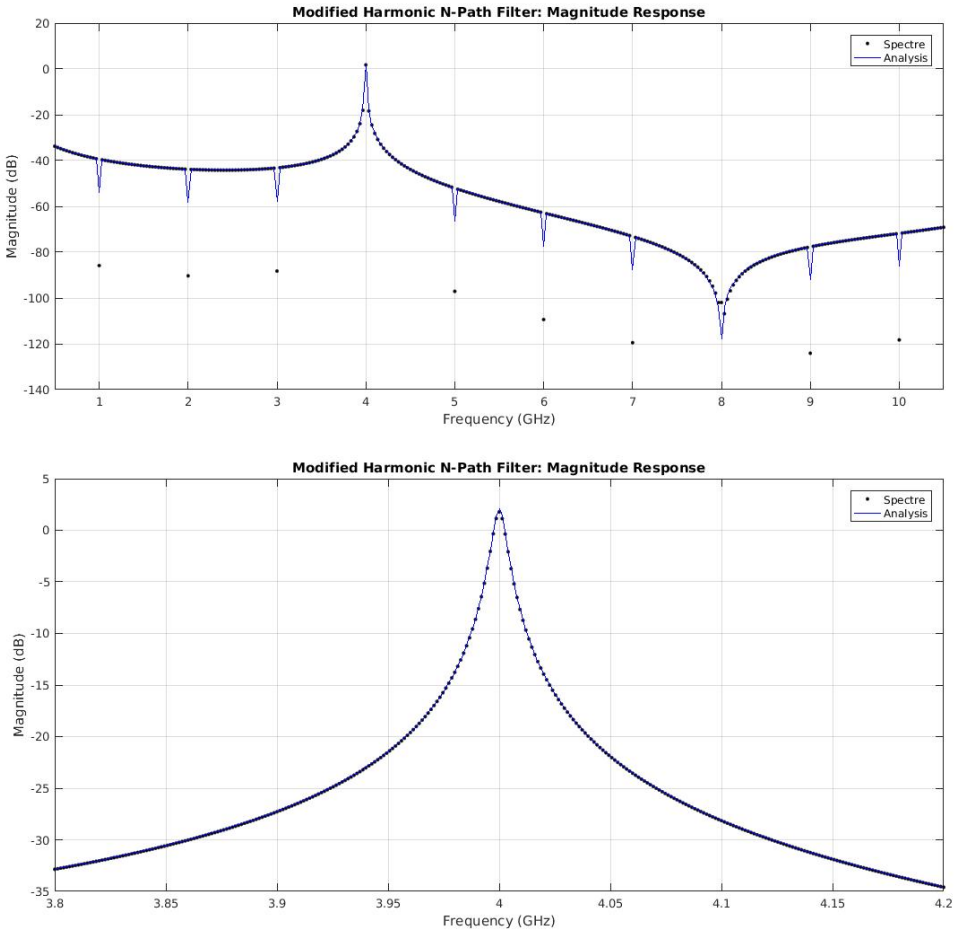

Figure A.9: Capacitor-Stacked Harmonic NPF: Spectre VS MATLAB

The only frequencies at which Spectre and MATLAB results don't agree are at harmonics of the clocking frequencies. This disagreement is due to the approximations made which don't hold good around the multiples of f_S.

While this idea appears appealing, to operate at mm-Wave frequencies, 8 clock phases need to be generated at more than 5 GHz frequency. This is extremely challenging in a 65 nm CMOS technology because of the power requirements and the rise and fall time limitations of the technology.

A.3 Capacitor-Stacked Harmonic Down-Converter

Due to the limitations associated with the capacitor-stacked harmonic down-converter, a solution was needed to utilize harmonics much higher than the 4th. The summation shown in equation (3.16) is one way to achieve the utilization of higher harmonics. This summation is performed using base-band OTAs in figure 3.11. However, since the capacitors store voltages close to DC frequencies, the addition can be performed by just stacking the capacitors. This can be done as shown in figure A.10.

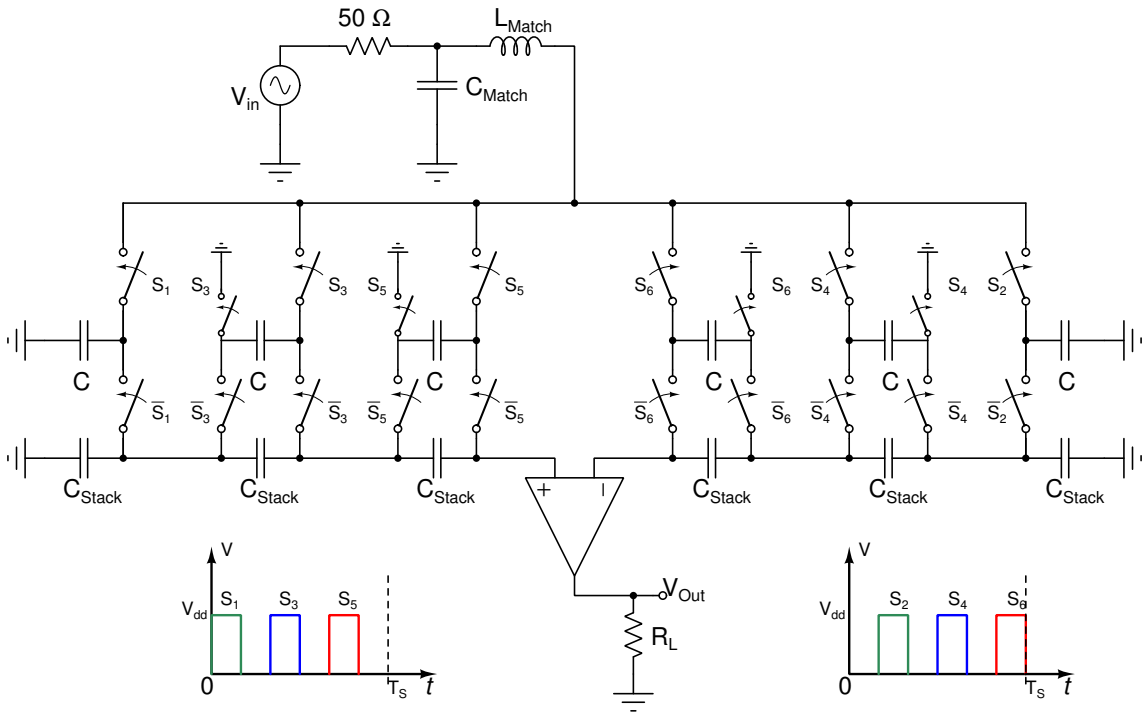

Figure A.10: Topology of the 15^{th} Harmonic Down-Converter

Realization of this scheme requires >20 switches which is more than 3 times of the number of switches needed in figure 3.11. This directly leads to a severe degradation in power and noise performance of the receiver.

Table A.1: Performance summary of the capacitor-stacked down-converter

Peak Input Frequency (= $15 \times f_S$)	38 GHz
Passive Conversion Gain (Input Frequency to DC)	+8.9 dB
Maximum Far-Away Attenuation	40 dB
Noise Figure	30 dB
Current Consumption	65 mA

Table A.1 shows the performance summary of this receiver. As seen from this table, the receiver has a very bad noise performance even with a current consumption of about 5 times as much as the receiver of figure 3.11.

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