SINGLE-STAGE RECEIVERS FOR 5G NETWORKS

A THESIS

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THESIS CERTIFICATE

This is to certify that the thesis titled **SINGLE-STAGE RECEIVERS FOR 5G NETWORKS**, submitted by **ALFRED FESTUS DAVIDSON**, to the Indian Institute of Technology Madras, for the award of the degree of **DUAL DEGREE (BACHELOR OF TECHNOLOGY & MASTER OF TECHNOLOGY)**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Prof. S. Aniruddhan
Research Guide
Associate Professor
Dept. of Electrical Engineering
IIT Madras, 600 036

Place: Chennai

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ABSTRACT

KEYWORDS: 5G mobile communication, current-reuse, low-noise amplifiers, millimeter wave circuits, mixers, phase-shifters, phased-arrays, receivers.

The next generation of mobile communication standards, 5G networks, are expected to satisfy the exponentially growing demand for wireless capacity and data-rates. 5G networks are also set to open up new possibilities and spur innovations in various domains. However, multiple technologies and paradigms need to be materialized to tap the full potential of 5G networks.

On the circuits side, the critical challenge is the implementation of phased-array architectures with multiple antennas and channels on the RF front-end to support beamforming and massive-MIMO. Area and power-efficiency are also crucial to be able to accommodate the entire array of transceivers.

This thesis presents a new phase-shifting architecture that simplifies the RF front-end implementation and reduces its area and power consumption. The proposed architecture achieves IQ down-conversion without the use of quadrature LO signals. The single-stage receiver topology, which has been used for lower carrier frequencies, also fits into the proposed phase-shifting scheme. The analysis and optimization of this topology to work at mmWave frequencies are also presented here.

A 28GHz receiver implementing the proposed optimized single-stage topology was designed and taped-out to validate its performance. The measured results are also presented in this thesis.

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ABBREVIATIONS

ADC	Analog-to-Digital Converter
BB	Baseband
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DNW	Deep-Nwell
EM	Electro-Magnetic
ESD	Electrostatic Discharge
IC	Integrated Circuit
IF	Intermediate Frequency
IQ	In-Phase Quadrature-Phase
ISS	Impedance Standard Substrate
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MIMO	Multiple-Input Multiple-Output
mmWave	Millimeter Wave
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PA	Power Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PPF	Poly-Phase Filter
RF	Radio Frequency
RTPS	Reflection-Type Phase-Shifter
SoC	System-on-Chip
TIA	Trans-Impedance Amplifier
VCO	Voltage-Controlled Oscillator

NOTATION

$\mathbf{F_{LO}}/\omega_{\mathbf{LO}}$	Local-Oscillator Frequency
$\mathbf{F_T}/\omega_{\mathbf{T}}$	MOSFET Transit Frequency
γ	MOSFET Noise Coefficient
$\mathbf{g_M}$	MOSFET Trans-conductance
$\mathbf{k_B}$	Boltzmann Constant
$\mathbf{r_o}$	MOSFET Output-Resistance
$\mathbf{R_s}$	Standard Characteristic Impedance (50Ω)
$\mathbf{T}$	Absolute Temperature

CHAPTER 1

INTRODUCTION

The increased demand for higher data rates, better quality of service, lower latency, and larger wireless capacity has led to a rapid race to the establishment and deployment of the next generation of mobile communication standards, 5G networks. This new standard is envisioned to open up new possibilities in domains such as communication, security, healthcare, transportation, and consumer electronics [13]. To make 5G networks a feasible solution to the increased demand, several technological innovations and advancements are being pursued both in academia and in the industry [3, 4, 22].

1.1 Key Technologies and Challenges in 5G Networks

A variety of potential paradigms and technologies are expected to go into the realization of 5G networks [17]. The previous generations of mobile communications have all used lower carrier frequencies (up to 6GHz), which has led to spectrum congestion and lower quality of connections. Low-frequency carriers also limit the bandwidth of operation and the maximum capacity. 5G networks will tap the unused spectrum in the millimeter-wave (mmWave) frequency range to meet the projected data rate and capacity requirements.

However, mmWave transmissions suffer from more significant path loss and shadowing. This poses severe constrains on the traditional base station-mobile station link budget. The small cell paradigm combats this issue by using an extensive network of

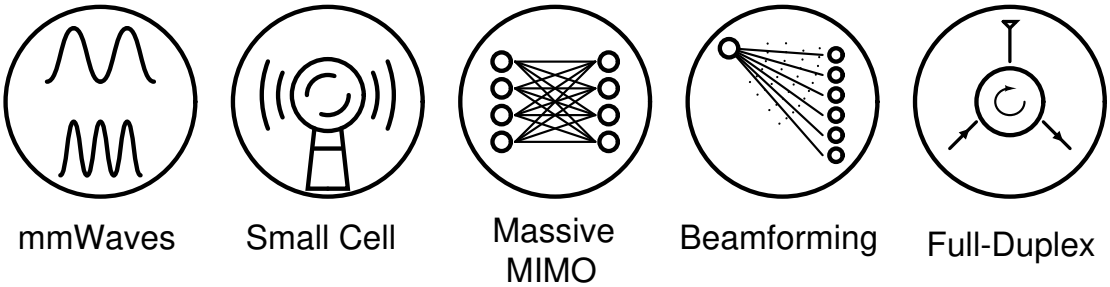


Figure 1.1: Potential enabling technologies for 5G [17]

closely spaced miniature base stations instead of one large base station. This reduced size base station is made feasible by the smaller antenna size required for mmWave signal transmission. Smaller antenna sizes also allow the placement of multiple antennas on the base station and mobile station, paving the way for paradigms such as massive MIMO (multiple-input multiple-output) and beamforming. Massive-MIMO enables the operation of multiple data-links simultaneously, and can significantly improve the spectrum efficiency. However, the co-existence of multiple broadcast links can pose severe interference problems. This is resolved by beamforming, which uses phased-arrays to create highly directional and power-efficient links. Beamforming also helps mitigate the difficulties in closing the link budget in mmWave channels. Paradigms like full-duplex, which can enable simultaneous transmission and reception over the same frequency to further improve spectrum efficiency, are also being considered for the 5G standard.

1.2 IC Design and 5G Networks

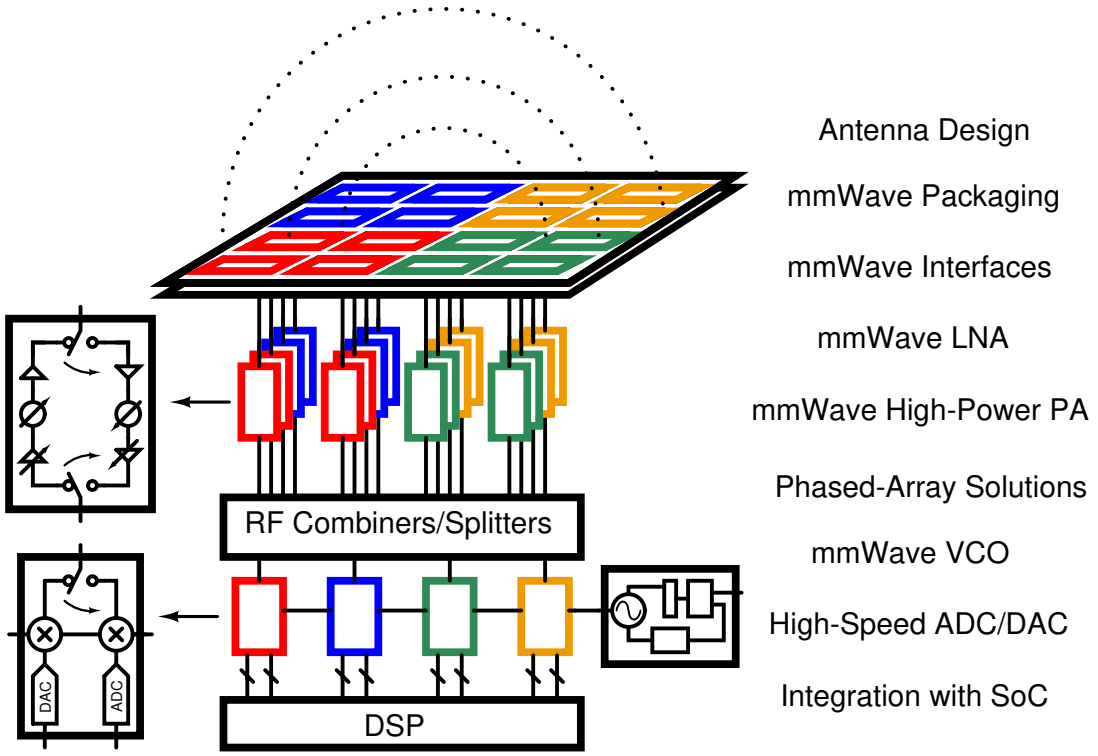


Figure 1.2: Typical 5G front-end architecture for supporting 4×4 MIMO with 4 antenna beamforming [3]

IC design for mmWave circuits presents a variety of challenges that need to be overcome. These include pushing transistors to operate while approaching their transit

frequencies, ensuring efficient signal transmission on top of lossy silicon substrates, and running additional EM simulations for design verification and validation.

In the context of mmWave 5G networks, the design and integration of multiple RF channels required to meet the link budget is a major challenge. This involves low-power mmWave phased-array SoC, low-power low-noise amplifiers, mmWave EM interfaces and packages, mmWave VCOs with wide tuning range, and high-power high-efficiency mmWave power amplifiers [13].

The phased-array RF front-end, which allows beamforming, requires an array of transceivers and antennas with independent phase control. We address the primary circuit and system-level challenges involved in designing the receiver segment of the phased-array. Considering the requirements of a mobile station, we present a new phase-shifting architecture that results in a more compact and low-power design. A receiver that implements a single-stage topology with current reuse fits naturally into the proposed phase-shifting scheme. A new optimized single-stage topology is presented here, along with the analysis and comparison of this topology with variants from past literature. A 28GHz receiver implementing this proposed single-stage topology has been designed and taped-out to validate its performance. The measured results are also presented here.

Chapter 2 presents the proposed integrated phase-shifting scheme in the context of phased-array receivers. Chapter 3 discusses the conventional single-stage receiver and its working principle. Chapter 4 presents the design and analysis of the proposed optimized single-stage receiver topology, while Chapter 5 contains its implementation details and Chapter 6 presents the measurement results. Chapter 7 concludes this thesis.

CHAPTER 2

THE PHASED-ARRAY

One of the key aspects of the mmWave 5G architecture is the use of phased-array RF front-ends with multiple antennas to support beamforming, which helps combat fading, shadowing, and path loss at mmWave frequencies. Several circuit architectures have been proposed in literature to integrate phase-shifters into a regular transceiver chain to make it a phased-array transceiver.

We consider the major phased-array receiver architectures and then illustrate a new phase-shifting architecture that results in a compact and low-power implementation.

2.1 Conventional Receiver Chain Implementations

We consider the conventional receiver chain consisting of an LNA, mixer, and ADC. A phased-array receiver can be realized using different phase-shifting architectures, such as LO-path phase-shifting [19, 23], RF-path phase-shifting [7, 11, 12, 18], digital phase-shifting [21] and hybrid phase-shifting [16].

The phase-shifting architecture employed changes the linearity, gain, noise, power, and area requirements of each block in the receiver chain [13]. Phase-shifting in the RF path results in a low-power and area-optimized design (Fig. 2.1). While this relaxes the linearity constraints on the mixer, the phase-shifter loss and noise figure become critical and need to be optimized. Phase-shifting in the LO-path increases the power and area overhead due to the presence of multiple mixers (Fig. 2.2). However, this scheme allows gain-invariant phase-shifting across the RF frequency range. Digital and hybrid phase-shifting results in a more flexible and reconfigurable architecture at the cost of much higher power and area overhead (Fig. 2.3), as multiple RF channels have to be independently processed at baseband.

All of the above architectures require a phase-shifting circuit that has variable phase control [6]. Phase-shifting can be achieved by using passive techniques like switched

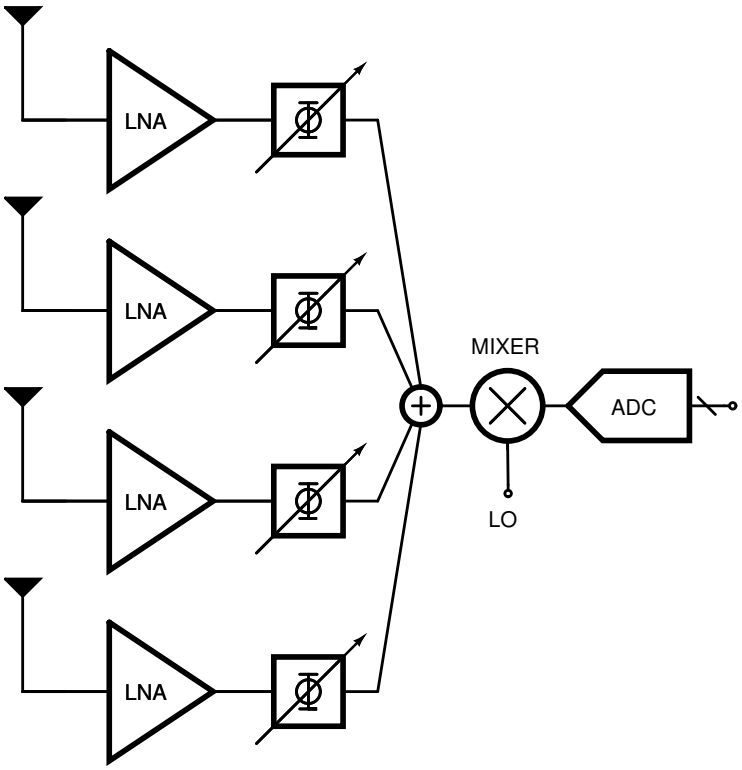


Figure 2.1: RF-path phase-shifting.

LC sections [5, 11, 12] and RTPS [7], or by using active techniques, involving IQ signal generation and interpolation [18, 23]. IQ signal generation can be achieved by using poly-phase filters (PPF) [14] or quadrature-hybrids [24].

Another critical implementation aspect is the choice of the IF frequency, leading to architectures such as direct-conversion, low-IF, sliding-IF, dual-conversion receivers, and direct-sampling. Direct-conversion receivers avoid the burden of image filtering and associated circuit power and area overheads, while the other IF architectures allow for easier signal processing and lower sensitivity to mismatch as they operate at a lower IF frequency [11].

Different schemes can be optimized for different requirements. We consider the requirements for a mobile station, which needs a low-power and area-efficient implementation. A direct-conversion RF-path phase-shifting scheme is chosen for this. We note that this scheme can be implemented for a variety of LNA and mixer topologies. We present an integrated phase-shifting scheme and single-stage receiver topology that complements each other to realize area and power optimization goals.

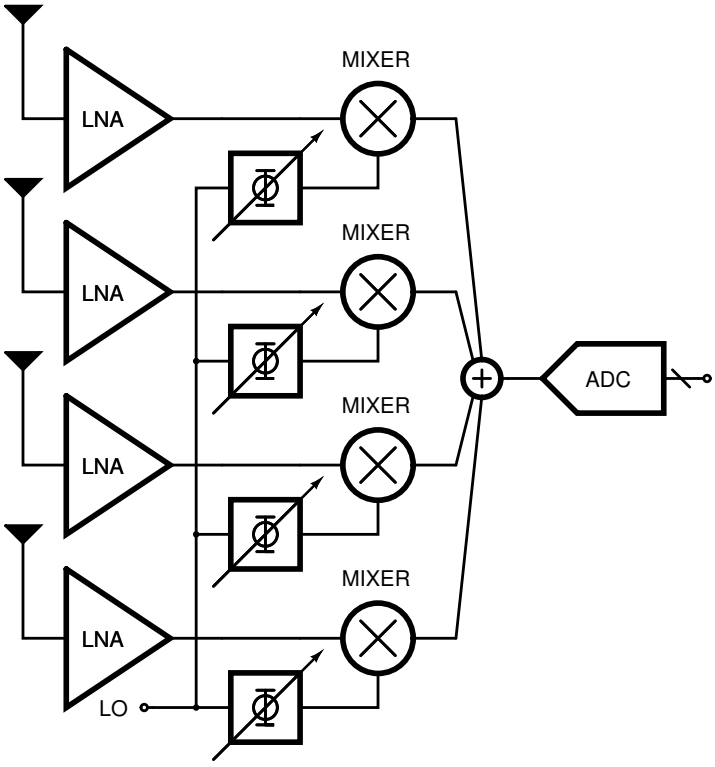


Figure 2.2: LO-path phase-shifting.

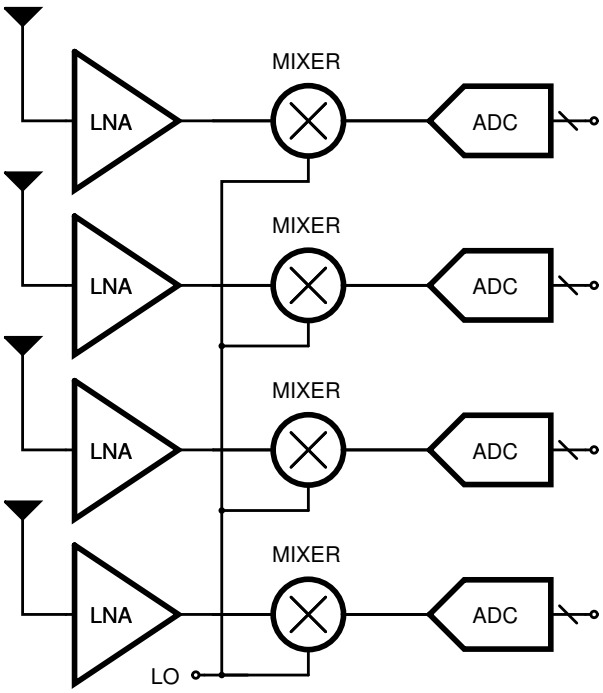
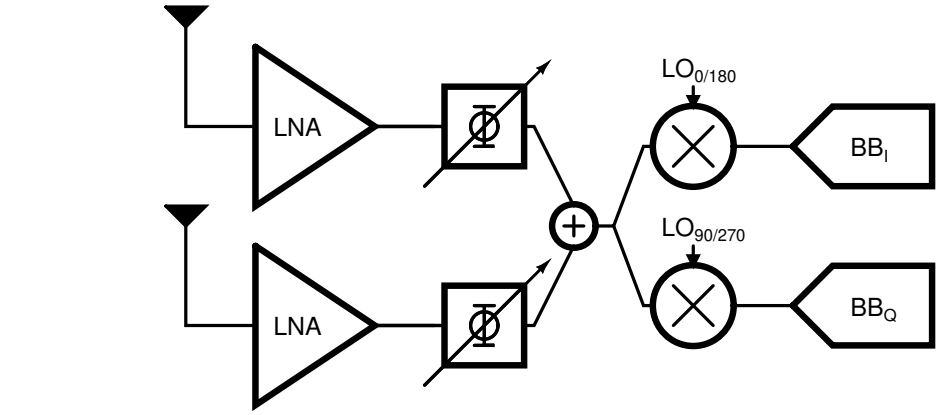


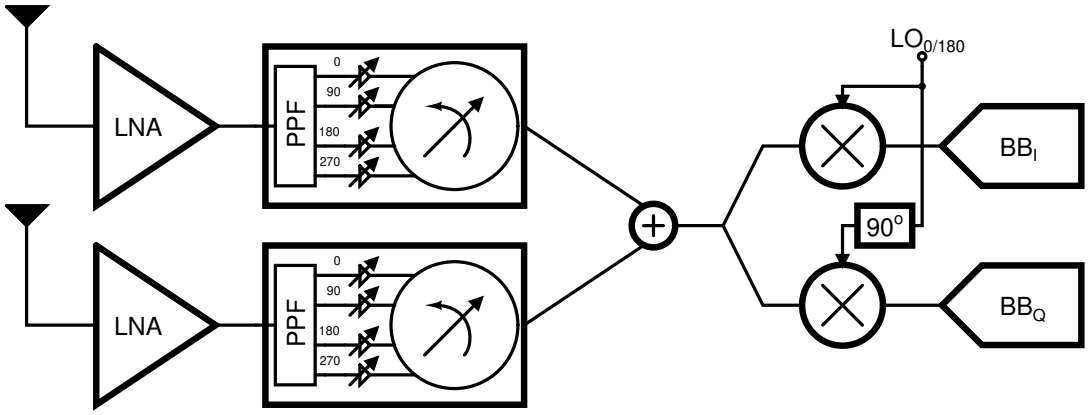
Figure 2.3: Digital phase-shifting.

2.2 Proposed Integrated Phase-Shifting Scheme

We first consider a conventional direct-conversion 2-channel phased-array receiver (Fig. 2.4a), with phase shifting in the RF path. Fig. 2.4b describes a potential implementation of this architecture. We note that we are generating multiple phase-shifted versions of the input in the RF path. We are also generating quadrature-phase LO signals to implement an IQ Receiver.



(a)



(b)

Figure 2.4: Conventional 2-channel phased-array direct-conversion receiver: (a) Top level block diagram; (b) Typical PPF-based implementation

The phase-shifter on the RF-path is essential for the phased-array to facilitate beamforming. The phase-shift on the LO-path is a constant 90° shift, as opposed to the variable phase-shifter on the RF-path. The LO-path phase-shift can be generated using a quadrature-hybrid, but it will lead to increased area overhead. A PPF-based implementation can be used, but it will require additional tuning and digital control for accurate quadrature generation. A QVCO is a viable solution for direct-conversion receivers

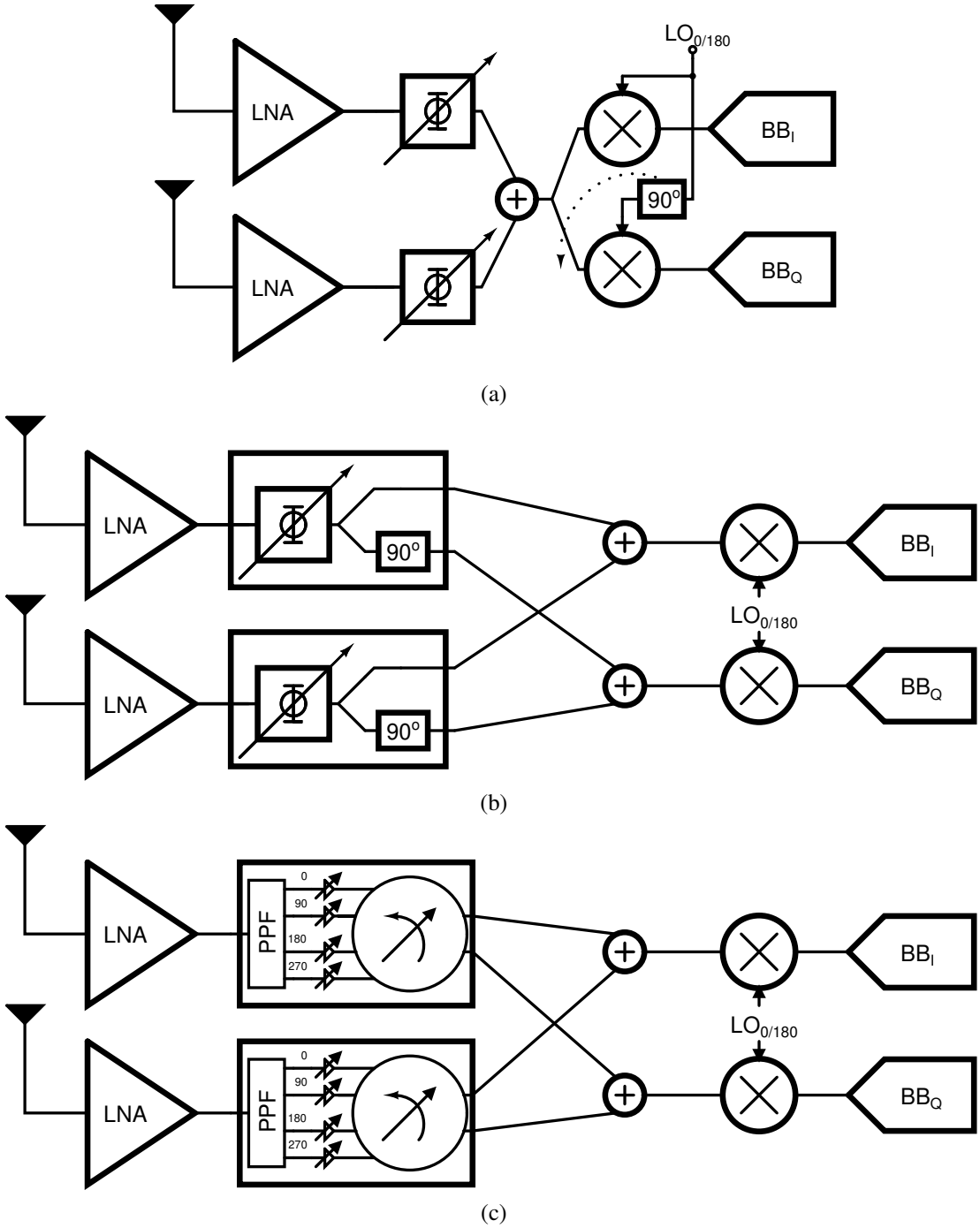


Figure 2.5: Proposed 2-channel phased-array receiver: (a) Development from conventional implementation; (b) Top level block diagram; (c) Current-steering PPF-based implementation.

[2, 11], as it can directly generate the required LO phases, but at the cost of tuning-range, phase-noise, power consumption, and area when compared to a regular VCO.

The proposed integrated phase-shifting scheme completely removes the need for quadrature LO signals, greatly simplifying the receiver architecture. This proposed architecture depicted in Fig. 2.5b can be understood as moving the 90° phase-shift from the LO-path onto the RF-path (Fig. 2.5a). Now, instead of the phase-shifter giving a single phase-shifted output, it must also give a 90° phase-shifted output as well.

To motivate the realization of this scheme, we consider an active PPF-based phase-shifting scheme on the RF-path. The PPF will generate quadrature phase-shifted versions of the RF signal, which will then be appropriately summed to get the required phase-shifts. Assuming a current-mode implementation, this is equivalent to a form of current-steering, where a part of the current is used and summed at the output of the phase-shifter. The proposed implementation scheme shows how the part of the current not used to generate the output phase can be utilized to generate a quadrature phase-shifted output as well. For this scheme to work, we need to show that for any given phase-shift on the RF-path, we can also generate quadrature phase-shifted outputs that can be down-converted by mixers without the need for quadrature LO signals.

2.3 Working of the Integrated Phase-Shifting Scheme

We assume that we have quadrature phases of the input signal, with a fixed amplitude. A PPF or a quadrature-hybrid can generate this. We also assume that if a part of the signal is used to generate one phase, the remaining part of the signal can be used to generate another phase. A current-mode implementation naturally gives this flexibility.

Our objective is to show that given the input quadrature phases 0°, 90°, 180° and 270°, we can generate quadrature phase-shifted signals of any required phase-shift.

Let v_k represent one of the input quadrature phases (0°/90°/180°/270°), and v_{k+1} be the input phase 90° shifted from it. Hence, in this notation, $v_{k+2} = -v_k$.

Let the required output phase lie in the quadrant characterized by the input phases v_i and v_{i+1} such that

$$s_{I+} = \alpha v_i + \beta v_{i+1} \tag{2.1}$$

where α and β are the scaling coefficients. We can also generate its differential counterpart as follows:

$$s_{I-} = \underbrace{\alpha v_{i+2} + \beta v_{i+3}}_{-s_{I+}} \tag{2.2}$$

This is the conventional implementation, where each input phase is used once to generate either the in-phase positive or in-phase negative signal. However, we note we can also generate the following signals using the part of the input signals not used in generating the in-phase output.

$$\begin{aligned} s_{Q+} &= (1-\beta)v_{i+1} + (1-\alpha)v_{i+2} \\ s_{Q-} &= (1-\beta)v_{i+3} + (1-\alpha)v_i \end{aligned} \tag{2.3}$$

Orthogonality of s_{I+} and s_{Q+} can be satisfied by ensuring that their dot product evaluates to zero, giving the relation

$$\begin{aligned} s_{I+} \cdot s_{Q+} &= (\alpha v_i + \beta v_{i+1}) \cdot \left((1-\beta)\, v_{i+1}^* + (1-\alpha)\, v_{i+2}^*\right) \\ 0 &= -\alpha(1-\alpha)|v|^2 + \beta(1-\beta)|v|^2 \\ \Rightarrow \quad & \alpha(1-\alpha) = \beta(1-\beta) \\ \Rightarrow \quad & \alpha + \beta = 1 \end{aligned} \tag{2.4}$$

It can also be shown that this relation for α and β also ensures that the magnitude of each of the output phases is equal for any given phase-shift. However, there is an amplitude dependence across phase-shifts, which can be corrected.

Hence, our integrated phase-shifting scheme is as follows:

1. Choose the quadrant in which the required output phase-shift is present. Let the input phases that form this quadrant be v_i and v_{i+1}
2. Choose the scaling factor α such that the required phase-shift is obtained with the combination $\alpha v_i + (1-\alpha)v_{i+1}$
3. The output phases will now be
   (a) $s_{I+} = \alpha v_i + (1-\alpha)v_{i+1}$
   (b) $s_{I-} = \alpha v_{i+2} + (1-\alpha)v_{i+3}$
   (c) $s_{Q+} = \alpha v_{i+1} + (1-\alpha)v_{i+2}$
   (d) $s_{Q-} = \alpha v_{i+3} + (1-\alpha)v_i$

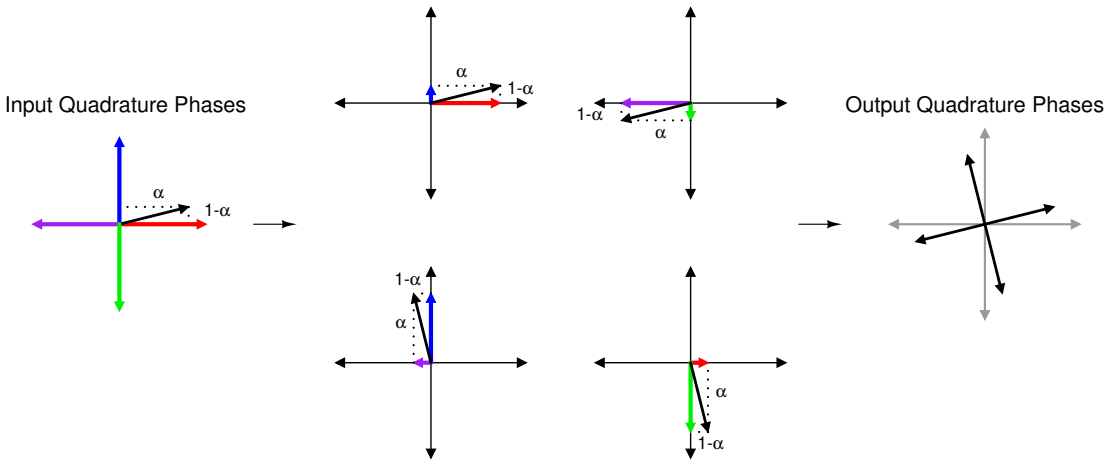


Figure 2.6: Illustration of the working of the integrated phase-shifting scheme.

It can be shown that the maximum to minimum amplitude variation for this phase-shifting scheme is 3dB (or a 1.5dB variation about the average). This scheme is illustrated in Fig. 2.6, where each of the input quadrature phases is split into two parts to generate the required output quadrature phases.

The key aspect of this scheme is the full use of the generated quadrature phases of the RF signal, which is used to achieve IQ down-conversion without the need for quadrature LO signals, significantly reducing the area and power requirements of the receiver. This is different from using a phase-shifter that can give quadrature phase-shifted outputs by using two independent paths for the I and Q outputs, and thereby incurring larger area and power overheads.

While we have eliminated the 90° phase-shift on the LO-path, we could have chosen to eliminate the phase-shifting in the RF-path instead [20]. However, the resulting topology would require multiple mixers to achieve IQ down-conversion, adding area and power penalties. We have emphasized a current-steering PPF-based RF-path phase-shifting for a more power-efficient architecture and compatibility with the single-stage topology that further brings down power and area. A quadrature-hybrid based approach has been proposed in [24], but instead of using the quadrature RF signals to eliminate quadrature LO signals, it attempts to use both the signals to down-convert two conjugate beams simultaneously, at the cost of additional mixers and baseband channels.

CHAPTER 3

THE BASIC SINGLE-STAGE RECEIVER

mmWave 5G architectures require multiple RF channels to meet the diversity and link budget requirements. Multi-antenna RF front-ends also allow for massive-MIMO and beamforming. We attempt a single-channel receiver block that can be easily integrated into such designs. We consider the requirements of a mobile station receiver, which has the added constrains of area and power so that the entire array of such receivers can be accommodated on the chip.

To accomplish this, we decide to adopt the single-stage topology, wherein low-noise amplification, down-conversion, and filtering are achieved in a single stage, reducing the area occupied. Such a topology can be realized using current-reuse techniques, which have the added benefit of lower power consumption. A receiver employing current-reuse between multiple stages would require a stacked implementation, which would result in voltage headroom issues. The single-stage receiver topology alleviates this issue by implementing the functionality of multiple stages onto a single stage by isolating these functions in the frequency domain.

The single-stage topology was first reported in [15], and has since been substantially modified and improved upon for various specialized requirements such as multi-band cellular receivers [1], high dynamic-range [8] and low-noise applications [9]. Since this topology uses the same devices for both baseband and RF functions, each stage's design is not independent of the other stages. There is an inherent trade-off between the performance specifications when the RF or baseband functions are optimized. We present a modified single-stage receiver topology that decouples some of these design aspects to allow for more straightforward optimization.

This chapter describes the conventional single-stage topology and its working, while the next chapter details the optimized topology.

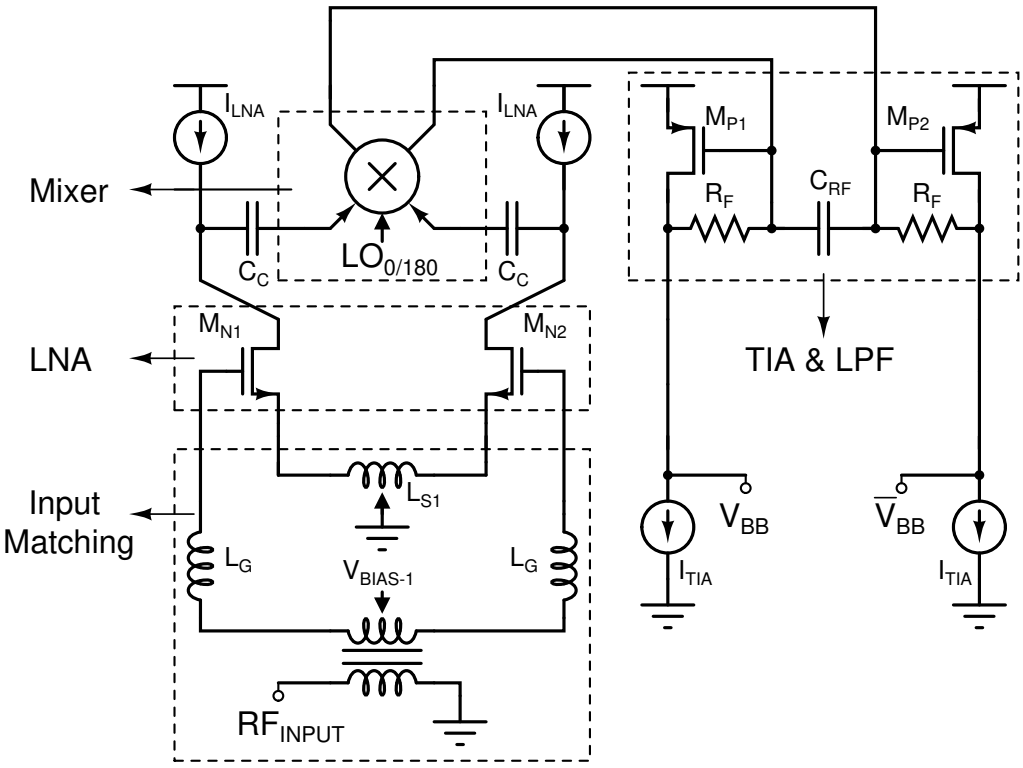


Figure 3.1: Conventional multi-stage receiver implementation.

3.1 Overview

The fundamental idea behind the single-stage topology is that the same components of the circuit perform different functions for RF and baseband signals, allowing the receiver chain to be condensed into a single stage. We develop this topology adapted from [9] by considering a multi-stage implementation of a receiver front-end, and show how the single-stage receiver topology accomplishes the same functionality.

3.2 Principle of Operation

Fig. 3.1 depicts a conventional multi-stage receiver chain with an input matching circuit and low-noise amplifier (LNA) that converts the input RF signal into a current, a current-mode passive mixer that down-converts the RF signal into baseband, and a trans-impedance amplifier (TIA) with first-order low-pass filtering (LPF). This same signal flow can be traced in the single-stage receiver shown in Fig. 3.2. The RF and baseband equivalent circuit of this topology is shown in Fig. 3.3 to clearly describe the circuit functionality.

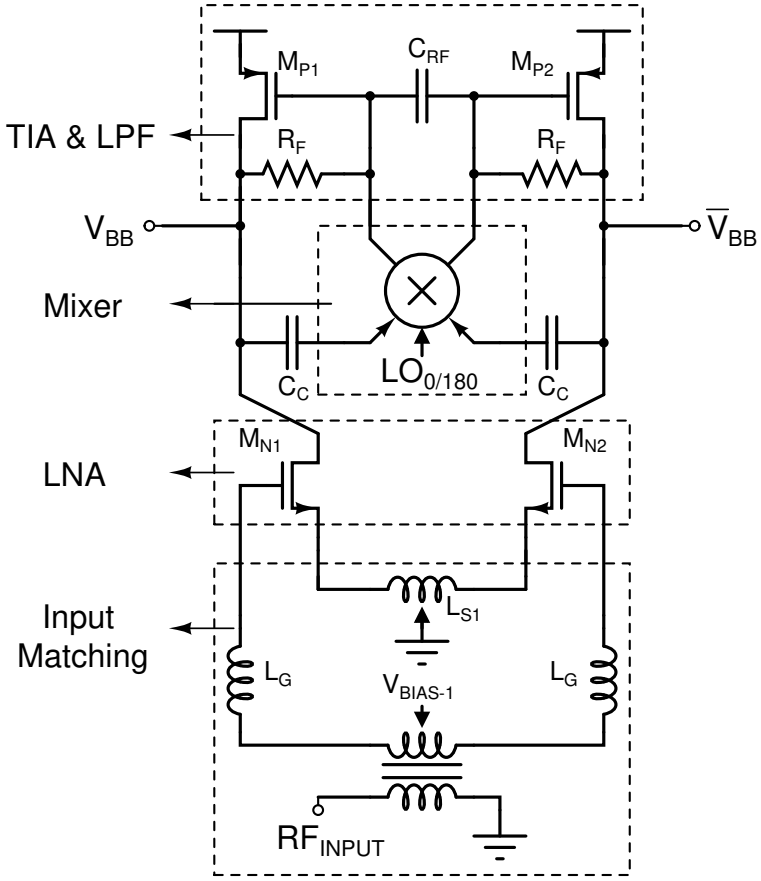


Figure 3.2: Conventional single-stage receiver implementation.

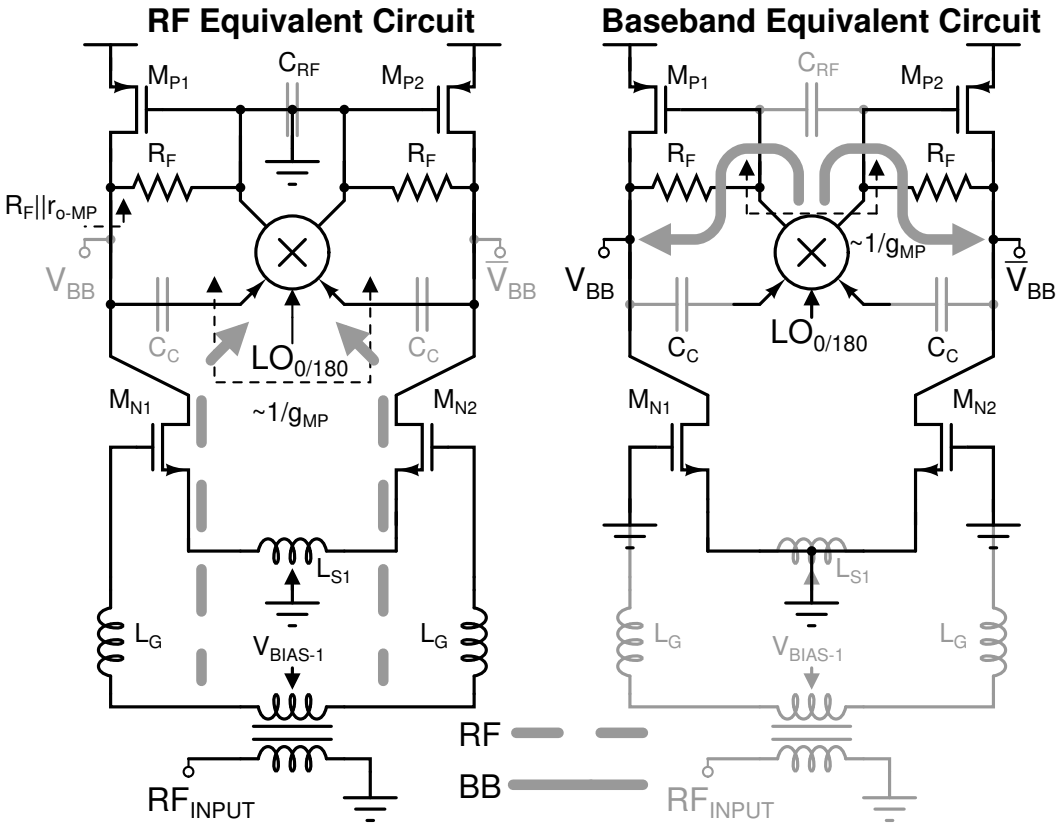


Figure 3.3: Equivalent small-signal schematic of the single-stage receiver.

Traversing from the input, we first have an input matching circuit and then the trans-conductor $M_{N\text{-}1,2}$, which converts the RF input into a current, functioning as the LNA. MOSFETs $M_{P\text{-}1,2}$ function as current sources for the LNA. With C_C behaving like a short circuit for RF signals, the RF current now flows into the low input impedance of the passive current-mode mixer as opposed to the larger impedance presented by $M_{P\text{-}1,2}$ and resistor R_F. This large resistance is a result of the capacitor C_{RF} behaving like a short circuit for RF frequencies, which then creates a virtual ground for the differential input signal.

The passive current-mode mixer down-converts the RF current into a baseband current, which then flows into the low impedance input of the trans-impedance amplifier. Here, C_{RF} behaves like an open circuit for the baseband signal. It also shunts any RF signal, creating a first-order low-pass filter. MOSFETs $M_{N\text{-}1,2}$ now function as a current source for the trans-impedance amplifier, which converts the baseband current into the output baseband voltage.

We again note that there are no headroom penalties with this topology as there is no stacking of stages, the same circuit behaves like an LNA/Mixer for RF frequencies and a trans-impedance amplifier/low-pass filter for baseband frequencies.

CHAPTER 4

DEVELOPMENT OF THE OPTIMIZED SINGLE-STAGE RECEIVER

From the basic single-stage receiver topology, we develop an optimized topology by addressing the specific challenges posed by mmWave circuit designs with the objective of optimizing area and power without compromising on performance.

In the multi-stage receiver shown in Fig 3.1, we note that the RF noise of $M_{N\text{-}1,2}$ and the baseband noise of $M_{P\text{-}1,2}$ directly add on to the signal path, and are dominant sources of noise. However, in a single-stage receiver, the same device's RF and baseband noise can add on to the signal path, deteriorating the noise figure. While a single-stage implementation does not leave much room for further optimization, the addition of another signal path for implementing an IQ receiver presents an opportunity to optimize both the paths together. We present a new implementation that achieves this optimization, and we compare its performance with implementations from prior literature. For this comparison, the circuits in Fig. 4.1, Fig. 4.2, Fig. 4.3 and Fig. 4.4 are assumed to consume the same current.

4.1 Overview

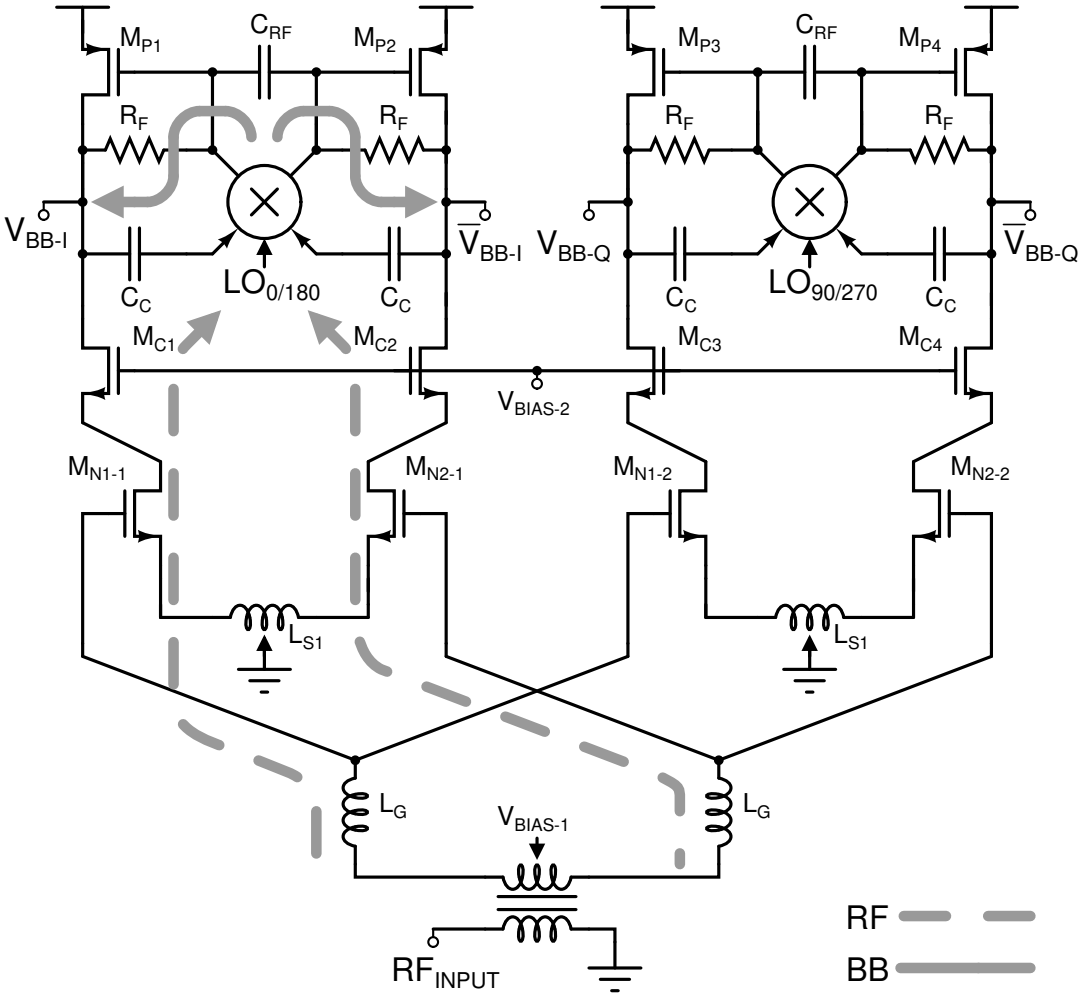


Figure 4.1: Single-stage receiver implementation - 1

In the basic topology depicted in Fig 3.2, we note that the baseband output node is at the drain of the input trans-conductor stage. The input trans-conductor needs to be designed at minimum length to realize a high F_T device that can operate at mmWave frequencies. This results in the device exhibiting significant channel length modulation. The amplified baseband voltage can modulate the g_M of the input trans-conductor, resulting in poor linearity. We mitigate this by adding a cascode structure to isolate the baseband output node and the input trans-conductor.

The conventional method to convert this topology into an IQ receiver involves creating a copy of the primary circuit with a shared input balun and inductor L_G (*Implementation - 1* in Fig. 4.1).

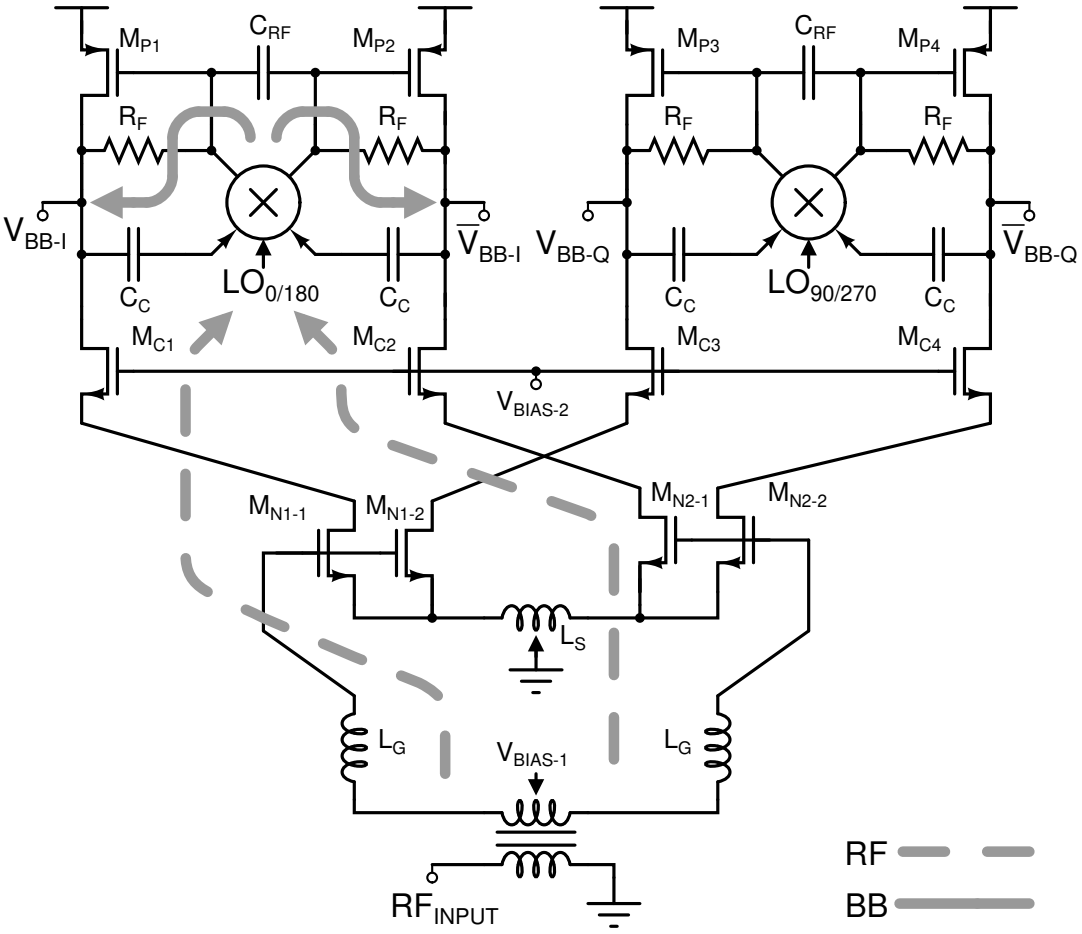


Figure 4.2: Single-stage receiver implementation - 2

However, we note that we can get a $4\times$ decrease in the required value of the source inductance by adopting *Implementation - 2* depicted in Fig 4.2, reducing the area of the circuit. Here, L_S=L_{S1}/2 for maintaining the input matching, while MOSFETs M_{N-1} and M_{N-2} in Fig. 4.1 are implemented as two independent split MOSFETs $M_{N1-1,2}$ and $M_{N2-1,2}$ respectively in Fig. 4.2.

In Fig. 4.1 and Fig. 4.2, we note that the noise of the input trans-conductor appears at the baseband output node both via the standard RF path after down-conversion, as well as directly via the baseband path through the cascode device. This does not allow for straightforward optimization of the receiver as a larger g_M input trans-conductor that increases the receiver gain also adds increased RF and baseband noise at the receiver output.

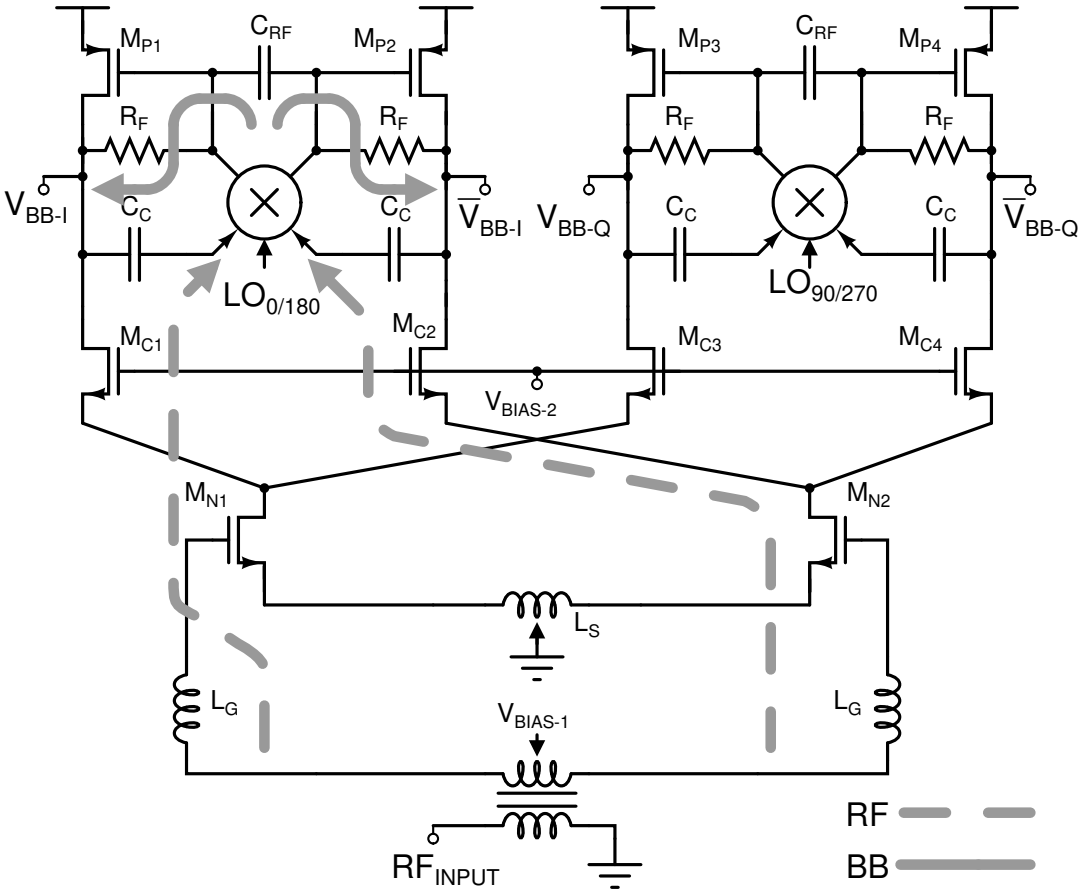


Figure 4.3: Single-stage receiver implementation - 3 adapted from [10].

Implementation - 3 (Fig. 4.3) depicts an improved implementation adapted from [10]. Here, the RF signal is split after the input trans-conductors M_{N-1} and M_{N-2}, resulting in a 3dB reduction in the noise due to the input trans-conductors. This can be interpreted as having two components in parallel, giving the same signal transfer function, but reducing the output noise spectral density.

We note that the cascode devices M_C act like a DC current splitter for the baseband trans-impedance amplifier. However, the current for the in-phase and quadrature-phase outputs are supplied by the same trans-conductors, resulting in reduced IQ isolation. Signals from node V_{BB-I} and V_{BB-Q} can potentially interfere with each other through M_{C1} and M_{C3} at the drain of M_{N1}.

Furthermore, the cascode and input trans-conductor devices contribute both to baseband and RF noise in this implementation, adding to the optimization problems of the single-stage topology.

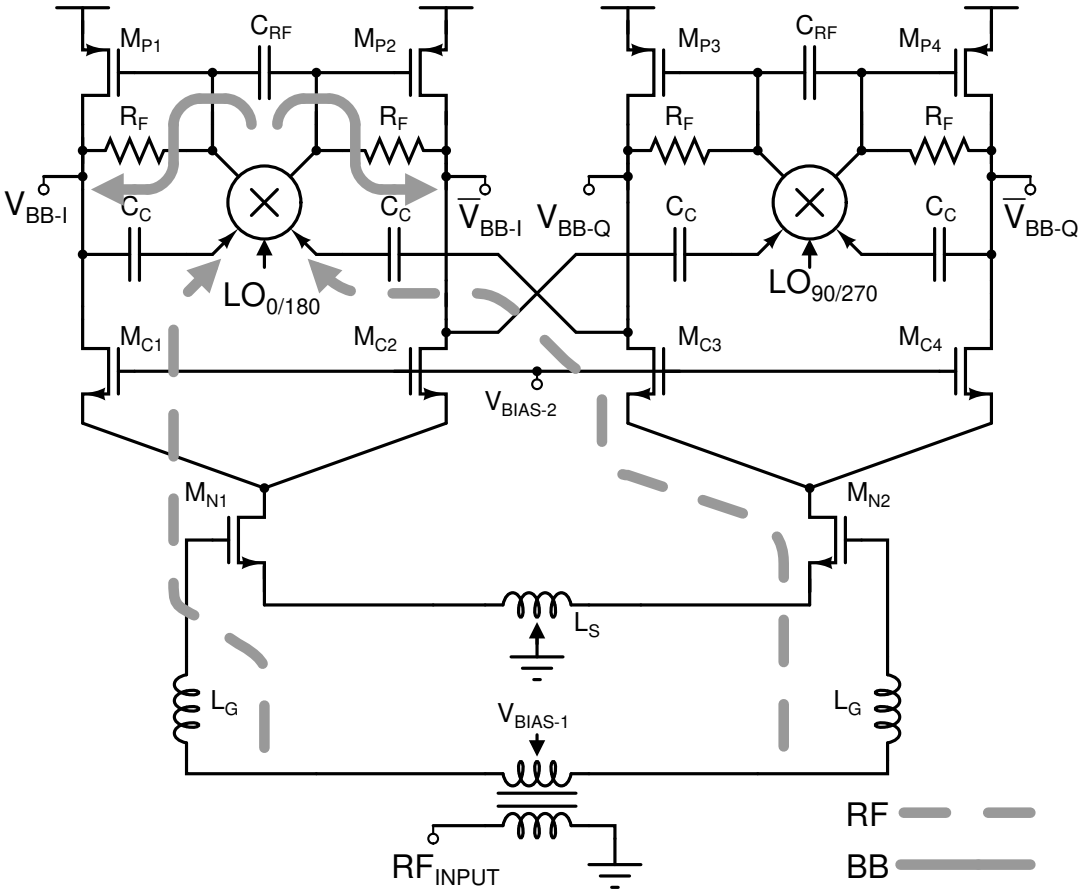


Figure 4.4: Proposed single-stage receiver implementation.

To improve the noise performance and improve the IQ isolation, we propose a new topology where the input trans-conductor's baseband noise path is nullified by making it a common-mode noise at the baseband output (Fig. 4.4). Now, the cascode devices' noise appears at the baseband output. However, the cascode devices' size and bias can be easily optimized to minimize the noise added by it without changing the receiver gain. Furthermore, while the signal transfer function is the same in all the considered IQ implementations (to a first-order approximation), we show in the next section that the output noise is reduced in the implementation of Fig. 4.4. Hence, this topology not only improves noise performance but also allows for more straightforward optimization. When compared to Implementation - 3, we note that in the proposed implementation, the baseband outputs are isolated without any direct path for interference, improving IQ isolation.

Finally, we note that the parasitic capacitances added by the MOSFETs significantly degrade the performance at mmWave frequencies. Due to the lower mobility of holes in PMOS devices, the trans-impedance amplifier devices will need to be sized larger than

the NMOS cascode devices. This would result in the RF current at the baseband output node being shunted to ground through the parasitic capacitances instead of flowing into the passive current-mode mixer. This issue is alleviated by adding a series inductor to present a higher impedance at RF frequencies (Fig. 4.5).

4.2 Circuit Analysis

Estimation of the gain and dominant noise contributions in the circuit are presented here. For the purpose of analysis, only the gate-source capacitance of $M_{N\text{-}1,2}$ and $M_{P\text{-}1,2,3,4}$ are considered. The input matching condition $R_S = \omega_T \times L_S$ is assumed to be satisfied. Analysis for the in-phase and quadrature-phases are identical, and hence the subscripts I and Q are dropped.

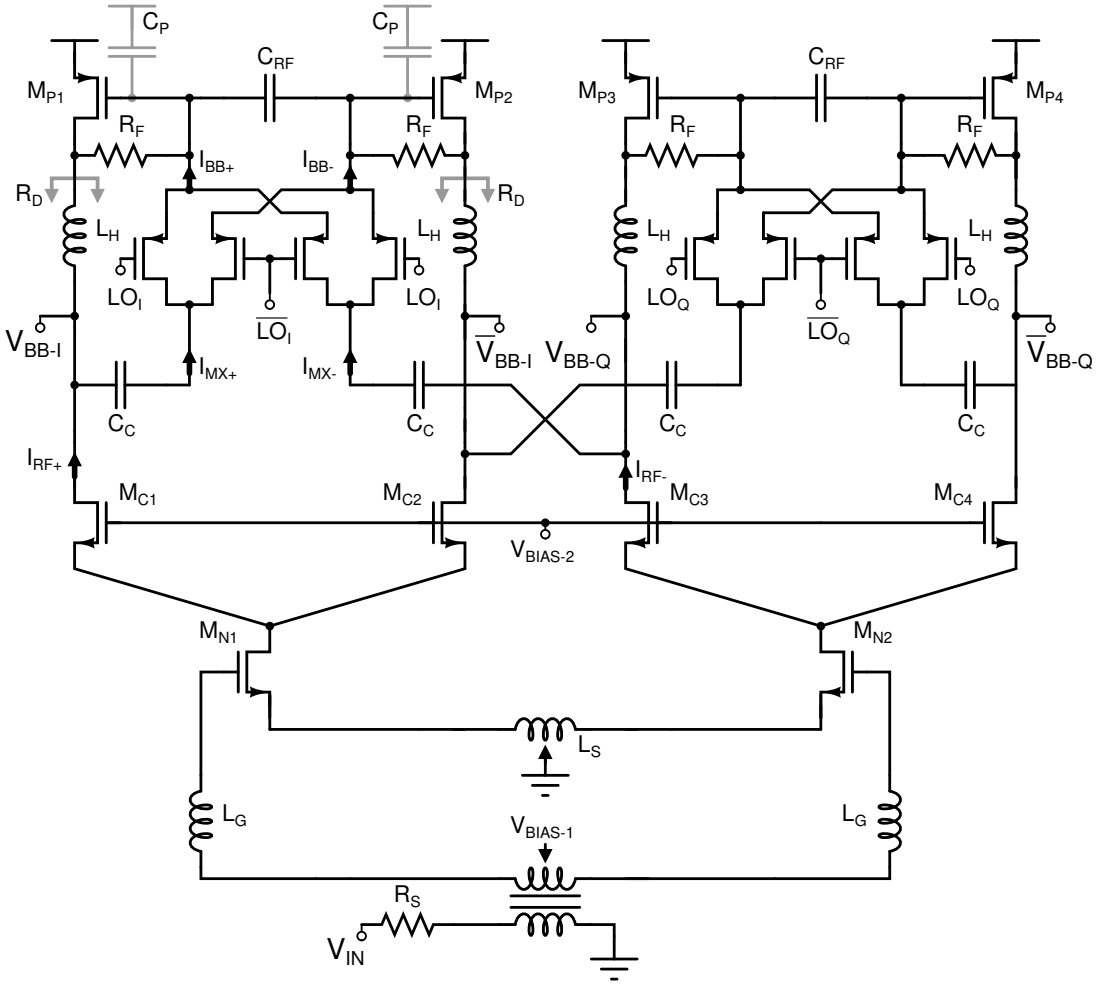


Figure 4.5: Schematic diagram of the proposed single-stage receiver.

4.2.1 Gain Analysis

Traversing the signal flow path, the LNA first amplifies the input RF signal into an RF current. Its trans-conductance gain is

$$\frac{I_{RF}^{+} - I_{RF}^{-}}{V_{IN}} = \underbrace{\sqrt{2}}_{\text{Balun}} \times \underbrace{Q}_{\substack{\text{Input} \\ \text{Matching}}} \underbrace{\left(\frac{g_{MN}}{2}\right)}_{\text{Trans-conductor}} \tag{4.1}$$

with terms corresponding to the balun, input matching and input trans-conductor respectively. This current then gets divided between the high impedance looking into the inductor L_H and the input impedance of the mixer. Assuming the capacitor C_{RF} to be a short circuit, the differential impedance looking into the inductor is

$$Z_{L,RF}(j\omega) = 2 \times (j\omega L_H + (R_F \parallel r_{o-P})) \tag{4.2}$$

while the differential impedance looking into the mixer at frequency $(\omega + k\omega_{LO})$ near $k\omega_{LO}$ is

$$Z_{IN,MZ}(\omega + k\omega_{LO}) = \left(\frac{8}{\pi^2 k^2}\right) \times Z_{TIA}(j\omega) \quad \forall \text{ Odd } k \tag{4.3}$$

which is proportional to the up-converted low baseband input impedance of the trans-impedance amplifier,

$$Z_{TIA}(j\omega) \approx \left(\frac{R_D + R_F}{1 + g_{MP}R_D}\right)\left(\frac{1}{1 + j\omega/\omega_{BW}}\right) \tag{4.4}$$

where the baseband bandwidth is

$$\omega_{BW} \approx \frac{1 + g_{MP}R_D}{(R_D + R_F) \times (C_P + 2C_{RF})} \approx \frac{g_{MP}}{C_P + 2C_{RF}} \tag{4.5}$$

This RF current that flows into the mixer is then down-converted, with a current transfer function from an input at frequency $(\omega + k\omega_{LO})$ near $k\omega_{LO}$ to an output at frequency ω given by

$$\frac{(I_{BB}^{+} - I_{BB}^{-})\,|_{\omega}}{(I_{MX}^{+} - I_{MX}^{-})|_{\omega+k\omega}} = \frac{2}{\pi k} \quad \forall \text{ Odd } k \tag{4.6}$$

Now, this baseband current is converted to the output voltage by the trans-impedance amplifier with a trans-impedance gain of

$$R_{TIA} \approx \left(\frac{(g_{MP} R_F - 1) \times R_D}{1 + g_{MP} R_D} \right) \left(\frac{1}{1 + j\omega/\omega_{BW}} \right) \approx \frac{R_F}{1 + j\omega/\omega_{BW}} \tag{4.7}$$

The trans-impedance amplifier also embeds first-order filtering, which can be tuned by changing ω_{BW}.

The total conversion gain of the receiver is

$$\frac{V_{BB}^{+} - V_{BB}^{-}}{V_{IN}} \approx \frac{\sqrt{2} \times Q}{\pi} \frac{g_{MN} R_F}{1 + j\omega/\omega_{BW}} \tag{4.8}$$

4.2.2 Noise Analysis

Only the noise contribution of the active MOSFETs is considered here for analysis and comparison. There are multiple pathways in which device noise can interfere with the signal, and these are analyzed individually. The single-stage receiver can be unrolled into its multi-stage receiver counterpart in Fig. 3.1 to see how different noise sources affect the signal. We consider 3 different pathways: direct RF noise, folded RF noise, and baseband noise.

The noise analysis compares the proposed single-stage receiver with other potential single-stage receiver implementations (Implementation 2 and 3). Hence, the noise due to the trans-impedance amplifier and the mixer, which are common in the described implementations, are not presented here.

While the standard sizing of $g_{MC} = \frac{g_{MN}}{2}$ results in approximately the same noise figure in all the implementations, we show that by suitably optimizing the trans-conductance, the noise figure of the proposed implementation can be further improved. The subscript n is used to denote the single-sided noise power spectral density. A number after the subscript n denotes the corresponding implementation identifier, while the letter p denotes the proposed implementation.

Direct RF Noise

We denote the noise added directly onto the RF signal at the frequency band of interest as direct RF noise. This is equivalent to the noise added by the LNA in a multi-stage implementation. Hence, in the optimized implementation, this is the in-band RF noise added by the input trans-conductor and cascode devices.

In Implementation - 2 (Fig 4.2), MOSFETs $M_{N\text{-}1,2}$ are split into two MOSFETs, which result in two independent noise sources, giving an in-band noise current of

$$\begin{aligned}\left(I_{RF}^{+}-I_{RF}^{-}\right)_{n|2} &= \underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma\frac{g_{MN}}{2}}_{\text{Split MOSFET}} \times \underbrace{\left(\overbrace{\frac{9}{16}}^{\text{M1-1}}+\overbrace{\frac{1}{16}}^{\text{M1-2}}\right)}_{\substack{\text{Source}\\ \text{Degeneration}}} \\ &= 4\mathrm{k_B T}\gamma g_{MN}\times\frac{5}{8}.\end{aligned} \tag{4.9}$$

In Implementation - 3 and the proposed implementation, the noise of MOSFET $M_{N\text{-}1,2}$ is from a single independent noise source, which then gets divided into two paths, giving a 3dB reduction in noise. The source degeneration further gives an additional reduction in the noise.

$$\begin{aligned}\left(I_{RF}^{+}-I_{RF}^{-}\right)_{n|3,p} &= \underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma g_{MN}}_{\text{Single MOSFET}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Current}\\ \text{Division}}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Source}\\ \text{Degeneration}}} \\ &= 4\mathrm{k_B T}\gamma g_{MN}\times\frac{1}{8}.\end{aligned} \tag{4.10}$$

However, Implementation - 2 does not have the noise of the cascode devices in the RF path. For Implementation - 3 and the proposed implementation, the noise due to the cascode devices can be shown to be

$$\begin{aligned}\left(I_{RF}^{+}-I_{RF}^{-}\right)_{n|3,p} &= \underbrace{4}_{\text{4 Devices}} \times \underbrace{4\mathrm{k_B T}\gamma g_{MC}}_{\text{Cascode Noise}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Current}\\ \text{Division}}} \\ &= 4\mathrm{k_B T}\gamma g_{MC}.\end{aligned} \tag{4.11}$$

Folded RF Noise

The mixer folds noise from higher harmonics into the signal band. However, the mixer gain from higher harmonics to the output baseband frequency decreases with an increase in the harmonic number, as described in (4.6). The degeneration by $\mathrm{L_S}$, results in different noise densities for each harmonic.

For Implementation - 3 and in the proposed implementation, the RF noise density at the output of the LNA at frequency $k\omega_{LO}$ is

$$\begin{aligned}\left(I_{RF}^{+}-I_{RF}^{-}\right)_{n|3,p}|_{k\omega_{LO}} = &\underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma g_{MN}}_{\text{Single MOSFET}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Current}\\ \text{Division}}} \\ &\times \underbrace{\frac{(1-k^2)^2+k^2\beta^2}{(1-k^2)^2+4k^2\beta^2}}_{\substack{\text{Source}\\ \text{Degeneration}}} \qquad \forall \text{ Odd } k\end{aligned} \tag{4.12}$$

where

$$\beta = \left(\frac{\omega_T}{\omega_{LO}}\right)\left(\frac{L_S}{L_S+L_G}\right) \tag{4.13}$$

For the Implementation - 2, the noise spectral density can be shown to be

$$\begin{aligned}\left(I_{RF}^{+}-I_{RF}^{-}\right)_{n|2}|_{k\omega_{LO}} = &\underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma\frac{g_{MN}}{2}}_{\text{Split MOSFET}} \\ &\times \underbrace{\frac{(1-k^2)^2+(5/2)k^2\beta^2}{(1-k^2)^2+4k^2\beta^2}}_{\substack{\text{Source}\\ \text{Degeneration}}} \qquad \forall \text{ Odd } k\end{aligned} \tag{4.14}$$

(4.9) and (4.10) are a special case of the above equations. The addition of the

cascode noise at higher frequencies is the same as (4.11) for Implementation - 3 and the proposed implementation.

Baseband Noise

The input signal after down-conversion flows through the trans-impedance amplifier, which is also a part of the single-stage receiver. Hence, the baseband noise of the devices also adds to the total output noise of the receiver. We note that C_{RF} and C_C are designed to behave as an open circuit for baseband frequencies, presenting a low impedance looking into L_D and preventing baseband signal or noise from flowing into the mixer respectively.

For Implementation - 2, the noise due to the input trans-conductor will be

$$\begin{aligned}\left(V_{BB}^{+}-V_{BB}^{-}\right)_{n|2} &= \underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma\frac{g_{MN}}{2}}_{\text{Split MOSFET}} \times \underbrace{\left(\frac{1}{g_{MP}}\right)^2}_{\substack{\text{Diode}\\ \text{Connection}}} \\ &= 4\mathrm{k_B T}\gamma g_{MN} \times \left(\frac{1}{g_{MP}}\right)^2\end{aligned} \tag{4.15}$$

Implementation - 3, which does not have a split MOSFET, also has baseband noise from the input trans-conductor.

$$\begin{aligned}\left(V_{BB}^{+}-V_{BB}^{-}\right)_{n|3} &= \underbrace{2}_{\text{Differential}} \times \underbrace{4\mathrm{k_B T}\gamma g_{MN}}_{\text{Single MOSFET}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Current}\\ \text{Division}}} \times \underbrace{\left(\frac{1}{g_{MP}}\right)^2}_{\substack{\text{Diode}\\ \text{Connection}}} \\ &= 2\mathrm{k_B T}\gamma g_{MN} \times \left(\frac{1}{g_{MP}}\right)^2\end{aligned} \tag{4.16}$$

This noise appears as common-mode noise for the proposed receiver, and hence does not appear at the differential baseband output.

However, both Implementation - 3 and the proposed implementation suffer from the noise of the cascode devices.

$$\begin{aligned}\left(V_{BB}^{+}-V_{BB}^{-}\right)_{n|3} &= \underbrace{4}_{\text{4 Devices}} \times \underbrace{4\text{k}_\text{B}\text{T}\gamma g_{MC}}_{\text{Cascode MOSFET}} \times \underbrace{\frac{1}{4}}_{\substack{\text{Current}\\\text{Division}}} \times \underbrace{\left(\frac{1}{g_{MP}}\right)^2}_{\substack{\text{Diode}\\\text{Connection}}} \\ &= 4\text{k}_\text{B}\text{T}\gamma g_{MC} \times \left(\frac{1}{g_{MP}}\right)^2.\end{aligned} \tag{4.17}$$

$$\begin{aligned}\left(V_{BB}^{+}-V_{BB}^{-}\right)_{n|p} &= \underbrace{2}_{\text{Differential}} \times \underbrace{4\text{k}_\text{B}\text{T}\gamma g_{MP}}_{\text{Cascode MOSFET}} \times \underbrace{\left(\frac{1}{g_{MP}}\right)^2}_{\substack{\text{Diode}\\\text{Connection}}} \\ &= 8\text{k}_\text{B}\text{T}\gamma g_{MC} \times \left(\frac{1}{g_{MP}}\right)^2.\end{aligned} \tag{4.18}$$

Summary

Let $g_{MC} = \alpha \times \frac{g_{MN}}{2}$, where $\alpha = 1$ is the conventional sizing of the cascode device with respect to the input trans-conductor considering equal current densities. In Table 4.1, RF current noise is normalized to $4\text{k}_\text{B}\text{T}\gamma g_{MN}$, while baseband voltage noise is normalized to $4\text{k}_\text{B}\text{T}\gamma g_{MN} \times \left(\frac{1}{g_{MP}}\right)^2$. Assuming β defined in (4.13) is large, the folded RF noise will follow the same relations as RF noise.

Table 4.1: Noise performance summary of various single-stage receiver implementations.

Noise Source		I - 2	I - 3	Proposed
RF	Trans-conductor	$5/8$	$1/8$	$1/8$
	Cascode	-	$\alpha/2$	$\alpha/2$
Baseband	Trans-conductor	1	$1/2$	-
	Cascode	-	$\alpha/2$	α

We note that for $\alpha = 1$, Implementation - 2, Implementation - 3 and the proposed implementation all have the same noise performance. However, choosing a smaller value of α results in the proposed implementation having the best noise performance. We also note that reducing α by modifying g_{MC} improves noise without affecting the gain (to a first-order), allowing for straightforward optimization.

4.2.3 Linearity Considerations

The single-stage receiver topology implements current reuse without the stacking of stages, alleviating voltage headroom issues. However, the presence of 3 MOSFETs in the stack limits the topology's performance with scaling in the supply voltage.

Assuming a large gain, the linearity of this topology is limited by the biasing of the cascode MOSFETs. The drain of the cascode device, which is the baseband output node, is biased by the diode-connected PMOS of the trans-impedance amplifier. There is flexibility in choosing the gate voltage of the cascode device.

From the previous section, we note that a lower g_{MC} improves noise performance. This can be achieved by increasing the overdrive of the cascode MOSFETs, resulting in a larger gate voltage of the cascode device. However, this will push the cascode device closer into the linear region, worsening the linearity performance.

This trade-off between noise and linearity can be optimized by changing the cascode gate bias voltage to get optimal performance for different receiver input signal levels.

4.3 Potential Adaptations of the Proposed Topology

4.3.1 Integration with the proposed Phase-Shifting scheme

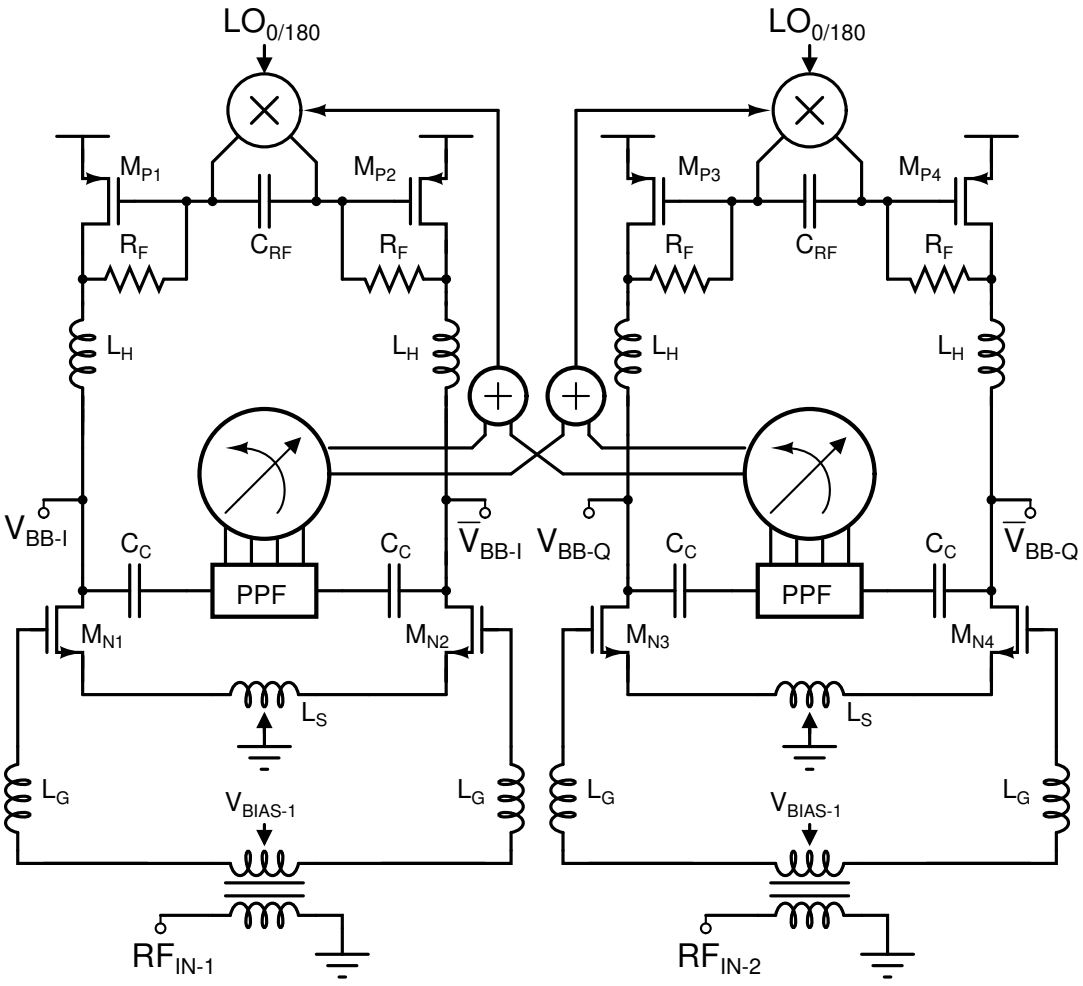


Figure 4.6: 2-Channel implementation of the proposed phase-shifting architecture using the single-stage receiver topology.

Fig. 4.6 depicts a 2-channel phased-array implementation using the proposed integrated phase-shifting scheme and the single-stage topology. We note that in the single-channel implementation, inductors L_H were the components that dominated the area. The 2-channel implementation, which still has the same number of L_H inductors, has only a moderate area increase compared to the single-channel implementation, substantiating the area-effectiveness of this implementation.

4.3.2 Adaptations for other Technologies/Operating Frequencies

In direct-conversion receivers implemented using the conventional single-stage topology, flicker noise is a significant concern as the input trans-conductor MOSFET's baseband noise also appears at the output [9, 10]. The proposed implementation effectively nullifies the baseband contribution of noise from the input trans-conductor, while allowing the cascode device to add baseband noise. This can be exploited to reduce flicker noise. Improving noise by reducing g_{MC} requires the cascode device to have larger overdrive voltages. In newer technologies with higher transit frequencies or systems with lower operating frequencies, this can also be achieved by increasing the cascode device's length without significant degradation of performance. This decouples the noise optimization between the RF and baseband paths. The input trans-conductor can have minimum length devices, improving the RF noise performance, and the cascode devices can have larger lengths, improving the baseband noise performance.

CHAPTER 5

OPTIMIZED SINGLE-STAGE RECEIVER IMPLEMENTATION DETAILS

To validate the working of the optimized single-stage receiver topology, we have designed and taped-out a 28GHz single-channel receiver on 65nm bulk CMOS process. The primary design considerations and details are presented in this chapter, while the next chapter presents the measured results.

5.1 Technology Considerations

We have used commercially available GP flavor of the 65nm bulk CMOS process from TSMC for our design. It can support a supply voltage of 1.2V, has one poly layer, nine copper metal routing layers, and one aluminium redistribution layer. While the process design kit (PDK) has a separate set of RF components for active and passive devices, careful layout considerations were given for the actives, and EM simulations using EMX were run to validate the performance of passives at mmWave frequencies.

One of the challenges in mmWave designs is the rapid deterioration of performance in a poorly designed layout. For mmWave designs, the extracted layout simulation results can be potentially very different compared to the schematic results, adding to the complexity of the design. Several layout techniques suitable for mmWave designs have been documented in literature [13] to get the optimal performance from the process. The problem of discrepancy between layout and schematic is usually resolved through iterations, manual parameter modeling, or by using characterized cells.

To see the degradation from schematic to layout, the transit frequency is plotted from the schematic and extracted layout simulations for different MOSFETs from the PDK. Here, the base PDK layout without any additional routing is used for the extracted layout simulation. As seen in Fig. 5.1, the F_T of the baseband device can vary by as much as 20% by just running an extracted layout simulation with the base layout. We

note that in schematic simulations, the baseband MOSFETs have better F_T than RF MOSFETs, but this relation is reversed in the extracted layout simulation. However, the RF MOSFETS were well characterized in the process, as the schematic and extracted base layout simulations exactly match.

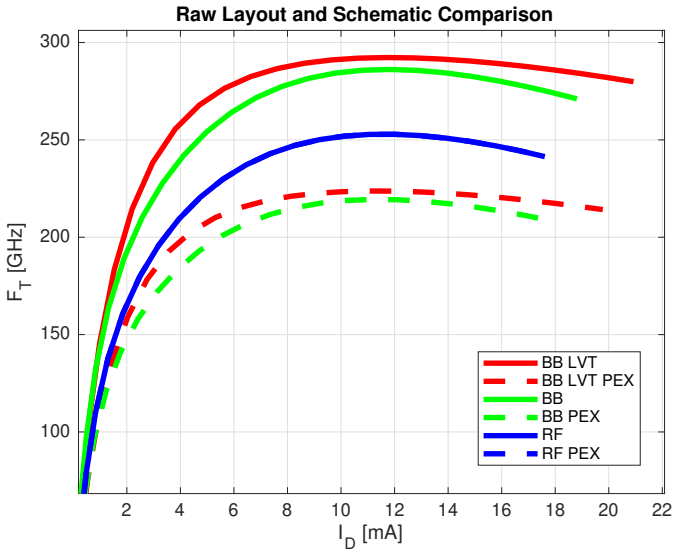


Figure 5.1: F_T comparison for the extracted base layout and schematic.

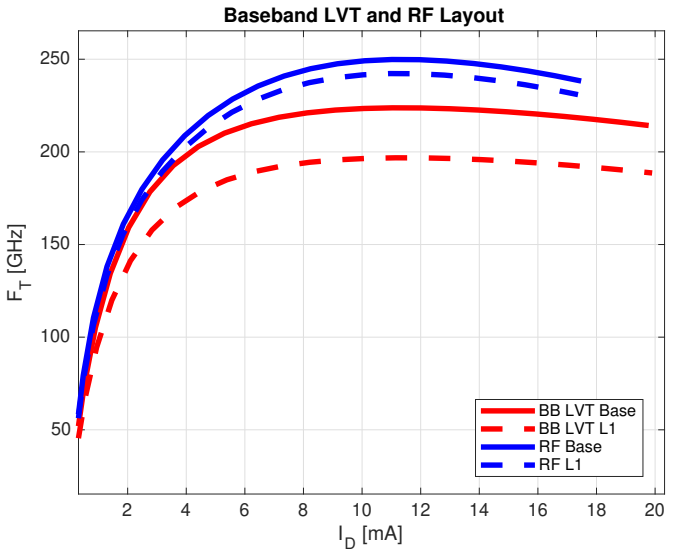


Figure 5.2: F_T comparison for the extracted base layout and layout routed to higher metal layers.

The extracted layout performance of different MOSFETs from the PDK was compared to get the optimal performance from the process. All of the layouts were routed to the same metal layer, with different layout styles optimizing between routing resistance and capacitance. Simulation results showed that the RF MOSFETs without the deep-nwell (DNW) had the highest transit frequency (Fig. 5.2). We note that the base

layout of the RF MOSFETs in the PDK is routed to higher metal layers and characterized. Simulation results show only a nominal degradation in performance after further routing. Hence, the schematic of RF MOSFETs in the chosen process was directly used for mmWave designs without extra modeling or characterization.

5.2 Receiver Considerations

The single-stage receiver contains the LNA, mixer, and filter of a standard implementation all sharing the same bias current. Hence, the design and optimization of this receiver topology involved ensuring that each component of the receiver was properly biased and functioning according to specifications.

An inductively degenerated common-source stage with a balun and a center-tapped source inductor was used for the input matching circuit. The inductor to resonate out the gate capacitance was realized through the routing lines. To improve the gain and noise performance, a secondary-tapped balun was used to bias the input of the LNA, as opposed to using an AC coupling capacitor and biasing resistor.

The LNA and trans-impedance amplifier were designed to meet the gain and bandwidth specifications, as described in equation (4.8) and Section 4.2.2. The cascode devices were designed for a balance between linearity and noise, as discussed in Section 4.2.3. The passive current-mode mixer was biased close to the supply voltage, resulting in PMOS switching device performing better than an NMOS device.

The layout was designed so that there was symmetry between the differential sections of the circuit as well as the IQ sections to reduce the effects of mismatch.

5.3 Peripheral Circuitry

On-chip 28GHz LO buffers were designed to drive the mixer switches. Single-ended LO input signals were assumed as inputs, and an on-chip balun was used to get differential signals.

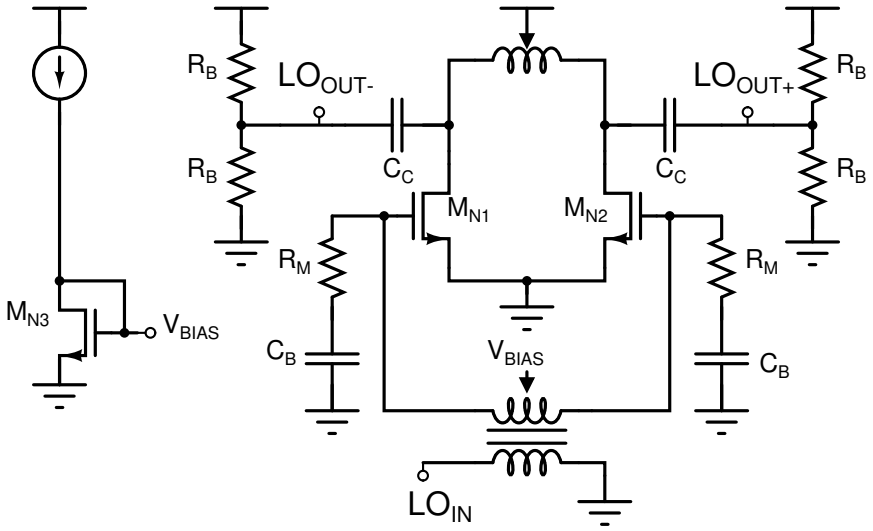


Figure 5.3: LO Buffer implementation.

The output of the receiver was supplemented by an output buffer to drive the 50Ω load. This was implemented as a standard 2-stage opamp in a voltage follower configuration. The large-sized MOSFETs in the second-stage required for driving the resistive load led to a larger capacitance at the input of the second stage. This compensated the opamp without the need for any compensation technique.

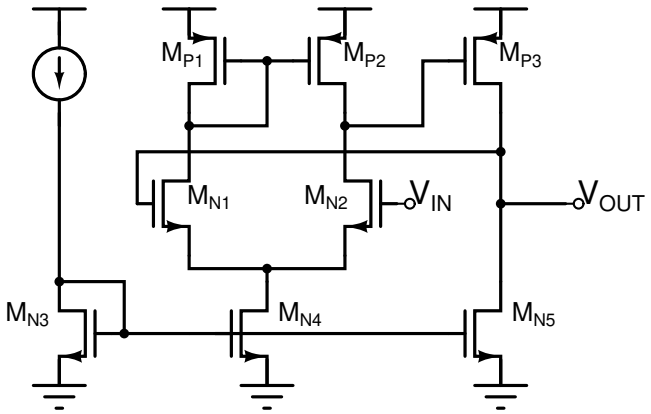


Figure 5.4: Output Driver implementation.

Three supply domains were created, one each for the receiver, LO buffer, and output driver. Each domain had its own decoupling capacitance to ensure a steady supply

voltage. The bond-pads were chosen to isolate the three supply lines, but share the ground across the domains. The bond-pads in the PDK provided ESD protection.

5.4 mmWave Layout Considerations

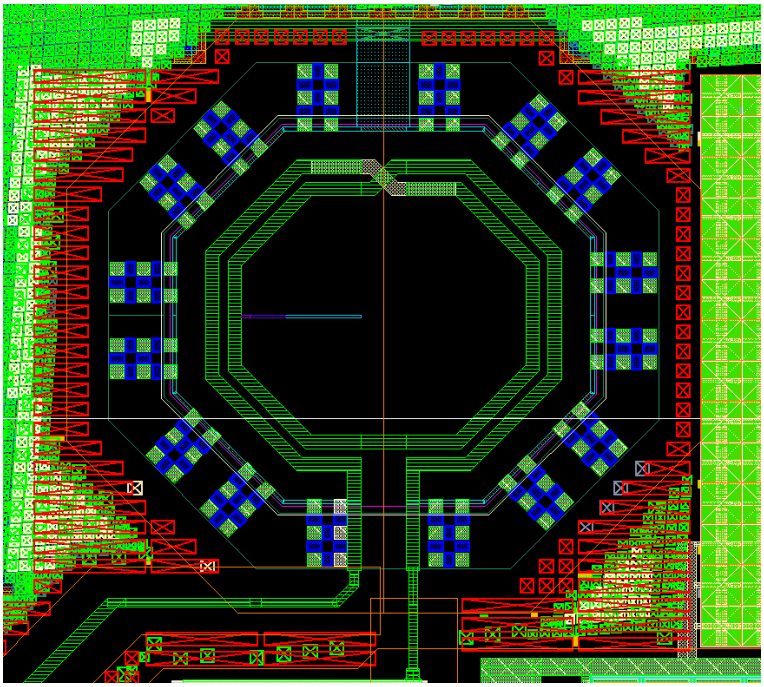


Figure 5.5: Inductor layout with ground ring and manual dummy placement.

mmWave layouts require careful floorplanning to ensure maximum isolation between components and proper grounding. All RF elements were encased in ground boxes to improve isolation between them. The process supported 45° bends, and they were used for all RF lines.

Manual dummy placement was done for diffusion and poly layers near inductors to meet the density requirements. Dummy exclusion layers were drawn over RF components with sufficient clearance.

Care was taken to ensure minimal overlap between RF lines and proper segmentation between actives and passive for EM simulation and parasitic extraction. The supply and ground lines were carefully simulated to ensure that any line inductance does not deteriorate the performance.

5.5 Testing Considerations

A chip-on-board solution was chosen for testing the chip. The RF and LO inputs were chosen to be supplied by probing, while the power and baseband outputs were to be wire bonded onto the PCB.

A GSG structure was used for the RF input, while a GSGSG structure was used for the 0° and 90° LO signals. An additional open structure was used for de-embedding the probing pads. Low-capacitance probing pads without ESD protection provided by the PDK were used to ensure that the pads do not degrade the performance.

Proper spacing and clearance for probing were considered for the pad floorplanning and layout.

Separate bias currents for the receiver, LO buffer, and output driver were tapped out of the chip to get independent control of the primary and peripheral circuits. The separate supply domains also allowed for independent characterization and debugging of power consumed in the chip.

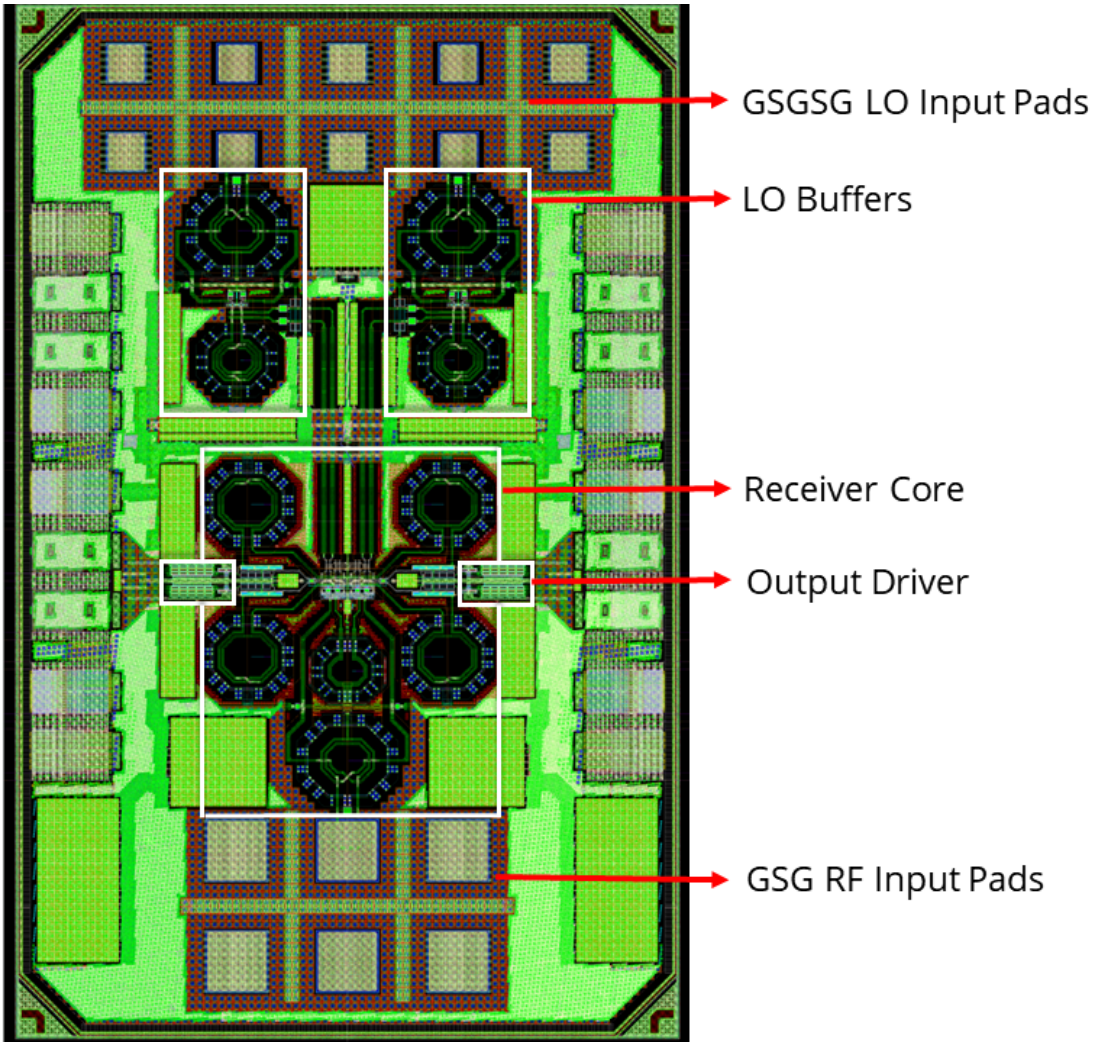


Figure 5.6: Designed layout of the chip.

CHAPTER 6

MEASUREMENT SETUP AND RESULTS

A 28GHz receiver was implemented to validate the performance of the proposed single-stage topology at mmWave 5G frequencies. A 1.4mm×0.9mm die was taped-out and measured using a chip-on-board solution. Chip measurement and characterization are still in progress at the time of writing. This chapter presents the measurement setup and partial measurement results of the implementation.

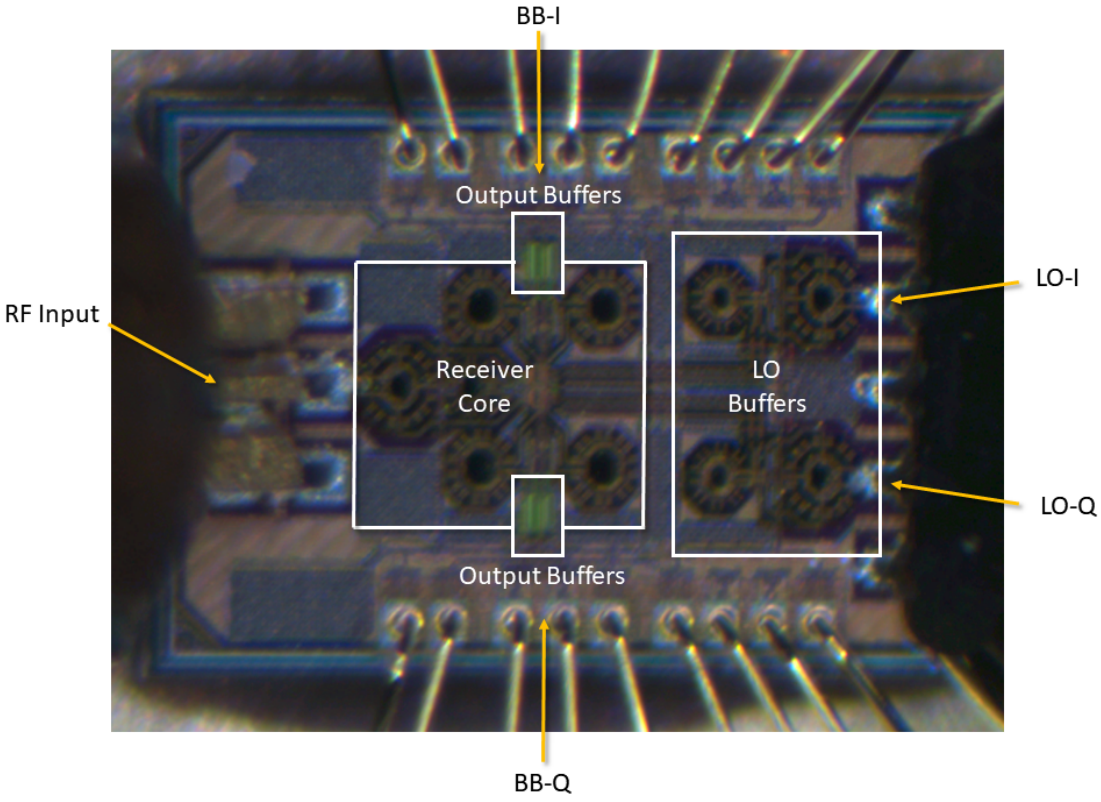


Figure 6.1: Fabricated die photograph.

6.1 Measurement Setup

A PNA-X Vector Network Analyzer was used for making all the measurements. The quadrature LO input signals were supplied through two synchronized PSG Analog Signal Generators. The power supplies and bias current were supplied using Precision Source/Measure Units. The mmWave stimuli (RF and LO signals) were applied to the chip using a Cascade Microtech (now Formfactor) probe station with GSG and GSGSG probes respectively. Differential baseband output signals were converted to single-ended signals using baluns on the PCB and measured using standard 1.85mm connectors. 3-port calibration was done using Keysight's 1.85mm calibration kit and Cascade's Impedance Standard Substrate (ISS).

All the instruments were connected through LAN and operated using SCPI commands sent from MATLAB. MATLAB codes were used to set up and transfer measurements on the VNA, control the signal generator in lockstep with the VNA to sweep the LO frequency, and sweep the bias currents/LO power to get optimal performance.

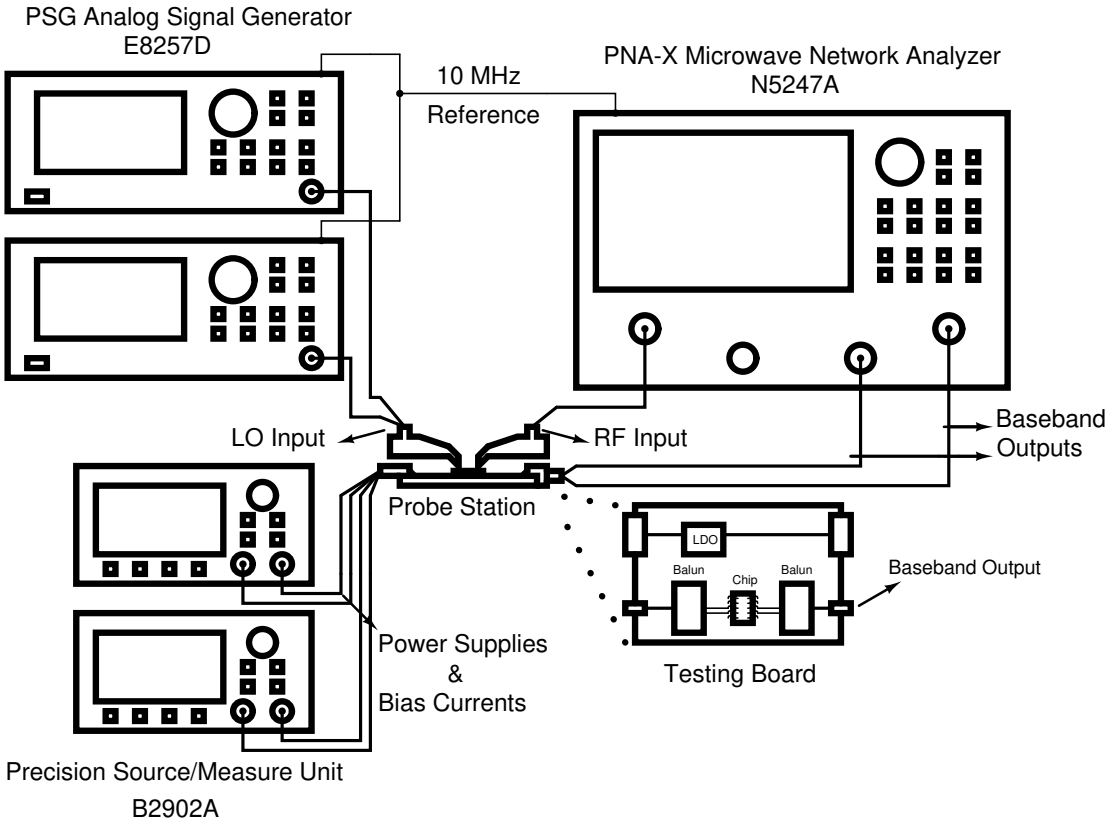
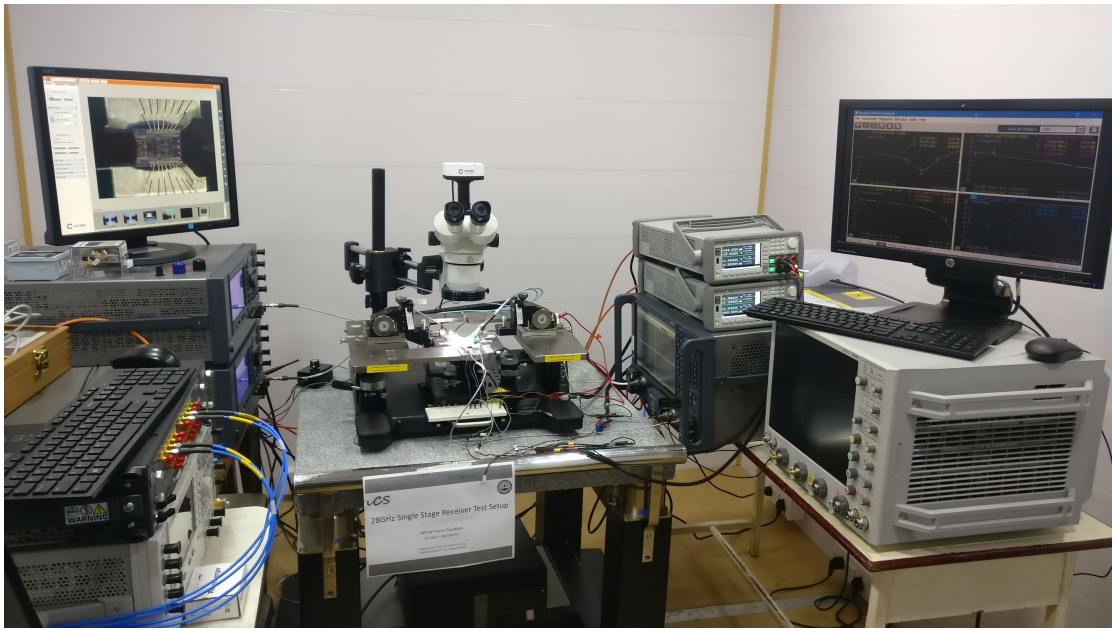
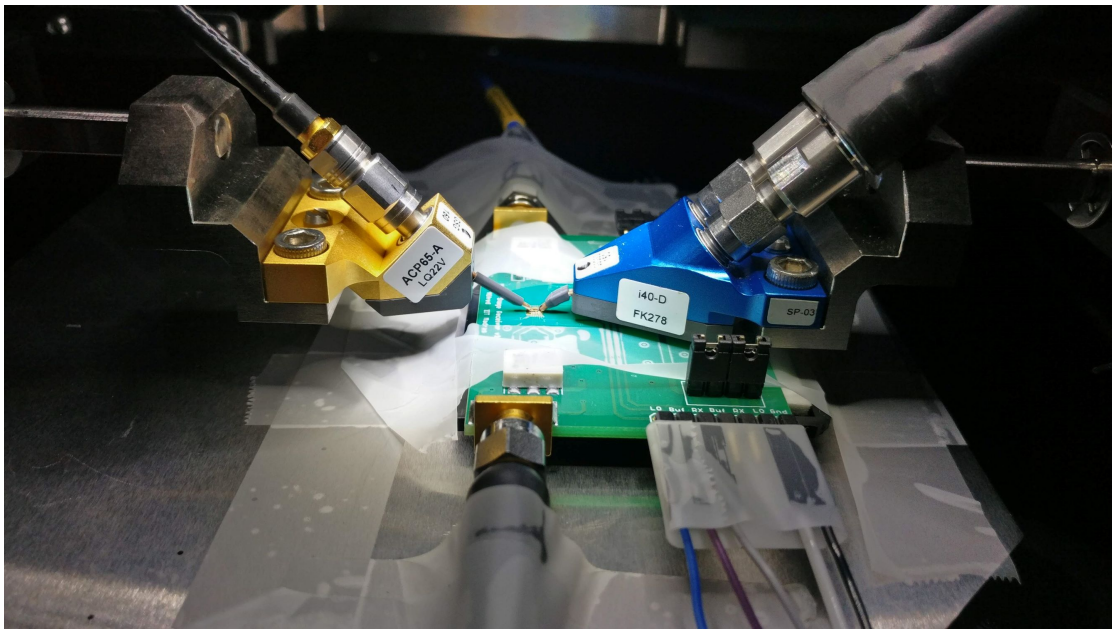


Figure 6.2: Measurement setup.



(a)



(b)

Figure 6.3: Test Setup: (a) Instruments setup; (b) Probing setup

6.2 Simulated and Measured Results

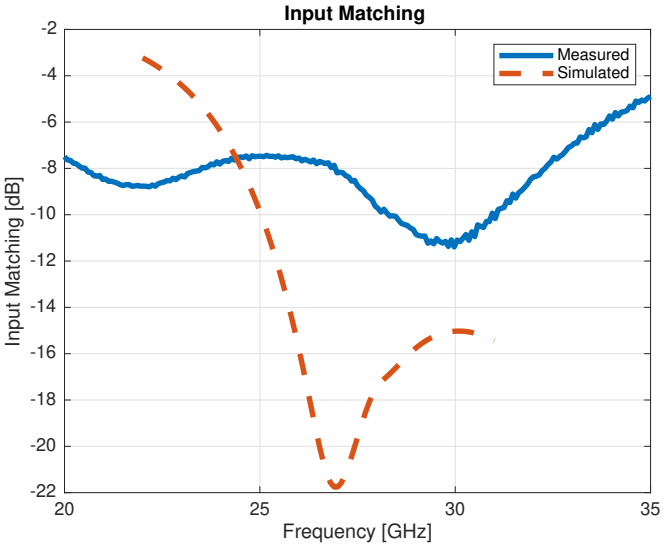
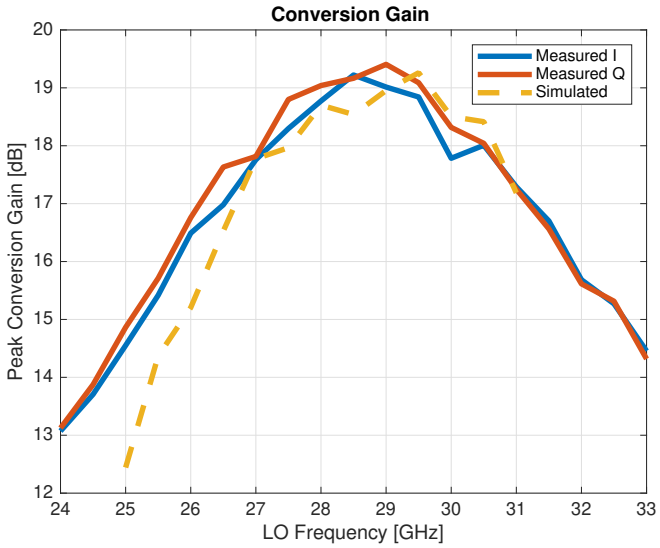
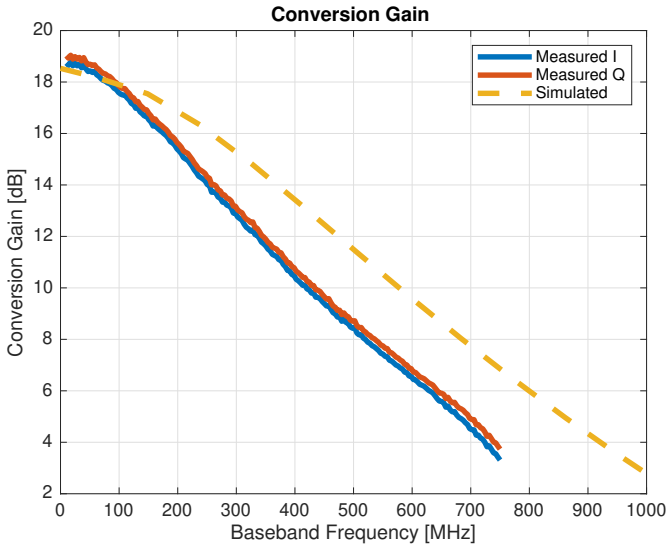


Figure 6.4: Measured S_{11} for F_{LO}=28GHz.

We note that the measured input matching characteristics are significantly different from the simulated value. This is attributed to the degradation of the probing pads as a result of repeated probing and measurements. Once one measurement cycle is properly calibrated and complete, additional chips will be measured to get the actual input matching performance. Even after degradation, S_{11} is still better than -10dB over the frequency range of interest, and hence the other performance parameters are not expected to degrade because of the probing pads.



(a)



(b)

Figure 6.5: Measured Gain: (a) Peak gain for different F_{LO}; (b) F_{LO}=28GHz.

While the measured peak gain in Fig. 6.5a is close to the simulated results, we note that we have not de-embedded the PCB baseband balun, PCB trace loss, and baseband connectors. A correction for this loss will increase the measured gain by 1-2dB. We also note in Fig. 6.5b that the bandwidth of the receiver has reduced.

We attribute this increased peak gain and decreased bandwidth to the process variations in the fabrication. These results are in line with a skewed FS corner die. Additional chip measurements from another lot are needed to confirm this.

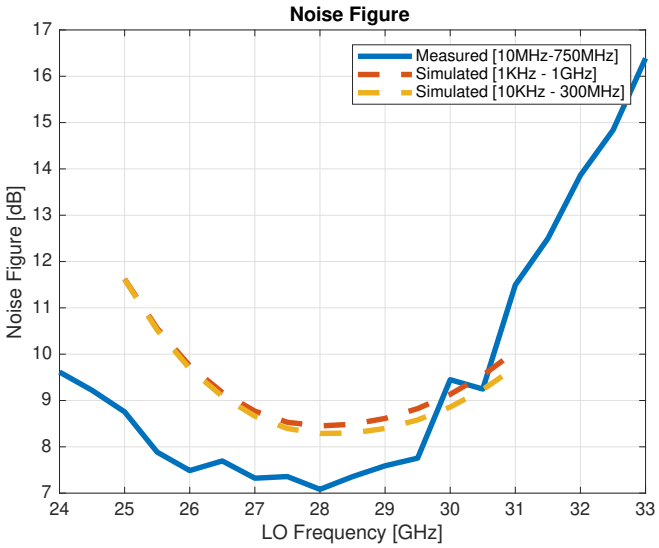


Figure 6.6: Measured noise figure.

The measured noise performance is better than the simulated results. One possible reason is that the degradation of input matching resulted in a more optimal input impedance in the noise circle. The FS corner die also has the best noise figure across all corners, further justifying the chip's process corner.

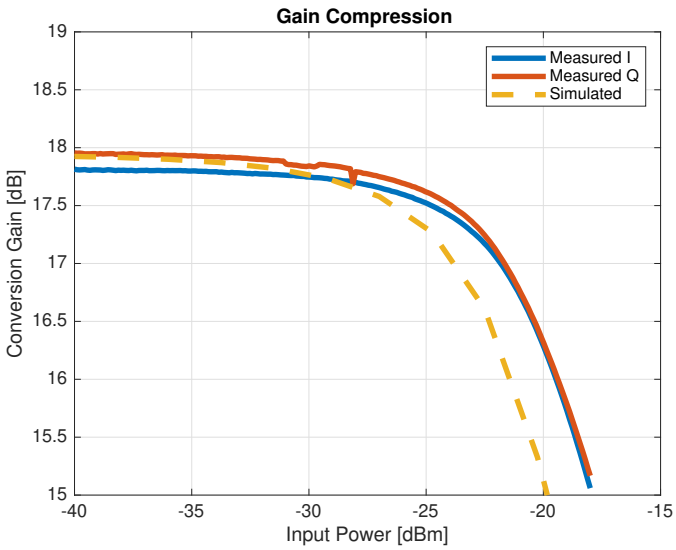
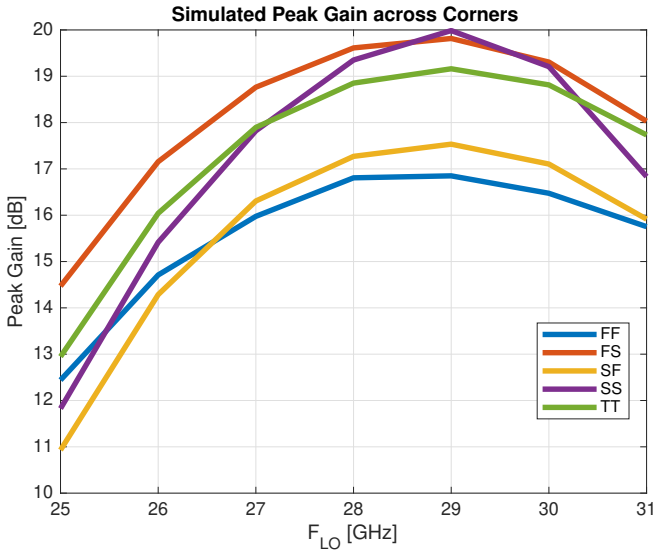
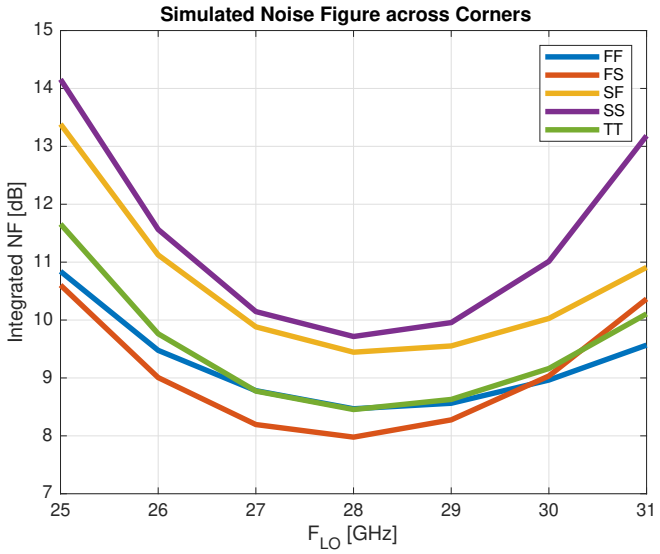


Figure 6.7: Measured Gain compression for F_{LO}=28GHz at 100MHz offset.

The measured input 1-dB compression point of the chip is close to the simulated results.



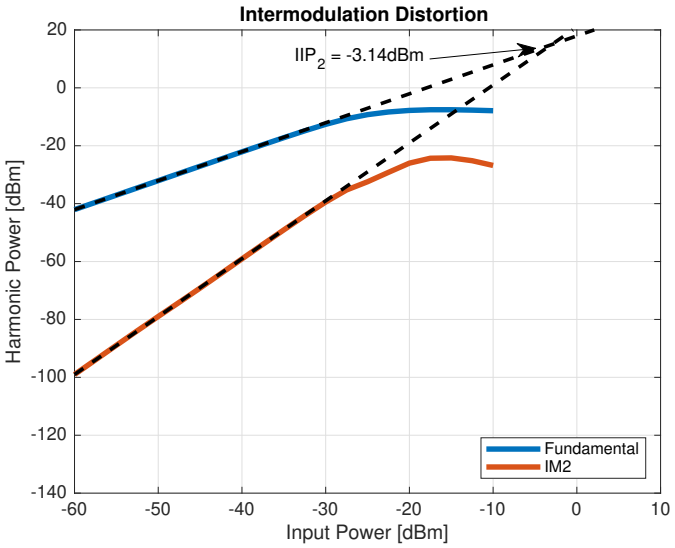
(a)



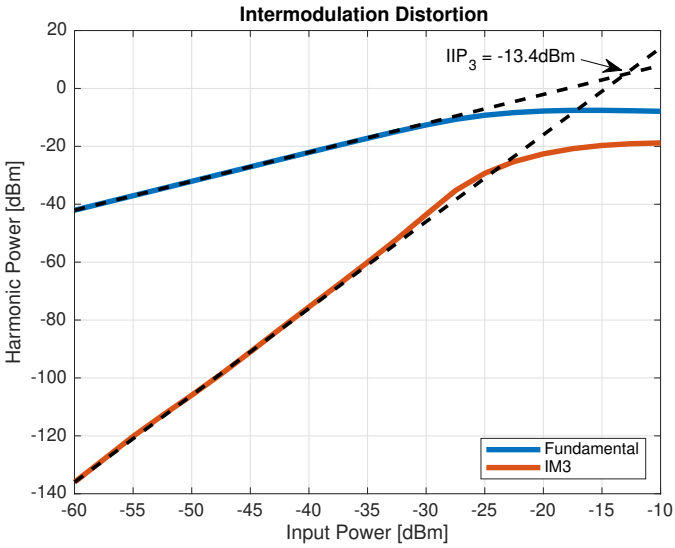
(b)

Figure 6.8: Process variation simulation: (a) Peak gain for different F_{LO}; (b) Noise Figure.

The process corner simulations validate the argument that the chip was fabricated in the FS corner. Simulation results show that a faster corner gives a larger bandwidth and lower gain, while a slower corner gives a higher gain and lower bandwidth. The FS corner gives the optimal balance of gain and bandwidth for noise.



(a)



(b)

Figure 6.9: Simulated linearity performance for F_{LO}=28GHz: (a) IIP_2 at 100MHz and 110MHz offset; (b) IIP_3 at 100MHz and 110MHz offset.

IIP_2 and IIP_3 measurements are yet to be calibrated and measured. Simulated results are presented here.

6.3 Comparison with other Receivers

Table 6.1: Performance comparison with other IQ Receivers

Metric	This Work	[11] LG JSSC '18	[16] CMU JSSC '18
Architecture	Direct Conversion		Heterodyne (IQ Outputs)
Process	65nm CMOS	28nm CMOS	65nm CMOS
Phase-Shifter/VGA	No	Yes	Yes
Tx-Rx Switch	No	Yes	No
Frequency [GHz]	26.5-29.5	25.8-28.0	25-30
Gain [dB]	17.6	30 to 69	34
Noise Figure [dB]	7.8	6.7 to 13.6	7.3
IP_{1dB} [dBm]	-21.5	-68.9 to -34.8	-29 to -21
IIP_2 [dBm]	-3.1*	-	-
IIP_3 [dBm]	-13.4*	-59.9 to -25.8	-
Area [mm^2]	0.18	-	0.32
Power [mW]	11.4*	33.8+	37#+
FoM_1 [dB]	8.7	7.6	-
FoM_2 [dB]	9.7	8.1	9.5

*Simulated +Estimated by excluding LO Circuitry #Estimated by excluding VGA and Combining Amplifiers

$$\text{FoM}_1 = 10 \times \log_{10}\left(\frac{10^{\text{Gain}/20} \times 10^{(\text{IIP}_3-10)/20}}{10^{\text{NF}/10} \times \text{Power[mW]} \times 10^{-3}}\right)$$

$$\text{FoM}_2 = 10 \times \log_{10}\left(\frac{10^{\text{Gain}/20} \times 10^{\text{IP}_{1\text{dB}}/20}}{10^{\text{NF}/10} \times \text{Power[mW]} \times 10^{-3}}\right)$$

We note that the proposed receiver architecture achieves a noise figure comparable to other prior work while consuming much lesser power. Additional gain can be achieved by adding baseband variable gain amplifiers. The proposed IQ receiver front-end occupies a significantly lesser area when compared to other implementations, while also having a better figure of merit (FoM).

CHAPTER 7

CONCLUSION & FUTURE WORK

An integrated phase-shifting scheme and optimized single-stage receiver topology that complements each other to realize area and power optimization goals was presented. The working of the integrated phase-shifting scheme was illustrated. Multiple variants of the single-stage topology were analyzed, and a new improved topology was proposed. A 28GHz receiver implementing the proposed single-stage topology was designed and taped-out to validate its performance.

While this work has shown the potential of the single-stage topology to function at the mmWave 5G spectrum, a design incorporating a phase-shifter in this topology needs to be implemented and validated to create a single RF receive channel required in the 5G phased-array architecture. This needs to be followed with a multi-channel implementation, where the proposed integrated phase-shifting scheme can be validated. Similar designs need to be implemented on the transmitter side, after which the complete RF front-end of a 5G beamforming transceiver IC can be designed.

APPENDIX A

Bonding and Board Details

Bonding Details

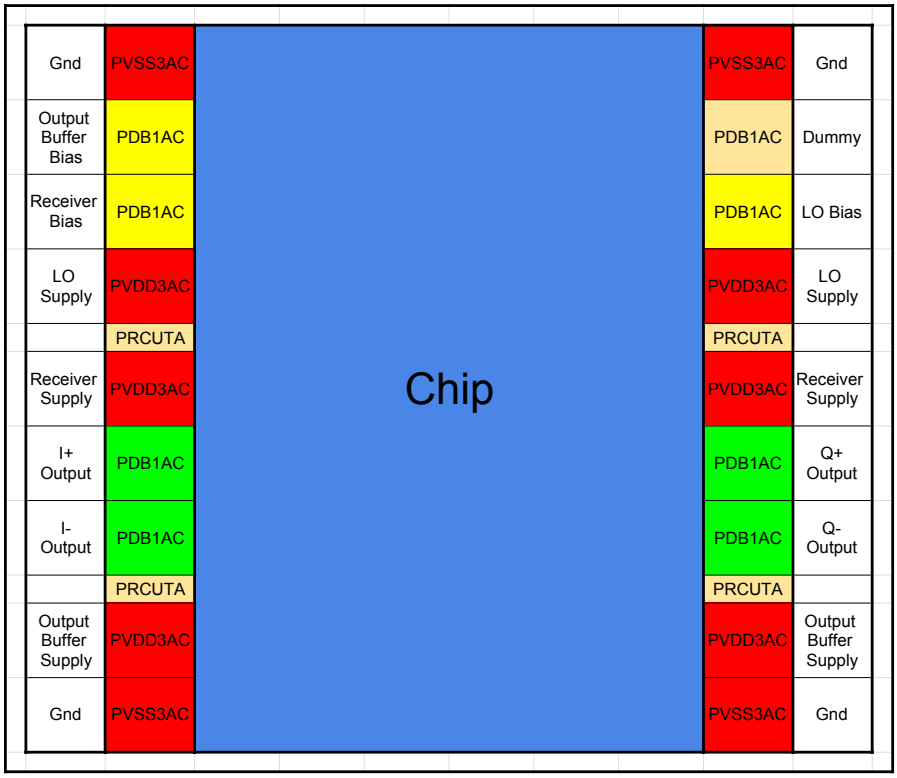


Figure A.1: Chip pinout

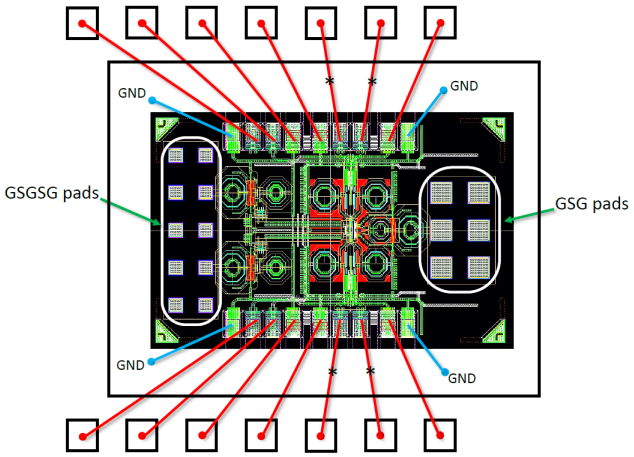
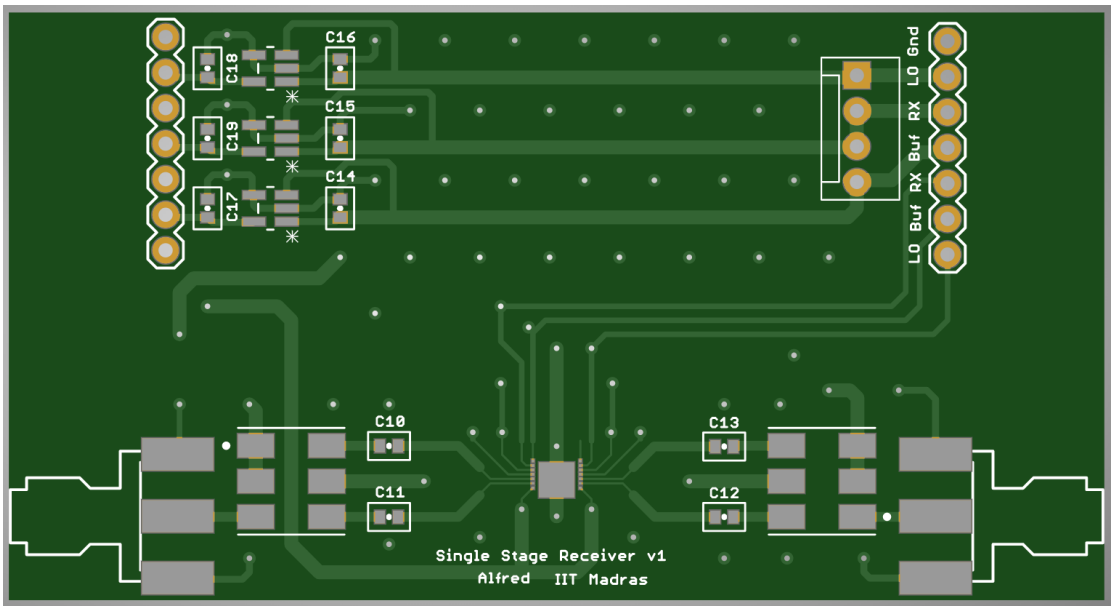
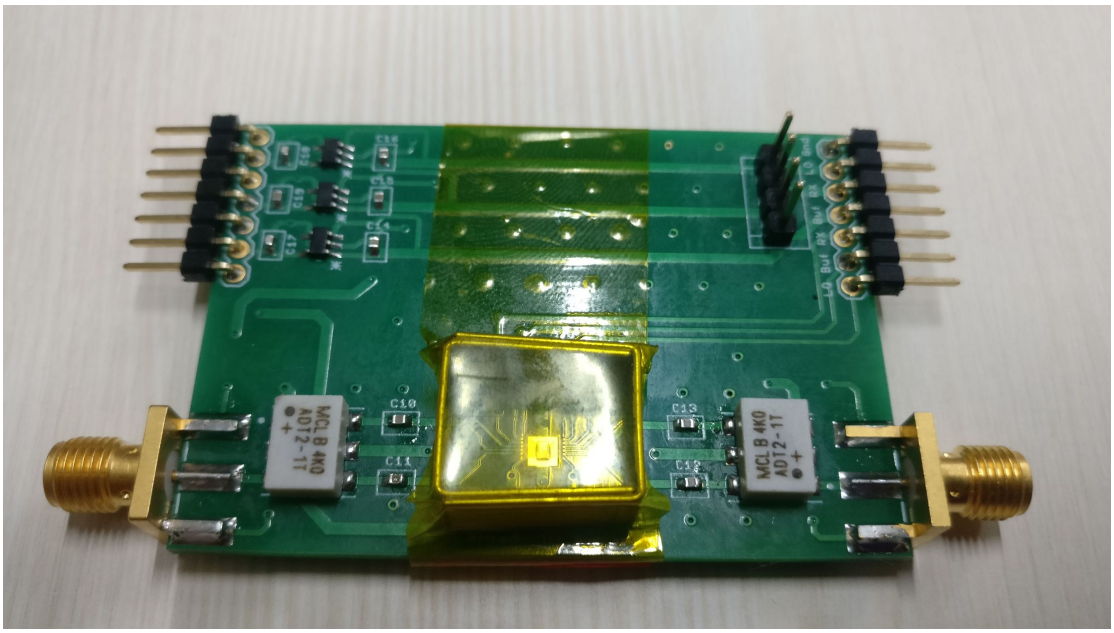


Figure A.2: Chip-on-board bonding plan.

Board Details



(a)



(b)

Figure A.3: Testing Board: (a) Design; (b) Assembled Board

The fabricated 1.4mm×0.9mm die had bond-pads of dimensions $69\mu m \times 57\mu m$. These were used to wire-bond the power supplies and baseband outputs of the receiver to the PCB which had larger pads of dimensions $160\mu m \times 160\mu m$.

A 60mm×42mm PCB was designed for testing the chip. Texas Instruments' TLV700 series LDO was used to generate the 1.2V supply. Minicircuits' ADT2-1T+ balun was used for the baseband output signals.

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