Design and Testing of Wideband RF Transmitter

A THESIS

Submitted by

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(EE15B072)

under the guidance of

Dr. Aniruddhan S.

for the award of

B.Tech. & M.Tech. Degree

in

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2020

Thesis Certificate

This is to certify that the thesis titled **Design and Testing of Wideband RF Transmitter** submitted by **Akshay Sethia** to **Indian Institute of Technology MADRAS** for the award of the degree of **Bachelor of Technology & Master of Technology**, is a bona fide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Place: Chennai

Date: July, 2020

Acknowledgement

I express my sincere gratitude to my project guide Dr. Aniruddhan S. for his constant support during the entire period of my Dual Degree Project. His friendly guidance and enthusiasm kept me motivated at all times.

I also express my gratitude towards my lab-mates: Alfred Festus Davidson and Abhilash Reddy for countless discussions which helped me in solving challenging problems. I would take a moment to thank scholar Lakshman B. This thesis would have been incomplete without his experience and knowledge in Board design. His support helped me in timely completion of the project.

I would like to express my regards to all my friends and lab-mates who motivated me to take-up and finish this project. It will be absolutely incomplete if I do not share my gratitude and love towards my parents and my brother who had been setting up a comfort zone for me at home and away from home to carry out my research work and the rest of my academic life.

Abstract

Transmitters have always been an integral of a wireless communication systems. As the communication frequency band is increasing, there is a rising demand for a wideband transmitter, flexible enough, to be used over a wide frequency band. We have designed and simulated one such flexible Tx, with operating frequency between 100MHz to 12GHz.

Typically, at block level, RF Transmitter consists of an up-conversion Mixer, LO-Buffer, Pre-PA and Power Amplifier(PA). The new topologies were designed with an aim of improving Power and Area efficiency of the existing chip. This eventually led to development of a new topology called Power Mixer which has all the sub-blocks of transmitter merged into a single unit.

The project also involved testing version 1 of the chip for which various test boards were also designed. The test boards had the flexibility of choosing the matching networks as per the need. For better accuracy in measurements, de-embedding boards were also developed to extract the power losses.

The boards developed were finally sent to the manufacturer for the fabrication and testing.

Contents

List of Figures

Abbreviations

RF: Radio Frequency

PA: Power Amplifier

BW: Bandwidth

BW of a mixer: Oscillation Frequency at which the conversion gain of the mixer falls by 3dB.

BB: Baseband

Tx: Transmitter

Flo: Oscillation Frequency

1 Introduction

1.1 Prior Work

Prior work on the design of the Wideband Transmitter is documented in the thesis **Wideband RF Transmitter in TSMC 65nm technology working from 100MHz to 12GHz**. The block level transmitter architecture is shown in Fig. 1.

It consists of 2 separate Up-Conversion mixers and pre-PAs for I and Q signals which are added up in the PA. Mixer uses a simple double-balanced passive mixer topology followed by a CMOS pre-PA to drive the PA. PA consists of a simple common source cascode amplifier topology where I&Q signals are added up using current addition technique. The output of the on-chip PA goes to the matching network to drive 50ohms load.

There are also 2 LO-Buffers which are used to drive the Switching Mosfets in the passive mixer. The LO-Buffer uses a simple resistive-load common source pseudo-differential amplifier topology.

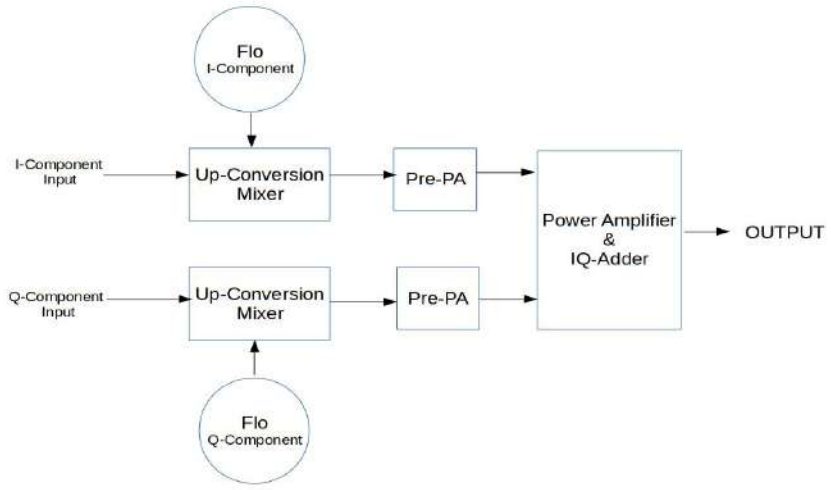

Figure 1: Tx Architecture 0

1.2 Contribution to IC Design

Taking a note of the previous Tx architecture, we tried to minimise the number of sub-blocks in the Tx architectures simultaneously improving gain and BW. The sub-blocks(to be discussed in next few sections) were designed at circuit level, based on the following topologies:

1.2.1 Topology 1:

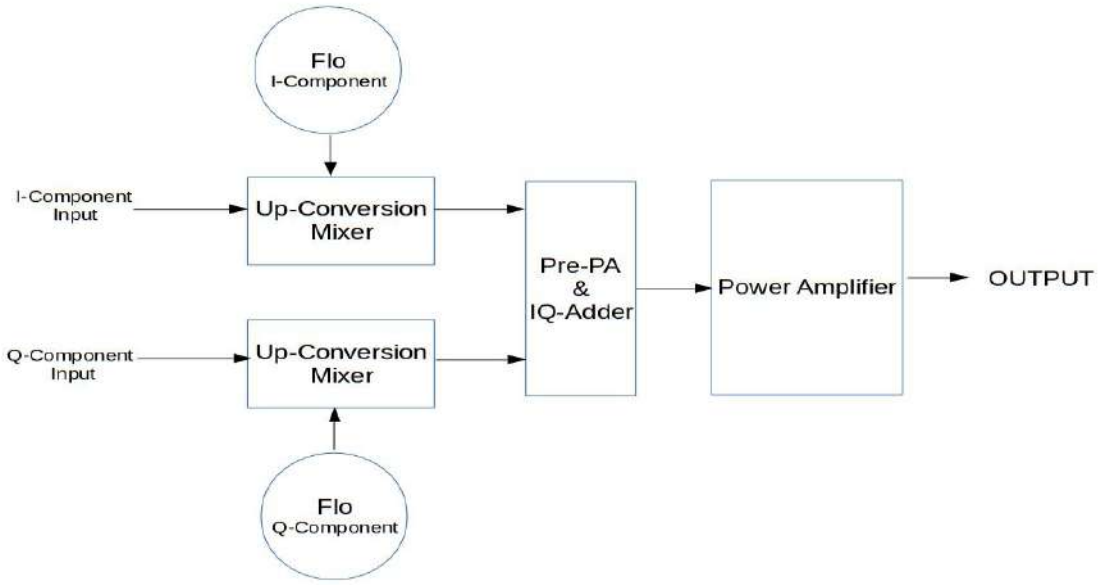

Figure 2: Tx Architecture 1

The maximum output power that can be delivered by the PA in Architecture 0 was reduced because of the adder combined with PA as the current was getting split for I&Q components. This issue was addressed by moving the addition of signals to the pre-PA stage. This would prevent the splitting of the PA current for 2 different signals and net output power delivered can be increased.
Although this topology didn't reduce the number of sub-blocks but it increased the net output power delivered to the load.

1.2.2 Topology 2:

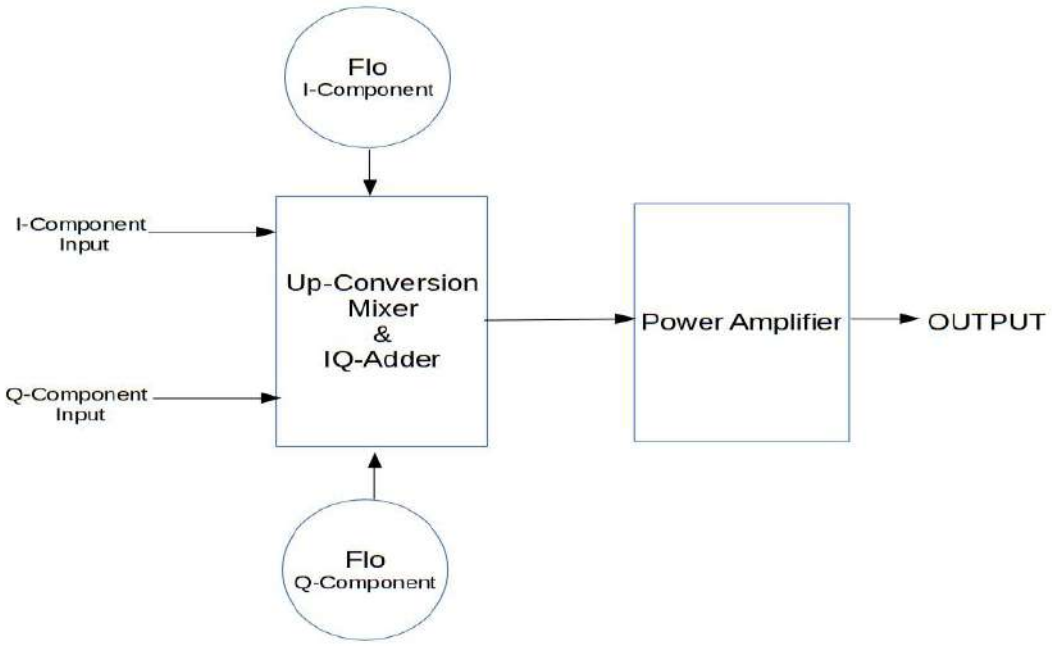

Figure 3: Tx Architecture 2

From the previous architecture, the adder can be moved from pre-PA stage to the mixer stage. Since, the addition of I&Q Signals is now happening in the mixer itself, there is no specific need of a pre-PA in the Architecture other than driving the high input capacitance of the PA.

If the input capacitance of the PA could be reduced and if the mixer could drive higher load capacitance, then the pre-PA can be safely eliminated.

By modifying the mixer and PA accordingly, we had completely removed pre-PA from the transmitter architecture.

1.2.3 Topology 3

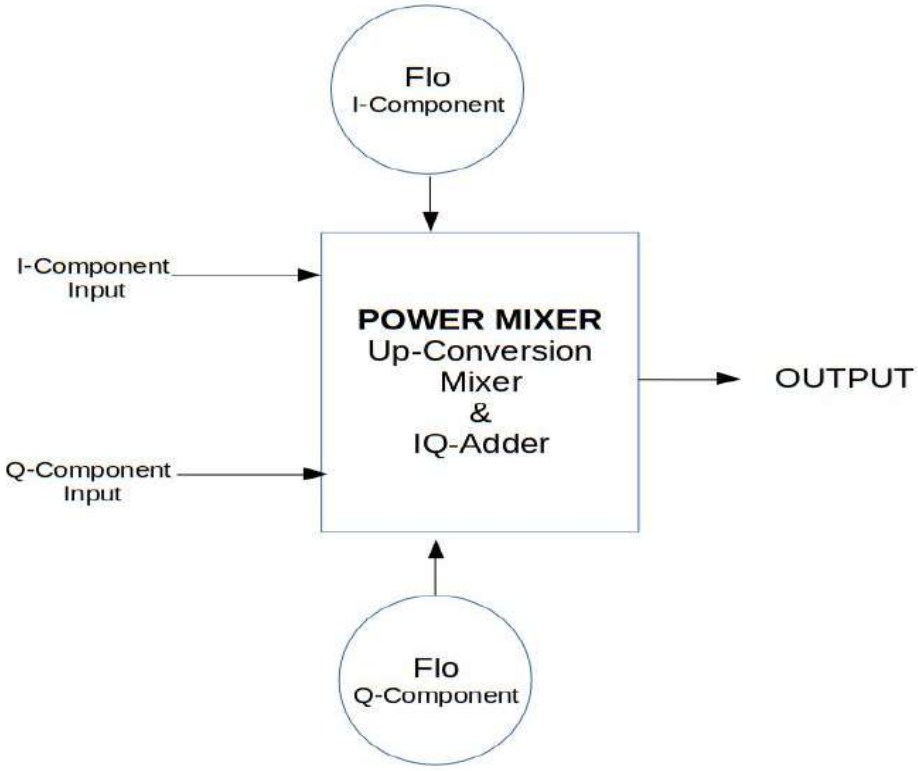

Figure 4: Tx Architecture 3

This is the new Transmitter Architecture we had tried.

In this architecture, the output power of the mixer is comparable to that of a standalone PA. This eliminates the need of an explicit PA in the transmitter architecture. This high output power mixer has been referred to as **Power Mixer** in this thesis. Along with the high power output, this mixer is also capable of adding I&Q-Signals. Thus all the functional sub-blocks (mixer, adder, PA) have been merged into a single unit called Power Mixer.

This way, the over-all Transmitter architecture consists of a Power Mixer and 2 pseudo-differential LO-Buffers.

1.3 Contribution to IC Testing

We have also worked on testing the version 1 of the chip which was designed by the scholar Kashyap V. Various PCB test boards were designed for this purpose.

1.4 Outline of the Thesis

In the next few section sections, we would be discussing about the sub-block used in the Tx architecture. Each section (from Section-2 to Section-4) will compare various circuit level architectures of the sub-blocks. We would be discussing about the various issues and their solutions in the design. Section-2 deals with designing of pre-PA which will act as a buffer between the Mixer and PA. Section-3 discusses about the various up-conversion Mixer designs.
Section-4 deals with merging all the sub-Blocks into one using called Power Amplifier. This block is a standalone block capable of performing signal up-conversion, addition and power amplification. Section-5 discusses about the Test Board design methodology for chip testing. It discusses about the Matching networks,power supply and test board schematics.
Last 2 sections, Section-6,7 has the concluding remarks and references used in the project.

2 Pre-PA

PA, due to it's large size, cannot be connected to Mixer directly. The large input capacitance of the PA makes it inevitable to have a low input capacitance buffer between the Mixer and the PA. This low input capacitance buffer is termed as pre-PA which acts as a low capacitance load at the output of the Mixer. In our design, pre-PA has additional facility of IQ-Signal adder. This helps in implementing the Tx Topology-1 as discussed in the previous section.

2.1 Topology 1: Simple Common source Amplifier

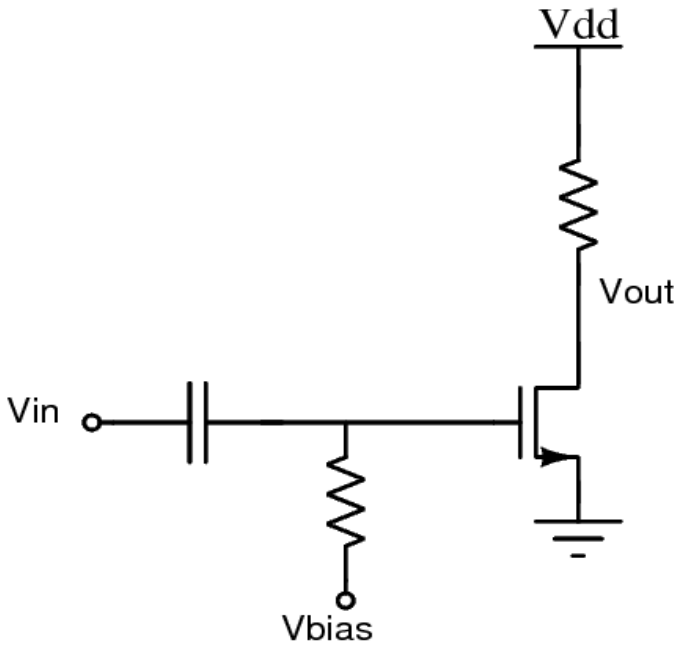

Figure 5: Simple Pre-PA

It's a simple Common source amplifier with resistive load. The design is meant to drive load capacitance of 250fF. The load resistance is set to 27Ω for a BW of approximately 22GHz to get a flat gain over 100MHz -12GHz. For high gain, the g_m of the nmos is set to 0.19S.

Results:

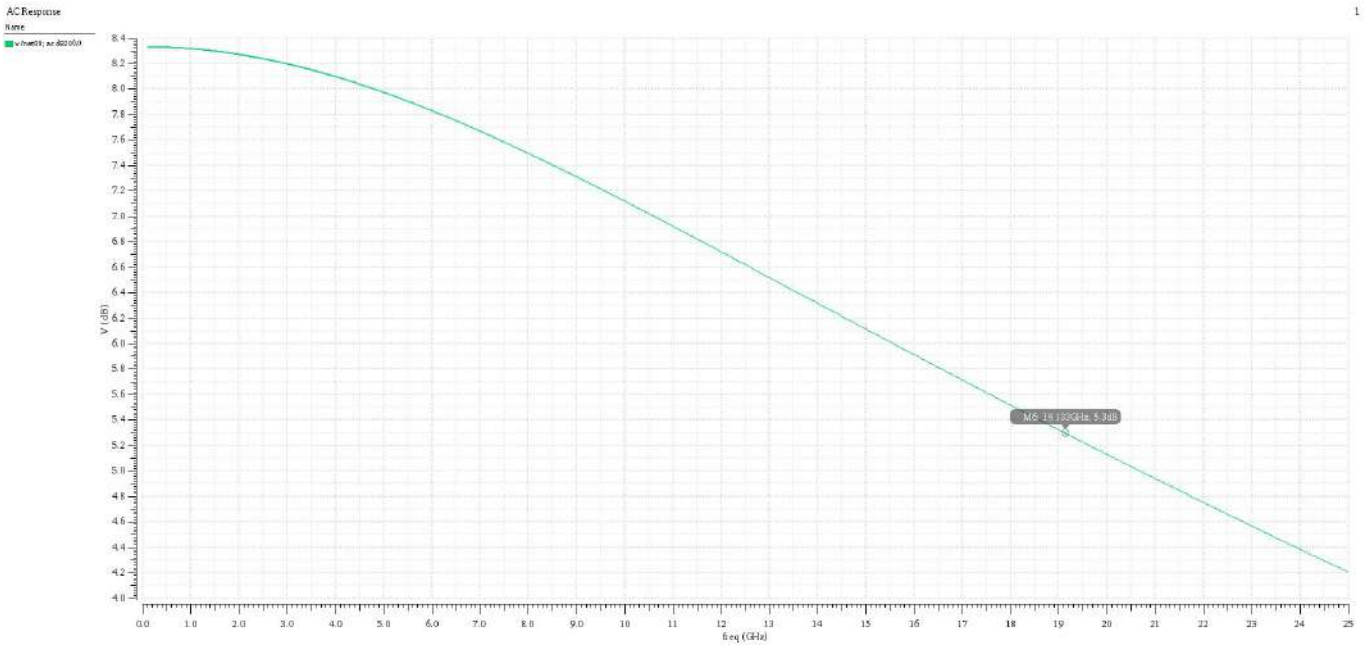

Figure 6: Pre-PA Gain vs Frequency

Observation: Observed gain is less than the calculated gain(14dB). It's because, due to the high current in the nmos, the value of rds is approximately 33Ω. This reduces the effective load at the output and so the maximum gain of the pre-PA falls down to 8.3dB. The BW has also reduced from 22GHz to 19GHz because of the capacitor C_{dd} at the drain of the mosfet.

A cascode device can be used to increase the over-all gain of the circuit.

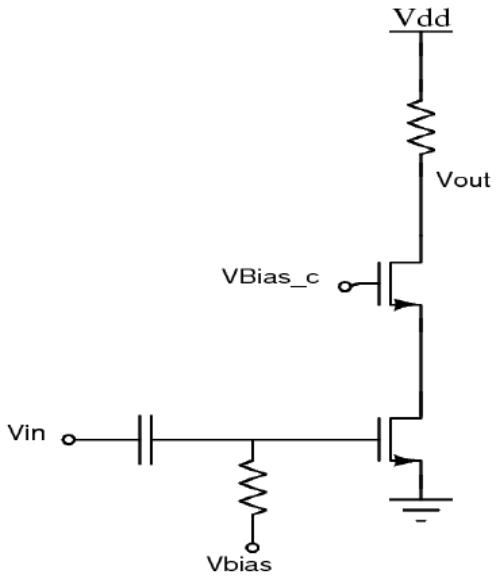

Figure 7: Pre-PA with Cascode Device

Result:

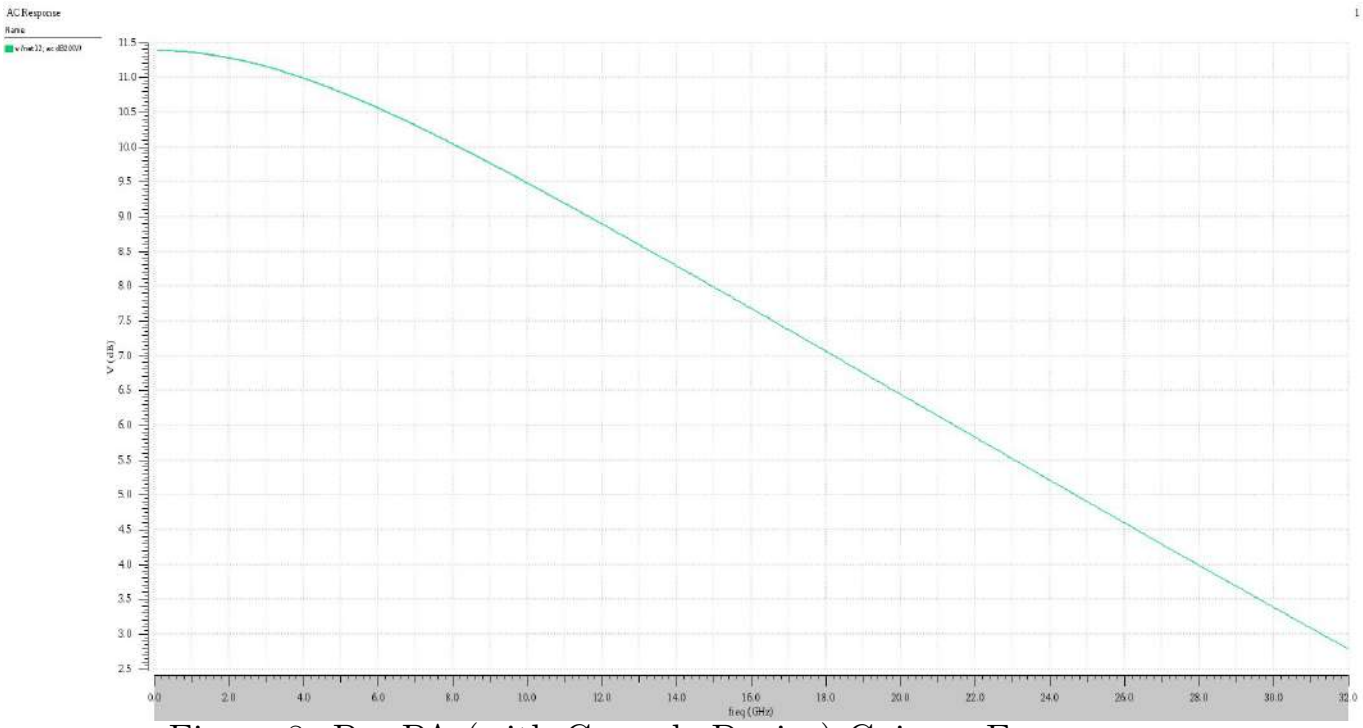

Figure 8: Pre-PA (with Cascode Device) Gain vs Frequency

The gain is now approximately 11.3dB, but the BW reduces to 14GHz. This is because of the high drain capacitance due to the large cascode nmos.

The BW can be extended using Peaking Inductor in series with the load resistor.

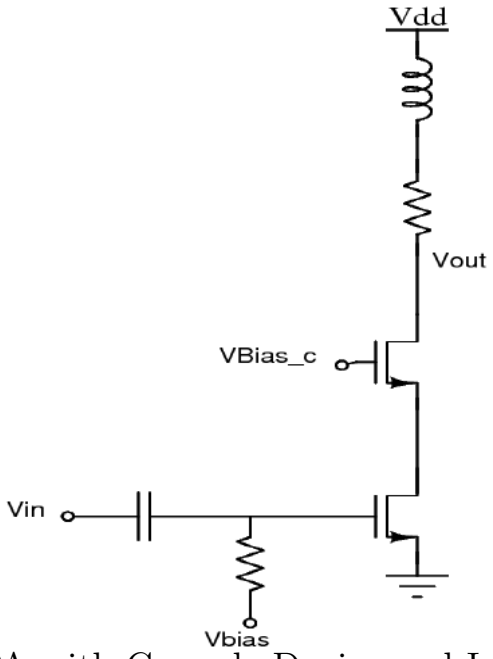

Figure 9: Pre-PA with Cascode Device and Inductor Peaking

The inductor value is calculated using the following formula:

$$L = \frac{R^2 C}{1.41}$$

where 'R' is the load resistance and 'C' is the load capacitance. The BW increases to about 1.8 times the BW without shunt peaking inductor:

$$BW_{new} = 1.8BW = \frac{1.8}{2\pi RC}$$

For the given value of resistor and load capacitor, inductor of 140pH is used in the circuit.

Results:

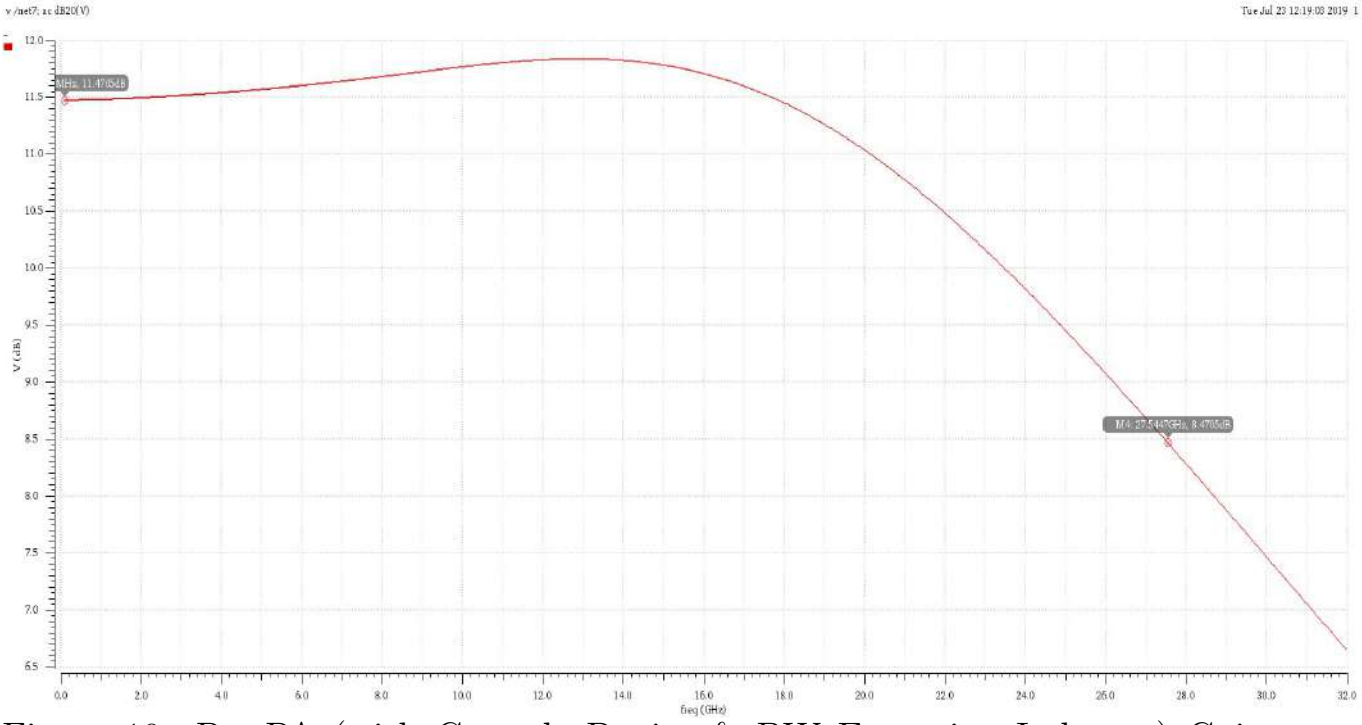

Figure 10: Pre-PA (with Cascode Device & BW Extension Inductor) Gain vs Frequency

Major Drawback: The input capacitance of the pre-PA is around 565fF which fails the main purpose of reducing the load on the mixer.

2.2 Topology 2: Pre-PA with IQ-Signal Adder

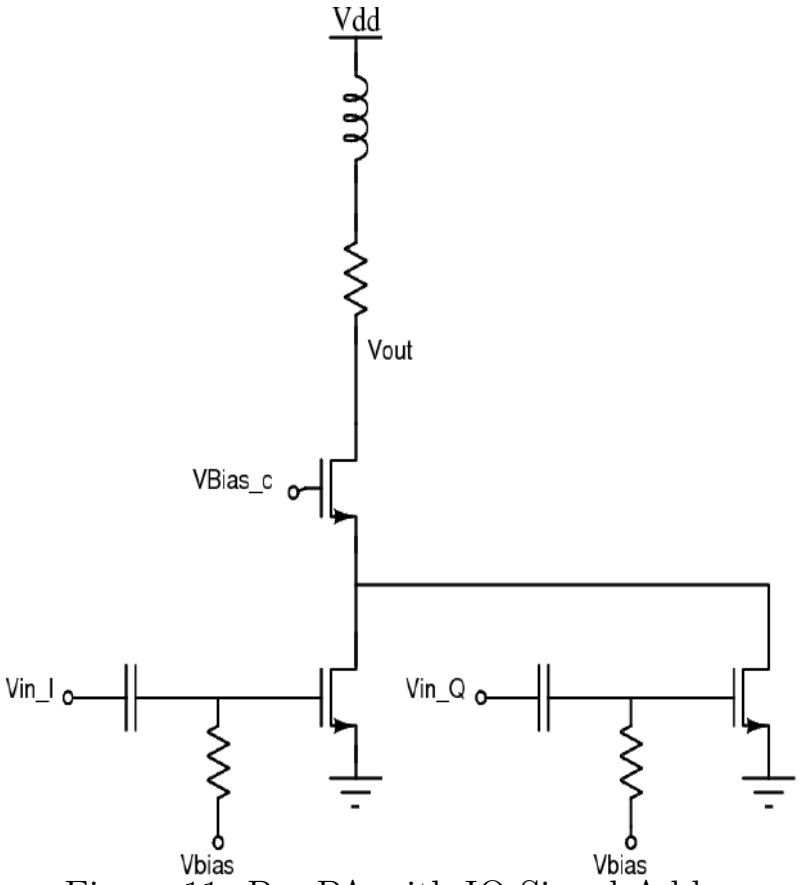

Figure 11: Pre-PA with IQ-Signal Adder

The issue mentioned in the previous section was corrected by compromising on the gain of the pre-PA. The size of the transconductor mosfet was reduced to get lower the input capacitance.

The input transconductor mosfet was also split into two, one for each I & Q signal. The output currents of the 2 transconductor mosfets are added up at the source of the cascode nmos. This way, IQ-Signal adder was also integrated in the pre-PA.

By reducing the transconductor sizes, the input capacitance of the pre-PA was reduced to 65fF for each I & Q signal.

Using the calculations as discussed in the previous section, a peaking inductor of 208pH was used for BW extension.

Results:

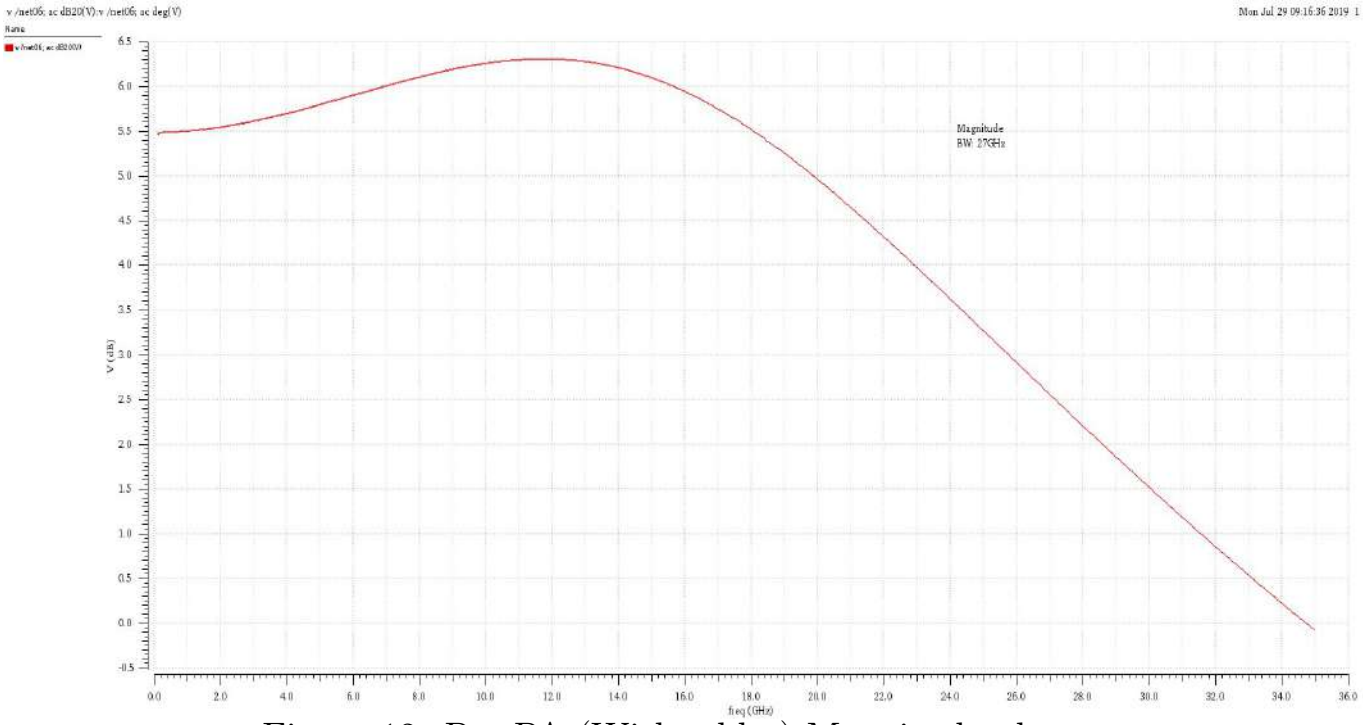

Figure 12: Pre-PA (With adder) Magnitude plot

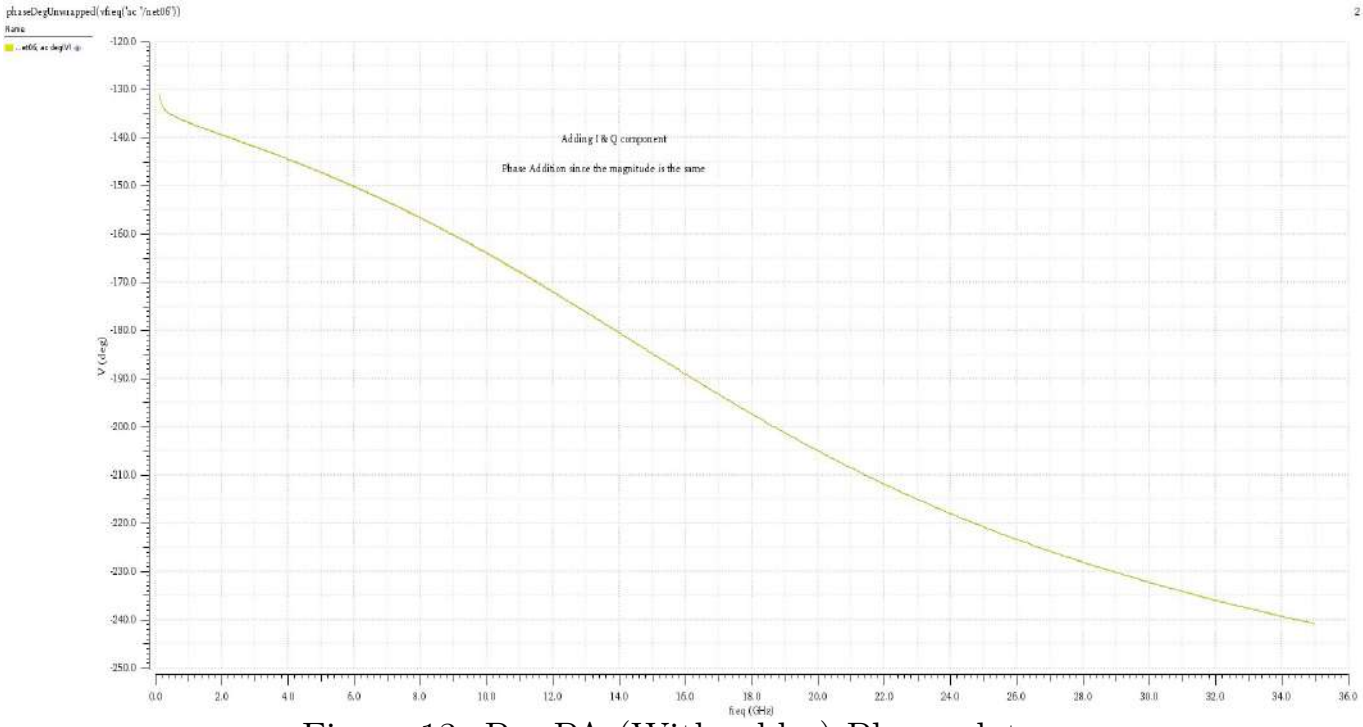

Figure 13: Pre-PA (With adder) Phase plot

From the magnitude and phase plot, it can be seen that the output is amplified sum of I & Q signals. Phase of input I-component and Q-component is 0 rad and $\pi/2$ rad. This pre-PA with adder can be used for topology-1 as discussed in section-1.

3 Mixer

In this section we will be briefly discussing about the various active Mixer topologies, their design procedures and pros & cons of the design.

3.1 Topology 1: Gilbert Cell

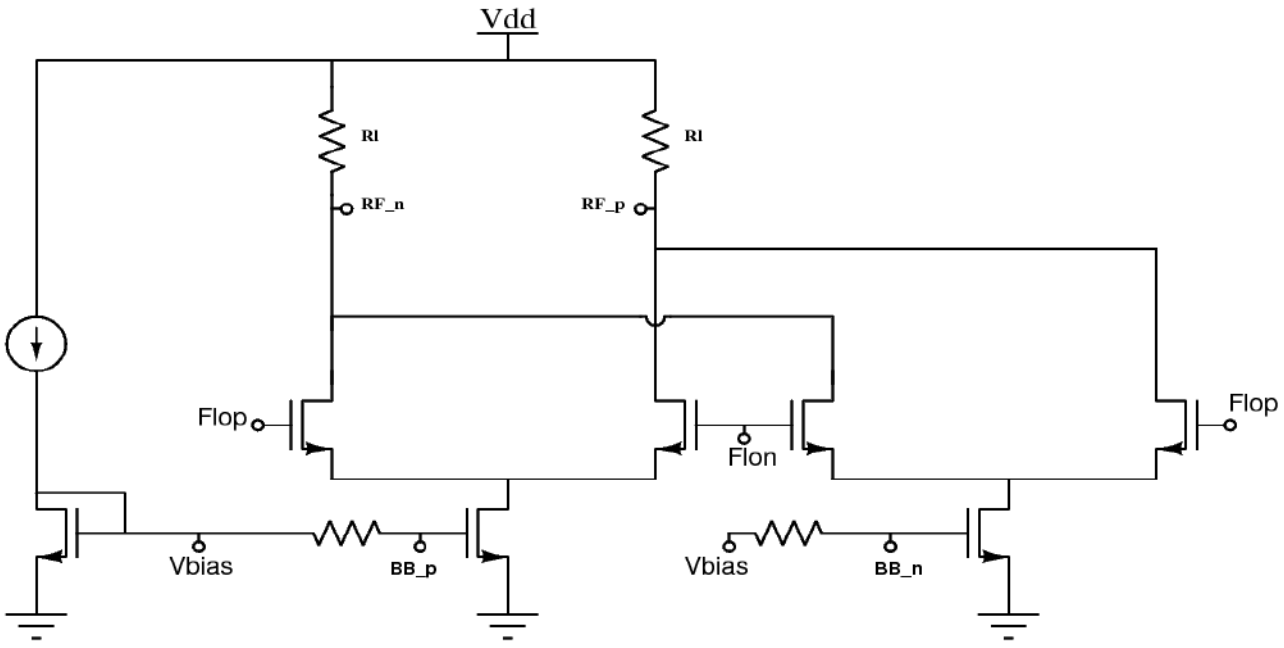

Figure 14: Gilbert Cell

For Tx Architecture 1, a simple double balanced gilbert cell mixer can be used to up-convert the signal. As compared to a passive mixer, it provides a good gain upfront. We get a reasonable gain of around 6.5dB at low frequency and 3db Bandwidth of around 16GHz. However, the gain is limited by the Resistor size (which is limited by the BW) and the current in the transconductor (which is limited by the size of the switching nmos). Increasing switching nmos size makes the designing of LO-Buffer impossible because of the high gate capacitance which causes the load resistance of the LO-Buffer to be very small. This limits the overall performance of the mixer.

Results:

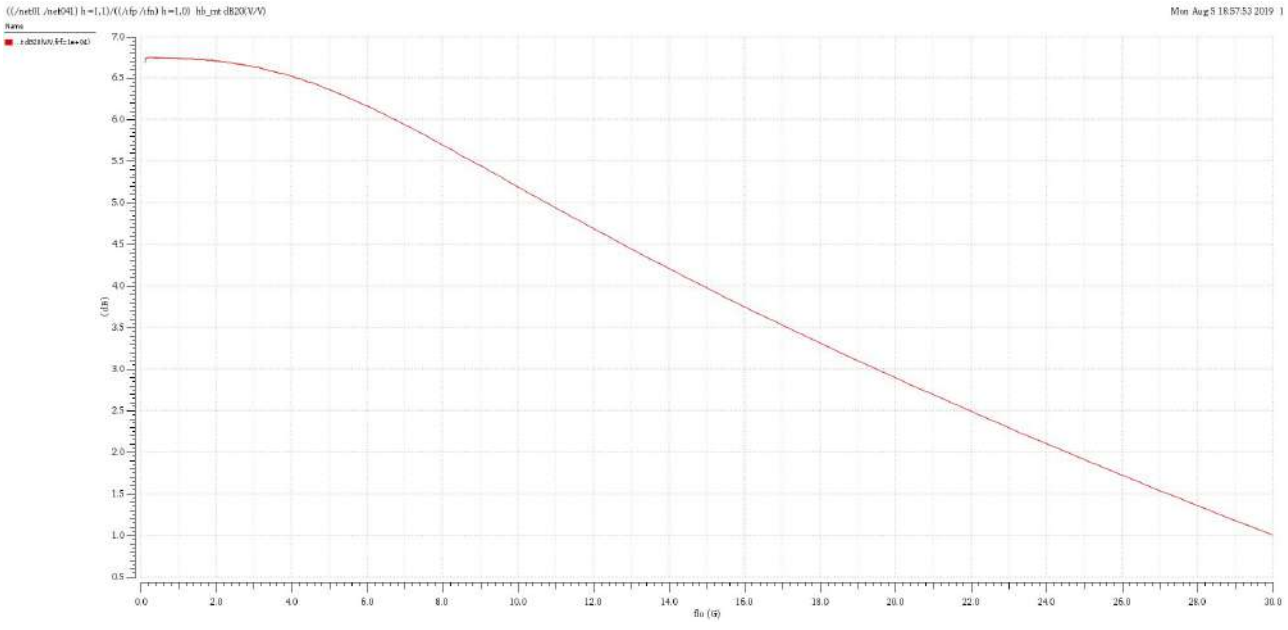

Figure 15: Gilbert Cell Conversion Gain vs Flo @ BB frequency=10KHz

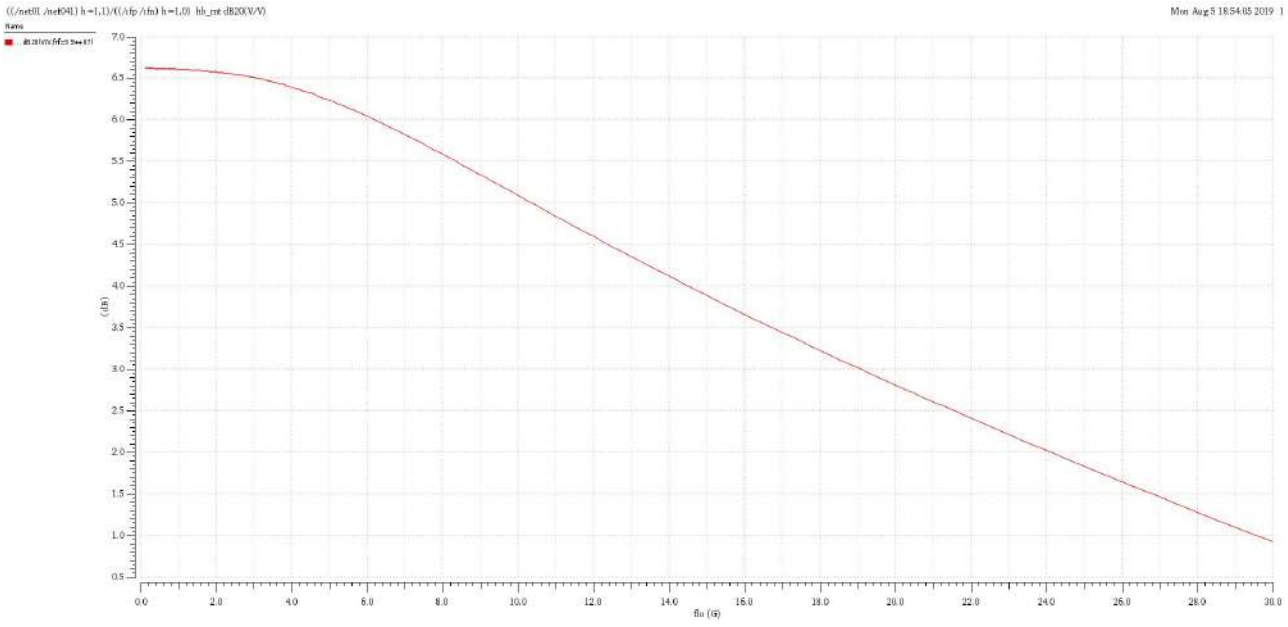

Figure 16: Gilbert Cell Conversion Gain vs Flo @ BB frequency=99MHz

The issue of low gain can be solved by:

i Adding a current bleeder pmos to push extra current through the transconductor via switching mosfets. This is not a preferred solution as the

size of the switching nmos has to be increased which means higher capacitance on the output nodes and also higher load capacitance for the LO Buffer.

ii Add a current bleeder pmos to push extra current through the transconductor by-passing the switching nmos. This would increase the gm of the transconductor and in turn the conversion gain. Also, since the signal at the drain of the transconductor is a Baseband/Low Frequency signal, the extra capacitance will have negligible effect on the overall performance of the circuit.

3.2 Topology 2: Glibert Cell with Current Bleeder

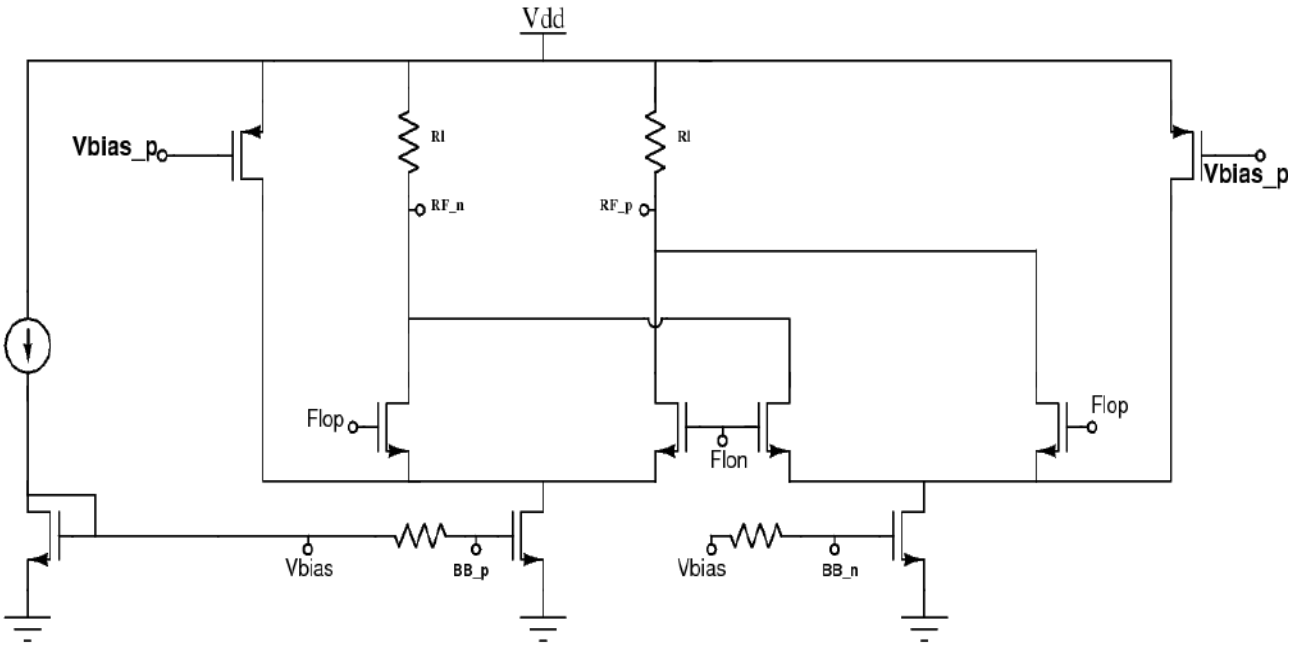

Figure 17: Gilber Cell with Current Bleeder

A current bleeder has been added to a Gilbert cell to increase the trancsonductance of the transconductor mosfet for higher gain. It's expected that as the current through the pmos transconductor is increased, the conversion gain of the mixer increases. However, it is observed that the increase

in conversion gain isn't proportional to the increase in bleeder current (keeping the over-drive voltage of the constant). This is due to the fact that as the current in the transconductor increases, it's rds starts falling and hence, lesser signal current goes through the switch to the load. This can be corrected by increasing the length of the transconductor keeping the over-drive voltage constant (as channel length modulation is inversely proportional to the length of the device). The increased capacitance at the drain of the transconductor doesn't effect the over-all performance of the circuit since the signal at that node is of low frequency. Simultaneously, length of the pmos current bleeder should also be increased to minimise the signal current leakage from rds of the pmos. This way we were able to increase the conversion gain of the mixer to around 19dB and BW of 18GHz.

Results: Load resistance =90Ω, load capacitance = 65fF

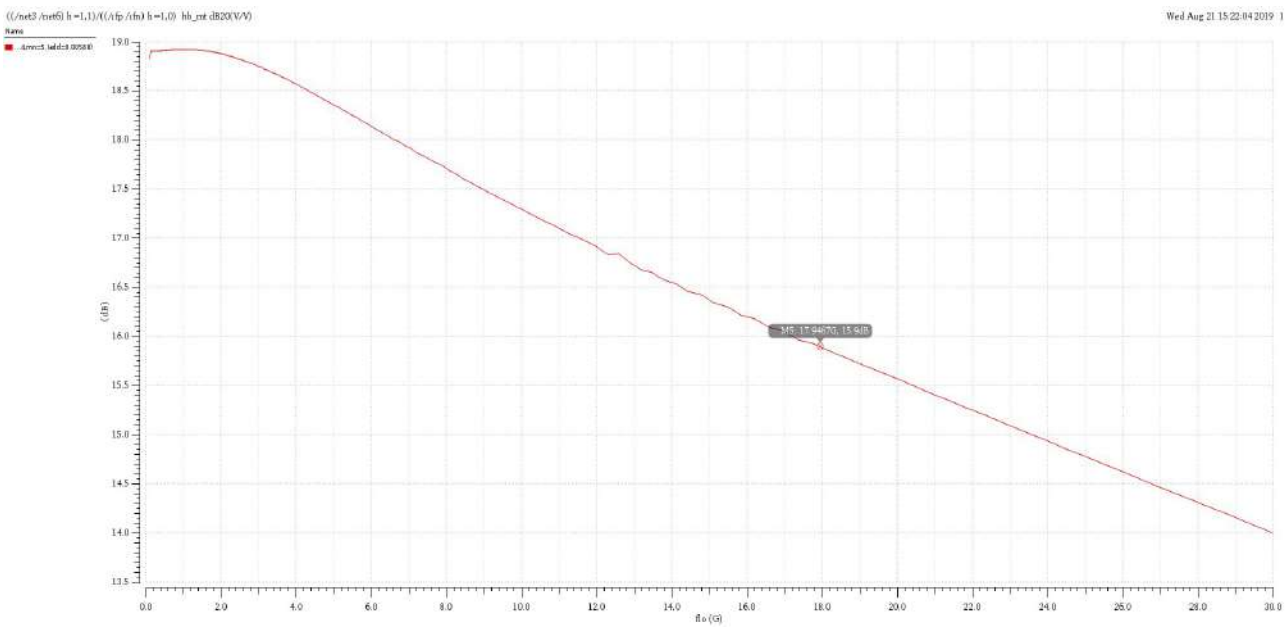

Figure 18: Gilbert Cell with Current Bleeder: Conversion Gain vs Flo @ BB frequency=10KHz

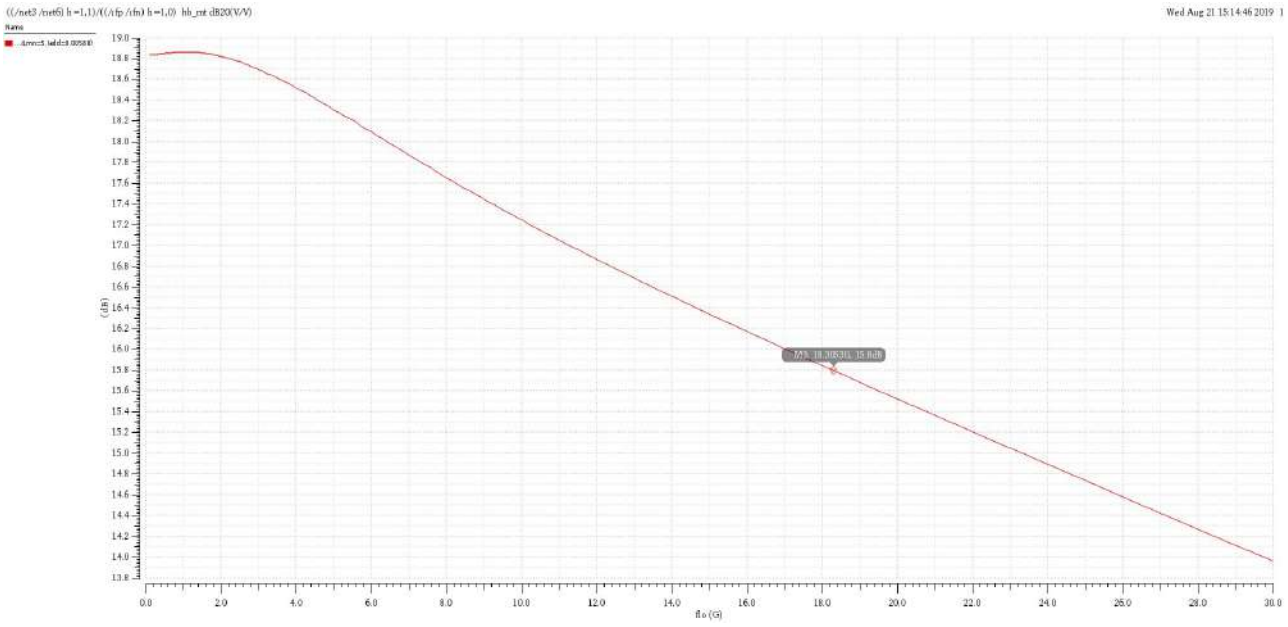

Figure 19: Gilbert Cell with Current Bleeder: Conversion Gain vs Flo @ BB frequency=99MHz

Till now we had use RF devices in the PDK which are well modelled for RF signals. Since the signals seen by the transconductor nmos and bleeder pmos in a BB Low frequency signal, we can replace these devices by an equivalent BB devices as they allow longer mosfets. This improved the conversion further to 22dB with a BW of approximately 18GHz. This topology is well suited for the Tx-Architecture 1 as discussed in section 1.2.1.

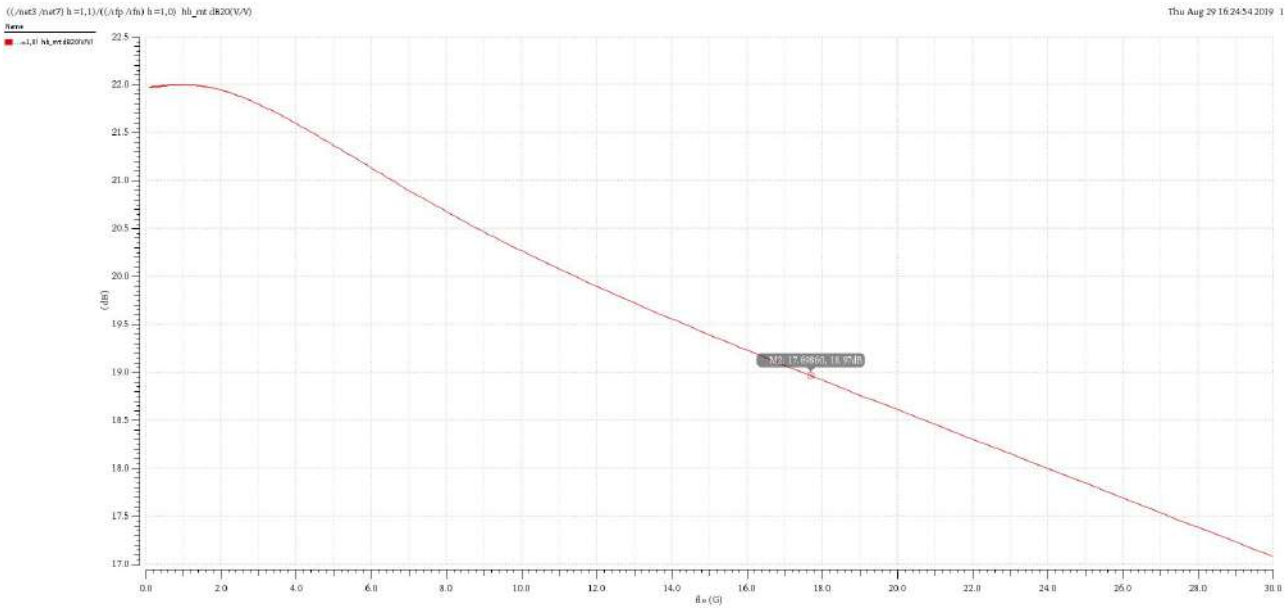

Figure 20: Gilbert Cell with Current Bleeder & BB NMOS Device: Conversion Gain vs Flo

3.3 Topology 3: Mixer With IQ-Signal Adder

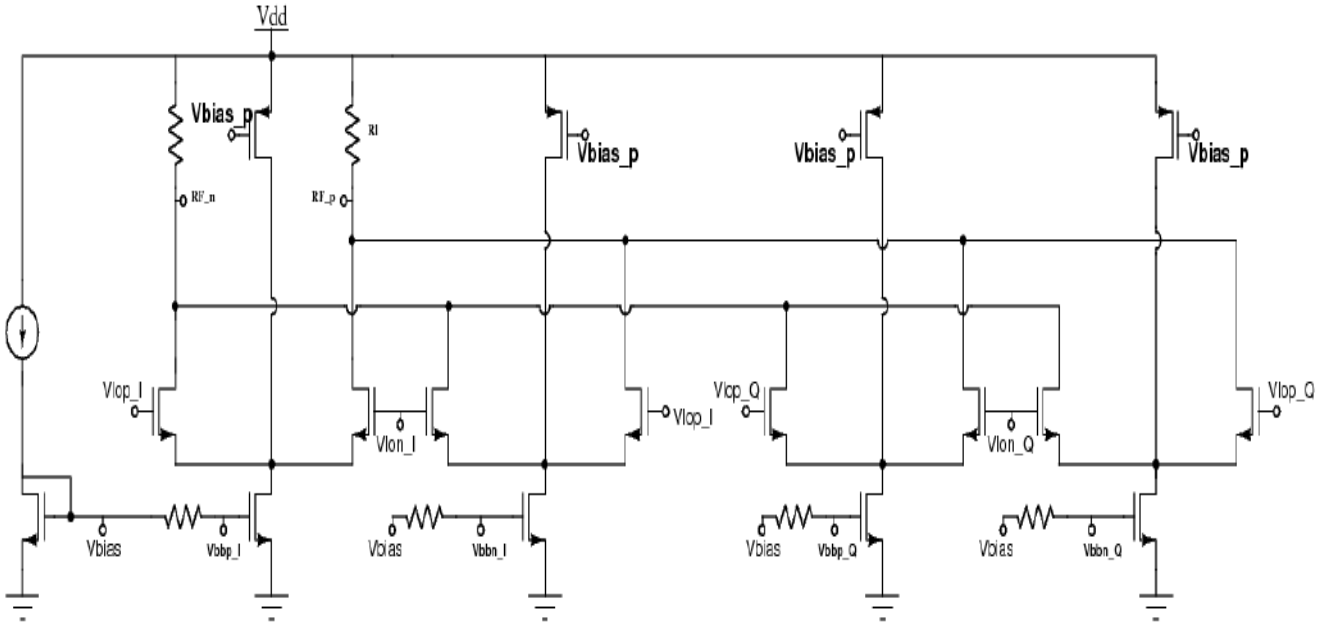

Figure 21: Gilbert Cell with IQ-Adder and Current Bleeder

This topology consists two gilbert cell with current bleeder for I & Q Components. The 2 signal currents are added up together and then fed to the

load resistor thus merging adder into the mixer itself. The load resistance has been reduced to 50Ω as the quiescent current in each resistor has doubled.
To remove the Pre-PA and drive PA directly from the mixer, the load resistance was reduced further from 50Ω to 27.5Ω. We could then drive higher load capacitance (input capacitance of PA) without compromising on the BW. Although this meant a compromise on the mixer conversion gain but we would be able to implement the architecture 2 as discussed in section 1.2.2.
This simulation was done by sweeping Flo and measuring the conversion gain over for various values of the load capacitance & keeping the Load resistor fixed.
Results: Load resistance = 27.5Ω

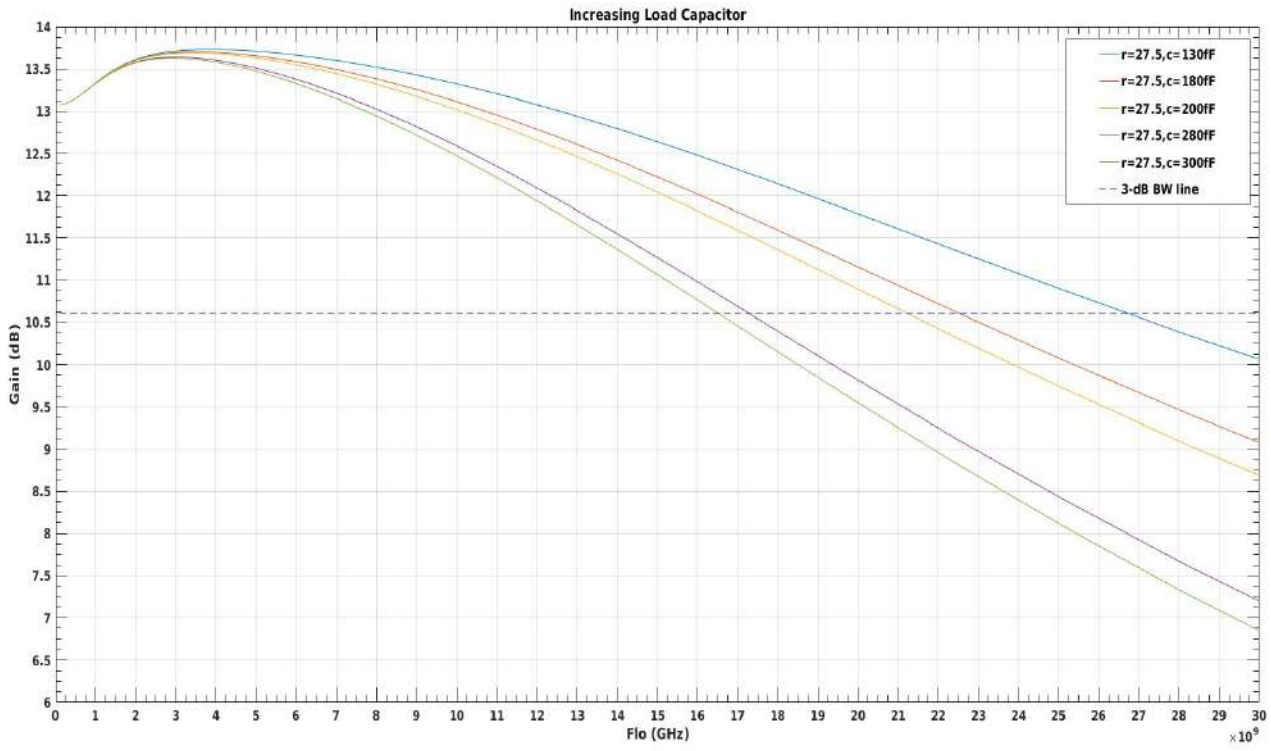

Figure 22: Mixer with IQ-Adder: Conversion Gain vs Flo

Observations: As expected, the conversion gain remains constant and the BW varies with the load capacitor values. The BW vs Load capacitance is summarised in the table blow:

Load Capacitance	3dB BW
130fF	27GHz
180fF	22GHz
200fF	21GHz
280fF	17GHz

Issues:

i BW can be improved using BW extension technique (to be discussed in the next section)

ii Low output referred 1-dB Compression point

3.4 Topology 4: Mixer with improved BW and 1-dB compression point

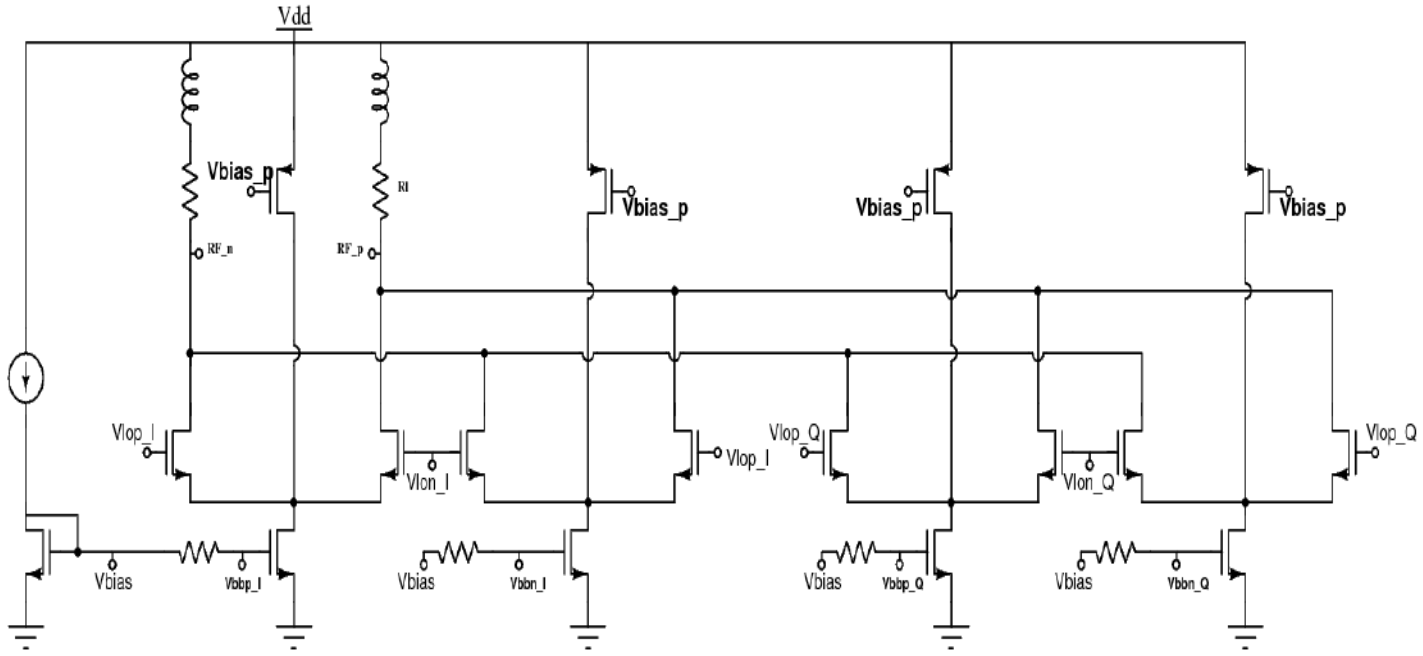

Figure 23: Mixer with BW Extension Inductor: Conversion Gain vs Flo

In this topology, a center-tapped shunt inductor has been added to the circuit. The inductor value is calculated using the following formula:

$$L = \frac{R^2 C}{1.41}$$

where 'R' is the load resistance and 'C' is the load capacitance. The BW increases to about 1.8 times the BW without shunt peaking inductor:

$$BW_{new} = 1.8BW = \frac{1.8}{2\pi RC}$$

So for R=27.5Ω , C=300fF, the inductance of the centre tapped inductor is 0.375nH.

This increases the BW from 17GHz to approximately 29GHz which can been seen in the **Results** section below.

Results:

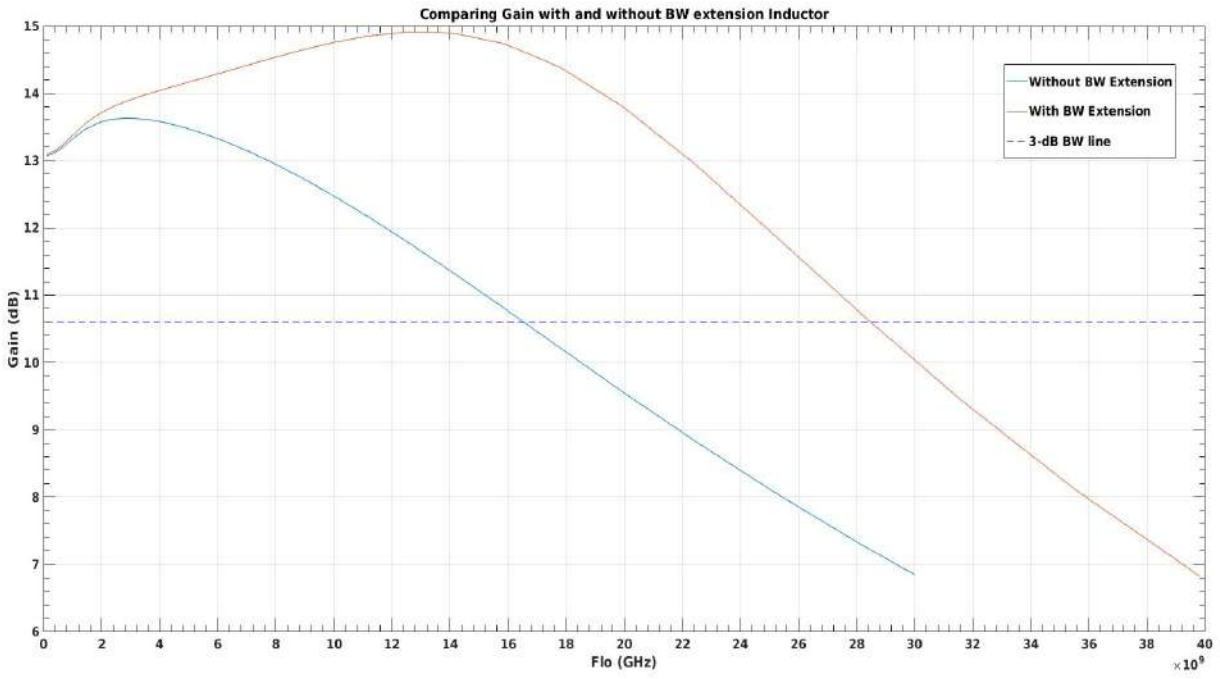

Figure 24: Conversion Gain vs Flo

Issue: The Output referred 1-dB compression point is -2dBm.

The output referred 1-dB Compression point is limited by the small current flowing in the switches. The input BB signal voltage limit equals I_d/g_m where I_d is the quiescent current through the switches and g_m is the transconductance of the transconductor nmos. The reduced over-all gain (because of the reduced load resistor) thus reduces the maximum output power of the mixer.

This can be corrected by increasing the size of switching nmos and reducing the size of current pmos to pump higher current through the switching branch. This increases the Output Referred 1dB compression point but hurts the BW as the capacitance at the output node has increased due to the increased drain capacitance of the switching nmos. Since, we are designing Mixer to operate till 12GHz, fall in BW from 28GHz is acceptable.

The resulting conversion gain vs Flo plot is shown below:

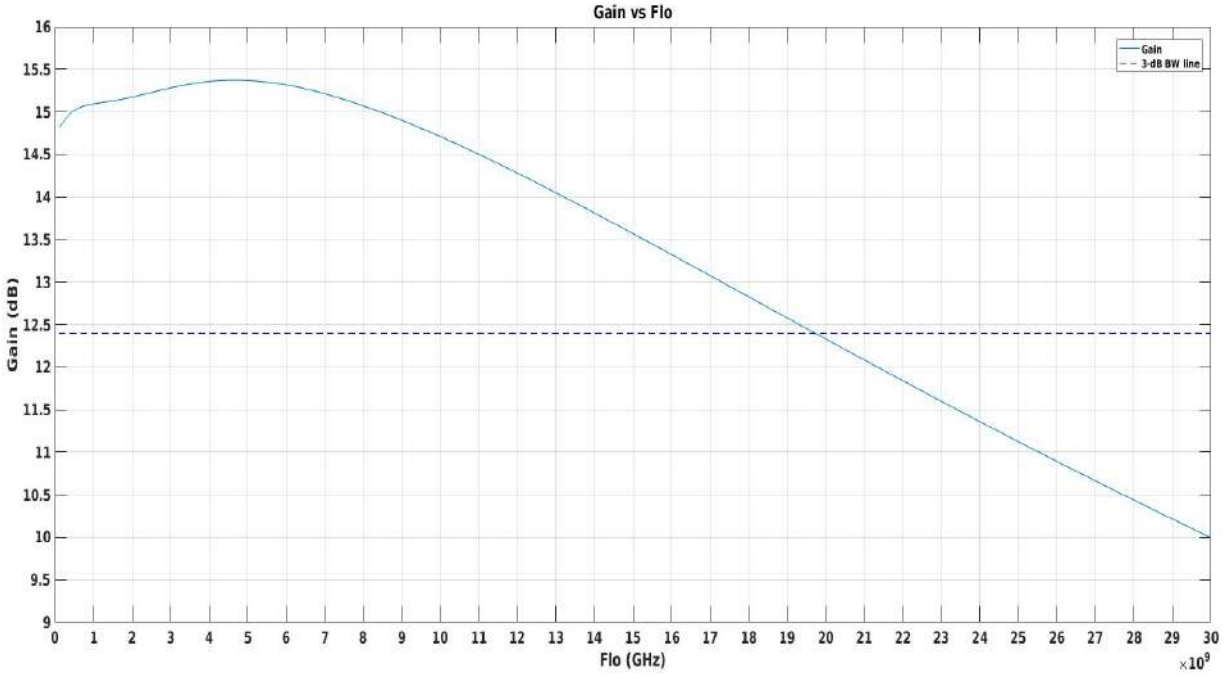

Figure 25: Conversion Gain vs Flo

The Output referred 1dB Compression Point of the mixer is 1.37dBm.

Parasitic Extraction:

To get more accurate simulation results, the parasitic capacitance and resistance were extracted and the model was used for simulation. The layout of transconductor nmos, switching nmos and current bleeder pmos was done. The parasitics thus extracted was used to model real mosfet which were then used in the simulation. The switch nmos size and current through them were also increased to get better 1dB compression point.

Result Post Parasitic Extraction:

The output referred 1dB compression improves to 2.04dBm

BW =19GHz, Load Capacitance = 300fF, Load Resistor= 27.5Ω

peaking inductor value: 565pH (centre-tap symmetric inductor with 2 turns)

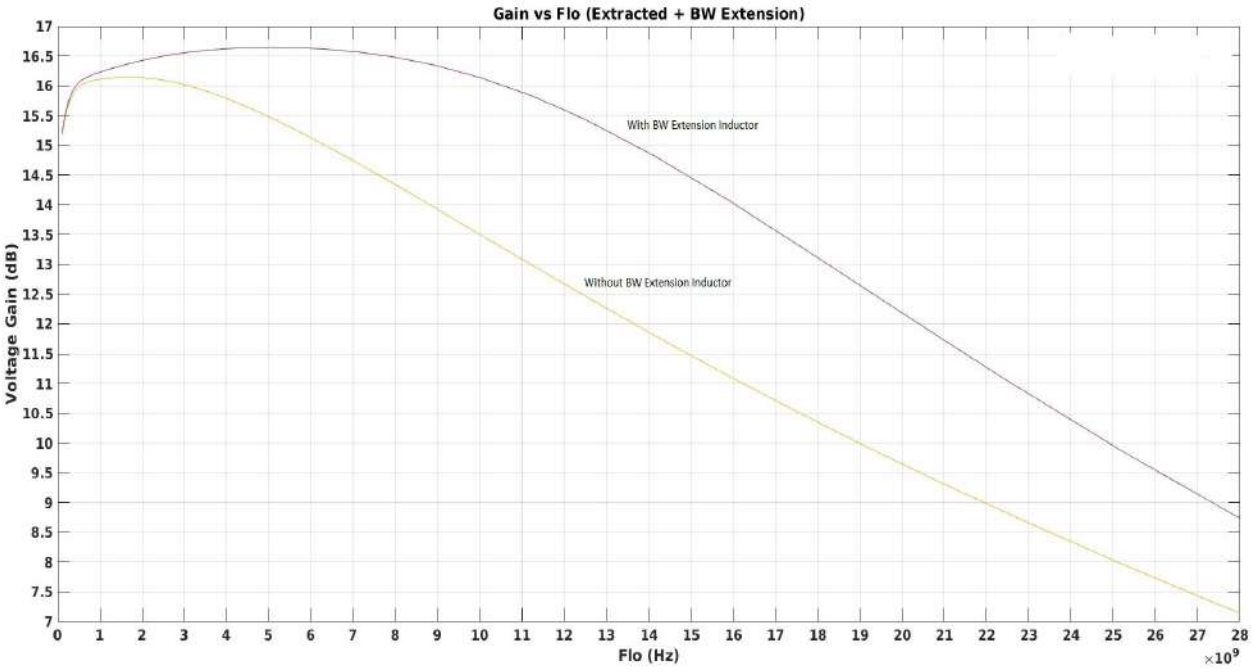

Figure 26: Conversion Gain vs Flo (Parasitic Extracted)

4 Power Mixer

Power Mixer is the term given to the mixer with high Output Referred 1dB compression point. The high output power from this mixer eliminates the need of a separate Power Amplifier.

This architecture thus combines Mixer, IQ-Adder and PA into a single unit and is useful in implementing Tx-Architecture 3 as discussed in section-1.

4.1 Topology 1: Power Mixer

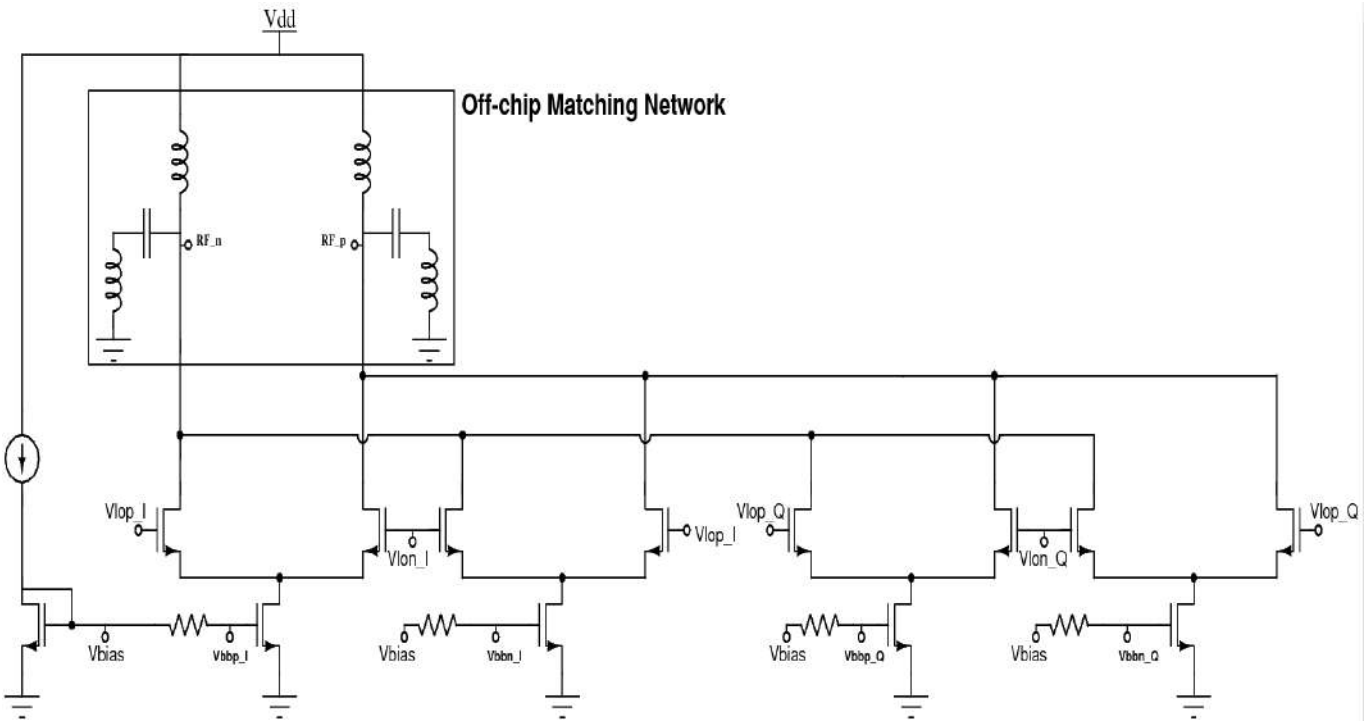

Figure 27: Power Mixer

This topology consists of double-balanced gilbert cell with current based signal adder. The topology is similar to the Mixer discussed in Section 3.3 except, the current bleeders have been removed. The switches and transconductor mosfets are 2.5V devices, power supply (VDD) used is 2.5V and has an off-chip matching network.

The off-chip matching network consists of a High-Pass pi-match network, to reduce the resistance from 50Ω to 12.5Ω.

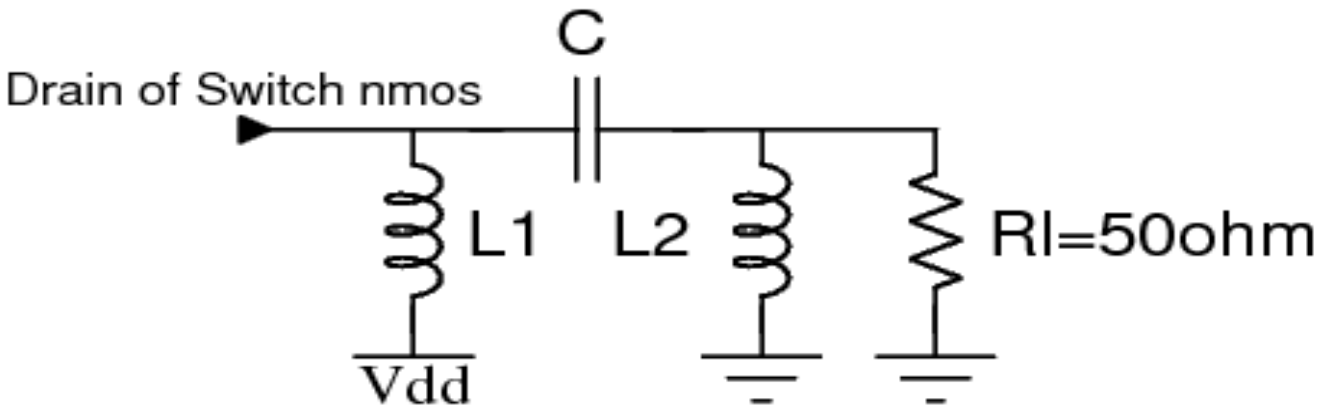

Figure 28: Matching Network

To get the values of the matching network, a python script[1] was developed to generate L1, C and L2 values for the given quality and oscillation frequency. Higher output power in the mixer is due to high current pumped through the switching branch and the load. This is done by increasing the size of the switching nmos and transconductor. The drain-bulk capacitance of the switching nmos in absorbed by L1 in the matching network.
Layout of Transconductor and Switches was also done for parasitic extraction which are shown below:

[1]Check appendices

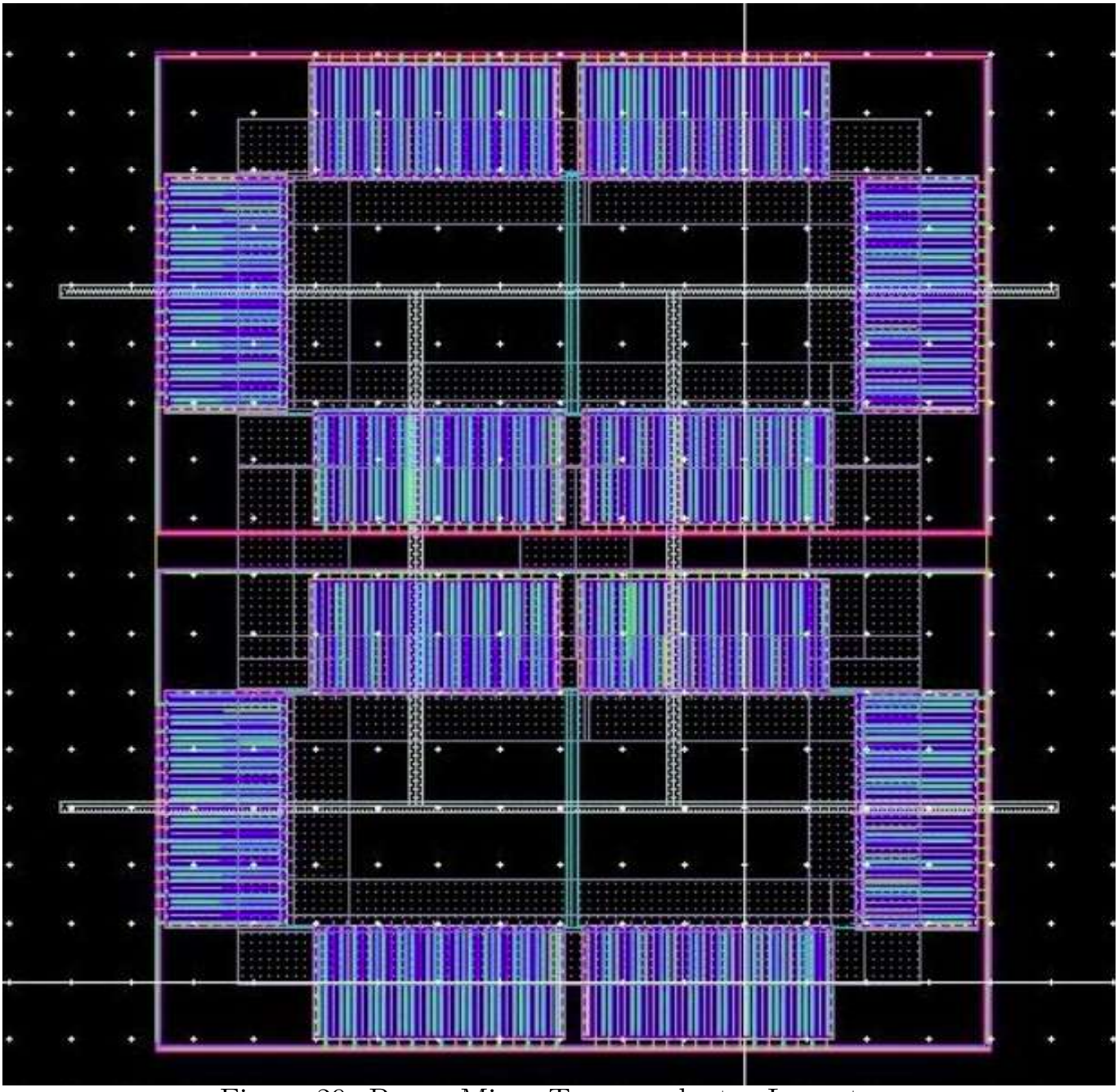

Figure 29: Power Mixer Transconductor Layout

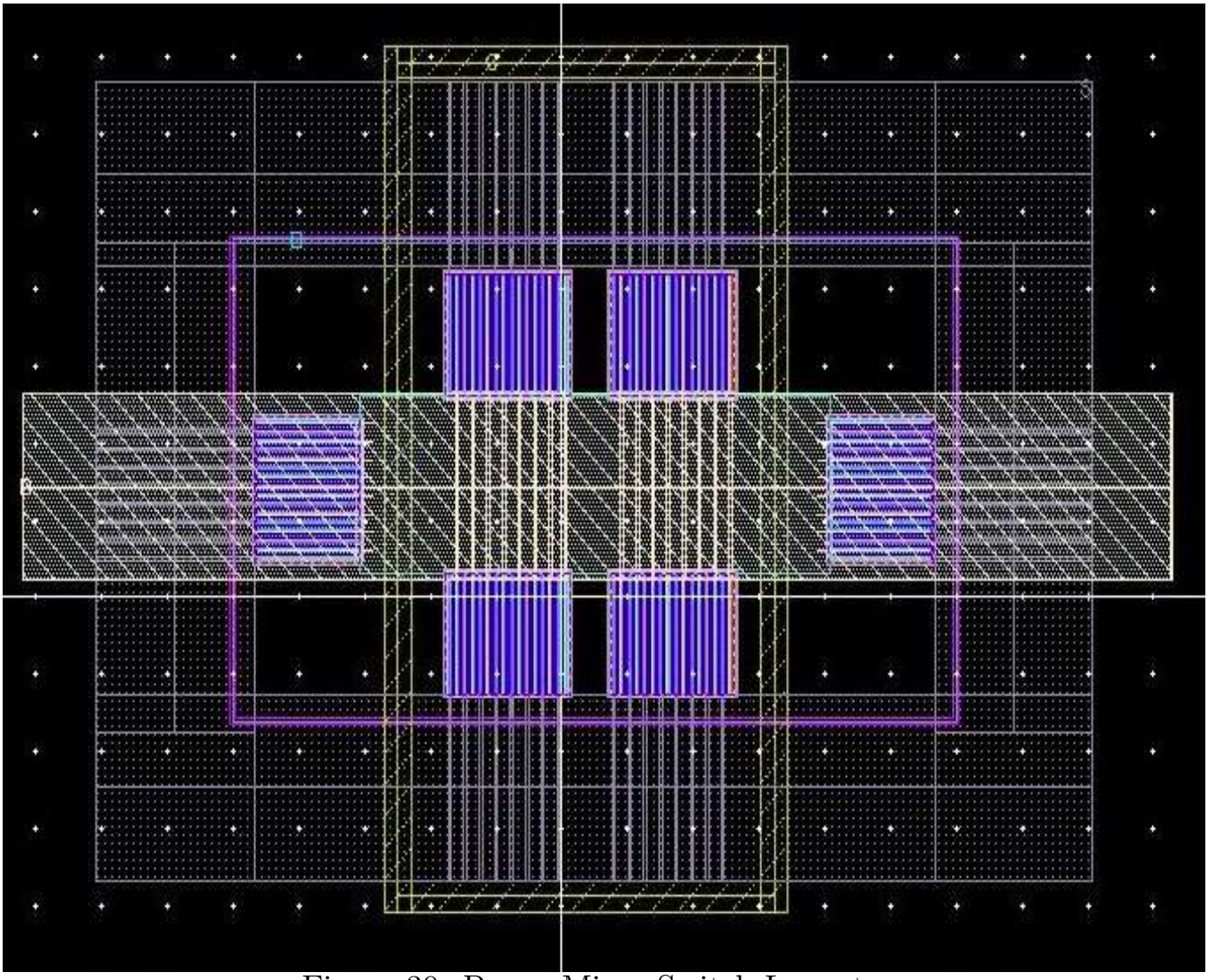

Figure 30: Power Mixer Switch Layout

The round-table layout topology were used to get thicker metal traces for the given area to sustain high current. Zipper layout topology was avoided as it would have given higher capacitance at the Drain and Source of the mosfet due to large trace widths.

Results:

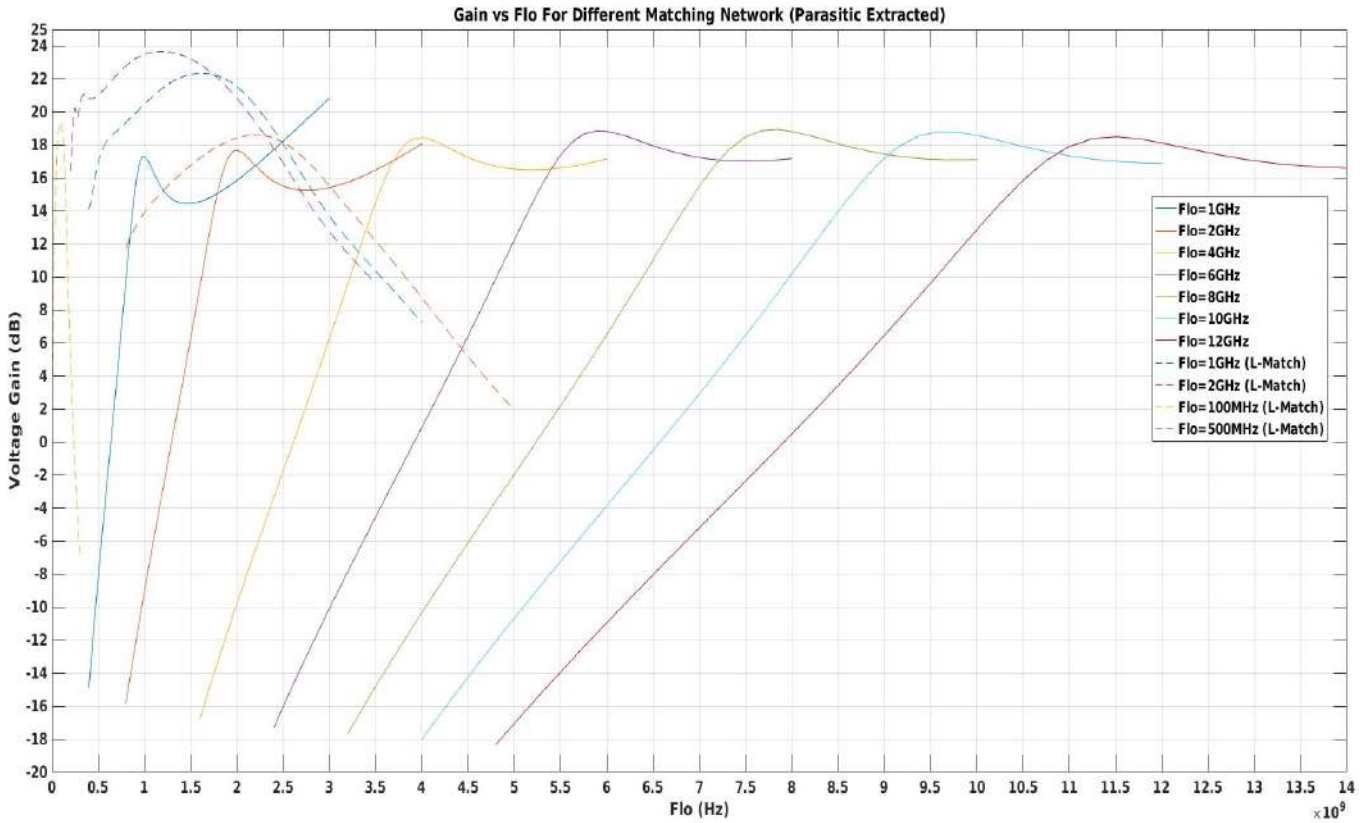

Figure 31: Conversion Gain vs Flo

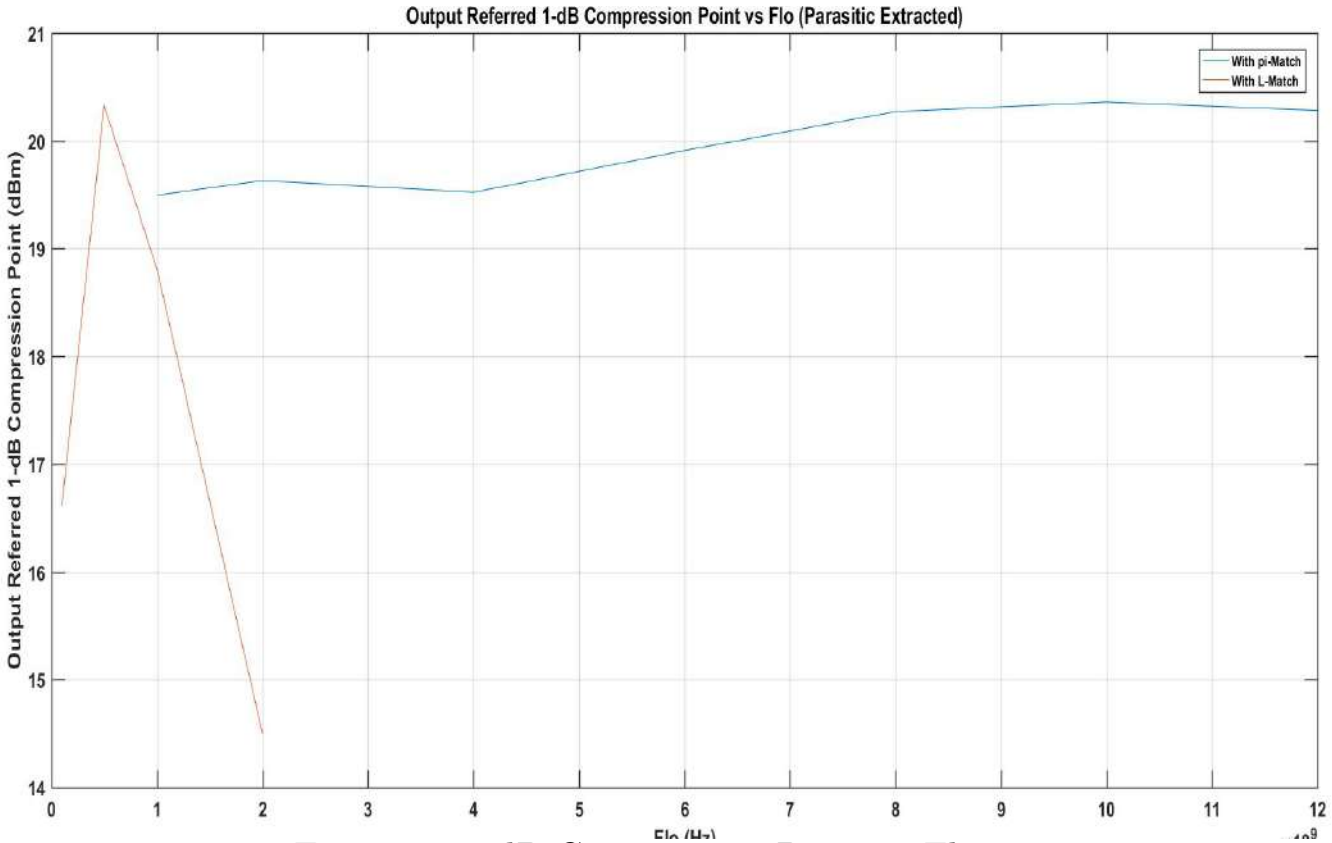

Figure 32: 1dB Compression Point vs Flo

Issues:

(i) Due to large size, the gate capacitance of the mixer switch is around 1pF which means the LO Buffer has to drive a load of 2pF. In this case, the load resistance of the LO-buffer is approximately 6.5Ω which is difficult to achieve.

(ii) Reducing the gate capacitance by reducing switch size causes the gm of the switching device to fall. This makes the voltage amplitude at the drain of the transconductor to increase and thus reduces the output compression point

4.2 Topology 2: Power Mixer with cascode NMOS

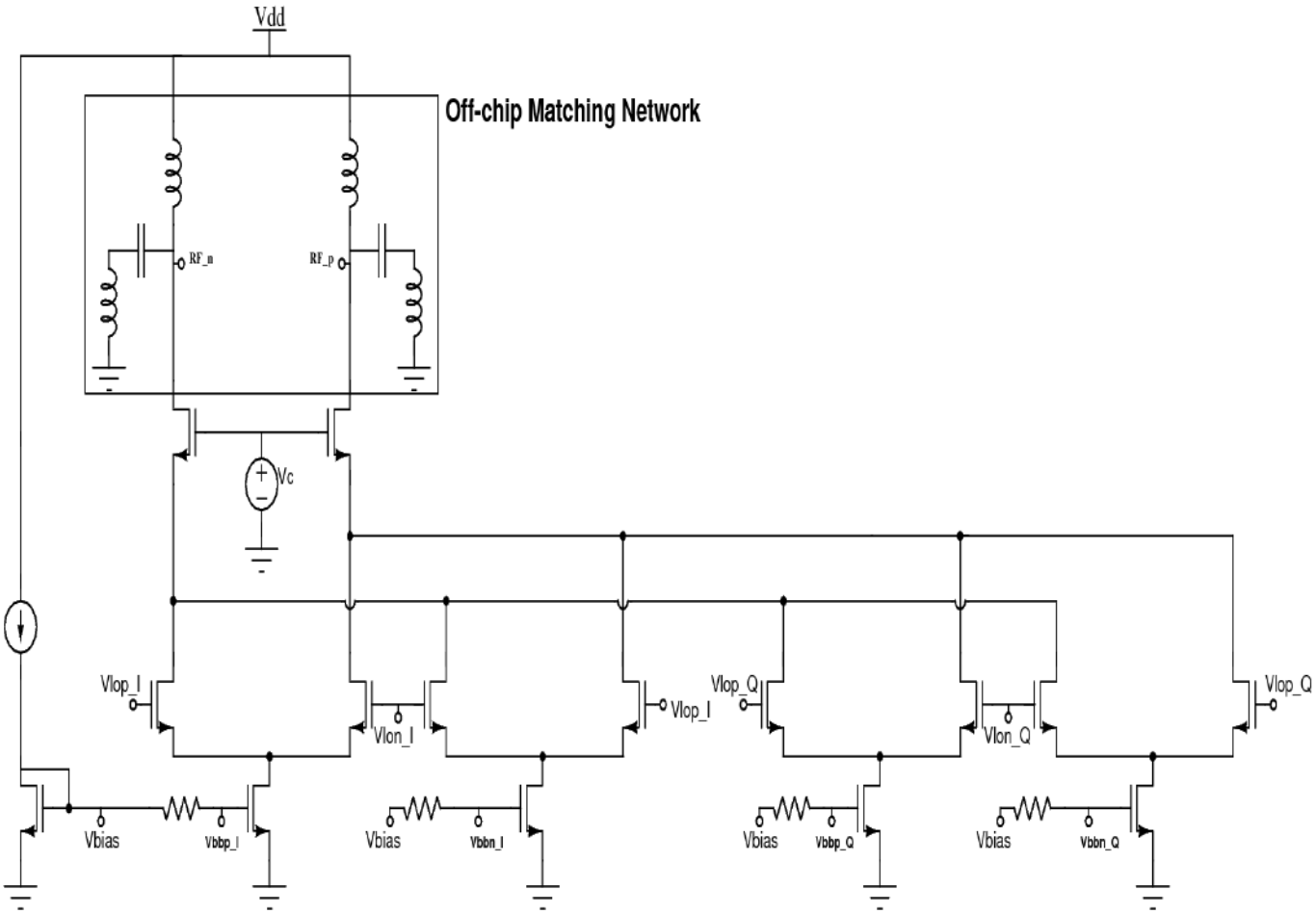

Figure 33: Power Mixer with Cascode NMOS

As discussed in the previous section, the high gate capacitance of the switching nmos made it impossible to design a LO-Buffer. To reduce this gate capacitance, we can use 1.2V nmos switching devices instead of 2.5V devices. To get the higher voltage swing at the output, a shielding cascode mnmos is used. It is a 2.5V device above the switching pairs and it's peak source voltage is kept less than 1.2V.

Voltage Biasing:

- The dc gate voltage of the switching nmos is kept at 0.6V. A sine wave with amplitude of 0.6V is applied to it.
- The cascode gate voltage is set to: $V_{ovswitch} + V_{gscascode}$
- Since, 2.5V nmos device can tolerate a maximum of 3V, the Vdd voltage is set to $(3 + V_{gcascode} - V_{th})/2$

  Explanation: The maximum Voltage at the drain of the cascode can be 3V and minimum voltage can be $V_{gcascode} - V_{th}$ to keep the nmos in saturation. For maximum amplitude, Vdd has to be the mean of the maximum and minimum voltages.

Device size and biasing:

Device	**Device Type**	**Size**	**Vov** ($V_g = 0.6$V)	I_d ($V_g = 0.6$V)
Cascode	2.5V nch	5400um/280nm	107.4mV	23.3mA
Switch	1.2V nch-lvt	440um/60nm	55mV	5mA
Transconductor	1.2V nch-lvt	1100um/300nm	87.54mV	10mA

Gate Bias Voltage:

Device	Gate Bias Voltage
Cascode	1.7V
Switch	0.6V
Transconductor	267mV

Vdd = 2.06V

$R_{load} = 50\Omega$

Power Consumed = 200mW

Results:

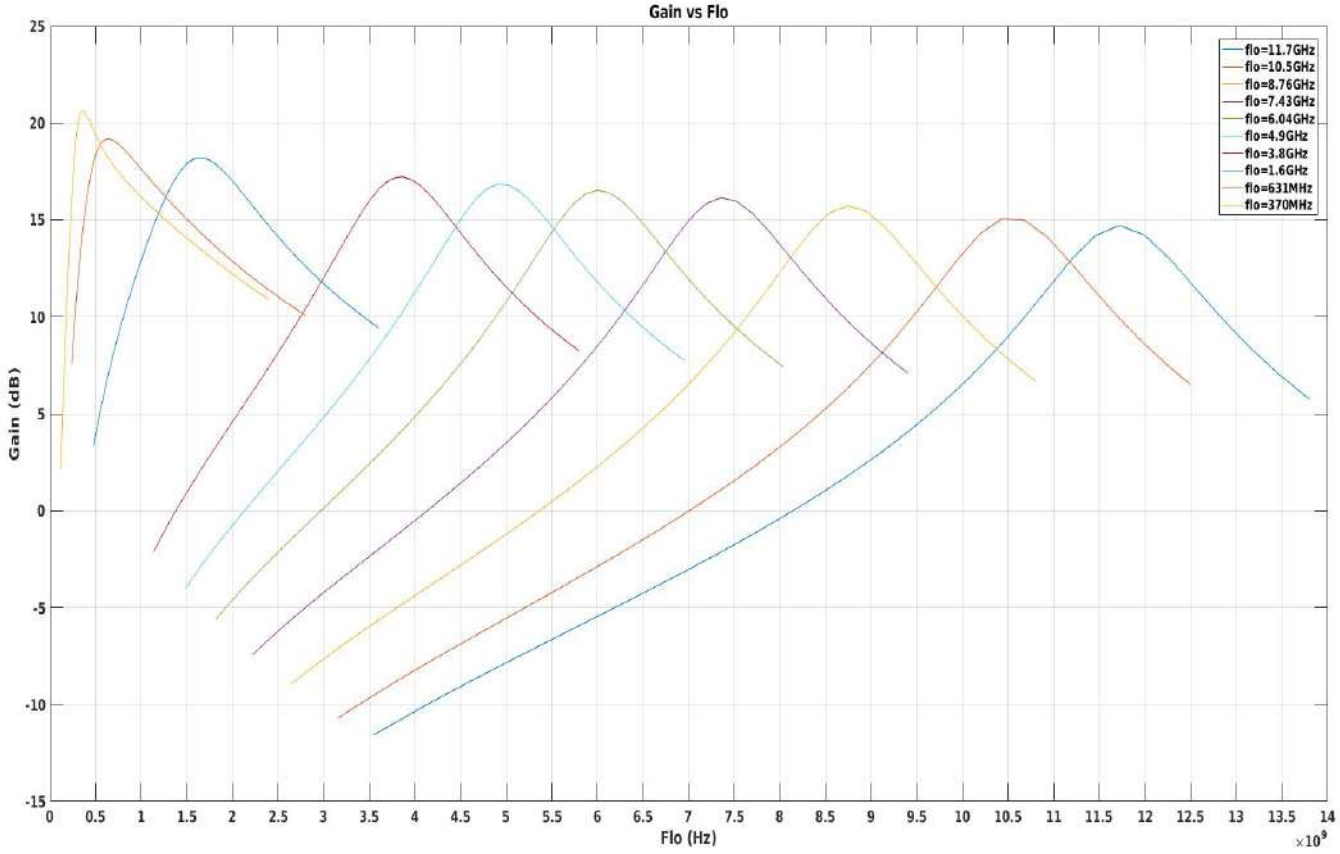

Figure 34: Power Mixer with Cascode: Gain vs Flo

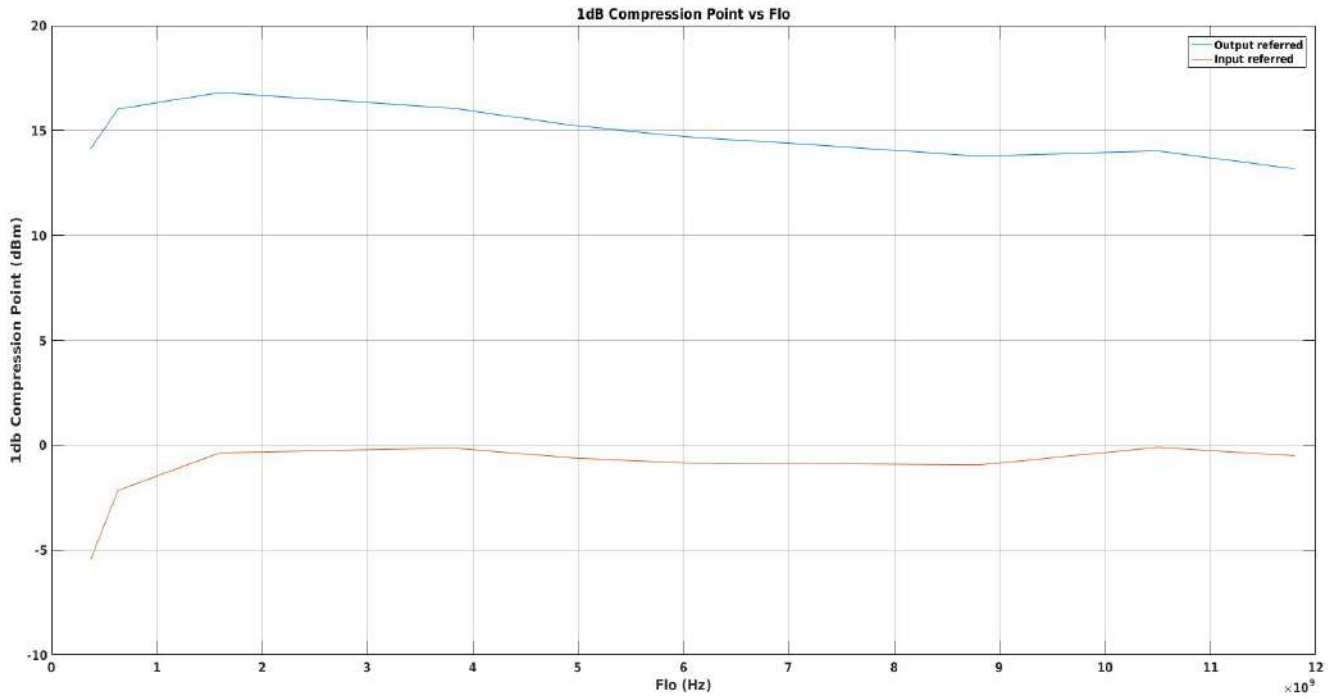

Figure 35: Power Mixer with Cascode: Output Power Compression vs Flo

It is observed that the gain and output power compression point reduces with the increase in frequency. It's because, part of the signal current is lost through C_{db} of the switching device. So, as the frequency of signal increases, the current loss increases and the output power compression point and conversion gain falls.

4.3 LO-Buffer and Power Mixer

The LO-Buffer designed is a single stage common source amplifier with inductor peaking(for higher BW). The output node was biased at 0.6V. This removes the need of a coupling capacitor between the LO-Buffer and the Mixer. The devices used are standard 1.2V devices. The V_{dd} of the buffer set to 1.2V with peak-to-peak output swing 1.1V. To drive the Power Mixer till 12GHz, the load resistance is set to 25Ω and the peaking inductor has an inductance of 120pH. A CMOS NOT gate wasn't used as LO-Buffers due to BW constraints. Multistage Lo-Buffers were avoided to minimise LO-Phase mismatches.

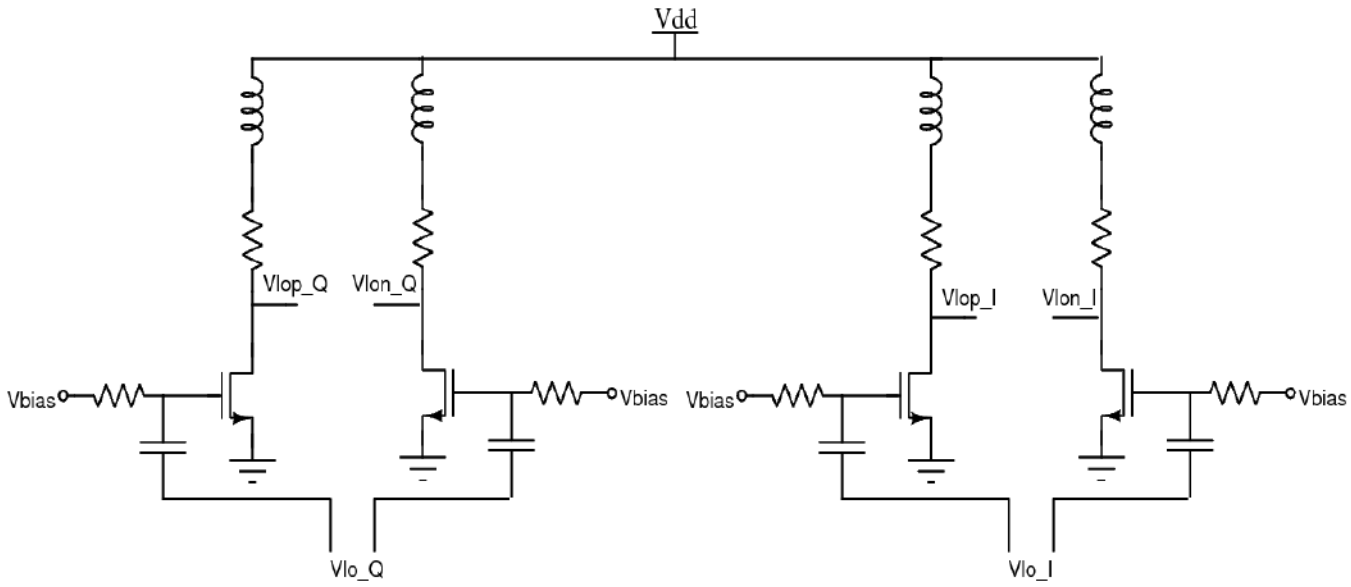

Figure 36: LO-Buffer for Power Mixer

Circuit Diagram of Power Mixer:

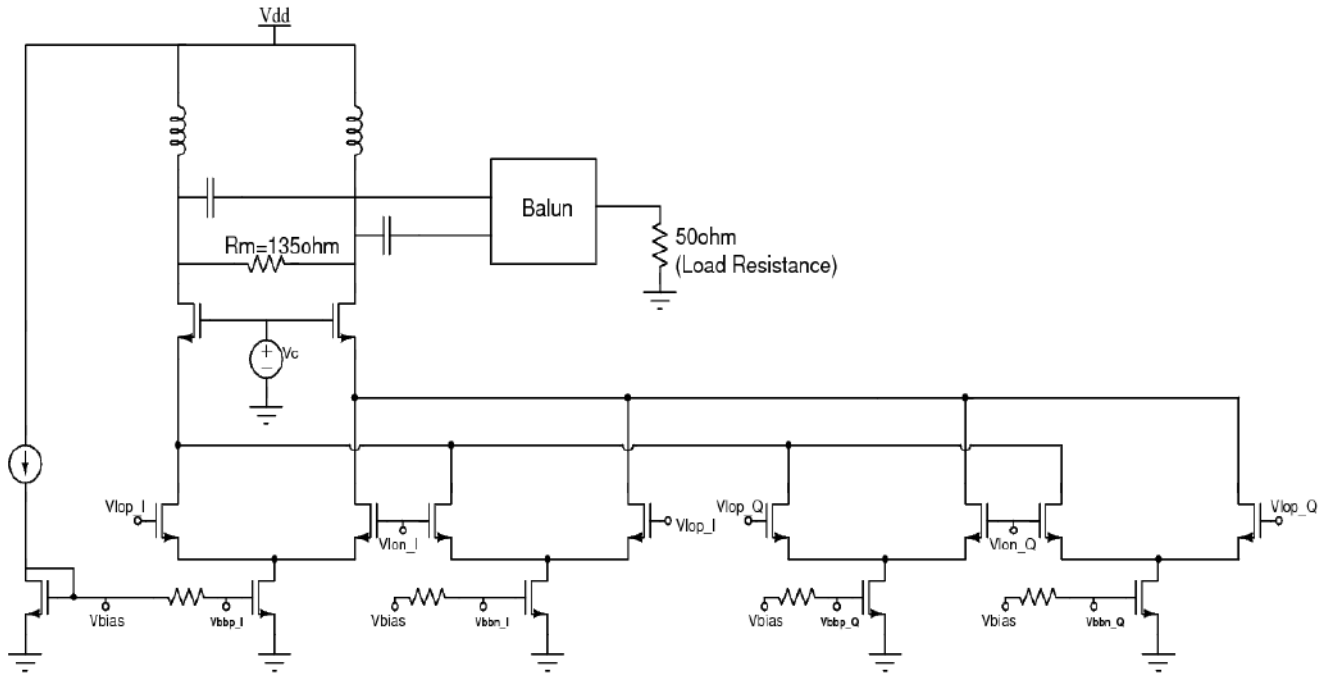

Figure 37: Power Mixer with output matching

A 2:1 Balun was used at the output to convert differential ended output to single ended output which would drive 50Ω load directly. To improve output impedance matching, a Resistor $R_m = 135\Omega$ was added to the circuit.

Results:

The LO-Buffer was connect to the Power Mixer and the gain was plotted for various values of Inductor in power mixer to get the necessary BW.

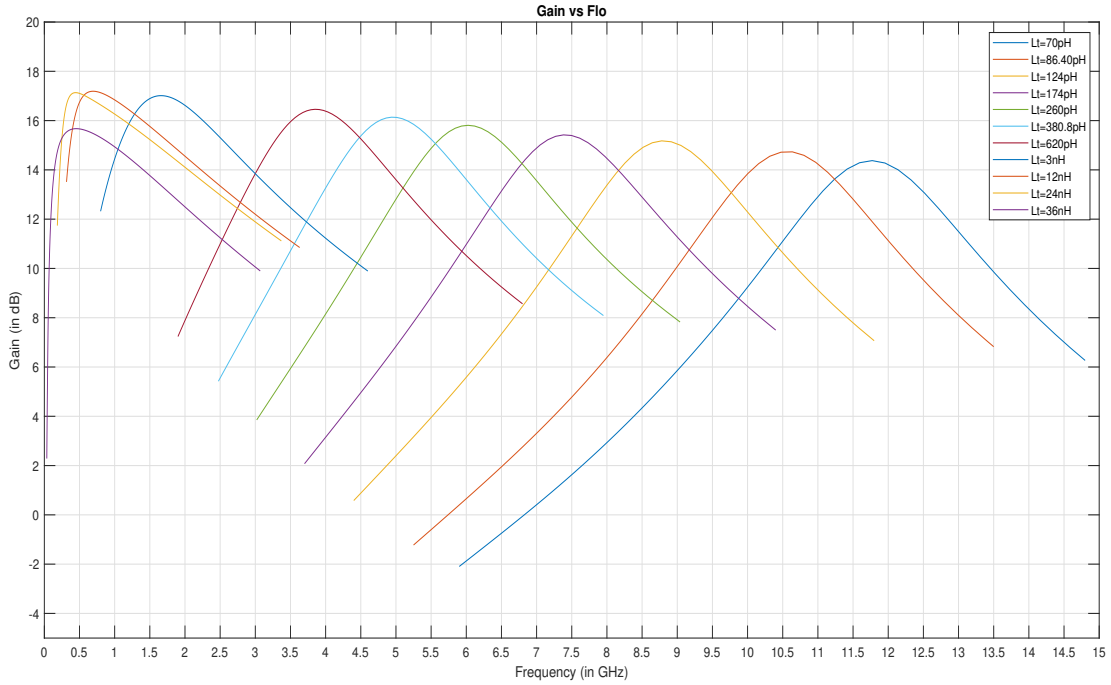

Figure 38: Power Mixer Gain vs Flo with LO-Buffer

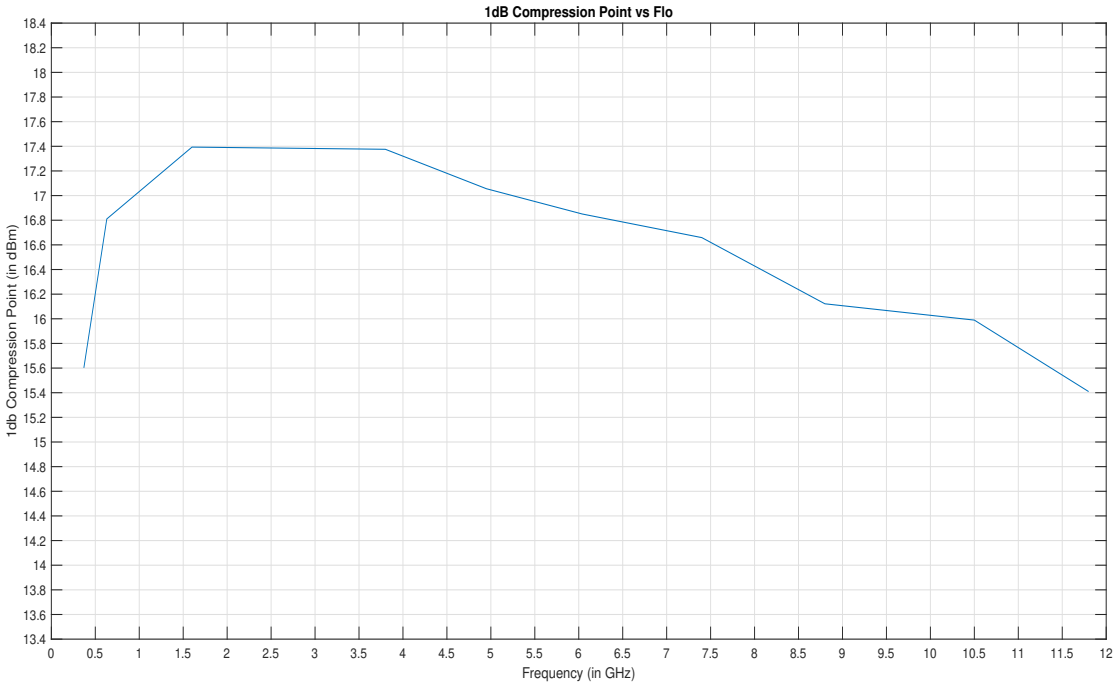

Figure 39: Power Mixer 1dB Compression vs Flo with LO-Buffer

4.4 PVT Variation and Mismatch analysis

To check the robustness of the circuit, PVT Variation and Mismatch analysis was performed. The circuit was tested at 5 frequencies across various corners and the results are documented below:

At Flo=11.72GHz:

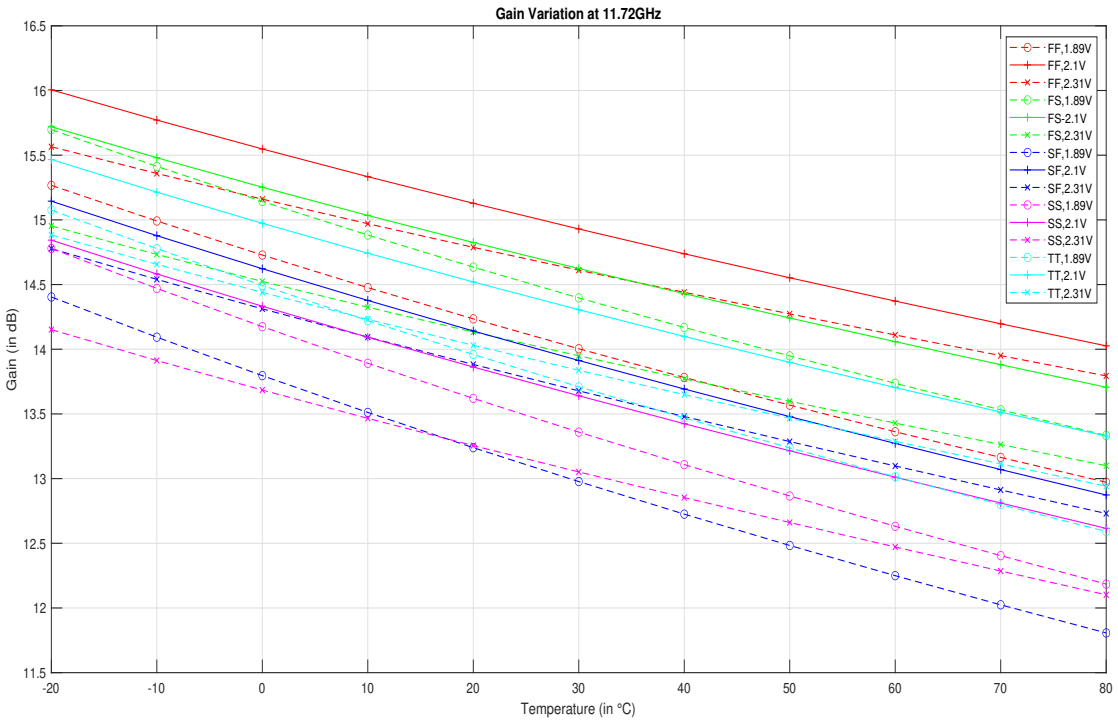

Figure 40: Effect of PVT Variation on Gain at 11.72GHz

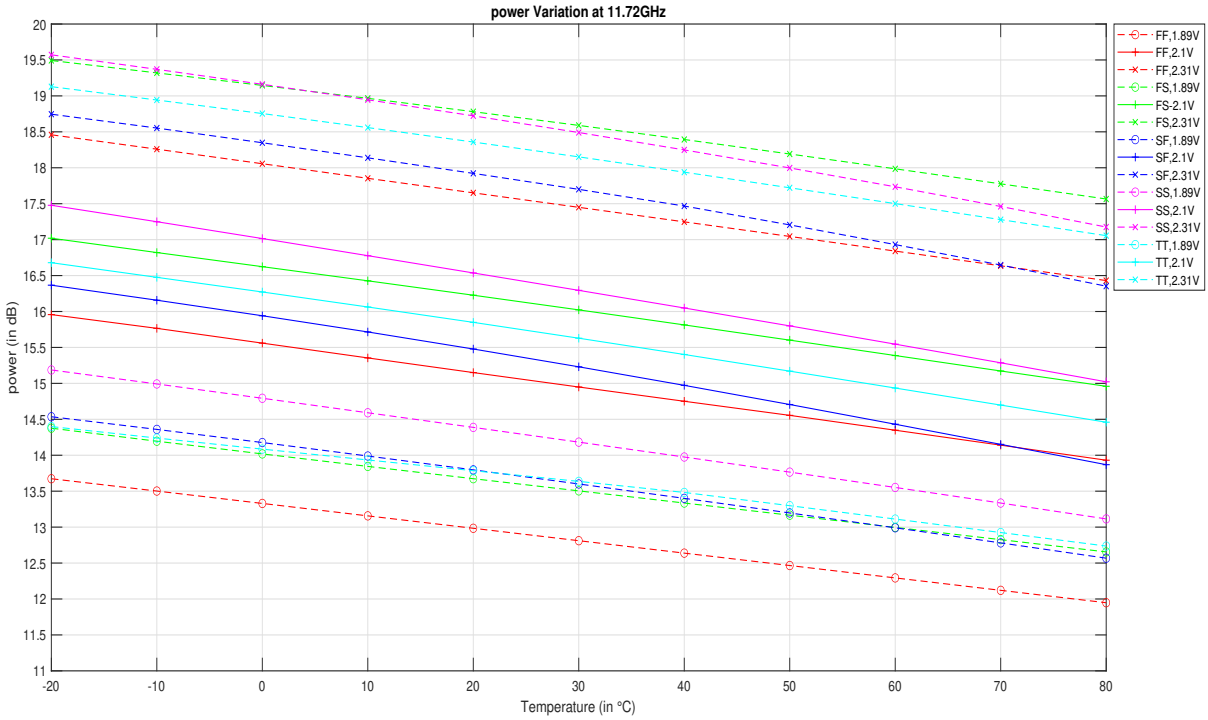

Figure 41: Effect of PVT Variation on Output Compression at 11.72GHz

At Flo=8.78GHz:

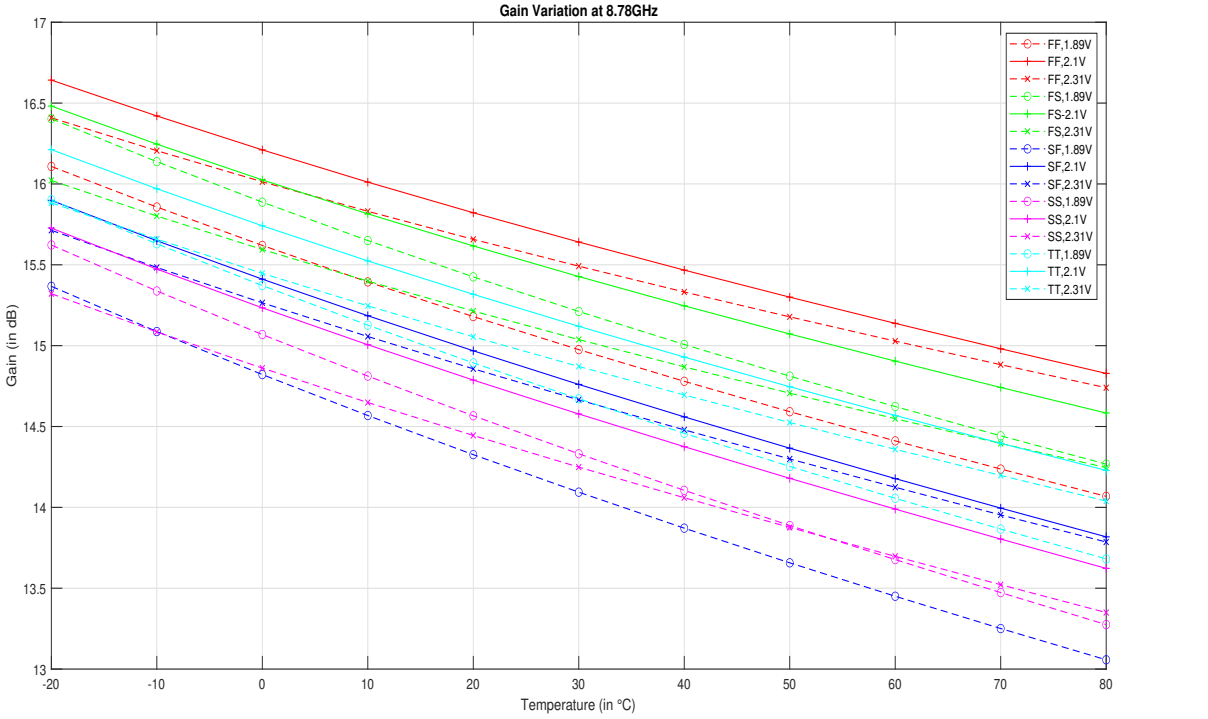

Figure 42: Effect of PVT Variation on Gain at 8.78GHz

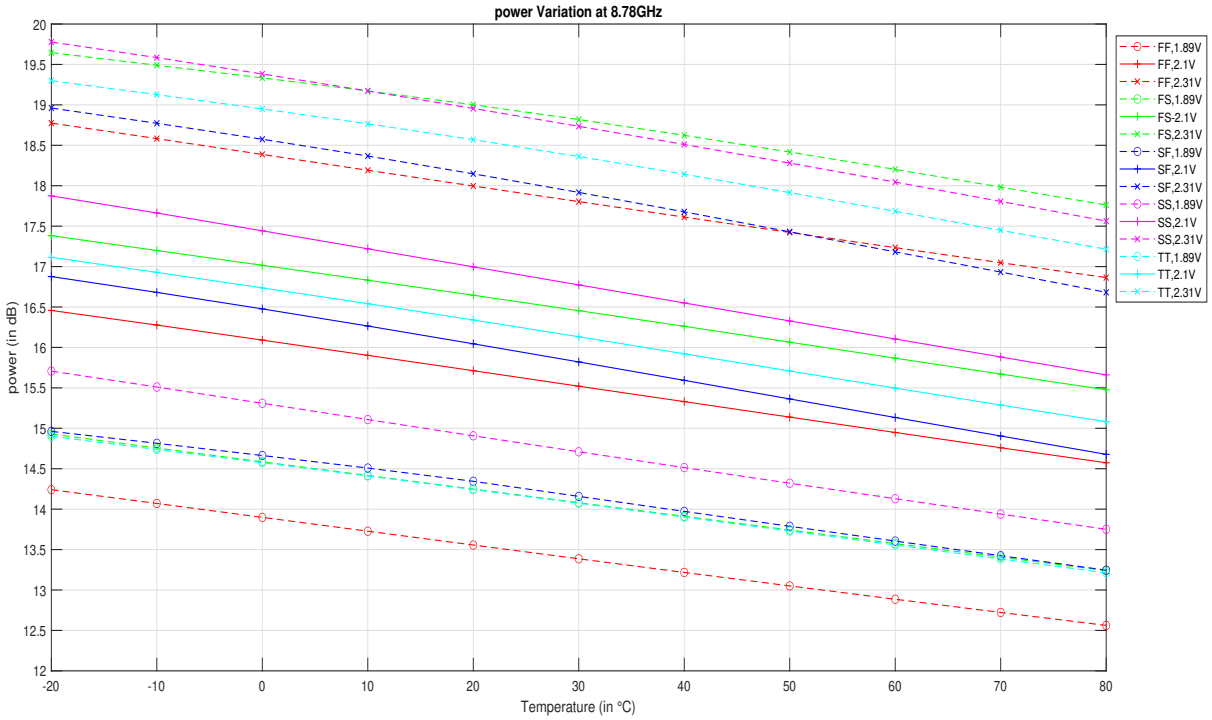

Figure 43: Effect of PVT Variation on Output Compression at 8.78GHz

At Flo=6.12GHz:

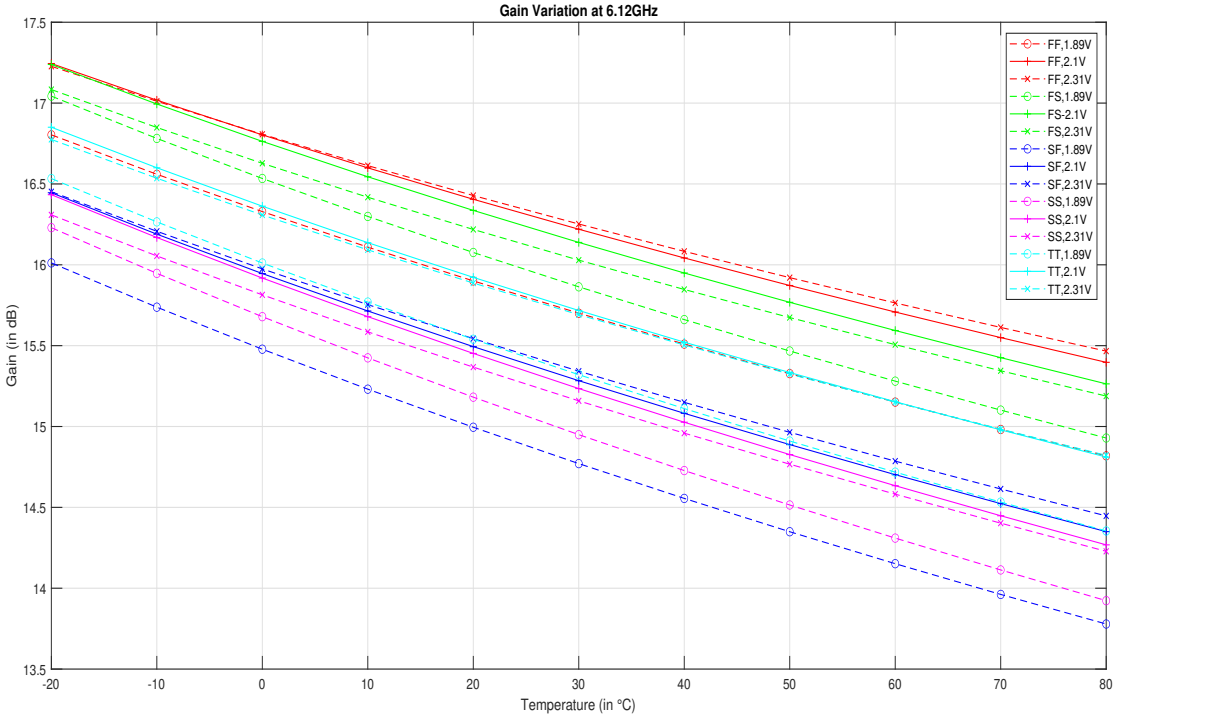

Figure 44: Effect of PVT Variation on Gain at 6.12GHz

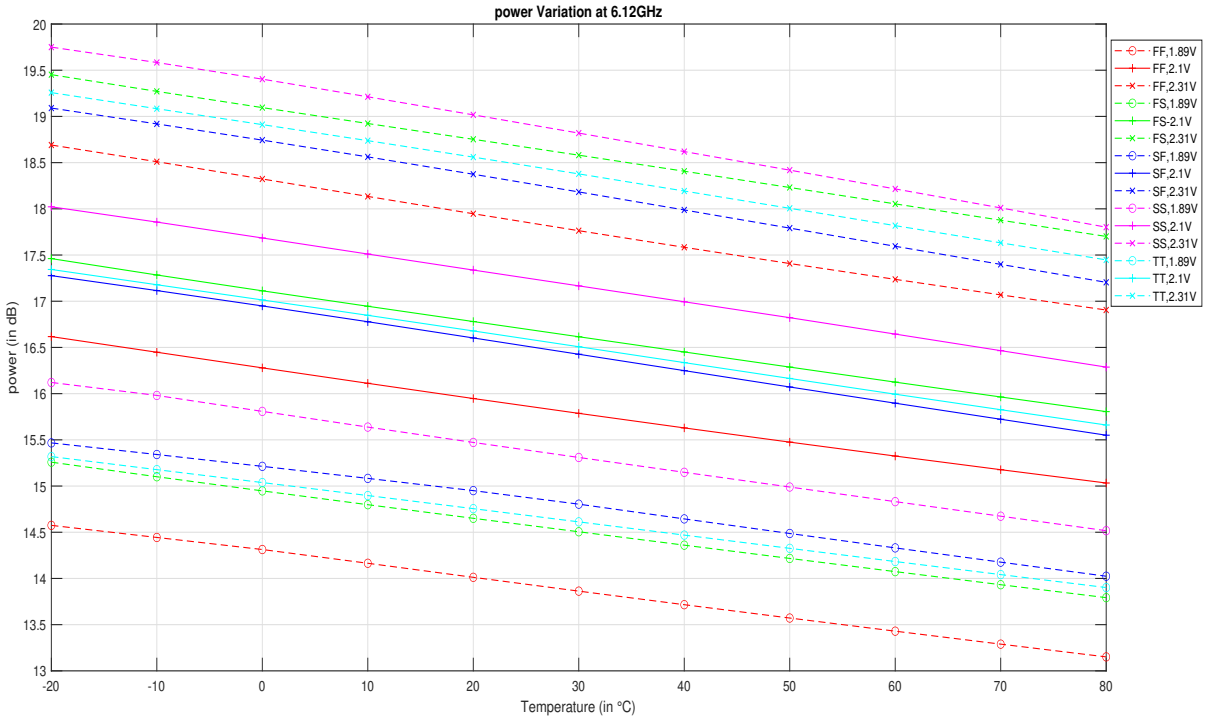

Figure 45: Effect of PVT Variation on Output Compression at 6.12GHz

At Flo=3.91GHz:

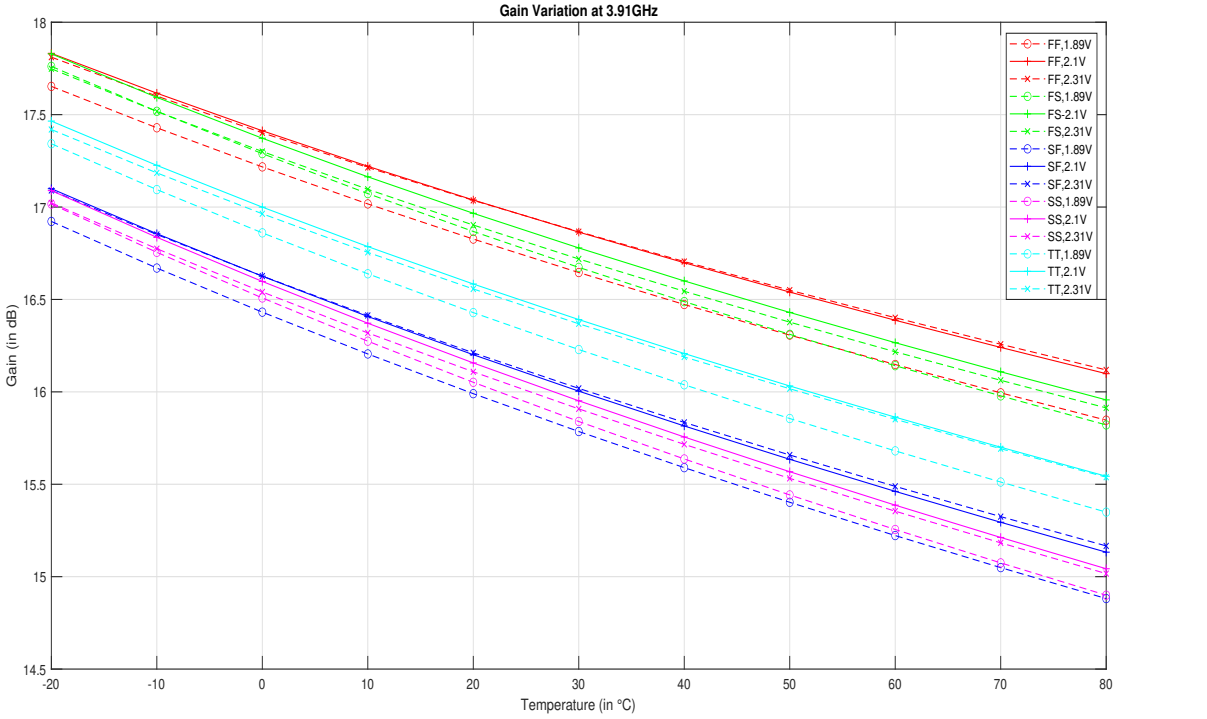

Figure 46: Effect of PVT Variation on Gain at 3.91GHz

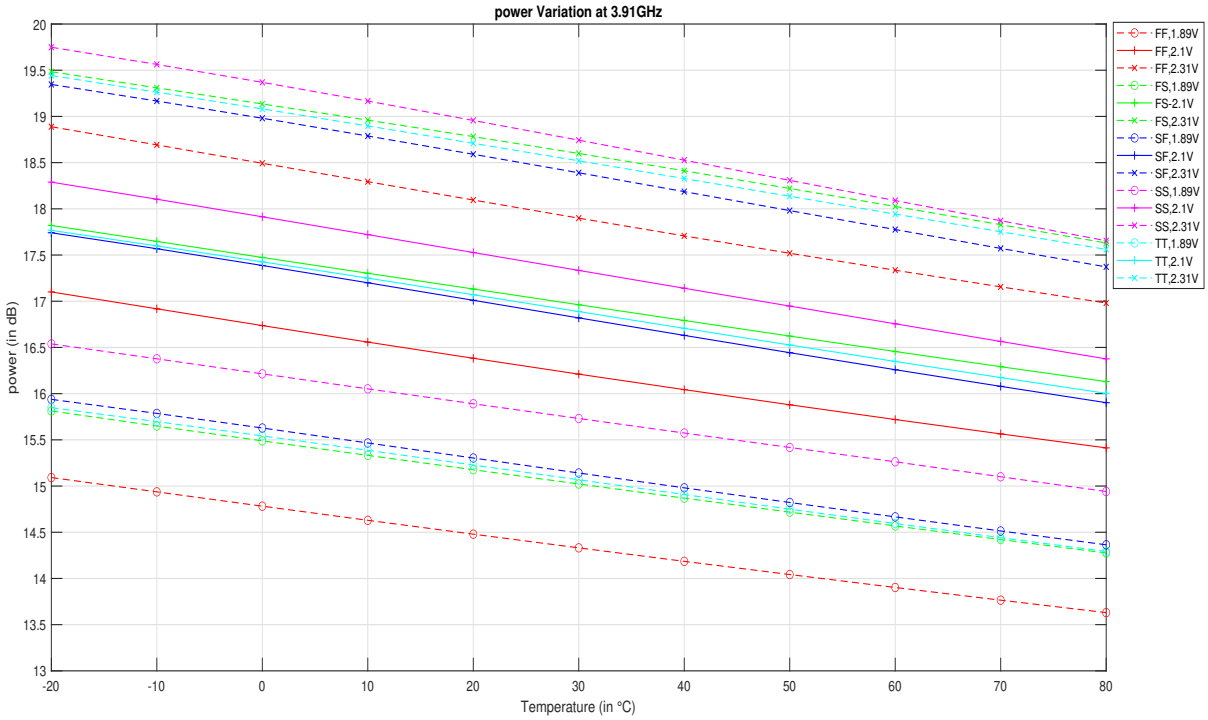

Figure 47: Effect of PVT Variation on Output Compression at 3.91GHz

At Flo=680MHz:

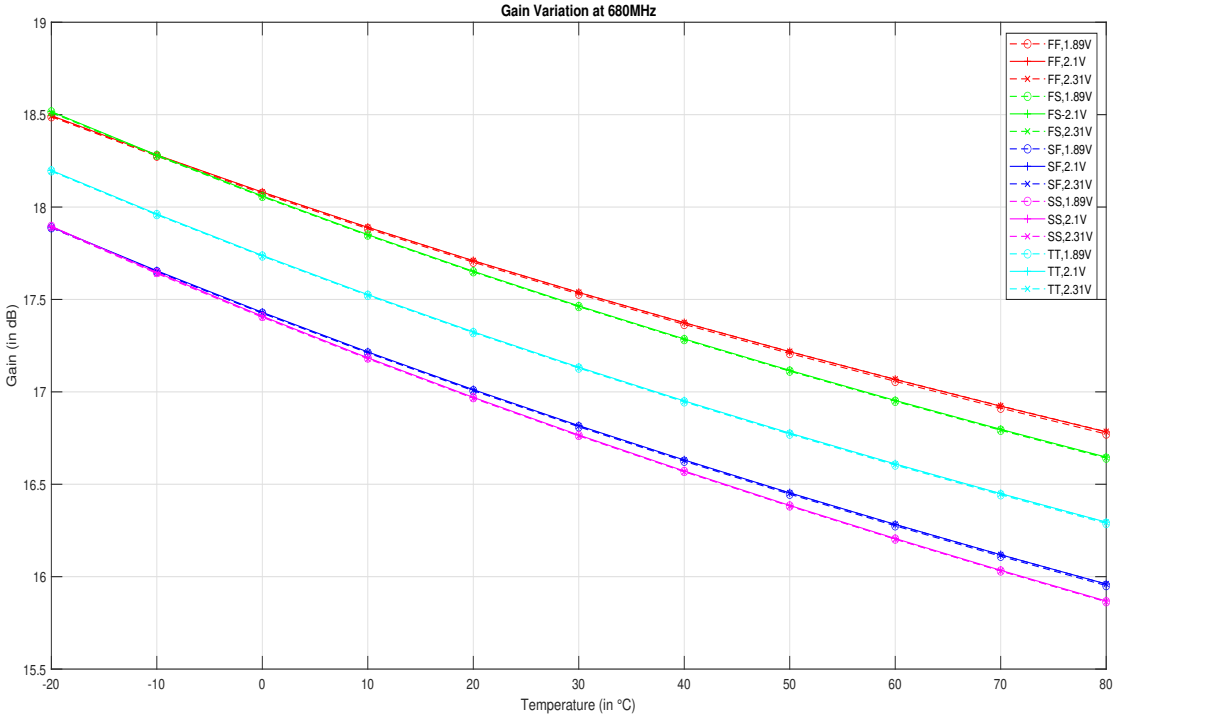

Figure 48: Effect of PVT Variation on Gain at 680MHz

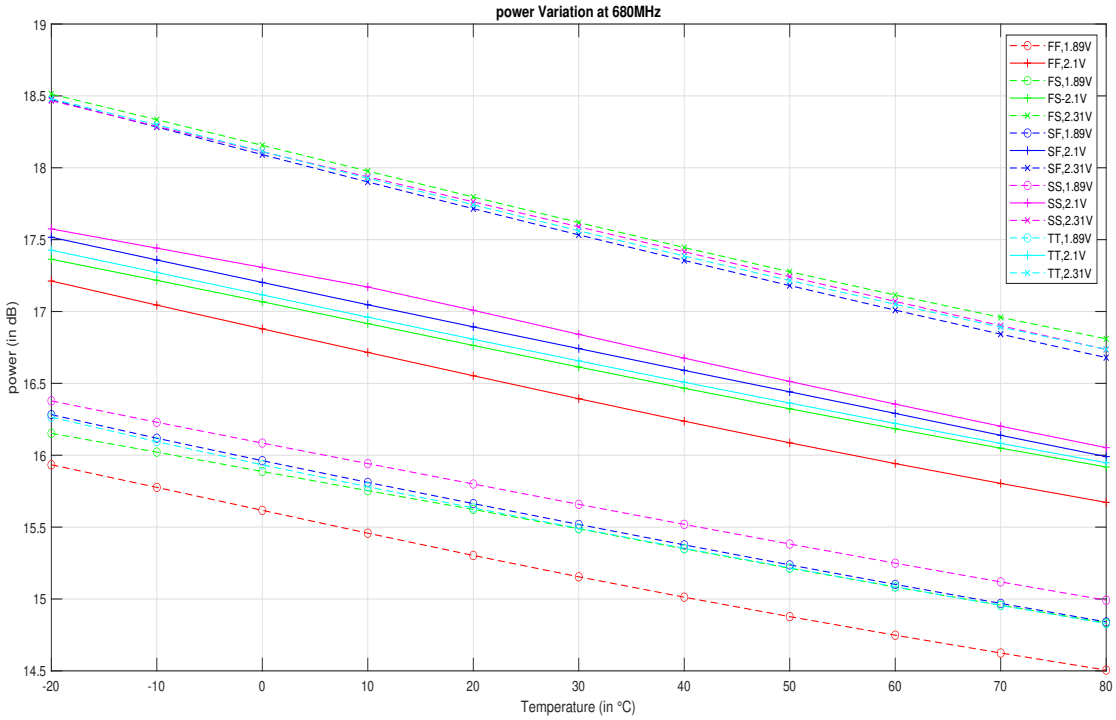

Figure 49: Effect of PVT Variation on Output Compression at 680MHz

Mismatch:

At Flo=11.72GHz:

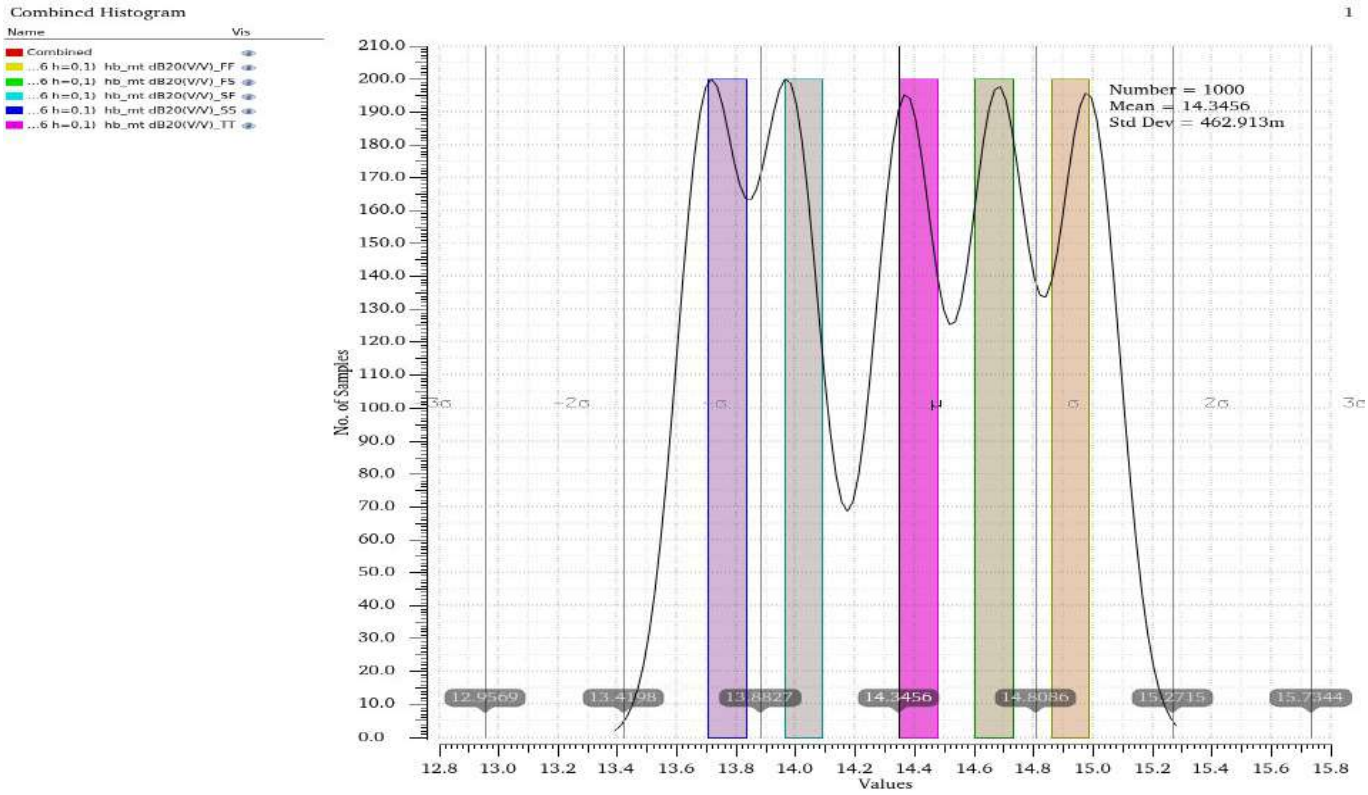

Figure 50: Mismatch Variation in Gain at 11.72GHz

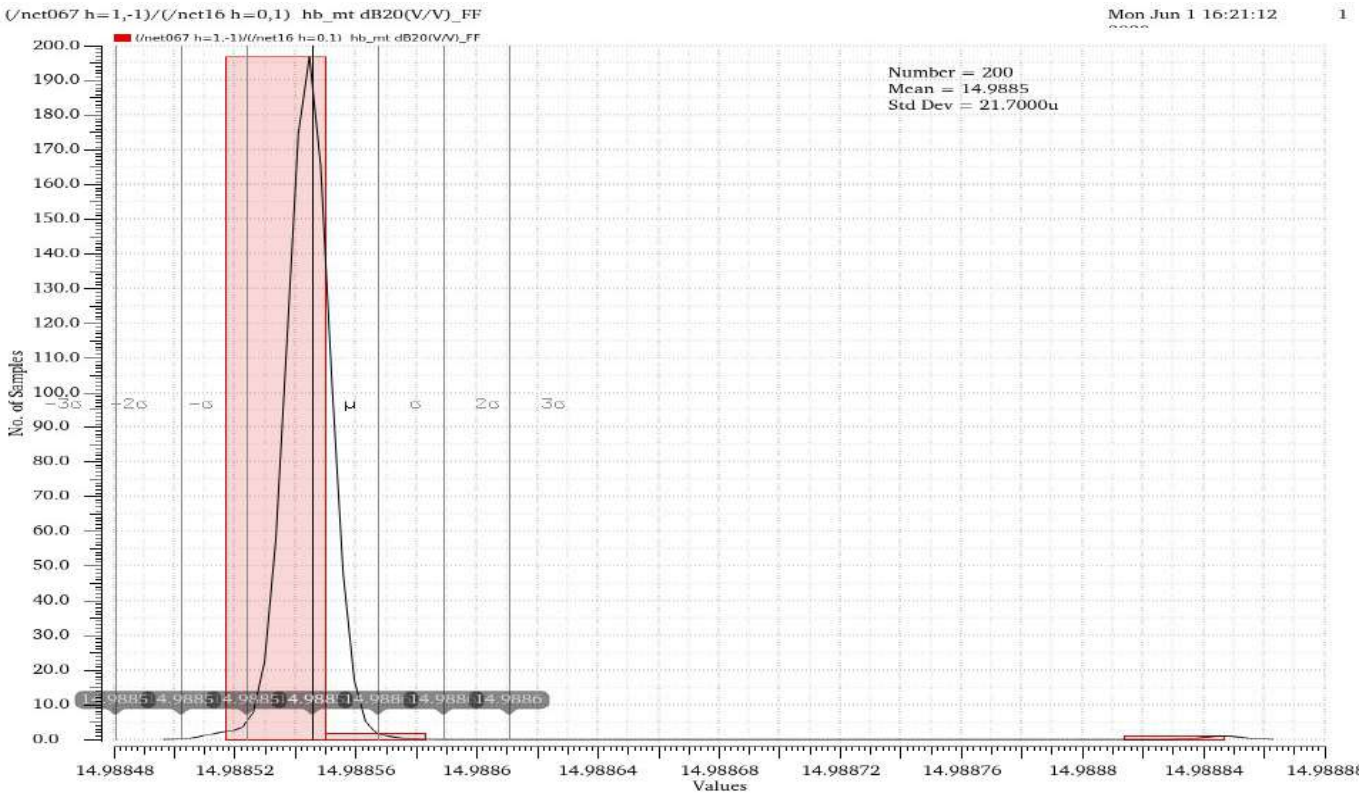

Figure 51: Mismatch Variation in Gain at 11.72GHz (FF corner)

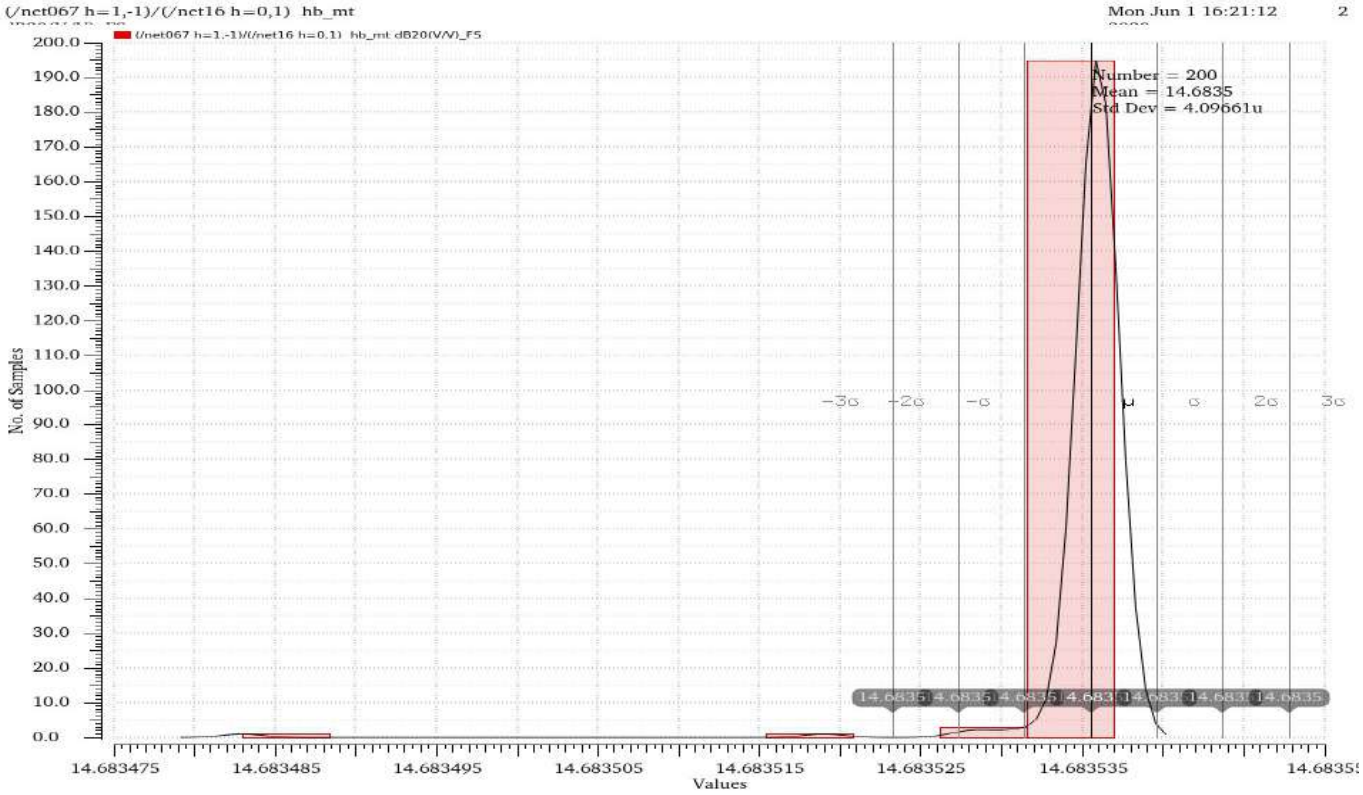

Figure 52: Mismatch Variation in Gain at 11.72GHz (FS corner)

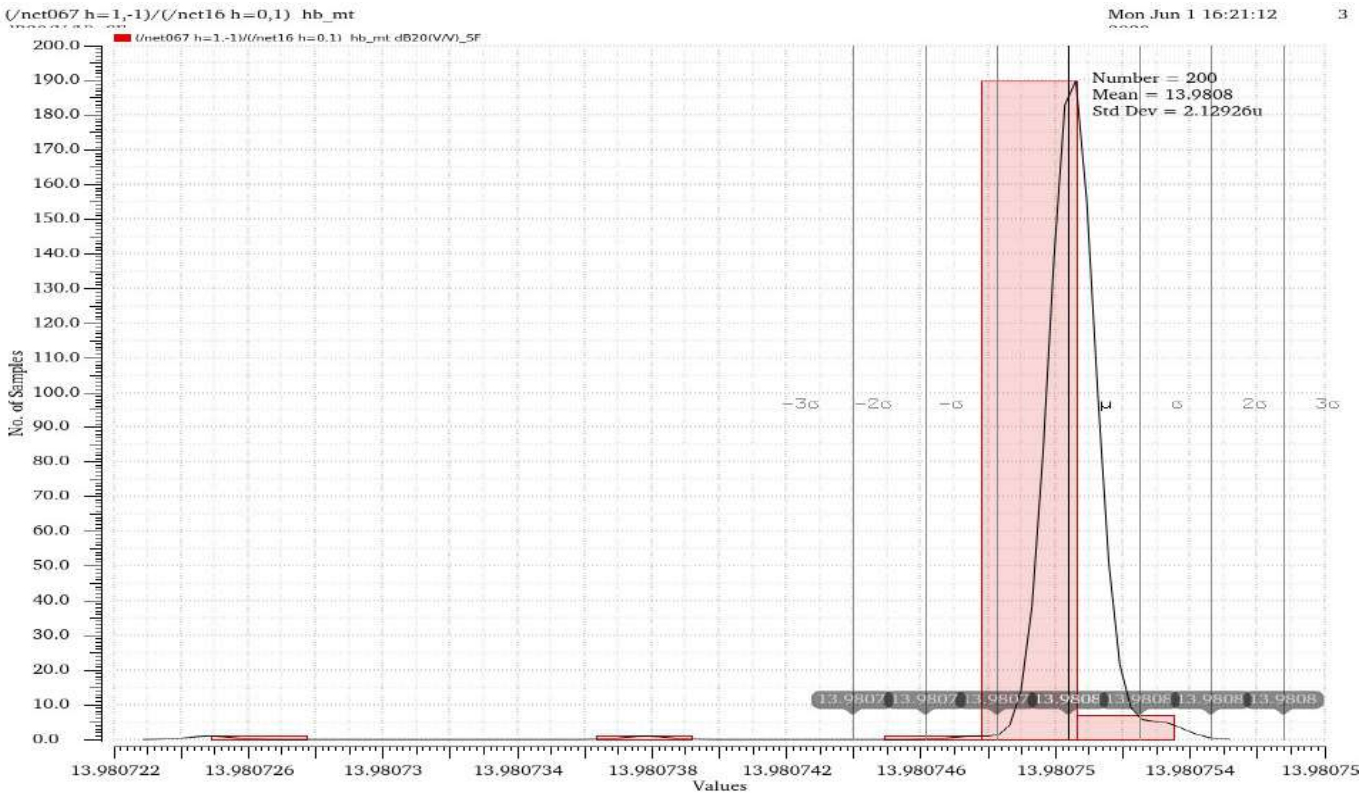

Figure 53: Mismatch Variation in Gain at 11.72GHz (SF corner)

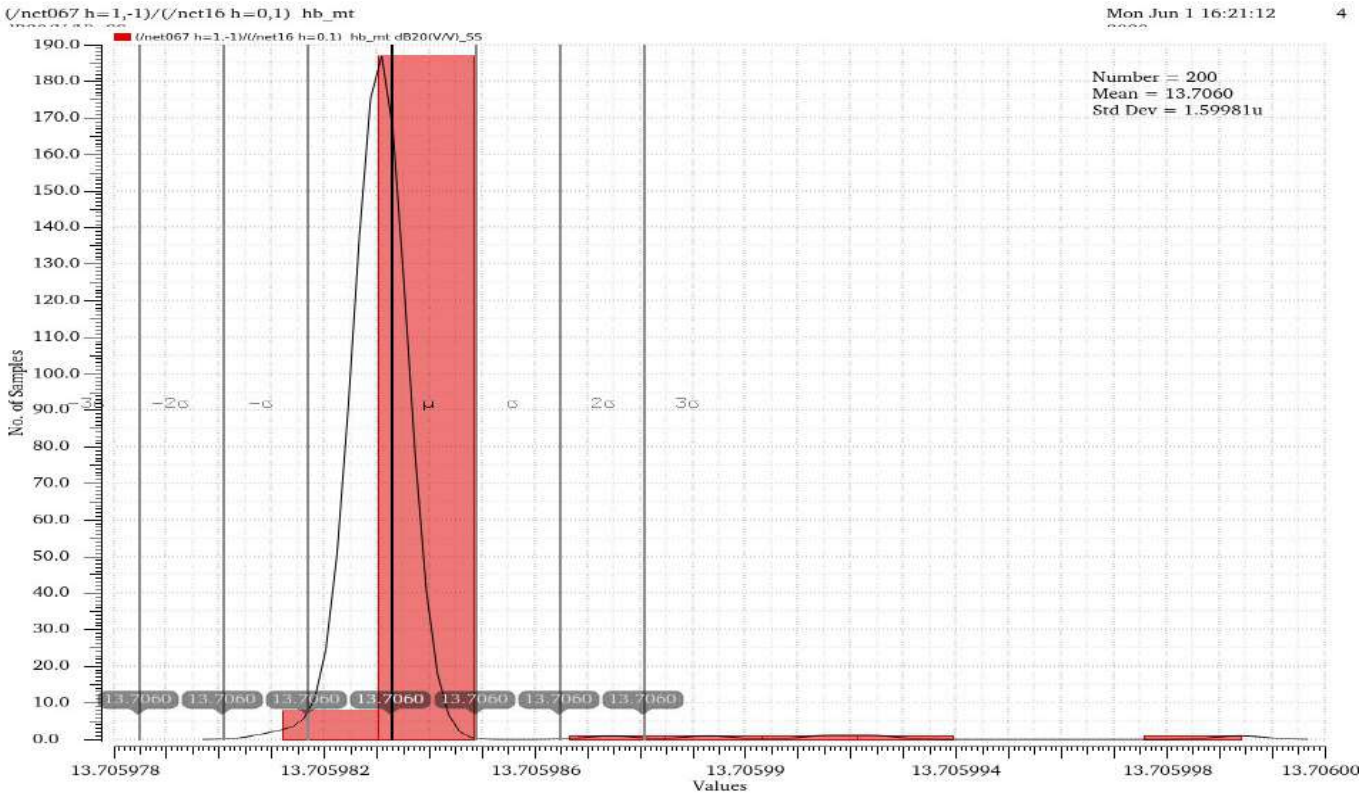

Figure 54: Mismatch Variation in Gain at 11.72GHz (SS corner)

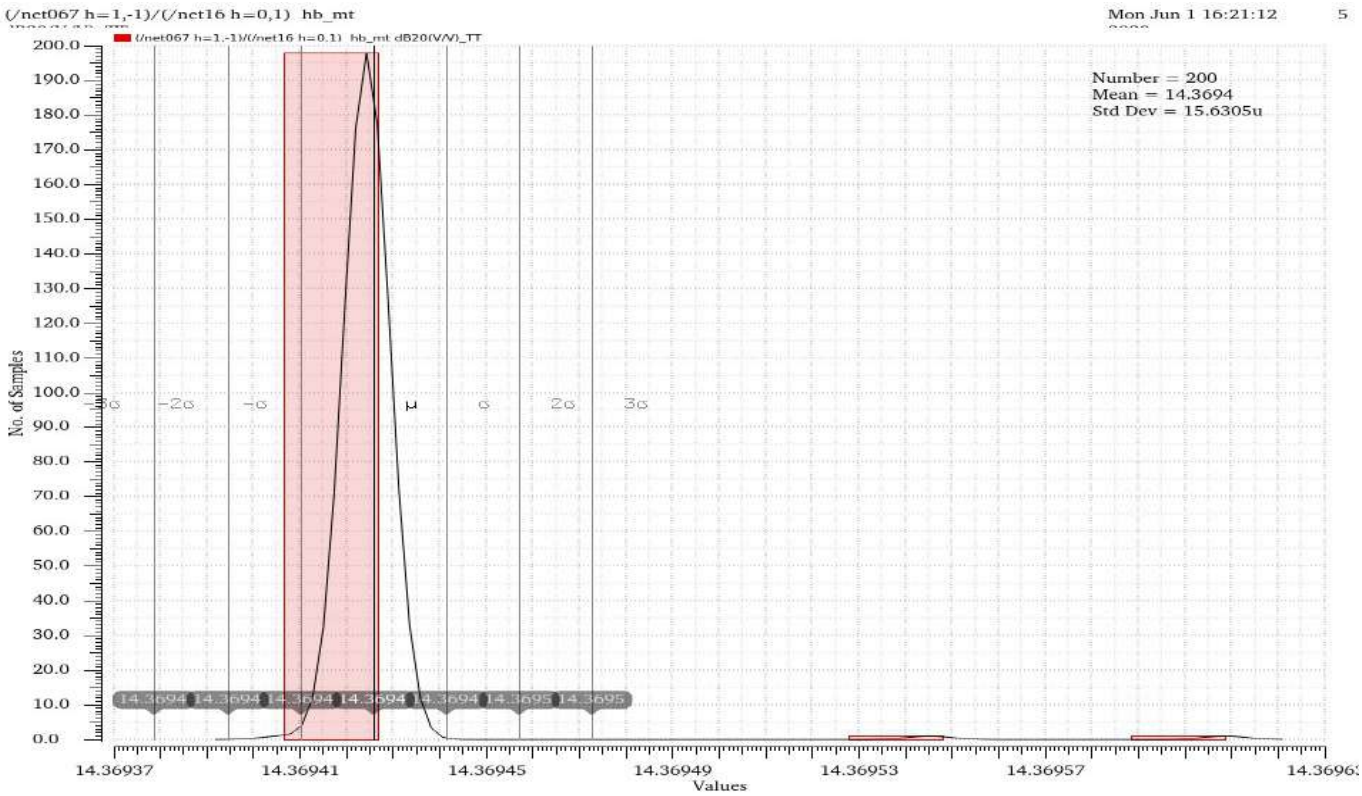

Figure 55: Mismatch Variation in Gain at 11.72GHz (TT corner)

At Flo=8.78GHz:

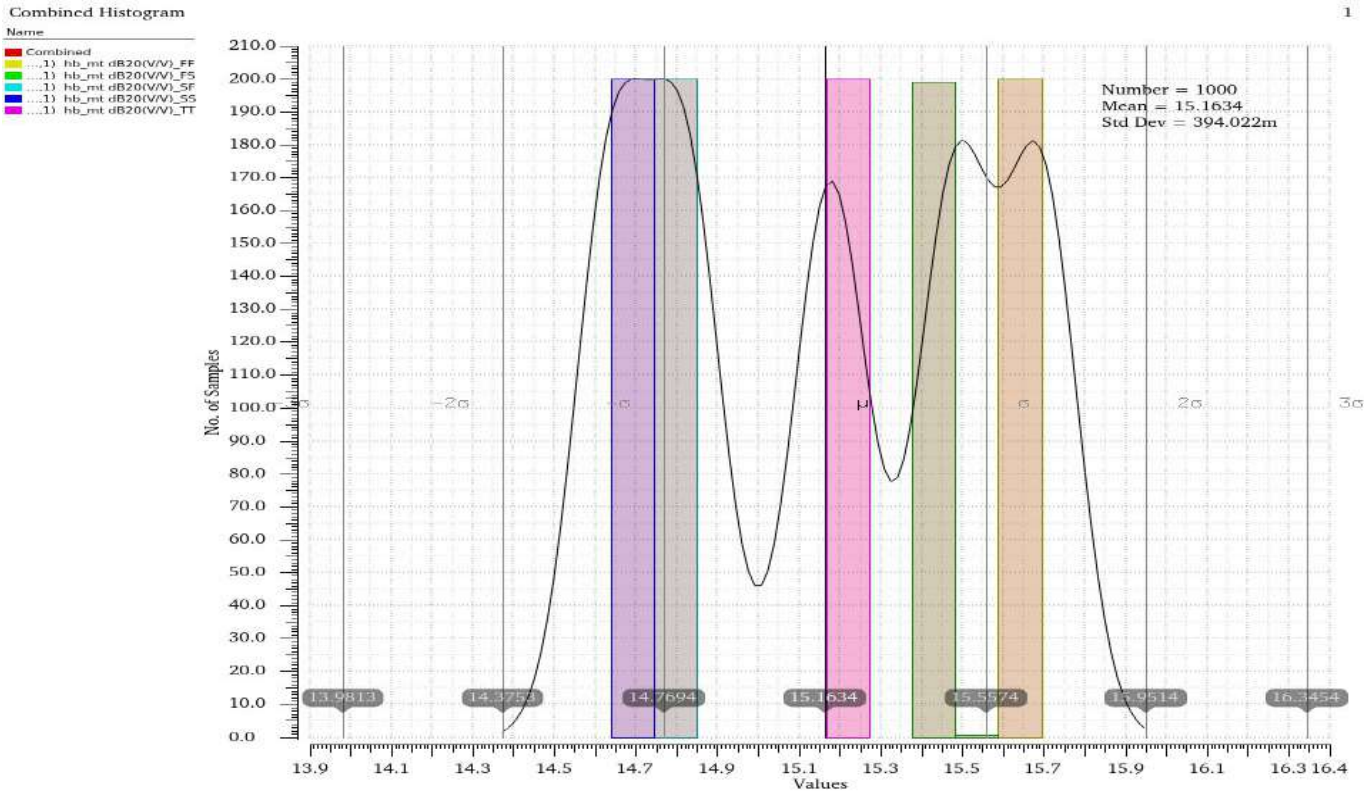

Figure 56: Mismatch Variation in Gain at 8.78GHz

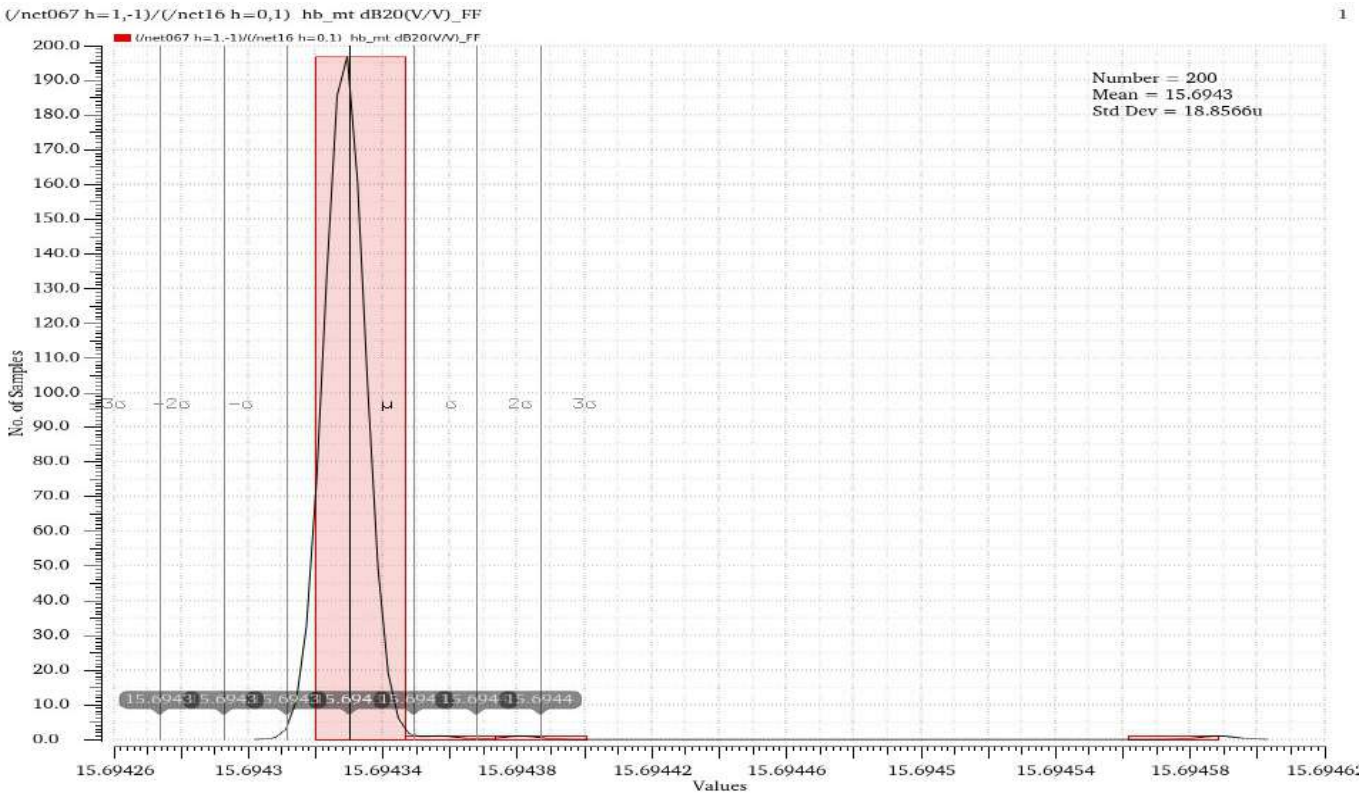

Figure 57: Mismatch Variation in Gain at 8.78GHz (FF corner)

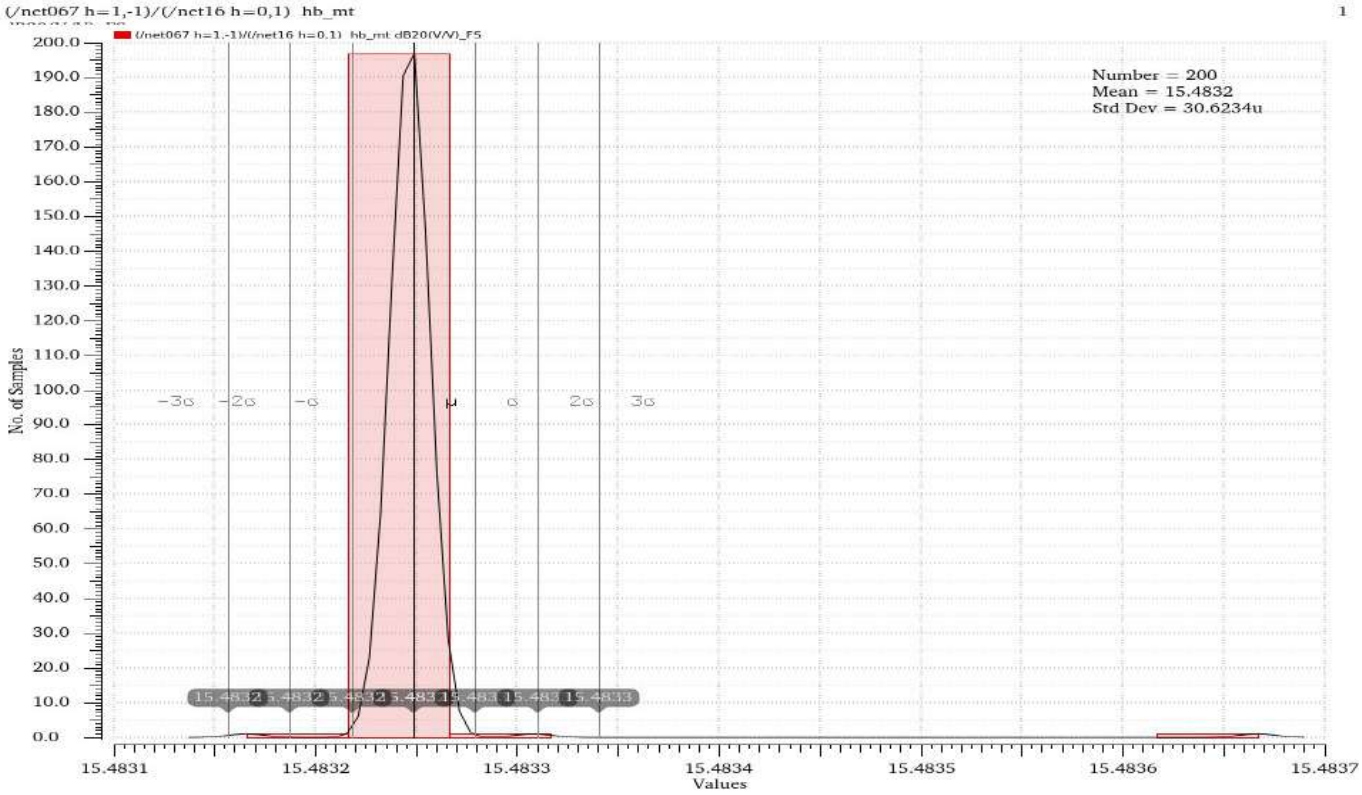

Figure 58: Mismatch Variation in Gain at 8.78GHz (FS corner)

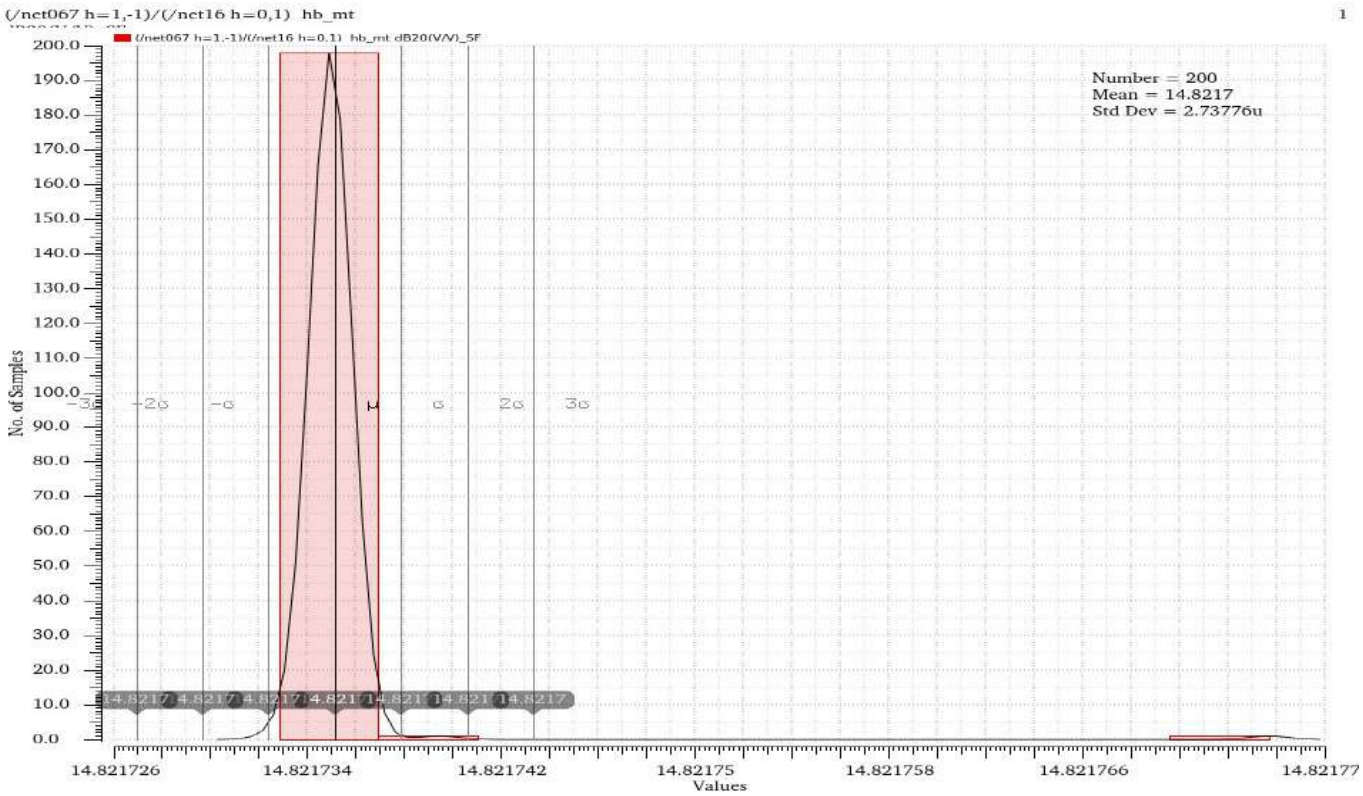

Figure 59: Mismatch Variation in Gain at 8.78GHz (SF corner)

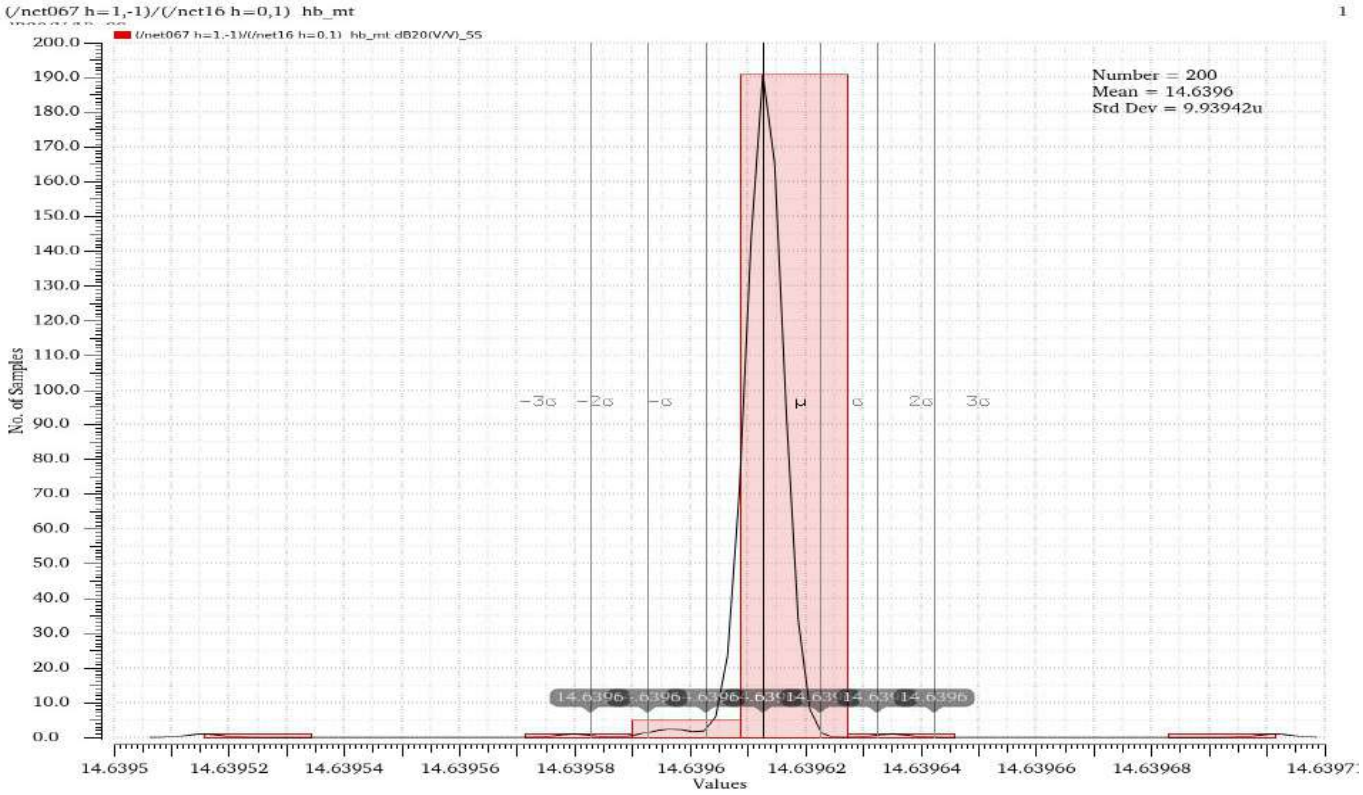

Figure 60: Mismatch Variation in Gain at 8.78GHz (SS corner)

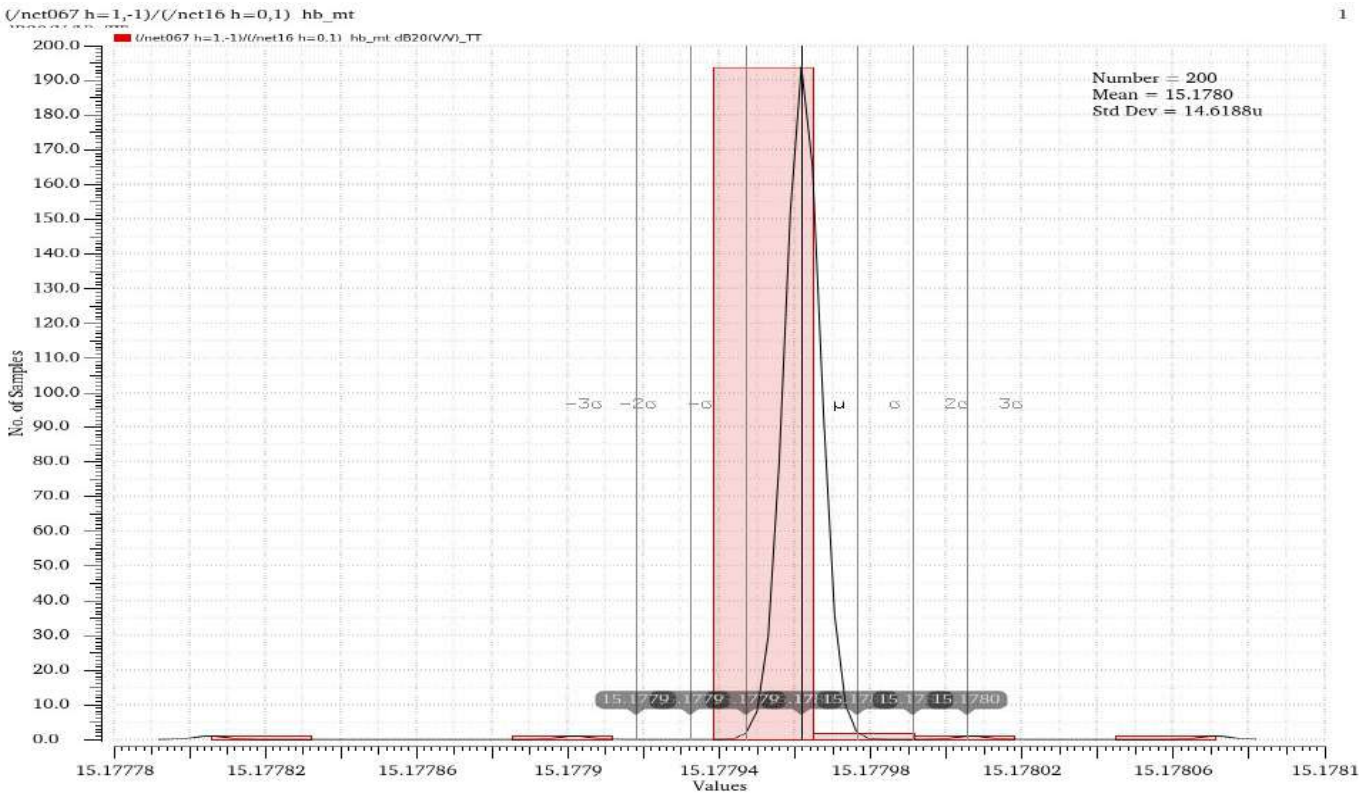

Figure 61: Mismatch Variation in Gain at 8.78GHz (TT corner)

At Flo=6.12GHz:

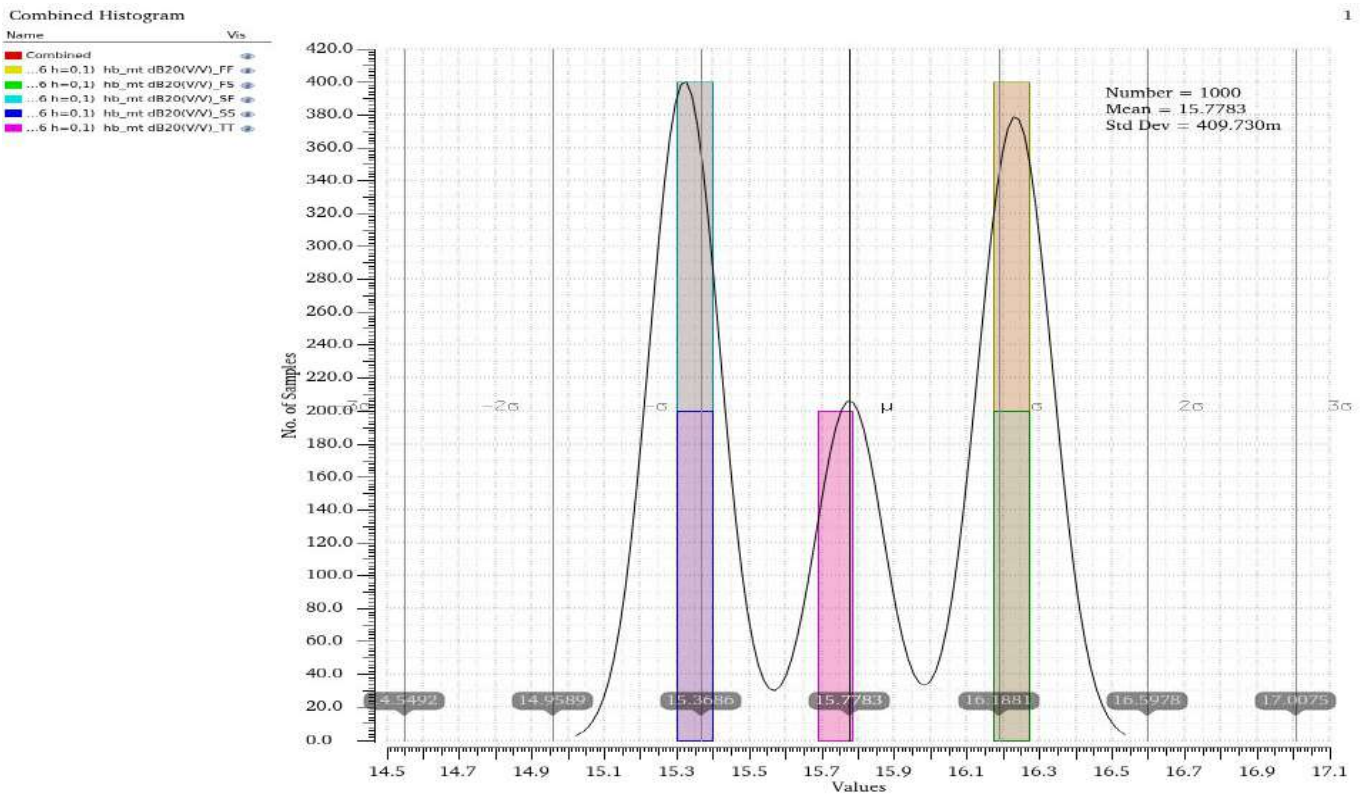

Figure 62: Mismatch Variation in Gain at 6.12GHz

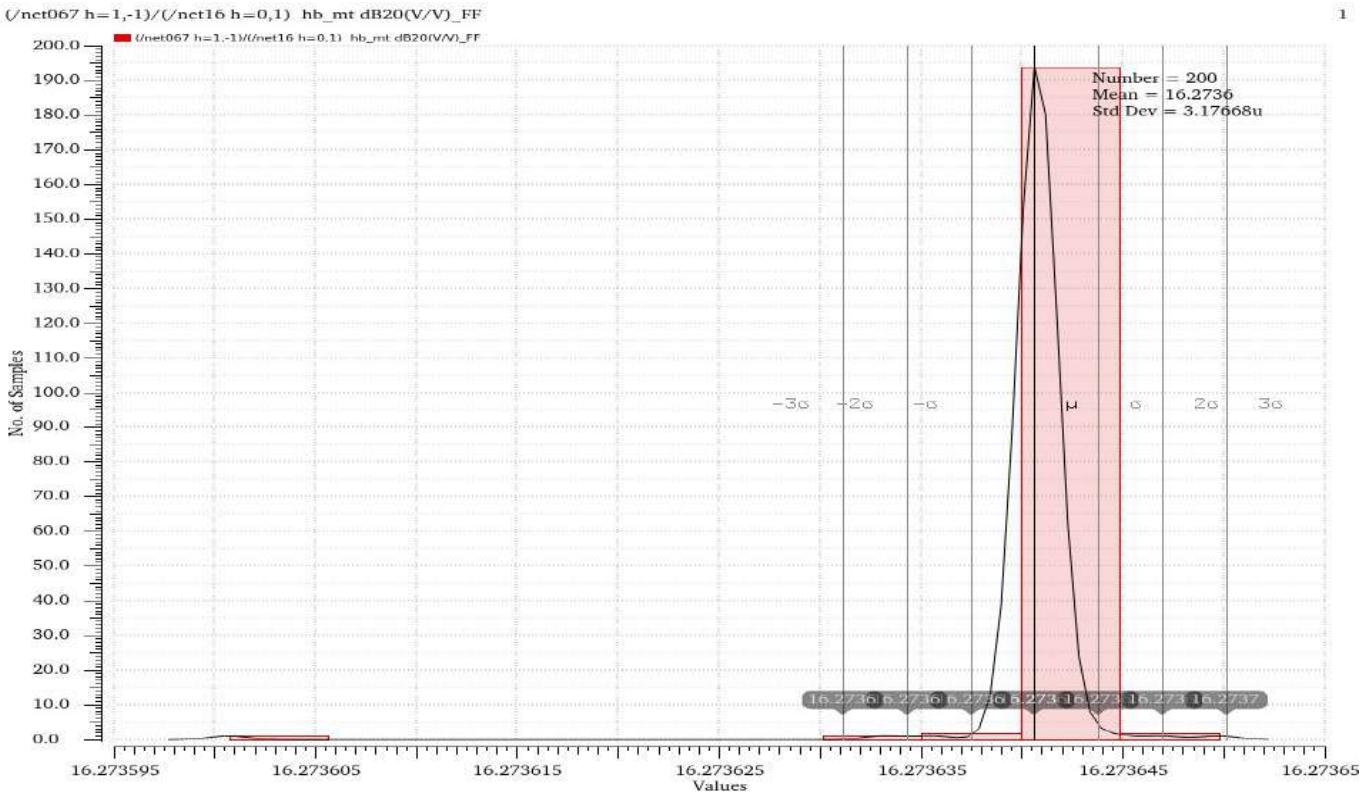

Figure 63: Mismatch Variation in Gain at 6.12GHz (FF corner)

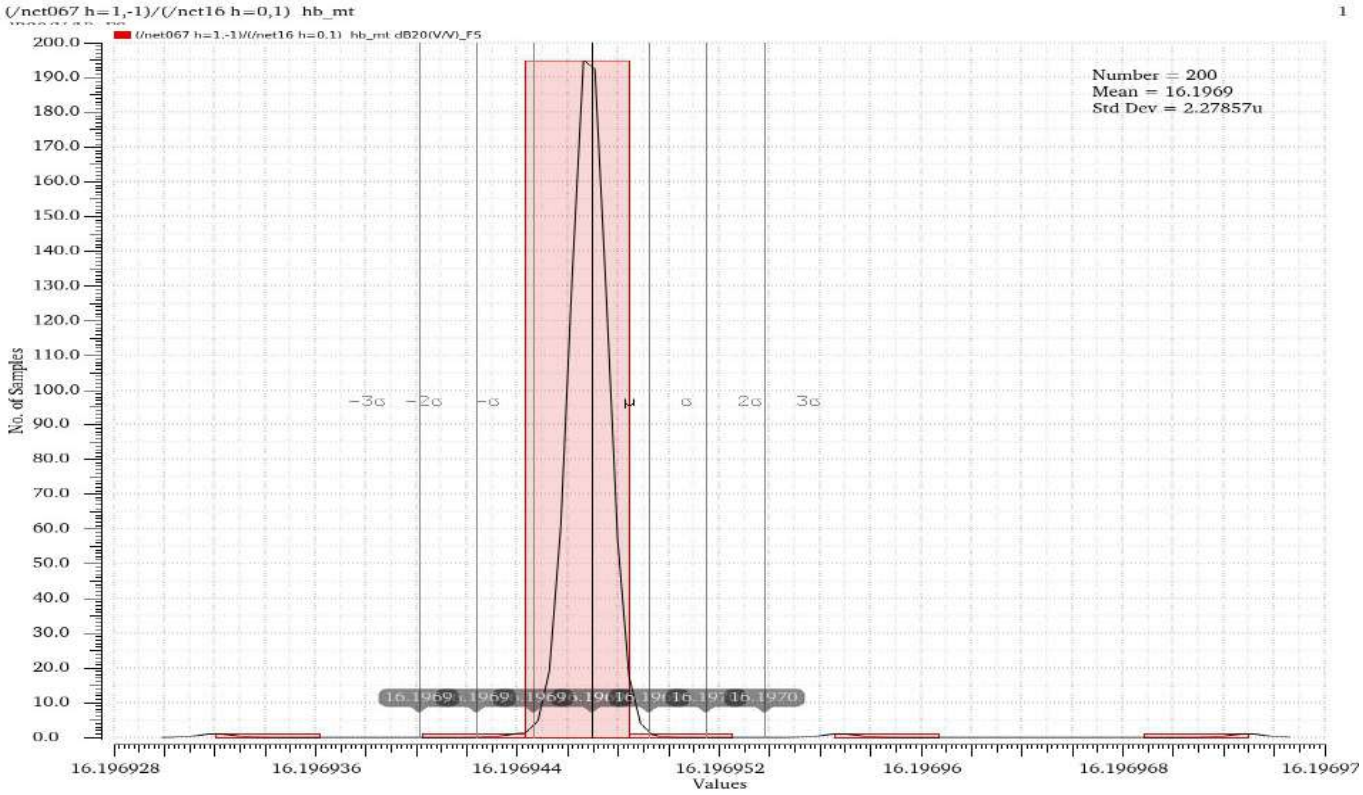

Figure 64: Mismatch Variation in Gain at 6.12GHz (FS corner)

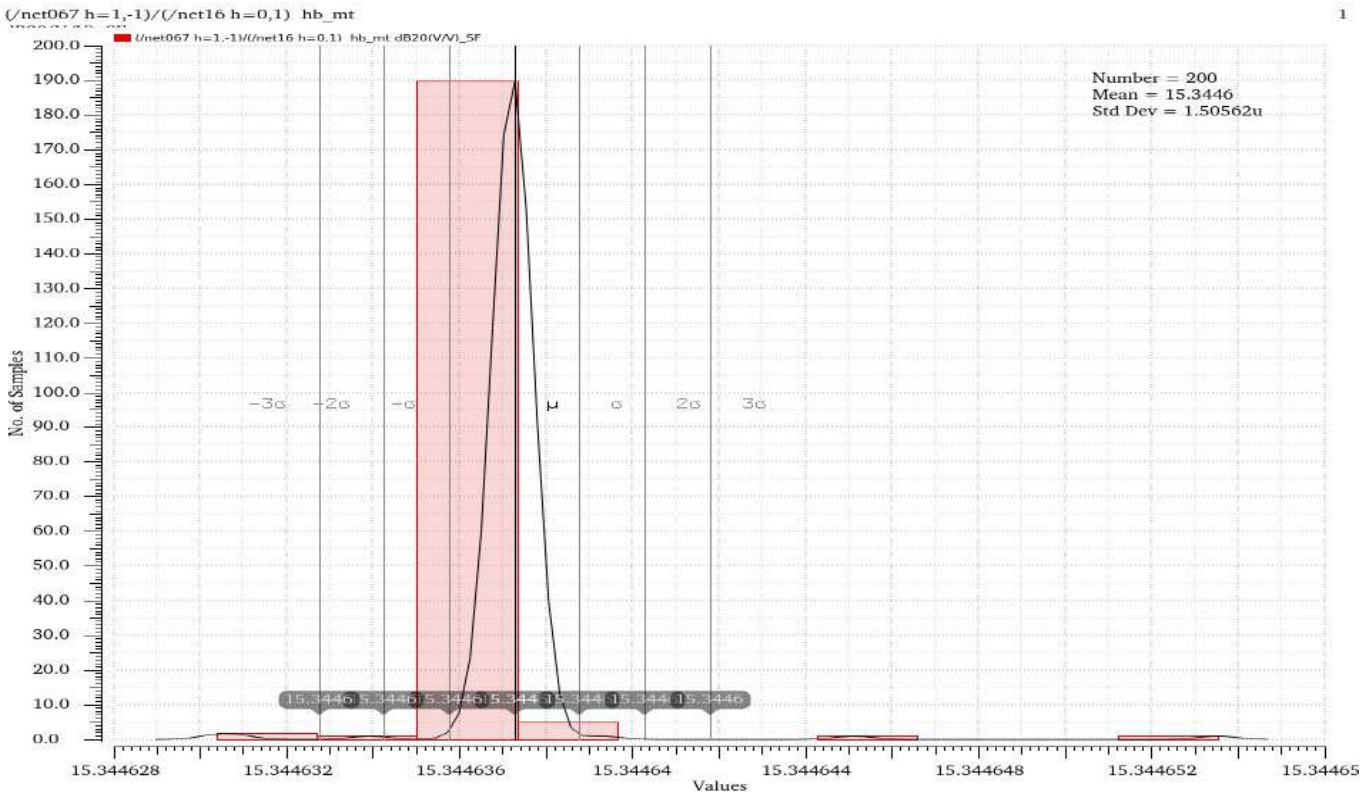

Figure 65: Mismatch Variation in Gain at 6.12GHz (SF corner)

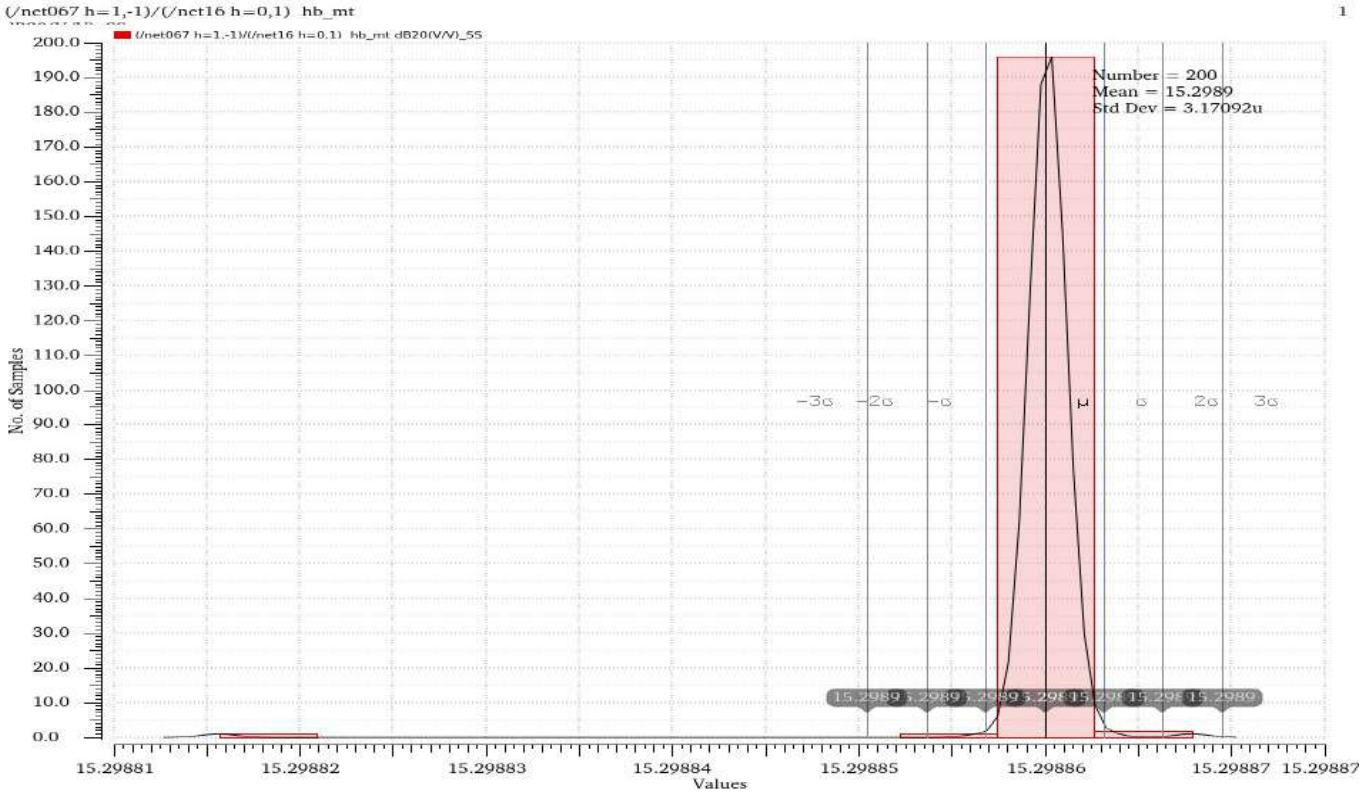

Figure 66: Mismatch Variation in Gain at 6.12GHz (SS corner)

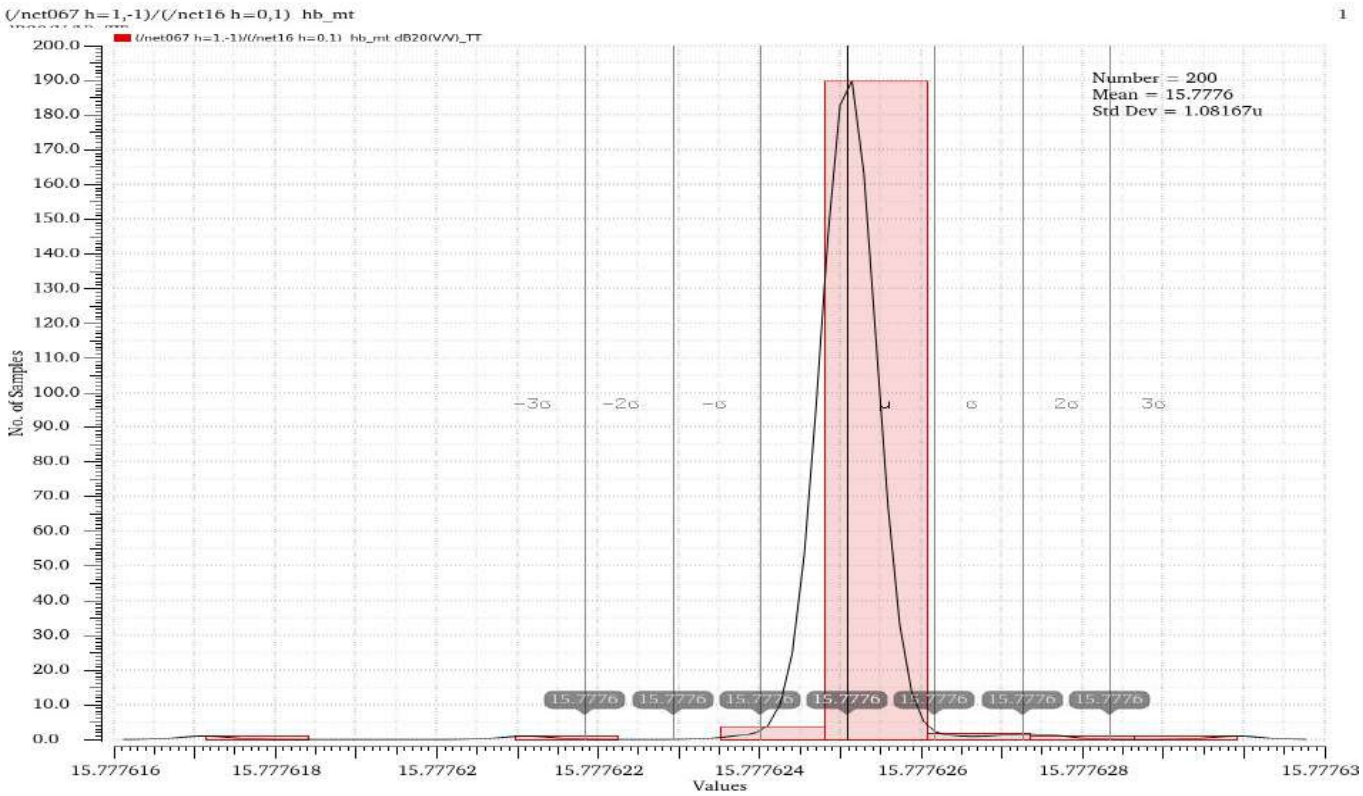

Figure 67: Mismatch Variation in Gain at 6.12GHz (TT corner)

At Flo=3.91GHz:

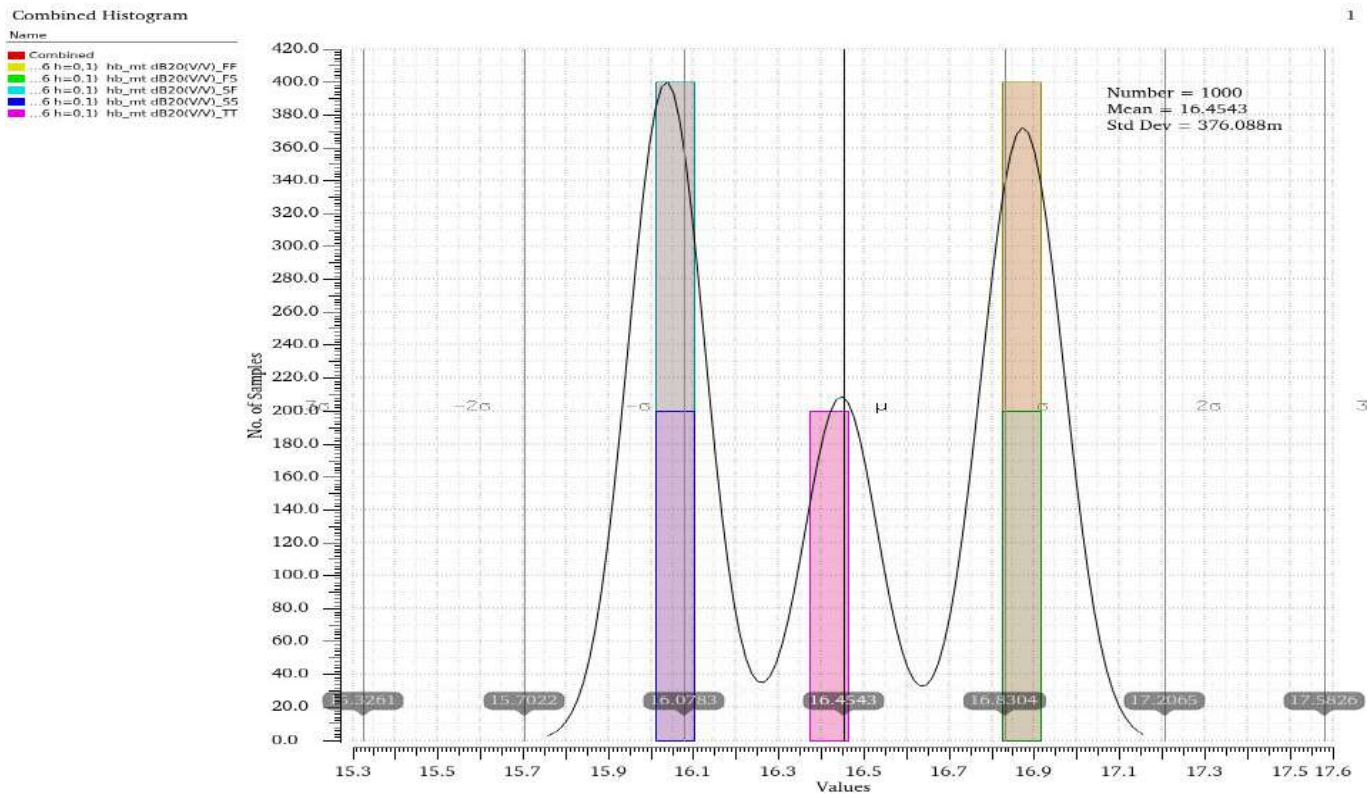

Figure 68: Mismatch Variation in Gain at 3.91GHz

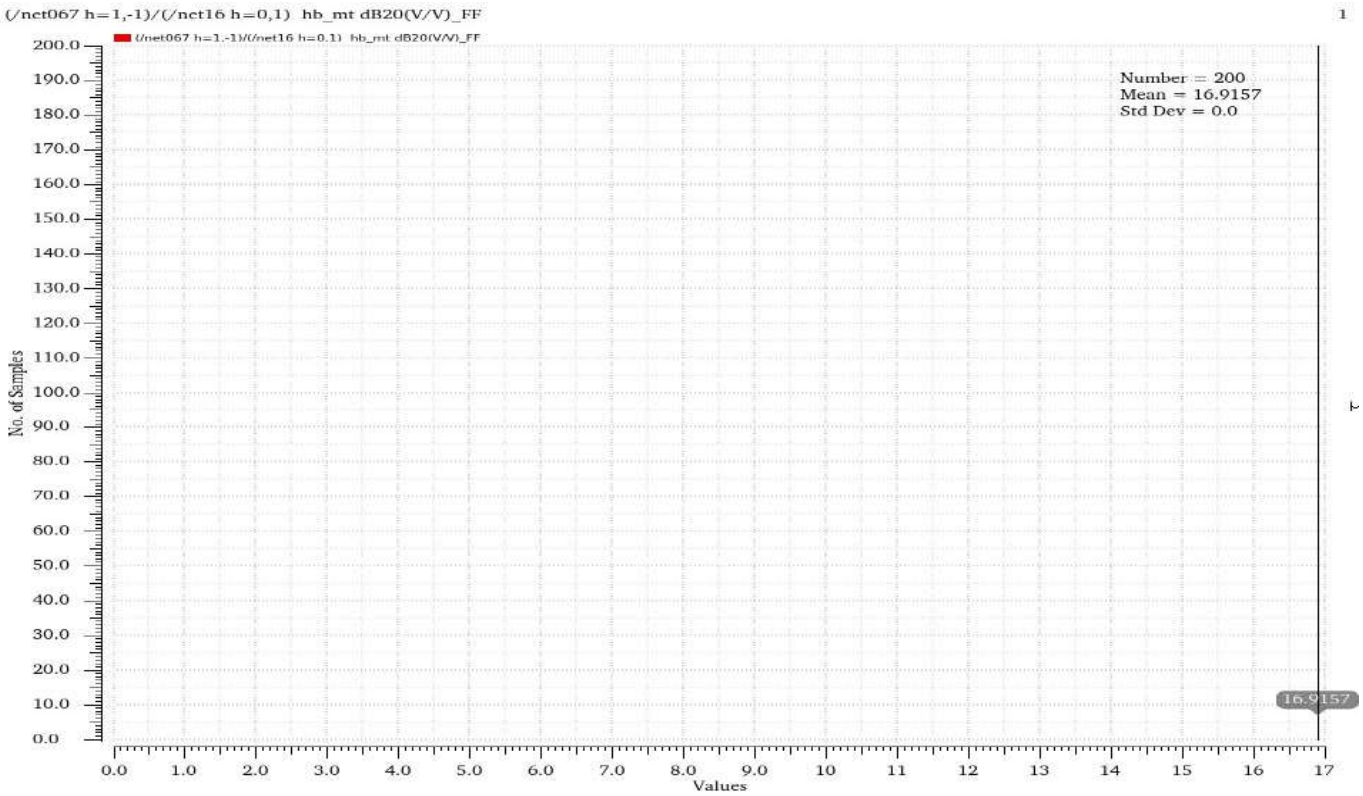

Figure 69: Mismatch Variation in Gain at 3.91GHz (FF corner)

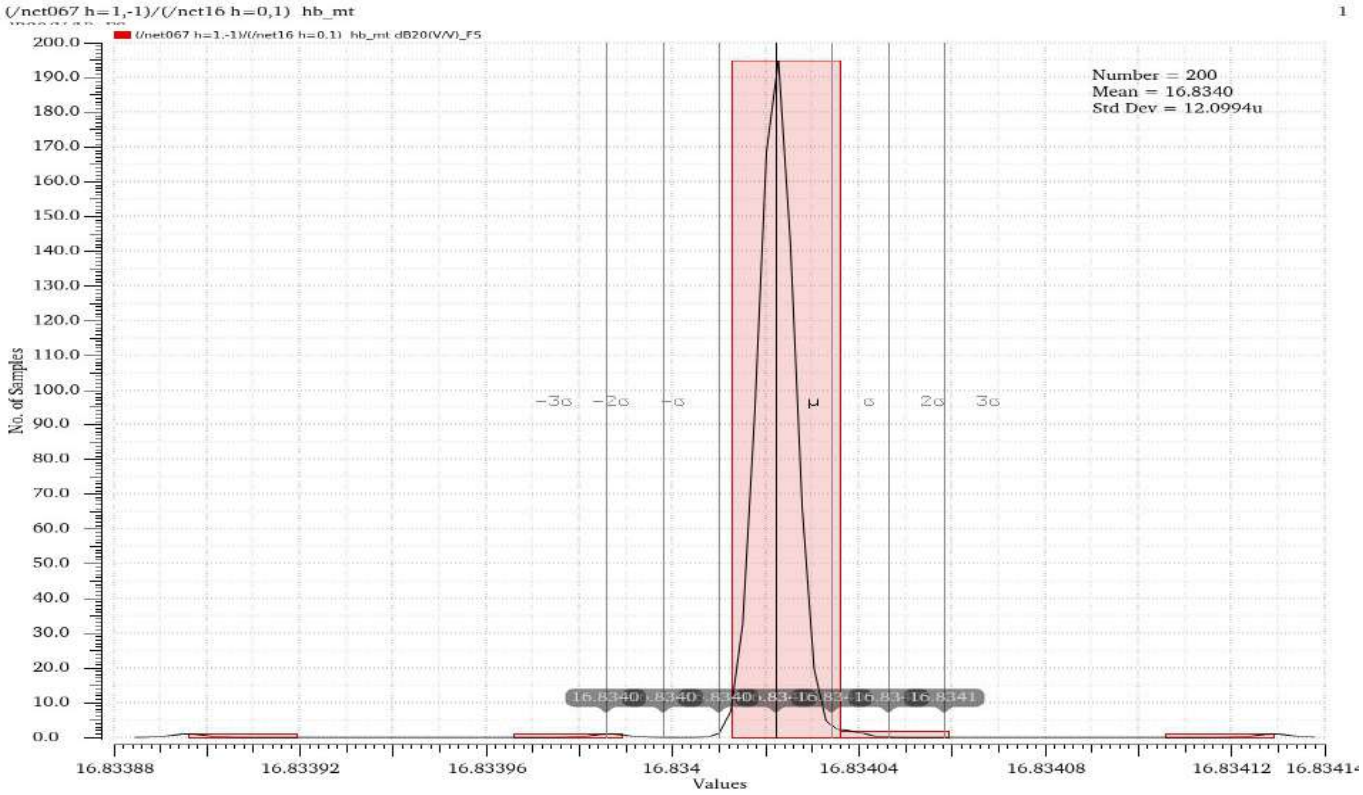

Figure 70: Mismatch Variation in Gain at 3.91GHz (FS corner)

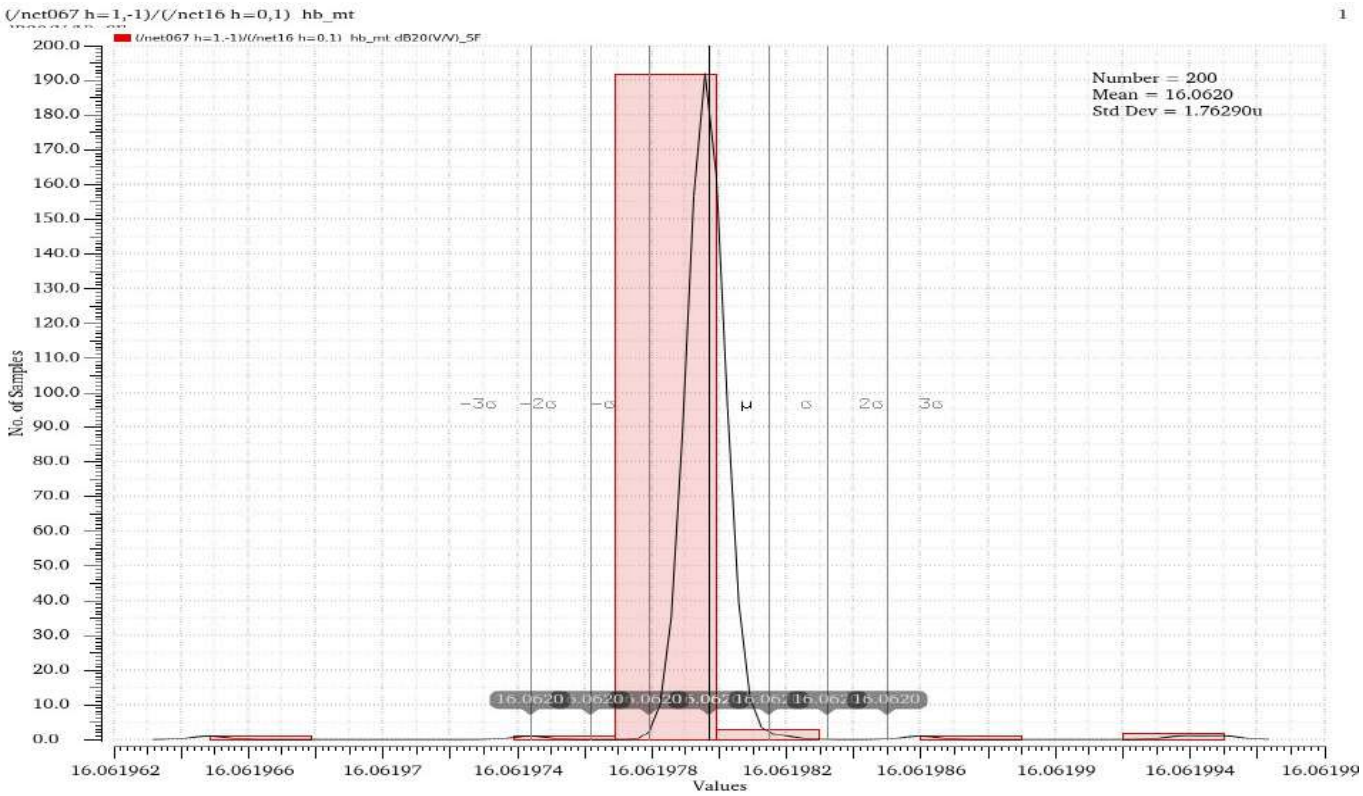

Figure 71: Mismatch Variation in Gain at 3.91GHz (SF corner)

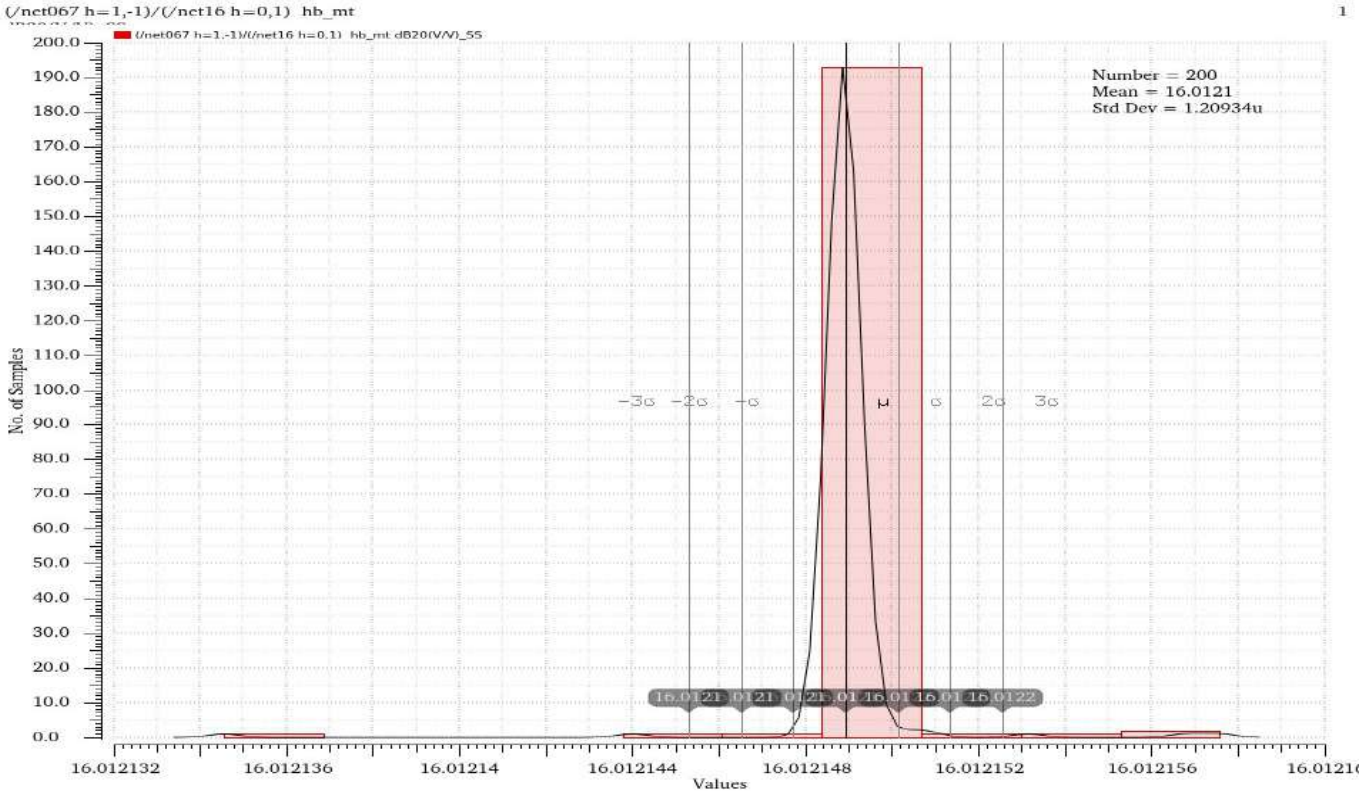

Figure 72: Mismatch Variation in Gain at 3.91GHz (SS corner)

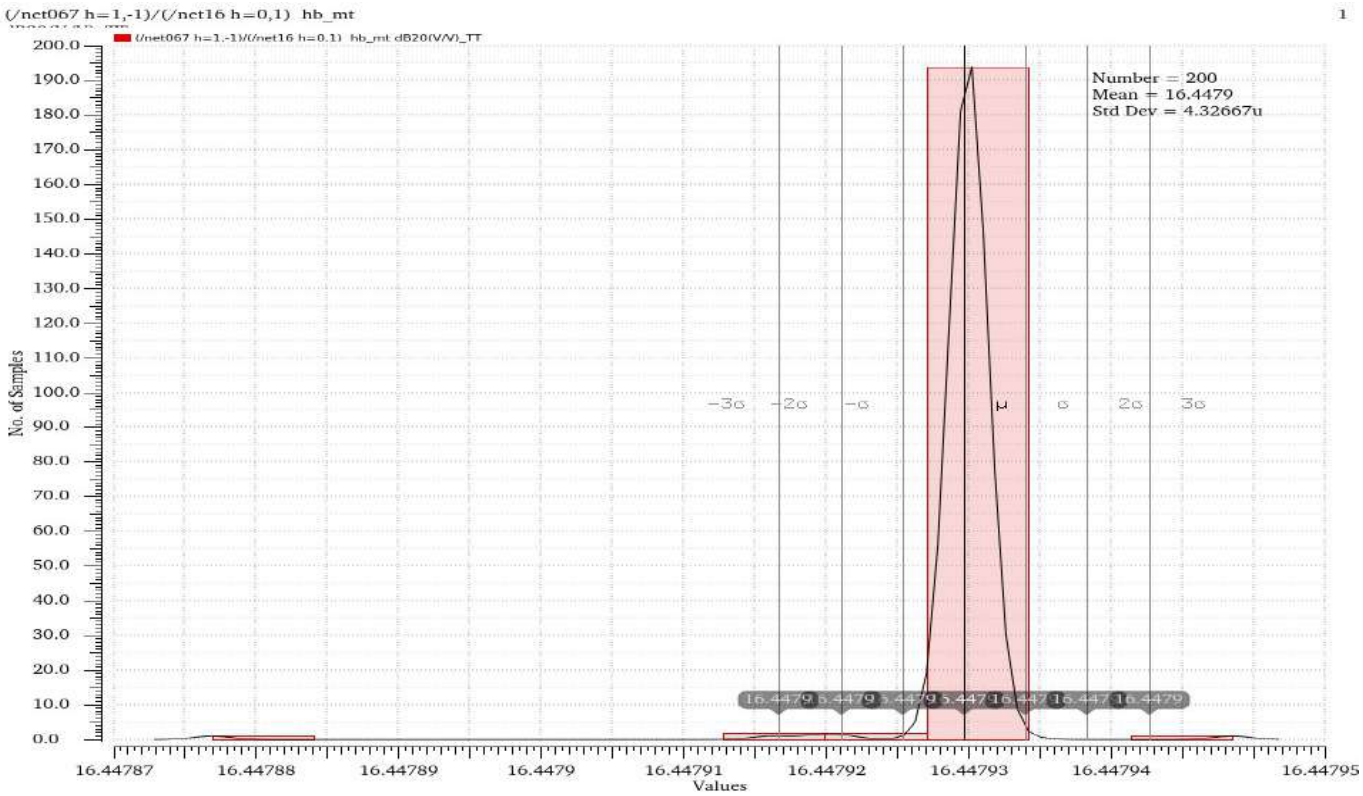

Figure 73: Mismatch Variation in Gain at 3.91GHz (TT corner)

At Flo=680MHz:

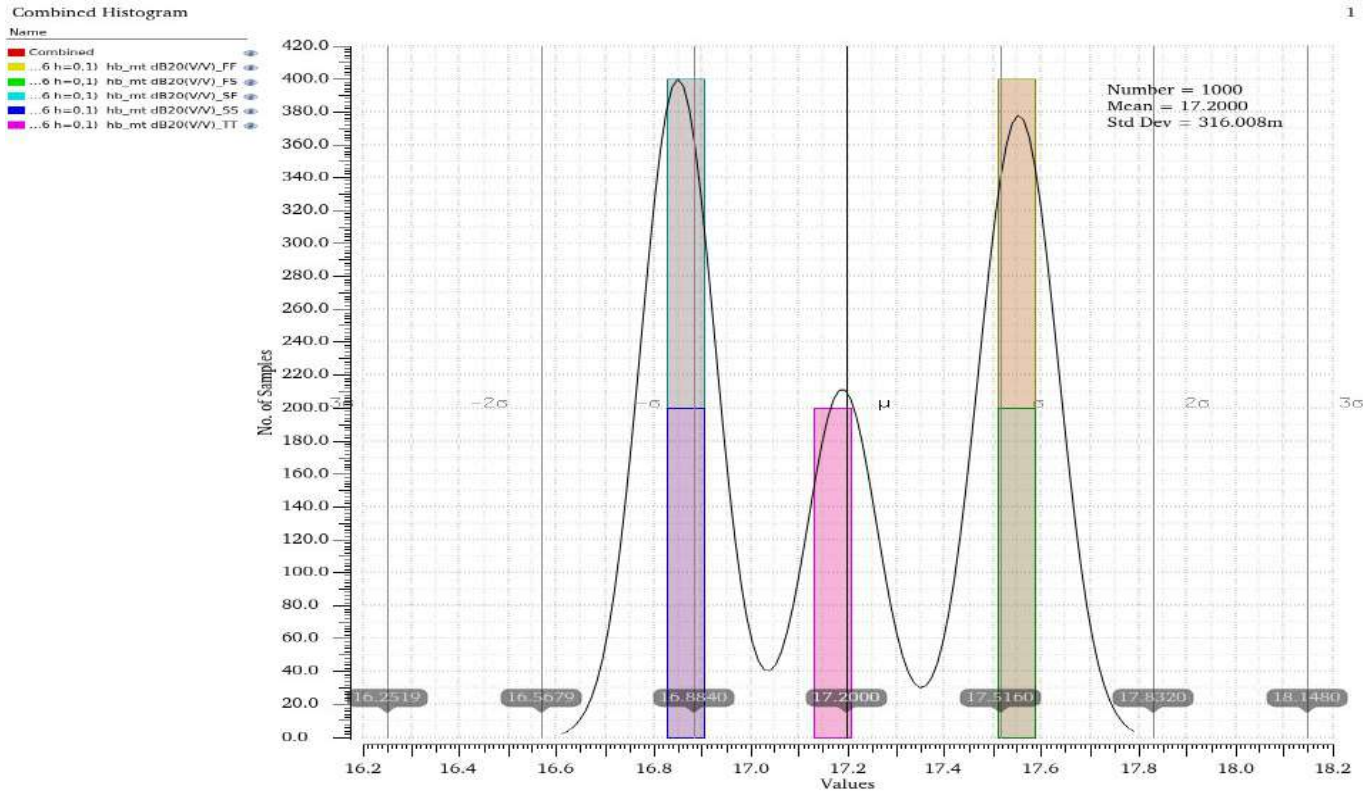

Figure 74: Mismatch Variation in Gain at 680MHz

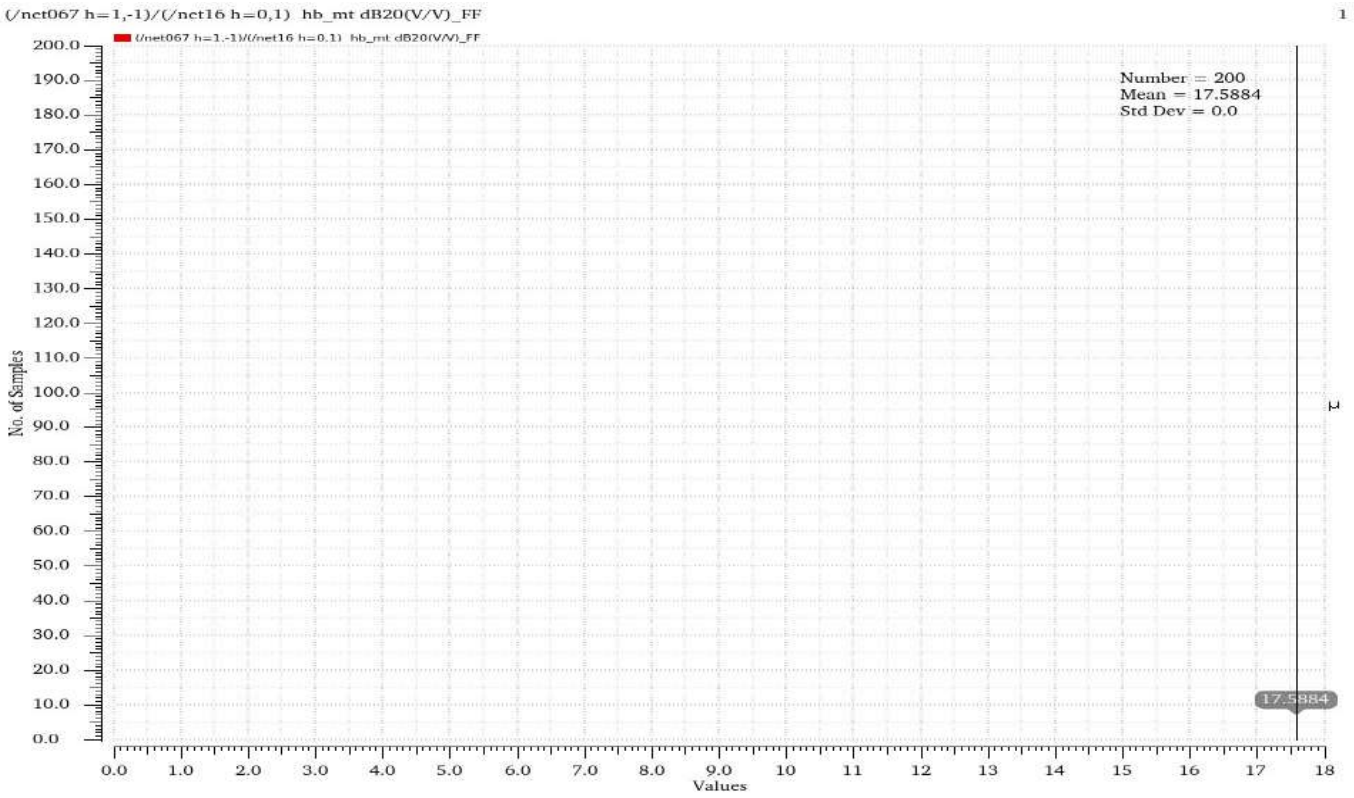

Figure 75: Mismatch Variation in Gain at 680MHz (FF corner)

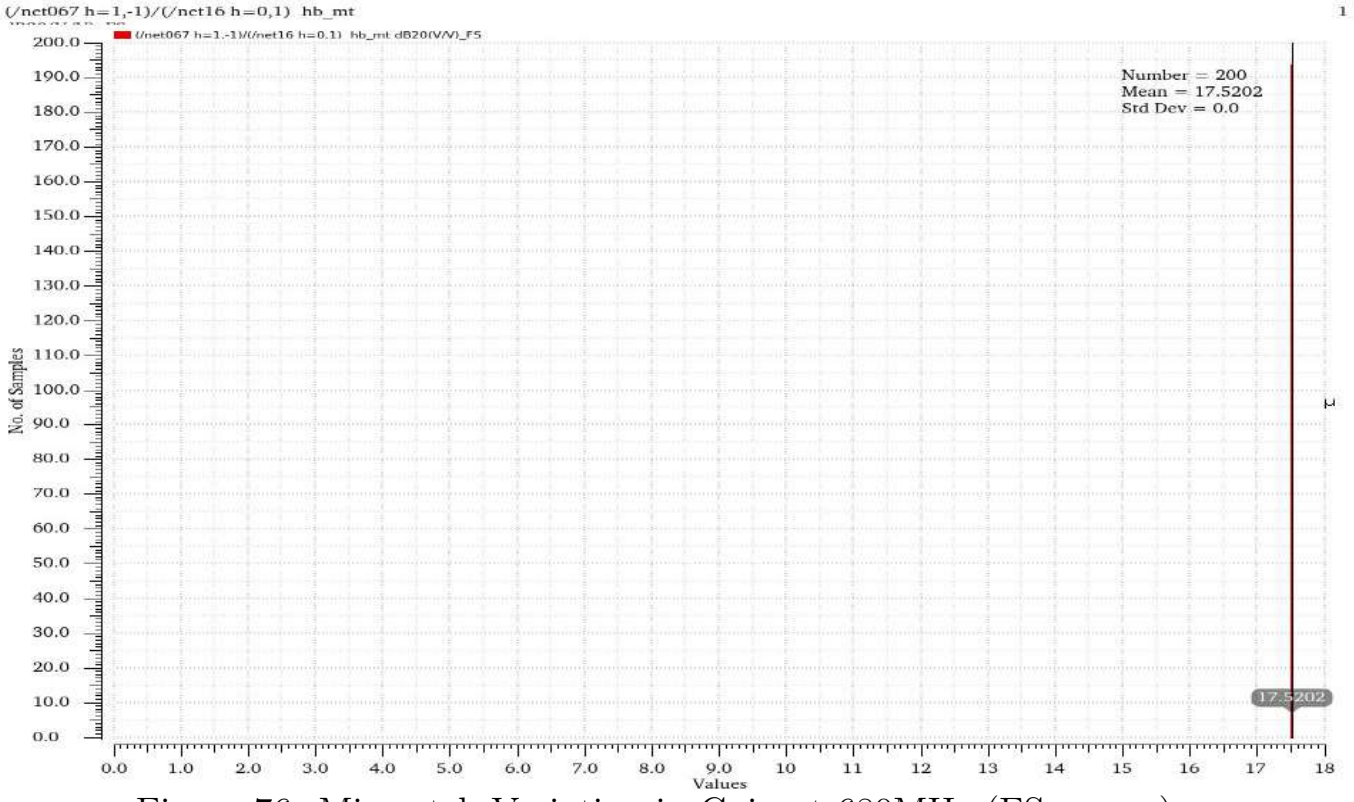

Figure 76: Mismatch Variation in Gain at 680MHz (FS corner)

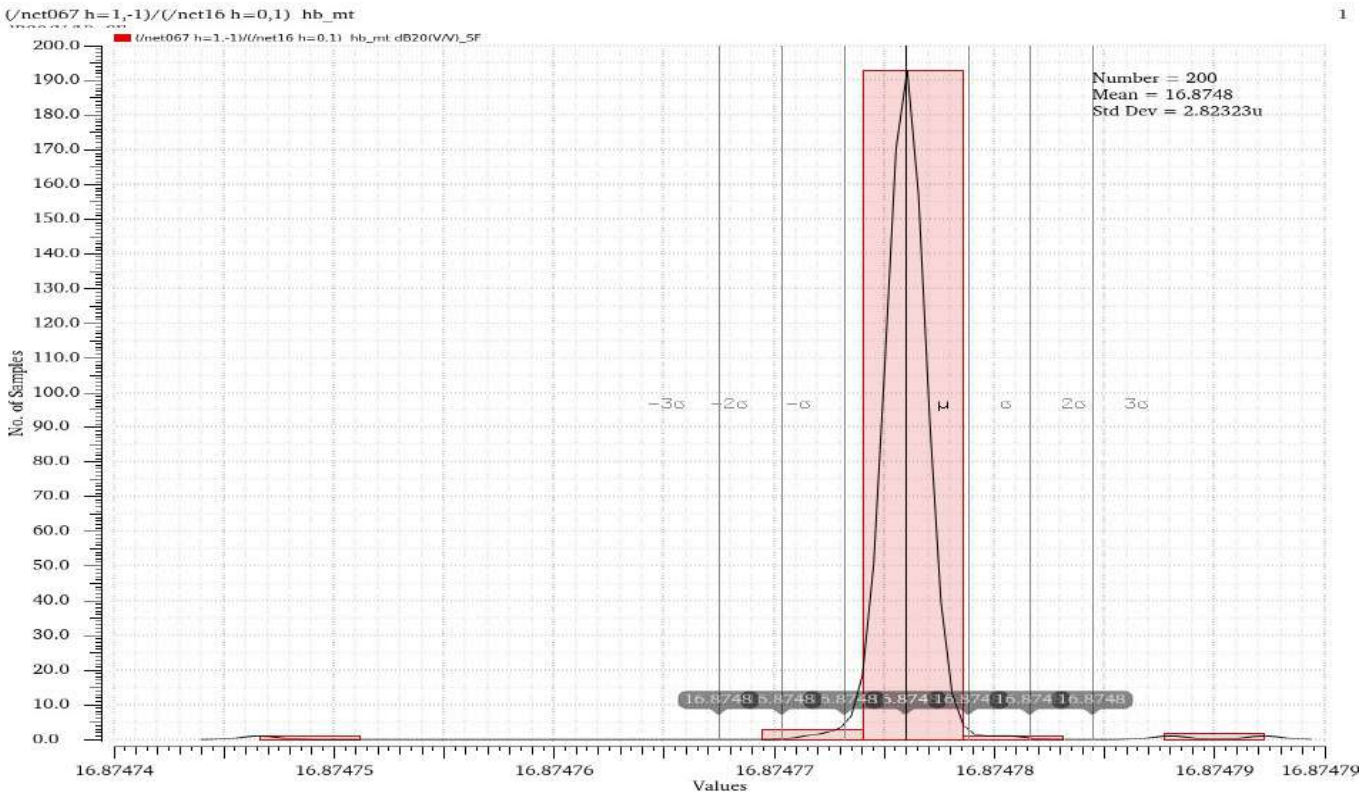

Figure 77: Mismatch Variation in Gain at 680MHz (SF corner)

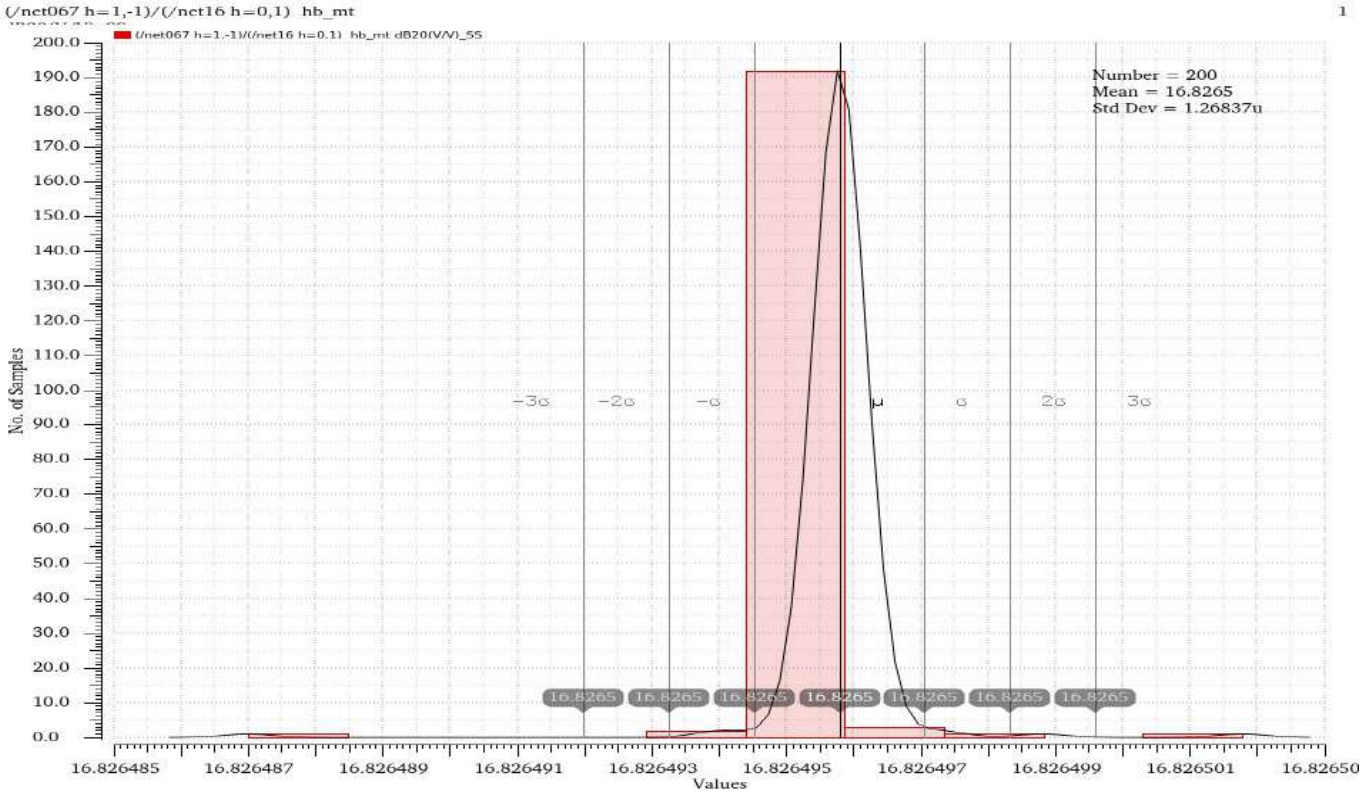

Figure 78: Mismatch Variation in Gain at 680MHz (SS corner)

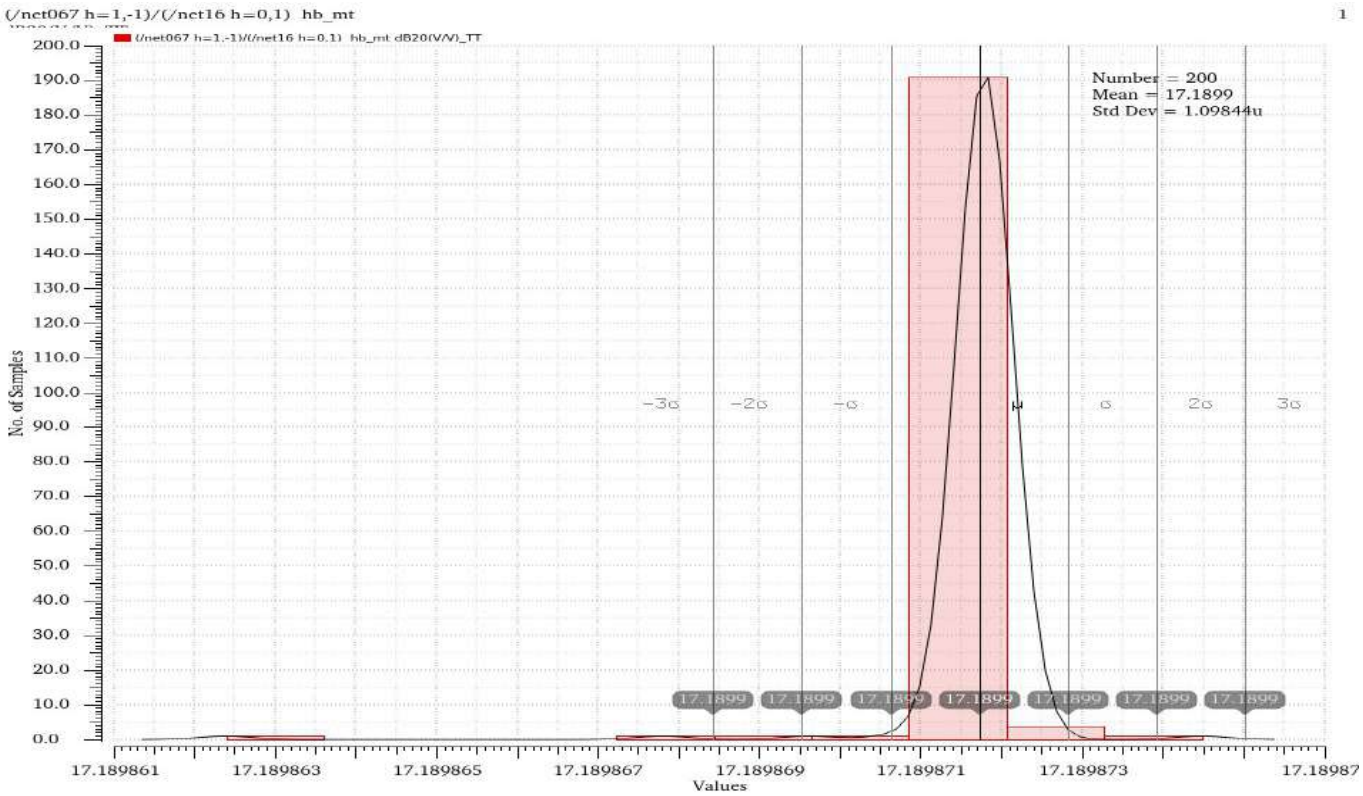

Figure 79: Mismatch Variation in Gain at 680MHz (TT corner)

AM-AM & AM-PM plots:

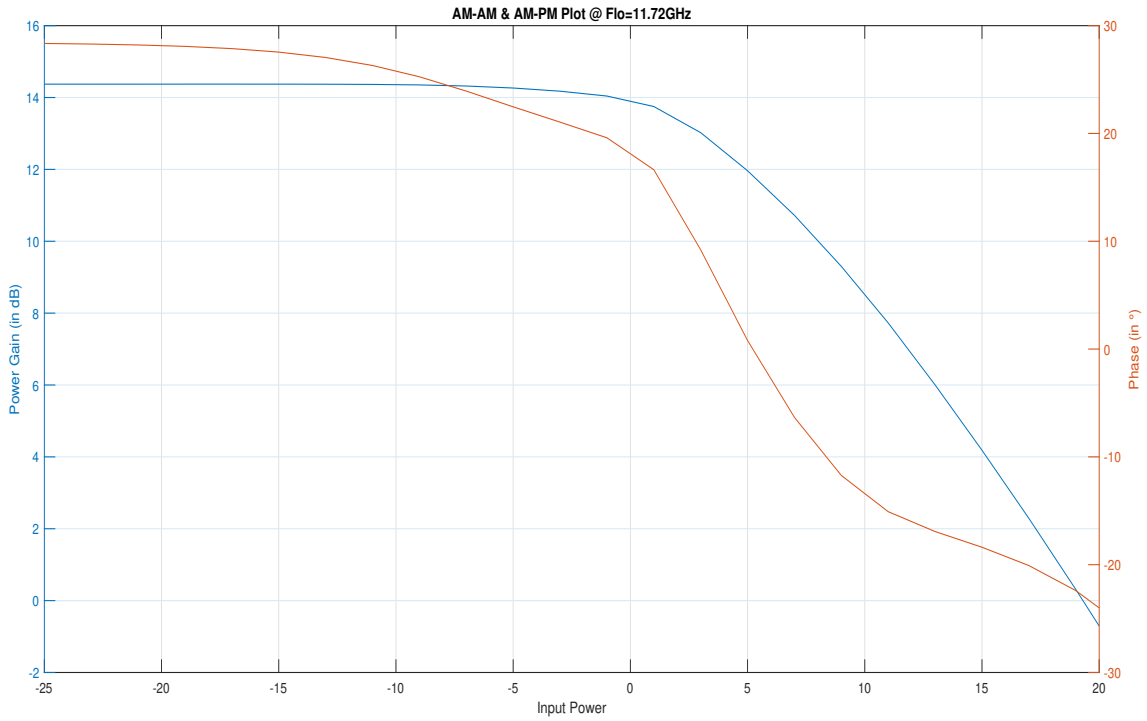

Figure 80: AM-AM, AM-PM plot at Flo=11.72GHz

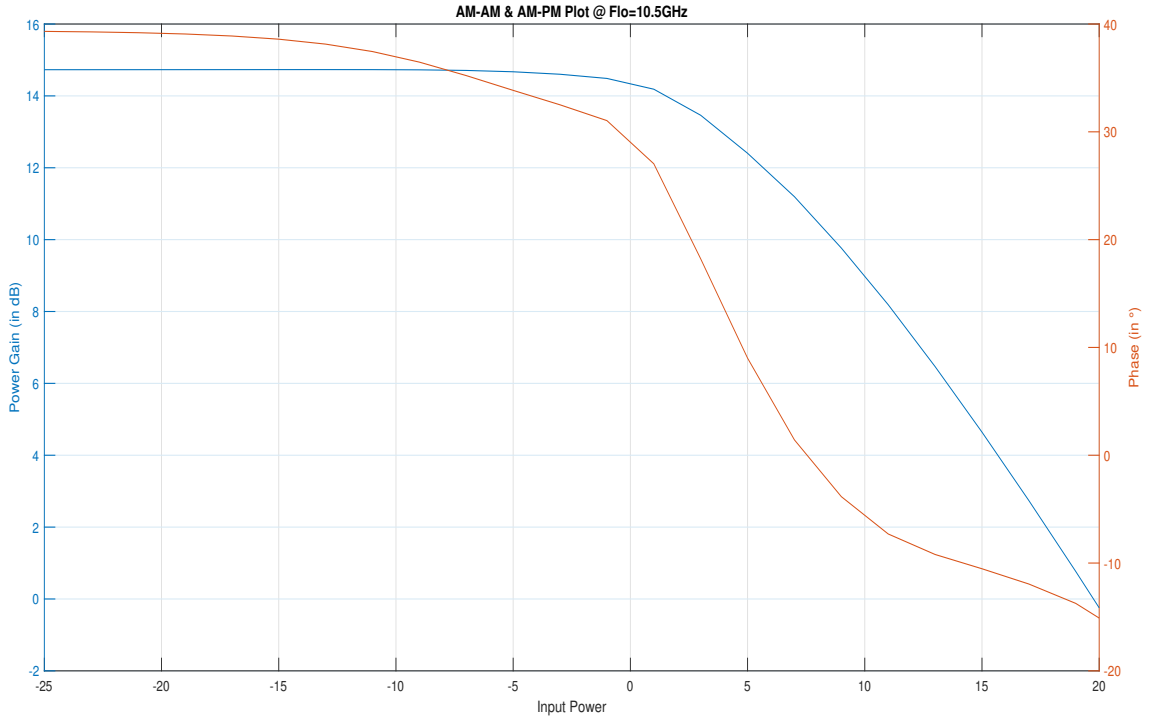

Figure 81: AM-AM, AM-PM plot at Flo=10.5GHz

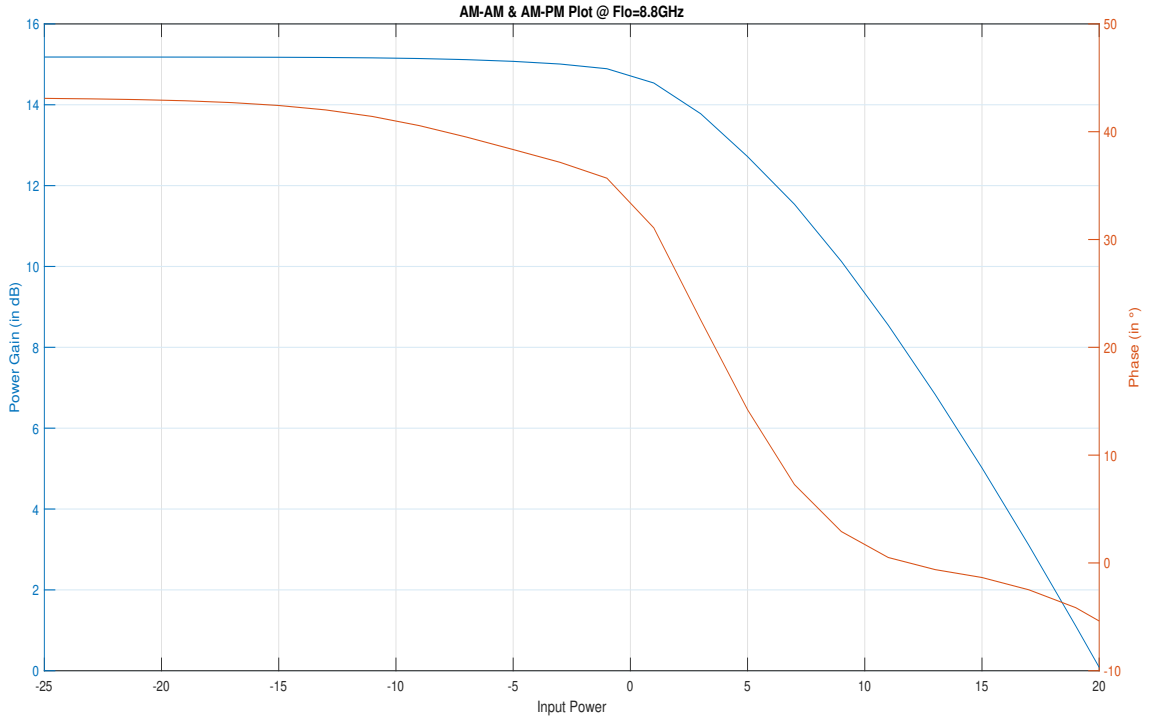

Figure 82: AM-AM, AM-PM plot at Flo=8.8GHz

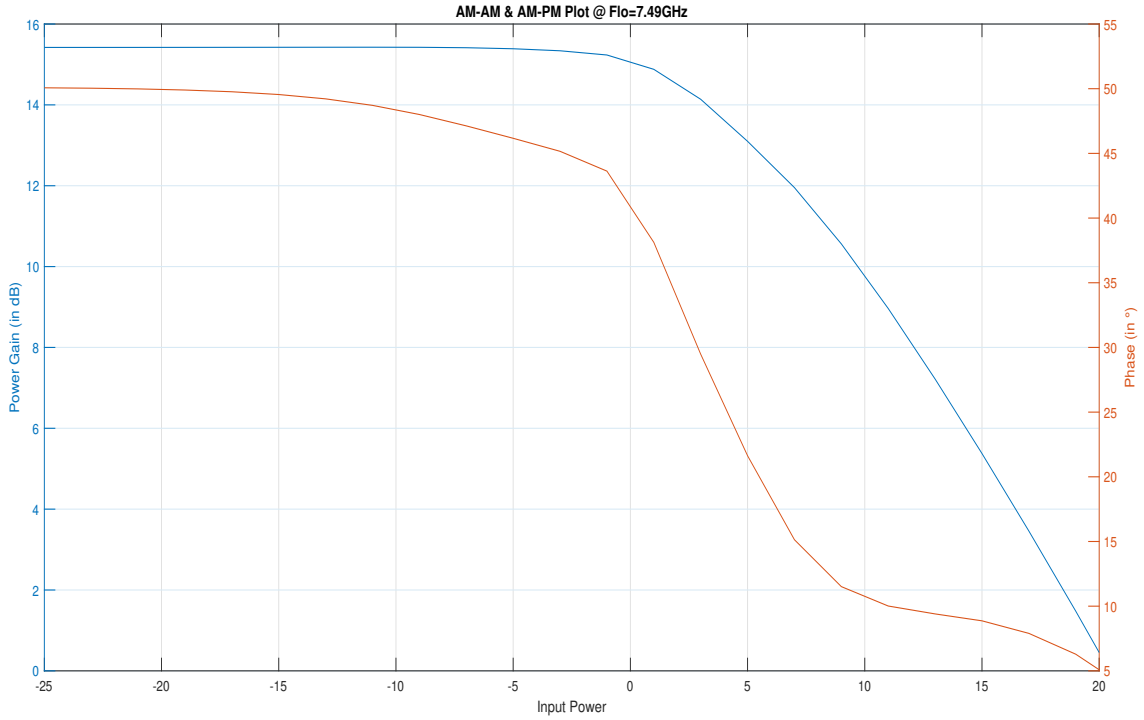

Figure 83: AM-AM, AM-PM plot at Flo=7.49GHz

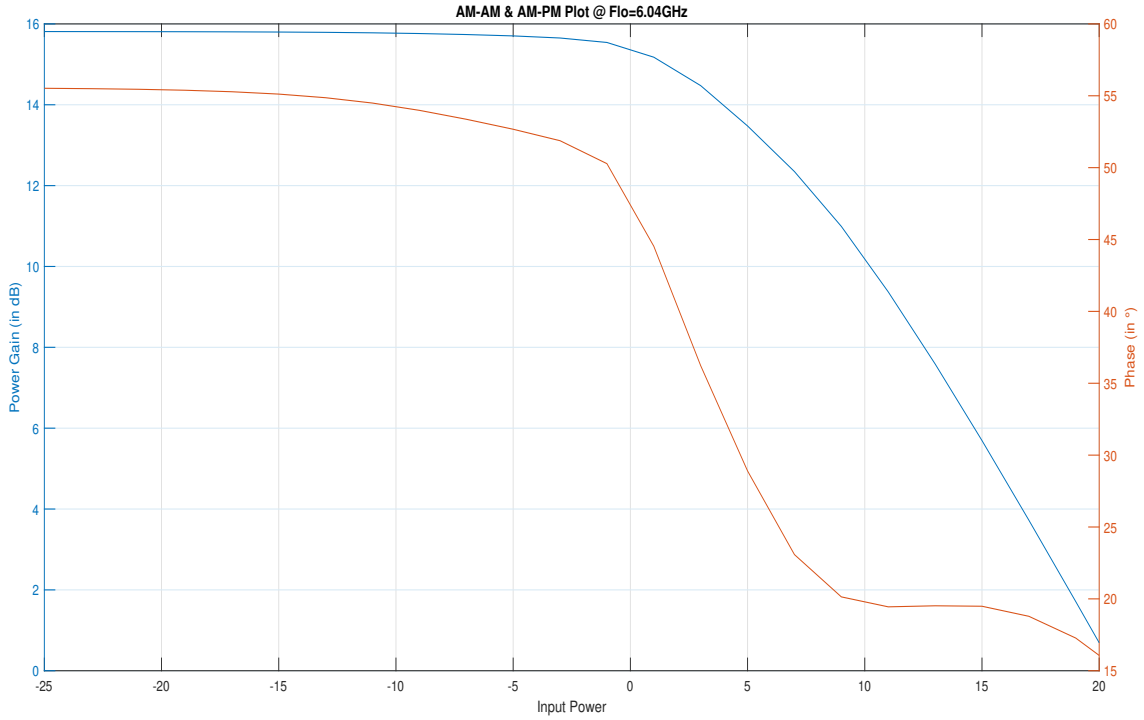

Figure 84: AM-AM, AM-PM plot at Flo=6.04GHz

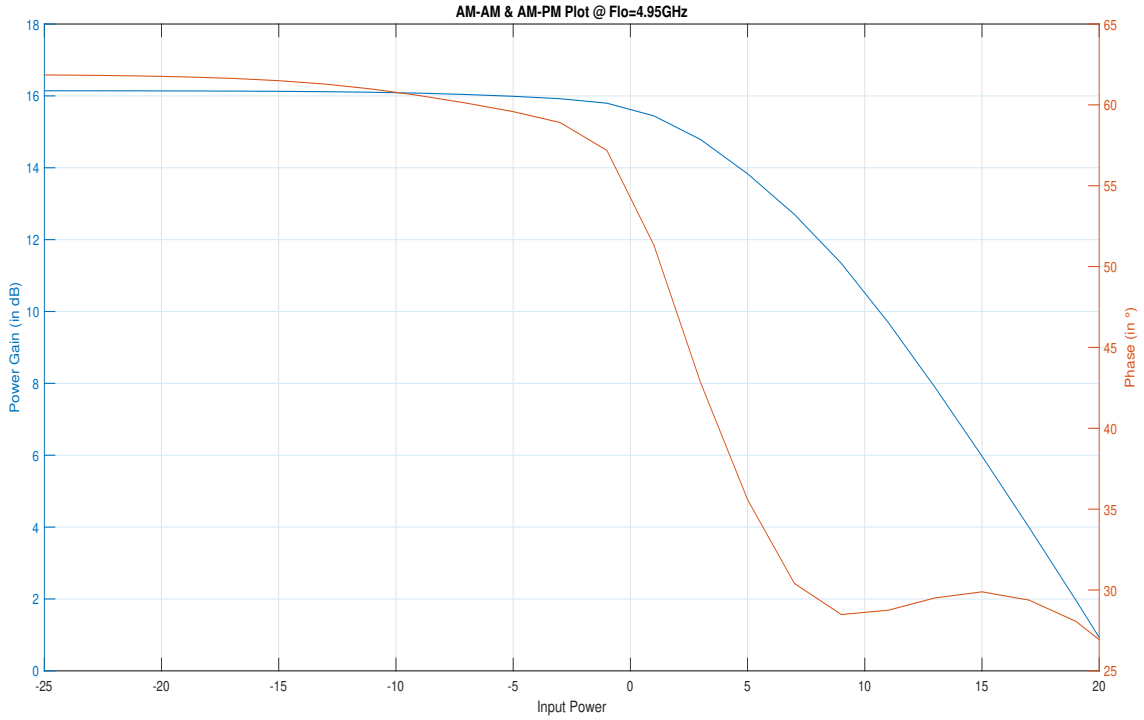

Figure 85: AM-AM, AM-PM plot at Flo=4.95GHz

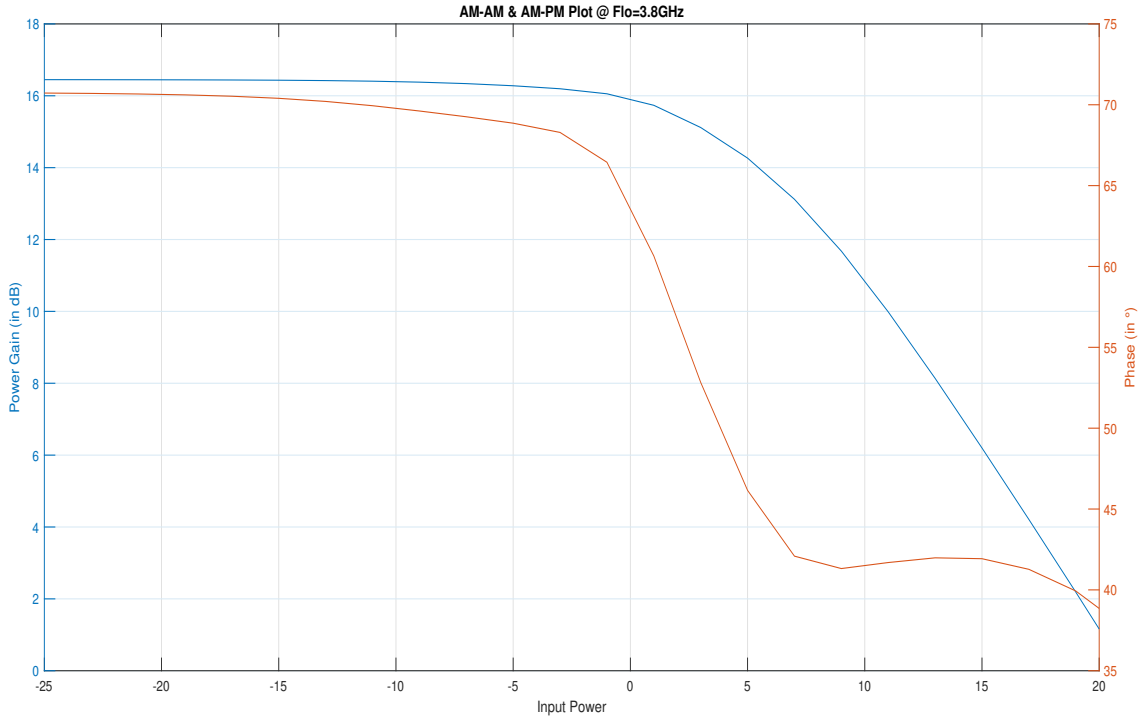

Figure 86: AM-AM, AM-PM plot at Flo=3.8GHz

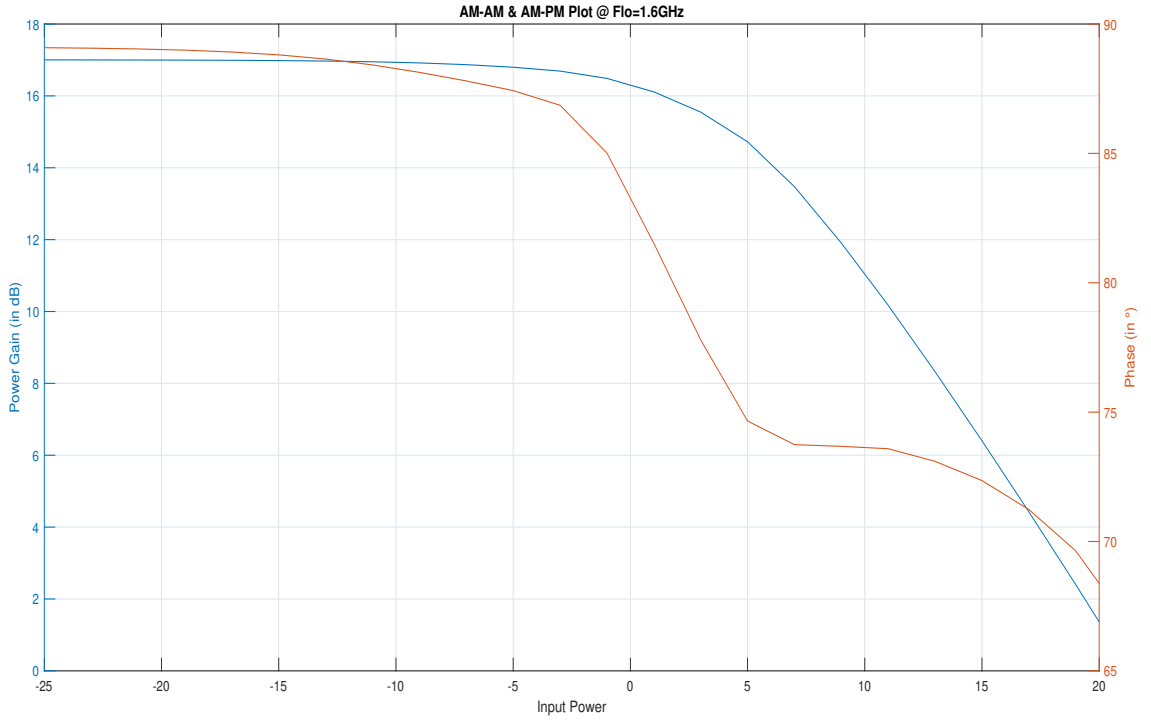

Figure 87: AM-AM, AM-PM plot at Flo=1.6GHz

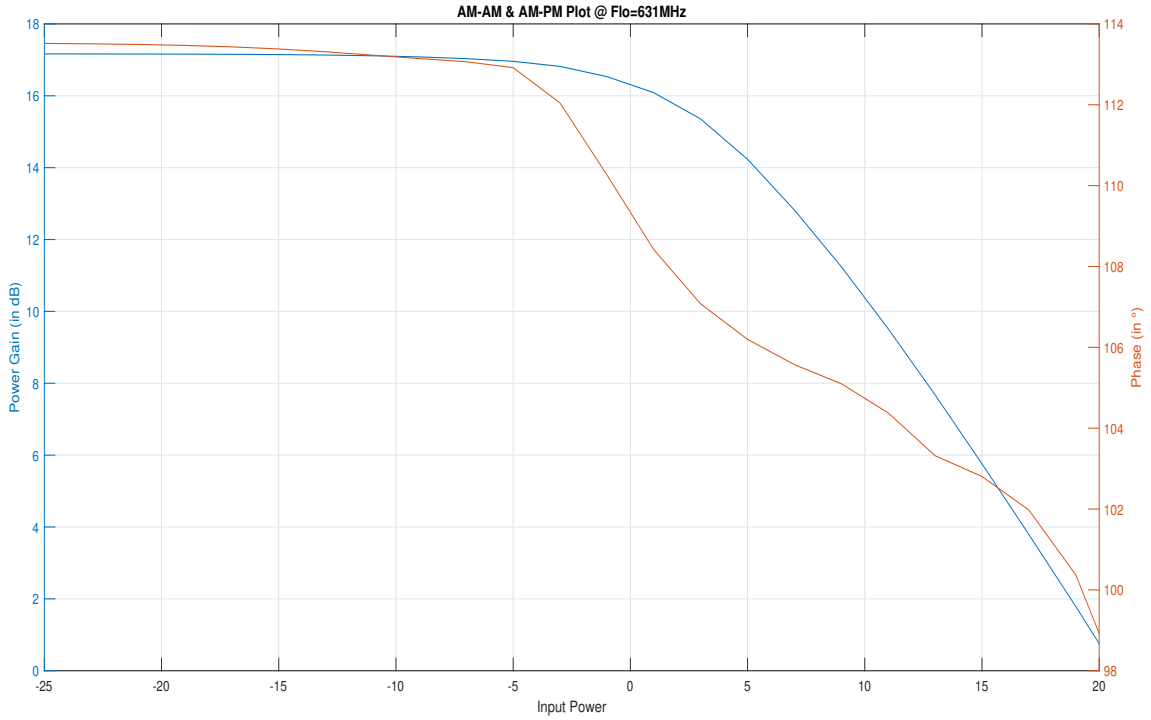

Figure 88: AM-AM, AM-PM plot at Flo=631MHz

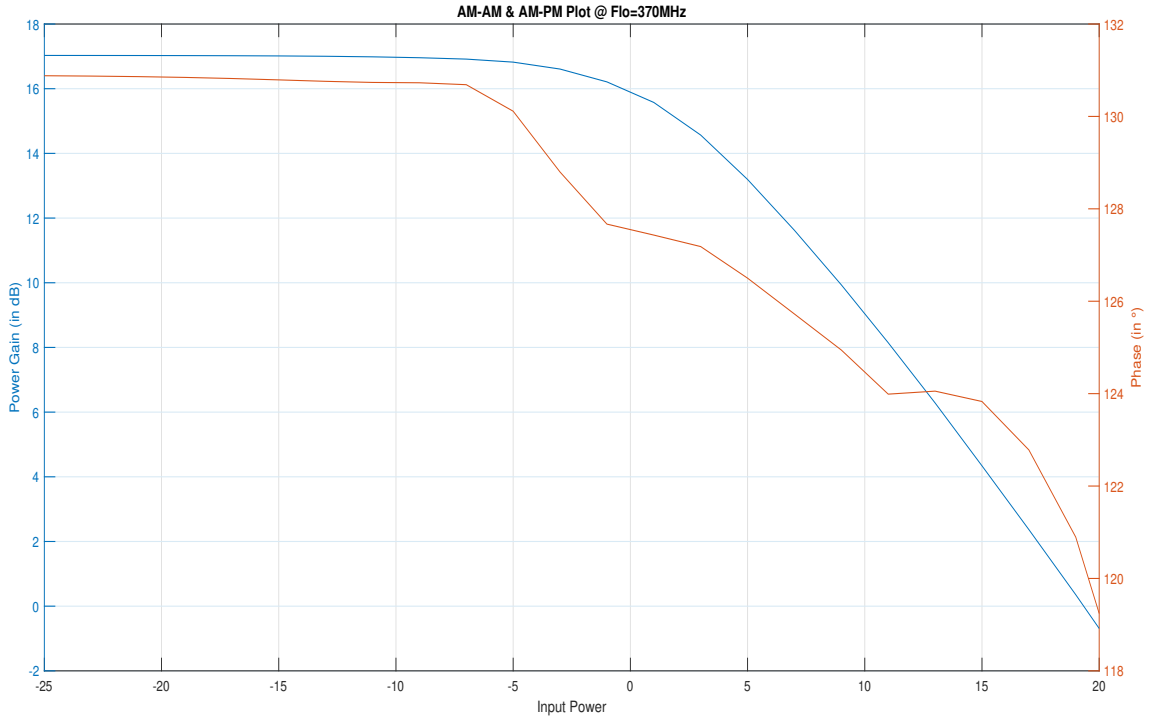

Figure 89: AM-AM, AM-PM plot at Flo=370MHz

5 Chip Testing

5.1 Introduction

The version 1 of the Wideband Tx chip which was tapped-out in the previous year was to be tested. PCB board with RF Traces, Variable Voltage Supply boards to power-up the chip and de-embedding boards for more accurate measurements were designed to test the chips. The first job was to choose the components and design the PCB boards.

Initially, RF board was designed to operate for 100MHz - 6GHz frequency range to test the chip functioning in this frequency band. Later, new boards would be designed for testing between 6GHz - 12GHZ. The board is design using FR-4 technology with the following stack-up:

		Layer stack up	
L1	TOP	0.060	Cu foil+plating
		0.500	Core
L2		0.035	Inner layer
		0.350	prepregs
L3		0.035	Inner layer
		0.500	Core
L4	BOTTOM	0.060	Cu foil+plating
		0.04	Soldermask
Total Thickness		1.58 +/-10% mm	

Figure 90: PCB Stack-up

The chip needs external IQ-Differential LO Signals and matching networks. For easier matching, the matching network components were placed at a distance of less than $\lambda/10$. Wideband external Bias-Tee was used at the output of the chip to bias the PA. The RF-Trace used co-planer waveguides whose widths were calculated using the "LinCalc" and ADS tools. For constant voltage supply, a

separate power supply board multiple variable output voltage pins using LDOs. To extract the power losses in the traces and other passive components, 2 separate sets of de-embedding boards, each for Output RF trace and LO-RF trace, were designed. For extracting the power loss, the traces and components were replicated and placed back-to-back on board. For efficient performance, layer L1 was used for the RF circuitry, L2 was used as ground, L3 was used for power traces and L4 was virtually unused except for ground to SMA connectors. To reduce the voltage drop across power traces, the width of these lines in L3 were kept thick. Multiple ground pins and multiple staggered vias were also put to have a uniform ground voltage across the board. Solder mask, over the co-planar waveguides, was also removed for better matching. Components with common footprints for different frequencies were selected to have a common board for the given frequency band.

List of the components and their uses are summarised below:

Component	**Footprint/Part Number**	**Purpose**
Tx Chip	QFN-40	Wideband Transmitter Chip
Resistor	0201	General Purpose
Capacitor	0201	Matching Network
Inductor	0201	Matching Network
Bias-Tee	TCBT-123+	Biasing PA
Balun	0805	Differential signal to single ended
SMA Connector	142-0801-801	RF-Connector
LDO	TPS74401	Power Source
UFL	CONUFL001-SMD-T	Impedance Measuring

5.2 Matching Network

The testing of the chip begins with the measurement of the output impedance of the power port and the input impedance of the LO Port. Accordingly, a matching network has to be decided to match the impedance to 50Ω.
Since, the matching network can't be finalised before measuring the impedance, a general footprint of the components was designed as shown in the topology given below:

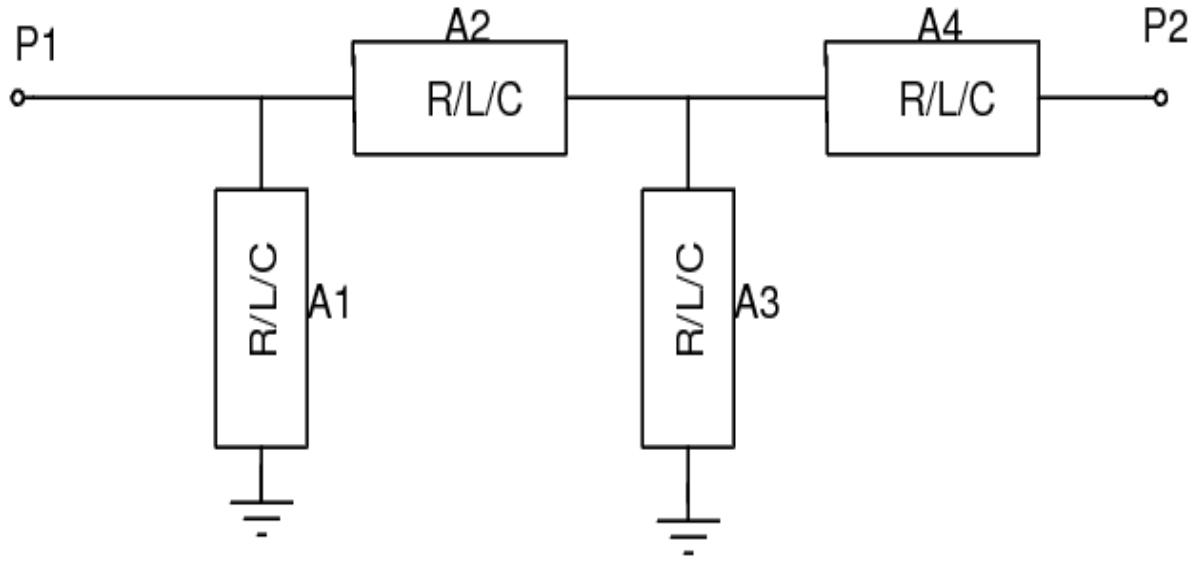

Figure 91: Single ended matching network

To get a $\pi - match$ between nodes P1 and P2, suitable components (R, L, C) can be placed at A1, A2, A3 while a zero ohm resistor can be placed at A4. Similarly, for a T-Match, components can be placed at A2, A3, A4 and A1 can be left open. This way, we can get both the matching topologies. This single ended topology is used at the Power Output pins as the 2 differential half outputs are a bit separated. For LO Inputs, since the 2 halves are close to each other, a differential topology (as shown below) is used.

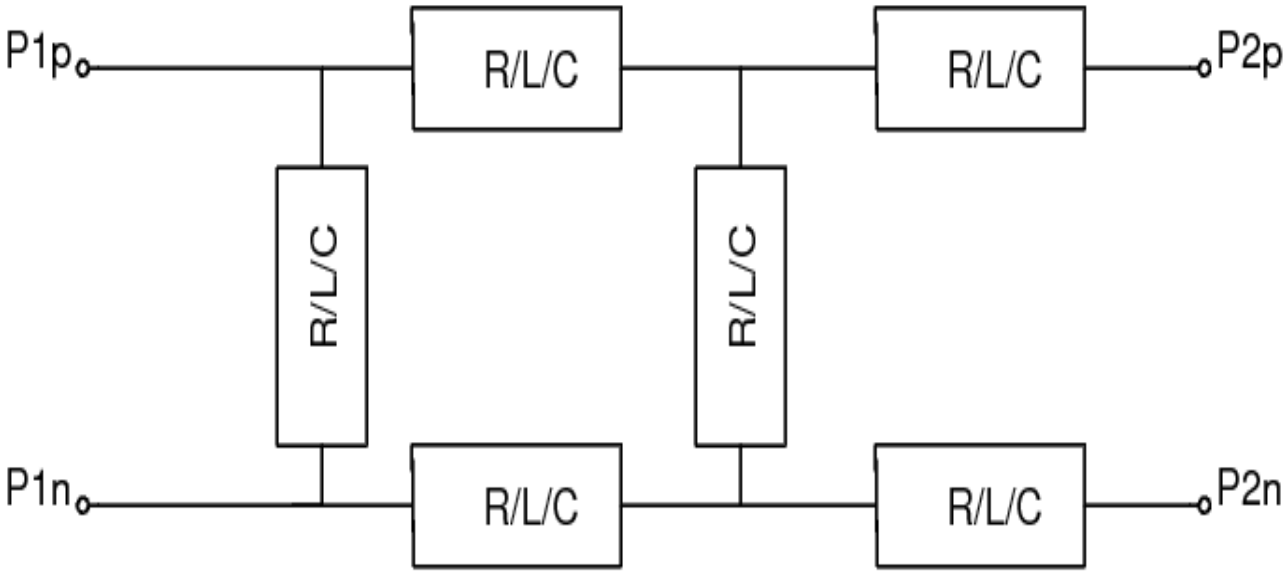

Figure 92: Differential matching network

The single ended matching network was further modified to be able to measure the impedance of the pins. The new layout is shown below:

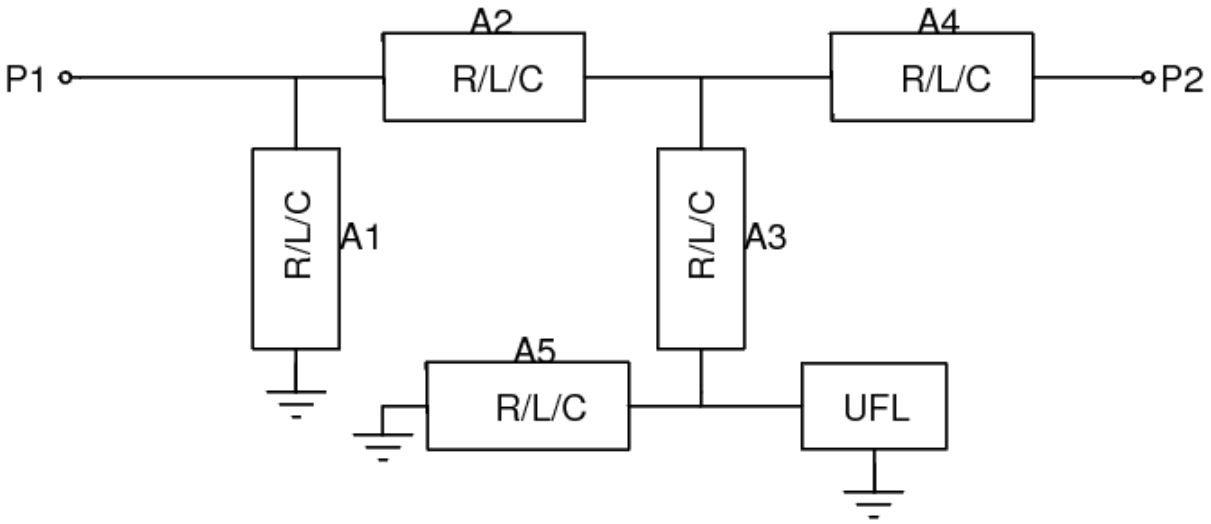

Figure 93: Single ended matching network

To measure the impedance of a pin, say pin 1., A1, A4, A5 are kept open and zero ohm resistors are placed at A2 and A3. The impedance at P1 can now be measured by connecting co-axial cable to the UFL. Similarly, for pin2, A3 and

A4 can be shorted suing zero ohm resistor and rest of the pads can be kept open. The idea is to short the path to the pin from UFL with zero ohm resistor and keep the other pad open.

When being used as a matching network, the UFL can be de-soldered, and the matching network can be made by placing the components at A1, A2,A3,A4 (as described previously) with a zero ohm resistor at A5 for ground.

In a similar way, the impedance of each pin in a differential port can be measured. The component topology is shown below:

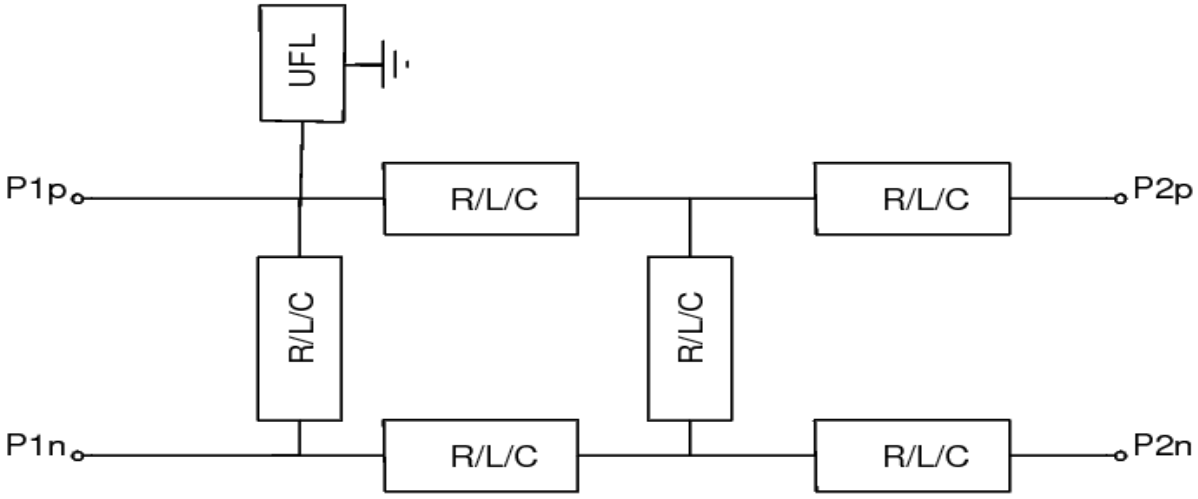

Figure 94: Differential matching network with UFL

The above mentioned matching topologies have also been used for Baseband matching, but a 50Ω at each input node should work.

5.3 PCB Schematic

A broad level schematic of the Tx-Chip test board is show below (Note, to keep it simple, power supply connections have been omitted):

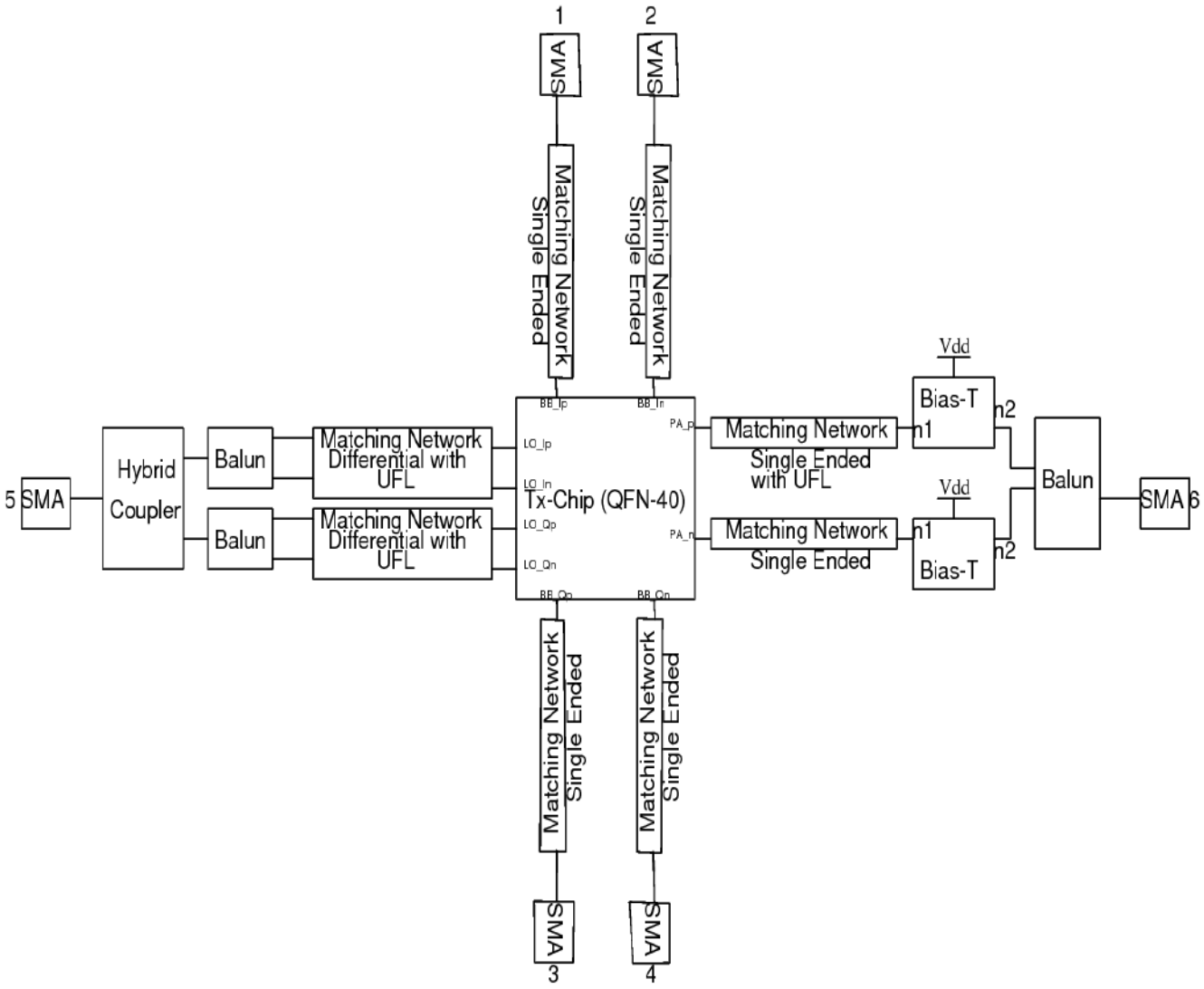

Figure 95: RF Board Circuit Diagram

The on-chip PA is biased using an external voltage supply through BiasT. Since, the matching network at the power output carries DC current, that network has to be a High Pass network. The matching network at the input of the LO signals can be either high pass or low pass.

The differential BB signals can be generated using a differential output voltage DAC or using a Low frequency balun. These signals can be fed to the chip using through the SMAs 1,2,3,4. The LO signal is fed through SMA 5. The Hybrid coupler splits the signal creating a 0degree and 90 degree phase shifted signals which are then fed to the Balun. This way, 4 signals with phase shift 0degree,

90degree, 180degree and 270degree are generated. The differential PA output signal is combined using a balun and the output is then available at SMA 6.

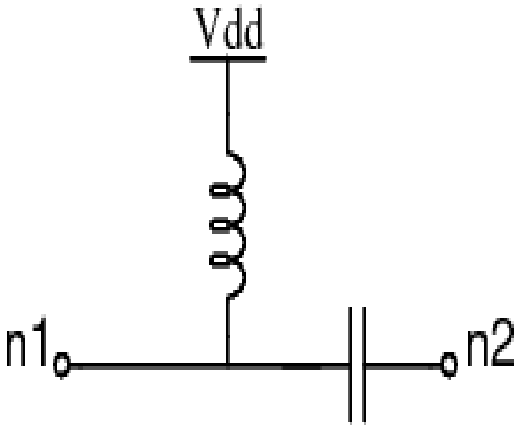

Figure 96: Bias-Tee

5.4 Power Supply

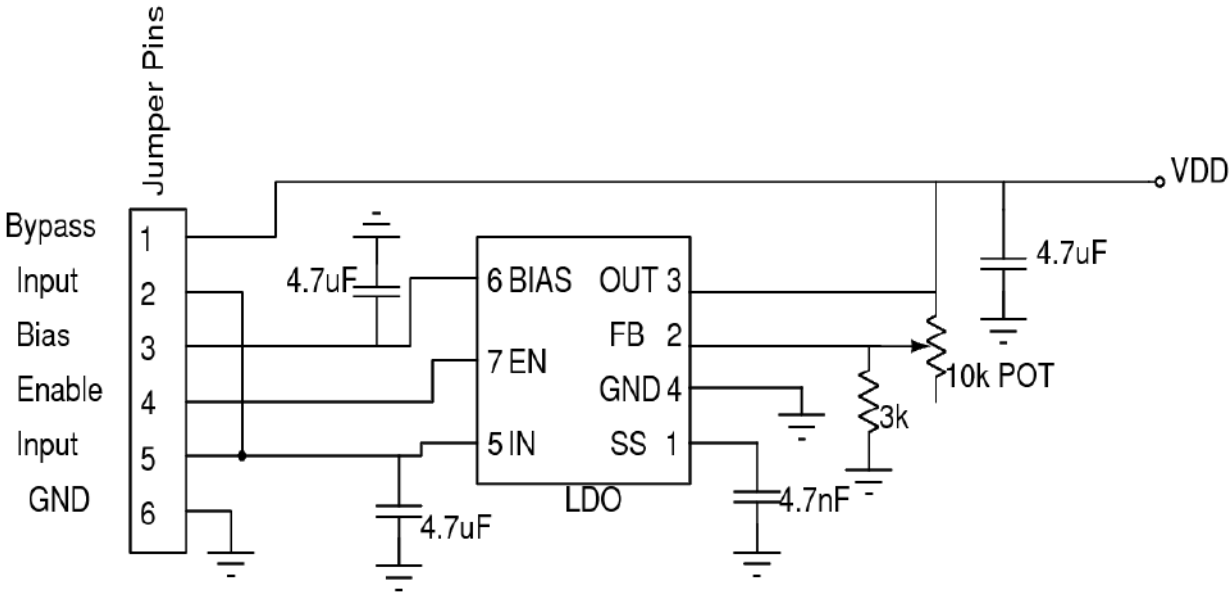

Figure 97: Power Supply Circuit Diagram

The values were chosen from the LDO datasheet by Texas Instruments. The input to the LDO is through the Jumper Pins (as shown in the schematic). The constant output voltage is available at VDD which can be adjusted using the

10kΩ variable resistor. It is governed by the following expression:

$$V_{out} = (\frac{R_1}{R_2} + 1)V_{ref}$$

where, R_{ref} is 0.8V, R_1 is the variable resistance from the pot, R_2 is 3kΩ $[R_2 < 4.99k\Omega]$

A bypass pin as (shown in the schematic) can be used to give direct supply from the source, bypassing the LDO. Enable pin is set to high when the output voltage has to be turned on.

A total of 7 such modules were replicated to power-up the Tx-Chip. These modules are capable of supplying voltage of 1V - 2.5V.

5.5 Layouts

Keeping the above discussion in mind, the PCB design layout was done and the gerber files generated were sent to the manufacturer:

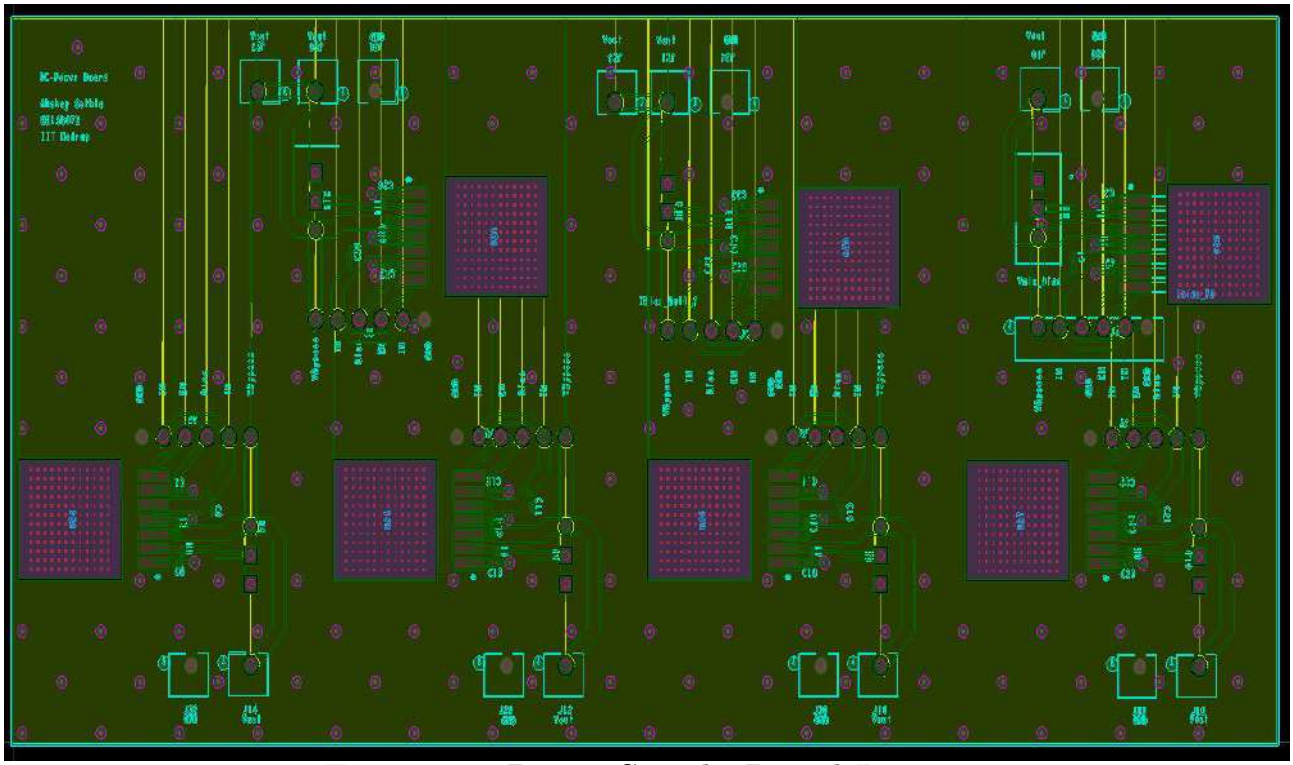

Figure 98: Power Supply Board Layout

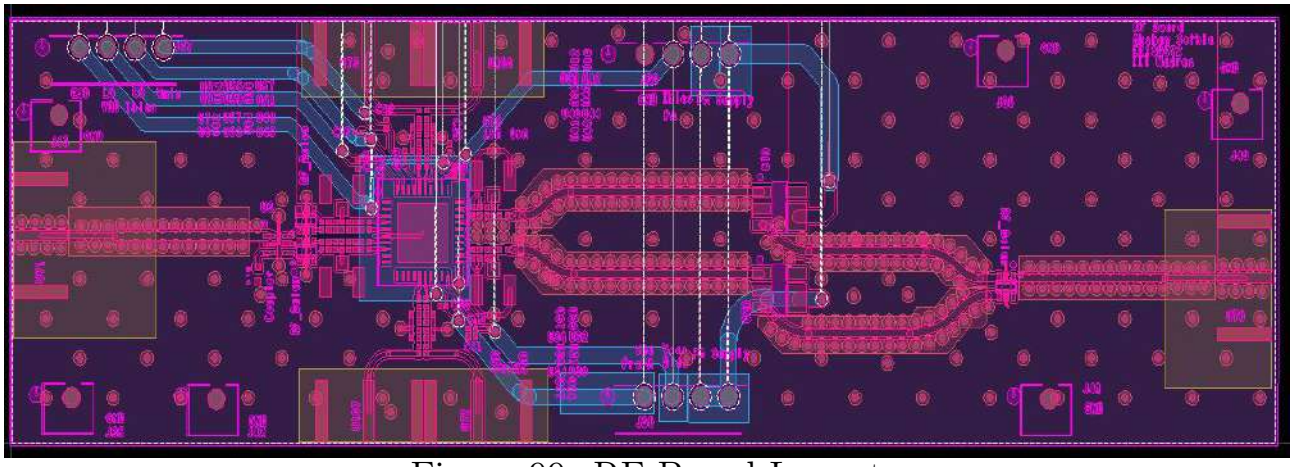

Figure 99: RF Board Layout

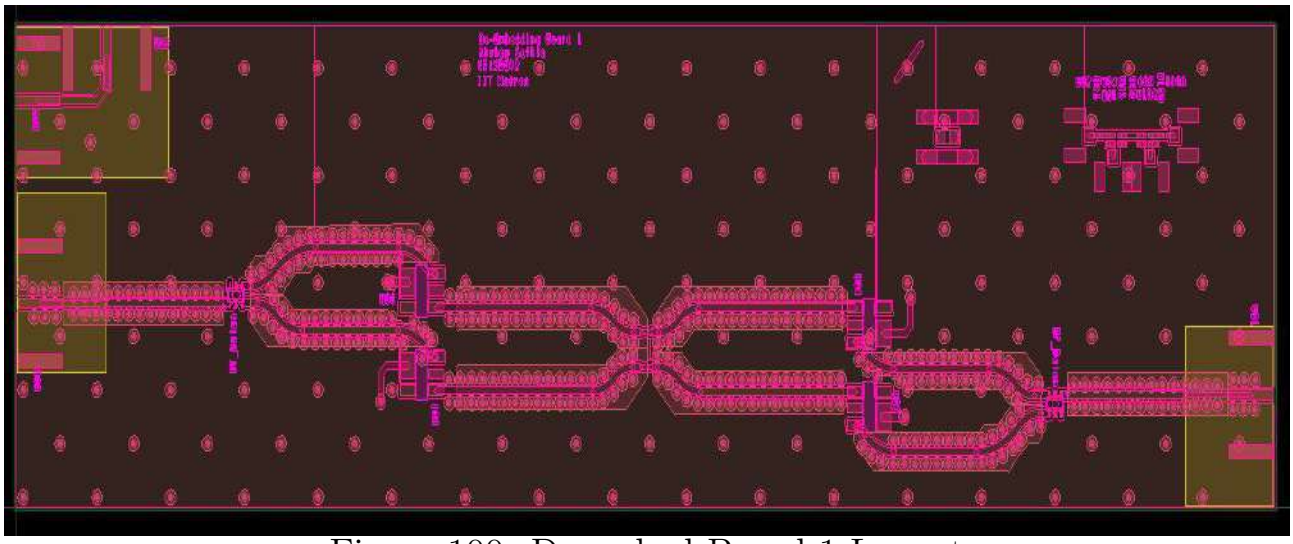

Figure 100: De-embed Board 1 Layout

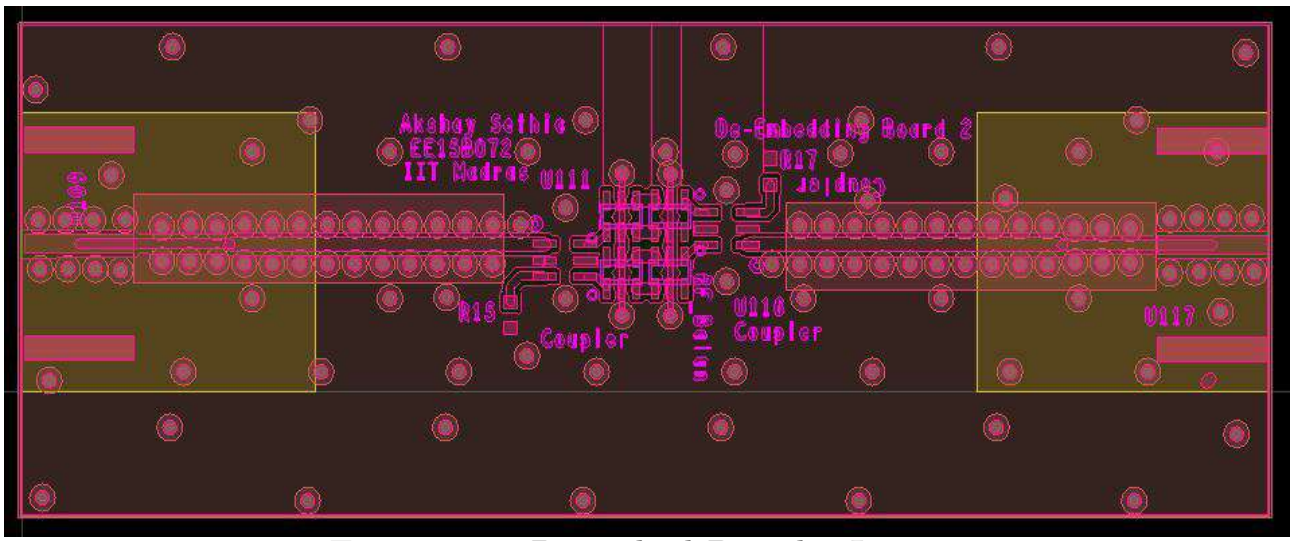

Figure 101: De-embed Board 2 Layout

6 Concluding Remarks & Future Scope

6.1 Concluding Remarks

The objective of the project was to design and test a Wideband transmitter with a flexible operating frequency ranging between 100MHz - 12GHz. It involved minimising the number of individual sub-blocks in the Transmitter and also improving their design and efficiency. We were able to merge all the sub-blocks of the transmitter into a single unit called power transmitter-operating in the given range of frequency- which reduced the number on-chip components significantly.

We were also able to design test boards for testing version-1 of the Transmitter, which involved designing critical RF-Traces for Wideband operations. The boards were designed using FR-4 technology for frequencies between 100MHz - 12GHz. These test boards were sent to the manufacturer for fabrication.

6.2 Future Scope

Although, a major part of the Transmitter has been designed and simulated, still there are some parts of the project which has to be done. A suitable matching network for the output of the Power Mixer with large drain capacitance and bond wire parasitics has to be designed. If that's successful, the chips can then be tapped-out and tested.

The PCBs were designed and fabricated, but due to time constraints, the testing wasn't completed. The version one of the chip is yet to be tested for the frequency band of 100MHz - 6GHz. If the testing is successful, the next step would be to test the chip for the frequencies between 6GHz-12GHz.

7 References

1 **Millimeter-wave Circuit and System Design in CMOS:** Basics and Recent Advances,Prof. Harish Krishnaswamy, Columbia University. Twenty third National Conference on Communications, IITM, Chennai, India.

2 **Wideband RF Transmitter in TSMC 65nm technology working from 100MHz to 12GHz:** KASYAP V KARUN

3 Sudip Shekhar, Jeffrey S. Walling and David J. Allstot, **"Bandwidth Extension Techniques for MOS Amplifiers "** IEEE Journal of Solid-State Circuits, vol.41, no. 11, pp.2424-2439, Nov 2006

4 Behzad Razavi, **RF Microelectronics**. Upper Saddle River, NJ, USA: Prentice Hall, 1998

8 Appendices

Python Code to generate Matching Network Component Values:

```
import math
f= input("Input the Oscillation Frequency:")
w=2*math.pi*f
Q=f/(600e6)
if Q<=2.3:
 Q=2.5


b=-31.25
a=351.5625/(Q*Q)
c=(Q*Q/4)+1
Rl1=(2*a)/(-b+math.sqrt(b*b-(4*a*c)))
Rl2=(2*a)/(-b-math.sqrt(b*b-(4*a*c)))
QL1=math.sqrt(12.5/Rl1-1)
QR1=math.sqrt(50/Rl1-1)
L12=50/(w*QR1)
C12=1/(w*w*L12)
C11=1/(w*QL1*(Rl1+(w*L12/40)))
L11=1/(w*w*(C11+1.2e-12))
C1=C11*C12/(C11+C12)
QL2=math.sqrt(12.5/Rl2-1)
QR2=math.sqrt(50/Rl2-1)
L22=50/(w*QR2)
C22=1/(w*w*L22)
C21=1/(w*QL2*(Rl2+(w*L22/40)))
#L21=1/(w*w*(C21+0.576e-12))
L21=1/(w*w*(C21+1.2e-12))
C2=C21*C22/(C21+C22)
print '\nTotal  Q=',Q
#print '\nQl= ', QL1, 'QR= ',QR1
```

```
#print 'net 1: (L1, L2, C)::',L11,L12,C1
print '\nQl= ', QL2, 'QR= ',QR2
print 'net 2: (L1, L2, C)::',L21,L22,C2
```