Full Duplex Receiver Using Time Selective Sampling of Received Signal in RF Domain

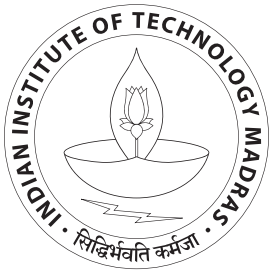
A Project Report

submitted by

SASANK GARIKAPATI

in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, MADRAS.
June 8, 2019

THESIS CERTIFICATE

This is to certify that the thesis entitled **Full Duplex Receiver Using Time Selective Sampling of Received Signal in RF Domain**, submitted by **Sasank Garikapati** (**EE15B057**), to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelors of Technology** is a bona fide record of the research work carried out by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Aniruddhan Sankaran
Research Guide
Associate Professor
Dept. of Electrical Engineering
IIT-Madras, 600 036

Place: Chennai

Date: June 8, 2019

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ABSTRACT

KEYWORDS: Full Duplex, Self Interference, Schematic, Layout

This work consists of the implementation of a novel method for accomplishing full-duplex communication using time selective sampling of the RF received signal at the antenna which is described in [1]. This work builds on an already existing architecture with a few blocks revamped for a better performance and with a few added features. The schematic level implementation of the circuit was optimized for noise and linearity. The layout of the circuit was completed clearing the DRC rules and matching the schematic and was sent for a tape-out. This work also deals with algorithms for retrieving the information in the signal from the time selective samples. The sampler was implemented in TSMC 65nm CMOS process and simulation results of parasitic extracted layout show a sensitivity of -71.8 dBm in the presence of a +5.6 dBm Tx signal. The received signal has a 20 MHz bandwidth, and the core receiver consumes 32.3mW from a 1.2 V power supply.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABBREVIATIONS

IBFD	In-Band Full Duplex
TDD	Time Division Duplexing
FDD	Frequency Division Duplexing
Tx	Transmitter
Rx	Receiver
SI	Self Interference
VCDL	Voltage Controlled Delay Line
PFD	Phase Frequency Detector
CP	Charge Pump
OTA	Operational Transconductance Amplifier
CMFB	Common Mode FeedBack
OFDM	Orthogonal Frequency Division Multiplexing
LLS	Linear Least Squares

CHAPTER 1

Introduction

(**Note:** The idea presented in this work has been published in [1] by Dr. Abhishek Kumar and this work primarily consisted of the implementation of the idea in circuit level.)

In typical wireless communication systems involving two terminals, each functioning as a transmitter and a receiver, the transmit signal and the received signal for each terminal is separated either in time or frequency. In the case where Time Division Duplexing (TDD) is employed, each of the terminals transmit and receive at different time slots but can use the same wireless channel for the link whereas in the case where Frequency Division Duplexing (FDD) is employed, each of the terminals transmit and receive simultaneously over different frequency bands. For an In-Band Full Duplex (IBFD) operation, the terminals transmit and receive simultaneously over the same frequency band. This could potentially *double* the spectral effeciency of the wireless communication system.

1.1 Challenges in In-Band Full Duplex

The main problem in implementing IBFD is the leakage from transmitter (Tx) to receiver (Rx) called the Self-Interference (SI) which poses serious challenges to the linearity of the RF frontend. This is due to the limited isolation from the Tx to Rx which results in a large amount of power (predominantly from the leakage

through Tx) at the input of the Rx thereby desensitizing the receive chain. In the case of TDD systems, since the Tx and Rx of a particular terminal do not operate simultaneously, there is no leakage from the Tx to Rx during the reception phase. In the case of FDD systems, use of frequency selective filtering which attenuates the signal at the Tx frequency helps in reducing the SI levels at the input of the Rx. This is however not possible in the case of same-channel Full Duplex (FD) systems since both the Tx and Rx use the same frequency band. Since the path loss is usually much greater than the isolation between the Tx and Rx, the component of Tx signal leaking into the Rx is much greater than the desired Rx signal. The SI must be suppressed as much as $106dB$ [2] for the SNR at the receiver to be equal to that of a TDD or FDD system. This SI, is usually suppressed over multiple domains (Antenna, RF, Analog and Digital) as a suppression of the order of $106dB$ is not feasible in a single domain.

1.2 Proposed Method

To accomplish SI-Cancellation, a time-selective sampling scheme is used which can potentially eliminate strong interference signals without the requirement of a high linearity RF front-end. In this work, we propose to sample the received signal at the antenna at the zero-crossing instants of the Self-Interference signal so as to generate SI-free samples. However, sampling a signal requires the tracking bandwidth of the sampler to be much greater than the maximum frequency of the signal. For RF pass-band signals, the maximum frequency content of the signal is a little greater than the carrier frequency ($f_c + 0.5B$). Hence, designing a sampler with such high tracking bandwidths is rather challenging. We instead try to implement a delay sampling approach which utilizes the implicit voltage to

delay conversion occurring at the antenna to simplify the design problem. This approach is explained in detail in Chapter 2.

CHAPTER 2

The Sampling Operation

The component of the received signal at the antenna containing information in both amplitude and phase can be represented as

$$V_{RX}(t) = A_{RX}(t)cos(\omega_c t + \phi_{RX}(t) + \phi_0) \tag{2.1}$$

Similarly, the component of the transmitted signal with the same carrier frequency leaking into the receive chain (self-interference) in a shared antenna system can be represented as

$$V_{TX}(t) = A_{TX}(t)cos(\omega_c t + \phi_{TX}(t)) \tag{2.2}$$

The zero-crossing instants of the self-interference during rising edges can be determined by Equation 2.3

$$\omega_c t_k + \phi_{TX}(t_k) = 2k\pi - \pi/2 \tag{2.3}$$

From Equations 2.1 and 2.3, we can determine the values of the samples of $V_{RX}(t)$ if it were sampled at the instants t_k by the Equation 2.4.

$$
\begin{aligned}
V_{RX}(t_k) &= A_{RX}(t_k)cos(\omega_c t_k + \phi_{RX}(t_k) + \phi_0) \\
&= A_{RX}(t_k)cos(\phi_{RX}(t_k) - \phi_{TX}(t_k) + \phi_0 + 2k\pi - \pi/2) \\
&= A_{RX}(t_k)sin(\phi_{RX}(t_k) - \phi_{TX}(t_k) + \phi_0)
\end{aligned} \tag{2.4}
$$

It can be observed from Equation 2.4 that the obtained samples are samples of the signal - $A_{RX}(t)sin(\phi_{RX}(t) - \phi_{TX}(t) + \phi_0)$ which is a baseband signal. This means that sampling the Rx signal at the zero-crossings of the Tx signal performs the down-conversion operation. However, the bandwidth of the sampled output becomes larger than that of the Rx signal due to the presence of phase modulation $\phi_{TX}(t)$ in $V_{TX}(t)$. This also makes the sampling operation non-uniform. Reconstruction of the original signal back from these samples can be accomplished with the complete knowledge of the Tx signal and is dependent on the type of modulation scheme, the number of samples obtained and the strength of the SI. For the special case when only amplitude modulation is present in both Tx and Rx, the obtained samples are the uniform samples of $A_{TX}(t)$ which is a baseband signal. Since the sampling rate is equal to the carrier frequency which is much larger than the bandwidth of the baseband signal, the Nyquist criterion is satisfied and the information contained can easily be retrieved from these samples. In a general case when information is contained in both amplitude and phase, more complicated reconstruction algorithms have to be implemented which shall be discussed further in Chapter 7.

2.1 Voltage to Delay Conversion

Directly sampling an RF signal requires a tracking bandwidth which is greater than the RF carrier frequency. Since the carrier frequency of the RF signal is usually very large, designing a sampler with such high tracking bandwidths is very challenging. The circuit design problem is greatly simplified by utilizing a delay sampling scheme described in [1].

For a shared antenna transceiver, the voltage at the antenna can be given by Equation 2.5

$$V_{ant}(t) = V_{TX}(t) + V_{RX}(t) \tag{2.5}$$

At the zero-crossing instants of $V_{TX}(t)$, the slope of $V_{TX}(t)$ is given by

$$S_{TX}(t_k) = \frac{d}{dt}[A_{TX}(t)cos(\omega_c t + \phi_{TX}(t))] \tag{2.6}$$

Assuming that the maximum frequency content of $A_{TX}(t)$ and $\phi_{TX}(t)$ is much smaller than ω_c, we can write this as

$$S_{TX}(t_k) \approx A_{TX}(t_k)\omega_c \tag{2.7}$$

Due to the presence of Rx signal, the zero crossing instants of $V_{ant}(t)$ get shifted with respect to the zero-crossing instants of $V_{RX}(t)$ to a first order approximation by $\Delta t(t_k)$ given by Equation 2.8

$$\Delta t(t_k) = \frac{V_{RX}(t_k)}{S_{TX}(t_k)} \tag{2.8}$$

From Equation 2.8, we can determine $V_{RX}(t_k)$ from $\Delta t(t_k)$ with the knowledge of $A_{TX}(t_k)$ and ω_c as

$$V_{RX}(t_k) = \Delta t(t_k) A_{TX}(t_k) \omega_c \tag{2.9}$$

Thus, by measuring $\Delta t(t_k)$, which is the delay between the edges of the signal at the antenna and the SI, we can determine $V_{RX}(t_k)$

CHAPTER 3

Implementation of the Sampler

The sampler proposed in [1] aims to convert the delay between the zero-crossing instants of two signals into a return to zero sample and hold voltage waveform. The block level architecture of the sampler is shown in Figure 3.1

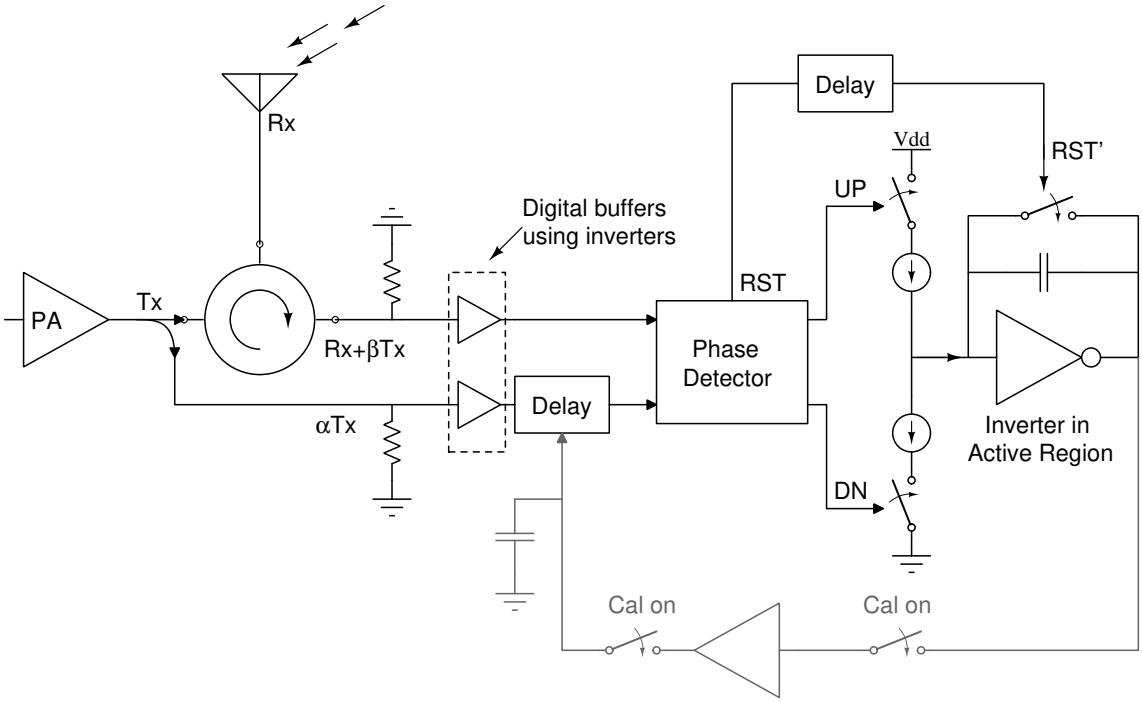

Figure 3.1: Block level architecture

A coupled Tx signal and the signal at the antenna are fed to buffer which hard limits the signal to rail voltages but preserves the zero-crossing instants of the signals. The coupled Tx signal is used as a reference from which the delay of the signal at the antenna is to be calculated. An additional delay offset is introduced between the paths so as to compensate for any delay mismatch in the Antenna and the tapped Tx path and the amount of delay required is set by a calibration loop. A

tri-state phase detector is used to determine the delay in the zero-crossings of both the paths. The signals from the phase detector are sent to a charge pump which pumps in charge proportional to the delay between both the paths. This charge is sampled on an active capacitor and is held until the RST' signal arrives. The signal RST' can be generated from the reset signal of the tri-state PFD by delaying the reset signal by an amount which decides the hold time of the sampler. When the RST' signal arrives, the charge on the capacitor is discharged through the switch and the capacitor becomes ready for the next sample to arrive.

The calibration loop is a delay locked loop incorporating an Operational Transconductance Amplifier (OTA) with a large gain followed by a capacitor essentially acting as an integrator. This loop tweaks the delay in the delay element such that the final output voltage ideally reaches 0. During the calibration phase, the antenna port must be disabled so as to have the same signal in both the paths. A a switch is added after the amplifier which can be used to disable the calibration loop and the voltage required to compensate for the delay is stored on the capacitor following the OTA. During the operation phase, the delay between both the paths is relatively slow to change and hence the switch closing the calibration loop can be opened.

3.1 Gain of the circuit

From Figure 3.1, we can write the output sampled voltage $V_{out}(t_k)$ in terms of delay $\Delta t(t_k)$ as

$$V_{out}(t_k) = \Delta t(t_k)\frac{I_{CP}}{C_{CP}} \tag{3.1}$$

From Equations 2.4 and 3.1, we can write

$$V_{out}(t_k) = \frac{1}{A_{TX}(t_k)\omega_c}\frac{I_{CP}}{C_{CP}}V_{RX}(t_k) \tag{3.2}$$

From Equation 3.2, we can observe that the gain of the circuit depends on the frequency of operation as well as on the amplitude of the Tx signal at that instant. This means that, in presence of amplitude modulation, the gain of the circuit can change over time. However, since the information about the transmit signal is present at the receiver, the output samples can be scaled appropriately to account for the variation in the gain.

CHAPTER 4

Schematic Level Design

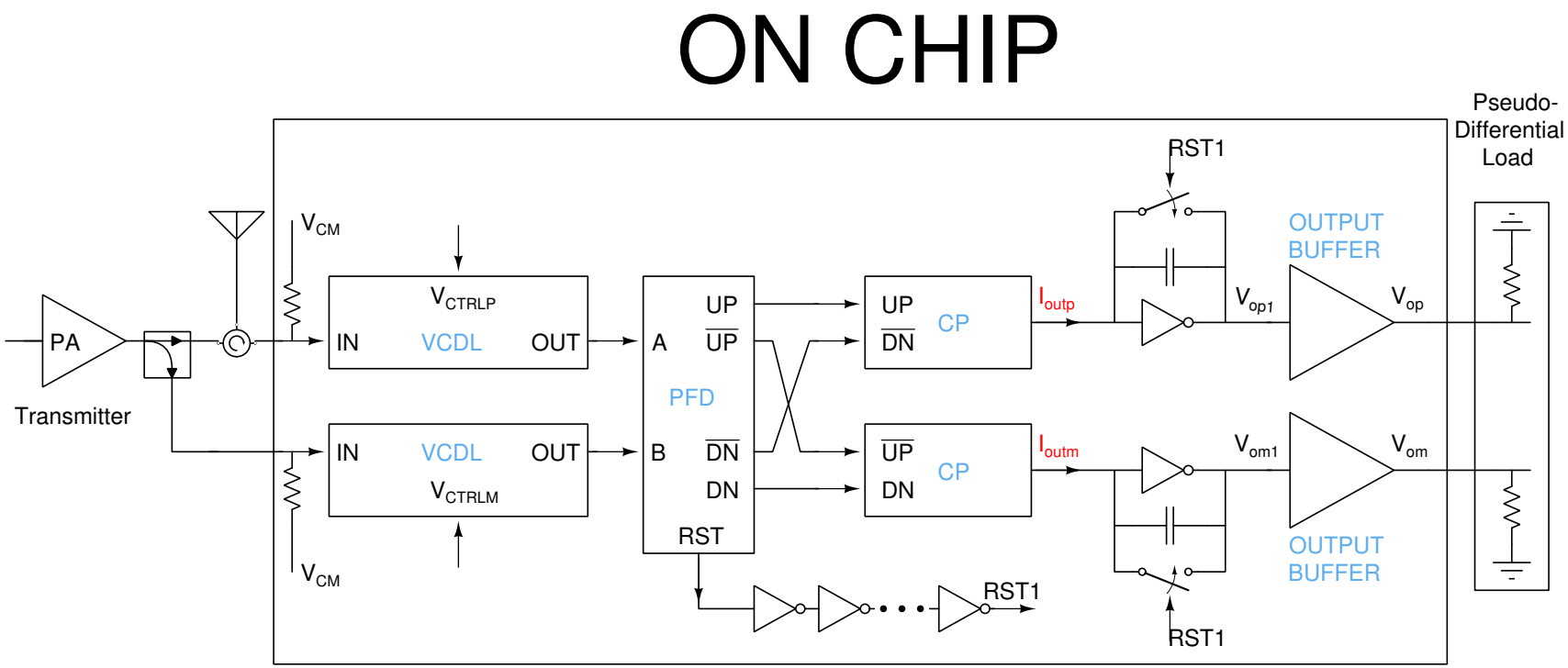

Figure 4.1: Overview of the schematic level design

The overview of the schematic level design (without the calibration loop) is shown in the Figure 4.1. The calibration loop is separately discussed in Section 4.8.

The various blocks in the design are described in the following sections.

4.1 Voltage Controlled Delay Line

The schematic of the VCDL is shown in Figure 4.2.

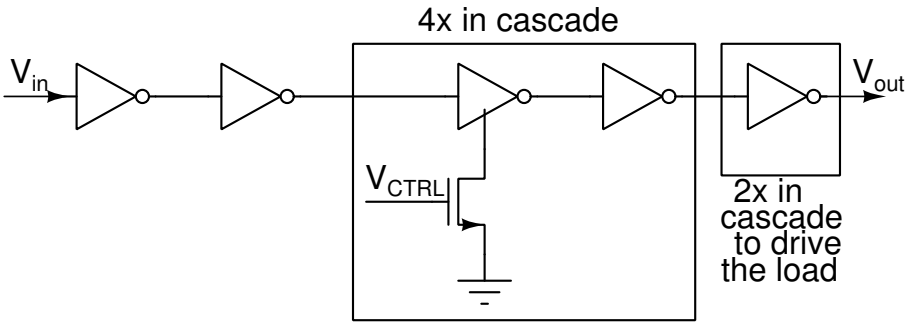

Figure 4.2: Voltage Controlled Delay Line

The VCDL is made of a cascade of inverters which hard limit the signal. A cascade of current starved inverters is used to produce a large amount of relative delay. The first inverter in the VCDL is made with large transistor widths so as to have minimum noise and be able to drive the load easily which results in a higher slope of the output waveform which reduces the noise injected by the subsequent blocks. It also uses thick-oxide devices for better power handling. The width of the first transistor is chosen such that the input capacitance does not affect the input matching too much and also on the other hand, the slope of the output waveform is limited by the gain of the inverter and not by the capacitance of the succeeding stage. Current starving the NMOS transistor in alternate inverters helps in exclusively delaying the rising edge of signal as only the rising edge of the signal is used by the PFD. This also precludes the need of having another

complementary control signal for the PMOS current if both the edges are to be delayed. This has an impact in the on-time of the input signal. However, since the delays we are interested are a small fraction of the on time (of the hard limited input signal), even though the on time reduces a little, there is no impact on the delay to voltage conversion characteristics.

The delay characteristics of the VCDL is shown in Figure 4.3.

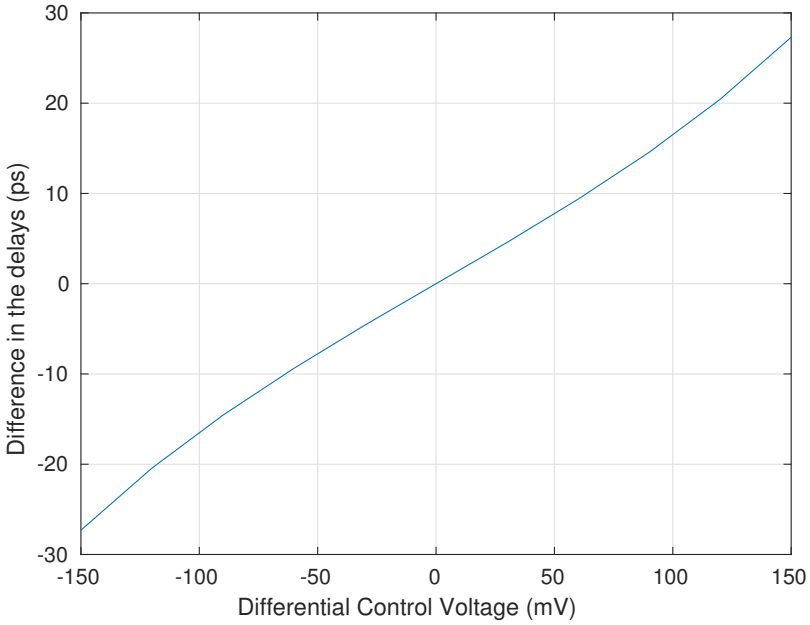

Figure 4.3: Characteristics of the VCDL

From Figure 4.3, we can observe that the VCDL can compensate for a relative delay of around $50ps$ in both the paths with a control voltage range of around $300mV$. In this, the differential control voltage rides on a common mode value of $750mV$. Further increasing the control voltage increases the delay but adversely affects the noise performance of the VCDL.

4.2 Input Resistor Bank

For matching the input to 50Ω, a 3-bit resistor bank is used which accounts for the change in resistance across process and temperature. The implementation of the resistor bank is shown in Figure 4.4.

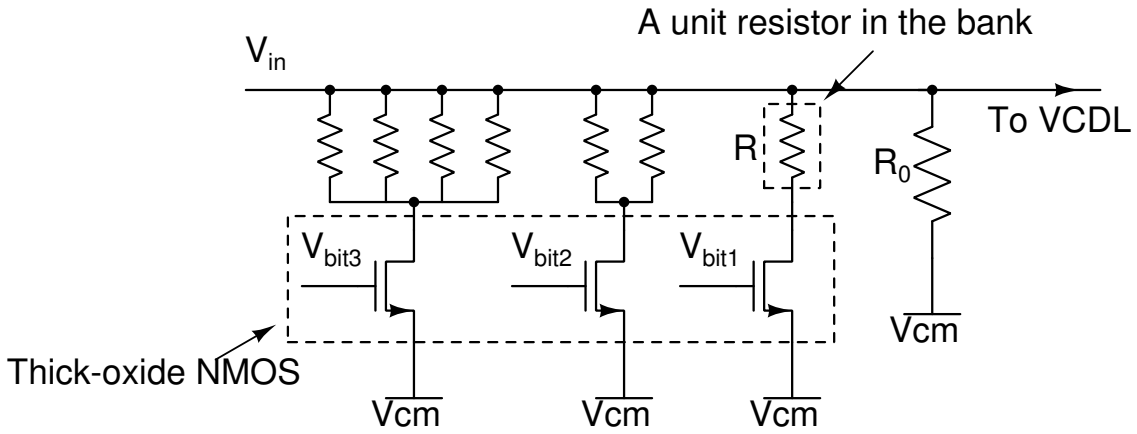

Figure 4.4: Input Resistor Bank

Thick-oxide NMOS devices were used for switches as Vcm is close to $600mV$ and hence a thin-oxide device might not get fully turned on on application of $1.2V$ at the gate of the device. So instead, $2.5V$ can be given to thick oxide device and since $2.5V - 0.6V = 1.9V > V_{th}$ of NMOS devices, the switch gets turned on.

4.3 Phase Frequency Detector

The implementation of the PFD is shown in Figure 4.5.

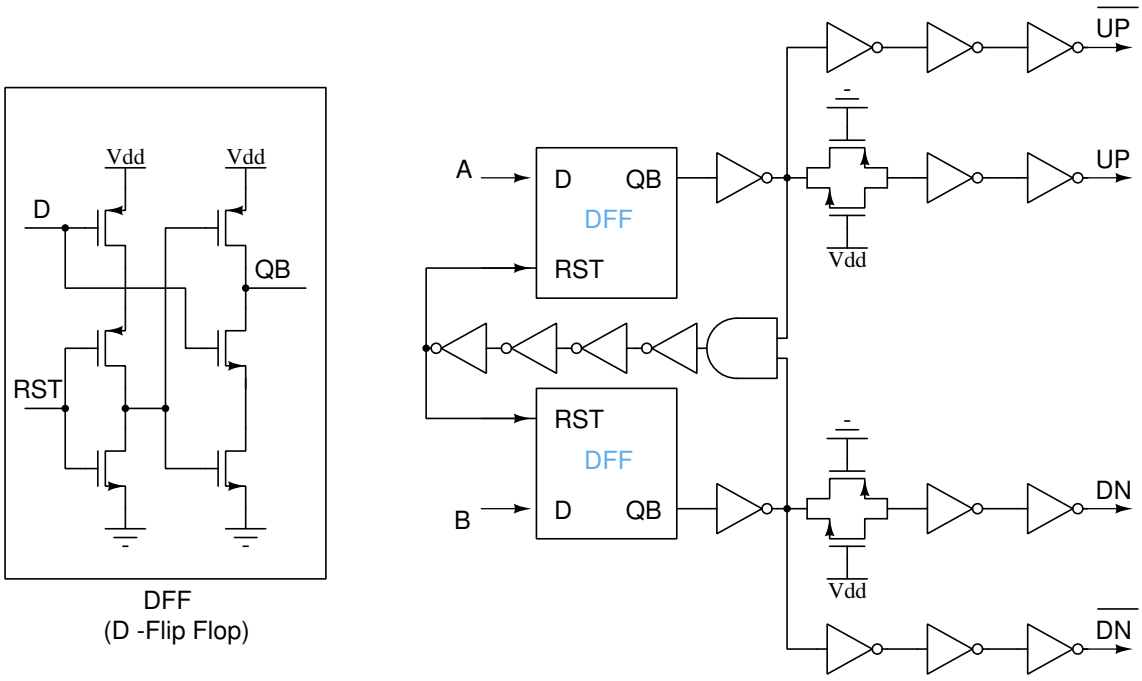

Figure 4.5: Phase Frequency Detector

The PFD is implemented using resettable D - flip flops, inverters and an AND gate. The D - flip flops used are modified TSPC flip-flops [3] which satisfy the required function for the PFD (the input is always VDD and the flip-flop can be reset). This flip-flop was used for the high speed requirement of the PFD. The AND gate is designed with strong PMOS transistors and weak NMOS transistors. This not only reduces the delay in the occuring of the rising edge but also gives a larger width for the reset pulse. This larger width of the reset pulse proves to be helpful in the reset stage which generates the reset signal for resetting the active capacitor. A transmission gate switch is used in the path to generate the *UP* and *DN* signals so that the edges of *UP* and $\overline{UP}$ coincide with each other which prevents offset in the output of the charge pump. The inverters act as buffers so as the drive the load capacitances of the charge pump and in the case of reset path, of the D - flip flop.

4.4 Charge Pump

The implementation of the Charge Pump (CP) along with its bias circuit is shown in Figure 4.6.

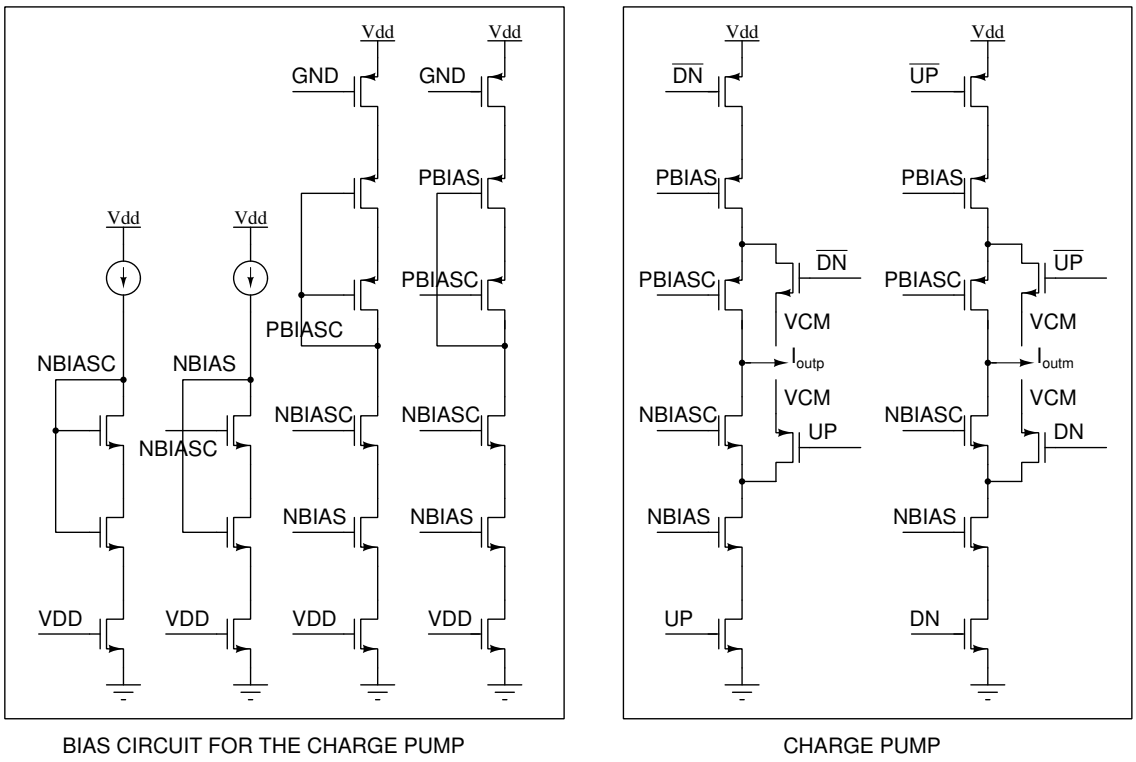

Figure 4.6: Charge Pump

The charge pump uses a source switched topology as it proved to have lesser feedthrough from the pulsed signals. A cascode structure was used to alleviate the effect of channel length modulation on the CP current. However, in a normal source switched charge pump, the time taken for the charge pump current to die down is large and even during the hold time, the charge pump injects charge into the active capacitor which is undesirable. Therefore, another switch is used to set the source voltage of the cascode transistor to Vcm, which is generated by a self-biased inverter. Doing so helps in quickly cutting off the current of the cascoded transistor and prevents any charging of the capacitor during the hold time. This switch is

implemented using the complementary transistor of the current controlling switch and is given the same signal as the current controlling switch. The bias circuit of the charge pump utilizes a poor man's cascode topology to generate the bias of the cascode devices and normal current mirror techniques for generating the bias of the current sources.

4.5 Active Capacitor and Reset Stage

The implementation of the active capacitor following the charge pump along with the circuit to generate the reset signal to reset the charge on the capacitor is shown in Figure 4.7.

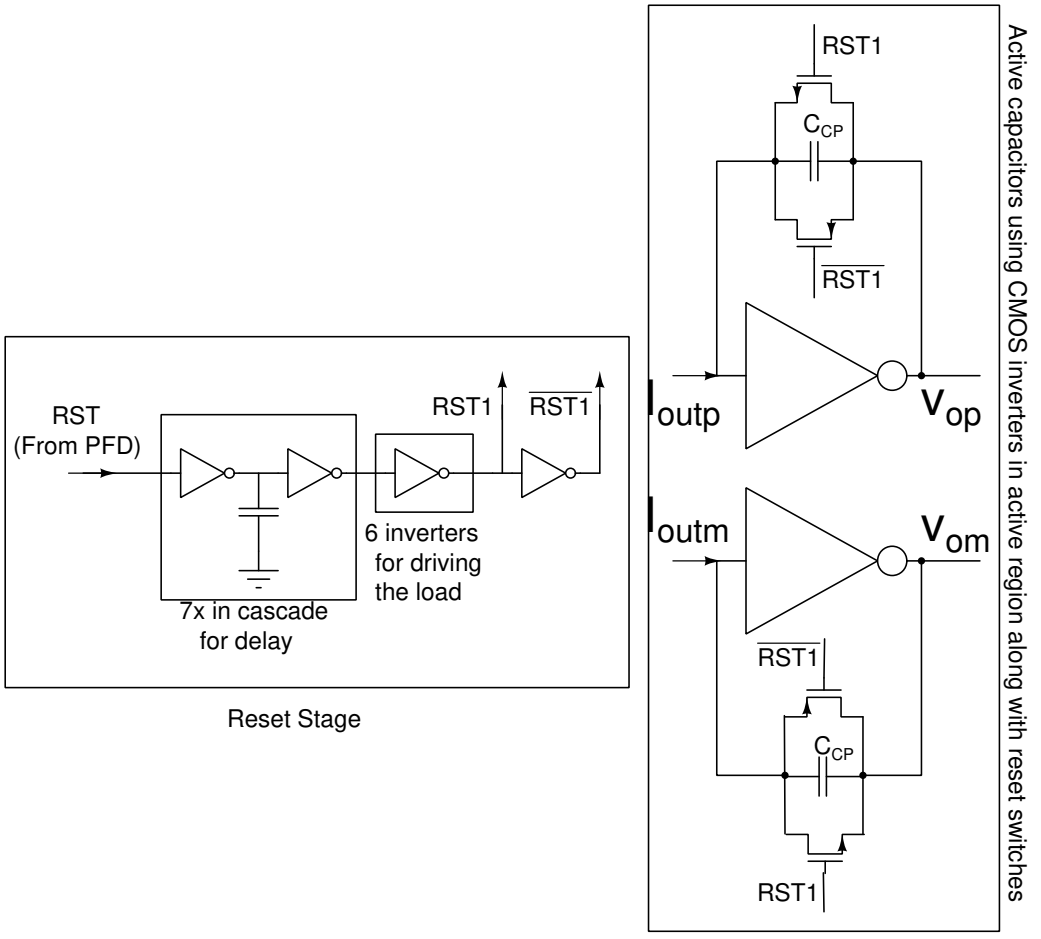

Figure 4.7: Active capacitor and reset stage

To store the charge injected by the charge pump, an active capacitor is used which incorporates an amplifier (implemented using CMOS inverters in active region) to ensure that the voltage at the drain of the current sources in the charge pump does not swing much. Initially the capacitor is reset and the CMOS inverters are self-biased due to the reset signals. When the charge pumps starts pumping current, since inverters are in the active region, the negative feedback ensures that the input of the inverter doesn't change much from the self-bias voltage. The total differential charge injected by the differential charge pump gets stored on the capacitors and the difference between the output voltages is proportional to the amount of differential charge injected by the charge pump.

4.6 Output Buffer

The implementation of output buffer along with a reset stage for its switch based biasing scheme is shown in Figure 4.8.

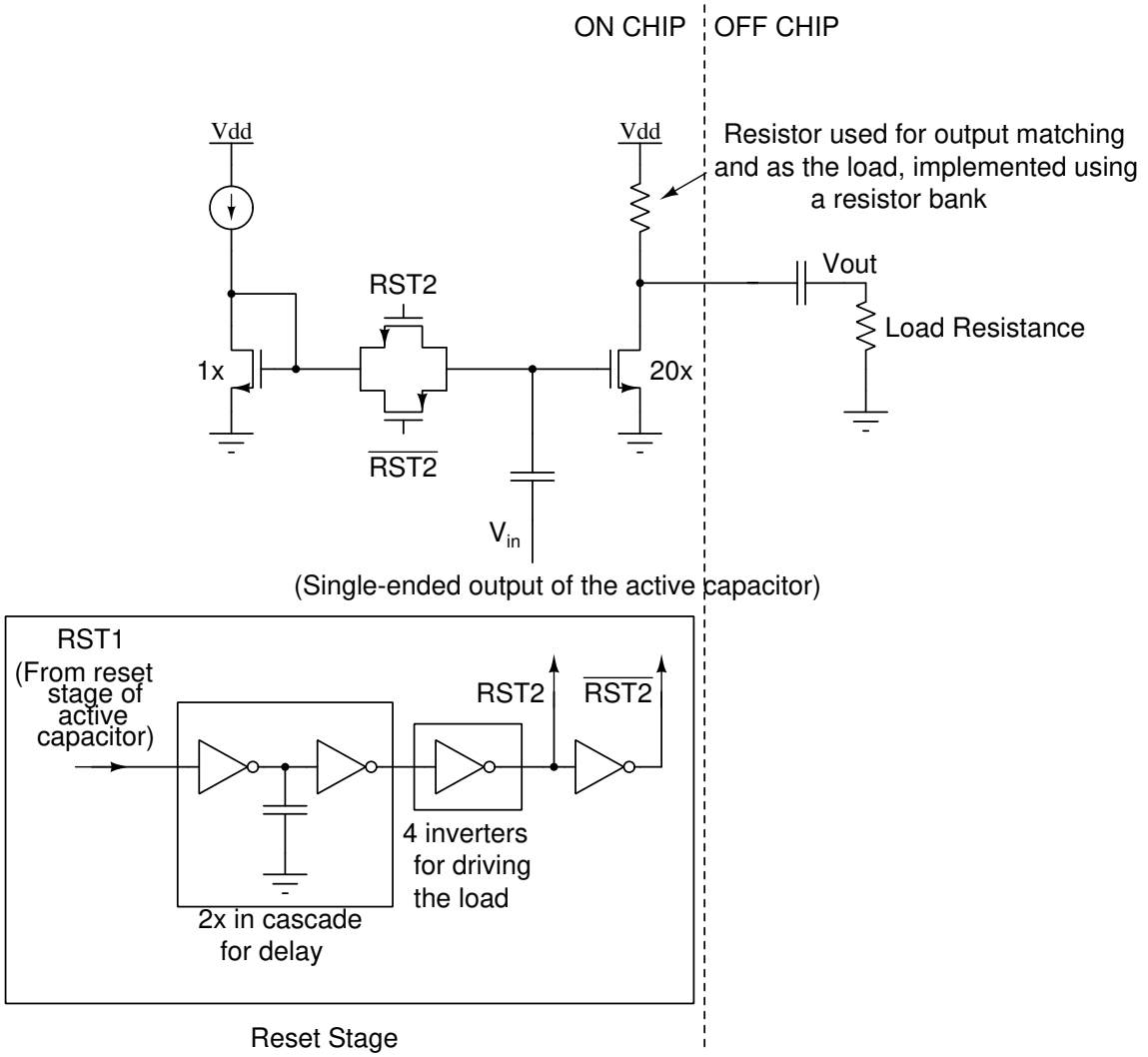

Figure 4.8: Output Buffer and Reset Stage for Biasing

The purpose of the output buffer is to drive the output load of 50Ω assumed to be that of the oscilloscope displaying the output waveform. Two single-ended common source amplifiers with resistive loads were employed for the buffer. This resistive load is also used to match the output to the load and hence is implemented using a 3-bit resistor bank to account for the process and temperature variations. Since the input to this buffer comes from the single-ended output of the active capacitor, which is a pulsed waveform whose height is of importance, an AC coupling capacitor was used to couple the output of the active capacitor to the input of the common source stage. However, a switch based biasing schemes is

used in which the quiescent voltage before the pulse arrives is set to the required DC voltage generated using a current mirror. This method is used because the input pulses, as discussed before are samples of $A_{RX}(t)sin(\phi_{RX}(t) - \phi_{TX}(t) + \phi_0)$ and could also possibly contain DC content. Thus merely AC coupling the output of the active capacitor will not work and can alter the quiescent voltage at the input of the output buffer. The DC voltage is reset after every pulse using a reset signal which is a delayed version of the reset signal used to reset the active capacitor.

4.6.1 Output Resistor Bank

The output resistor bank is implemented in a similar way as that of the input resistor bank but using PMOS switches as the resistor is connected to Vdd instead of Vcm. The implementation of the resistor bank is shown in Figure 4.9.

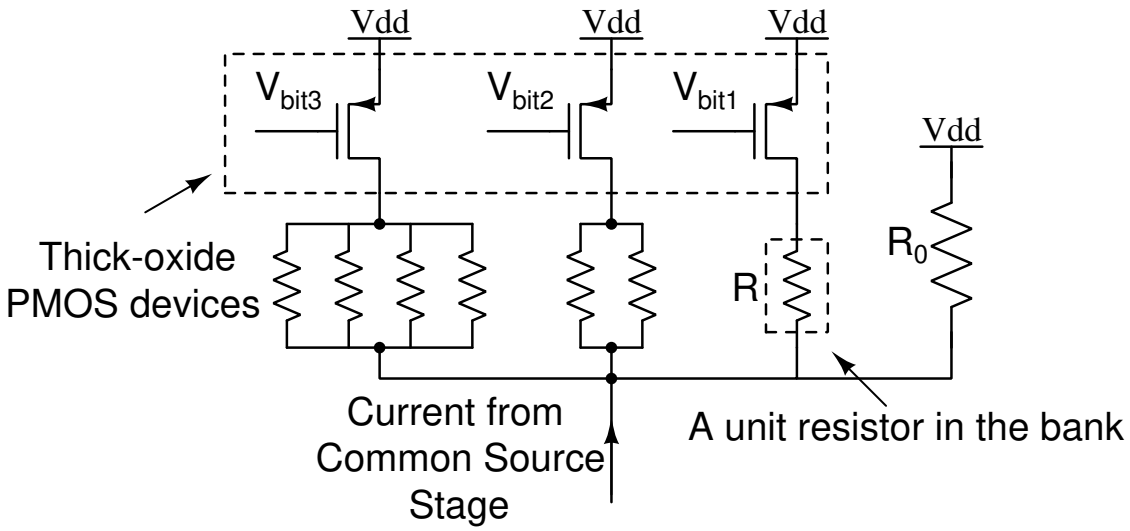

Figure 4.9: Output Resistor Bank

4.7 Reset Buffer

The purpose of the reset buffer is to buffer the reset signal from the PFD enough such that it can drive a 50Ω load. A delayed version of the reset signal can be used as a clock to sample the output signal as the reset pulse arrives every time a sample arrives. The reset buffer is implemented using a chain of sufficient number of inverters so as to drive a 50Ω load without changing the slope of the signals significantly. Another chain of inverters are used to generate the complement of the reset signal with one of the inverters replaced by a transmission gate to ensure matching in the delays. This helps in obtaining a differential clock signal and will not be affected much by supply noise.

4.8 Calibration Loop

The architecture of the calibration loop is shown in Figure 4.10

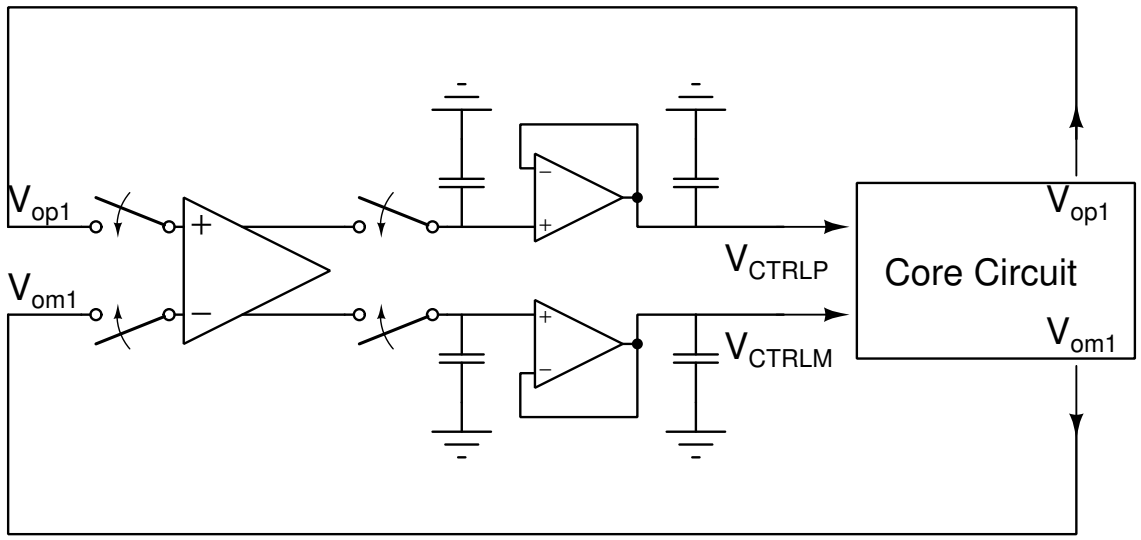

Figure 4.10: Calibration Loop

When the calibration loop is set to run, the switches in Figure 4.10 are closed. The received signal is assumed to be off and thus difference in the delays in both the paths will result in an output pulse generated by the core circuit, whose height is proportional to the delay. These output pulses are fed to a 5-transistor differential Operational Trans-conductance Amplifier (OTA) followed by capacitors. The OTA followed by the capacitors act as an integrator which integrates the sampled voltage. Ensuring negative feedback by controlling the voltages of the VCDLs appropriately, the delay in both the paths can be made equal. These capacitors store the voltage which is supposed to control the VCDLs after the calibration loop is switched off. However, since the control voltage of the VCDL goes to the gate of a thin-oxide CMOS transistor, whose gate-leakage current is substantial, the capacitor tends to discharge at an intolerable rate. Thus, a buffer implemented using a single-ended OTA (in unity gain feedback) employing thick-oxide transistors which have substantially lower gate leakage is placed after these capacitors. A capacitor is placed after this buffer to ensure that there is no high-frequency noise at the input to the VCDL, however, this capacitor cannot be large enough because the pole introduced by the buffer should be at a high frequency to ensure proper stability.

The switches in the calibration loop are implemented using transmission gates switches.

4.8.1 Calibration Loop Amplifier

The implementation of the OTA in calibration loop is shown in Figure 4.11

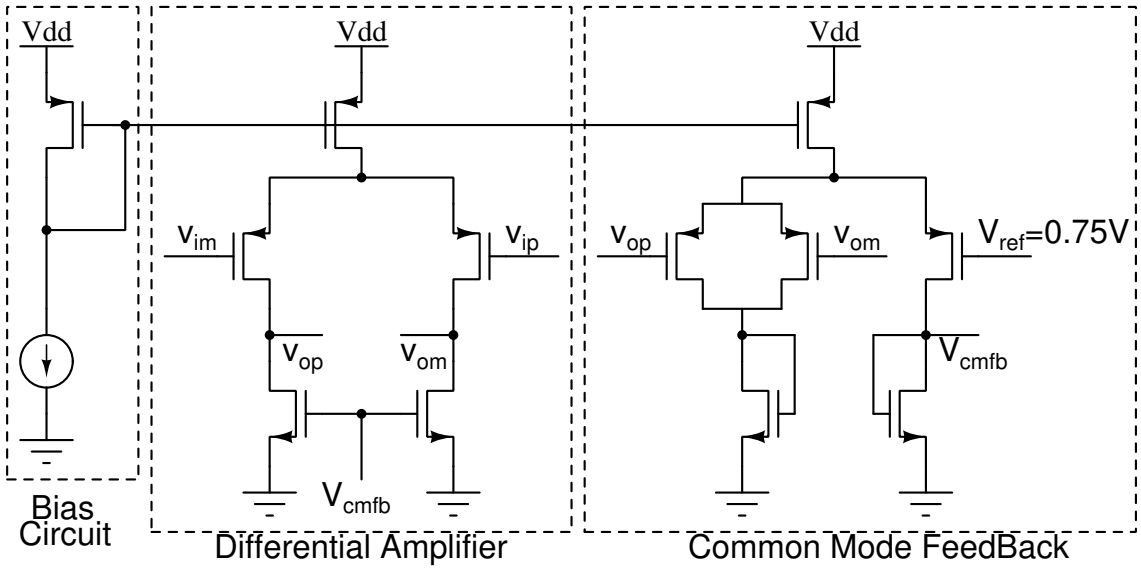

Figure 4.11: OTA in calibration loop

The OTA uses a 2.5V supply and thick oxide devices. A PMOS input stage was used as the common mode voltage at the input to this amplifier is 600mV which is very close to the V_{th} of a thick-oxide NMOS device. The common mode of the output is set using a Common Mode FeedBack (CMFB) circuit to 750mV which is the common mode assumed by the VCDL. A diode connected load with same width as the active load in the OTA was used in the CMFB circuit and the tail current source also has the same width as that of the OTA. The CMFB circuit does not require a high gain as the gain provided by the differential amplifier's NMOS transistor is quite large. The relatively lesser gain also helps in having a better phase margin for the CMFB.

4.8.2 Buffer for the Control Voltages

The implementation of the control voltage buffers is shown in Figure 4.12.

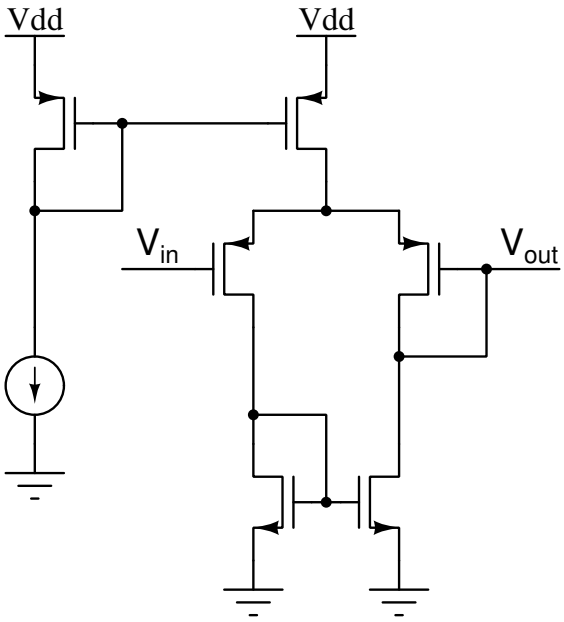

Figure 4.12: Buffer for the control voltages in calibration loop

The buffer for control voltages also uses a $2.5V$ supply and a PMOS input device as the input common mode voltage is $750mV$ and can go as low as $600mV$ which will drive a thick-oxide NMOS into cut-off region if used.

CHAPTER 5

Layout Snapshots

The top level snapshot of the layout is shown in Figure 5.1.

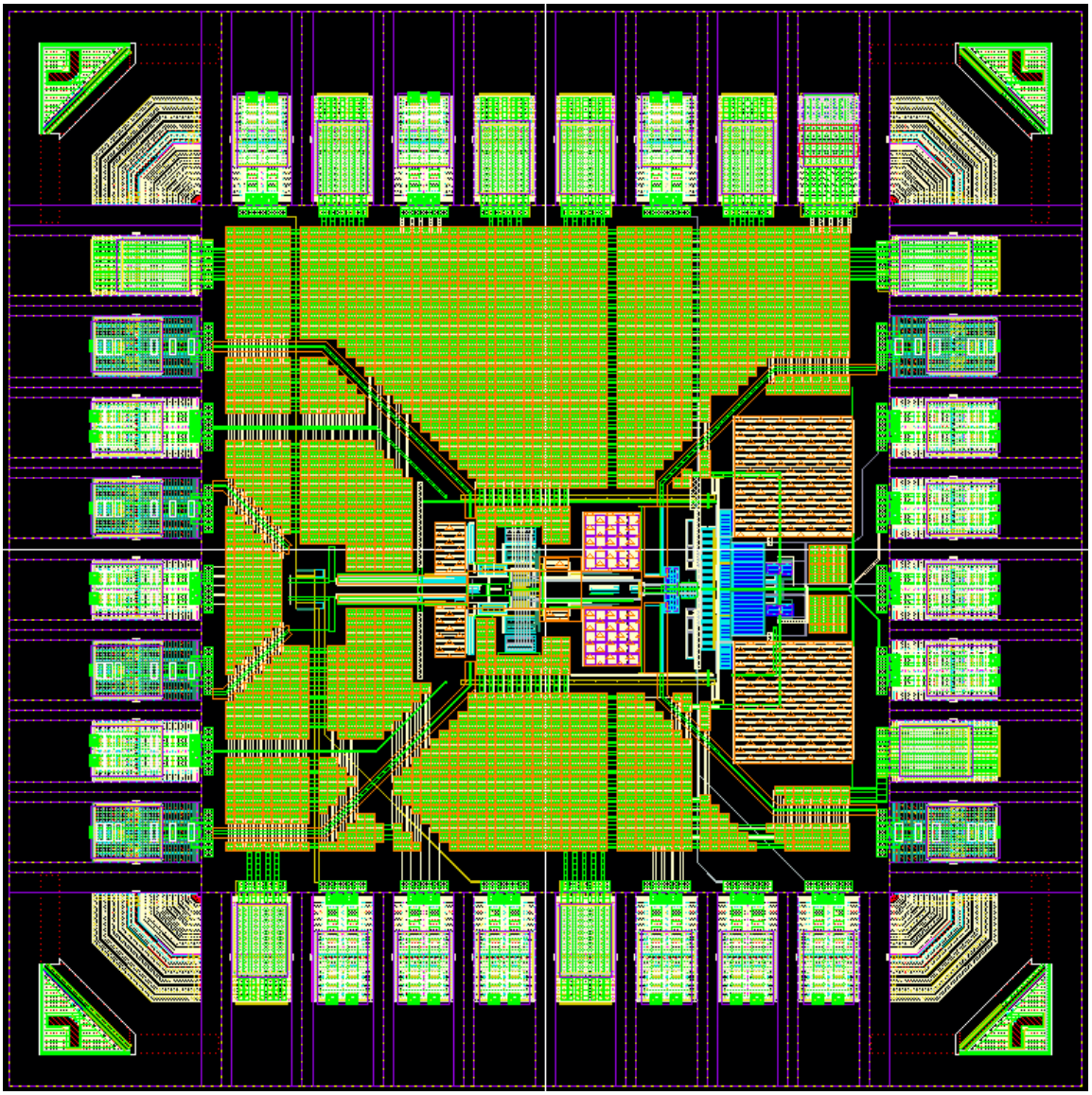

Figure 5.1: Top Level Snapshot of the Layout

The layout without the pad ring and decaps is shown in Figure 5.2

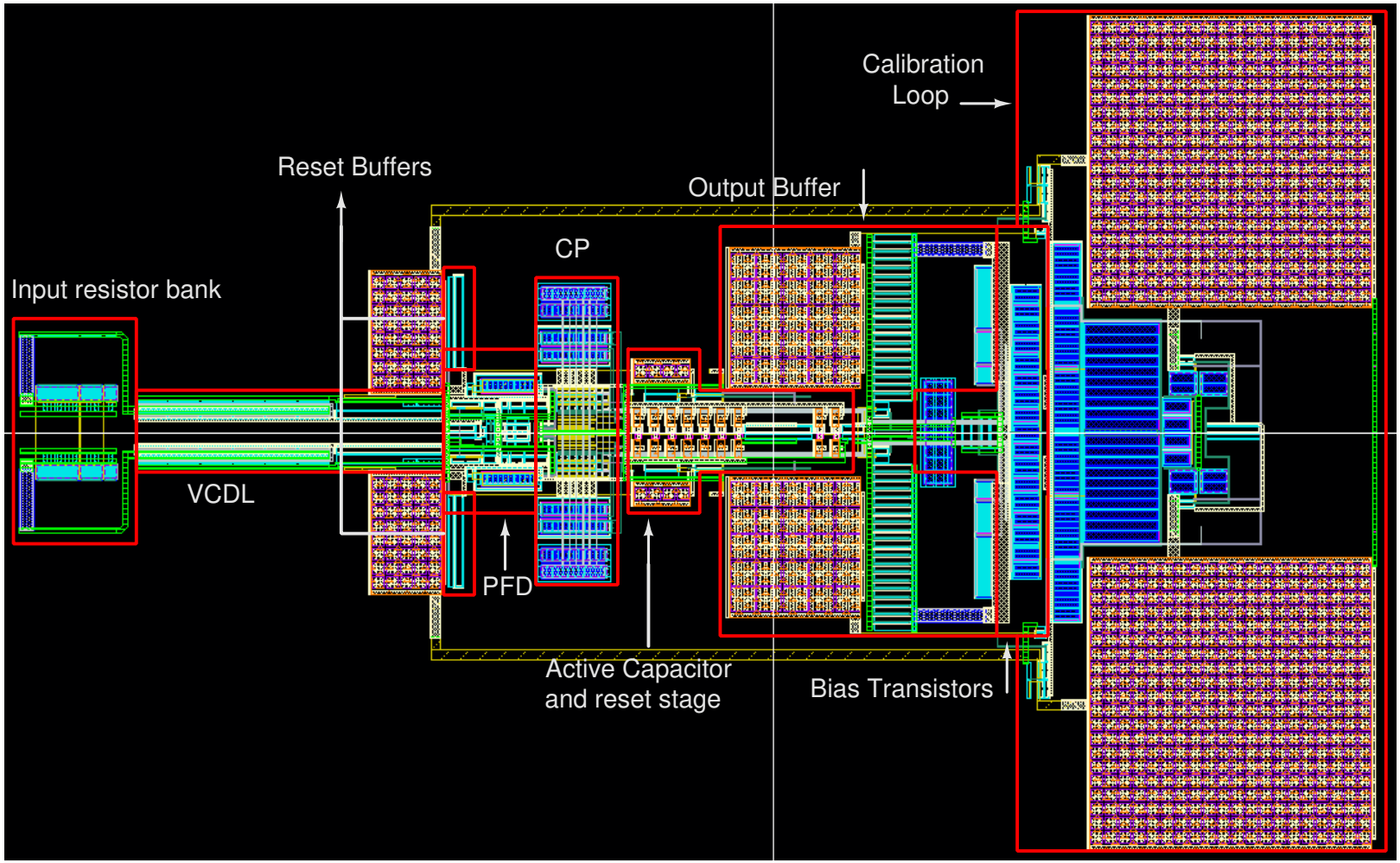

Figure 5.2: Layout without pad rings and decaps

26

CHAPTER 6

Simulation Results

This chapter deals describes the performance of the circuit through simulation results run on Cadence SpectreRF platform. It is divided into two sections:

1. Schematic level simulation results which describe the results obtained before the parasitic extraction of the layout.
2. Parasitic extracted simulation results which describe the results obtained after the parasitic extraction of the layout.

All the simulations were performed along with pad capacitances and bond-wire inductances. The Tx components of the cancellation path and the receive path are assumed to have an amplitude of $600mV$ unless otherwise stated.

6.1 Schematic Level Simulation Results

This section describes the simulation results which were obtained before the parasitic extraction of the layout.

6.1.1 Delay to Voltage Conversion Characteristics

The delay to voltage conversion characteristics of the sampler is shown in Figure 6.1. The delay in the input and the cancellation path is varied from $0ps$ to $70ps$ and the output sampled voltage is plotted against it. Also, the ratio between the output

sampled voltage and the delay (which gives a measure of the gain) is plotted on the same figure.

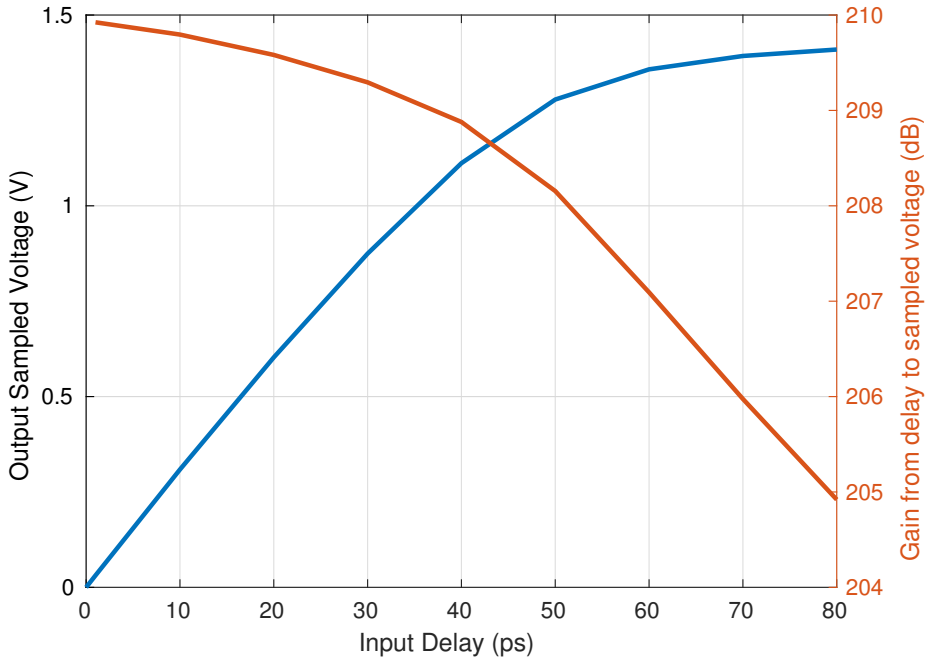

Figure 6.1: Delay to voltage conversion characteristics of the schematic level design

6.1.2 Noise Performance

The noise performance of the sampler is shown in Figure 6.2. The delay in the input is varied from 0*ps* to 70*ps* and the output sampled noise is plotted against it.

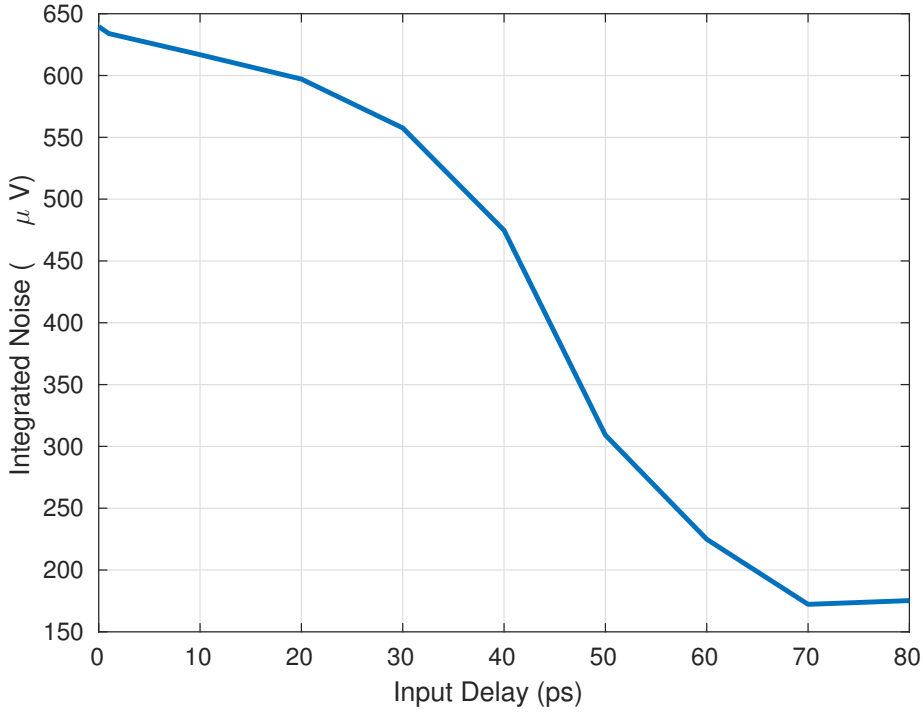

Figure 6.2: Noise performance of the schematic level design

We can observed that the noise seems to be decreasing with increase in input delay which seems counter-intuitive. However, if we divide the noise by the gain of the circuit at the operating point corresponding to the delay, we get input referred noise as shown in Figure 6.3. This gain is different from the gain plotted in Figure 6.1. For noise, we must assume that the circuit is operating at an operating point corresponding to the input delay and to obtain the input referred noise, the noise must be divided by $\frac{dV_{out}}{dV_{in}}$ at the given t_d. For the linearity performance, we measure the value of $\frac{V_{out}}{V_{in}}$.

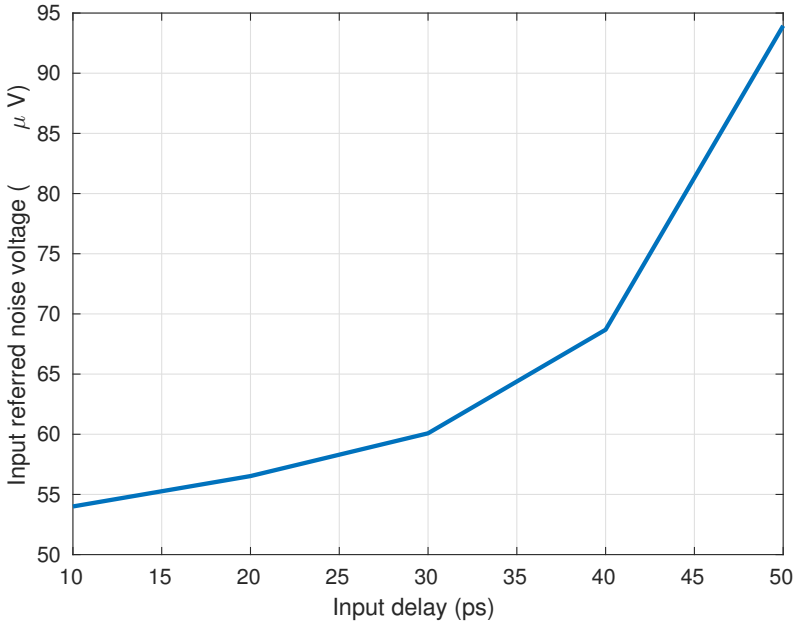

Figure 6.3: Input referred noise of the schematic level design

The output noise of the circuit also depends on the amplitude of the Tx component in both the paths. The integrated output noise variation with the Tx amplitude is shown in Figure 6.4.

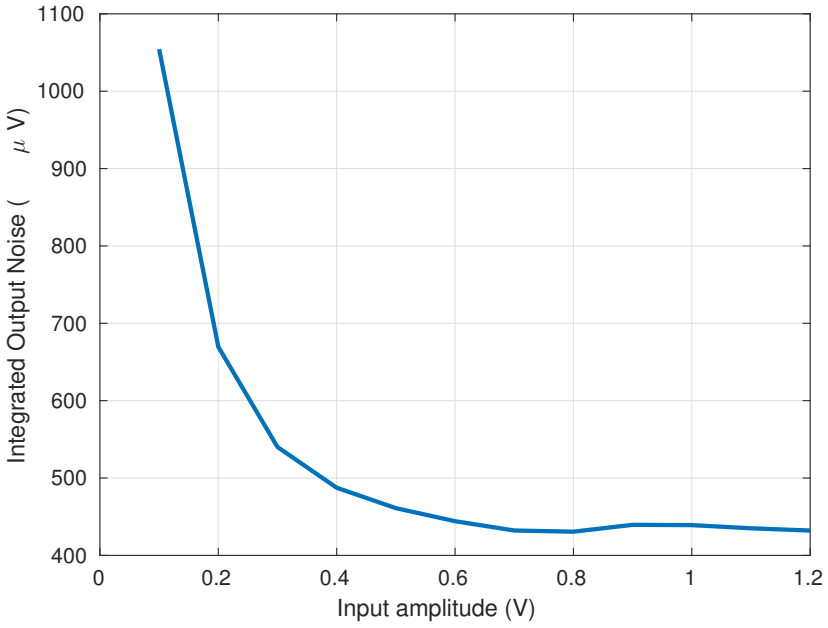

Figure 6.4: Output noise variation with Tx amplitude

The gain of the circuit is dependent on the amplitude of the Tx component and thus the input referred noise doesn't scale by the same factor when derived from output noise for different amplitudes. The input referred noise variation with Tx amplitude is shown in Figure 6.5.

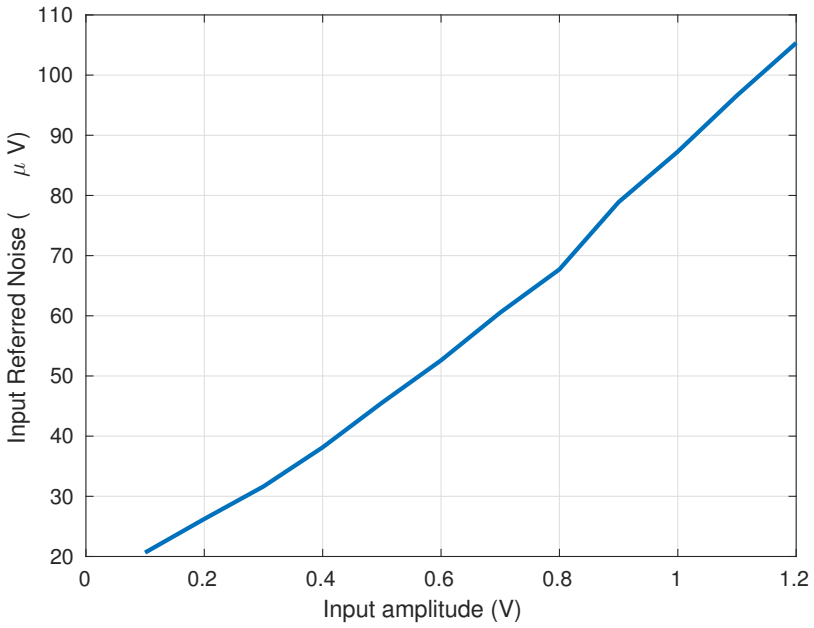

Figure 6.5: Input referred noise variation with Tx amplitude

We can observe from Figure 6.5 that the input referred noise is better for a lower Tx amplitude. The input referred noise directly translates to the noise figure and hence, the noise figure of the receiver improves with reduction in the amplitude of the Tx component. Therefore, any isolation between the Tx path and the Rx path improves the noise performance of the circuit.

6.1.3 Input and Output Matching

Resistor Banks

The value of the input resistor bank's resistance at different process corners for different codes is shown in Table 6.1.

Code	TT Corner	FF Corner	SS Corner
000	73.8Ω	51.8Ω	95.7Ω
001	62.8Ω	43.5Ω	82.1Ω
010	54.6Ω	37.5Ω	71.9Ω
011	48.3Ω	32.9Ω	63.9Ω
100	43.3Ω	29.3Ω	57.5Ω
101	39.3Ω	26.5Ω	52.3Ω
110	35.9Ω	24.1Ω	47.9Ω
111	33.1Ω	22.1Ω	44.2Ω

Table 6.1: Input resistor values for different bit codes

The value of the output resistance (resistor bank in parallel with the *rds* of the NMOS transistor) at different process corners for different codes is shown in Table 6.2.

Code	TT Corner	FF Corner	SS Corner
000	35.2Ω	24.6Ω	45.7Ω
001	37.7Ω	26.5Ω	48.8Ω
010	40.6Ω	28.6Ω	52.3Ω
011	43.9Ω	31.2Ω	56.3Ω
100	47.8Ω	34.2Ω	60.9Ω
101	52.4Ω	37.9Ω	66.3Ω
110	58.0Ω	42.4Ω	72.8Ω
111	64.9Ω	48.2Ω	80.5Ω

Table 6.2: Output resistor values for different bit codes

Input Matching

The input matching characteristics is shown in Figure 6.6 by plotting the S_{11} at the input port against frequency of operation.

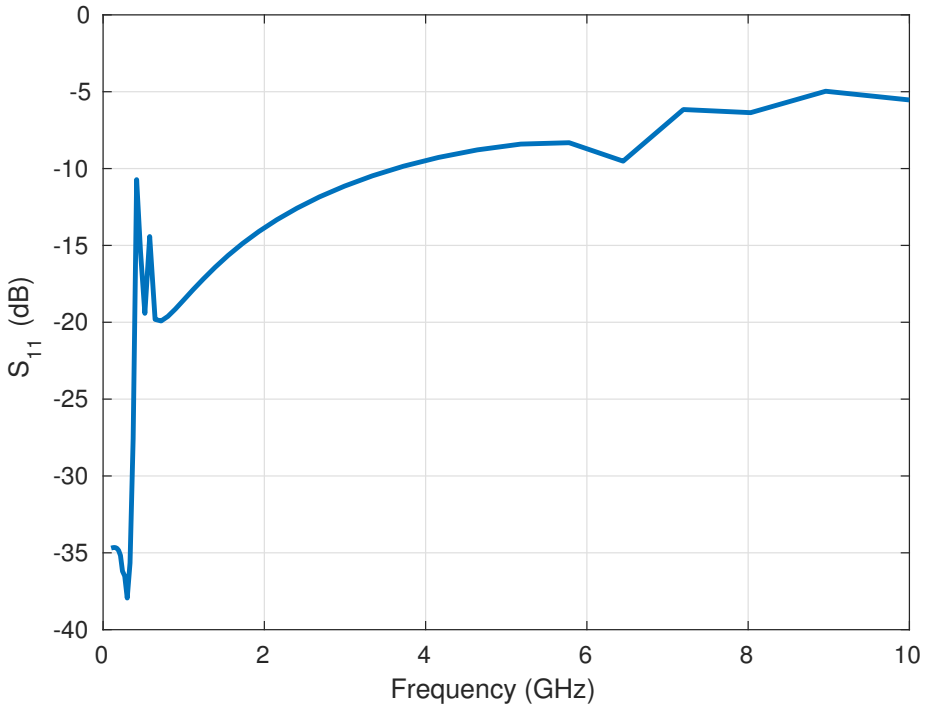

Figure 6.6: Input matching of the schematic level design

Output Matching

The output matching characteristics is shown in Figure 6.7 by plotting the S_{11} at the output port against frequency of operation.

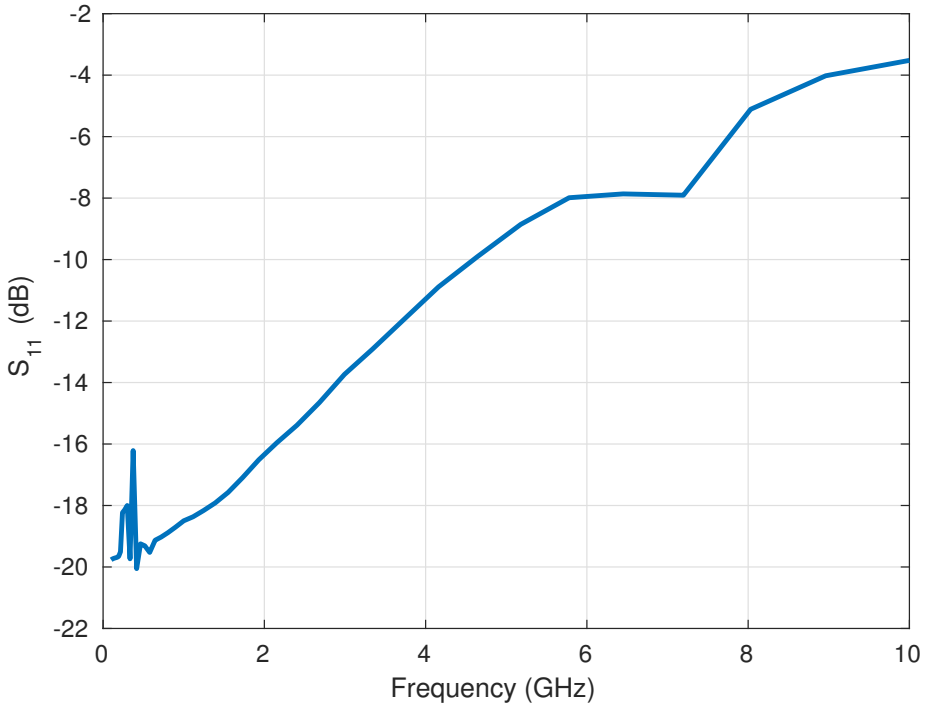

Figure 6.7: Output matching of the schematic level design

6.1.4 Calibration Loop Performance

The performance of the calibration loop was measured by observing the output voltage (which gives a measure of the delay between the rising edges of both the inputs) when a delay of 40*ps* is applied between the input and the calibration loop is set to run. The transient response of the output votlage is shown in Figure 6.8.

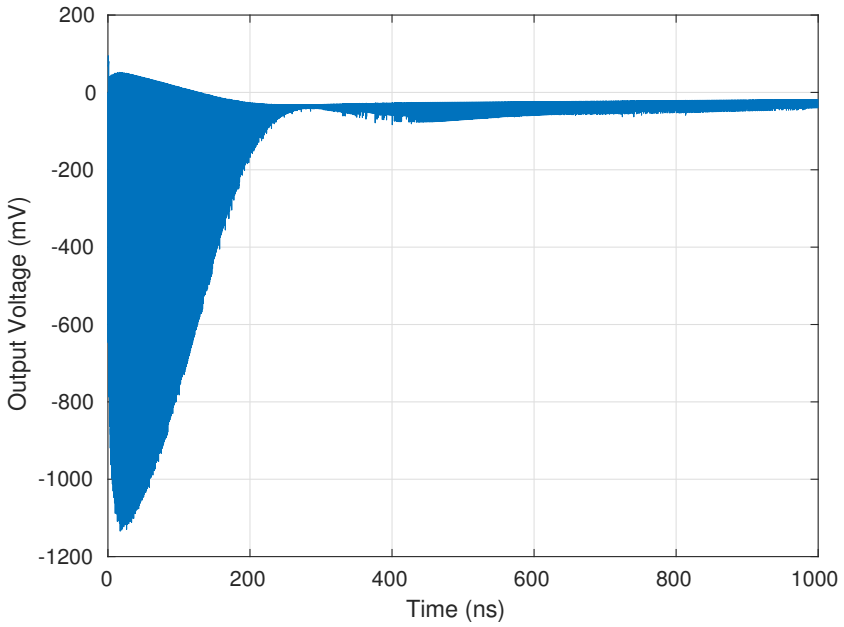

Figure 6.8: Settling behavior of the calibration loop in schematic level design

It can be observed from Figure 6.8 that the calibration loop settles within $1\mu s$.

Stability of the calibration loop

The Bode plot for the open loop gain of the calibration loop (assuming a feedback factor of 1) is shown in Figure 6.9. It was observed that the feedback factor (which depends on the circuit delay to voltage conversion characteristics and VCDL characteristics) is usually less than 1. Hence, the phase margin of the calibration loop in practice will be greater than that of the phase margin of the loop with unity gain feedback.

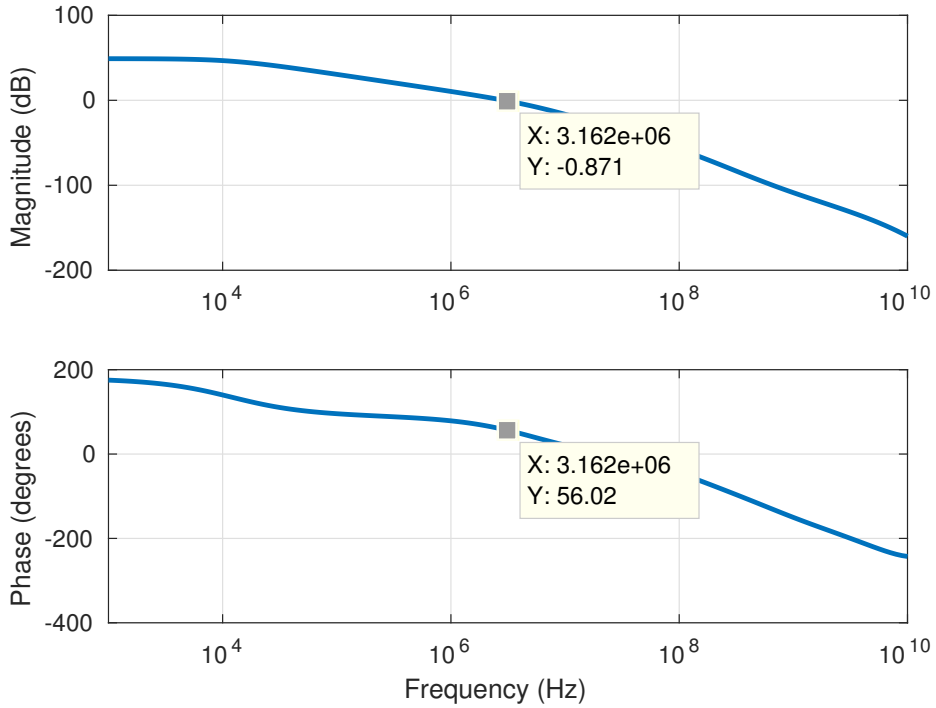

Figure 6.9: Bode plot of open loop gain of the calibration loop

The bode plot of the open loop gain of the common mode feedback in the calibration loop amplifier is shown in Figures 6.10 (for the case when the loop is on) and 6.11 (for the case when the loop is off). The change in the bode plot is due to the presence of a capacitor after the calibration loop amplifier which is not connected to the amplifier when the loop is off.

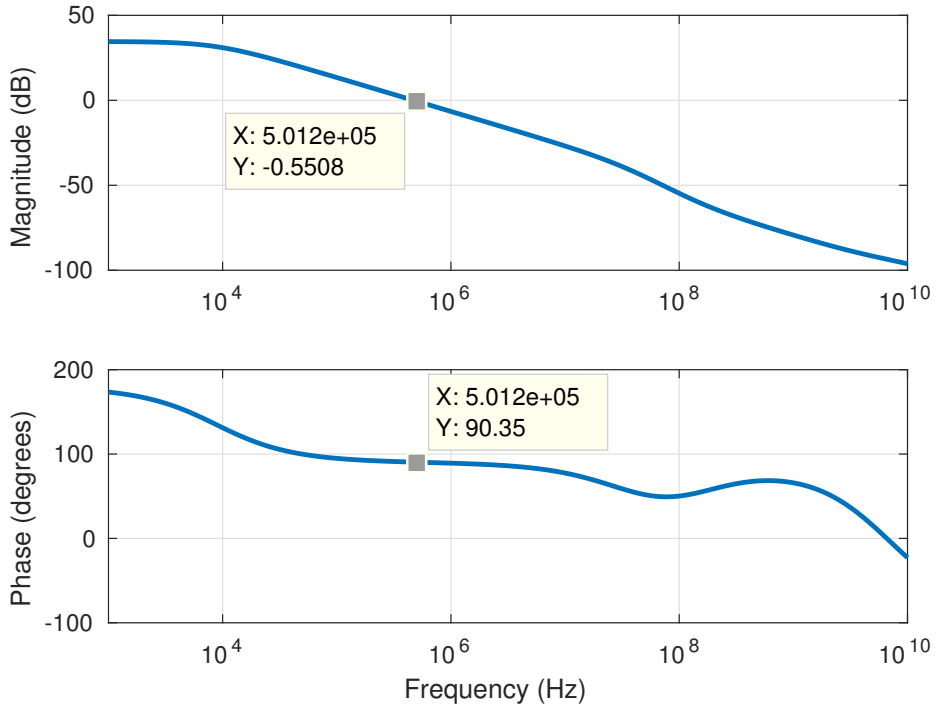

Figure 6.10: Bode plot of CMFB in calibration loop amplifier when loop is switched on

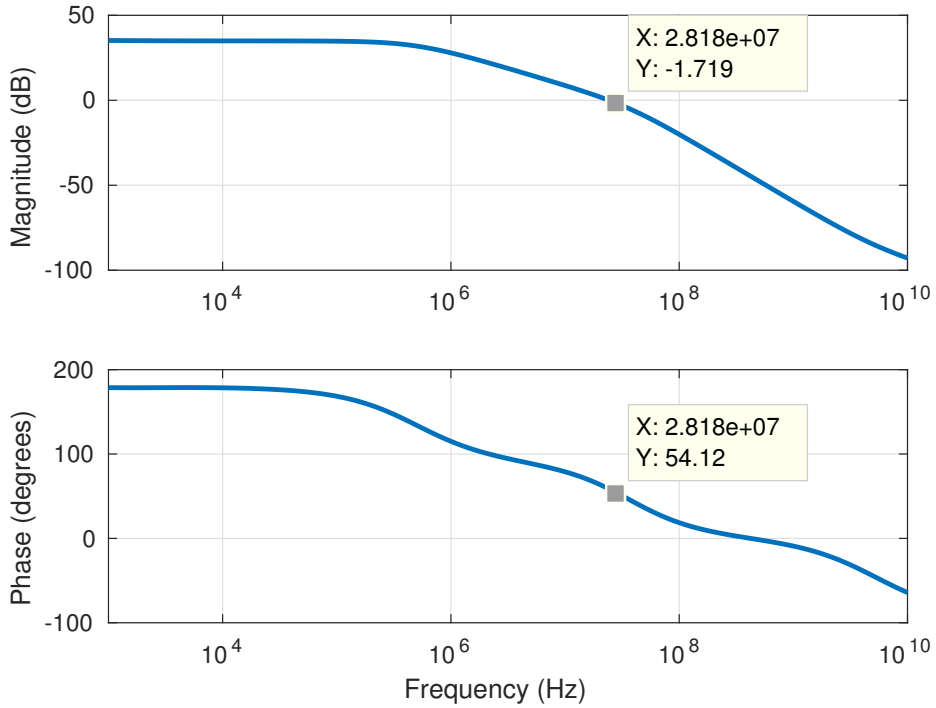

Figure 6.11: Bode plot of CMFB in calibration loop amplifier when loop is switched off

6.1.5 Power Consumption

The total power consumed by the core circuit without the buffers is 30.1mW. The distribution of the power across various blocks is shown in Figure 6.12.

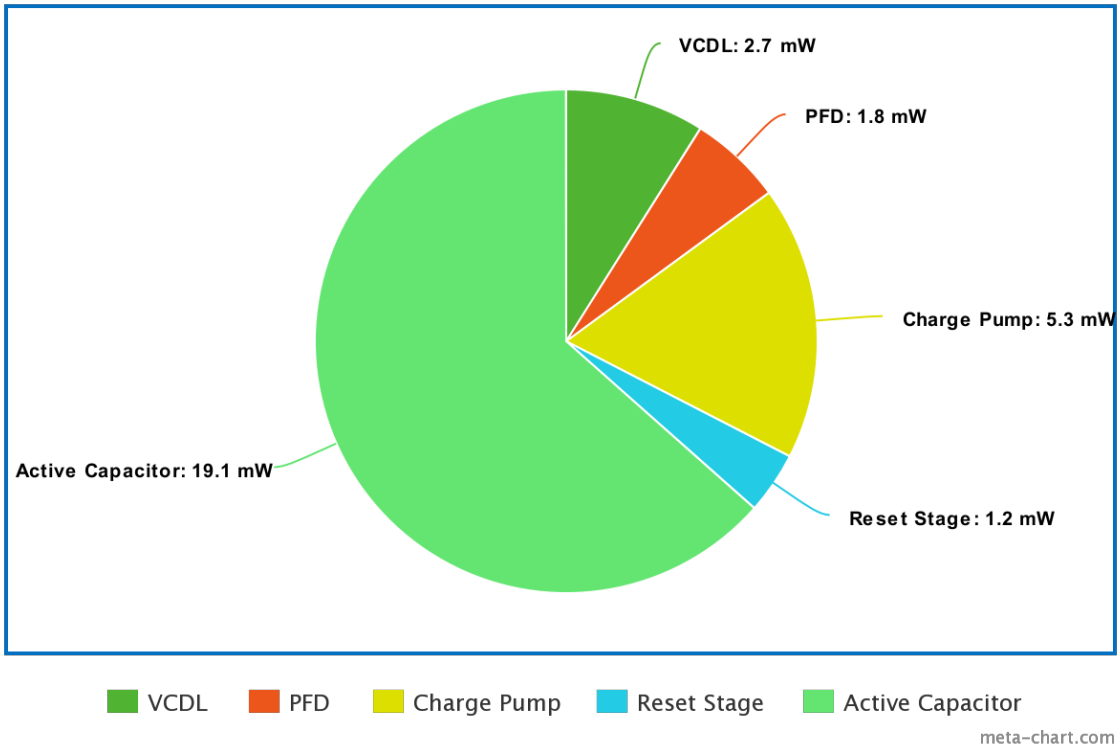

Figure 6.12: Distribution of power from the core supply

6.2 Parasitic Extracted Simulation Results

This section describes the simulation results which were obtained after the parasitic extraction of the layout.

6.2.1 Delay to Voltage Conversion Characteristics

The delay to voltage conversion characteristics of the sampler is shown in Figure 6.13. The delay in the input and the cancellation path is varied from 0ps to 70ps and

the output sampled voltage is plotted against it. Also, the ratio between the output sampled voltage and the delay (which gives a measure of the gain) is plotted on the same figure.

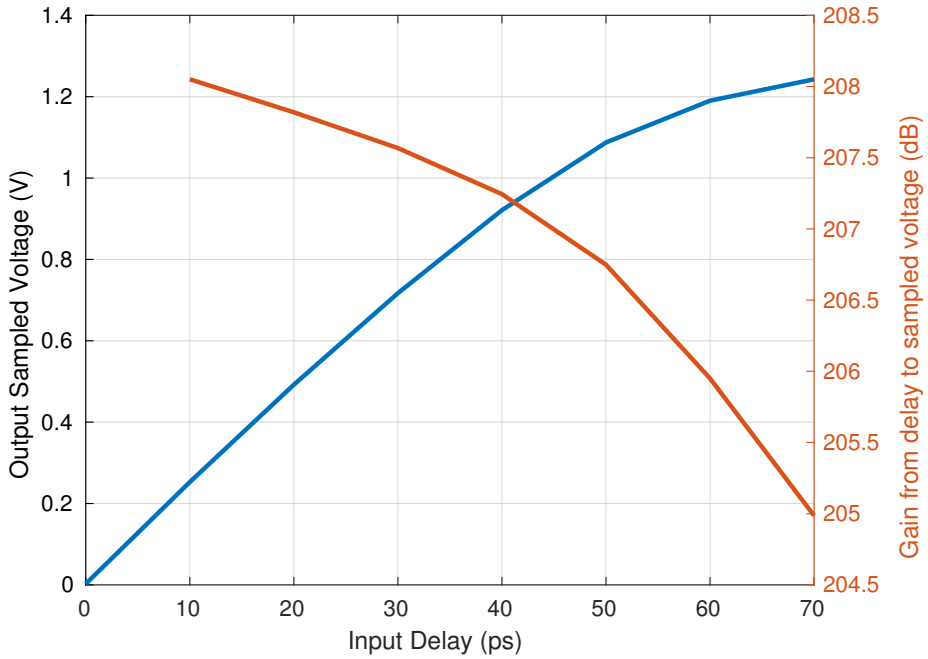

Figure 6.13: Delay to voltage conversion characteristics of the parasitic extracted cellview

6.2.2 Noise Performance

The noise performance of the sampler is shown in Figure 6.14. The delay in the input is varied from 0*ps* to 70*ps* and the output sampled noise is plotted against it.

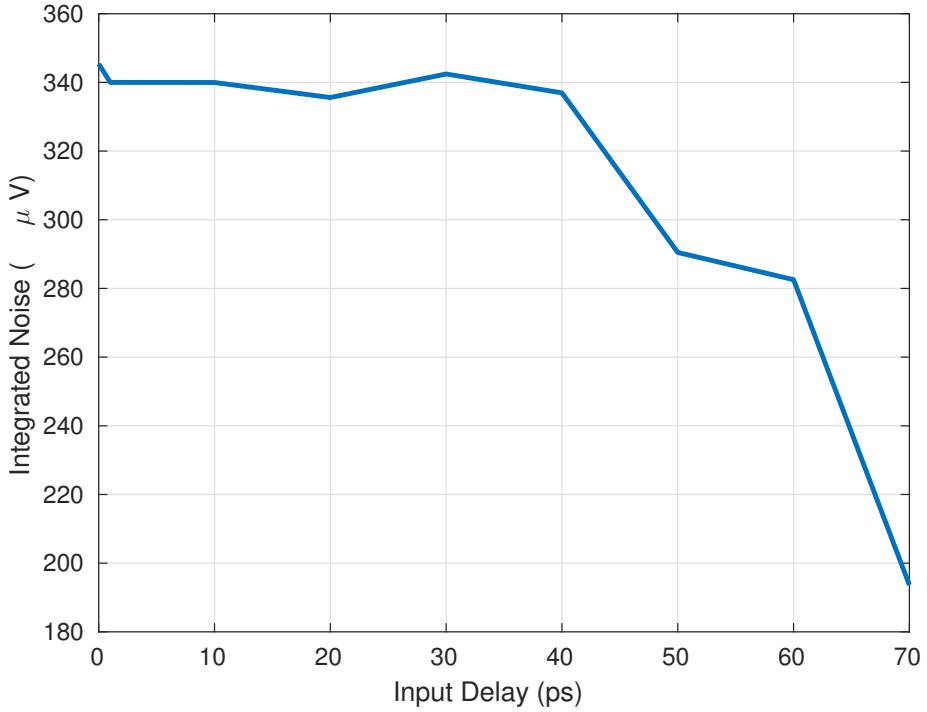

Figure 6.14: Noise performance of the parasitic extracted cellview

The input referred noise is shown in Figure 6.15.

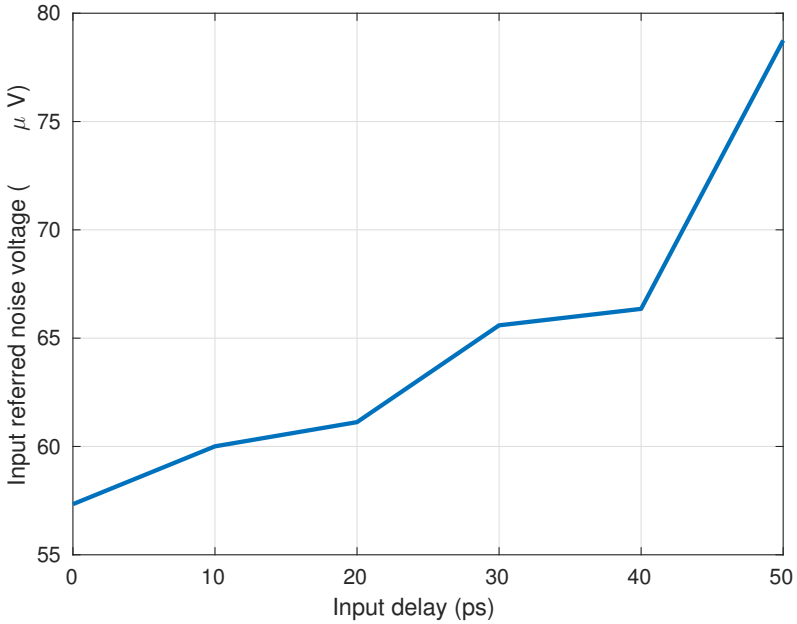

Figure 6.15: Input referred noise of the parasitic extracted cellview

6.2.3 Input and Output Matching

Input Matching

The input matching characteristics is shown in Figure 6.16 by plotting the S_{11} at the input port against frequency of operation.

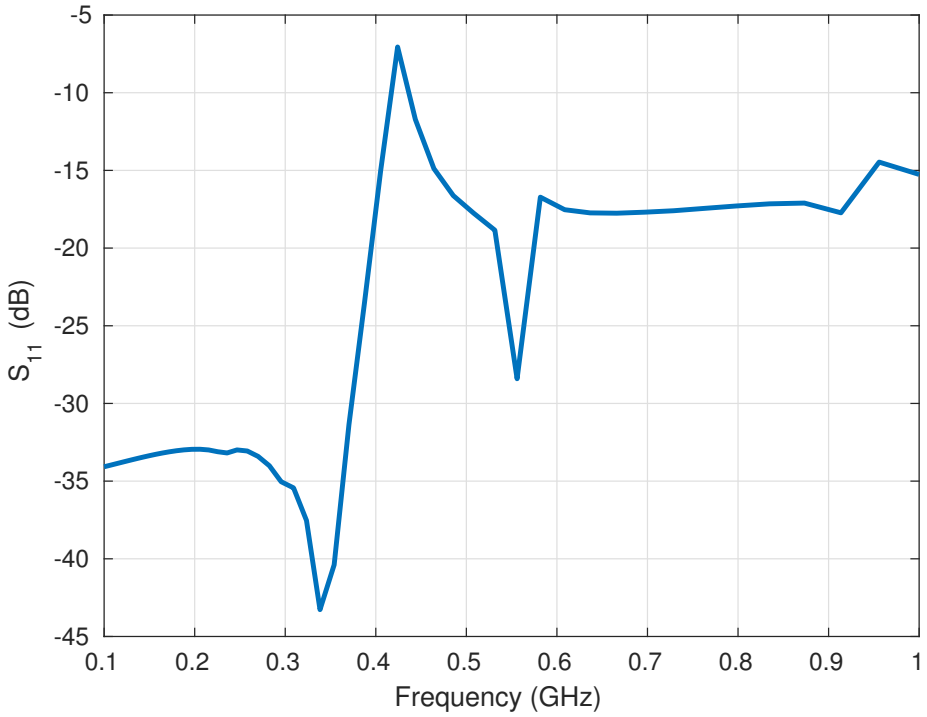

Figure 6.16: Input matching of the parasitic extracted cellview

Output Matching

The output matching characteristics is shown in Figure 6.17 by plotting the S_{11} at the output port against frequency of operation.

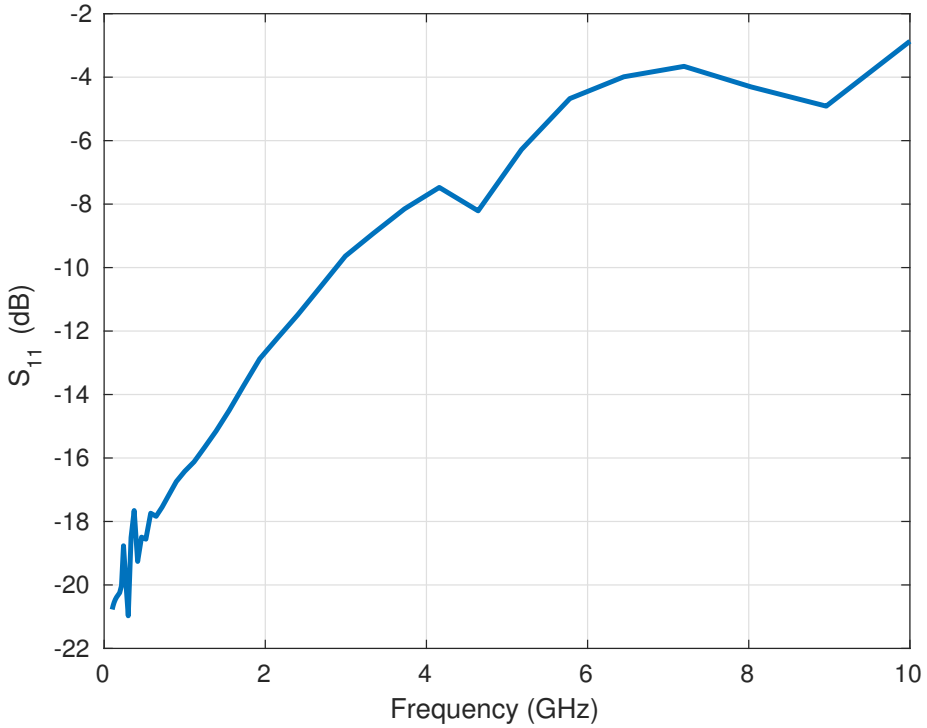

Figure 6.17: Output matching of the parasitic extracted cellview

6.2.4 Calibration Loop Performance

The performance of the calibration loop was measured by observing the output voltage (which gives a measure of the delay between the rising edges of both the inputs) when a delay of 40*ps* is applied between the input and the calibration loop is set to run. The transient response of the output votlage is shown in Figure 6.18.

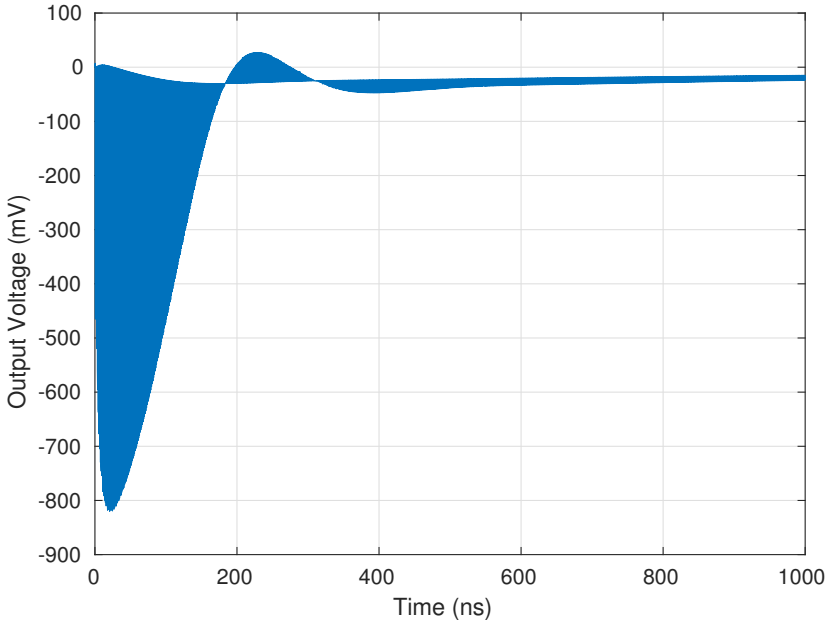

Figure 6.18: Settling behavior of the calibration loop post parasitic extraction

It can be observed from Figure 6.18 that the calibration loop settles within $1\mu s$

6.2.5 Power Consumption

The power consumption from the various supplies are shown in Figure 6.19 and blocks using the various supplies are given in Table 6.3.

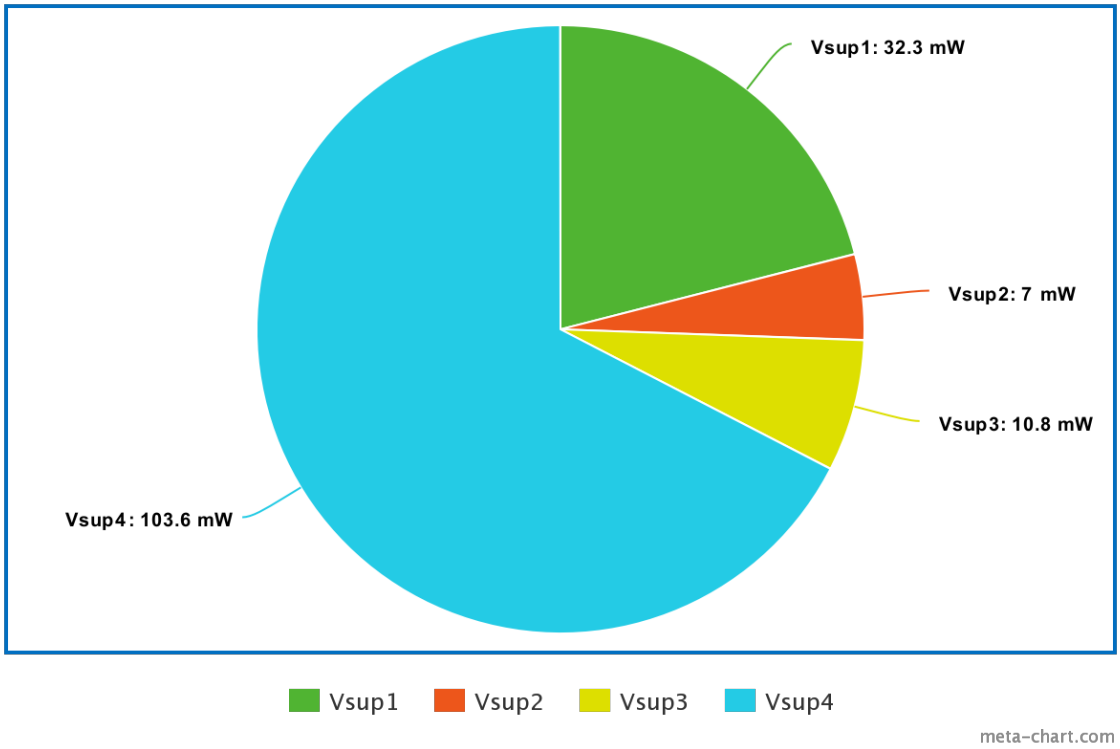

Figure 6.19: Power consumption from different supplies of the parasitic extracted cellview

Supply	Blocks using the supply
Vsup1 (1.2V)	Core circuit - VCDL, PFD, CP, Active capacitor and reset stages
Vsup2 (1.2V)	Reset buffers and bulks of PMOS switches in transmission gates
Vsup3 (2.5V)	Calibration loop and derived current sources
Vsup4 (2.5V)	Output buffer and ESD protection circuit

Table 6.3: Blocks using the power supplies

6.3 Mismatch Analysis Results

Monte-Carlo simulations were performed on the PFD to check for the variation in the delay, Charge Pump to check for the variation in the current and the calibration loop to check for the stability. This section describes the results of these simulations.

6.3.1 Mismatch in PFD

The delay mismatch in the PFD between the *UP* and $\overline{UP}$ signals, between the *UP* and *DN* signals and the variation in on time of the *UP* signal when no input delay is given is observed for 200 runs by applying both process variation and mismatch. The results are tabulated in Table 6.4.

	Minimum	Maximum	Mean	Std. Dev.
UP and *UPB*	-2.24ps	-1.54ps	-1.89ps	118fs
UP and *DN*	-430fs	332fs	667as	147fs
On time of *UP*	39.5ps	40.6ps	40.1ps	214fs

Table 6.4: Mismatches in the PFD

6.3.2 Mismatch in Charge Pump

The mismatches in the charge pump currents - UP current, DN current and the Difference - are tabulated in Table 6.5.

	Minimum	Maximum	Mean	Std. Dev.
UP Current	2.28mA	2.53mA	2.39mA	40.2μA
DN Current	2.35mA	2.54mA	2.44mA	36.1μA
Difference	-154μA	77.2μA	-56.7μA	35.9μA

Table 6.5: Mismatches in the CP

6.3.3 Mismatch in Calibration Loop Amplifier

Monte-Carlo analysis was performed on the calibration loop to determine the variation in the phase margin of the loop in unity gain feedback as well as to determine the variation in the phase margin of the CMFB loop. The results of the simulation are tabulated in Table 6.6.

	Minimum	Maximum	Mean	Std. Dev.
DC Gain	48.5dB	49.0dB	48.9dB	127mdB
Unity Gain Feedback PM	57.4°	58.8°	58.2°	320m°
CMFB PM	90.44°	90.55°	90.47°	22.91m°
CMFB PM in off state	58.2°	59.2°	58.7°	214m°

Table 6.6: Variations in the calibration loop amplifier performance with process

CHAPTER 7

Reconstruction Algorithms

The reconstruction algorithms were primarily based on [4], which tries to cancel the SI in a similar way of sampling the received signal at the zero-crossings of the SI. However, it works with the signals after I-Q down-conversion which are baseband signals. The method used by [4] is explained in Section 7.1 and the extension of the method to RF signals is explained in Section 7.2

7.1 Self-Interference Cancellation Through Advanced Sampling

Self-Interference Cancellation Through Advanced Sampling (SICTAS) receiver proposes to sample the received signal in the I-Q branches after passing through the LNA and mixer at the precise instants when the quadrature components of the self-interference from the local transmitter have zero-amplitude level. This helps in releasing the whole dynamic range of the ADC (which would have to be very large if the interference was present) for digital conversion. This method proposes to recover the desired symbols from these samples.

7.1.1 System Model

The work considers a full-duplex link with two nodes (remote and local) each emplying OFDM with $2N-1$ sub-carriers ranging from $f_{-N+1} = (-N+1)/T$ to

$f_{N-1} = (N-1)/T$ where T denotes the OFDM symbol period without the cyclic prefix portion. For a particular time period, let w_r denote the actual symbols modulating the sub-carriers in the remote transmitter, w_l denote the actual symbols modulating the sub-carriers in the local transmitter $\widetilde{w}_r$ denote the symbols multiplied by the respective sub-carrier channel response of the remote transmitter and $\widetilde{w}_l$ denote the symbols multiplied by the respective sub-carrier channel response of the local transmitter (assuming that the cyclic prefix is large enough to eliminate inter-block interference).

7.1.2 Zero-crossings of the local transmitted symbols

The complex base-band representation of the local transmitted symbols can be represented as two associated real valued signal streams, each representing a quadrature component. Let $\widetilde{x}_l(t)$ be the complex base-band representation of the received self-interference symbol. Then, the Fourier series expansion of the real part can be written as

$$\begin{aligned}\Re\{\widetilde{x}_l(t)\} &= \sum_{n=-N+1}^{N-1} \Re\{\widetilde{w}_{n,l} e^{j\frac{2\pi}{T}nt}\} \\ &= \frac{1}{2}\sum_{n=-N+1}^{N-1} (\widetilde{w}_{n,l} + \widetilde{w}^*_{-n,l}) e^{j\frac{2\pi}{T}nt} \\ &= \frac{1}{2}\sum_{n=-N+1}^{N-1} a_{n,l} e^{j\frac{2\pi}{T}nt}\end{aligned} \tag{7.1}$$

In general, the set of co-efficients $\{a_{n,l}\}$ need not produce the required number of zeroes, thus, requiring an auxiliary tone.

7.1.3 Auxiliary Tone

To ensure that the number of zero-crossings in the quadrature components of the local transmitted signal are sufficient, an auxiliary tone is added to each of the quadrature branches so as to satisfy the condition for obtaining $2N$ zero-crossings which will eventually produce $2N$ samples. This auxiliary tone can be represented as

$$\begin{aligned} s_{au}(t) &= A_{au} cos(2\pi f_{au} t) \\ &= \frac{A_{au}}{2}(e^{j\frac{2\pi}{T}Nt} + e^{-j\frac{2\pi}{T}Nt}) \end{aligned} \tag{7.2}$$

If $A_{au} > \sum_{n=-N+1}^{N-1} |\widetilde{w}_{n,l}|$, it can be shown that each quadrature component will have $2N$ zero crossings. We can obtain the values of the sampling instants from the knowledge of transmitted symbols and the self-interference channel response.

7.1.4 Non-Uniformly Sampled OFDM Reception

Let the sampling instants be denoted by $\{t_{I,i}\}$ and $\{t_{Q,i}\}$. Let $\boldsymbol{y}_I$ and $\boldsymbol{y}_Q$ denote the vectors containing the samples of the in-phase and quadrature components respectively. $\boldsymbol{y}_I$ are the samples of

$$y_I(t) = \Re\{\widetilde{x_r}(t) + \widetilde{x_l}(t)\} + z_I(t) + s_{au}(t)$$

where $z_I(t)$ denotes the real part of the noise and $\widetilde{x_l}(t)$ be the complex base-band representation of the desired symbol. We obtain

$$\boldsymbol{y}_I = \widetilde{\boldsymbol{x}}_{I,r} + \boldsymbol{z}_I \tag{7.3}$$

where $\widetilde{x}_{I,r}$ and z_I denote the samples of the in-phase (real) component of the remote signal and noise at $\{t_{I,i}\}$ since $\Re\{\widetilde{x_I}(t_{I,i})\} + s_{au}(t_{I,i}) = 0$.

$$\begin{aligned}\Re\{\widetilde{x_r}(t_{I,i})\} &= \sum_{n=-N+1}^{N-1} \Re\{\widetilde{w}_{n,r} e^{j\frac{2\pi}{T} n t_{I,i}}\} \\ &= \frac{1}{2} \sum_{n=-N+1}^{N-1} (\widetilde{w}_{n,r} + \widetilde{w}^*_{-n,r}) e^{j\frac{2\pi}{T} n t_{I,i}}\end{aligned} \tag{7.4}$$

Defining an exchange matrix $\boldsymbol{J}$ such that

$$\boldsymbol{J}_(p,q) = \begin{cases} 1, & q = 2N - p \\ 0, & q \neq 2N - p \end{cases}$$

and

$$\boldsymbol{V}_I = \begin{bmatrix} e^{-j\frac{2\pi}{T} t_{I,1}(N-1)} & \dots & e^{j\frac{2\pi}{T} t_{I,1} N} \\ \vdots & \ddots & \vdots \\ e^{-j\frac{2\pi}{T} t_{I,2N}(N-1)} & \dots & e^{j\frac{2\pi}{T} t_{I,2N} N} \end{bmatrix}$$

we obtain

$$\widetilde{\boldsymbol{x}}_{I,r} = \frac{1}{2} \boldsymbol{V}_I \left(\begin{bmatrix} \widetilde{\boldsymbol{w}}_r \\ 0 \end{bmatrix} + \begin{bmatrix} \boldsymbol{J}\widetilde{\boldsymbol{w}}^*_r \\ 0 \end{bmatrix} \right) \tag{7.5}$$

Similar equations can be written for the quadrature (imaginary) components and the subscripts of vectors and variables corresponding to the quadrature components have subscript Q (in place of I). If the sampling time instants are pairwise different, then the matrices $\boldsymbol{V}_I$ and $\boldsymbol{V}_Q$ are invertible. We can estimate the received symbols by using the Equation 7.6

$$\check{\boldsymbol{w}}_r = \boldsymbol{G}(\boldsymbol{V}_I^{-1}\boldsymbol{y}_I + j\boldsymbol{V}_Q^{-1}\boldsymbol{y}_Q) \tag{7.6}$$

where $\boldsymbol{G} = \begin{bmatrix} \boldsymbol{E} & 0 \end{bmatrix}$ where $\boldsymbol{E} = diag\begin{bmatrix} E_1 & \dots & E_{2N-1} \end{bmatrix}$ is a diagonal frequency domain equalization matrix whose element E_n compensates for the distortion induced by the remote channel to the n^{th} sub-carrier.

From the equations 7.3, 7.5, and 7.6 we obtain

$$\begin{aligned} \check{\boldsymbol{w}}_r &= \boldsymbol{E}\widetilde{\boldsymbol{w}}_r + \boldsymbol{G}\widetilde{\boldsymbol{z}} \\ &= \boldsymbol{E}\boldsymbol{H}_r\boldsymbol{w}_r + \boldsymbol{G}\widetilde{\boldsymbol{z}} \end{aligned} \tag{7.7}$$

where $\widetilde{\boldsymbol{z}} = \boldsymbol{V}_I^{-1}\widetilde{\boldsymbol{z}}_I + \boldsymbol{V}_Q^{-1}\widetilde{\boldsymbol{z}}_Q$.

From the above equation, we can conclude that with the knowledge of the channel response, the symbols $\boldsymbol{w}_r$ can be obtained.

7.1.5 Performance of the SICTAS receiver

In the presence of AWGN without fading, ideally the EVM must be equal to $\frac{1}{SNR}$ if there are no guard bands. The EVM performance of the SICTACS receiver was simulated and it was found that the $EVM = \frac{1}{SNR}$.

7.2 Reconstruction from RF samples

We would like to extend the algorithm used by the SICTAS transceiver by taking the samples of the RF signal directly without down-conversion to base-band.

7.2.1 Sampling a passband signal

In the current situation, the signal is a passband signal. One cannot always retrieve the information present in a passband signal by uniformly sampling the signal at the Nyquist rate of $2B$ where B is the bandwidth. Uniform sampling at a rate of $2B$ is possible only if the signal spectrum's lower bound is an integral multiple of the bandwidth [5]. However, the signal can be retrieved by sampling non-uniformly at an average rate of $2B$ irrespective of the position of the band by choosing an appropriate sampling set [6]. Since the number of zero-crossings of the locally transmitted RF signal in a given time frame is more than the number of samples required to satisfy the Nyquist criterion, we might be able to retrieve the information from these samples as these samples satisfy a necessary condition (i.e., average sampling rate > Nyquist rate). So, we must determine an algorithm which can use these samples to retrieve the information.

7.2.2 Signal reconstruction using Linear Least Squares (LLS)

Reconstruction based on LLS assumes the signal to be composed of a few basis functions. For a band-pass signal, the basis functions can assumed to be complex exponentials uniformly spaced in the frequency (both positive and negative) domain within the band. Let us consider a signal $x(t)$ sampled at time instants $\{t_n\}$ spaced non-uniformly in time and generated by a random process. We try to obtain an estimate of the signal, $\check{x}(t)$:

$$\check{x}(t) = \sum_{p=1}^{P} c_p e^{j2\pi f_p t} \tag{7.8}$$

where $e^{j2\pi f_p t}$ are the basis functions and c_p are the respective complex weights of the basis functions. Since the signal under consideration is real, we might as well choose the basis functions to be sine and cosine functions instead of complex exponentials and choose real weights. This will result in the estimate

$$\check{x}(t) = \sum_{m=1}^{M} a_m cos(2\pi f_m t) + b_m sin(2\pi f_m t) \tag{7.9}$$

taking the samples at time instants $\{t_n\}$, the above estimates at these time instants can be written in a matrix form:

$$\boldsymbol{x_s} = \boldsymbol{A}\boldsymbol{c} \tag{7.10}$$

where $\boldsymbol{x_s}$ is a vector of N signal samples, $\boldsymbol{A}$ is an $N \times 2M$ matrix containing the values of the basis functions (corresponding to columns) at the sampling instants (corresponding to rows) and $\boldsymbol{c}$ contains the $2M$ weights to be estimated in order to reconstruct the signal.

Linear Least Squares

The LLS algorithm provides a solution to the matrix equation such that the in-sample square-error, $\epsilon_{is}^2 = ||\boldsymbol{x_s} - \boldsymbol{A}\boldsymbol{c}||^2$ is minimized. $\boldsymbol{c}$ is estimated by the performing the operation

$$\boldsymbol{c} = (\boldsymbol{A}^\intercal \boldsymbol{A})^{-1} \boldsymbol{A}^\intercal \boldsymbol{x_s} \tag{7.11}$$

which is said to minimize ϵ_{is}^2. From the estimated value of $\boldsymbol{c}$, the signal can be

reconstructed using the corresponding basis functions from equation 7.9.

7.2.3 OFDM reception using LLS with non-uniform samples

The LLS algorithm can be used for OFDM reception by choosing the basis functions to be sine and cosine functions at the frequencies of the sub-carriers. All the samples at the zero-crossings of the locally transmitted RF signals can be considered for reconstruction. Let us consider an OFDM system with sub-carriers having the frequencies $f_c + \frac{n}{T}$ where n ranges from $-N$ to N excluding 0 and $w_{n,r} = a_{n,r} + jb_{n,r}$ be the symbols modulating the remote signal's sub-carriers. The remote signal can be represented as

$$x_{RF,r}(t) = \sum_{\substack{n=-N \\ n\neq 0}}^{N} a_{n,r} cos\Big(\frac{2\pi}{T} nt + 2\pi f_c t\Big) - b_{n,r} sin\Big(\frac{2\pi}{T} nt + 2\pi f_c t\Big) \tag{7.12}$$

Let the number of instants when the component of locally transmitted signal in the receiver is 0 be M and these instants be denoted by $\{t_m\}$ and are used for sampling the received signal. At these instances, the received signal is composed only of the component of remote signal and noise. The symbols modulating the remote signal can be estimated using the LLS algorithm discussed in section 7.2.2 and if only the sine and cosine functions at the sub-carrier frequencies are used as the basis functions, the symbols can be directly obtained from the result of the algorithm. The matrix $\boldsymbol{A}$ is of the following form:

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{A_c} & \boldsymbol{A_s} \end{bmatrix}$$

where

$$\boldsymbol{A_c} = \begin{bmatrix} cos((2\pi f_c - 2\pi\frac{N}{T})t_1) & \dots & cos((2\pi f_c + 2\pi\frac{N}{T})t_1) \\ \vdots & \ddots & \vdots \\ cos((2\pi f_c - 2\pi\frac{N}{T})t_M) & \dots & cos((2\pi f_c + 2\pi\frac{N}{T})t_M) \end{bmatrix}$$

and

$$\boldsymbol{A_s} = \begin{bmatrix} -sin((2\pi f_c - 2\pi\frac{N}{T})t_1) & \dots & -sin((2\pi f_c + 2\pi\frac{N}{T})t_1) \\ \vdots & \ddots & \vdots \\ -sin((2\pi f_c - 2\pi\frac{N}{T})t_M) & \dots & -sin((2\pi f_c + 2\pi\frac{N}{T})t_M) \end{bmatrix}$$

The vector $\boldsymbol{x_s}$ contains the values of the received signal at the sampling instances.

Performance of non-uniform OFDM reception using LLS

The EVM of the sampling process is computed using $N = 4$, $T = 4 \times 10^{-7}$, $f_c = 10^9$ and the SNR is varied from $10dB$ to $50dB$. 200 bursts were used for averaging the EVM. The noise is filtered such that it lies in the band $0.98 - 1.02GHz$. A 4-QAM modulation scheme was used in the simulations. The output EVM (EVM obtained by using zero-crossing samples and LLS) is plotted against the input EVM (EVM obtained by using I-Q sampling which is the ideal case) and shown in Figure 7.1.

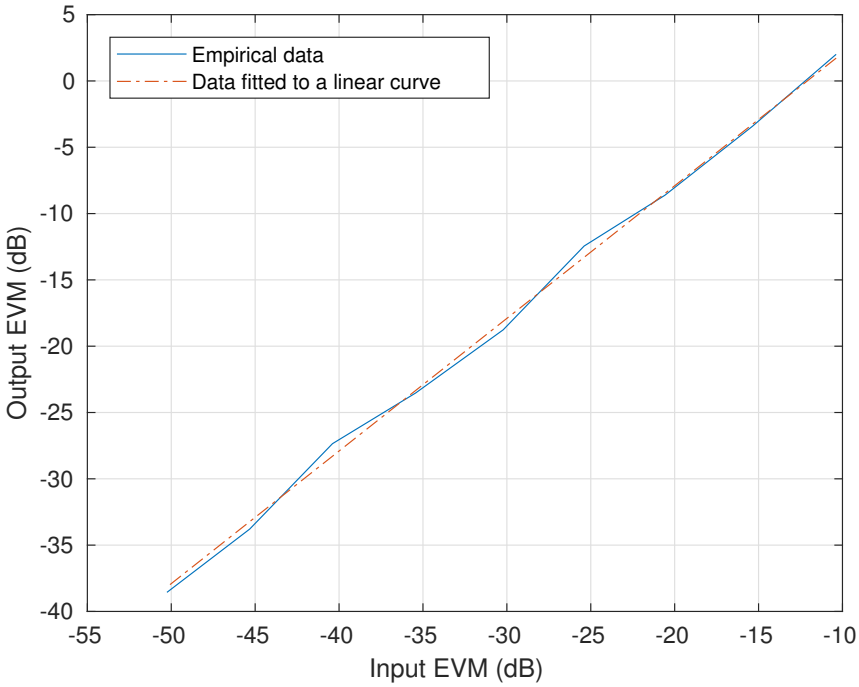

Figure 7.1: Output EVM vs Input EVM when samples at zero crossings are taken and the signal is reconstructed using LLS

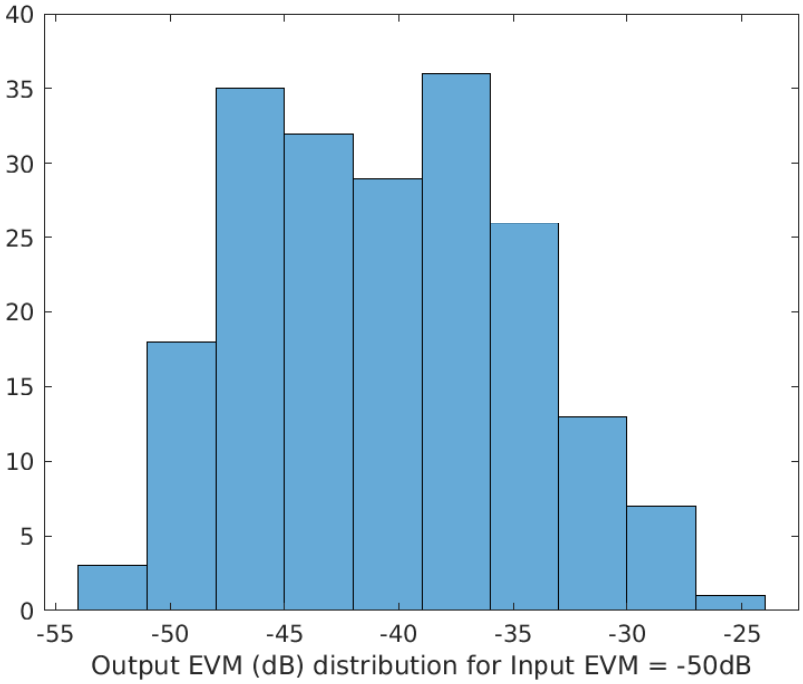

Figure 7.2: Distribution of output EVM for an SNR of $50dB$

From Figure 7.1, we can observe that the characteristics of output EVM is linear

in dB scale with respect to the input EVM. On an average, the output EVM is around $12dB$ greater than the input EVM which corresponds to a loss of $12dB$ in the link budget. Though the input EVM is almost constant for different bursts with the same SNR, the output EVM varies a lot. The distribution of the output EVM for an SNR of $50dB$ (Input EVM of $-50dB$) is shown in figure 7.2. From the distribution, we can observe that the output EVM spans a range of around $30dB$ which might be detrimental for the BER performance of the receiver.

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