Millimeter Wave RF Boards

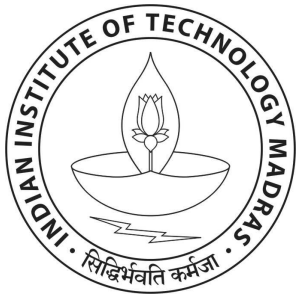
A Project Report

submitted by

M. PRASHANT

in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY



DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

JUNE 2019

THESIS CERTIFICATE

This is to certify that the thesis titled **Millimeter Wave RF Boards**, submitted by **M. PRASHANT**, to the Indian Institute of Technology, Madras, for the award of the degree of **Bachelor of Tehnology**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Date: 11th June 2019

ABSTRACT

KEYWORDS: Mmwave, Transceiver, Schematic, Layout

This thesis presents the design, development and testing of three RF boards for mmwave. The frequency of operation is 28 Ghz. This is a part of the 5G Testbed project and modifies the existing Version 0 mmwave transceiver to give Version 0.5 . The first two boards are evaluation boards to test the new upconverting mixer (ADMV1013) and downconverting mixer (ADMV1014) ICs from analog devices. The third board is the Version 0.5 mmwave transceiver, built using the above two ICs and other ICs as well. It is a single channel direct conversion transceiver that supports a bandwidth of 400 MHz.

TABLE OF CONTENTS

ABBREVIATIONS

Tx	Transmitter
Rx	Receiver
UC	Upconverter
PA	Power Amplifier
LNA	Low Noise Amplifier
Attn	Attenuator
PLL	Phase Locked Loop
IF	Intermediate frequency
LO	Local oscillator
LDO	Low dropout
CPWG	Coplanar waveguide
SDO	Serial Data Output
SDI	Serial Data Input
SCLK	Serial Clock
BPF	Bandpass filter
LPF	Low pass filter
EM	Electromagnetic
Eval	Evaluation

CHAPTER 1

INTRODUCTION

The 5G testbed project already has an existing Version 0 transceiver board for mmwave. It is a single channel superheterodyne transceiver with bandwidth 100 MHz, IF of 3.5 GHz and RF of 28 GHz. It has two passive mixers, TGC4407-SM and HMC1065LP4E which both have a frequency doubler. Hence the LO required is 12.25 GHz, which is generated by a PLL LMX2594.

The idea was to then build a single channel direct conversion transceiver using active mixers, to eliminate some components. So for this purpose, two new mixers from Analog devices were chosen. These are the ADMV1013 (Upconverter) and ADMV1014 (Downconverter). They are active mixers with gain 23dB and 17dB respectively. They support higher bandwidths (400 MHz) as compared to Version 0 mixers. Further, they have a frequency quadrupler. This is another advantage as then an LO of only 7 GHz is required. (Note : The Bandwidth of 400 MHz is 200 MHz along the In phase and 200 Mhz along the Quadrature phase. These appear as the two sidebands across the 28 GHz central frequency. Hence the LO frequency is exactly 28/4 = 7 GHz). They also have a variable attenuator so that the gain can be changed depending on the input power received or output power required.

Three boards were developed using these mixers. The first two are evaluation boards to test the ADMV1013 and ADMV1014 respectively. They are four layer boards with 6.6 mils thick dielectric Rogers4350B material. The third one is the Version 0.5 mmwave transceiver board. It is a single channel direct conversion transceiver with bandwidth (and baseband) 400 MHz, RF of 28 GHz, LO of 7 GHz. This board has six layers with the same dielectric as before. The specifics, schematic, layout and simulations of each board are dealt with in Chapter 2,3 and 4 respectively.

Simulations were done using the HFSS (High frequency structure simulator) and ADS (Advanced design system) softwares. S parameter files for the components were obtained from the corresponding manufacturers and websites. Schematic simulations were done using these in ADS, and the final components were selected based on the

results. After the layout was done, the board file was loaded into HFSS and the RF lines (waveguides) were simulated to obtain their s parameters. These s parameters in conjunction with the components s parameters were once again simulated in ADS to obtain the final EM simulation (also called co-simulation) results. The EM simulation results of each board are shown in this report.

CHAPTER 2

UPCONVERTER EVALUATION BOARD

The Upconverter Evaluation board was built to test the ADMV1013 upconverter in conjunction with the power amplifier HMC863A. The PA requires a bias controller HMC980 which is also present. It has U.FL connectors for the baseband inputs, SMAs for the LO inputs and 2.92mm edge connectors for the 28 GHz output. It has provisions to attach a heat sink although this is not currently used. The board has two supply voltages: 6V and 5V. It uses CPWGs for the 28 GHz and 7 GHz (LO) lines and microstrips for the baseband inputs.

The Upconverter requires two supplies, 3.3V for the analog and RF pins and 1.8V for the digital pins. The IC has digital reset and SPI pins. There are various sub modules present inside the IC like the envelope detector, LO Quad circuit, Transmitter Bandgap etc. It has various registers that control these sub modules and the registers can be set via the SPI pins. The IC can perform conversion to an IF as well as direct conversion to baseband. In the present case, only direct conversion is used and the IF pins are NC (not connected). It has four baseband pins - differential Inphase and differential Quadrature. The LO is also differential.

The board consists of four modules:

1. Standalone Upconverter Evaluation module
2. Standalone Power Amplifier Evaluation module
3. Upconverter + Power Amplifier module
4. 14dB resistor attenuator

Let us look at these modules individually.

2.1 Standalone UC eval module

This module is comprised of just the Upconverter and its associated elements like bypass capacitors, bias resistors etc. It was made to test the upconverter functionality. The

four microstrip lines for the baseband inputs are length matched. The two CPWGs for the LO inputs are also length matched. This module has its own 3.3V supply, which is different from 3.3V supply for the UC+PA module.They however share a common 1.8V supply. These supplies are generated by LDOs TLV75733 and TLV75718 respectively which take in 5V as input. There is a pi matching network at the ADMV output, however only two elements have been used. The block diagram for this module is shown below.

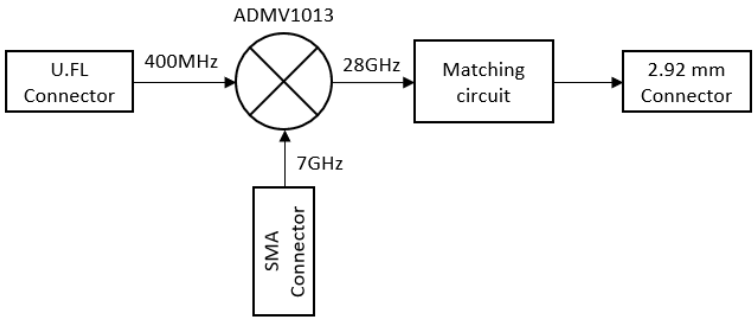

Figure 2.1: Block diagram of Standalone Upconverter Eval module

The EM Simulation setup and results for this module are shown in Fig. 2.2, Fig. 2.3 and Fig. 2.4 .

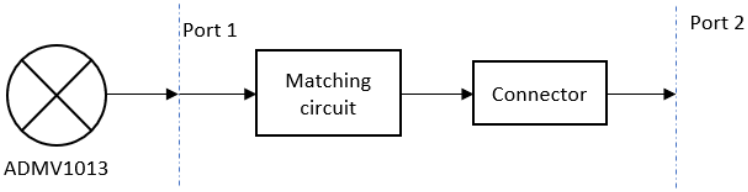

Figure 2.2

2.2 Standalone PA eval module

This module is comprised of the power amplifier, the bias controller and their associated elements. It was made to test the power amplifier functionality. The bias controller requires 6V as supply. The PA itself does not require any supply. It gets gate voltage and drain voltage from the bias controller. The power amplifier gives 24dB gain at 28GHz. There are two CPWGs connected to its input and output. The block diagram for this module is shown in Fig. 2.5.

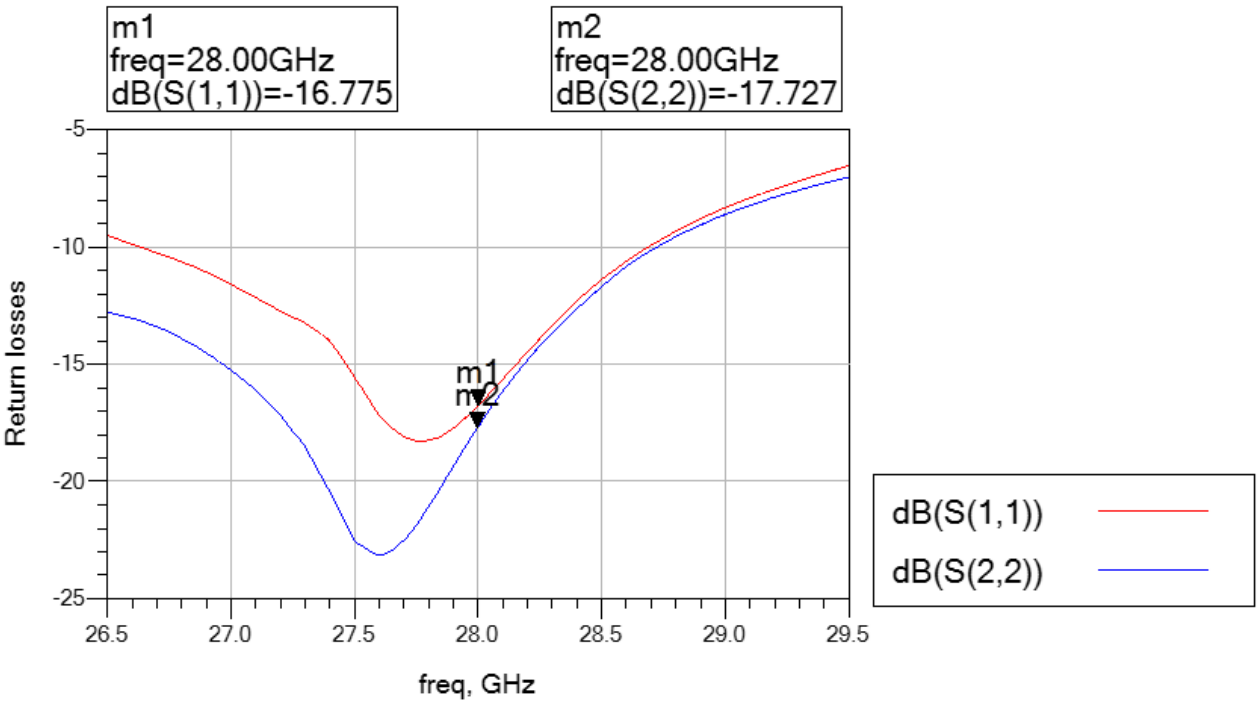

Figure 2.3

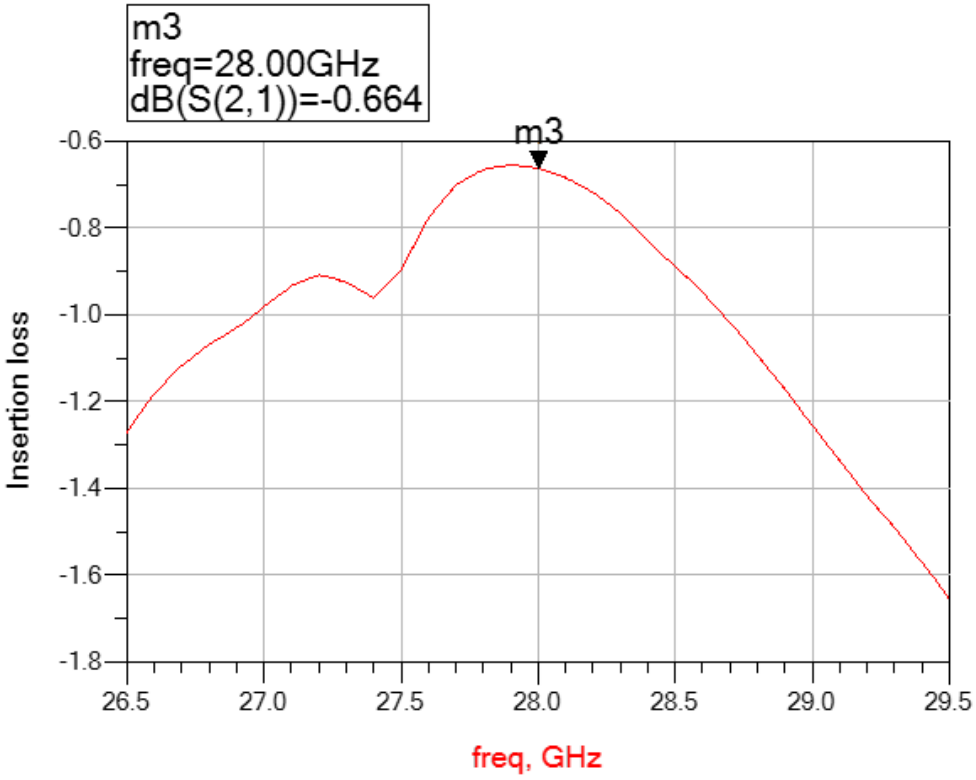

Figure 2.4

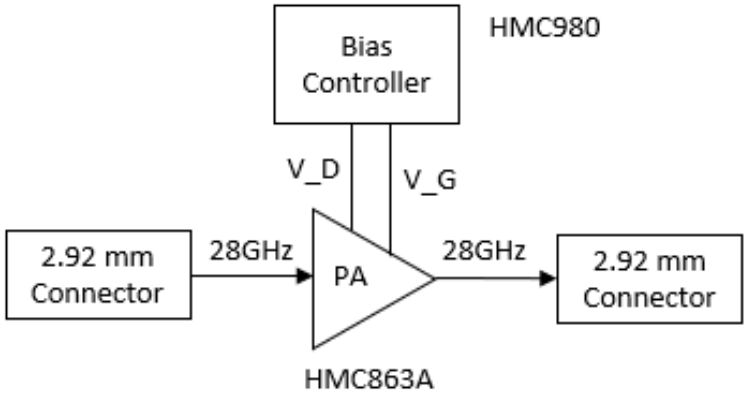

Figure 2.5: Block diagram of Standalone PA Eval module

2.3 UC+PA module

This is the most important part of the board. It comprises of the upconverter, power amplifier, bias controller and their associated elements. It is used to test the cascade of the upconverter and power amplifier. There is a pi matching network between the upconverter and PA, of which only two elements have been used. Similar to the standalone UC eval module, the microstrips and LO CPWGs are length matched. As mentioned before, this module and the standalone module have separate 3.3V power supplies and a common 1.8V supply. This is because both the upconverter ICs together draw 1.1A of current at 3.3V and 6mA at 1.8V, whereas the TLV757 series LDOs can provide a maximum of 1A current only. The block diagram for this module is shown below.

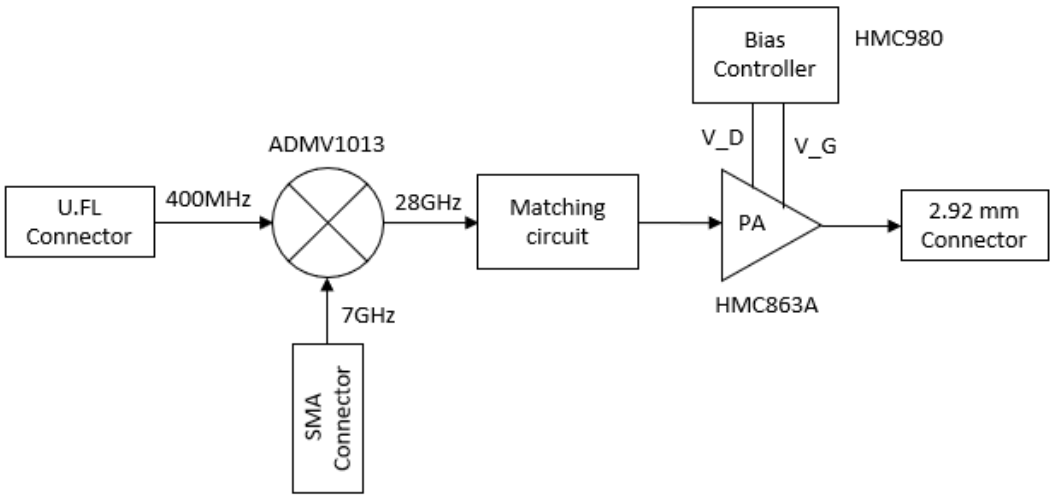

Figure 2.6: Block diagram of UC+PA module

The EM Simulation setup and results for this module are shown in Fig. 2.7, Fig. 2.8

and Fig. 2.9 . It should be noted that in Fig. 2.9, the expected (or ideal) gain is 24 dB i.e. the gain of the PA. Instead we get 22.5 dB which is quite close.

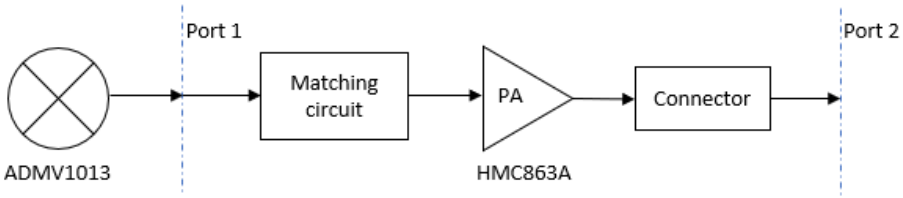

Figure 2.7

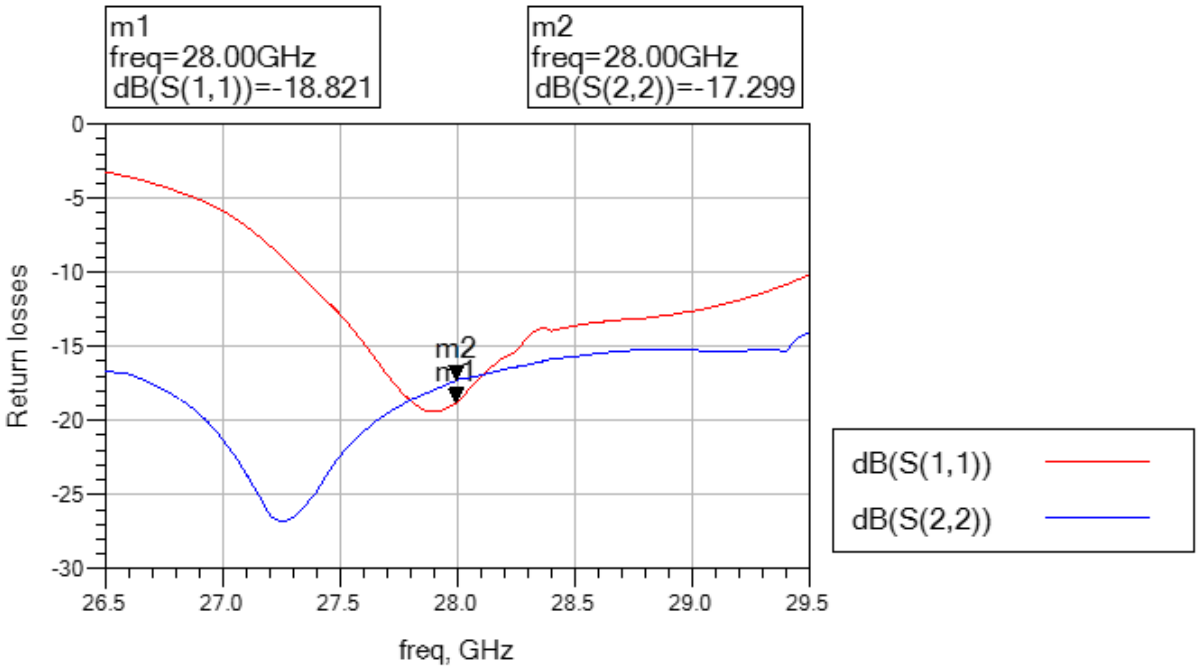

Figure 2.8

2.4 14dB Resistor Attenuator

As the name suggests, this is a 14dB differential attenuator built using only resistors. It was required in the phased array board of the testbed, and so it was added to this board to test its functionality. The circuit diagram is given in Fig. 2.10 .

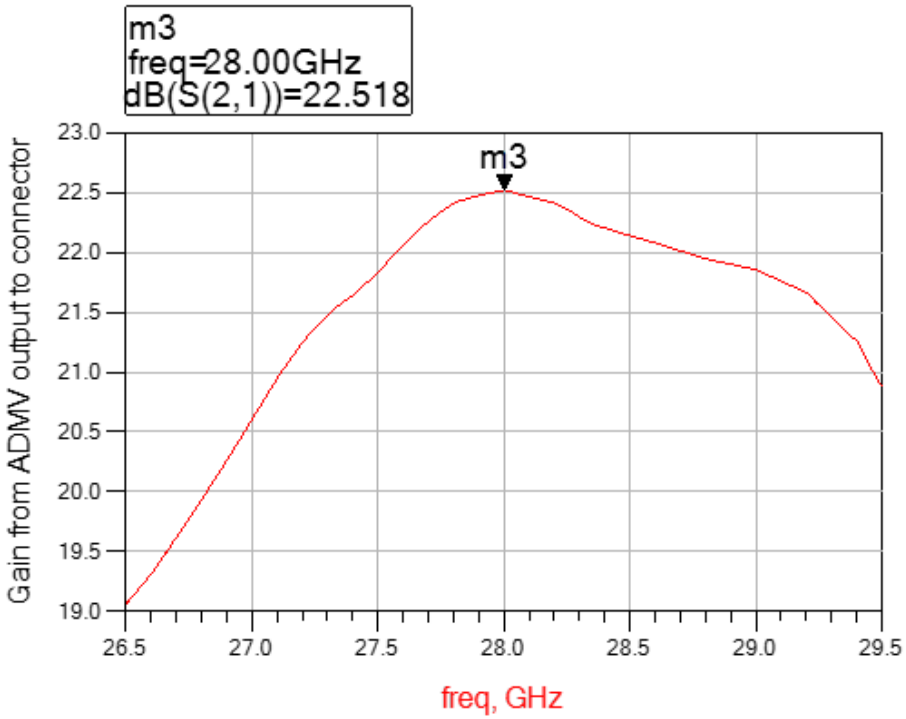

Figure 2.9

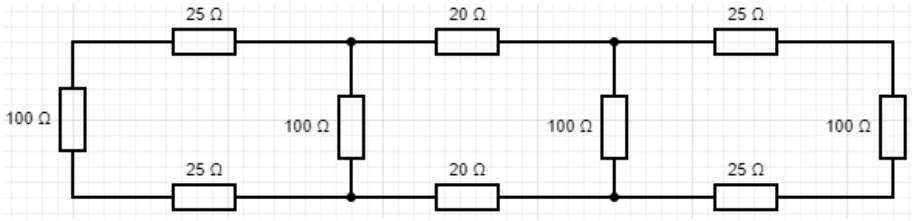

Figure 2.10: Circuit diagram of 14dB resistor attenuator

The layout of the entire Upconverter Evaluation Board is shown in Fig. 2.11 .

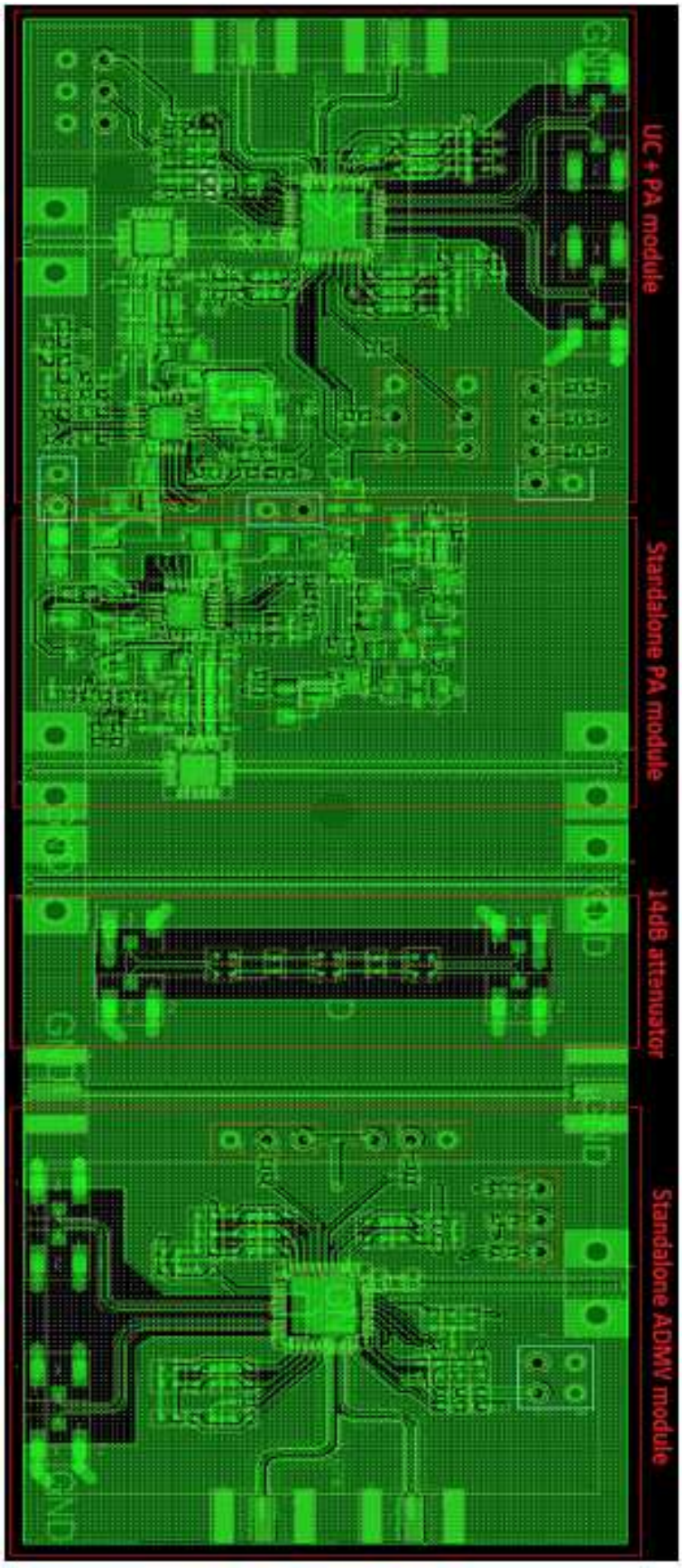

Figure 2.11: Layout of Upconverter Evaluation board

CHAPTER 3

DOWNCONVERTER EVALUATION BOARD

The Downconverter Evaluation board was built to test the cascade of the ADMV1014 downconverter and the LNA HMC1040LP3CE. A digital attenuator ADRF5730 has been added between the ADMV and LNA to maximize the dynamic range of the input. Earlier the P1dB of the mixer is the limiting factor (corresponds to maximum input power of -32 dBm) whereas now the limiting factor is the P1dB of the LNA (corresponds to maximum input power of -11dBm). Hence we get an extra 21dBm input power range. Many of the other details are similar to the upconverter IC (and eval board). It has SMAs, U.FL connectors, 2.92mm edge connectors, CPWGs and microstrips. The mixer IC has SPI pins through which internal registers can be controlled. There is a pi matching network between the mixer and the digital attenuator, of which only two elements have been used.

The mixer has a gain of 17dB while the LNA has a gain of 23 dB. The board has two supplies of 5V and -3.3V. The mixer IC requires 3.3V for the analog and RF pins, 1.8V for the digital pins and 1.5V for the internal lna. The attenuator requires -3.3V and 3.3V while the LNA IC requires 2.5V. All these voltages are generated using TLV757 series regulators. The ADRF5730 has an attenuation range of upto 31.5dB in 0.5dB steps with an insertion loss of 2dB. It has SPI pins to control the attenuation. The block diagram and layout of the board are shown below.

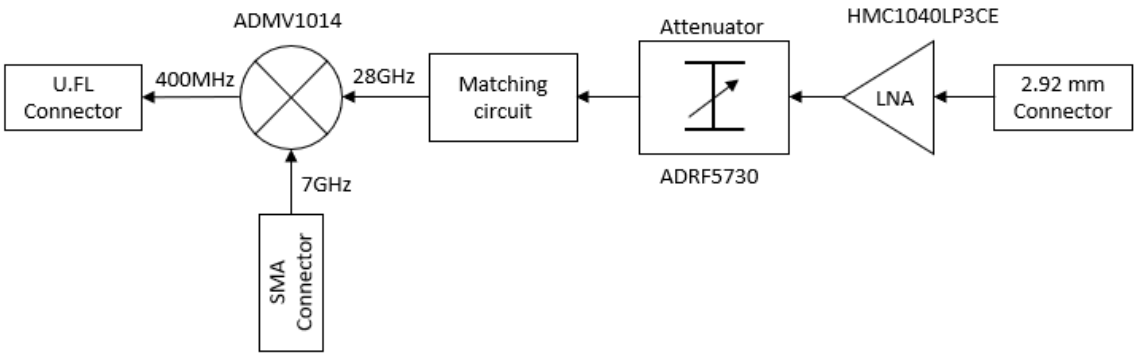

Figure 3.1: Block Diagram of Downconverter Evaluation board

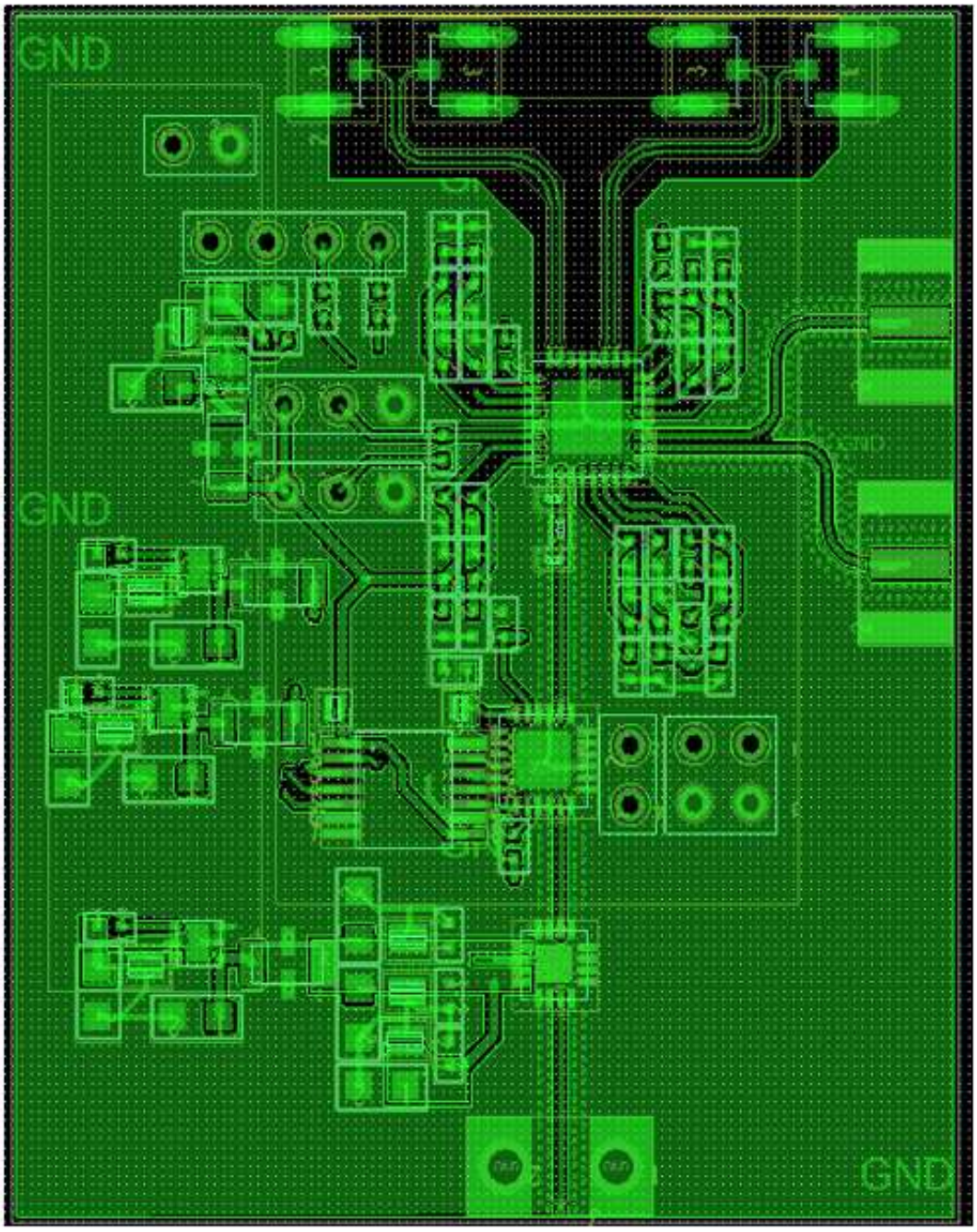

Figure 3.2: Layout of Downconverter Evaluation board

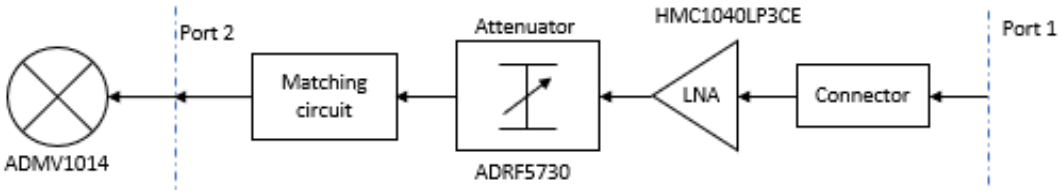

Figure 3.3

The EM Simulation setup and results are shown in Fig. 3.3, Fig. 3.4 and Fig. 3.5 . The expected gain in Fig. 3.5 is (lna gain - attenuator insertion loss) = 23 - 2 = 21dB.

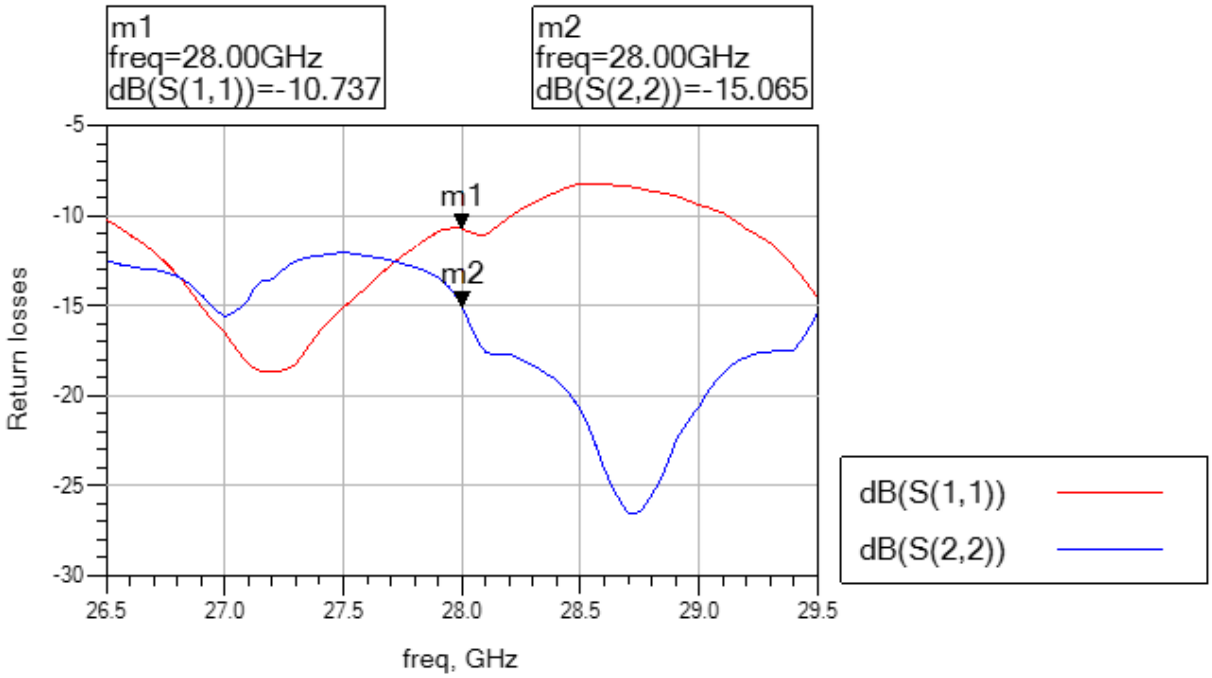

Figure 3.4

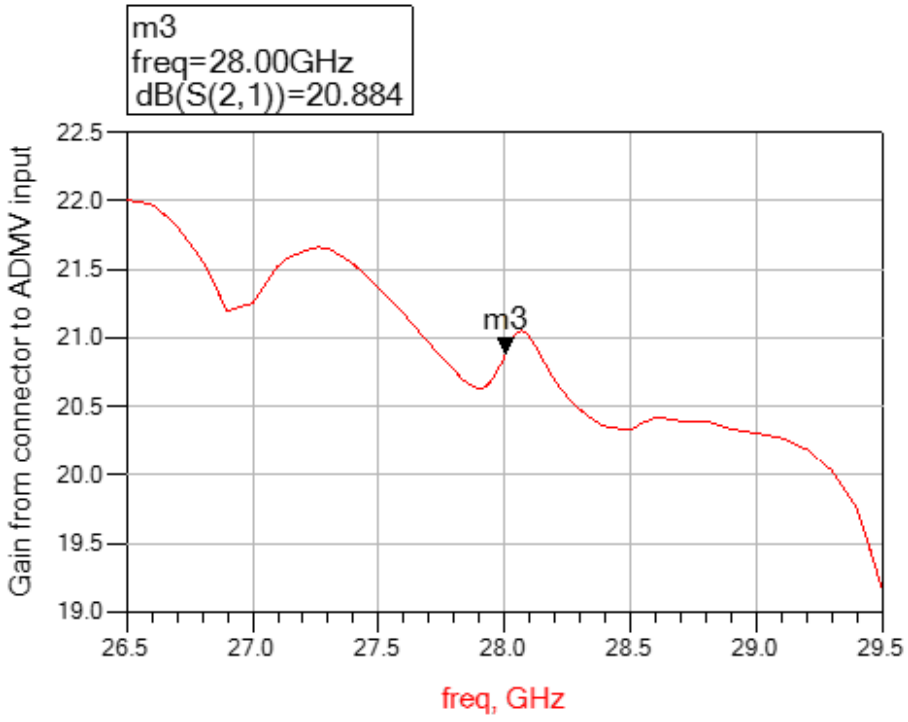

Figure 3.5

CHAPTER 4

VERSION 0.5 TRANSCEIVER BOARD

This is a transceiver board built using the ADMV1013 and ADMV1014 mixers. It is a six layer board with dimensions 10cm x 5cm. It has a PLL (LMX2594) that generates 7 GHz LO for the mixers. It is a single channel direct conversion transceiver. The block diagram is given below.

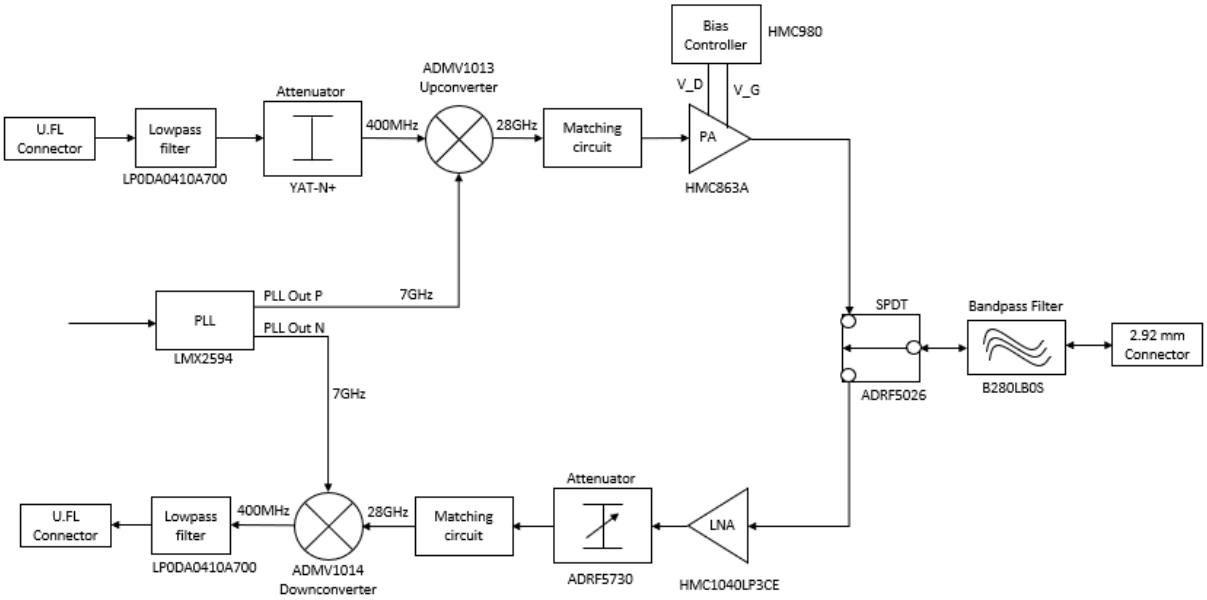

Figure 4.1: Block Diagram of transceiver board

There are a few changes as compared to the Version 0 board. There is only one PA (Version 0 had two in cascade) as the active mixer itself gives 23 dB gain. The switch has been changed to ADRF5026, as the previous one ADRF5020 was quite lossy and also required an LDO, as its operating voltage was 5.5V . ADRF5026 operates at 3.3V . As mentioned earlier, the digital attenuator ADRF5730 was added to increase the input dynamic range. A fixed attenuator (of Yat-N+ series) is added after the LPF to ensure that the input P1dB of the mixer is not crossed. The mixers have differential LO inputs but one of the inputs has been terminated with 50 ohms, thereby making it single ended. The layout of the board is given below.

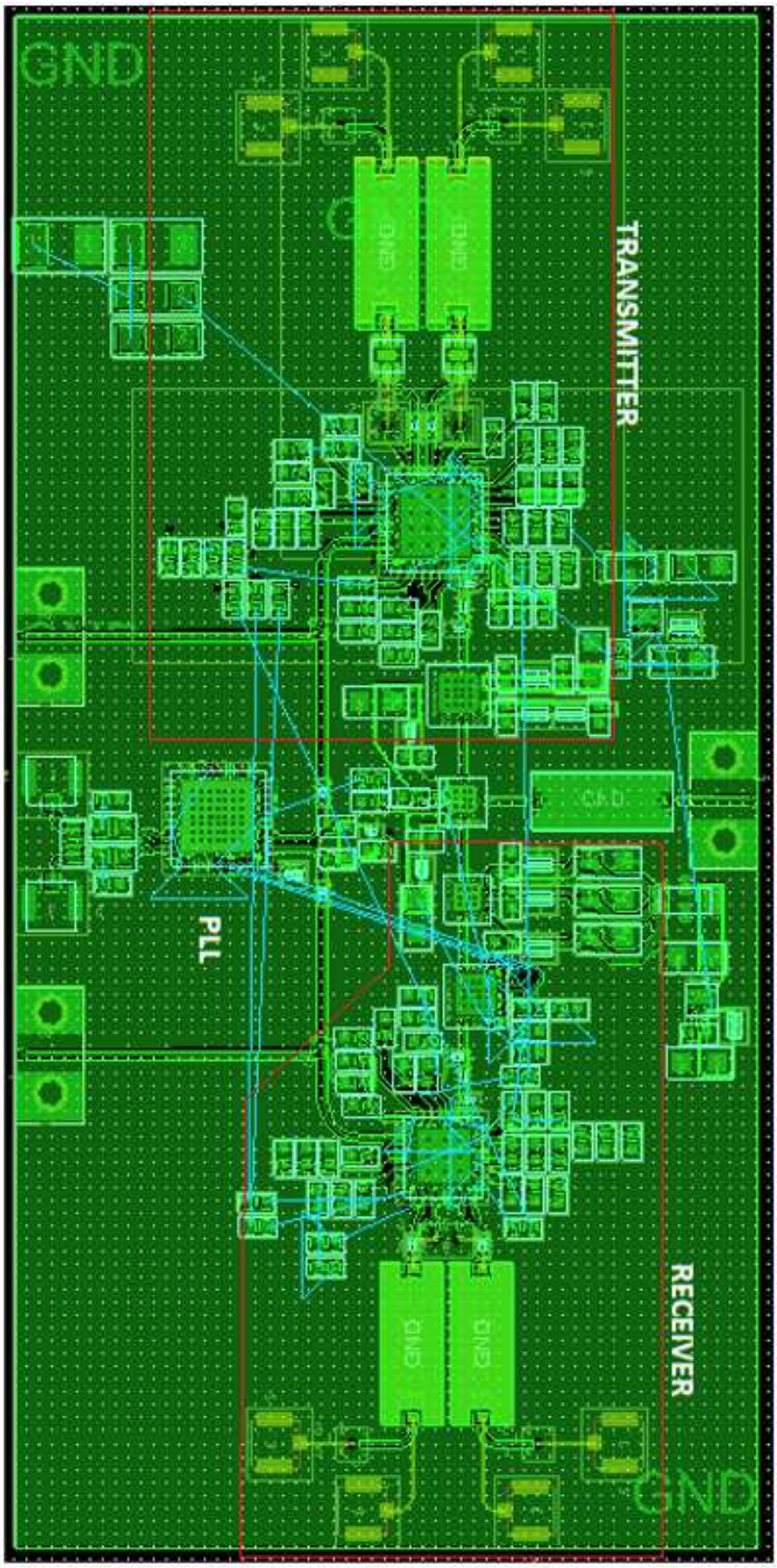

Figure 4.2: Layout of transceiver board

The EM Simulation setup and results for the 28GHz Tx are shown in Fig. 4.3, Fig. 4.4 and Fig. 4.5 . The expected gain in Fig. 4.5 is 20 dB. The total transmitter gain is 18.2 + 23 = 41.2 dB

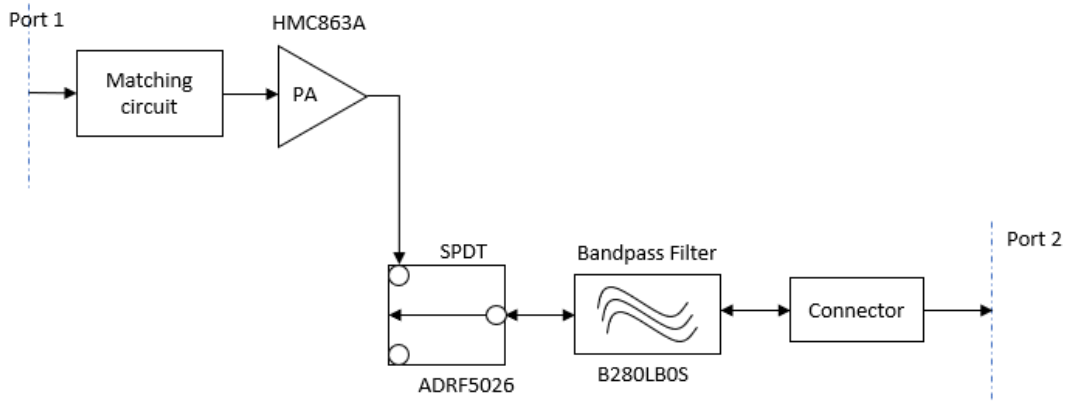

Figure 4.3

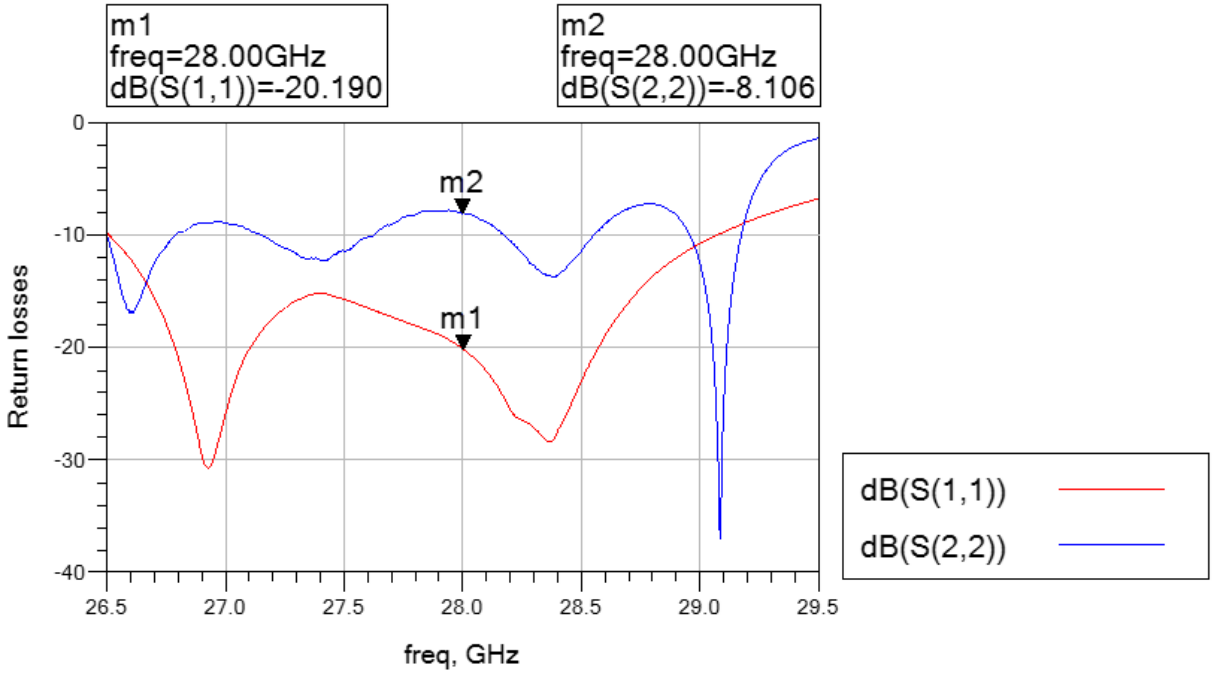

Figure 4.4

The EM Simulation setup and results for the 28GHz Rx are shown in Fig. 4.6, Fig. 4.7 and Fig. 4.8 . The expected gain in Fig. 4.8 is 19 dB. The total receiver gain is 17 + 17 = 34 dB

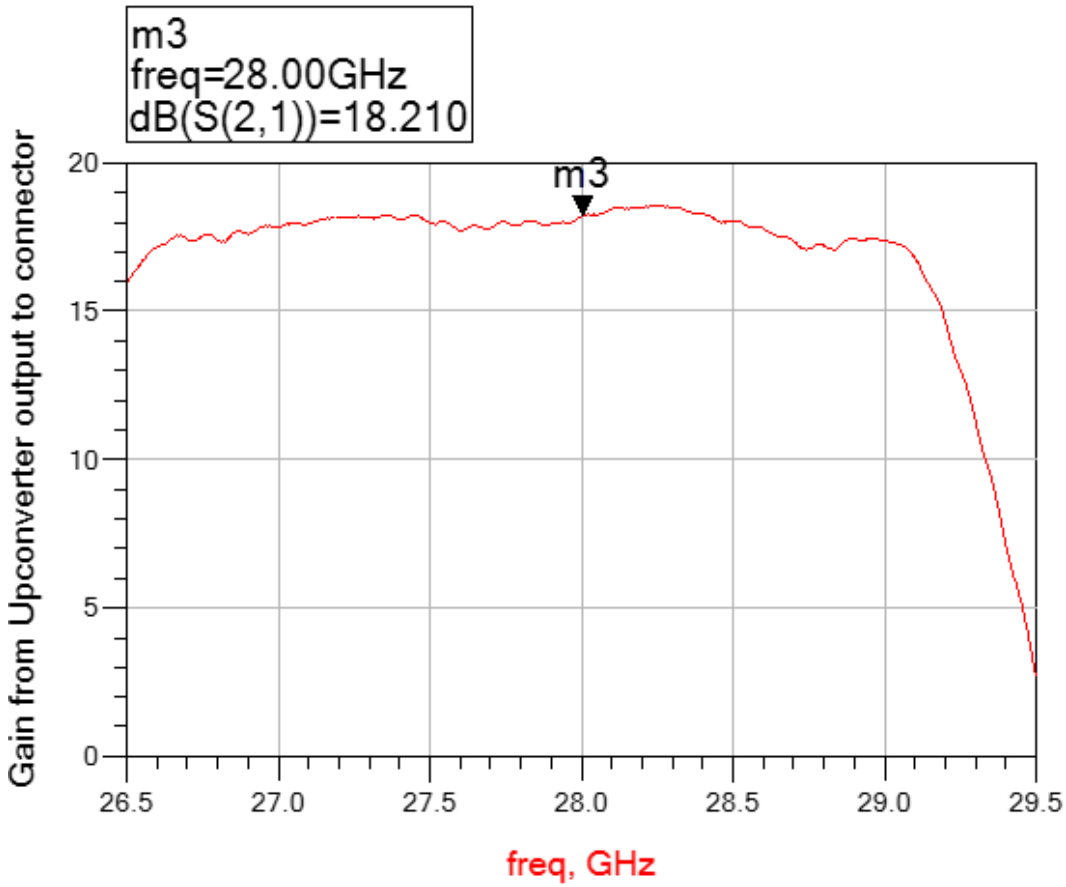

Figure 4.5

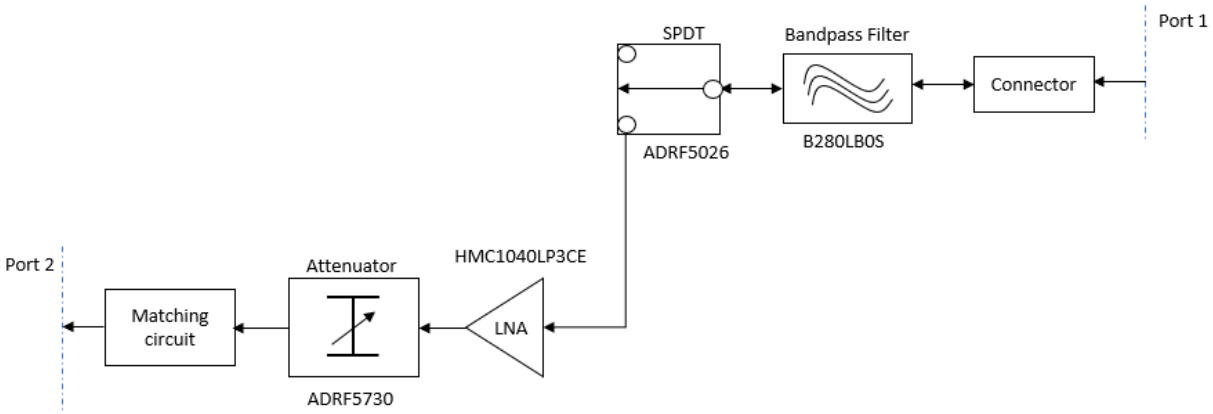

Figure 4.6

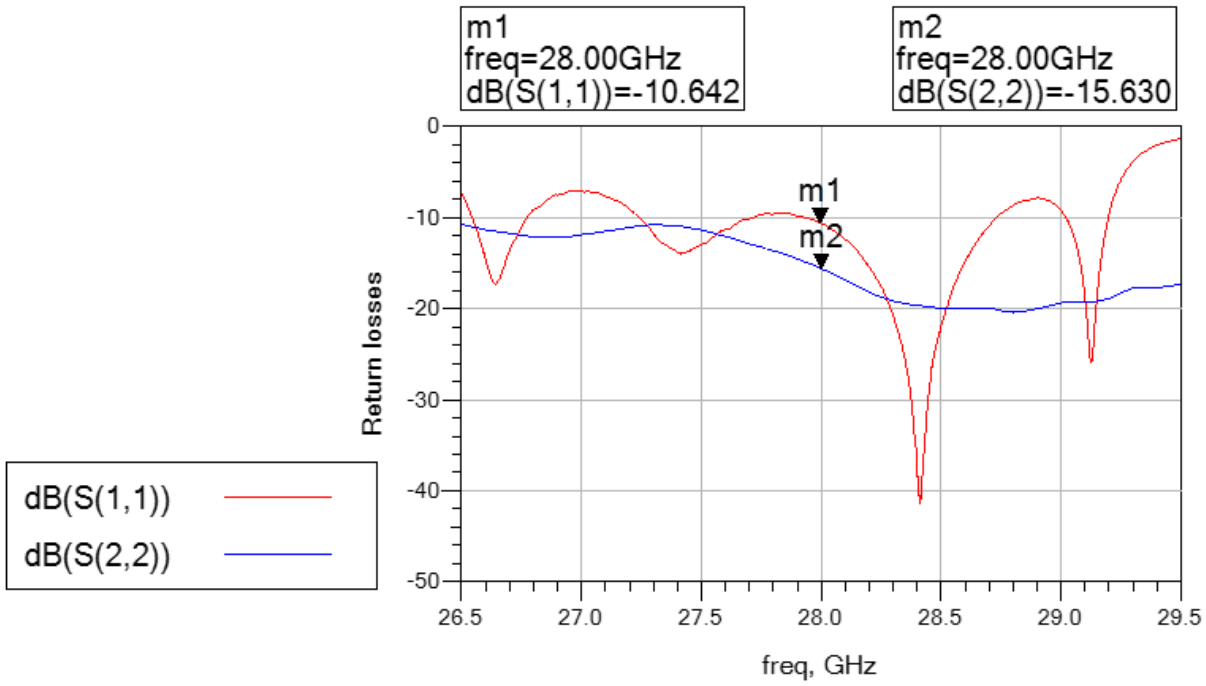

Figure 4.7

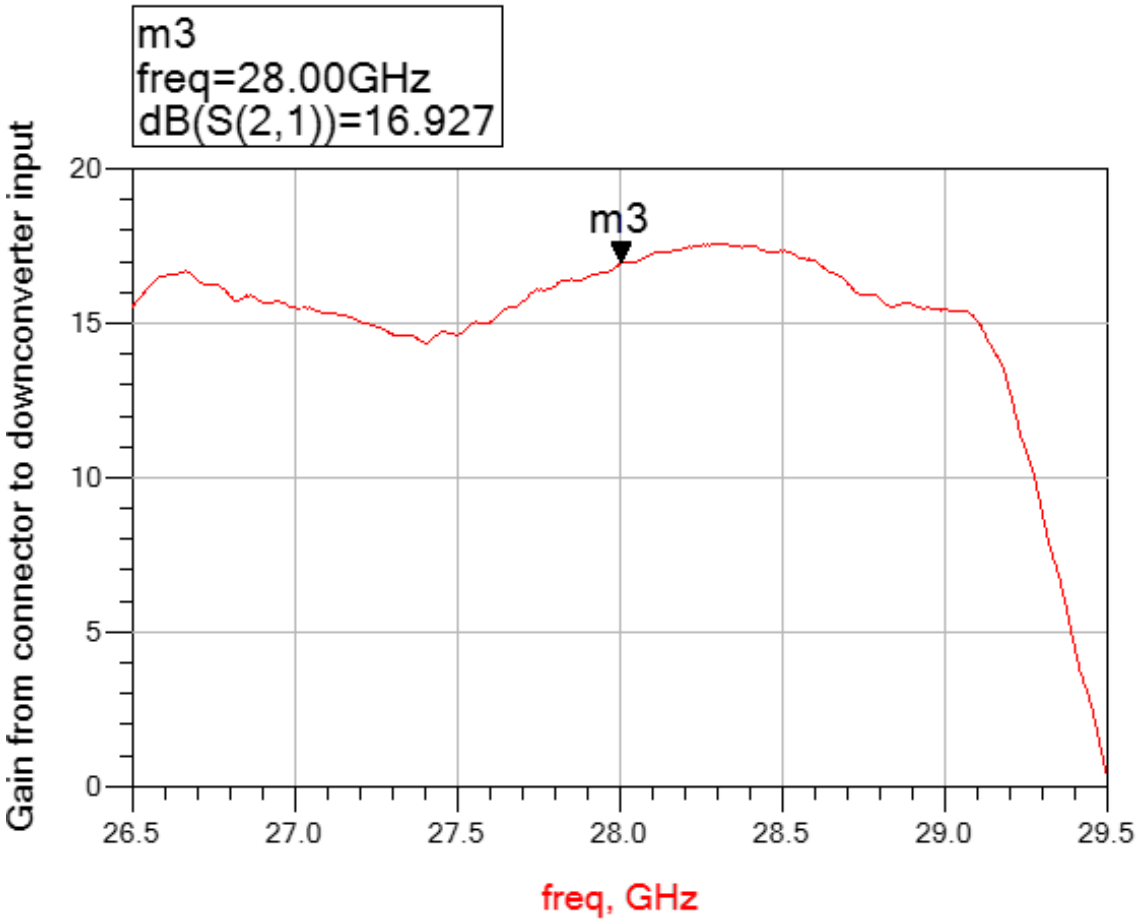

Figure 4.8

The EM Simulation setup and results for the 7GHz LOp are shown in Fig. 4.9 and Fig. 4.10 .

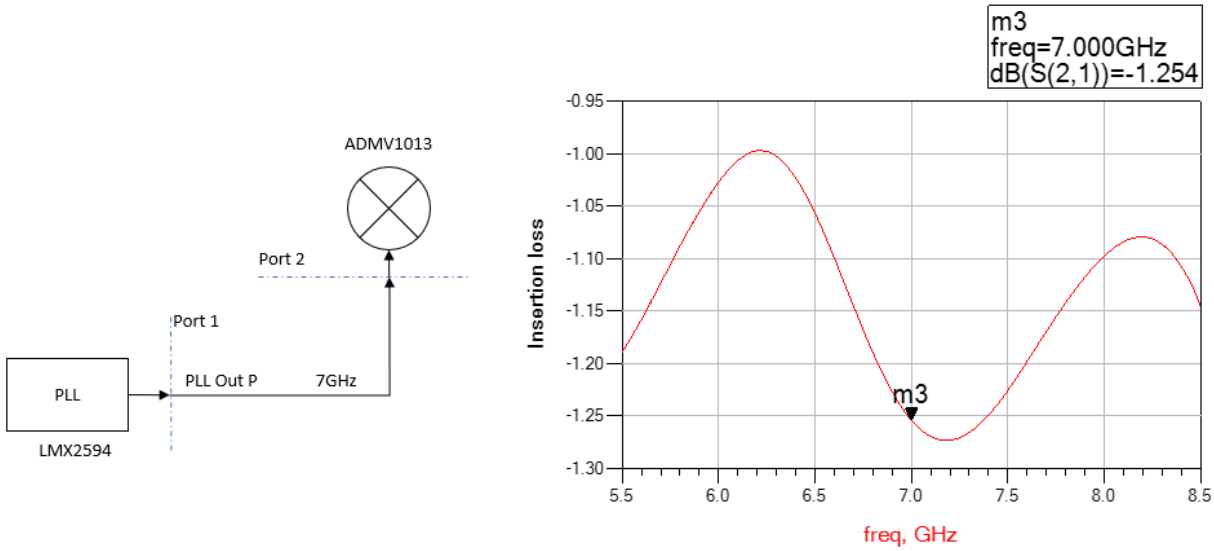

Figure 4.9

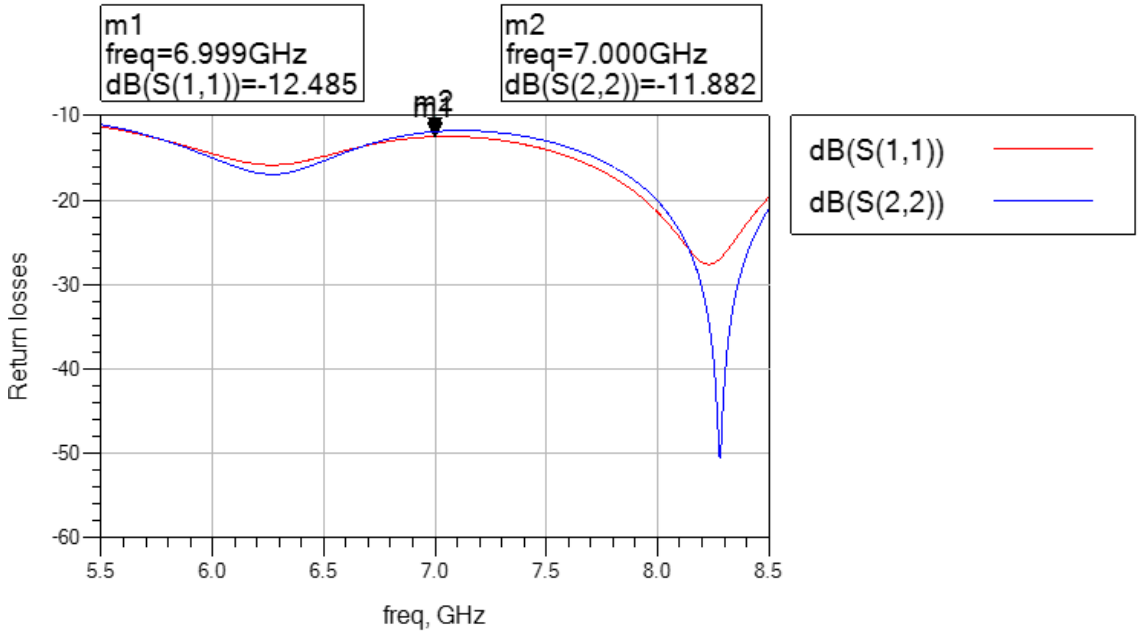

Figure 4.10

The EM Simulation setup and results for the 7GHz LOn are shown in Fig. 4.11 and Fig. 4.12 .

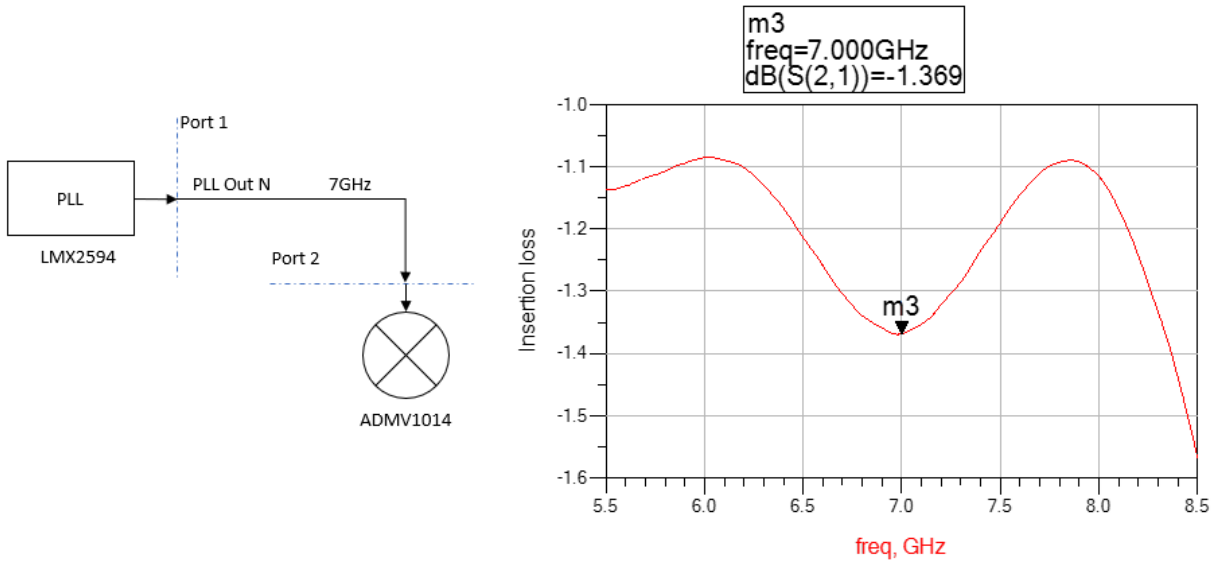

Figure 4.11

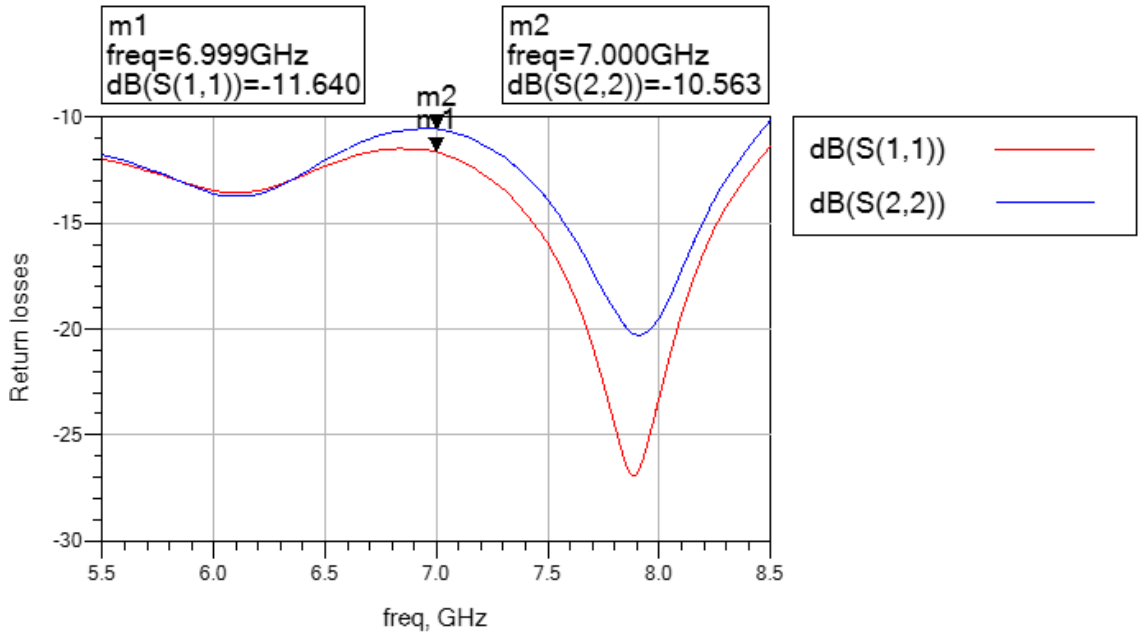

Figure 4.12

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