A Low Power VCO for Bluetooth Frequency Synthesizer

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled A Low Power VCO for Bluetooth Frequency Synthesizer, submitted by Nitesh Subramanian Naidu, to the Indian Institute of Technology Madras, for the award of the degree of Master of Technology, is a bonafide record of the work done by his under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

This project involves the design of a low power VCO for Bluetooth. The Bluetooth frequency range is $2.4\,\mathrm{GHz}$ to $2.485\,\mathrm{GHz}$. The VCO frequency range is $4.8\,\mathrm{GHz}$ to $4.97\,\mathrm{GHz}$ and quadrature carriers are obtained by dividing the VCO output by a factor of 2. The bluetooth phase noise specification is $-121\,\mathrm{dBc/Hz}$ at $2\,\mathrm{MHz}$ offset and $-90\,\mathrm{dBc/Hz}$ at $100\,\mathrm{kHz}$ offset for $2.4\,\mathrm{GHz}$ carrier frequency. The architecture used is a voltage biased VCO with a programmable tail resistance. The current in the VCO can be adjusted by programming the 2-bit tail resistor bank. As the current is not exactly defined across corners the tail resistor needs to be programmed appropriately. The capacitor bank is used for coarse tuning and MOS varactors for fine tuning. The supply to the VCO is given by an on-chip LDO. The LDO is a two stage Miller compensated Opamp which drives the PMOS output stage. The VCO output swing is sensed by a peak detector which gives an appropriate output to program the resistor bits such that the output swing as well as the phase noise specification is met. The design is implemented in a $65\,\mathrm{nm}$ CMOS process from TSMC. The area of the chip is 447μmX385μm.

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ABBREVIATIONS

VCO	Voltage Controlled Oscillator
PN	Phase Noise
LDO	Low drop out regulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
OPAMP	Operational Amplifier
Q	Quality Factor

CHAPTER 1

INTRODUCTION

1.1 Motivation

Bluetooth is a wireless standard used for exchanging data over short distances using short-wavelength UHF radio waves in the ISM band. A bluetooth transceiver requires quadrature carriers in the $2.4\,\mathrm{GHz}$ to $2.485\,\mathrm{GHz}$ frequency range. For this, a fractional N frequency synthesizer is required. The most important building block of the synthesizer is the VCO. In this work we have designed a low power VCO for bluetooth application.

It is desirable that this characteristic be relatively linear i.e. Kvco does not change significantly with tuning range. Along with the VCO, the most important part is generation of quadrature signals as most of the modern communication systems use one or the other form of quadrature mixing. One such application is, image rejection in direct conversion receivers, where both I and Q local oscillator (LO) signals are necessary to avoid any signal corruption after down conversion to baseband. There are three commonly used methods of generating quadrature signals. They are:

- Using quadrature master-slave flip-flop: Here, the VCO has to be designed for twice the required frequency. This technique works well for frequencies below 10 GHz.
- Using poly-phase filters: This approach uses VCO at the same frequency, but is not a power efficient method, as it needs drivers to drive the filter, which consume significant amount of power. Moreover, designing a poly-phase filters for a wide-band operation is not feasible, as it needs precise RC tuning to obtain quadrature signals.
- Using coupled oscillators: Here, two VCOs are coupled in such a way that, their steady state output waveforms lock in quadrature to one another. Ideally coupled oscillators have lower phase noise compared to a standalone oscillator, if the coupling network is noiseless.

The aim of this project is to design a low power VCO at twice the required frequency, satisfying the Bluetooth specifications, along with an on-chip LDO and a peak detector.

1.2 Performance parameters of oscillators

An oscillator used in RF transceivers must satisfy two requirements: (1)the frequency of output or purity of the output and (2)interface specifications eg. drive capability or output swing.

1.3 Basic principles of oscillator

An oscillator generates a periodic output. As such, the circuit must involve self sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. An oscillator may be viewed as a badly designed negative feedback amplifier such that the its phase margin is zero or negative.

In VCO designs, the preferred way is to use LC cross-coupled oscillator owing to its good phase noise performance. One disadvantage is that use of inductors makes the circuit consume more space. We wish to build a negative feedback oscillator using LC-tuned amplifier stages. The figure given below shows a stage where C_1 denotes the total capacitance seen at the output node and $R_p$is the total parallel resistance at the resonance frequency.

At low frequencies L_1 dominates the load.

$$\frac{V_{out}}{V_{in}} = -g_m L_1 s \tag{1.1}$$

At this point the gain is very small and phase is around -90^o. At resonance frequency ω , the tank reduces to R_p and

$$\frac{V_{out}}{V_{in}} = -g_m R_p \tag{1.2}$$

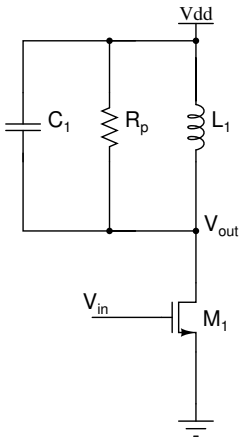

Figure 1.1: Tuned amplifier

The phase shift is now -180^o At high frequencies,

$$\frac{V_{out}}{V_{in}} = -g_m \frac{1}{C_1 s} \tag{1.3}$$

Now the gain again diminishes and the phase is +90^o. We see that the circuit provides a phase of 180^o with possible adequate gain of $g_m R_p$ at ω_o. We simply need to increase the phase shift to 360^o by inserting another stage in the loop. The circuit oscillates if the loop gain is equal to or greater than unity

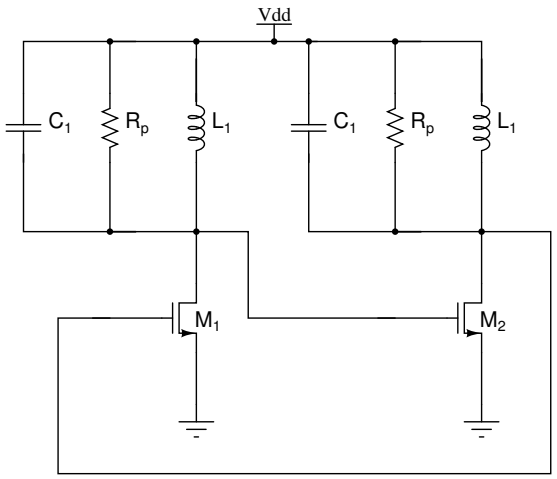

Figure 1.2: Cascade of two tuned amplifier in feedback loop

$$(g_m R_p)^2 >= 1 \tag{1.4}$$

1.4 Phase Noise

An ideal oscillator produces a perfectly-periodic output of the form x(t)=Acos(ω_ct). The zero crossings occur at exact integer multiples of T_c=2π/ω_c. In reality however the noise of the oscillator devices randomly perturbs the zero crossings. To model this perturbation we write x(t)=Acos(ω_ct+ϕ_n(t)), where ϕ_n(t) is a small random phase quantity that deviates the zero crossings from integer multiples of T_c. The term ϕ_n(t) is called Phase noise (PN).

Suppose the local oscillator suffers from phase noise and the desired signal is accompanied by a large interferer, the convolution of the desired signal and the interferer with the noisy LO spectrum results in a broadened down-converted interferer whose noise skirt corrupts the desired IF signal.

From Leesson's formula PN is [5]

$$L(\Delta\omega) \propto \frac{1}{A^2}\frac{KT}{C}\frac{\omega o}{Q}\frac{1}{\Delta\omega^2} \tag{1.5}$$

This formula gives us an idea of various aspects to be kept in mind before starting our design.

1.5 Organization of Thesis

Chapter 1 introduces the basics of oscillation and phase noise.

Chapter 2 gives the details of the VCO architecture used and challenges involved in implementing the VCO.

Chapter 3 discusses the design details of the On-Chip LDO.

Chapter 4 introduces the peak detector circuit designing.

Chapter 5 concludes the thesis with layout of VCO and simulation results after layout extraction of the VCO.

CHAPTER 2

VCO Architecture and Design

2.1 VCO Architectures

Power efficient architecture is required for Bluetooth. The output power is directly dependent on the dc power consumption of VCO. In a given process, the Q is fixed. Thus increasing output amplitude is the easiest way to reduce PN. There are many architectures proposed in literature. Some include nMOS cross coupled with pMOS current source or nMOS current source with pMOS cross coupled, but in these architectures the main problem is due to the flicker noise of the current source. Hence to reduce the PN relatively more current needs to be burnt. nMOS(or pMOS) only architecture does not have the best dc to RF power conversion efficiency for a given tank load. Complementary CMOS architecture reuses the current, hence provides double the amplitude of that of an nMOS or pMOS only VCO. In this topology, parasitic capacitances are slightly higher due to the use of pMOS, but for the targeted frequency (5 GHz) and tuning range, the effect is minimal. In the voltage biased architecture there is no current source and the flicker noise contribution by it is absent. In the voltage biased VCO the current changes from SS to FF corners. Hence to maintain a well defined current this topology of VCO comes with a programmable tail resistor. The tail resistance consists of a fixed resistor and a two bit programmable resistor.

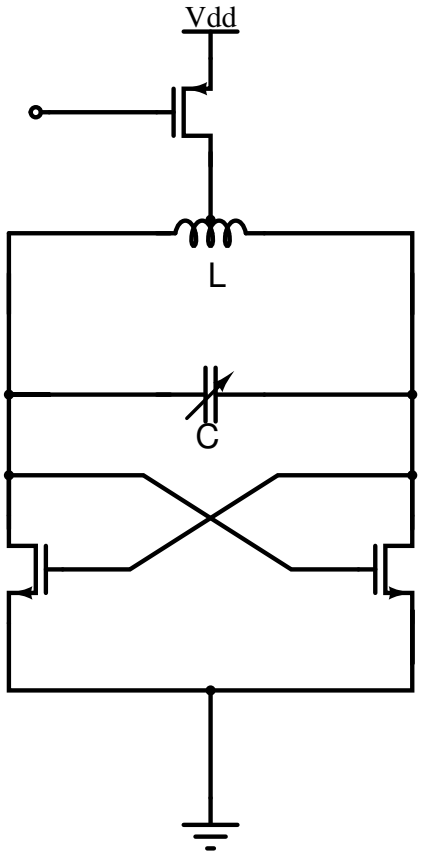

Figure 2.1: nMOS cross coupled with pMOS current source VCO

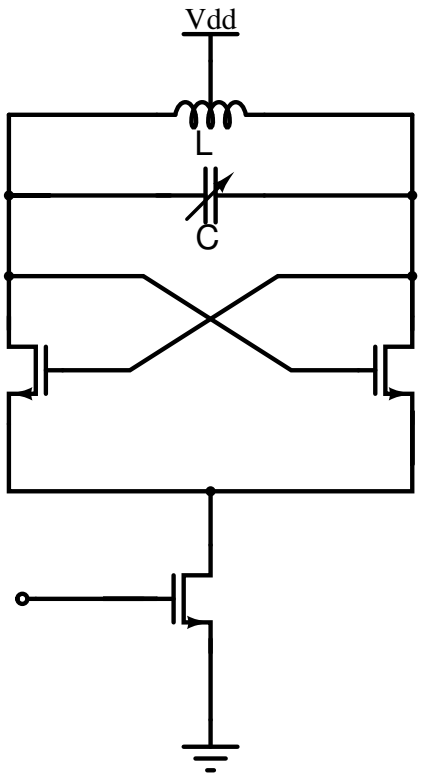

Figure 2.2: nMOS cross coupled with nMOS current source VCO

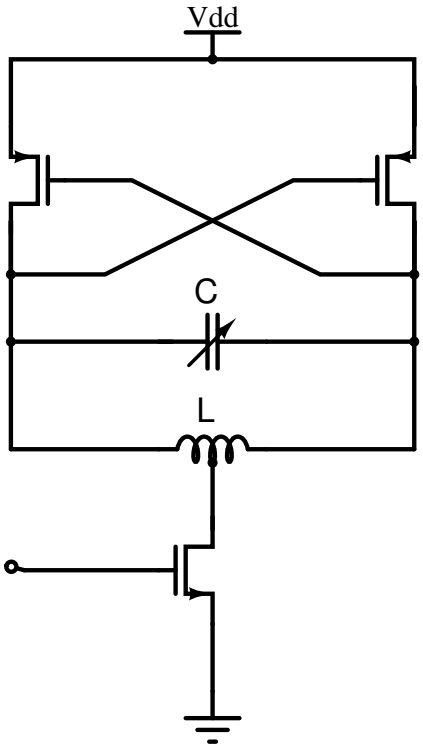

Figure 2.3: pMOS cross coupled with nMOS current source VCO

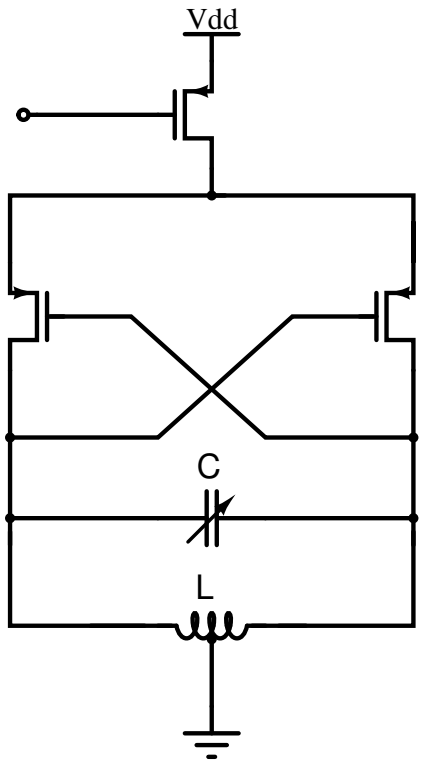

Figure 2.4: pMOS cross coupled with pMOS current source VCO

2.2 Voltage biased VCO architecture

The voltage biased VCO has more advantages compared to the current biased VCO. We choose to go ahead with the voltage biased VCO. In our VCO topology, the capacitor bank has a 4-bit coarse tuning. The tuning is such that all the frequency bands are covered in all the corners. The VCO being voltage biased needs an on-chip LDO as the supply rails are noisy and degrades the PN severely. The VCO is powered by a 1V supply. The LDO needed is a 1.2 V to 1 V converter with low output noise such that it does not degrade the PN significantly.

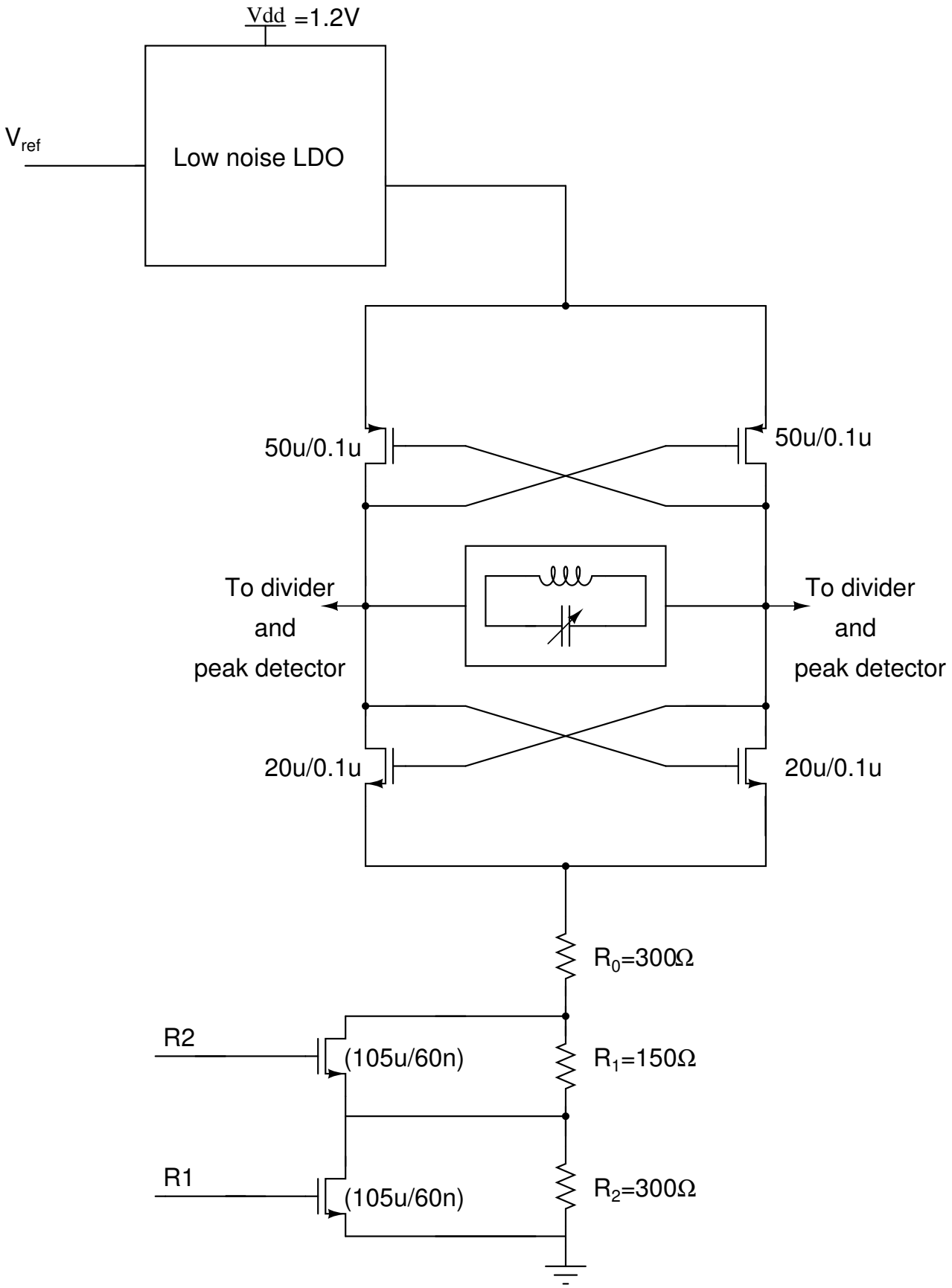

Figure 2.5: VCO schematic

2.3 VCO Design

2.3.1 Choice of Inductor

To achieve a good phase noise specification with low power, the Q(quality factor) of the tank should be maximized. The Q of the tank is mainly dominated by the inductor as the capacitor Q are usually much high. Here R_s represents the series loss of the inductor and ω_o is the resonance frequency.

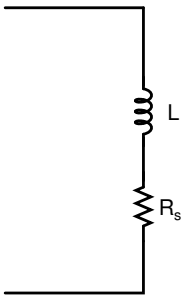

Figure 2.6: Inductor with a series loss

$$Q = \frac{\omega_o L}{R_s} \tag{2.1}$$

We try to use a high value of inductor with a high Q from the design library. In our design we are trying to reduce the power consumption. Use of high inductor value will lead to high value of parallel resistance (R_p).

$$R_p = \omega_o L Q \tag{2.2}$$

If R_p is high, we need to burn less start-up current. One more constraint is that if we use very high inductor values we need to use very low capacitor values for covering the same frequency band and this may degrade the tuning range and also PN, also use of high inductor values demands very large area. In our case library inductor of $2\,\mathrm{nH}$ with Q of 21 at $5\,\mathrm{GHz}$ used in the design. The inductor area consumes about 300ux300u of area. Using very low capacitors may be problematic owing to the parasitic capacitors which may become dominant.

2.3.2 Capacitor bank

The switches in the capacitor bank should be as large as possible so that it does not degrade the Q of the bank. But if the size of the switch is too large then the C_{gd} of the switch leads to AM to PM conversion resulting in PN degradation. Kvco between 100-200MHz/V is maintained across tuning range and PVT. MOM capacitor is used owing to its high density and better Q for the same value of capacitor of MIM type. The capacitor bank has capacitance of sizes 1X, 2X, 3X, 4X where X is the minimum value of the single ended capacitor whose value is $40\,\mathrm{fF}$.

The minimum value of capacitor (single ended) used in the bank is 40 fF and the maximum value is 320 fF. Due to the capacitor bank, the Q of the bank now becomes less than 21 because of loading. The approximate Q of the tank is given below.

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{C_1}{C_{total}Q_1} + \frac{C_3}{C_{total}Q_3} + \frac{C_4}{C_{total}Q_4} + \frac{C_4}{C_{total}Q_4} \tag{2.3}$$

$$C_{total} = C_1 + C_2 + C_3 + C_4 + C_{ext} + C_{varactor} \tag{2.4}$$

In the above equation the capacitor values are differential and the C_{total} comes to be about 560fF. Here the loss in the varactor is not considered. Tha calculation results in Q_{tank} of 19. Now the R_p of the tank is as follows:

$$\frac{R_p}{\omega_o L} = Q_{tank} \tag{2.5}$$

The R_p is 1.19 kΩ roughly in the range of 5 GHz. For a fixed value of current in the VCO the differential output swing is given by:

$$V_{out} = \frac{2}{\pi} I_o R_p \tag{2.6}$$

By rule of thumb, the capacitance associated with the gate-drain overlap of the

switch is kept ten times lower than the single ended capacitor of the particular branch in off state. The gate-drain overlap capacitance of the first branch is 4 fF.

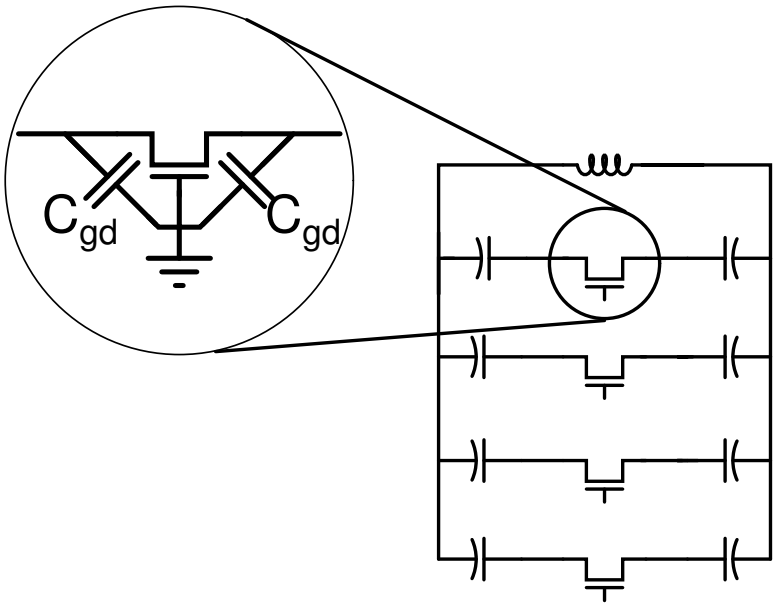

Figure 2.7: MOS switch parasitics

The on-state overlap capacitance does not matter as the MOS switch acts as an effective short for the current. An external capacitor of 196 fF is used for tuning correction. When all the capacitors in the bank are turned off, the tuning is determined by the external capacitor and the overlap capacitance of the switches.

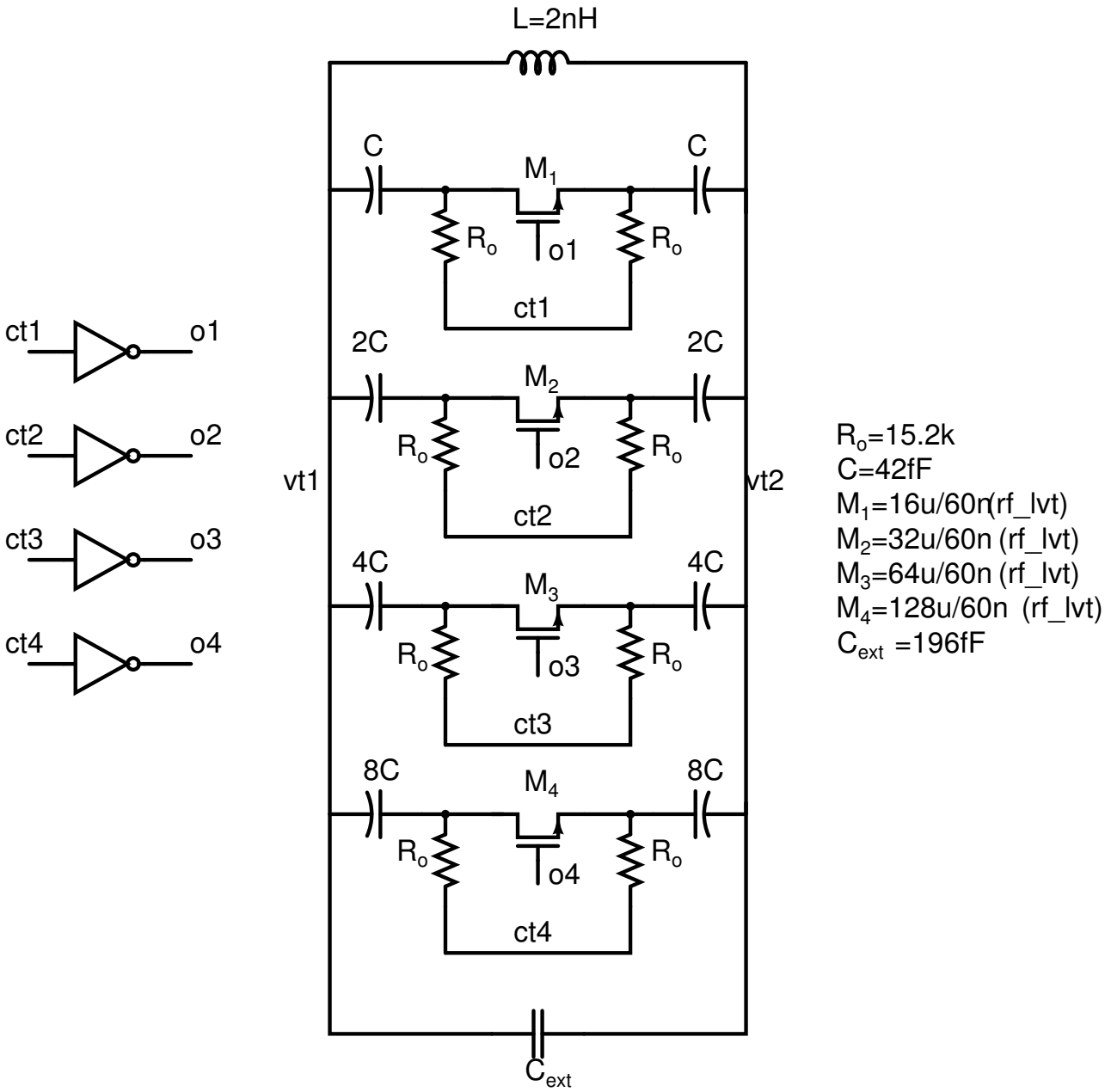

Figure 2.8: Capacitor bank

2.3.3 Varactor

The choice of varactor is such that there should not be any dead zone in the tuning range and the minimum value of ΔC should be greater than the step size in the capacitor bank. The varactor used is a nMOS capacitor in a n-well which has a monotonic change in capacitance with applied bias voltage. In our circuit we have used two nmos capacitors of appropriate sizes. The gate of the varactor(positive) is connected to a fixed bias voltage of 600mV, and the input to the VCO is given to the negative terminal of the varactor. Very high value of varactors gives rise to high value of Kvco.

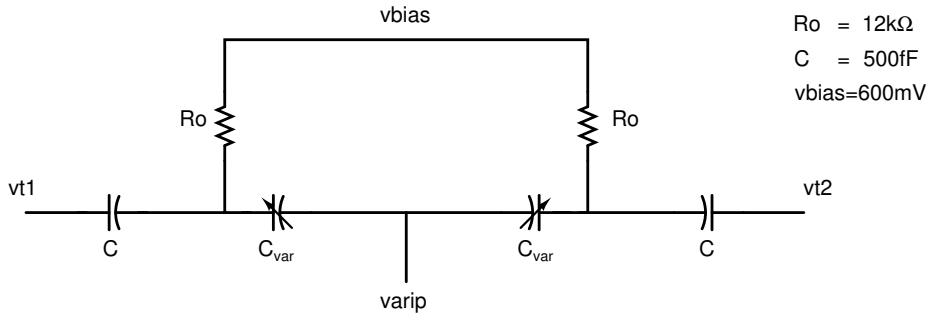

Figure 2.9: Varactor biasing

$$K_{vco} = \frac{\omega_o \Delta C}{2C_{total}\Delta V} \tag{2.7}$$

If Kvco becomes too high it may increase the unity loop gain of the PLL. Kvco is kept between $100\,\mathrm{MHz}$-$200\,\mathrm{MHz}$ in this design.

Degradation of Q due to varactor

As we change the input voltage to the VCO the capacitance of the varactor changes from 42 fF-164 fF (single ended). Using SP analysis in cadence, the series resistance of the varactor comes to be about 17Ω at 80^oC

The worst case Q of the varactor (Q_{var}) turns out to be as follows

$$Q_{var} = \frac{1}{\omega_o R_s C_{var}} \tag{2.8}$$

Taking C_{var}=164fF, the value of Q_{var} comes out to be about 12. In the calculations ω_o is taken to be 4.8GHz since ω_o decreases as C increases. The Q of the varactor is boosted by a factor as shown in equ(3.8)

$$Q_c = 1 + \frac{C_{total} - C_{var}}{C_{var}} Q_{var} \tag{2.9}$$

Using these values and plugging it in the given equation below,

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{C_1}{C_{total}Q_1} + \frac{C_3}{C_{total}Q_3} + \frac{C_4}{C_{total}Q_4} + \frac{C_4}{C_{total}Q_4} + \frac{C_{var}}{C_{total}Q_{var}} \quad (2.10)$$

The value of Q_{tank} comes out to be 16, and the corresponding value of R_p is 1kΩ

2.3.4 Tail resistance

In the voltage biased VCO, as mentioned before , the current is not well defined and changes from corner to corner. Hence, we have a programmable tail resistance. Another advantage of the tail resistance is that it increases the common mode impedance and improves the PN. A fixed resistance of 300Ω is used and a 2-bit resistor bank of 150Ω and 300Ω is used. The resistors are in parallel with nMOS whose on-state resistance is 4Ω which can act as an effective short. R1 corresponds to 300Ω and R2 150Ω.

2.3.5 Negative resistance

We have used an nMOS-pMOS cross-coupled pair in the design. The inductor and capacitors always come with a resistive component. This resistive component is responsible for decaying down of the oscillations. We therefore need active devices which can act as a negative resistance to overcome the loss. The cross-coupled devices need to have transconductance such that the loss is appropriately compensated. As we are using both pMOS-nMOS pair the oscillation condition becomes:

$$\frac{2}{g_{mp} + g_{mn}} = R_p \quad (2.11)$$

In SS corner we try to simulate our VCO and we short the tail resistance as the current in SS corner will be low. In this case the current is 530 μA. The transconductance of nMOS and pMOS is 2.26 mS and 2.3 mS respectively. We see that the neagative

resistance value is as per the above equation and it is less than R_p value ensuring that the VCO will oscillate.

2.3.6 VCO simulation results

Transient simulation

The transient response at SS corner 80^oC is shown fig 2.10.

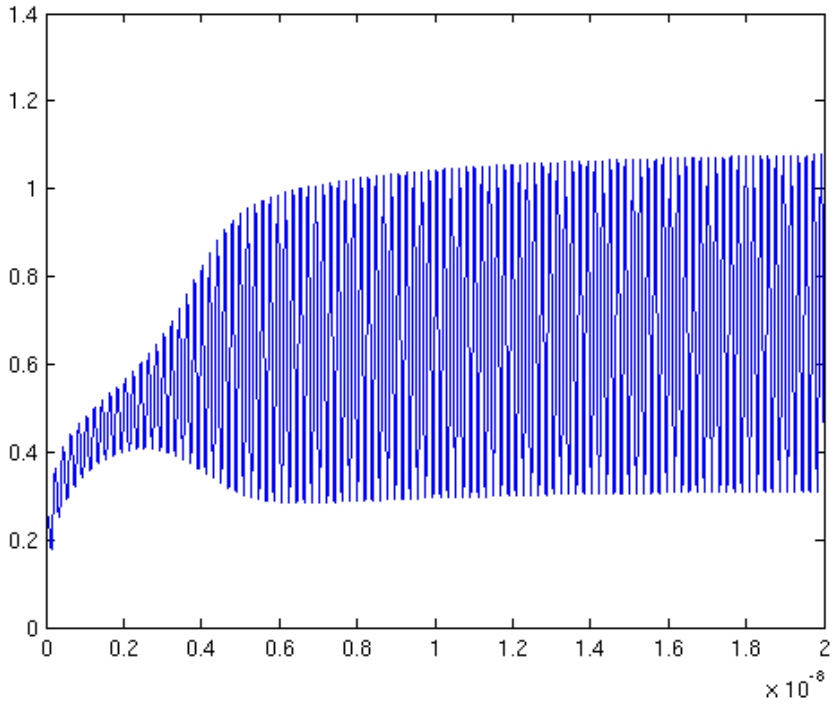

Figure 2.10: Single ended transient response at SS corner 80^oC

Tuning range

The VCO tuning range is presented in fig 2.11, 2.12, 2.13

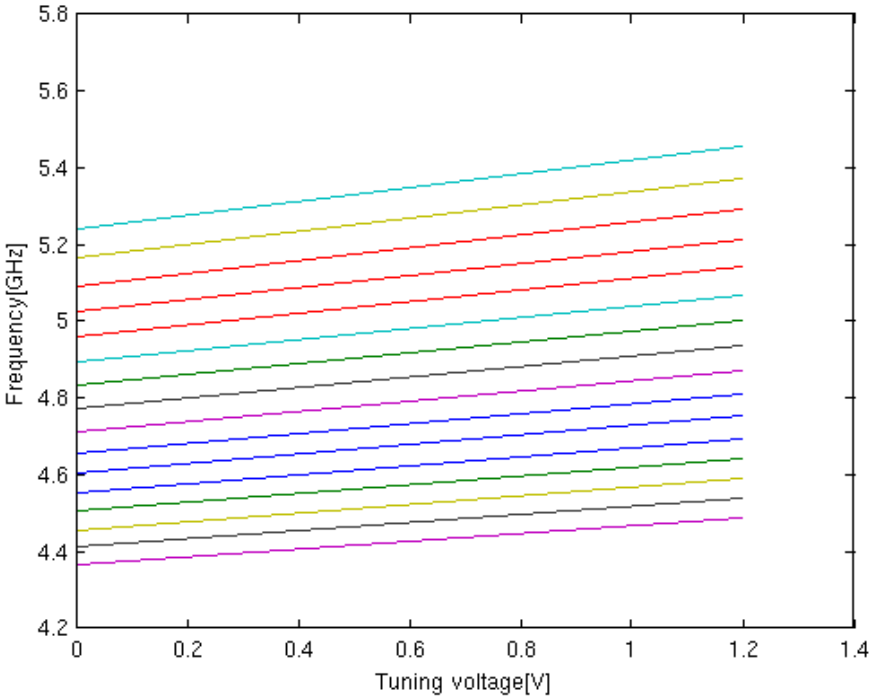

Figure 2.11: Tuning curve for TT corner

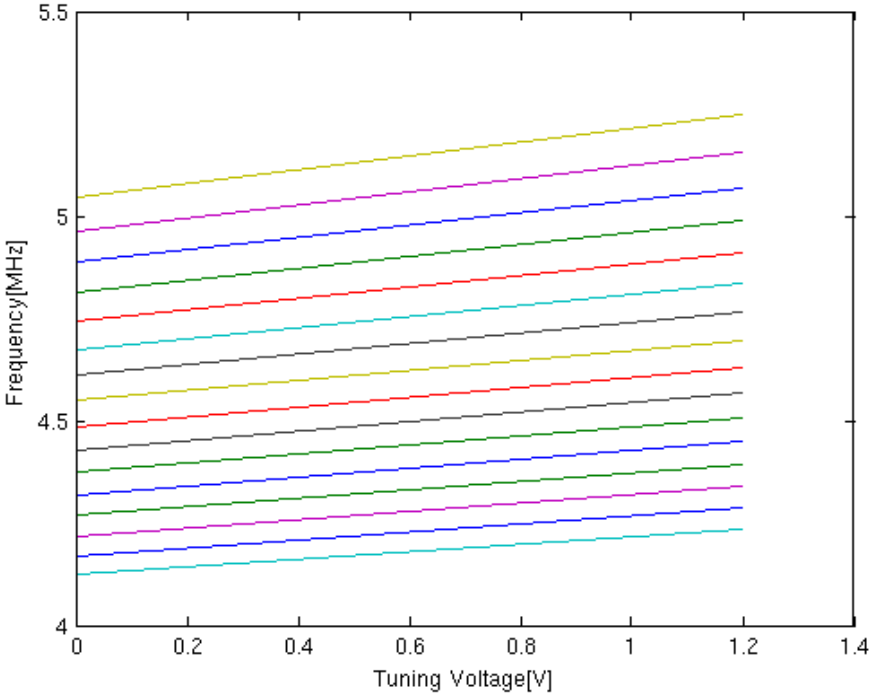

Figure 2.12: Tuning curve for SS corner

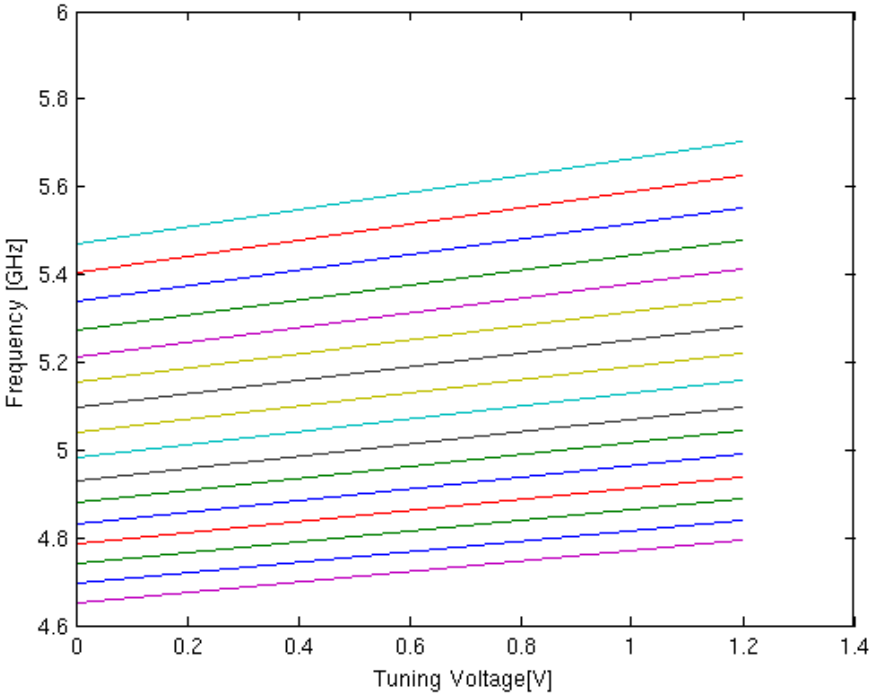

Figure 2.13: Tuning curve for FF corner

Phase Noise

The fig 2.14 shows the plots of phase noise of the VCO for a carrier frequency of 4.8 GHz

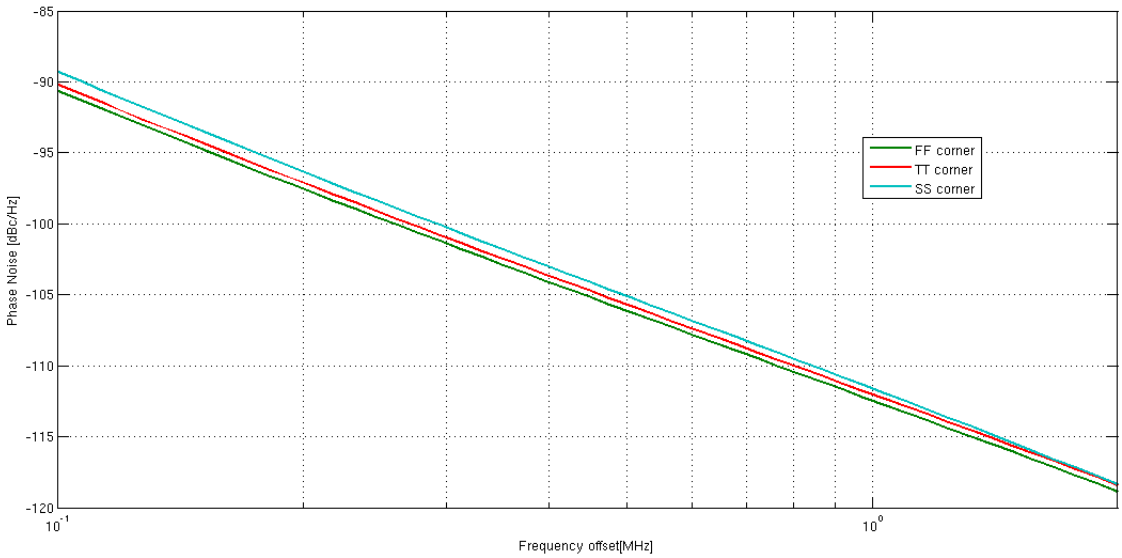

Figure 2.14: Phase noise plots at 4.8GHz carrier frequency

CHAPTER 3

On-chip LDO

3.1 Design of LDO

The supply rails is noisy and cannot be used to power the VCO. The supply noise needs to be filtered out. Thus we need an LDO to power the VCO. The LDO needs to be of low output noise and better PSRR. In our design, we use a two stage OPAMP driving an output PMOS transistor which provides current to the VCO. The phase noise of the VCO at 2 MHz offset is to be -121 dBc/Hz at 2.4 GHz. The LDO bandwidth therefore should be maintained above 2MHz. It should filter out all the supply noise upto 2 MHz and also be low noise. By burning more current in the first stage or increasing the g_m of the input stage transistors the output noise can be reduced.

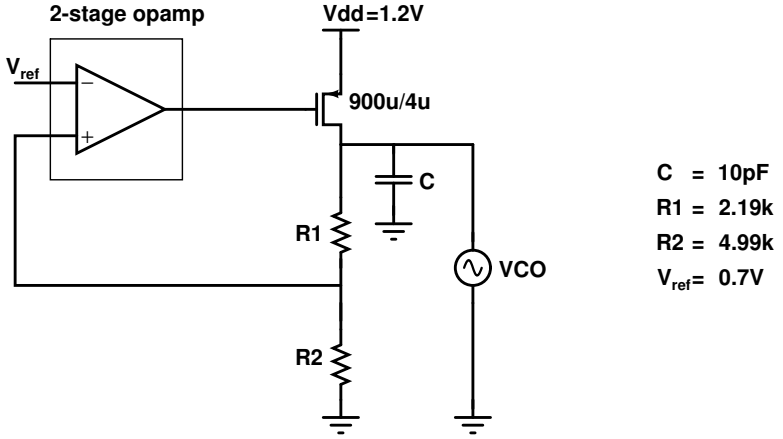

Figure 3.1: LDO with VCO load

3.2 Implementation of LDO

The schematic of the two-stage OPAMP used in the LDO is given below.

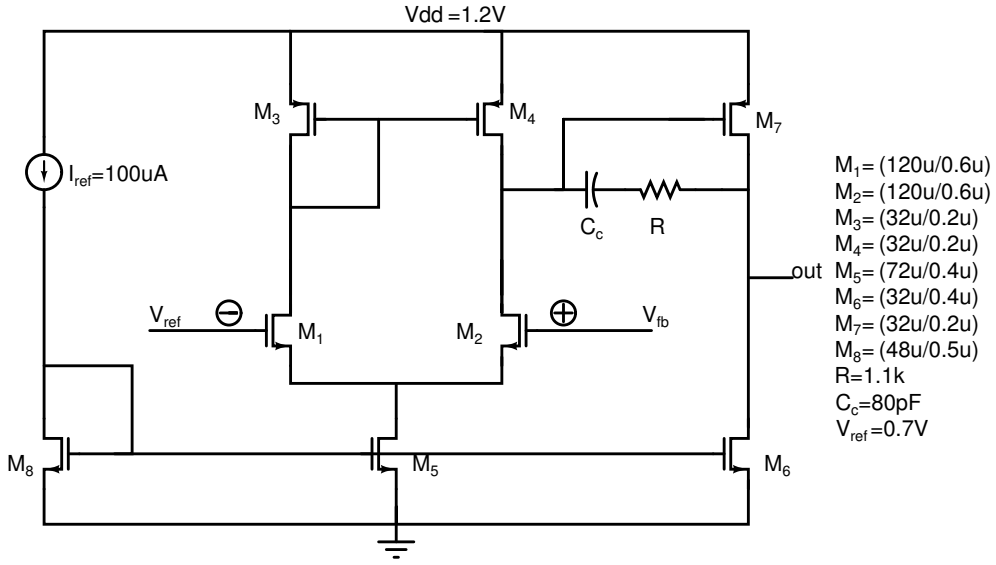

Figure 3.2: 2-stage OPAMP

The two stage OPAMP is used in the LDO. A miller capacitor (moscap) of 80 fF is used for stability. The loop gain and phase plot is shown in fig 3.3.

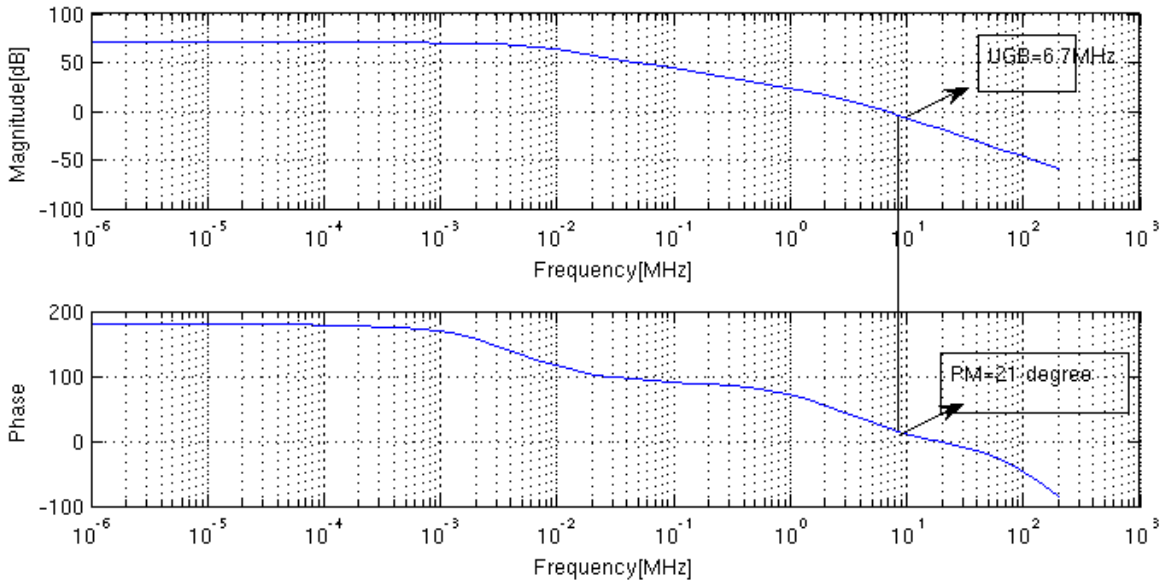

Figure 3.3: Loop Gain and Phase Plot without Load

The bandwidth of the LDO without loading is $6.7\,\mathrm{MHz}$. The DC gain of the loop is $77\,\mathrm{dB}$ and phase margin 21^o.

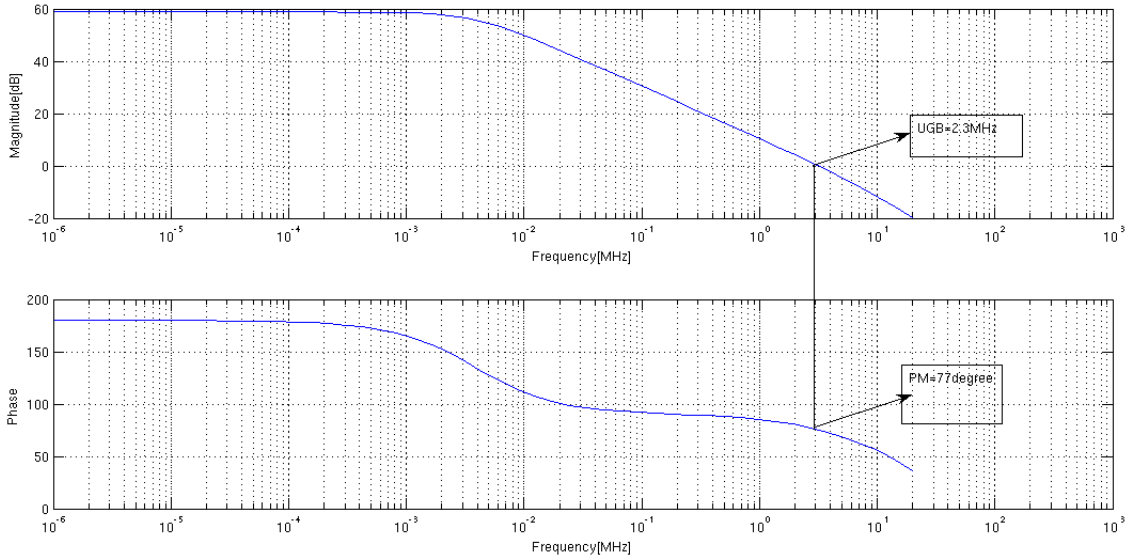

Figure 3.4: Loop Gain and Phase Plot with VCO Load

The bandwidth of the LDO with VCO load is $2.3\,\mathrm{MHz}$. The DC gain of the loop is 55 dB and phase margin is maintained at 77^o for stability. If the phase margin is kept too low, then there is a sudden voltage drop at the output during the start of the circuit and the VCO may stop oscillating. To avoid this we have maintained a good phase margin value for the loop. The LDO needs to reject the supply noise and a good PSRR is required to avoid degradation of PN due to supply noise. AS the loop gain is maintained high upto the bandwidth, any noise injected will be rejected by the LDO. The current consumption of the LDO is 360 uA in SS corner and goes upto 410 uA in FF corner. This current is the current burnt in the LDO which is not a part of the VCO. The fig 3.5 shows the PSRR of the LDO with the VCO load. A worst case phase noise degradation of $1.8\,\mathrm{dBc/Hz}$ is observed for $9\,\mathrm{nV/sqrt(Hz)}$ of white noise.

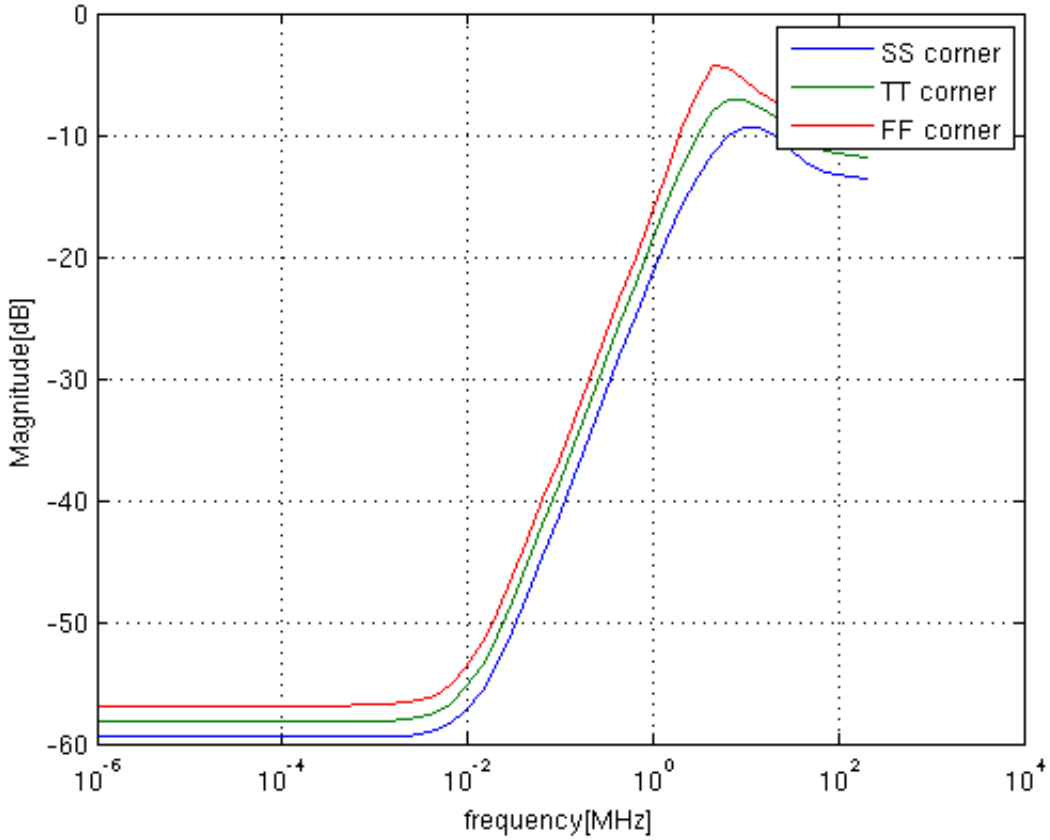

Figure 3.5: PSRR plot

3.3 LDO noise

The LDO output noise is shown in fig3.6. The output noise at $2\,\mathrm{MHz}$ is $12\,\mathrm{nV/sqrt(Hz)}$

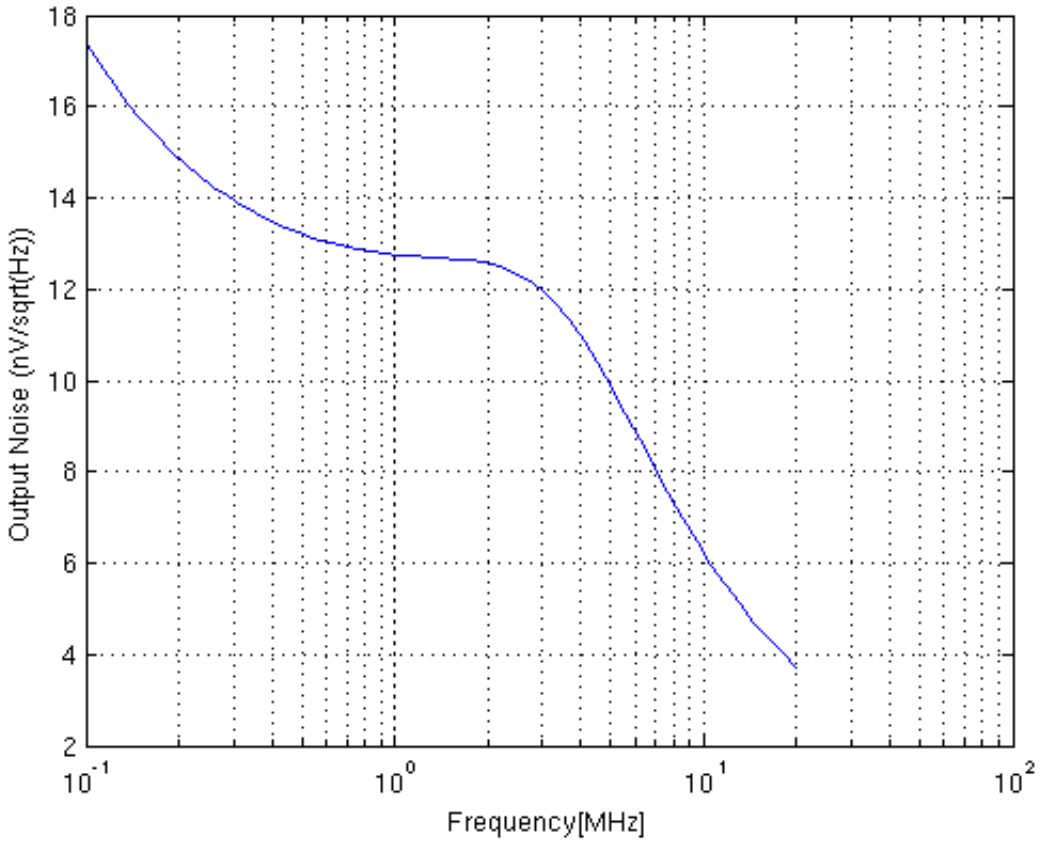

Figure 3.6: LDO noise plot

CHAPTER 4

Peak Detector

4.1 Need for peak detection

The ampltude of the VCO changes from corner to corner, for a given value of tail resistor. Hence, it becomes necessary to detect the amplitude of oscillation and program the resistor bank appropriately. We sense the output and drive a circuit whose output is a one-bit signal indicating whether the output is above a threshold or not. About 200 μA current can be saved in this scheme. For the same tail resistance, the current consumed in the VCO is FF corner is more than the current consumed in the SS corner. In the FF corner the phase noise specification is over met by simply consuming more power which is not needed. Thus the signal given by the peak detection circuit enables us to program the resistor bank externally.

4.2 Implementation of Peak Detector

In the peak detection circuit we sense the output of the VCO from coupling capacitors and use it to drive an nMOS differential pair circuit with a nMOS current source.

In the circuit shown below, the drive signal sets the voltage such that the tail transistor M_1 is biased at 400 mV. The tail transistor M_1 cannot be biased exactly at 400 mV by using a fixed drive as the tail node voltage will change from SS corner to FF corner. We therefore need a negative feedback circuit which will keep the tail node at a fixed voltage. We make use of a replica biasing scheme in which will set the voltage at the tail node to be 400 mV.

In fig the peak_ref is set as 400 mV so that the value of peak_out is nearly 400 mV.

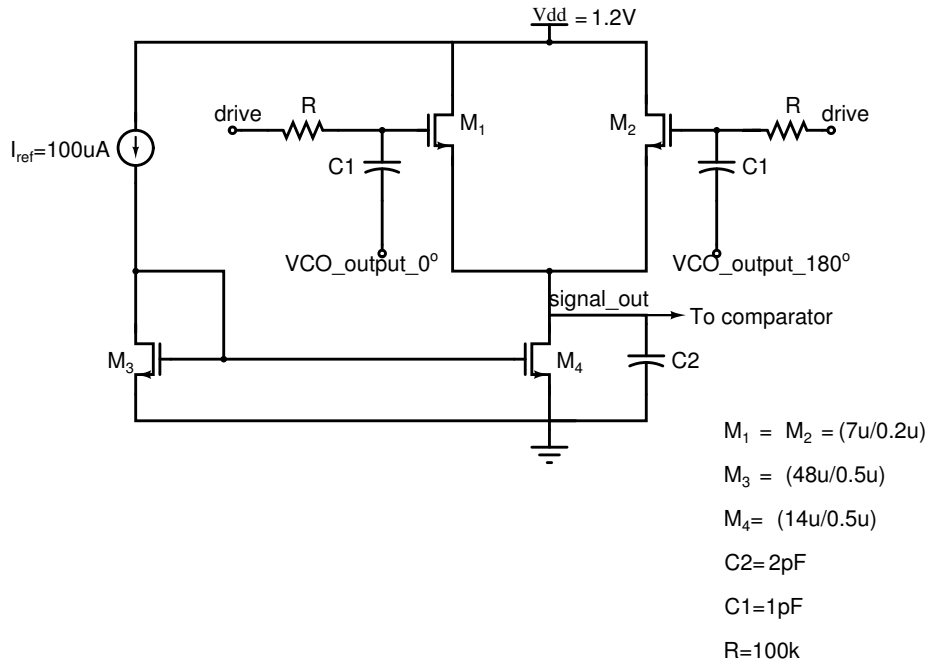

Figure 4.1: nMOS differential input of the peak detection circuit

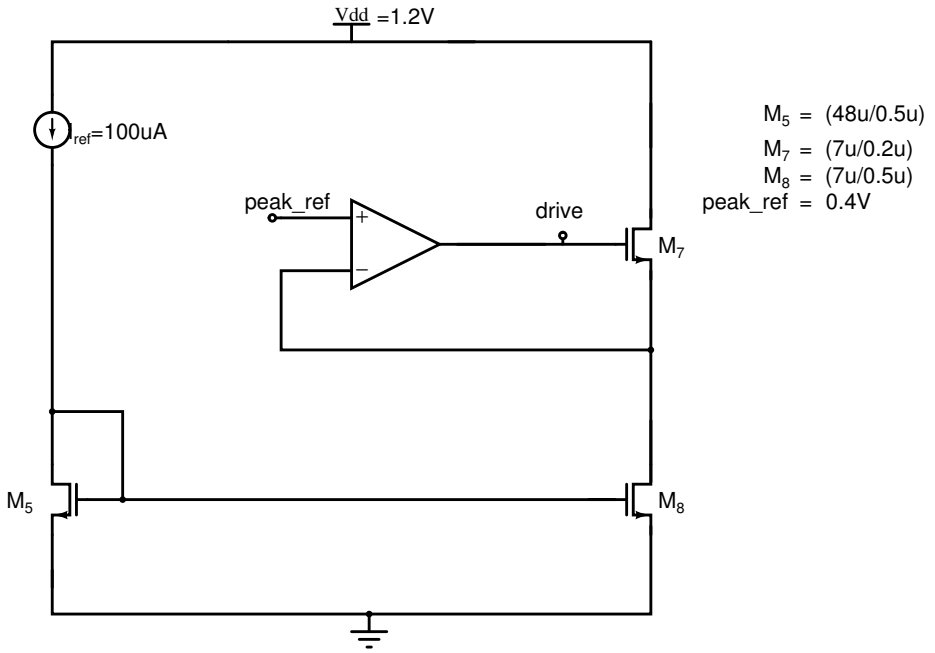

Figure 4.2: Negative feedback circuit to set the voltage of tail node of peak detection circuit

The differential output of the VCO, through a coupling capacitor is fed to the peak detector circuit. The transconductance of the differential pair is $275\,\mu$S. The power consumption in the replica bias is $15\,\mu$A. The total power consumption in the peak detector circuit in steady state is within $50\,\mu$A.

4.3 Working of Peak Detector

When the output of the VCO through a coupling capacitor is fed to the input nMOS differential pair is fed, the current through the nMOS pair will be higher than the current in the tail transistor. Since the current in the tail transistor is less than the nMOS differential pair transistors the tail node voltage will ramp up. The tail node voltage will increase to such a point that the average current in the nMOS pair will be equal to the current in the tail transistors. Through calibrations we see that the average increase in tail node is half times the single ended peak voltage. The tail node voltage is fed to the input of a differential pair as shown in the figure below. The reference to this differential OPAMP is 500 mV. We have chosen this reference to be 500 mV as this value ensures if the differential peak to peak amplitude of the VCO is above 1 V . Therefore, the peak_thresold is set to be 500 mV. The output of the OPAMP is fed to a series of five inverters which provide a high gain. If the tail node of the nMOS differential pair (signal$_o utin fig 5.3) is greater than 500\,mV, which corresponds to 1\,V of VCO differential peak to pea$

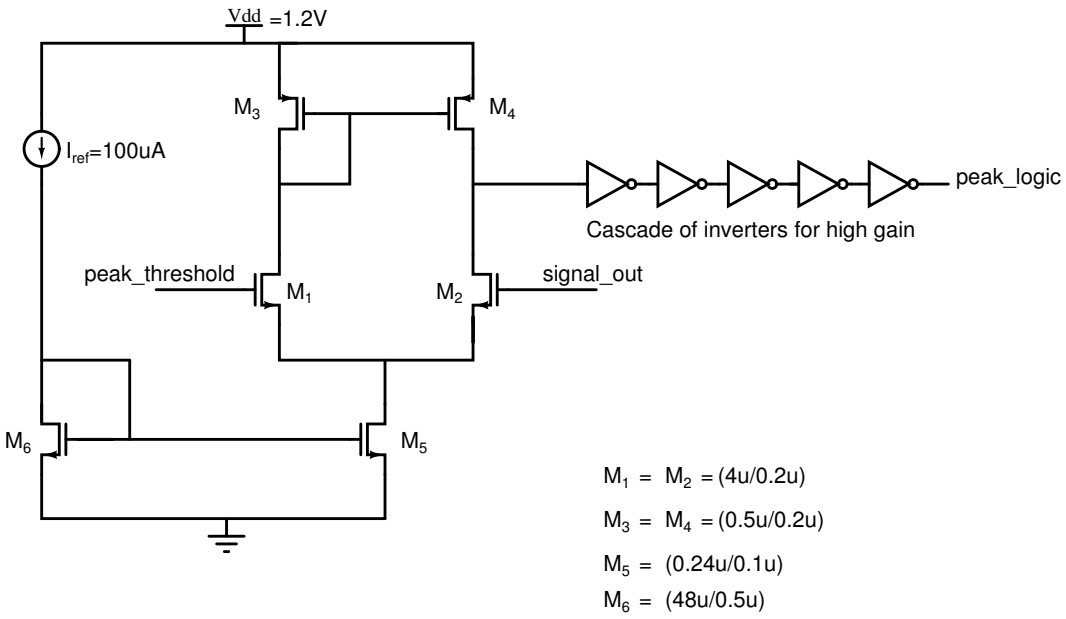

Figure 4.3: Negative feedback circuit to set the voltage of tail node of peak detection circuit

4.4 Simulation Results for peak detector

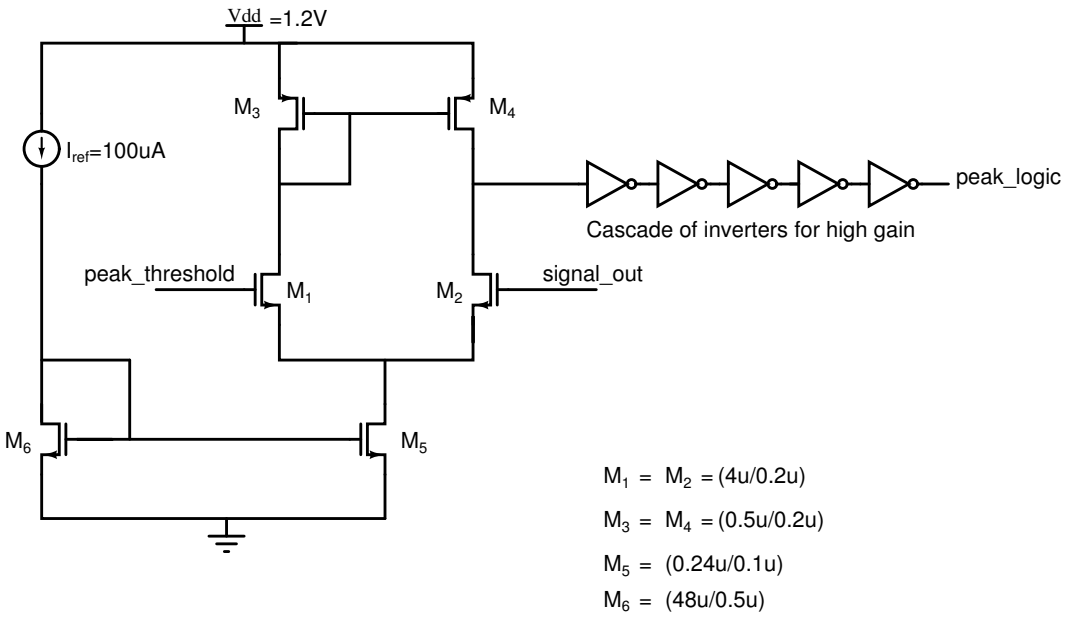

Figure 4.4: Negative feedback circuit to set the voltage of tail node of peak detection circuit

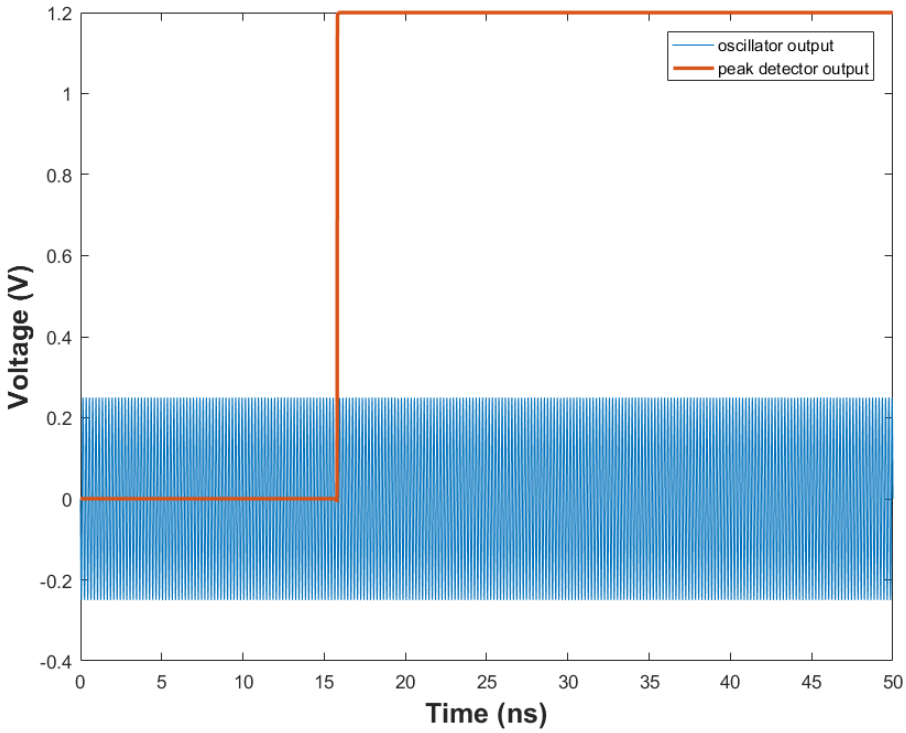

Figure 4.5: Peak detector output for oscillator swing of $1V_{p-p}$

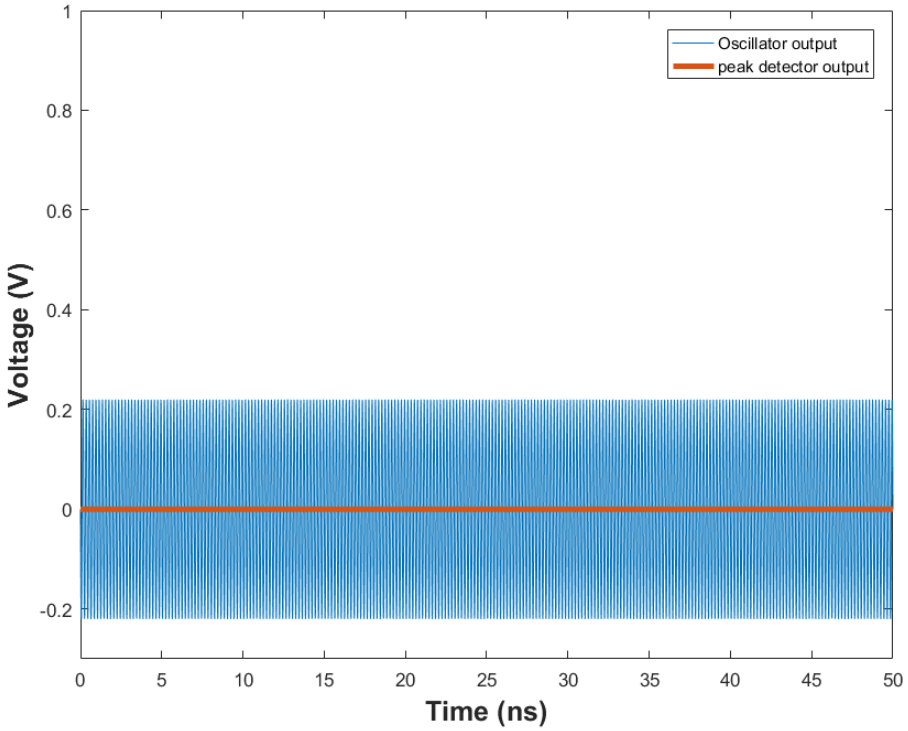

Figure 4.6: Peak detector output for oscillator swing of 900mV_{p-p}

CHAPTER 5

LAYOUT AND POST-LAYOUT SIMULATION RESULTS FOR THE VCO

5.1 Layout of the VCO

The layout of the VCO including the LDO, peak detector and dividers is shown in figure 5.1. The design occupies an area of 0.45 mmX0.38 mm.

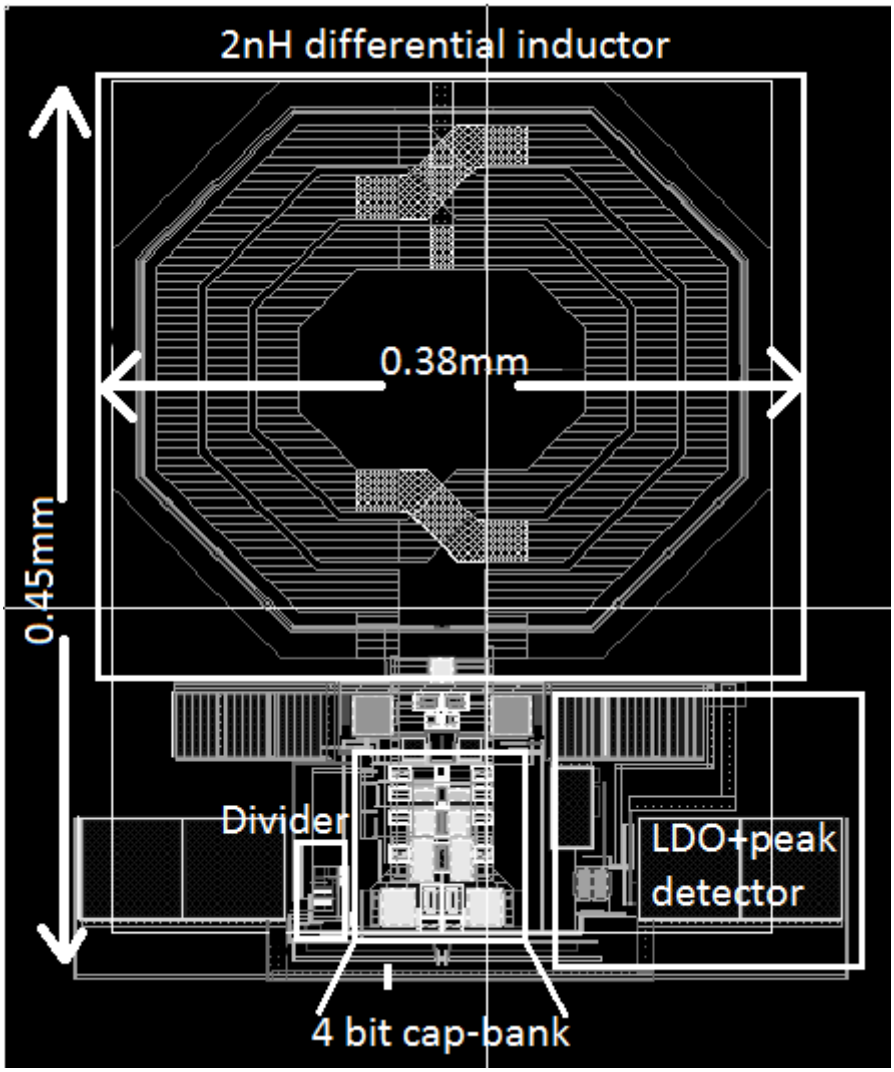

Figure 5.1: Layout of the VCO.

5.2 Post-layout simulation results

5.2.1 VCO tuning range

The VCO tuning range is shown in the figures gives below. As mentioned early, the maximum frequency attained in the SS corner is kept to be slightly above 5 GHz and the minimum frequency at FF corner is kept below 4.8 GHz. The tuning curves in the respective corners is shown.

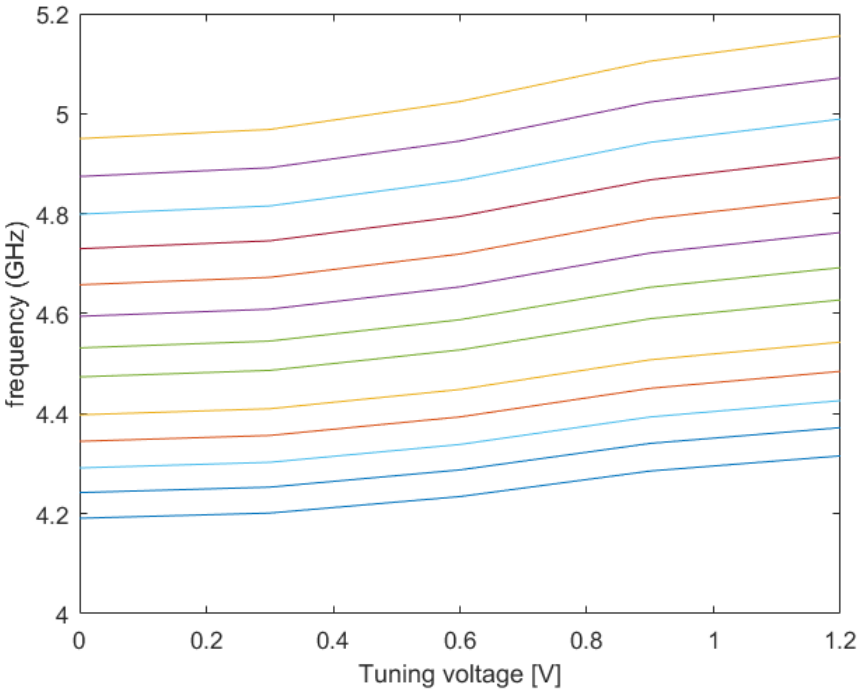

Figure 5.2: Tuning range in SS corner

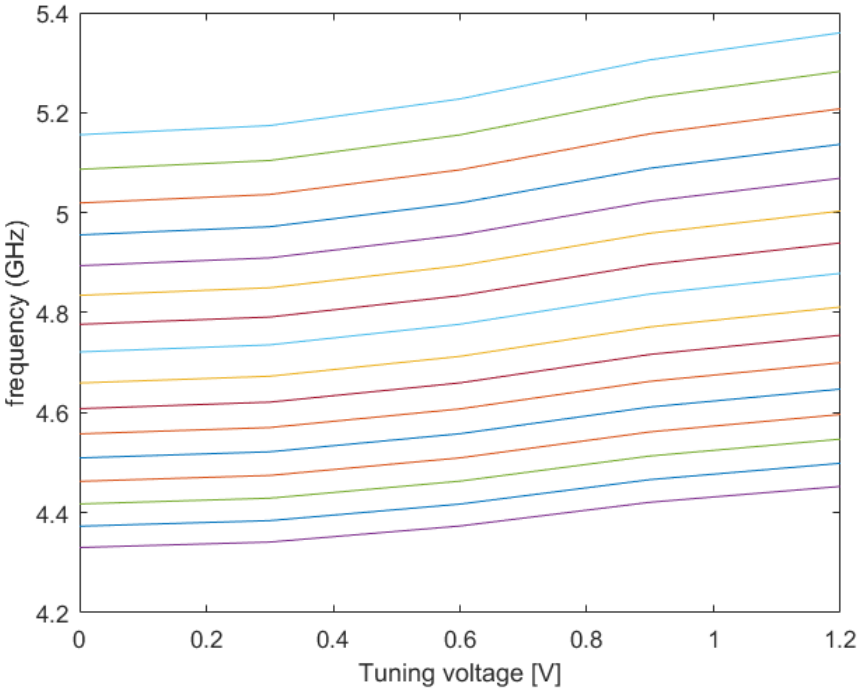

Figure 5.3: Tuning range in TT corner

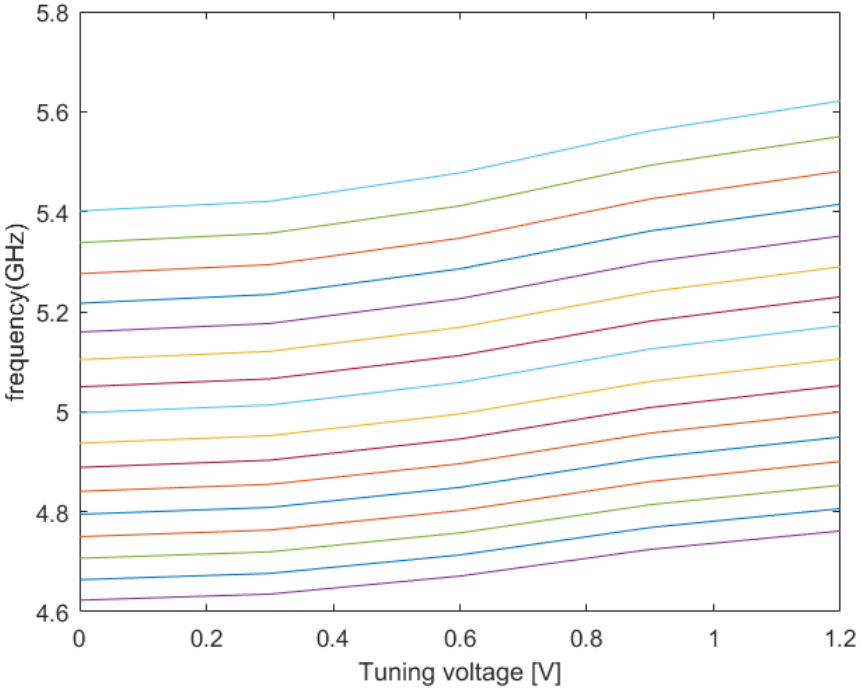

Figure 5.4: Tuning range in FF corner

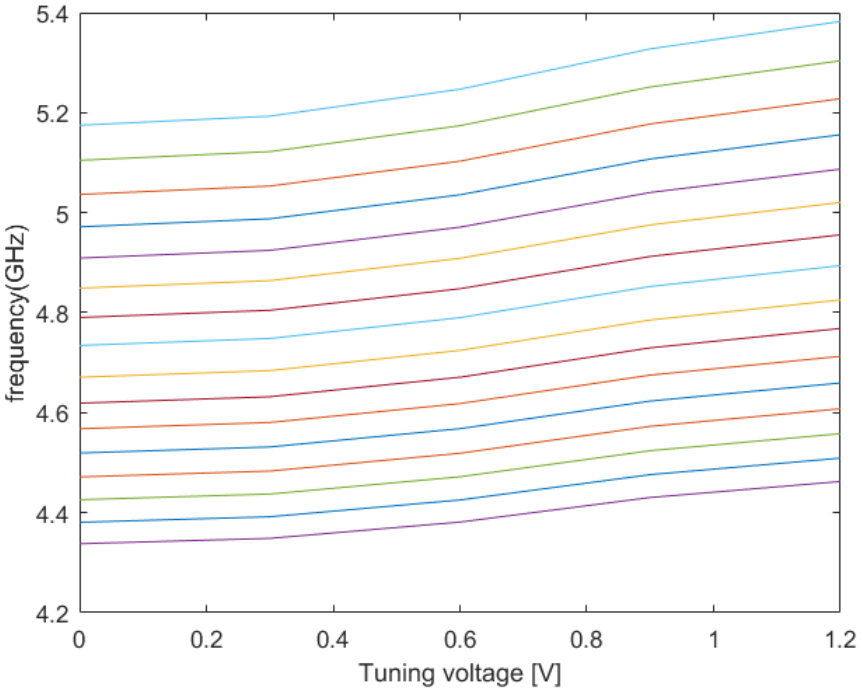

Figure 5.5: Tuning range in FS corner

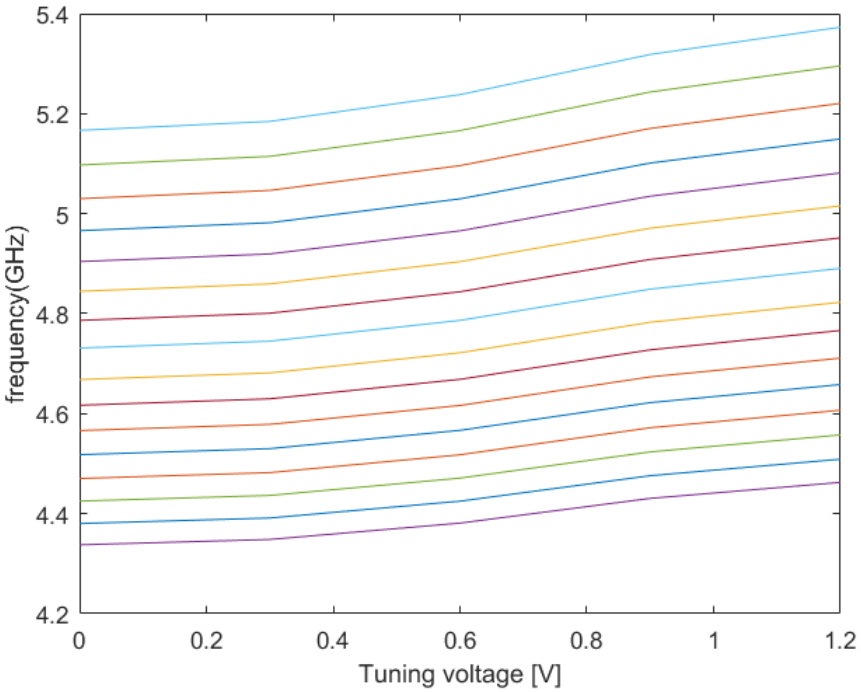

Figure 5.6: Tuning range in SF corner

5.2.2 Phase noise simulation results

The phase noise plots are presented in fig 5.7.

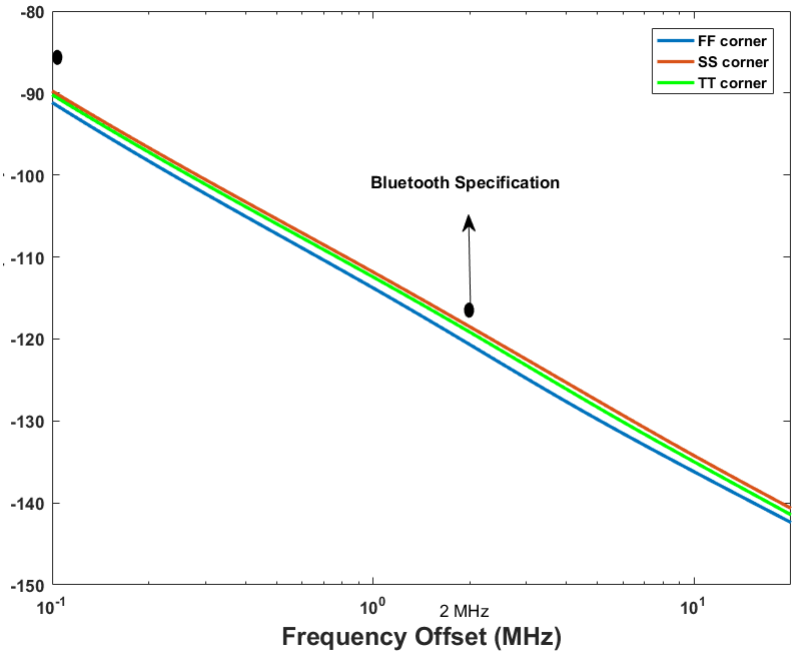

Figure 5.7: PN at 4.8 GHz carrier frequency

CHAPTER 6

Appendix

The tables presented below gives an idea of choice of bits for the capacitor bank and resistor bank in the respective corners. The first four rows of each table gives the idea of bits to be used for tuning in 5 GHz range and lower four rows gives an idea of tuning in 4.8 GHz range. Here ct1 ct2 ct3 ct4 is the cap bank bits where ct1 is LSB ct4 is MSB. R1 R2 corresponds to the resistor bank where R1 is MSB (300Ω) and R2 is LSB (150Ω)

Table 6.1: SS corner simulation results at 80^{o}C

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 1	1 1 1 1	1.2V	5.118GHz	-116.3dBc/Hz	1.18V	519uW
1 1	1 1 1 1	0V	4.93GHz	-117.6dBc/Hz	1.06V	507uW
1 0	1 1 1 1	1.2V	5.14GHz	-116.8dBc/Hz	0.82V	357uW
1 0	1 1 1 1	0V	4.94GHz	-113.7dBc/Hz (spec not met)	0.6V	310uW
1 1	0 0 1 1	1.2V	4.88GHz	-117.3dBc/Hz	1.12V	514uW
1 1	0 0 1 1	0V	4.72GHz	-118.5dBc/Hz	1V	498uW
1 0	0 0 1 1	1.2V	4.89GHz	-115.8dBc/Hz	1.12V	514uW
1 0	0 0 1 1	0V	4.72GHz	-112.5dBc/Hz (spec not met)	0.5V	226uW

Table 6.2: SS corner simulation results at 0^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 1	1 1 1 1	1.2V	5.13GHz	-115.9dBc/Hz	1.36V	509uW
1 1	1 1 1 1	0V	4.94GHz	-117.2dBc/Hz	1.26V	509uW
1 0	1 1 1 1	1.2V	5.16GHz	-116.9dBc/Hz	0.93V	368uW
1 0	1 1 1 1	0V	4.94GHz	-113.7dBc/Hz (spec not met)	0.6V	310uW
1 1	0 0 1 1	1.2V	4.89GHz	-116.8dBc/Hz	1.32V	512uW
1 1	0 0 1 1	0V	4.72GHz	-118.2dBc/Hz	1.22V	505uW
1 0	0 0 1 1	1.2V	4.91GHz	-119.6dBc/Hz	0.86V	329uW
1 0	0 0 1 1	0V	4.73GHz	-113.3dBc/Hz (spec not met)	0.56V	310uW

Table 6.3: TT corner simulation results at 80^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	1 1 0 1	1.2V	5.06GHz	-117dBc/Hz	1.22V	539uW
1 0	1 1 0 1	0V	4.89GHz	-118dBc/Hz	1.14V	542uW
0 1	1 1 0 1	1.2V	5.07GHz	-116.5dBc/Hz	1.06V	453uW
0 1	1 1 0 1	0V	4.9GHz	-117.6dBc/Hz	0.95V	446uW
1 0	1 0 0 1	1.2V	4.93GHz	-117.6dBc/Hz	1.2V	540uW
1 0	1 0 0 1	0V	4.77GHz	-118.5dBc/Hz	1.12V	542uW
0 1	1 0 0 1	1.2V	4.89GHz	-117dBc/Hz	1.04V	452uW
0 1	1 0 0 1	0V	4.79GHz	-118dBc/Hz	0.93V	445uW

Table 6.4: TT corner simulation results at 0^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	1 1 0 1	1.2V	5.07GHz	-116.8dBc/Hz	1.4V	538uW
1 0	1 1 0 1	0V	4.93GHz	-118dBc/Hz	1.33V	547uW
0 1	1 1 0 1	1.2V	5.08GHz	-116.7dBc/Hz	1.2V	455uW
0 1	1 1 0 1	0V	4.9GHz	-117.9dBc/Hz	1.15V	454uW
1 0	1 0 0 1	1.2V	4.94GHz	-117.4dBc/Hz	1.39V	540uW
1 0	1 0 0 1	0V	4.77GHz	-118.6dBc/Hz	1.32V	547uW
0 1	1 0 0 1	1.2V	4.89GHz	-117.2dBc/Hz	1.22V	546uW
0 1	1 0 0 1	0V	4.79GHz	-118.4dBc/Hz	1.14V	546uW

Table 6.5: FF corner simulation results at 80^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
0 1	1 0 1 0	1.2V	4.99GHz	-117.4dBc/Hz	1.48V	586uW
0 1	1 0 1 0	0V	4.83GHz	-119dBc/Hz	1.24V	611uW
0 0	1 0 1 0	1.2V	5GHz	-117.5dBc/Hz	1.2V	533uW
0 0	1 0 1 0	0V	4.85GHz	-118.5dBc/Hz	1.13V	541uW
0 1	0 0 0 1	1.2V	4.81GHz	-118.9dBc/Hz	1.29V	603uW
0 1	0 0 0 1	0V	4.66GHz	-119.7dBc/Hz	1.22V	613uW
0 0	0 0 0 1	1.2V	4.81GHz	-118.2dBc/Hz	1.18V	536uW
0 0	0 0 0 1	0V	4.67GHz	-119dBc/Hz	1.1V	542uW

Table 6.6: FF corner simulation results at 0^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
0 1	1 0 1 0	1.2V	5GHz	-117.4dBc/Hz	1.48V	586uW
0 1	1 0 1 0	0V	4.84GHz	-118.6dBc/Hz	1.41V	600uW
0 0	1 0 1 0	1.2V	5.01GHz	-117.2dBc/Hz	1.38V	530uW
0 0	1 0 1 0	0V	4.85GHz	-118.5dBc/Hz	1.32V	540uW
0 1	0 0 0 1	1.2V	4.81GHz	-118.9dBc/Hz	1.29V	603uW
0 1	0 0 0 1	0V	4.66GHz	-119.7dBc/Hz	1.22V	613uW
0 0	0 0 0 1	1.2V	4.81GHz	-118.2dBc/Hz	1.18V	536uW
0 0	0 0 0 1	0V	4.67GHz	-119dBc/Hz	1.1V	542uW

Table 6.7: FS corner simulation results at 80^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	0 0 1 1	1.2V	5.13GHz	-117dBc/Hz	1.28V	538uW
1 0	0 0 1 1	0V	4.95GHz	-118dBc/Hz	1.18V	544uW
0 1	0 0 1 1	1.2V	5.14GHz	-116.4dBc/Hz	1.12V	456uW
0 1	0 0 1 1	0V	4.96GHz	-117.5dBc/Hz	1V	453uW
1 0	0 0 0 1	1.2V	4.87GHz	-118dBc/Hz	1.22V	542uW
1 0	0 0 0 1	0V	4.72GHz	-118.9dBc/Hz	1.13V	545uW
0 1	0 0 0 1	1.2V	4.88GHz	-117.5dBc/Hz	1.05V	455uW
0 1	0 0 0 1	0V	4.73GHz	-118.4dBc/Hz	0.94V	449uW

Table 6.8: FS corner simulation results at 0^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	0 0 1 1	1.2V	5.14GHz	-116.7dBc/Hz	1.38V	535uW
1 0	0 0 1 1	0V	4.95GHz	-118.1dBc/Hz	1.18V	546uW
0 1	0 0 1 1	1.2V	5.15GHz	-116.5dBc/Hz	1.29V	456uW
0 1	0 0 1 1	0V	4.97GHz	-117.8dBc/Hz	1.2V	458uW
1 0	0 0 0 1	1.2V	4.88GHz	-117.9dBc/Hz	1.41V	530uW
1 0	0 0 0 1	0V	4.72GHz	-119.1dBc/Hz	1.34V	538uW
0 1	0 0 0 1	1.2V	4.89GHz	-117.7dBc/Hz	1.24V	446uW
0 1	0 0 0 1	0V	4.73GHz	-118.9dBc/Hz	1.15V	445uW

Table 6.9: SF corner simulation results at 80^oC

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	0 0 1 1	1.2V	5.12GHz	-116.7dBc/Hz	1.24V	533uW
1 0	0 0 1 1	0V	4.94GHz	-117.7dBc/Hz	1.14V	537uW
0 1	0 0 1 1	1.2V	5.14GHz	-116.2dBc/Hz	1.08V	450uW
0 1	0 0 1 1	0V	4.96GHz	-117.2dBc/Hz	0.96V	445uW
1 0	0 0 0 1	1.2V	4.87GHz	-117.7dBc/Hz	1.17V	537uW
1 0	0 0 0 1	0V	4.71GHz	-118.5dBc/Hz	1.08V	538uW
0 1	0 0 0 1	1.2V	4.88GHz	-117.2dBc/Hz	1.04V	447uW
0 1	0 0 0 1	0V	4.72GHz	-118dBc/Hz	0.9V	439uW

Table 6.10: SF corner simulation results at 0^{o}C

R1 R2	ct1 ct2 ct3 ct4	VCO i/p	output frequency	PN @2MHz	differential p-p amplitude	power
1 0	0 0 1 1	1.2V	5.13GHz	-116.3dBc/Hz	1.41V	533uW
1 0	0 0 1 1	0V	4.95GHz	-117.6dBc/Hz	1.33V	542uW
0 1	0 0 1 1	1.2V	5.15GHz	-116.2dBc/Hz	1.25V	450uW
0 1	0 0 1 1	0V	4.96GHz	-117.5dBc/Hz	1.16V	452uW
1 0	0 0 0 1	1.2V	4.87GHz	-117.4dBc/Hz	1.36V	539uW
1 0	0 0 0 1	0V	4.71GHz	-118.6dBc/Hz	1.29V	545uW
0 1	0 0 0 1	1.2V	4.89GHz	-117.3dBc/Hz	1.2V	452uW
0 1	0 0 0 1	0V	4.73GHz	-118.5dBc/Hz	1.11V	450uW

CHAPTER 7

CONCLUSION

A low power VCO was presented in this thesis. The VCO is required to tune from $4.8\,\mathrm{GHz}$ to $5\,\mathrm{GHz}$ across process corners and this is done by capacitor bank for coarse tuning and MOS varactor for fine tuning . The peak detector allows us to set the current across PVT. The VCO current consumption is around 550uA and LDO current consumption is 360uA. The total power consumtion including VCO LDO and peak detector is $1.2\,\mathrm{mA}$. The FoM(figure of merit) of the VCO is 189.5dB and FoMT is 195.5dB

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