Design of Low power Dividers for a Bluetooth Frequency Synthesizer

A Project Report

submitted by

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THESIS CERTIFICATE

This is to certify that the thesis titled Design of Low power Dividers for a Bluetooth Frequency Synthesizer, submitted by Dipti Ranjan Tripathy, to the Indian Institute of Technology Madras, for the award of the degree of Master of Technology, is a bonafide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Thank you, Almighty God for always being there for me,having a life in lifeless body overcoming Life threatening situations.

Finally, I would like to acknowledge my parents, and my brothers, very hopeful for me, ofcourse I will make them proud by serving for my nation by joining Indian Engineering Service in IRSSE(Indian Railway Service of Signal Engineers).

ABSTRACT

This paper presents a generic architecture for programmable multi-modulus dividers (MMD) for low-power and Bluetooth Frequency Synthesizer applications. The proposed architecture uses cascaded divide by 2/3 cells in a ripple fashion except for the last cell, which is a P/P+1 dual modulus prescaler used to adjust the minimum division ratio and the required division range. This approach provides an optimized architecture with minimum current consumption, the smallest area and minimum number of control bits for designing the MMD with a unit step increment. Also a 1:2 frequency divider is designed to generate quadrature carriers with optimised phase mismatch between in-phase and quadrature.

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ABBREVIATIONS

CLK	Clock
CML	Current Mode Logic
DFF	D Flip-Flop
ETSPC	Extended True Single Phase Clock
I/Q	In-phase Quadrature
MMD	Multi Modulus Divider
PLL	Phase-Locked Loop
TSPC	True Single Phase Clock
VCO	Voltage Controlled Oscillator

CHAPTER 1

INTRODUCTION

1.1 Motivation

Bluetooth standard frequency synthesizer is widely used now a days having challenge in optimum power with frquency coverage for all channels. Style of the frequency synthesizer can be an integer-N type with programmable integer frequency dividers or Fractional-N type synthesizer. However, for multi-standard applications, it is often difficult to cover multiple frequency bands using an integer frequency synthesizer whose step size is limited by the reference frequency. In order to achieve fine step size to cover the multi-band channel frequencies, one has to lower the reference frequency in an integer-N synthesizer design, which results in a high division ratio for the phase-locked loop(PLL) and thus high in-band phase noise. In contrast, fractional- N synthesizers allow the PLL to operate with a high reference frequency and also achieve fine step size by constantly swapping the loop division ratio between integer numbers, thus on an average dividing by a fractional number. A fractional-N synthesizer can include either a multi-modulus divider or dual modulus prescalers. Dual modulus prescalers are used in the current design. As the Bluetooth frequency range is narrow, overdesign of division range of the feedback divider is avoided to have minimum hardware in the design.

The aim of this project is to design a low power programmable divider with an input frequency from $4.804\,\mathrm{GHz}$ to $4.96\,\mathrm{GHz}$ and variable modulus of 240 to 248, also to design 1:2 divider to generate qudrature carriers from voltage controlled oscillator(VCO) output.

1.2 Organization of Thesis

Chapter 2 discusses architechture and working principle of programmable divider.

Chapter 3 has a detailed disscussion of implementation of programmable divider.

Chapter 4 discusses divider 1:2 for in-phase and quadrature generation.

Chapter 5 discusses about buffers used to interface with VCO.

Chapter 6 discusses layout of dividers and placement with VCO.

Chapter 7 shows simulation results.

Chapter 8 concludes the thesis.

CHAPTER 2

PROGRAMMABLE DIVIDER

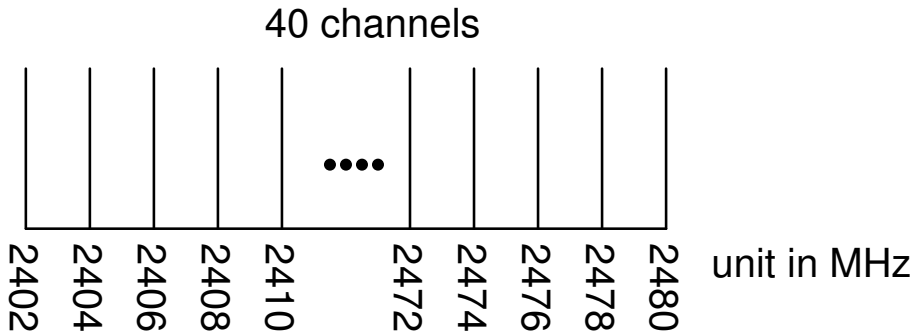

Figure 2.1: Bluetooth frequency range.

Bluetooth range is shown in figure 2.1. To accomodate all channels and to lock to the same reference frequency feedback divider in PLL should be programmable. Simultaneous control in tuning of VCO output frequency and programmable divider are needed to attain the particular channel frequency.

2.1 Programmable Divider Division Range

VCO frequency varies from $4.804\,\mathrm{GHz}$ to $4.96\,\mathrm{GHz}$,then division range 240-248 assuming $20\,\mathrm{MHz}$ reference frequency.

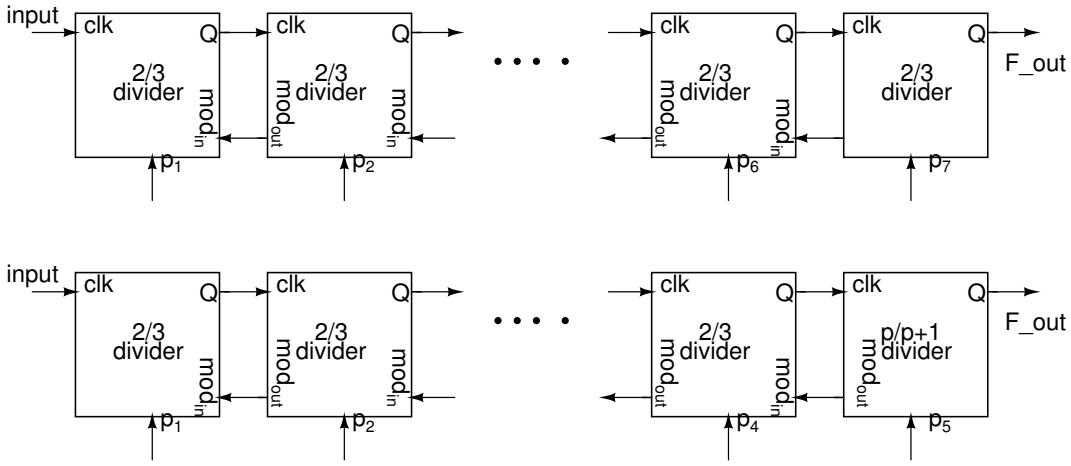

Figure 2.2: Programmable divider.

If we cascade 7 stages cascade of 2/3 dividers in a fashion as in figure 2.2, division ratio can be from 128 to 255 with 7 bit control but lower range is way too low than desired, which leads to overdesign of hardwares with more control bits.

Lower range can be varied by making last stage p/p+1 divider as in [1], where p is higher than 2.

Algorithm Of Division Range:

Lower range of division is given by $p * 2^{n-1}$, where p/p+1 is last stage divider. Range of division is given by 2^n. So according to required range of division, number stages n can be determined, then p is evaluated.

Table 2.1: Division range.

no of stages	last stage	min div	max div
7	2/3	128	255
5	14/15	224	255

As shown in table 2.1 setting p to 14 and number of stages n to 5, division range covers the required range.

2.2 Architechture Of Programmable Divider

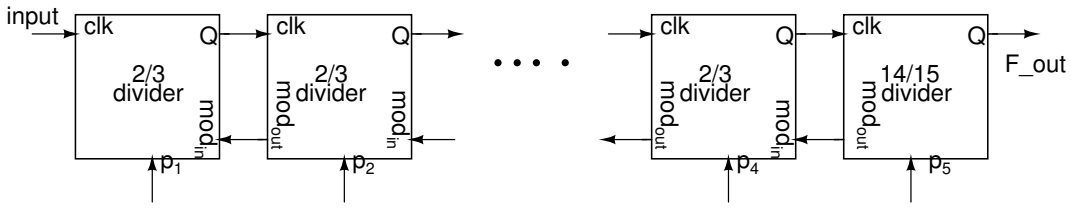

Figure 2.3: Programmable divider.

It consists of 2/3 divider cells connected like a ripple counter as shown in figure 2.3. Significant lower power dissipation is an advantage of this design. With this architecture, power optimization of each cell is easily achieved by downscaling the current as discussed in [2]. Its modular structure permits an existing design to be easily adapted for changes in input frequency or division range, simply by adding or removing cells from the chain. first three stages are true single phase clocked(TSPC) Flip-Flops because of its high speed and low power operation. TSPC FF can not operate at a low frequency below $100\,\mathrm{MHz}$ reliably because of dynamically hold nodes leaks to undesired level. Static dividers are used at low frequency in latter stages which also consume negligible power.

2.3 Working Principle of Programmable Divider

The operation principle is that, once in a division cycle, the mod signal for a given cell becomes high, so that the cell can divide by 3, depending on the state of its programming input. If the mod control state is 1, division by 3 occurs. If the state is a 0, the cell divides by 2 as usual. Division by 3 means that the period of its output signal is increased by one period of its input signal.

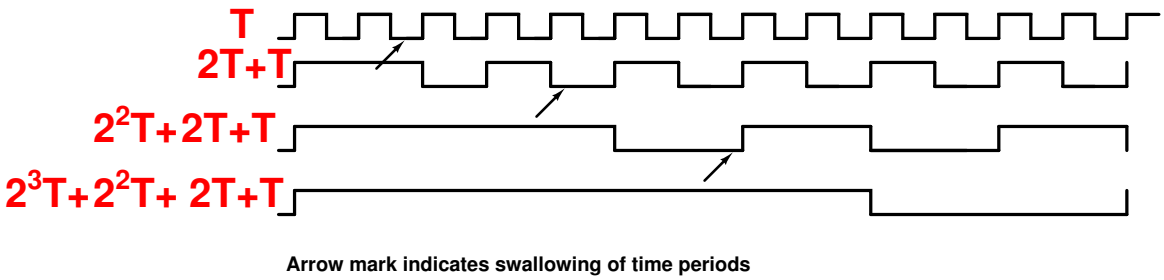

Figure 2.4: Timing diagram, source: M H perrott course material for highspeed dividers.

Figure 7.8 shows how cascade of 2/3 dividers provide division range swallowing extra cycles whcih successively happens in all cells in a ripple fashion. Here figure also shows timing diagram 4 cascade 2/3 cells assuming all control bits are high.

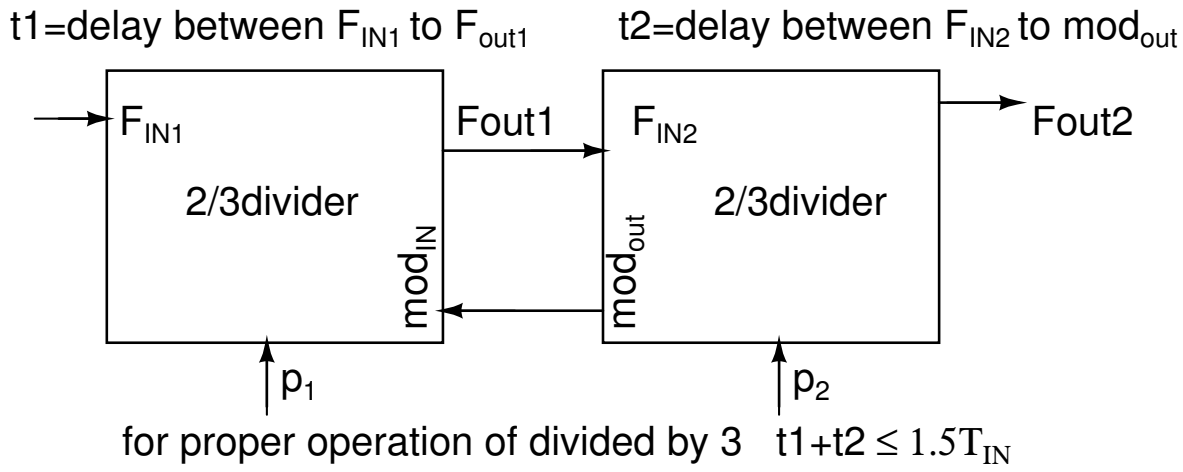

Figure 2.5: Cascaded 2/3 dividers.

For each cell delay between input signal and mod_{in} signal must be less than 1.5 times its input signal as shown in figure 2.5. As discussed in [3] the critical timing requirement here is whether every cell swallows one period of its input correctly when required inputs are active. Swallowing of one period should be in modular fashion which propagates along cells to ensure total accumulation of time periods at the output for correct division range.

CHAPTER 3

IMPLEMENTATION OF PROGRAMMABLE DIVIDER

3.1 TSPC Divider

3.1.1 TSPC Flip-Flop Fundamentals

Several topologies are available for frequency prescalers in the GHz range, including current-mode logic (CML), TSPC logic, and extended true single phase clocked (ET-SPC) logic. CML prescalers are analog logic cells that consume high power (up to tens of milliwatts) and provide the highest speed among known topologies. Because of their high power consumption, the CML prescalers are used only for high frequencies where other topologies cannot operate. TSPC dividers are well known for their low power consumption comparing to the CML implementation, but their application is limited to relatively low frequencies. With the development of CMOS technologies, the improvement of the intrinsic speed of a device makes it possible for the TSPC logic gates to replace CML even in high-frequency ($10\,\mathrm{GHz}$) applications TSPC prescalers consume the lowest power, typically on the order of several hundred microwatts, but suffer from low operating speed. ETSPC prescalers use dynamic logic similar with that in TSPC cells but have one less transistor in each branch, improving the maximum operating speed at the cost of constant direct current.

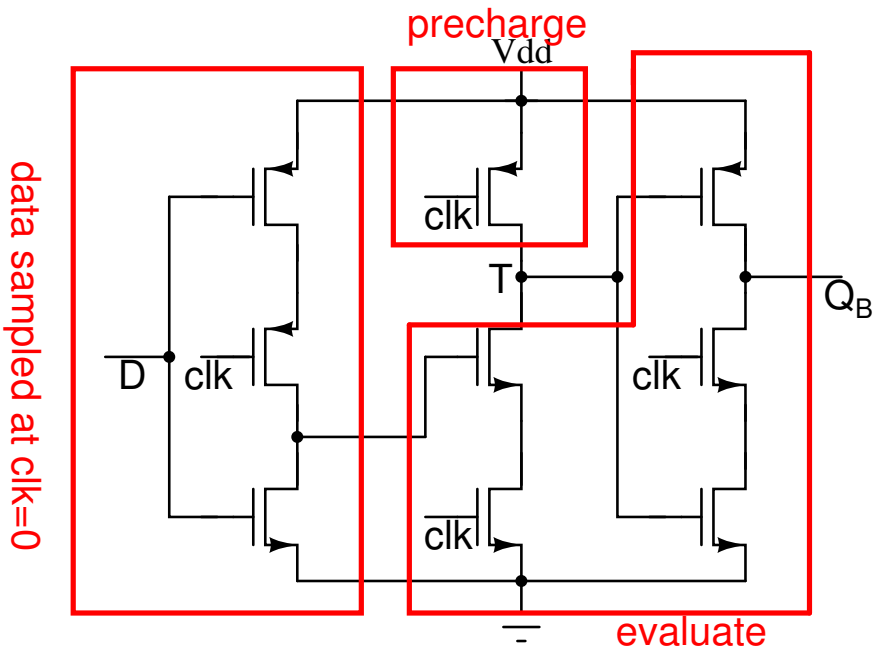

Figure 3.1: TSPC Flip-Flop.

Inverted data Q_B is sampled at positive edge of clock.

Power dissipation is given by

$$P_d = f * C_{eff} * V_{dd}^2 \tag{3.1}$$

where $C_{eff} = \sum_{i=1}^{n} \alpha_i * K_i * C_i$,

α_i is switching probability at node i,

K_i is swing range coeficient at node i,

C_i is capacitance at node i,

which is discussed in detail in [4].

The first branch samples input data during a negative cycle of a clock signal and holds the data during a positive cycle, the second branch precharges a node T during the negative clock cycle and evaluates the data during the positive cycle, and the third one passes the evaluated data during the positive cycle and holds the output during the negative cycle. Therefore, the evaluation result in the second branch decides the output of the flip-flop(FF). When the input is high, the charge on the node T holds, and output Q_B goes low immediately after the clock rises high. On the other hand, when the input is low, the node T has to be discharged before Q_B goes high, which inherently limits

the speed of TSPC FF operation. Optimum sizing can be done with respect to power, delay or frequency of concern as given in [5].

3.1.2 TSPC FF Operation

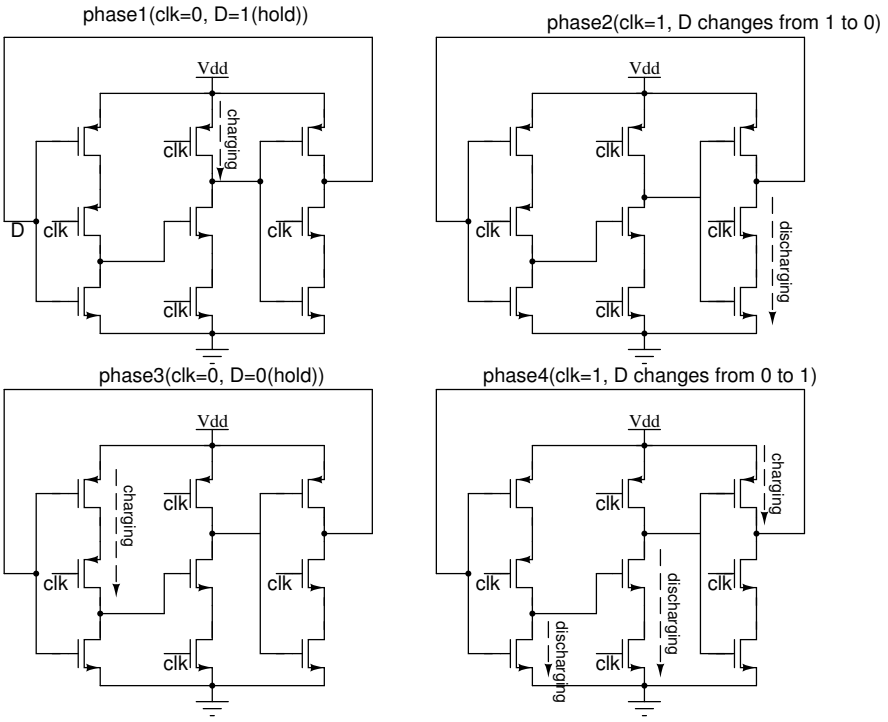

Figure 3.2: TSPC Operation.

As given in [6] all timing phases are shown as shown in figure 3.2. Phase 1 and phase 3 consist of charging of particular nodes with no output toggling.Phase2 consists of discharging of node D with resulting output toggling. phase 4 is the worst case limiting high frequency operation. max frequency is given by

$$F_{in} \leq \frac{1}{2 * t_{phase4}} \tag{3.2}$$

3.1.3 TSPC 2/3 Divider

Initial Design

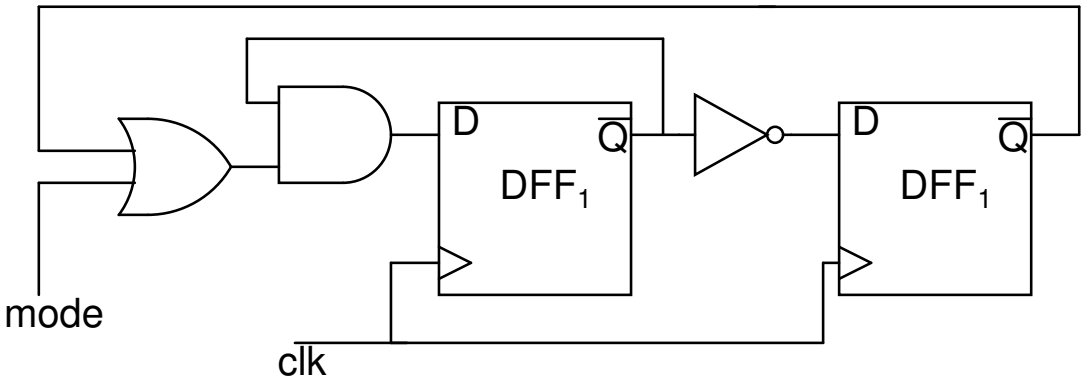

Figure 3.3: TSPC 2/3 divider.

Dual-modulus prescalers can be synthesized by using more than one TSPC Flip-Flops(FFs) and additional feedback logic gates. A general diagram of the proposed prescaler is shown in figure 3.3 wherein the D flip-flops(DFFs) can be any type. The two operation modes are switched by the external control signal mode. When mode is high, the feedback signal from is blocked and the prescaler operates in the same way as a divide-by-2 divider. When mode is low, the prescaler operates in the divide-by-3 mode. An advantage of this implementation is that the feedback logic gates can be absorbed by the first stage of first DFF.

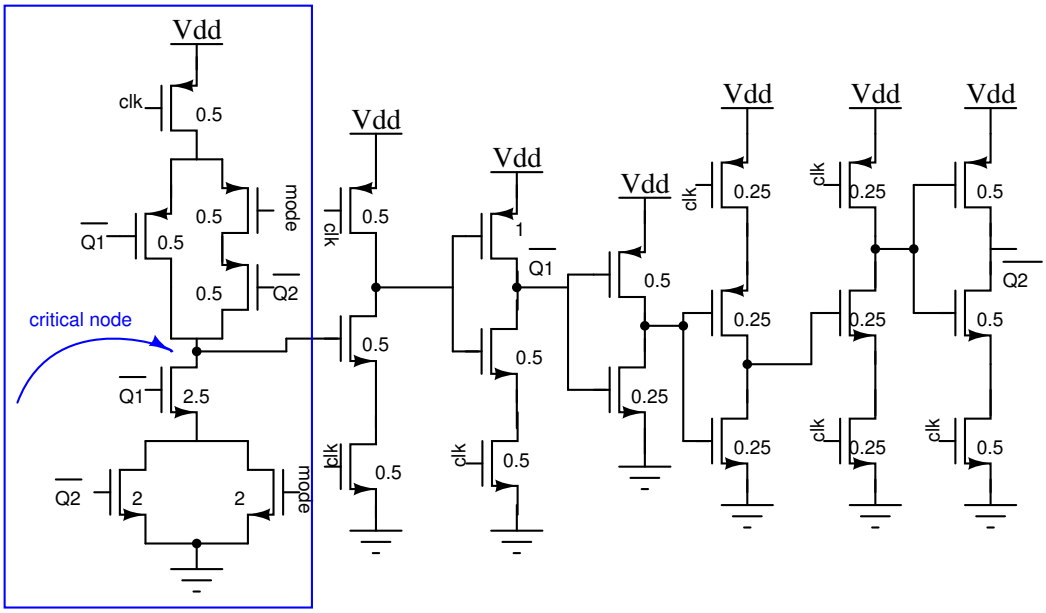

Figure 3.4: TSPC 2/3 divider.

Note: Numbers written beside transistors everywhere are widths in μm,the length of all transistors are the same which is $60\,\mathrm{n}m$.

Here one drawback is the critical node as shown in figure 3.4, transistors need to be sized larger for charging and discharging of the node resulting in higher dynamic power consumption.

Improved Design

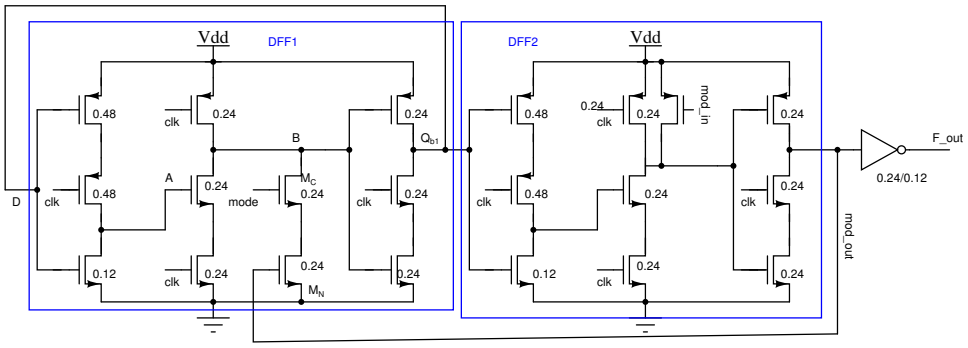

Figure 3.5: TSPC 2/3 divider

To get division ratio of 3, two DFFs need to be cascaded with some logic. Due to incorporation of logic gates between two D flip-flops (DFFs), speed of dual-modulus prescalers is usually much slower than that of a 1:2 divider consisting of a TSPC DFF. In a divide-by-2 mode, it is almost identical to a single TSPC DFF, except for small extra parasitic capacitance added to the node B. hence, the maximum operating speed is close to that of the single TSPC DFF.

As shown in figure 3.5 in the divide-by-3 mode, since the output of DFF2 skips the first branch of the DFF1 and forces the node B to low directly, the delay of the added path can be extended to one and half clock cycles as given in [7]. Therefore, driving the output to high is no longer a critical path, which is in contrast with th single-TSPC DFF, and the operating speed in this mode can be even faster than that of the divide-by-2 mode. Here if the positions of M_N and M_c are switched, the operating speed of the divide by-3 mode can be further improved with the penalty of reducing the divide-by-2 speed. Slower speed in divided by-2 mode is due to higher capacitance contribution by M_N to node B. Higher speed in divided by-3 mode is due to better switching of M_N to pull down the node B to ground level. Therefore, it is possible to create a standalone high-speed divide-by-3 prescaler by removing M_c.

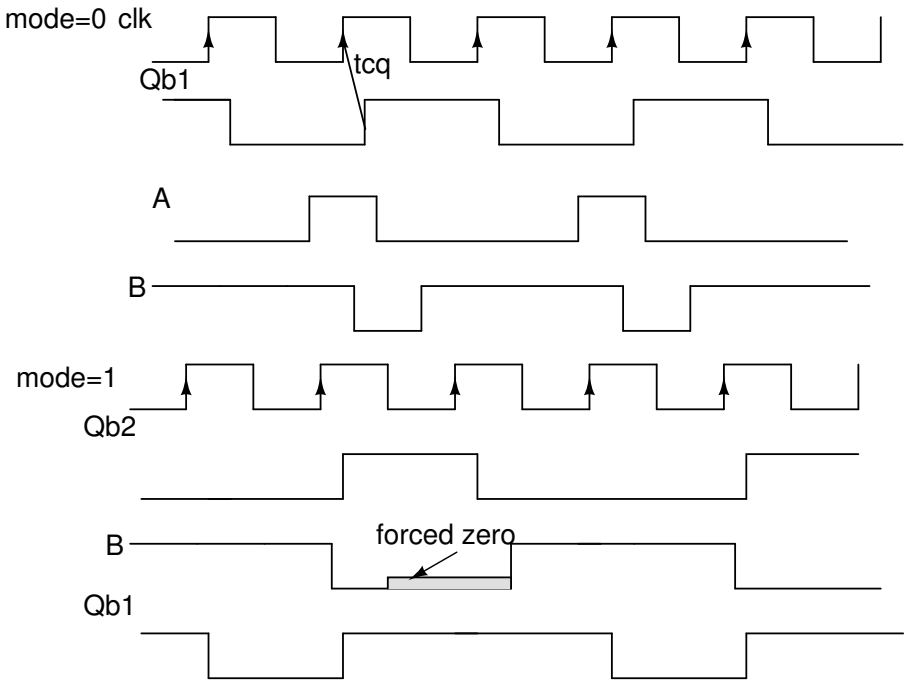

Figure 3.6: TSPC 2/3 timing diagram.

As shown in figure 3.6 node B is forced to zero one more cycle. As a result output logic high is extended one more cycle to get divide by 3 operation.

3.1.4 ETSPC Divider

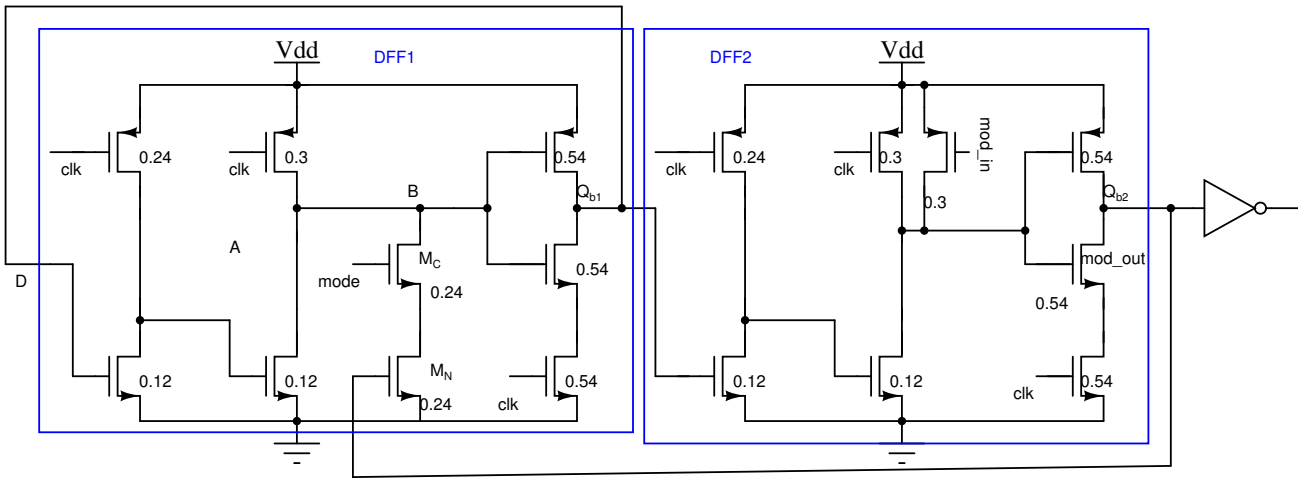

Figure 3.7: ETSPC 2/3 divider.

As given in [8], [9] ETSPC logic can be used for high frequency prescaler and MMD design. In ETSPC extra transistors removed in the branches of TSPC to lower the capacitance at the nodes as shown in figure 3.7, but still retaining function with a ratioed logic style. Sizing of transistors should be proper to mantain well defined logic

levels at nodes. Due to high frequency of operation it is initially prefered for first stage of programmable divider, but it has two drawbacks as given below.

1. Design is narrow band.

2. There is static power consumption.

Later it is observed that with low V_t transistors TSPC divider itself can operate well in desired high frequency with optimum power dissipation, so TSPC divider is retained in the first stage of programmable divider but with higher sizing for reliable operation as shown below in figure 3.8.

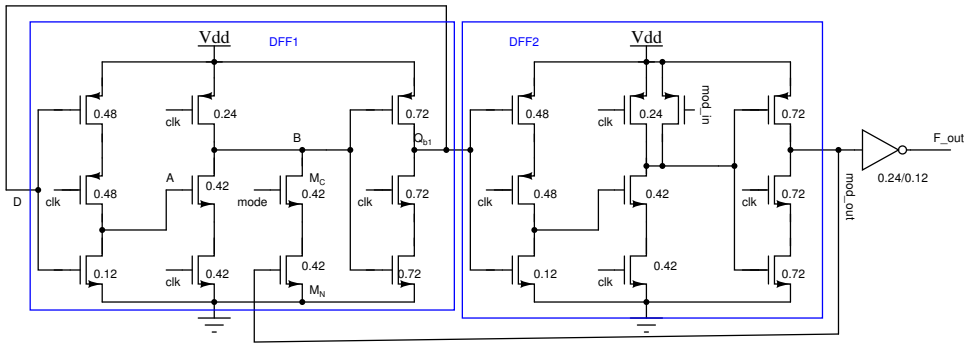

Figure 3.8: TSPC 2/3 divider for first stage.

3.1.5 Failure of TSPC FF at Low Frequencies Below 500 MHz

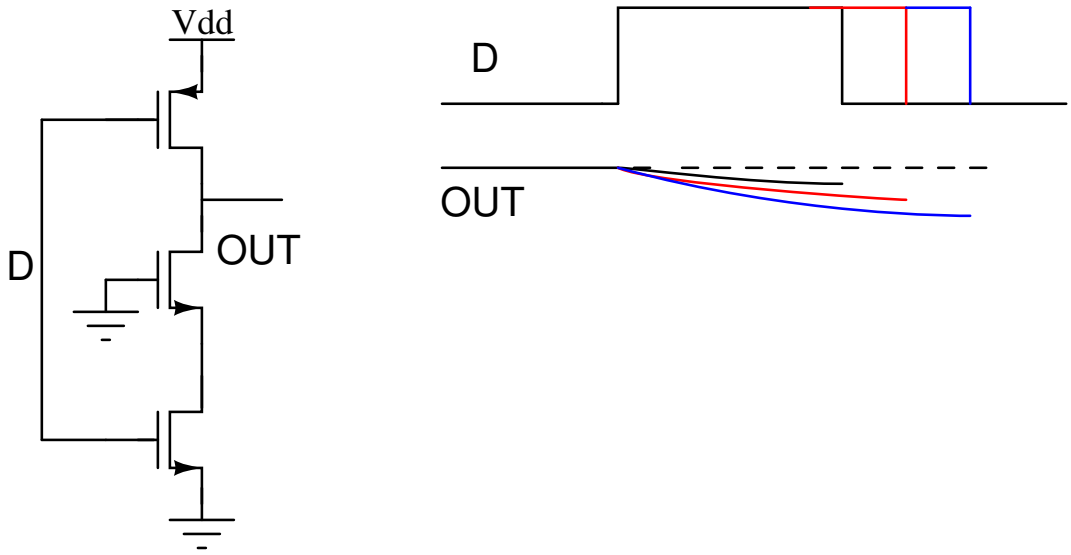

Figure 3.9: TSPC FF failure at low frequencies (MHz range).

As shown in figure 3.9 even if input D to nMOS is zero, there is a discharging current

through nMOS stack which reduces the logic high level. As frequency decreases node OUT goes to undefined logic level, so TSPC FF operation fails.

3.2 Low Frequency Divider

3.2.1 Design of Low Frequency Latch

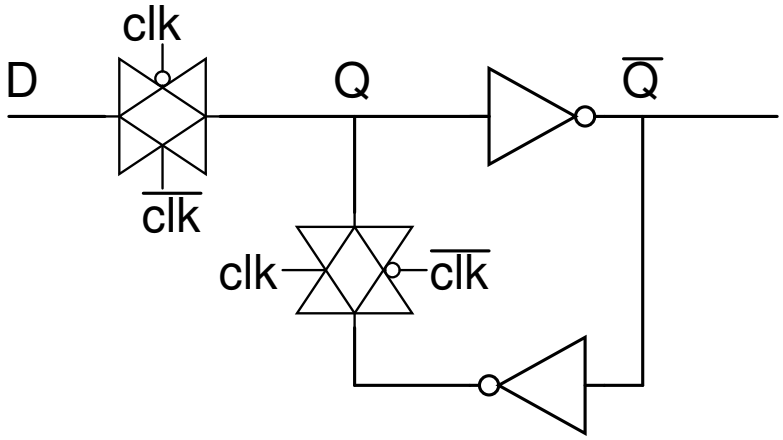

Figure 3.10: Static latch conventional.

The robust conventional flipflop as shown in figure 3.10 consists of 16 transistor structure.It can not operate reliably at frequencies above $100\,\mathrm{MHz}$ with optimised power consumption. The problem at high frequency is due to higher pMOS capacitance, higher power consumption is due to higher clock load and static keeper.

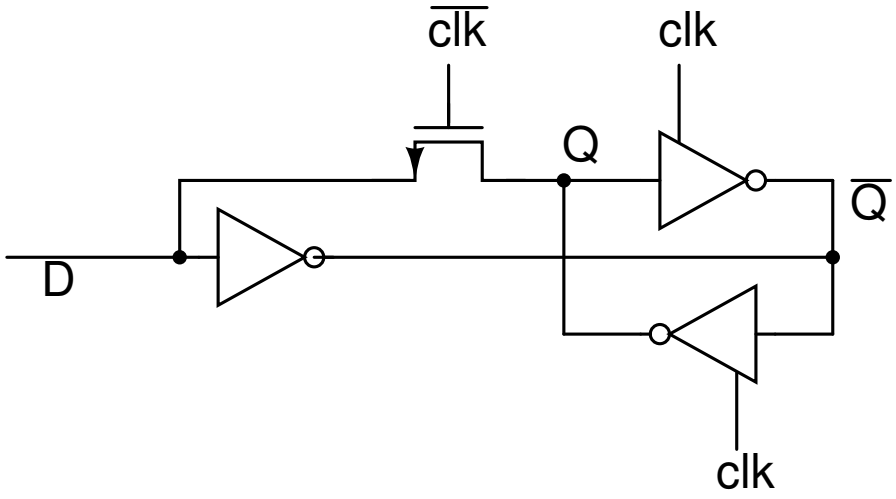

Figure 3.11: Latch.

To lower clock power consumption, the flip-flop uses only nMOS clocked transistors as shown in figure 3.11. The gate of nMOS transistors effectively has less capacitance than a pMOS, yielding faster switching and lower power for the clock circuitry. The latch circuitry is created by two cross-coupled TSPC inverter with clock control through gate of nMOS. Keeper is active only one half cycle, so has very low power consumption.

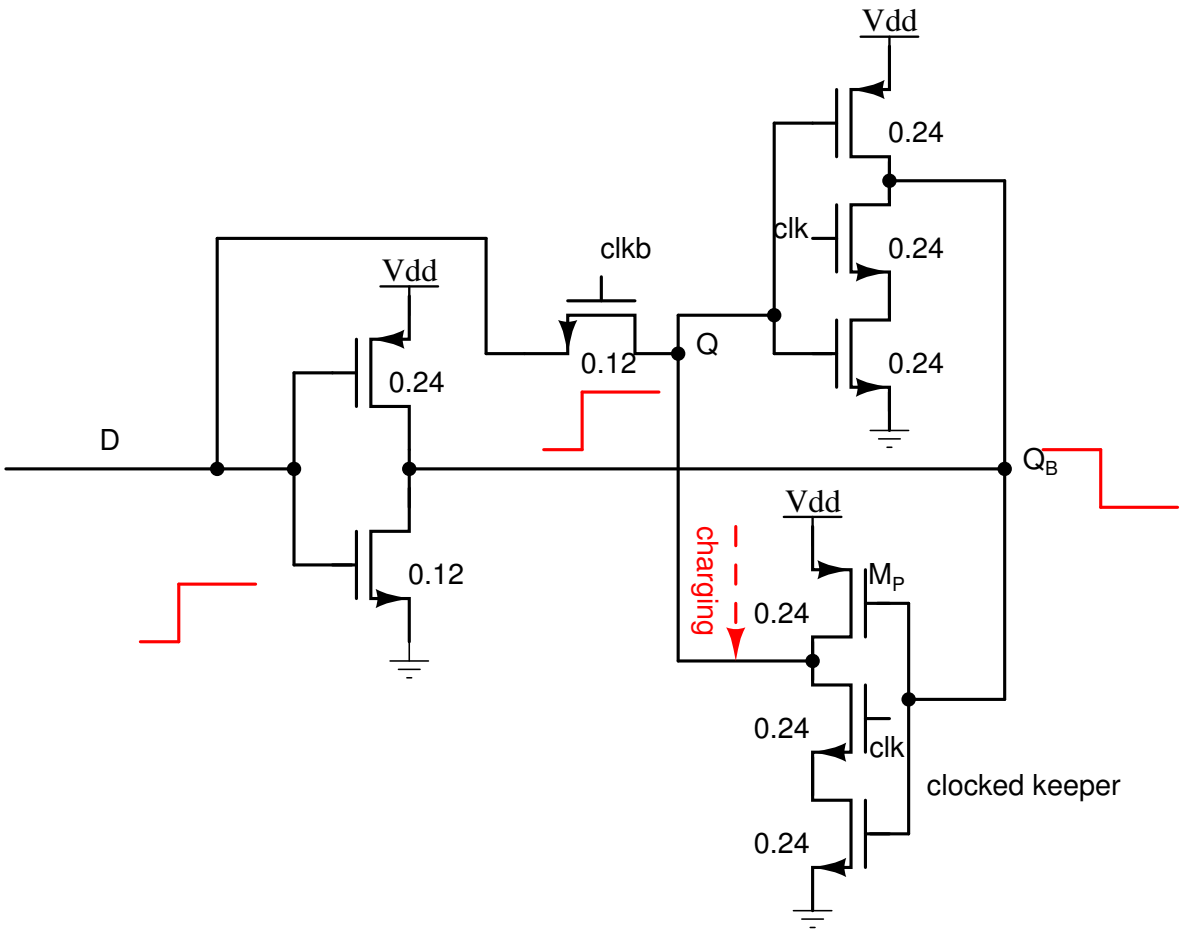

Figure 3.12: Operation of the latch.

Threshold drop due to nMOS pass transistor is managed as shown in figure 3.12. If input D is high, Q_B can go low easily, then node Q can be pulled up through M_P of clocked keeper.

3.2.2 Low Frequency FF

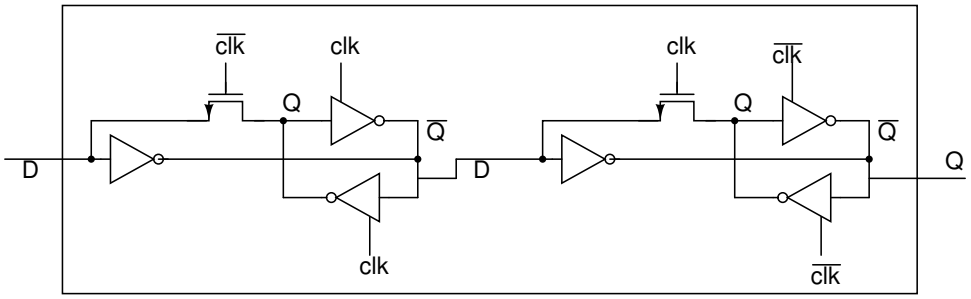

Figure 3.13: Flip-Flop.

This is cascade of negative latch and positive latch, so a positive edge triggered flipflop is designed. As discussed in [10] this FF does not operate for the following condition $V_t > V_{dd} - V_t$. To obtain operation at extremely low voltages, low-threshold pass transistors must be used. The resulting FF has very low power consumption, while having a small clock load and a very small data load.

3.3 2/3 Divider

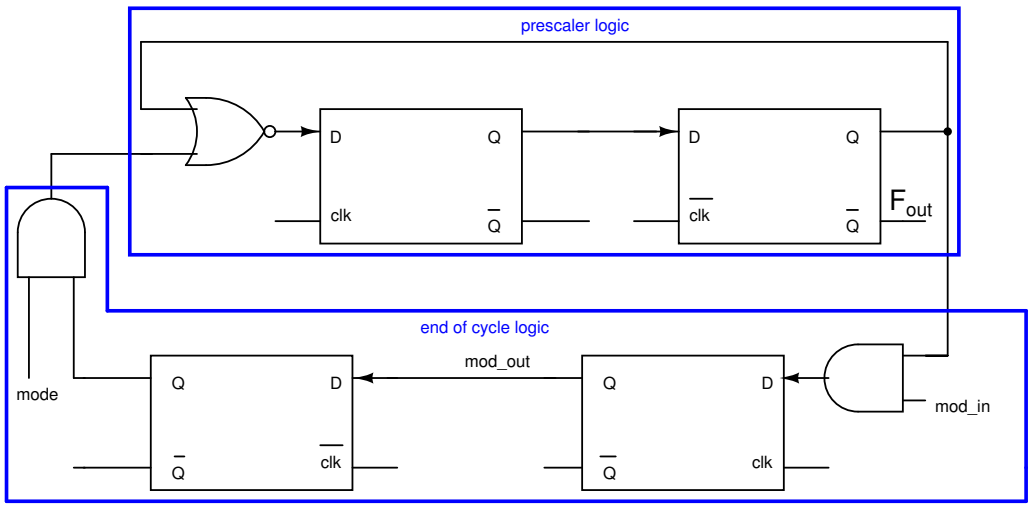

Figure 3.14: 2/3 divider.

This is most popular prescaler and end of cycle logic as given in [2]. This 2/3 divider cell comprises two functional blocks, as depicted in 3.14. The prescaler logic block divides upon control input signal by the end-of-cycle logic. The end-of-cycle logic determines the instaneous division ratio of the cell. When mod_{in} signal becomes active once in a division cycle, the state of the mode is checked, and if mode= 1, the end-of-cycle logic forces the prescaler to swallow one extra period of the input signal. In

other words, the cell divides by 3. If mode = 0, the cell stays in division by 2 mode.Also divider always reclocks the mod_{in} signal and outputs to the previous stage.

3.4 14/15 Divider

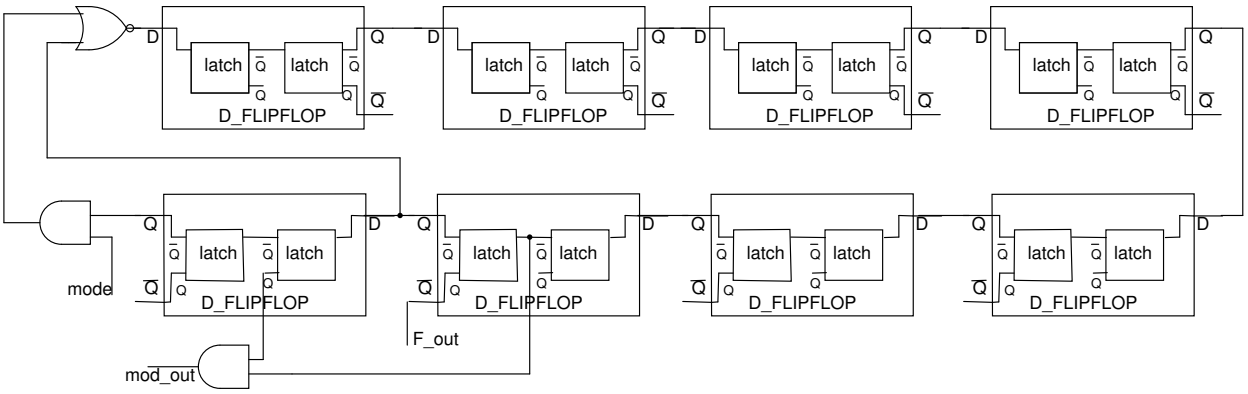

Figure 3.15: 14/15 divider.

p/p+1 divider design is done by cascading flip-flops in Johnson counter fashion in which inverted output of last stage is fed to first stage as shown in figure 3.15. As given in [1] if p is even structure is simple with $\frac{p}{2} + 1$ no of FFs.mod_{out} signal is generated considering two things as given below.

- It should be of same frequency as of output signal.
- It must be of less than 50% dutycycle so after reclocking from the previous stage new mod signal should be active once in a division cycle.

It is cascaded at last stage of programmable divider to control the lower range of division.

It is a synchronous block, so there is no jitter accumulation as in previous cascaded 2/3 cells.

CHAPTER 4

DIVIDER 1:2 FOR GENERATION OF QUADRATURE CARRIERS

If frequency of operation of VCO and following stage is same, there can be interaction through supply pulling resulting phase noise degradation. So VCO can be designed twice higher frequency which can delivered to next stage through a divider.

4.1 Architechture Of I/Q Divider

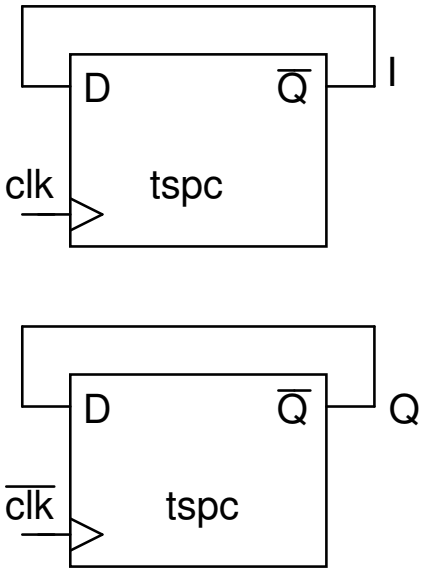

Figure 4.1: IQ generation using TSPC.

In highspeed master-slave dividers, it is common practice to design the slave as the dual of the master so that they can be both driven by a single clock. However, duality requires one of the latches to incorporate pMOS devices in the signal path, hence lowering the maximum speed. For IQ generation from TSPC FF two independent Flipflops can be used for the purpose as shown in figure 4.1, as clock(CLK) and inverted CLK are available from VCO. TSPC FlipFlop is already designed for high frequency operation,

which is tested for I/Q generation but initial phase can create I/Q phase mismatch, so it is not a robust structure. Topologies in which both CLK, inverse CLK can be coupled as in [11], [12],[13],[14] are tried, in which phase mismatch can be eliminated.

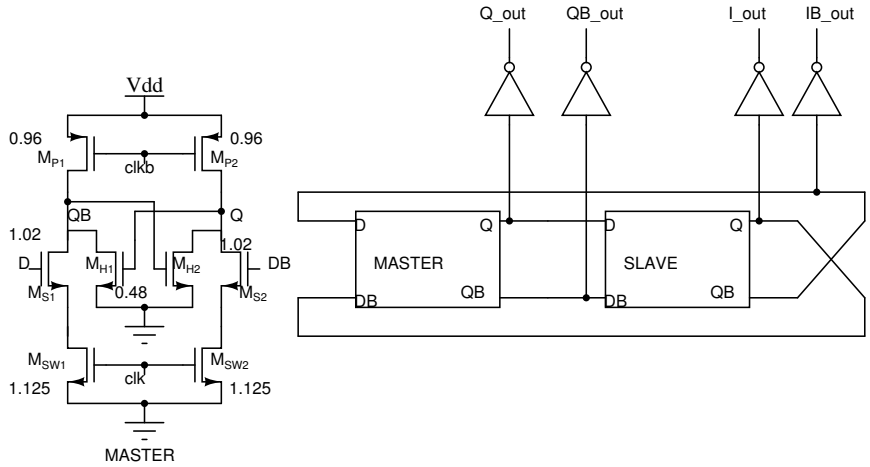

Figure 4.2: I/Q divider.

This is modification of divider given in [11] by divider given in [12], which provides 50% duty cycle with very high frequency of operation and low power consumtion.

The 1/2 frequency divider employs two D-latches in a master-slave configuration with negative feedback. As shown in figure 4.2, the divider utilizes two identical D-latches that are driven by complementary clocks CLK and CLKb. Each latch consists of two sense devices M_{S1}, M_{S2}, a regenerative loop having hold devices M_{H1}, M_{H2}, nMOS switching transistors M_{SW1}, M_{SW2} and two pull-up devicesM_{P1}, M_{P2}. The higher speed of the divider is due to fewer stages in the critical signal path.

4.2 I/Q Divider Operation Principle

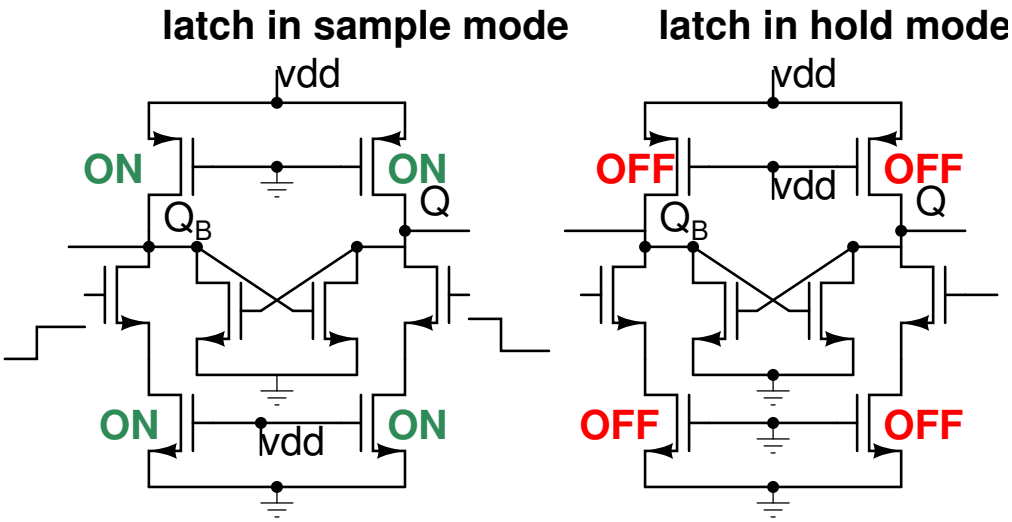

Figure 4.3: I/Q divider operation.

Load resistor in dividers play important role in both fast and correct operation, it can simply be a resistor or from active devices. Small load is required to make the RC time constant smaller for fast operation where as large load is needed for better swing at the outputs.

As shown in figure 4.3 the impedances of the pMOS devices are low in the flipping mode and high in the latched mode, which makes the time constant small and the driving signal large when required.

In holding mode both sampling and switching nMOS transistors are off. As pMOS input is swinging up, that charges one of the output node through C_{gd}, other node goes down through regenerative loop action.

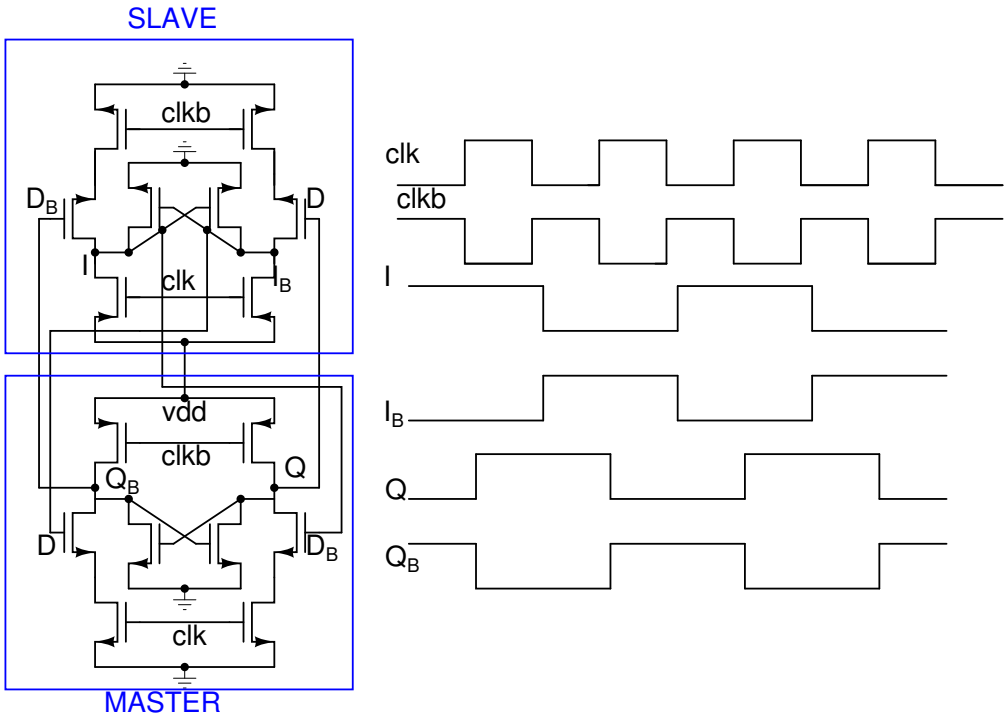

Figure 4.4: I/Q divider timing diagram.

Outputs of MASTER block are Q and Q_B, that of SLAVE are I and I_B. As master is sampling data when CLK is high, Q and Q_B change at positve edge of CLK whereas I and I_B change every negative edge of CLK. Outputs I and Q can be seen clearly in figure 4.4 which is $90°$out of phase, i.e, in-phase and quadrature.

CHAPTER 5

PREAMPLIFIER

Need for preamplifier:

Two reasons to use preamplifier are given below. 1. Divider for I/Q functions correctly if input swing is rail to rail.

2. There is isolation of VCO from divider.

5.1 Preamplifier or Buffer

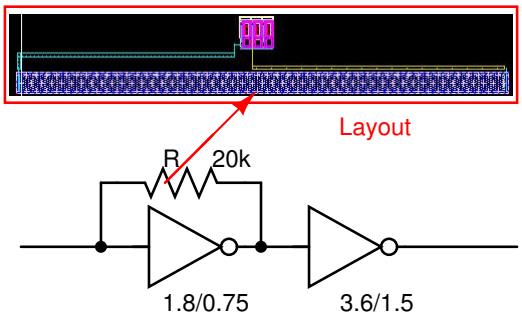

Figure 5.1: Preamplifier.

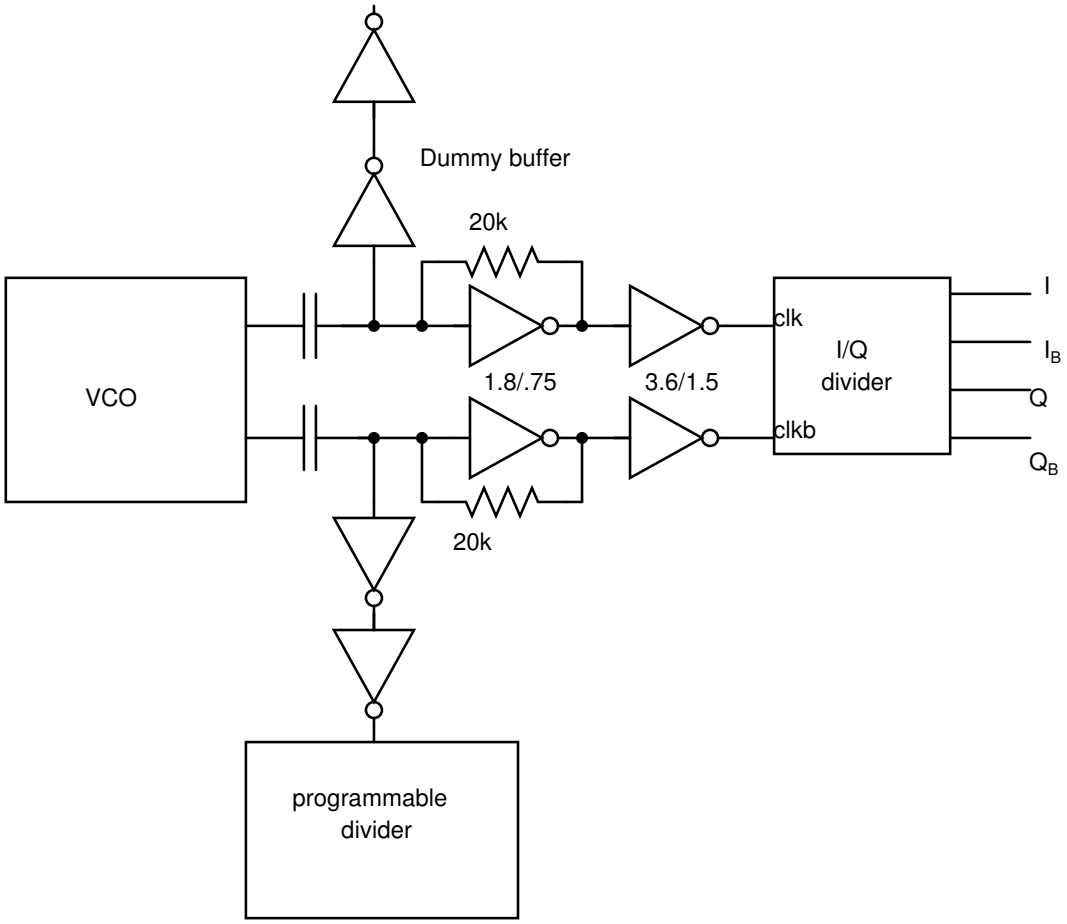

Figure 5.2: VCO,preamplifier and divider.

As shown in figure 5.1 20k feedback resistor used in the first stage of buffer takes considerable space in layout. As shown in figure 5.2 only two resistors are used for setting common mode of input to buffer. Three buffers are needed for the purpose as programmable divider input is single ended, but one dummy buffer is used to ensure symmetrical loading to VCO.

CHAPTER 6

LAYOUT OF DIVDERS

6.1 Layout Of The Programmable Divider

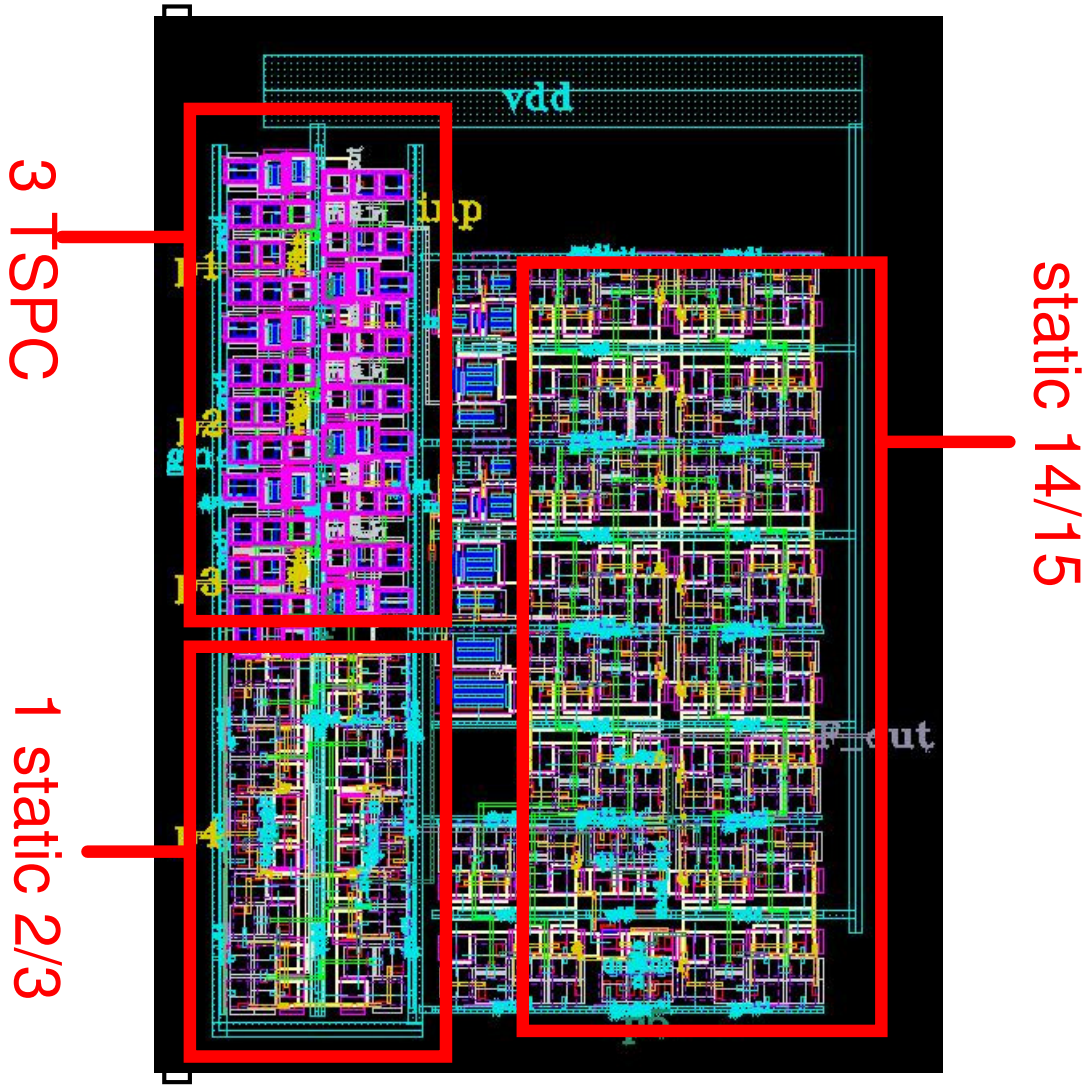

Figure 6.1: Programmable divider layout.

Layout size is $18\,\mu m$x$27.5\,\mu m$.Layout is easier as local signal wiring among 2/3 cells and same dividers are reused in design in some cases.

6.2 Layout Of The I/Q Divider

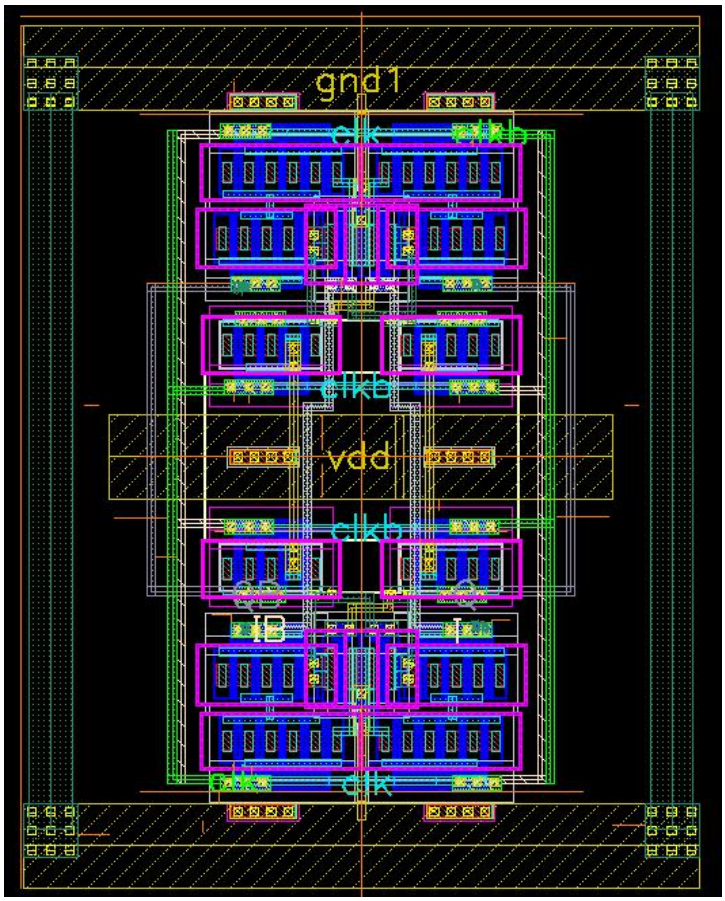

Figure 6.2: I/Q divider layout.

Layout size is $8\,\mu m$x$10.3\,\mu m$ symmetry in wiring capacitances are very critical to maintain for low power low capacitance designs. Because very small capaciatance difference can lead to phase mismatch issues.

6.3 Placement with VCO

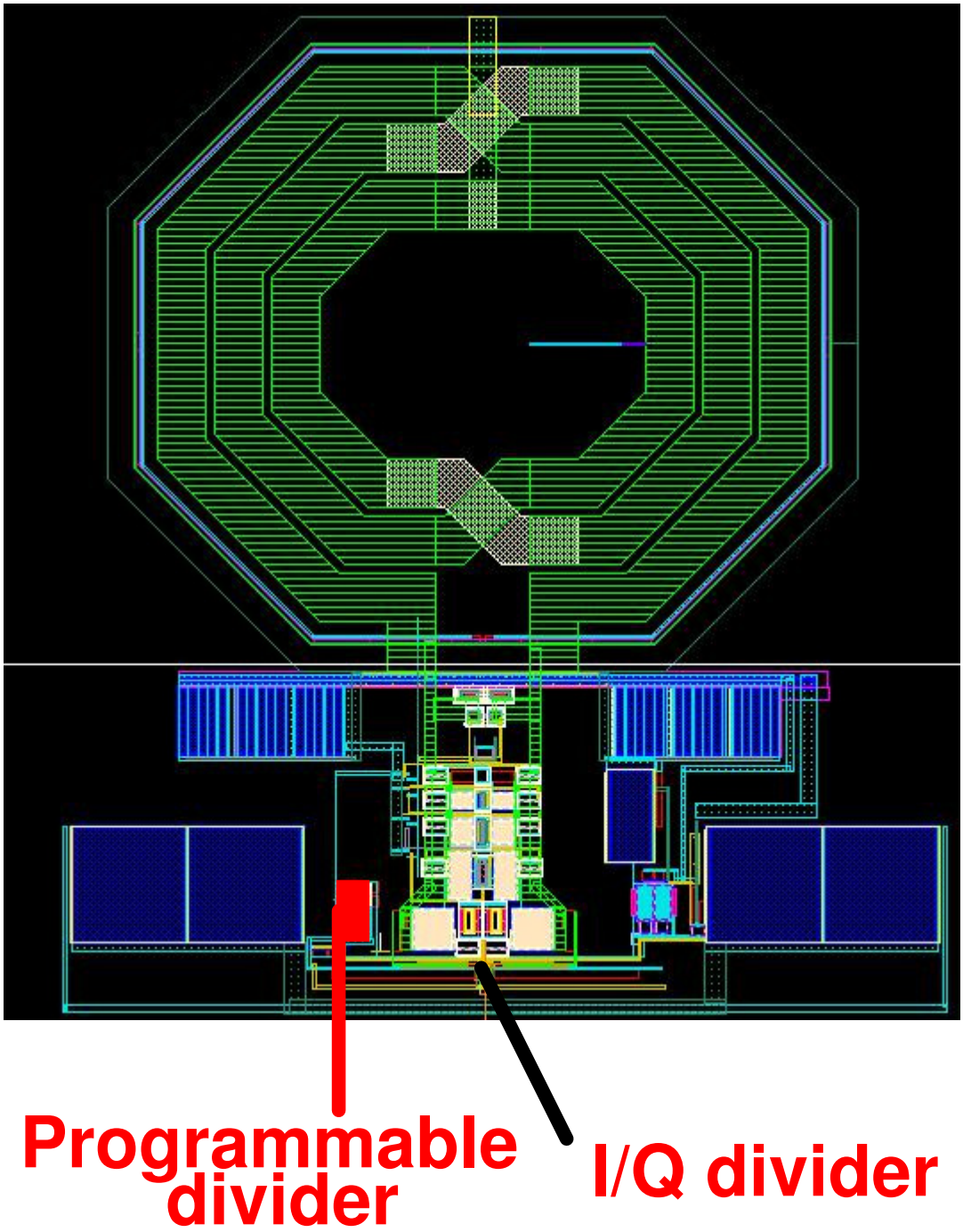

Figure 6.3: Placement of VCO with dividers.

I/Q divider was placed symmetrically to avoid phase error in I and Q signals.

CHAPTER 7

SIMULATON RESULTS

7.1 Simulation Results of Programmable Divider

7.1.1 Division Ratio Range

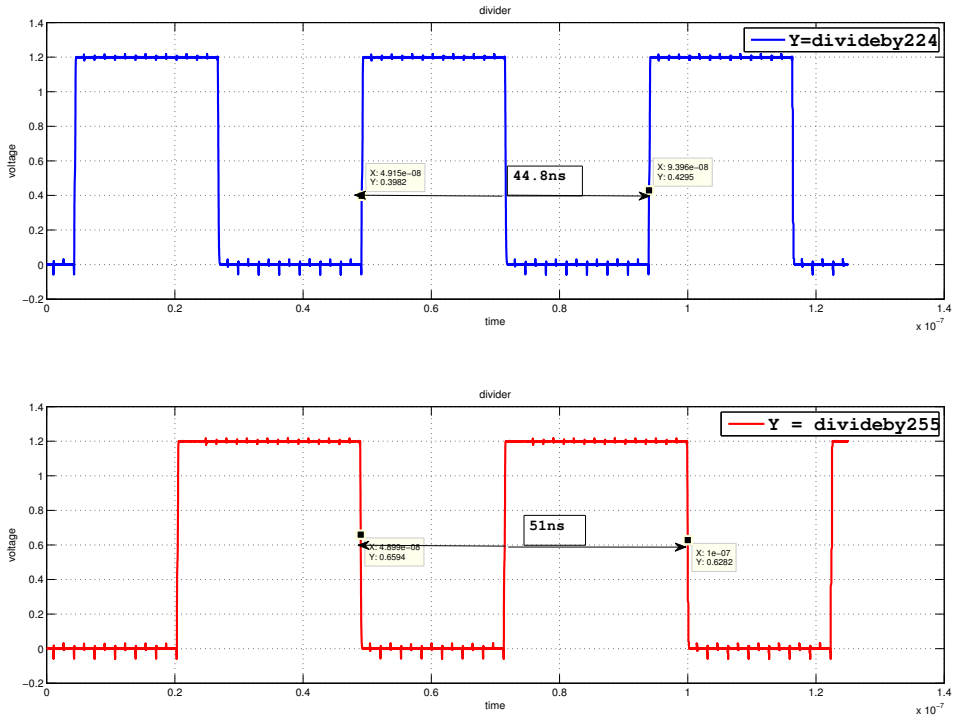

Figure 7.1: Division range

Minimum division ratio 224 and maximum division ratio of 255 are simulated.

7.1.2 Internal Output Signals of Each 2/3 Cell

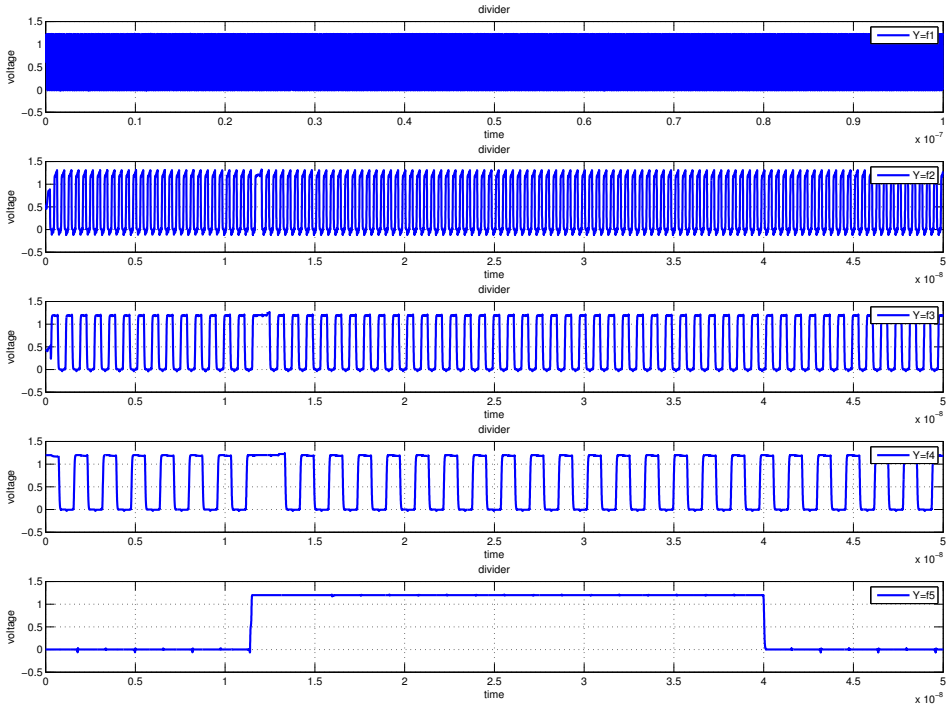

Figure 7.2: Output signals of each stage.

This simulation shows how time periods are swallowed in each cell in modular fashion.

7.1.3 Internal Mod Signals into Each 2/3 Cell

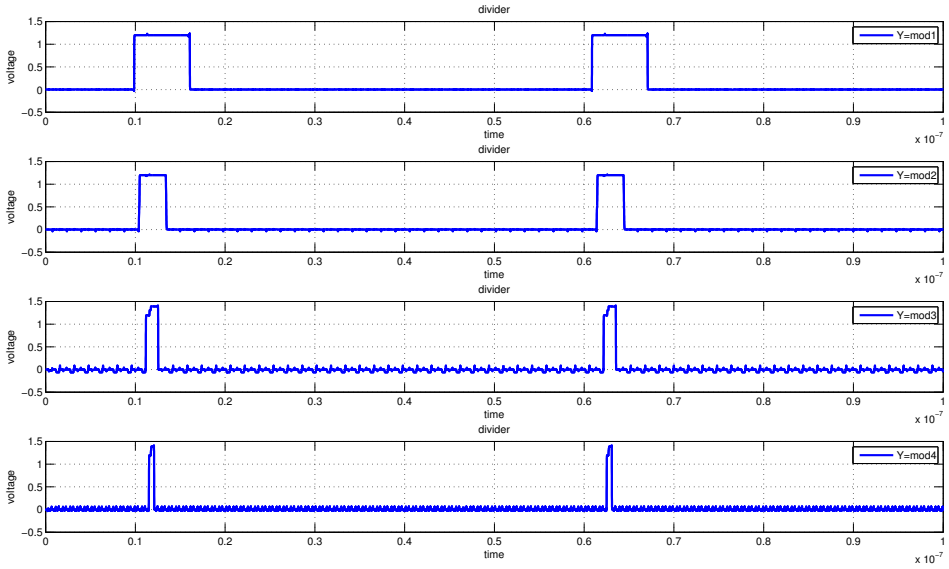

Figure 7.3: Mod out signals of each stage.

This simulation gives understanding of triggering time of each cell of 2/3 divider to accumulate one time period of its input. Each mod signal are of same frequency same as output ,which is high only once in full output cycle.

7.1.4 Noise Floor of Last Stage of Programmable Divider

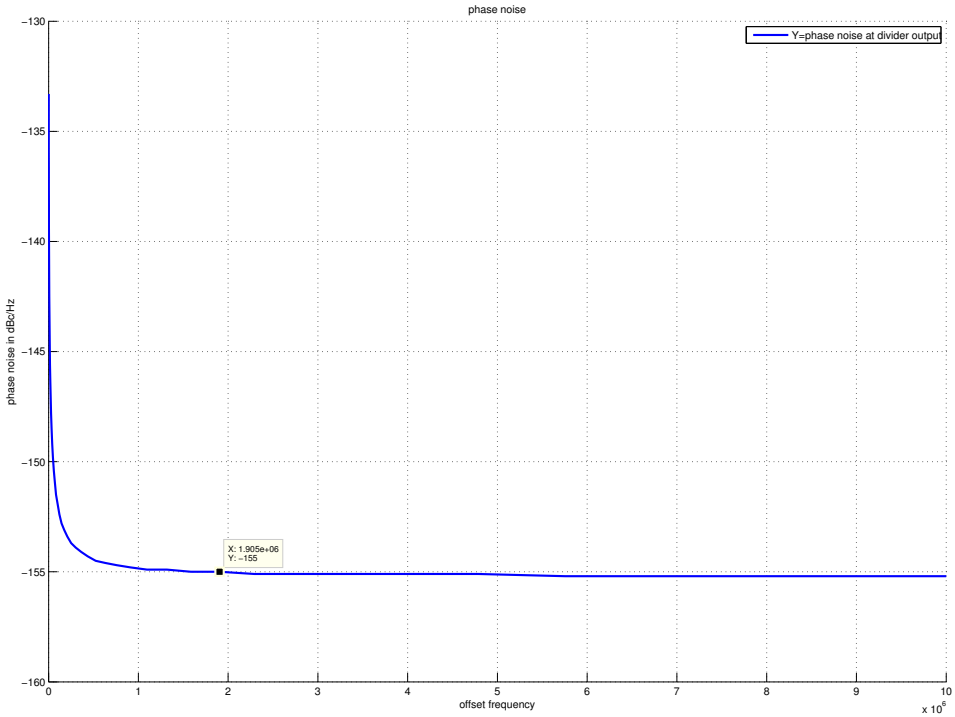

Figure 7.4: Noise floor of 14/15 stage.

Noise Floor of Last stage 14/15 divider was $-155\,\mathrm{dBc/Hz}$ at $2\,\mathrm{MHz}$ offset with output at $20\,\mathrm{MHz}$. It inherently limits the minimum phase noise at the output.

7.2 Simulation Results Of I/Q Divider

7.2.1 Phase Difference Between I and Q

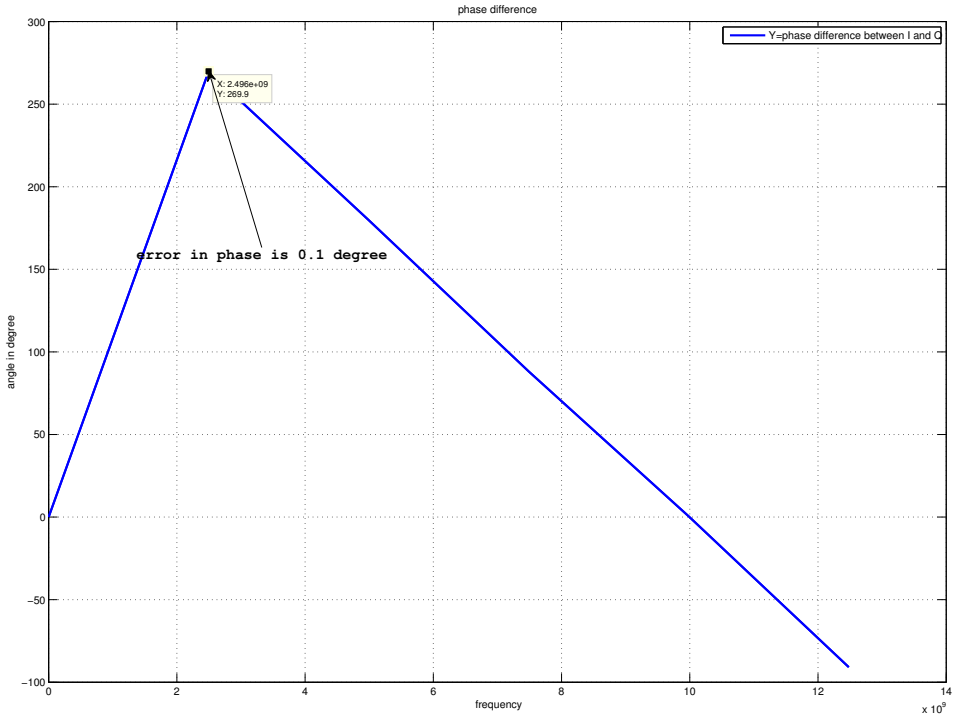

Figure 7.5: Phase error in difference between I and Q.

Error in phase is $.1°$ as ideally phase difference between I and Q should be $90°$

7.2.2 Phase Noise at the Output of Divider

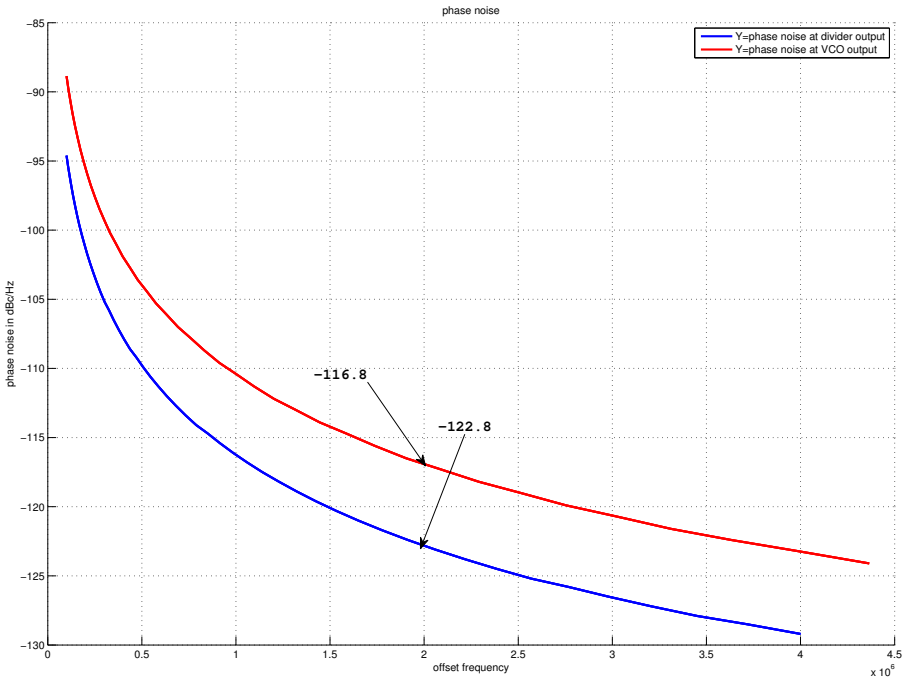

Figure 7.6: Phase noise of VCO and I/Q divider.

Phase noise at the output of divider is $-122.8\,\mathrm{dBc/Hz}$ which shows $6\,\mathrm{dB}$ improvement over VCO output.

7.2.3 Montecarlo Simulation of Phase Error

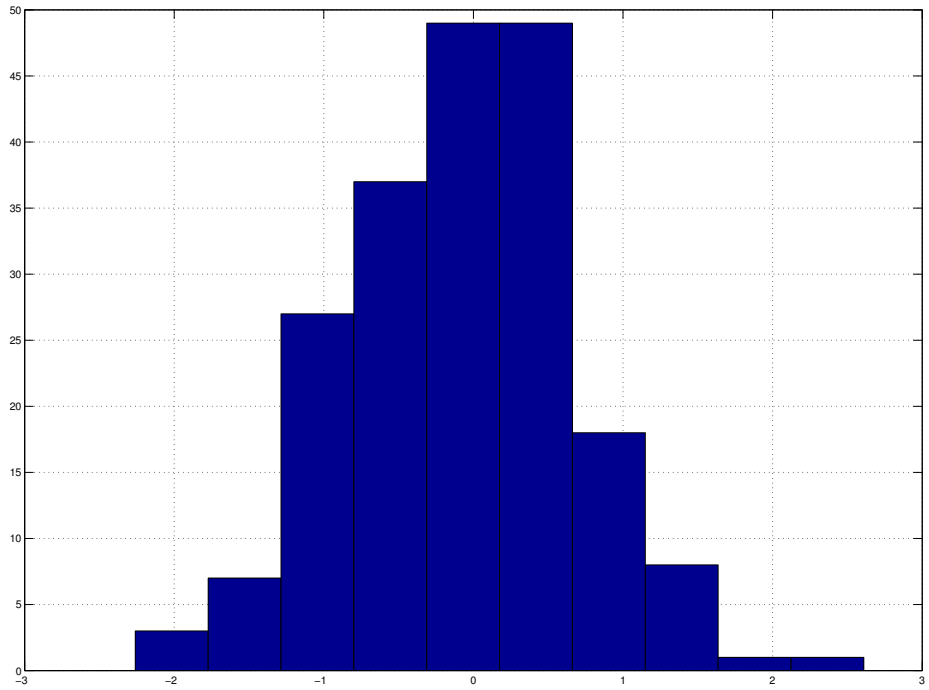

Figure 7.7: Histogram of phase error.

Post layout monte carlo simulation is done in phase error of divider. Standard deviation of phase error was $0.7°$. It can be reduced only by increasing device sizes thereby increasing power.

7.3 Power Consumption

Table 7.1: Summary.

Design	Total current
Programmable divider	$150\,\mu A$
I/Q Divider	$350\,\mu A$
3 buffers	$400\,\mu A$
Total	$900\,\mu A$

Total power consumption including buffers is $1080\,\mu\mathrm{W}$, this is considering typical corners.There is variation of power across corners with worst case in FF corner. Variation of total current of I/Q divider and Programmable divider across all process corners are shown below

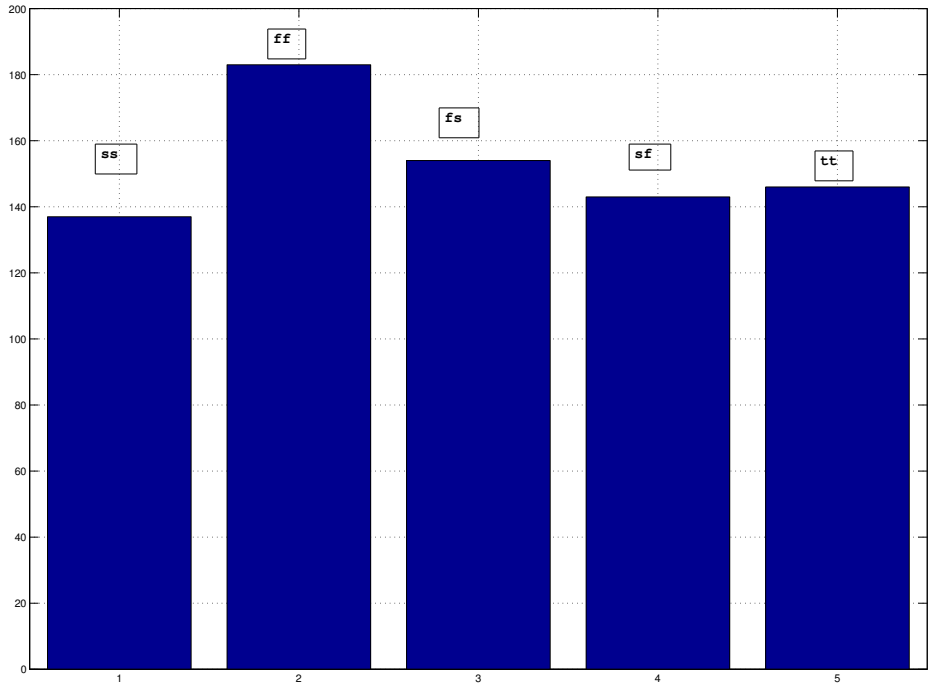

Figure 7.8: Variation of total current of programmable divider across corners.

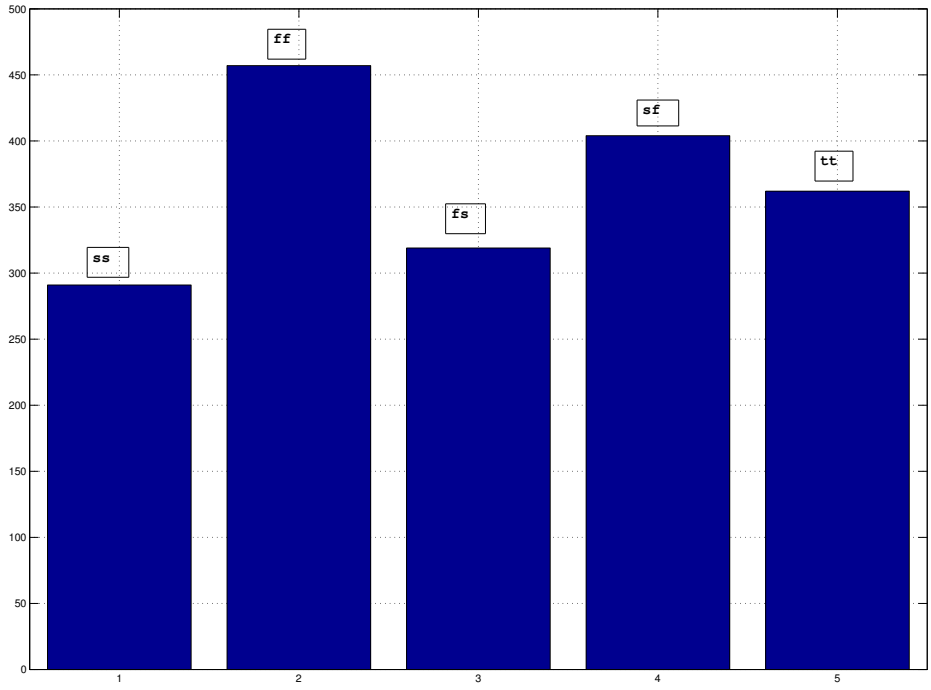

Figure 7.9: Variation of total current of I/Q divider across corners.

FF corner shows highest power consumption in each case.

CHAPTER 8

CONCLUSION

A low power programmable feedback divider and an output 1:2 divider for generation of quadrature carriers were presented in this thesis. The division range of designed programmable divider is from 224 to 255 covering required Bluetooth frequency range with an average power consumption of $180\,\mu W$. Phase error of output I/Q divder is 0.1° considering all process corners and temperature variations with an average power consumption of $420\,\mu W$.

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